To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

RENESAS

Design Manual

PFESiP®
(Platform for Embedded System in a Package)

EP-1 Series

Ver.2.0

MC-10501
MC-10502
MC-10503
MC-10505
MC-10506
MC-10507

Document No. A19068EJ2V0DM00 (2nd edition)
Data published June 2009 NS

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

These commodities, technology or software, must be exported in accordance with the export administration regulations of the exporting country. Diversion contrary to the law of that country is prohibited.

- **The information in this document is current as of June, 2009. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. In addition, NEC Electronics products are not taken measures to prevent radioactive rays in the product design. When customers use NEC Electronics products with their products, customers shall, on their own responsibility, incorporate sufficient safety measures such as redundancy, fire-containment and anti-failure features to their products in order to avoid risks of the damages to property (including public or social property) or injury (including death) to persons, as the result of defects of NEC Electronics products.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".
  The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)
(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).

M8E0904E

Major Revisions in This Edition

Location	Contents
p.62	Modification of **3.4.1 (7) Mode setting pin**
p.62	Modification of **3.4.1 (8) Providing the files for pin placement evaluation**
p.80	Modification of **Table 4-7. Recommended Operating Range**
p.179	Addition of **6.11 Output Waveform Noise**
p.180	Addition of **6.12 Reset Pin**
p.182	Addition of description of **7.1.1 Pins for connections between PFESiP/V850EP1 and gate array (memory interface for SiP internal connection, DMA signal)**
p.185	Modification of **Figure 7-4. Test Register That Can Be Read- or Write-Accessed from PFESiP/V850EP1**
p.186	Addition of **Figure 7-5. Example of the Connections Between the PFESiP/V850EP1 and Gate Array**
p.187	Modification of **7.3.1 Boundary-Scan test (NEC_BSCAN) application**
p.187	Modification of **Figure 7-6. Boundary-Scan Test (NEC_BSCAN)**
p.214	Modification of **Table 9-2. Recommended Oscillation Frequency Range and Configuration**
p.217	Modification of **Figure 9-4. Oscillator Configuration**
p.218	Addition of **9.4.3 Notes on oscillator block (OSBx)**
p.267	Addition of **9.7.1 (2) (a) Calculating the modulation frequency**
pp.267,268	Addition of **9.7.1 (2) (b) Calculating various frequencies**
pp.272 to 297	Addition of **9.8 Analog PLL**
pp.298 to 302	Addition of **9.9 Power on Reset**
pp.321 to 345	Addition of **CHAPTER 11 PACKAGES**
p.374	Addition of **E.1.6 High Speed Signal Transmission**
p.375	Addition of **E.1.9 Analog PLL**
p.375	Addition of **E.1.10 Power on Reset**

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

To obtain the latest documents when designing, contact an NEC sales office or a distributor.

PREFACE

Readers This manual is intended for users who wish to evaluate developing PFESiP EP-1 Series products that use the microcontroller function chip with an on-chip V850E2 CPU core (PFESiP/V850EP1) and an NEC Electronics CMOS embedded array EA-9HD Series chip.

Purpose This manual summarizes various restrictions and cautions for designing LSI chips, by understanding the functions of the PFESiP/V850EP1 and using an EA-9HD Series microcontroller. Furthermore, various restrictions and cautions regarding the section where the PFESiP/V850EP1 and EA-9HD Series microcontroller are connected, which are unique to the PFESiP EP-1 Series, are also stated. Make sure to thoroughly read this manual and follow the items (general items, cautions, and restrictions) stated in this manual, in order to smoothly design the LSI chips. If the items are not followed, the quality and performance of the LSI products may degrade and malfunctioning may occur.

How to Read This Manual It is assumed that readers of this manual have general knowledge of electricity, logic circuits, microcontrollers, SRAM, Page ROM and SDRAM.

Conventions

Data significance: Higher digits on the left and lower digits on the right		
Active low representation:	xxxZ (Add Z after pin or signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numeric representation:	Binary .....XXXX or XXXXB	
	Decimal XXXX	
	Hexadecimal ...XXXXH	
Prefix indicating power of 2		
(Address space, memory capacity):	K (kilo):	$2^{10} = 1,024$
	M (mega):	$2^{20} = 1,024^2$
	G (giga):	$2^{30} = 1,024^3$
Data type:	Word	... 32 bits
	Halfword	... 16 bits
	Byte	... 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to PFESiP EP-1 Series

Document Name	Document No.
V850E2 Architecture User's Manual	U17135E
PFESiP EP-1 Series Design Manual	This manual
PFESiP/V850EP1 Product Data User's Manual	A19069E
PFESiP/V850EP1 Hardware (CPU Function) User's Manual	A19070E
PFESiP/V850EP1 Hardware (USB Function) User's Manual	A19071E
PFESiP/V850EP1 USB Function Sample Software Application Note	A19349E

Documents related to PFESiP EP-1 Evaluation Board

Document Name	Document No.
PFESiP EP-1 Evaluation Board Technical Information User's Manual	A19350E
PFESiP EP-1 Evaluation Board Lite Technical Information User's Manual	A19354E

Documents related to development tools

Document Name			Document No.
RX850 Pro User's Manual	Ver.3.21	Basics	U18165E
	Ver.3.20	Installation	U17421E
	Ver.3.21	Technical	U18164E
	Ver.3.20	Task Debugger	U17422E

Documents related to EA-9HD Series

Document Name	Document No.
EA-9HD Series Design Manual	A13282E
EA-9HD Series Memory Macro Design Manual	A13367E
CMOS-9HD Series, EA-9HD Series Mega Macro Design Manual	A13941E
CMOS-9HD Series, EA-9HD Series Block Library	A13052E

Documents related to OPENCAD

Document Name	Document No.
OPENCAD™ OPENCAD Release Note User's Manual	A15049J
OPENCAD OPC_VSHELL User's Manual	A15050E
OPENCAD Static Timing Analyzer Tiara User's Manual	A15056J
Design for Test TESTACT, NEC_SCAN2 User's Manual	A15059E
Design for Test DFT Compiler/TetraMAX User's Manual	A14964E
Design for Test NEC_BIST, NEC_TESTBUS, NEC_SCAN/SCAN2, NEC_BSCAN/BSCAN2 User's Manual	A15168E

CONTENTS

LIST OF FIGURE (1/4)

LIST OF FIGURE (2/4)

LIST OF FIGURE (3/4)

LIST OF FIGURE (4/4)

LIST OF TABLE (1/2)

LIST OF TABLE (2/2)

CHAPTER 1 INTRODUCTION

1.1 Features

PFESiP (platform for embedded system in a package) is a new ASIC solution that quickly, cost-effectively, and safely provides customized LSIs with expanded functions, by developing a gate array and a general-purpose function chip into an SiP (system in a package), performing advance verification, and providing the SiP as a master device.

The EP (embedded processor) -1 Series are quickly, cost-effectively, and safely customizable microcontrollers, for which a microcontroller is applied to a general-purpose function chip and a dedicated microcontroller and gate array master suitable for SiP development are provided and integrated into a single package (see Figure 1-1), as part of the PFESiP product series.

An SiP-suited I/O pad layout is used, sharing of packages is sought, and innovations regarding cost reduction, test simplification, and noise control have been made. In contrast to a configuration in which a microcontroller and a gate array are used separately, the number of components, the mounting area, and the unit price can be reduced. There are functional limitations in contrast to an SOC, but if the specifications match, the development cost and development period can be reduced (see Figure 1-2).

Figure 1-1. Concept of PFESiP

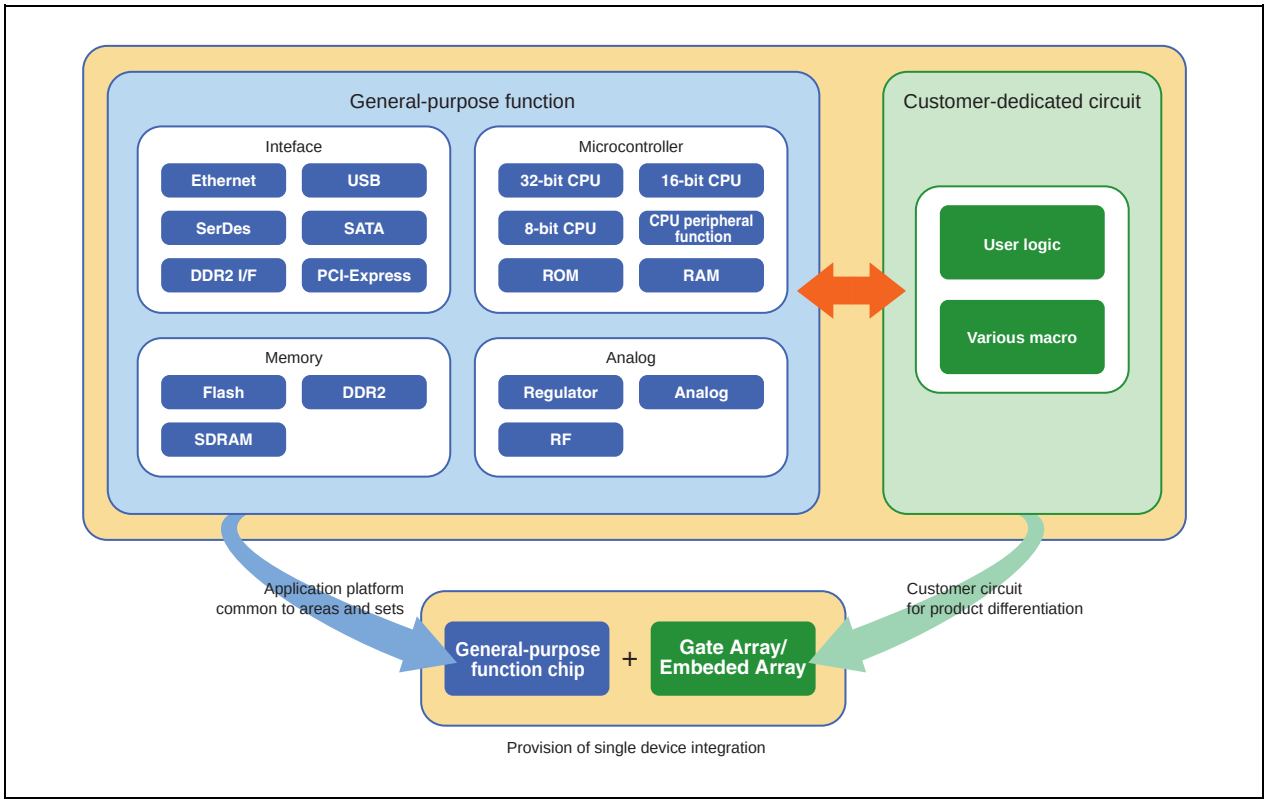
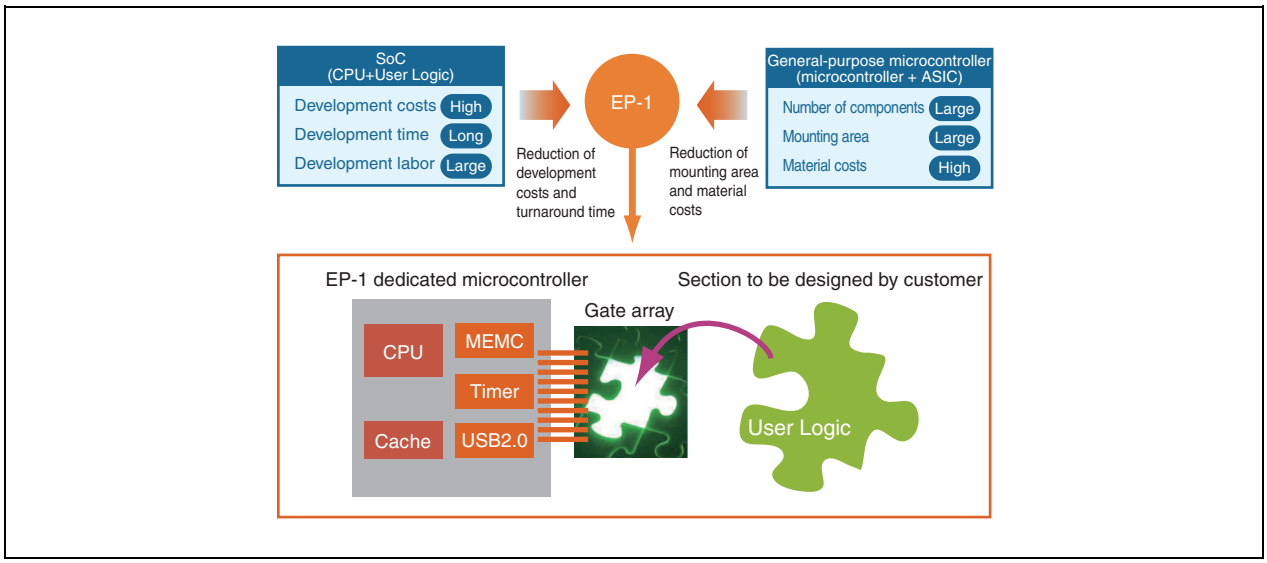


Figure 1-2. EP-1 Series Solves System Development Problems



1.2 EP-1 Series Product Lineup

The EP-1 dedicated microcontroller PFESiP/V850EP1 employs a high-end 32-bit RISC CPU core (V850E2 (NBA85E2S) core). Tables 1-1 and 1-2 show 16-bit and 32-bit versions of external busses for which the number of gates that can be used vary. Each version provides three master devices, thus providing a total of six master devices.

Table 1-1. Product Lineup (External Bus: 16-bit version)

Master	Package				Number of Usable Pins (Gate array)
	Gate array (Available Gate count)	PBGA	FPBGA		
		464 pins (25 × 30 mm)	452 pins (22 × 22 mm)	433 pins (17 × 17 mm)	
		1.00 mm ball pitch	0.80 mm ball pitch	0.65 mm ball pitch	
MC-10501	80 K	○	No development plan	No development plan	80
MC-10502	160 K	○	○	To be planned	80
MC-10503	240 K	○	○	No development plan	80

Table 1-2. Product Lineup (External Bus: 32 bit version)

Master	Package		Number of Usable Pins (Gate array)
	Gate array (Available Gate count)	PBGA	
		550 pins (25 × 30 mm)	
		1.00 mm ball pitch	
MC-10505	80 K	○	80
MC-10506	160 K	○	120
MC-10507	240 K	○	120

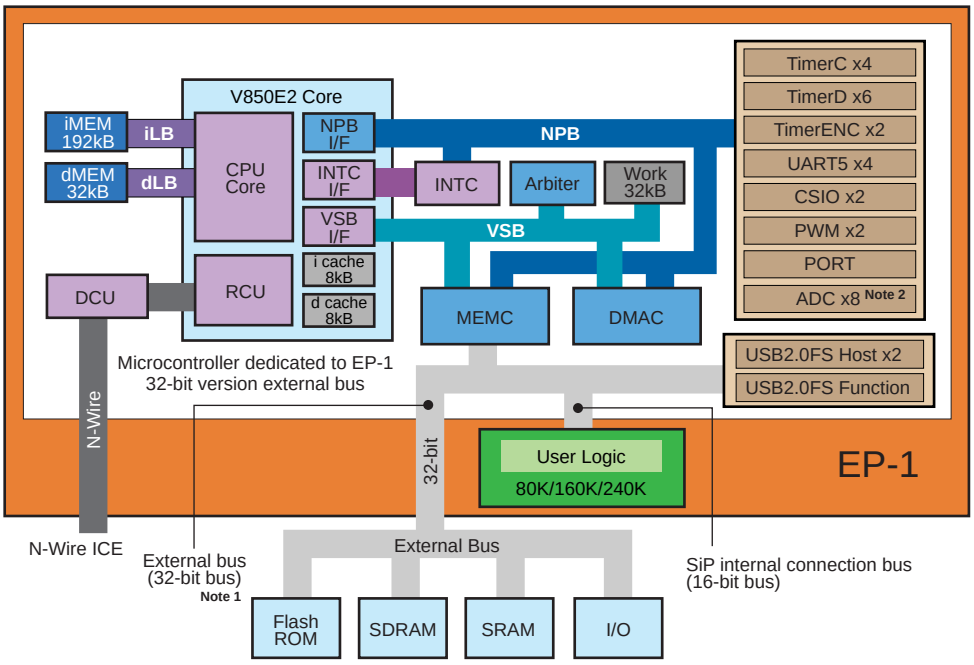
1.3 EP-1 Series Configuration

Within a PFESiP/V850EP1, a PFESiP and a user logic are connected via a memory bus, as shown below.

An EP-1 Series LSI is configured of an EP-1 dedicated microcontroller (PFESiP/V850EP1) and a gate array that can form a logic circuit.

Within the EP-1 Series LSI, the PFESiP/V850EP1 and gate array are connected via a memory bus, as shown below.

Figure 1-3. EP-1 Series Configuration



Notes 1. The 16-bit and 32-bit external buses are provided.

2. Only 32-bit external bus is available for ADC function.

For the chip configuration of the EP-1 dedicated microcontroller PFESiP/V850EP1, see **CHAPTER 2 PFESiP/V850EP1 OVERVIEW**.

1.3.1 Features of gate array

The EP-1 Series gate array is a high-density and high-speed embedded array (EA-9HD Series) that uses 3/4 layer wiring employing a 0.35 μm CMOS process and has a channel-less architecture (SOG).

It can be mounted with various highly-functional cores and capacity cells for EMI noise reduction, and EMI noise can be further reduced using it in combination with an SSCG (spread-spectrum clock generator) macro.

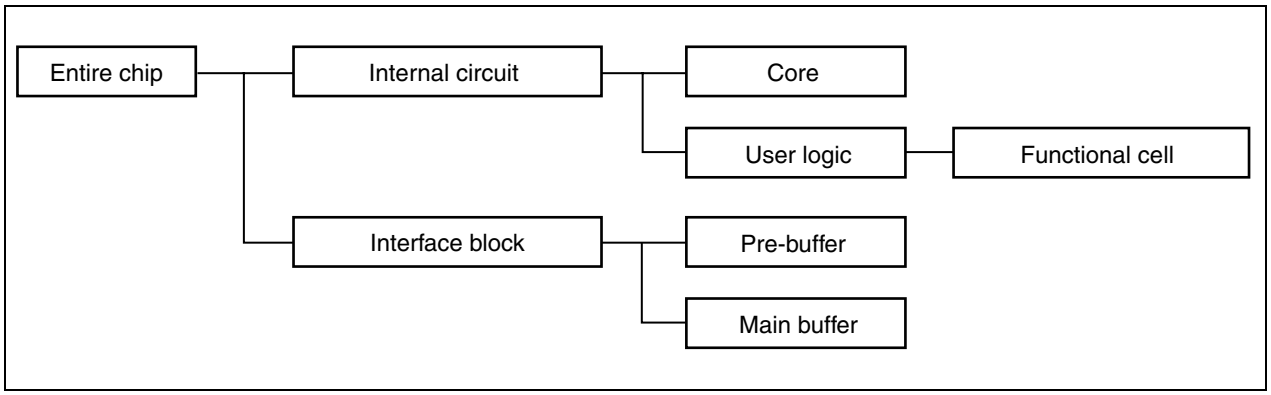
The following table lists the EA-9HD Series features.

Process:	0.35 μm process Si gates, 3-layer metal wiring, 4-layer metal wiring
Input interface:	LVTTL compatible
Internal blocks:	More than 190 types of function blocks Includes high-speed low power; compatible with CMOS-8L Series Scan path block Driver for clock tree synthesis
Variety of macros:	Serial interface (μPD71051) Timer/counter (μPD71054) Interrupt controller (μPD71059) UART + FIFO (PC16550D) Cell-based IC-type memory (For CB-9 Series) Gate array type memory (For CMOS-9HD Series)
Variety of peripheral blocks:	LVTTL input/5 V tolerant input buffer LVTTL input buffer with fail-safe function 5 V tolerant output buffer for CMOS TTL 5 V tolerant output buffer 5 V full-swing buffer LVTTL output buffer Buffer for PCI bus specification High drive capability buffer (I_{OL} = 24.0 mA) Low-noise output buffer Buffer with internal pull-up resistor (5 kΩ/50 kΩ) Buffer with internal pull-down resistor (50 kΩ) Clock driver dedicated input block Digital PLL (for phase control) Digital PLL (for multiplication) GTL+
Power consumption:	0.16 μW/MHz/cell (internal gate, operating factor: 0.3)
Power supply voltage:	3.3 ±0.3 V / 5.0 ±0.5 V
Operating frequency:	75 MHz

1.3.2 Gate array chip configuration

Gate array generally include the following elements.

Figure 1-4. Gate array chip configuration



The meanings of these elements are described below.

Elements	Description
Core	A function block and memory macro that includes a large number of gates, such as a CPU core or peripheral macro (megamacro) There are cell-based IC type macros and gate array type macros.
User logic	Circuits created by the user using functional cells
Functional cell	A cell that contains basic functions such as OR, AND, and flip-flop
Interface block	A block used as an interface for external pins
Prebuffer	A buffer that is used to control the main buffer and that includes an interface block
Main buffer	A buffer that is used as an interface for external devices and that includes an interface block
On-chip circuits	All circuits other than the interface block

Remark The interface block is a general term that refers to the input buffer, output buffer, and bidirectional buffer.

1.3.3 Transistor configuration of gate array

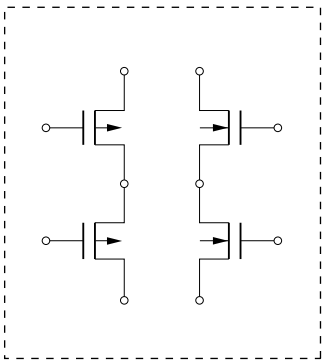
Figure 1-5 represents the gate array internal cell equivalent circuit.

Each cell of the gate array can be configured as a device such as a two-input NAND/NOR gate, an inverter, or a buffer.

A CMOS circuit consists of a P-channel MOS transistor (P-ch.Tr) and an N-channel MOS transistor (N-ch.Tr).

Normally, either the P-ch.Tr or the N-ch.Tr is in the OFF state.

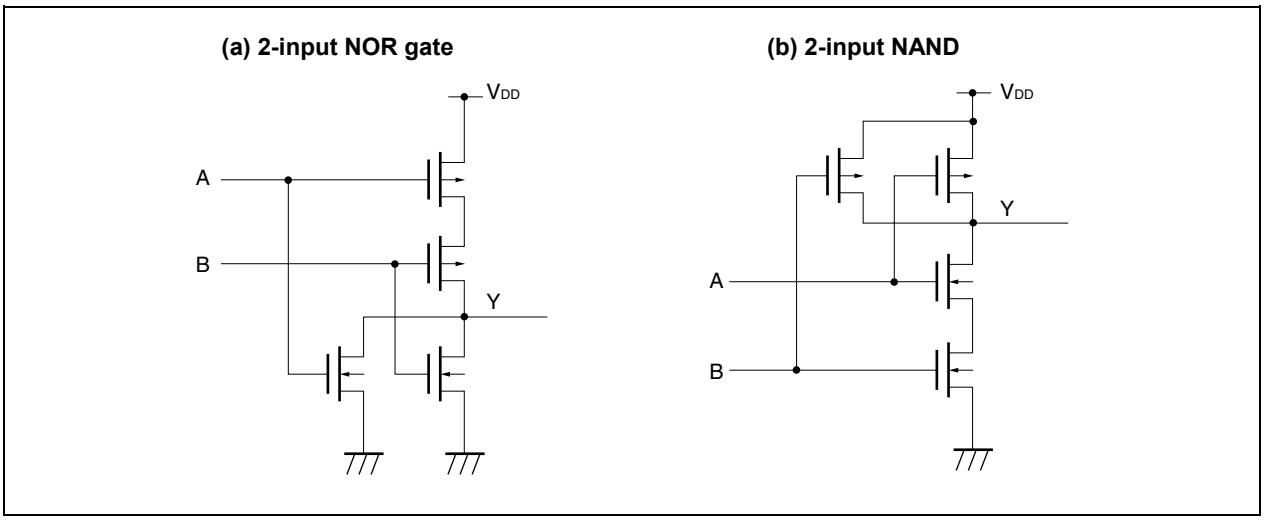
Figure 1-5. Internal Cell Equivalent Circuit



Because virtually no power flows in the steady state, power consumption for a CMOS circuit is extremely low. A CMOS circuit consumes current mostly during switching. Because a high transient current flows during switching, a highspeed capacitor with a high capacitance must be inserted between the power supply and ground, or the impedance of the power supply lowered. In addition, if a waveform with a slow rise/fall time is applied to a CMOS circuit, both the P-ch.Tr and N-ch.Tr will remain in the ON state for a period of time, causing a through current to flow between the P-ch.Tr and N-ch.Tr. Consequently, the current consumption increases, and may cause malfunctioning.

Figure 1-6 (a) and (b) show the equivalent circuits of a 2-input NOR gate and a 2-input NAND gate. Because the ON resistance of the N-ch.Tr is about fifty percent less than that of the P-ch.Tr, a large current can be sent through the N-ch.Tr. Therefore, as shown in Figure 1-6 (a), the ON resistance of the output rise side at the NOR gate, which is serially connected to the P-ch.Tr, becomes larger, and the drive capability of the load drops. In CMOS embedded arrays, the NOR fan-out drive is slower than the NAND fan-out drive. Because of this, the NAND blocks should be used as much as possible to increase the speed and stability of the circuit. For the same reason, complex gates that serially connect many transistors tend to be slow, and therefore should not be used in high-speed circuits. Complex gates should be used when speed is not as important to improve cell utilization.

Figure 1-6. Equivalent Circuit



1.3.4 3.3 V and 5 V I/O interface

With the EA-9HD Series that uses a type of 0.35 μm transistor processing technology, the standard power supply voltage that configures the gate array block is assumed to be 3.3 V. Even in the case of embedded arrays, the EA-9HD Series, which uses transistor processing technology that employs a 0.35 μ m process, features a standard power supply voltage of 3.3 V. Therefore, the EA-9HD Series is provided with an interface block capable of connection with conventional 5 V LSIs.

Because the LVTTL input block of the EA-9HD Series inputs 3.3 V signals, it cannot receive 5 V signals. The 5 V signals are received by a 5 V tolerant input block. Assuming that the power supply voltage of future embedded array peripheral circuits will be 3.3 V, this 5 V tolerant input block can also receive 3.3 V signals. In addition, the LVTTL input block is also available with a fail-safe function that can be used for hot insertion and removal.

For output buffers, the high output level of the LVTTL output block is the same as for the conventional embedded array V_{DD}. In addition, a 5 V tolerant output block is also available. The 5 V tolerant output block differs from the conventional one in that it can pull up a pin at 5 V, which is higher than the LSI power supply voltage. It therefore becomes possible to connect the pin to a 5 V bus line.

A 5 V full-swing buffer can also be optionally used with an EP-1 Series microcontroller. 5 V input and output can be realized by separately providing a 5 V power supply. Unlike in the case of a 5 V tolerant output block, no external pull-up is required, thereby reducing the number of external parts as well as the static power consumption. While a 5 V power supply is separately provided, the internal power supply voltage is 3.3 V. In cases when using 5 V full-swing buffer, note with caution that there is some buffer placemnet restriction. For details, refer to **CHAPTER 10 CAUTIONS ON USE OF 5 V FULL-SWING BUFFER**.

Refer to **9.1 LVTTL and 5 V Tolerant Blocks, 5 V full-swing buffer** for details of each block.

1.3.5 Selection of memory

Cell-based IC-type and gate array type memory macros can be used in the gate array.

These two types have the features shown below, so when selecting then, users should be advised to select the type that best fits their circuit characteristics.

Type	Advantages	Disadvantages
Cell-based IC-type memory	• Size is small • Speed is high • Bit/word freedom is high.	• After the base is made, the changes are impossible.
Gate array type memory	• It is possible to change the size if it is possible to lay it out after the base is made.	• Size is large • Speed is low • The bit/word combination is fixed.

Type			Size Range
Cell-based IC-type	High-speed RAM	1-port/synchronous	1 to 32 bits, 32 to 2K words (Variable in 1-bit/8-word units)
		2-ports/synchronous (RW + R)	1 to 32 bits, 32 to 2K words (Variable in 1-bit/16-word units)
	High-density RAM	1-port/synchronous	1 to 32 bits, 16 to 2K words (Variable in 1-bit/16-word units)
		2-port/synchronous (W + R)	1 to 32 bits, 32 to 1K words (Variable in 1-bit/8-word units)
Gate array type	High-density RAM	1-port/asynchronous	Bit/word fixed. See **Table 3-4** for combinations.
		2-port/asynchronous (W + R)	Bit/word fixed. See **Table 3-4** for combinations.

1.4 EP-1 Series Package

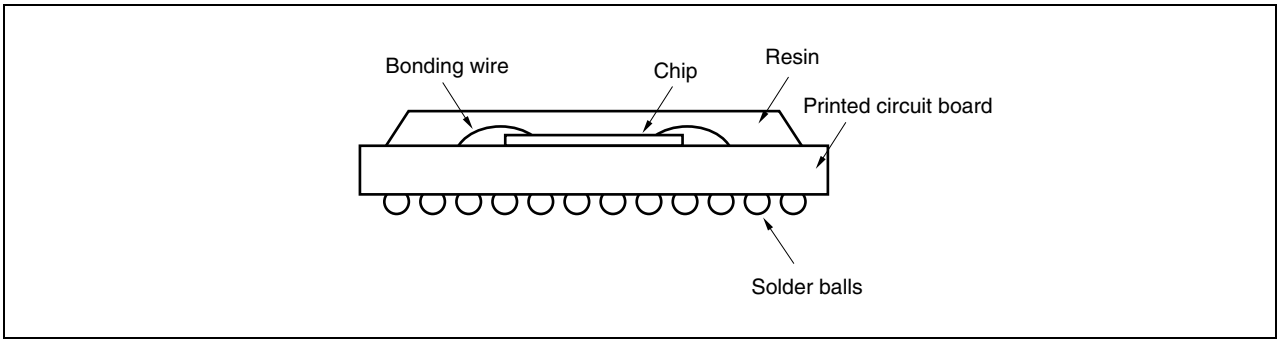
BGA that is adopted in EP-1 series is a multi-pin package for LSI.

It is one type of surface mount package, with balls of solder lined up on the back of a printed circuit board and used in place of leads. The LSI chip is mounted on the surface of the printed circuit board and sealed with mold resin or potting.

The EP-1 Series is configured of a PBGA that uses glass-epoxy-type plastic resin for the printed wiring board.

Figures 1-7 shows the cross-sectional view of a PBGA.

Figure 1-7. Cross-sectional View of a PBGA



1.5 Development Flow

The EP-1 Series uses a gate array to perform unique functions to be used in combination with a microcontroller. Figure 1-8 shows the entire development flow.
First, system specifications, such as whether the specifications of microcontroller chips that can be incorporated suit the system specifications, whether any functions are lacking, and whether the lacking functions can be performed by hardware or software, are evaluated.

In development of the EP-1 Series, the EP-1 Series development evaluation board of a prototyping environment is used.

The EP-1 Series development evaluation board is equipped with a microcontroller chip to be mounted on the EP-1 Series. Consequently, it can also be used to evaluate the system specifications when initiating development. The functions to be performed by a gate array are evaluated by implementing them on the FPGA (field programmable gate array) on the development board. Hardware debugging can be performed in advance for the development board, as a prototype of the EP-1 Series. Furthermore, the development board can also be used for advance software development and prior system evaluation.

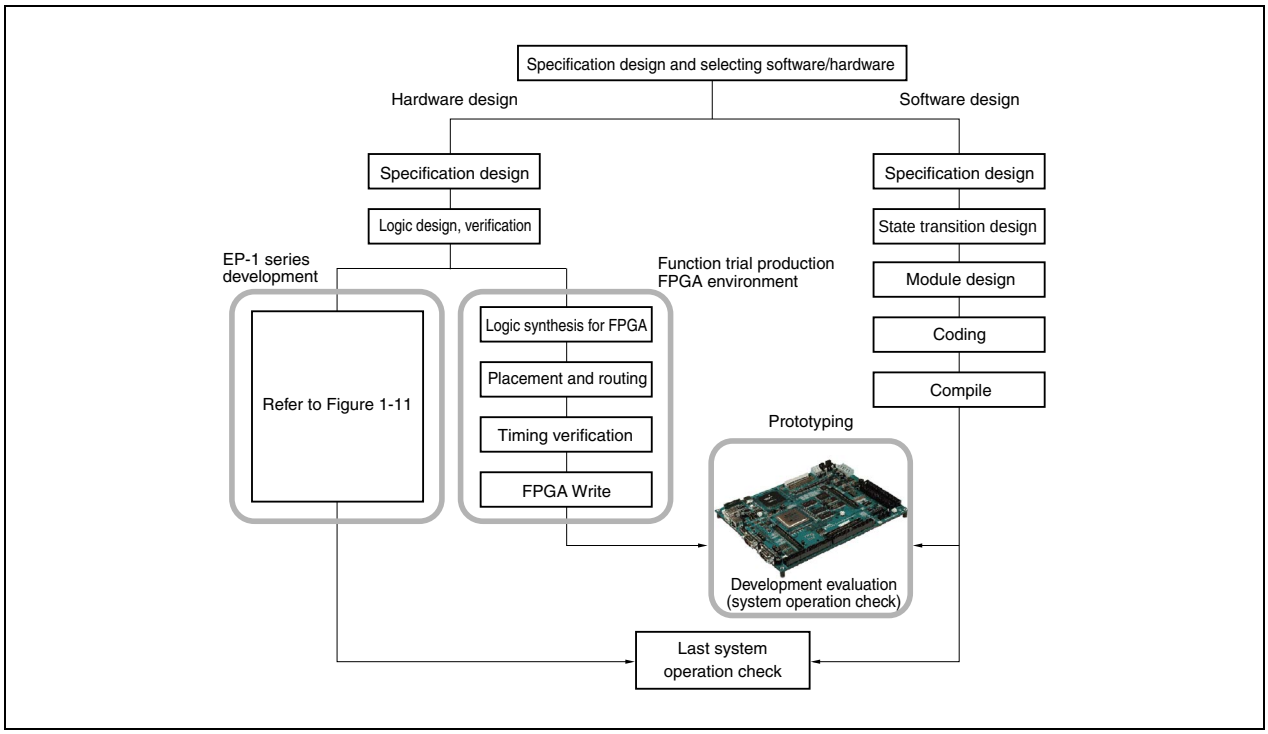
The development evaluation board can be used to implement a major part of function designing and verification in advance, based on the specifications and system design. The design, however, must be corrected in accordance with the circuit design rules specific to gate arrays as well as the design rules taking the internal specific connections to SiPs into account.

In gate array development, physical aspects must also be evaluated. In consideration of the constraints as an SiP, the gate array master device and package are selected and pin layout is performed in accordance with the specifications such as circuit size, power consumption, and the required number of pins. The subsequent design flow is identical to that of a normal gate array.

When gate array designing has been completed, gate arrays are manufactured, developed into SiPs together with dedicated microcontrollers, passed through selection tests and examinations, and finally shipped. In a standard case, an engineering sample (ES) can be produced in about 30 days after gate array manufacturing has been started.

Development is completed upon confirmation by a device manufacturer that there are no problems in system evaluation using the engineering sample.

Figure 1-8. EP-1 Series Development Flow



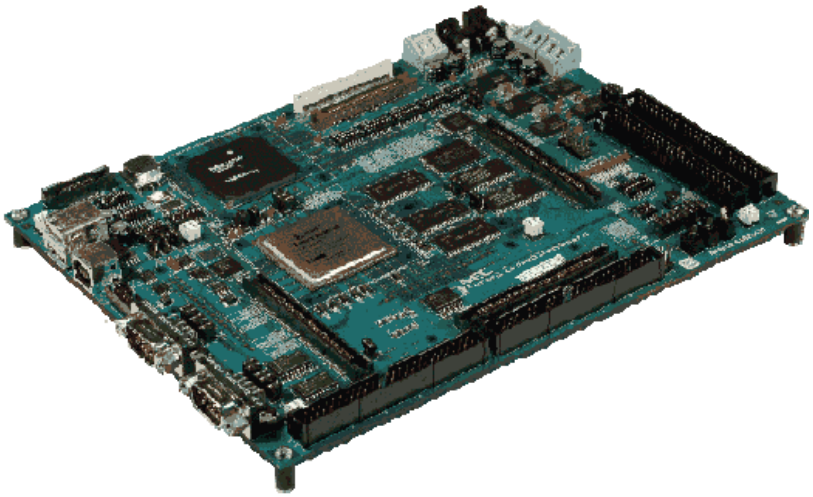
1.5.1 Prototyping environment

The EP-1 Series development evaluation board is directly mounted with the microcontroller chip to be mounted on the EP-1 Series (see Figure 1-9 (a) and (b)). Not only can it be used for developing the actual EP-1 Series, it can also be used to check the performance such as whether a conventional microcontroller and gate array can be replaced by an FPGA, or evaluate trade-off between software and hardware. Two types of development evaluation boards, a standard development evaluation board (for users performing full-scale prototyping) and a compact development evaluation board (for users evaluating the introduction of an EP-1 Series microcontroller) are provided.

Figure 1-10 (a) and (b) shows a block diagram of the board. The gate array functions that form pairs with the microcontroller chip in the SiP are configured by the FPGA on the board. Devices, such as SDRAMs, a flash memory, and an SRAM, which are required for general systems, are also mounted on the board. A more systematic evaluation can be performed by connecting the functions required by device manufacturer systems and the board via the system expansion connector.

Figure 1-9. EP-1 Series Development Evaluation Board

(a) EP-1 Series Evaluation Board (Substrate size: 168 × 220 mm)



(b) EP-1 Series Evaluation Board Lite (Substrate size: 105 × 130 mm)

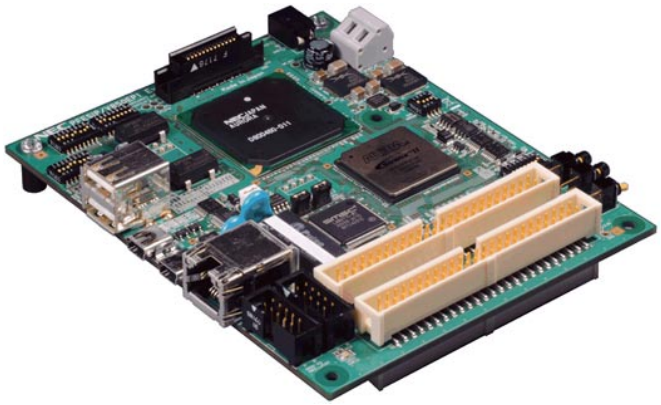
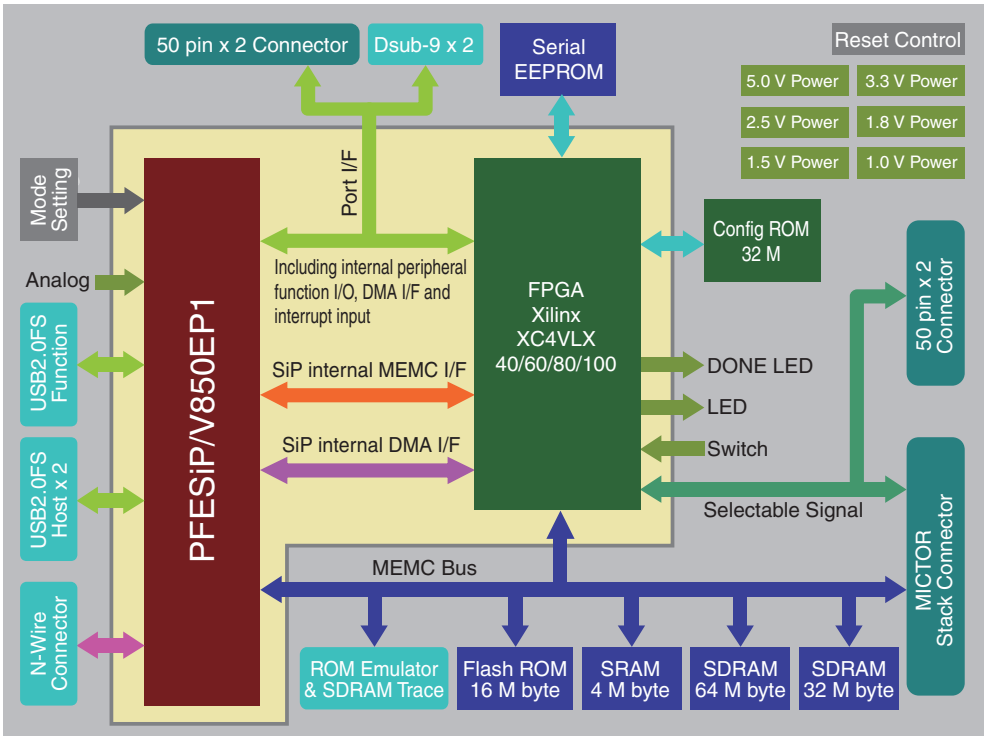
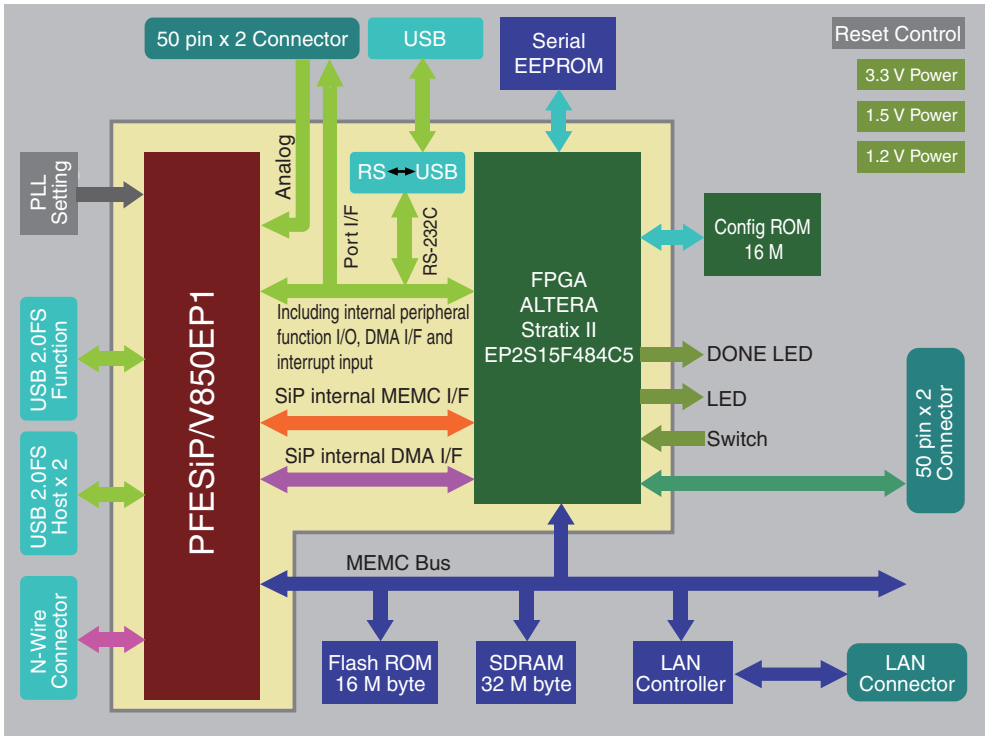


Figure 1-10. EP-1 Series Development Emulation Board (Block Diagram)

(a) EP-1 Series Evaluation Board



(b) EP-1 Series Evaluation Board Lite



1.5.2 Software development flow

To develop software by using the EP-1 Series, use PFESiP/V850EP1 evaluation chips to create an emulation board.

NEC Electronics provides PFESiP/V850EP1 evaluation boards that are mounted with PFESiP/V850EP1s.

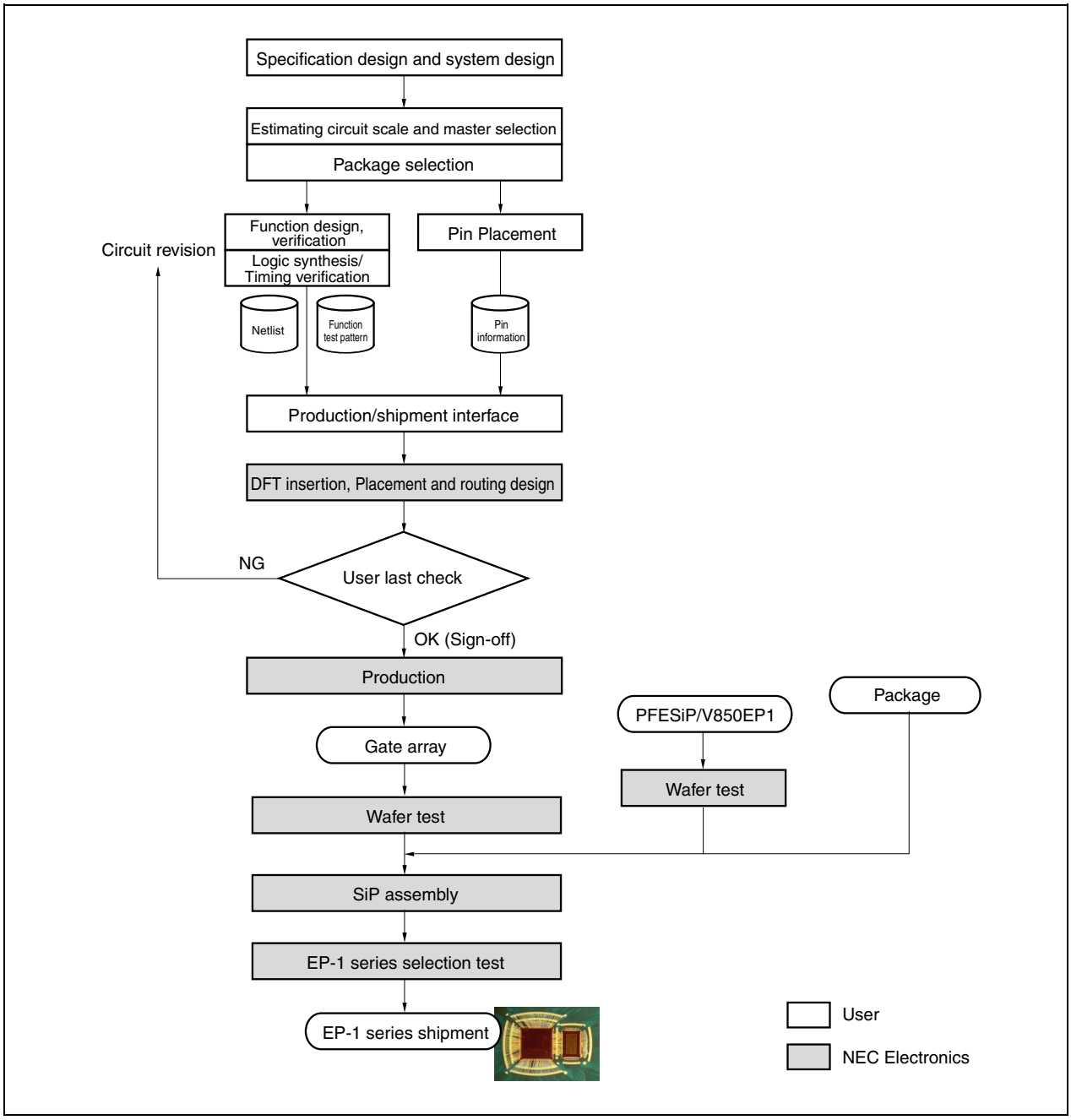
Contact NEC Electronics for details of the PFESiP/V850EP1 evaluation board.

1.5.3 Gate array development flow

This section shows the gate array development flow (overview). For details, see **3.6 Gate Array Development Flow**.

Figure 1-11 shows the flow from gate array development until SiP manufacturing and shipping.

Figure 1-11. Gate Array Development Flow (Outline)



(1) Specification design and system design

Design the specifications for efficiently creating the required functions at low cost.

The specification design and system design of the blocks to be configured by the gate array are almost completed in processes of specification design, system design, and prototyping as an SiP.

Here, re-evaluate and correct the specifications in consideration of the design constraints specific to gate arrays. Evaluate the internal circuit data flow, clocks, and interfaces and estimate the memory macros.

(2) Circuit size estimation and master selection

The EP-1 Series is provided with 16-bit and 32-bit external buses. The master can be selected from a total of six masters, including three masters which have different numbers of gates that can be used for the gate array block.

See **1.2 EP-1 Series Product Lineup** for details.

(3) Power consumption estimation and package selection

Five types of PBGA (plastic ball grid array) packages can be used with the EP-1 Series.

To select a package in accordance with the required specifications, estimate power consumption and the number of pins used, because the number of pins than can be used and thermal capacity differ for each package. See **1.2 EP-1 Series Product Lineup** for details.

(4) Pin layout

The pin layout of the EP-1 Series determines the pins to be used for the gate array.

The layout of microcontroller pins, power supply pins, and unused pins is predetermined.

(5) Function design and verification

Design the circuit in compliance with the design rules of the EA-9HD Series which is the gate array master.

Design and verify via function modeling using general HDL descriptions.

When prototyping has been performed with an FPGA, the HDL codes must be rewritten in order to comply with the EA-9HD Series design rules and to replace I/Os and macros. (A conversion tool is also provided.)

Use a memory compiler when a RAM or a ROM is required in the circuit. A required RAM or ROM library can be easily created by specifying the bit width and number of words.

SiP internal connection signals are restricted by constraints related to the circuit configuration.

(6) Logic synthesis/timing verification

Convert the circuit that has been described in HDL into a gate-level netlist via logic synthesis.

The circuit size and operating frequency must be optimized, because they vary depending on the conditions of logic synthesis.

The SiP internal connection signals are to be designed in accordance with the microcontroller specifications.

Describe these characteristics to a synthesis script and apply them as timing constraints.

Perform timing verification in accordance with the AC characteristics of the microcontroller after synthesis.

Finally, perform formal verification at the RTL and a design rule check (DRC).

(7) Design data interface

Submit to NEC Electronics a verified netlist and pin information file, and a function test pattern of the designed gate array.

Test circuit insertion by a DFT (design for test) tool will be performed by NEC Electronics.

Afterward, placement and routing, and ATPG (test pattern generation) are performed, whereafter a path delay file (SDF), the test coverage result, and a list of undetected faults are fed back to the designer at the device manufacturer. When there are problems upon performing timing verification and checking the test coverage, based on this information, correct the circuit and go through the same flow again.

When all checking have been completed, the process will be signed off.

(8) From gate array manufacturing to SiP shipping

Electrically test the gate arrays that are in a silicon wafer state after having been manufactured (wafer test).
The gate array will be mounted on a single semiconductor package together with a tested dedicated microcontroller chip and encapsulated in resin after wire connection has been performed.
Perform an electrical test again after the gate array has been packaged (selection test).
Finally, the gate array will be shipped as the EP-1 Series after having passed examination processes, such as appearance examination.

1.6 Advance ordering of base wafer and rework due to revision of metalization wafer for EP-1 Series

In an EP-1 series, the user logic area has the same structure as a gate array. For that reason, by deciding the cores and the number of user logic gates in advance, the user can, during the time when the circuit is being designed, make recommendations up to the point just before placement and routing when the mask is being created (prediffusion is completed). This process is called advance ordering of the base wafer. Then after the simulation is ended, placement and routing are implemented.

Through this system, it is possible to further shorten the delivery period until the ES (Engineering Sample). However, it is necessary to meet the following conditions and arrange the following data in order to carry out advance ordering of the base wafer. Furthermore, when mounting a capacity cell as a countermeasure against EMI, note that the base wafer cannot be ordered in advance.

[Conditions for advance ordering of base wafer for EP-1 series]

(1) The following points should be decided.
  (a) The type of cell-based IC-type macro and the number used.
  (b) The type of package used and the number of pins.

(2) A forecast should be prepared through outline study of the following points.
  (a) Package allowable power consumption
  (b) Simultaneous operations
  (c) Critical path
  (d) The cell utilization rate of the user logic unit should not increase to the point where wiring is impossible.
  (e) The allocation positions of the I/O buffers should be determined (should not be changed).

(3) Approval for the base mask order should be obtained from the user.

[Data required for advance ordering of base wafer for EP-1 series]

(1) The information required in (1) above for the conditions for advance ordering of base wafer.

(2) A netlist that satisfies the following points (formats which can be interfaced at NEC Electronics: EDIF, PWC)
  (a) A netlist which includes the number of each block in (1) (a) in the above conditions for advance ordering of base wafer, and which will permit the embedded array design rule check program to end normally. Errors related to circuit information, however, are irrelevant.
  (b) The circuit scale at the time when the user logic unit is finalized, should have the increase kept to within 5%, judging from the scale of the netlist used for advance ordering of base wafer. The number of gates can increase only up to the number of logic circuits that can possibly be included in the base.

[Notes on advance order of base wafer and rework because of revision of metalization wafer for EP-1 series]

If an advance order for a base wafer is made or if only the metalization wafer must be reworked due to revisions, the pin positions cannot be changed. If pin positions must be changed, the base wafer must be revised. However, changing from the LVTTL buffer/5 V tolerant buffer to the FILL CELLNote is possible. Moreover, the driving capability can basically be changed if the LVTTL buffer is used and the type of the buffer is the same.

In other cases, contact NEC Electronics if it is necessary to change the pin positions.

CHAPTER 2 PFESiP/V850EP1 OVERVIEW

A PFESiP/V850EP1 is a microcontroller function chip that was developed on the assumption of SiP development and uses a V850E2 CPU core. The CPU core operates at 200 MHz (max.) and the internal bus at 100 MHz (max.). This CPU core incorporates an instruction cache and a data cache. Furthermore, it incorporates a DMA controller, an interrupt controller, general-purpose ports, timers, a serial interface, an A/D converter, a memory controller, a host controller supporting USB 2.0 FS (Full-Speed) and LS (Low-Speed), and a function controller supporting USB 2.0 FS (Full-Speed), as peripheral functions.

A ROM, a page ROM, or an SRAM, and an SDRAM can be connected as external memories.

A PFESiP/V850EP1 also incorporates an instruction RAM and a data RAM, and enables high-speed processing by executing an external program by transferring it to the instruction RAM.

In application evaluation of software, the internal debug controller unit (DCU) can be used to perform debugging by the N-Wire in-circuit emulator and downloading of programs.

Similar to a general-purpose microcontroller that incorporates a V850E CPU core, a PFESiP/V850EP1 can execute middleware such as JPEG, JBIG, MH/MR/MMR, and TCP/IP at high speeds. It is also provided with middleware that can perform processing such as voice recognition and voice synthesis, which, by combining them with the aforementioned middleware, can easily create a multi-media system.

Integrated development environments such as an optimization C compiler, a debugger, and an in-circuit emulator are also provided. For a detailed description of PFESiP/V850EP1s, see **PFESiP/V850EP1 Hardware (CPU Function) User's Manual (A19070E)**.

2.1 Functions

(1) V850E2 CPU core

In contrast to the V850E1 CPU, the V850E2 CPU has an expanded 7-stage pipeline and uses together a 128-bit fetch bus to achieve a high throughput.

It uses 2-byte length basic instructions and supports high-level languages by which it increases the object code efficiency with C compilers and achieves downsizing of program sizes.

Furthermore, the internal NBA85E2S CPU core of a PFESiP/V850EP1 incorporates an instruction cache and a data cache of 8 KB 4-way set associative configurations.

(2) WDREG001PDA [word] W [bit] C1 (preliminary)

A PFESiP/V850EP1 is provided with a function that remaps chip select signals that are output by the CPU and DMA controller, before it is connected to actual external memories. Enabling or disabling of the instruction or data cache can be set only in units of chip select signals that are output by the CPU; however, by using the remap function, multiple chip select signals can be assigned to a single SRAM or SDRAM, thus enabling composite placements of instruction cache enable areas, data cache disable areas, and data cache enable areas for a single SRAM or SDRAM. A high performance can be secured while reducing the number of external memories, by using this function.

(3) Internal high-capacity RAM

A PFESiP/V850EP1 incorporates three types of high-capacity RAMs for separate purposes.

RAM Type	Capacity	Function Name	Circuit Name	Fetch	Connection Bus
Instruction RAM	192 KB	Instruction RAM	iLB_RAM	available	iLB
Data RAM	32 KB	Data RAM	dLB_RAM	available	dLB
Work RAM	32 KB	Work RAM	VSB_RAM	available	VSB

(a) Instruction RAM (iLB_RAM)

An instruction RAM of 192 KB is mounted on an iLB bus. The iLB bus employs a wide 128-bit fetch bus and is accessed at latency = 3 by using a high-speed CPCLK. It can be used for application programs that require execution in real-time. It is used mainly for programs and fixed data.

(b) Data RAM (dLB_RAM)

A data RAM of 32 KB is mounted. It is a high-speed data RAM that is accessed in one CPCLK clock. It is used mainly for variable data and stacks.

(c) Work RAM (VSB_RAM)

A RAM of 32 KB is connected to the internal VSB bus which is a synchronous bus. In contrast to the instruction RAM connected by the iLB bus or the data RAM connected to the dLB bus, it requires 2 VBCLK clocks to be accessed, but it can be accessed faster than external memories.

The work RAM can be assigned to the CSZ2 area that is set by using the CSC0 register or it can be set not to use this function.

Furthermore, the work RAM can be used to execute programs and access data. Particularly, when the CPU is executing by using only the instruction RAM or data RAM, DMA transfer between an external memory and the work RAM can be processed in parallel.

(4) External bus interface for SiP internal connection and DMA interface

A PFESiP/V850EP1 is provided with an external bus interface dedicated to SiP internal connection and a DMA interface, which are independent from the external bus interface, as subsets of the external bus interface, and placed to facilitate the creation of SiP products. These interfaces promote the optimization of drive performance for SiP internal connection. Note that DMA flyby transfer cannot be performed between these interfaces and the external bus interface, because they are independent buses.

(5) USB2.0FS/LS

A PFESiP/V850EP1 incorporates a host controller supporting USB 2.0 FS/LS and a function controller supporting USB 2.0 FS.

(6) Bus control unit (BCU)

The bus control unit starts the required external bus cycles, based on a physical address obtained by the CPU. If there is no bus cycle start request from the CPU when it fetches instructions from an external memory area, it generates a prefetch address and prefetches an instruction code. The prefetched instruction code is retrieved to the instruction queue within the CPU.

The BCU controls the DRAM controller (DRAMC), page ROM controller (ROMC), and DMA controller (DMAC), and performs accessing of external memories and DMA transfer.

(a) SDRAM Controller

The SDRAM controller generates SDRASZ, SDCASZ, and DQM0 to DQM3 signals, and controls accessing to the SDRAM.

Furthermore, it is provided with a refresh function supporting CBR refresh cycles and a dynamic self refresh function by external input.

(b) Page ROM controller (ROMC)

The page ROM controller supports accessing of ROMs with a page access function.
It performs a comparison with the bus cycle immediately before and controls the wait between normal accessing (off-page) and page accessing (on-page). It supports page widths of 8 to 128 bytes.

(c) DMA controller (DMAC)

The DMA controller performs data transfer between memories and I/Os in place of the CPU.
The transfer types are flyby (1-cycle transfer) and 2-cycle transfer. The transfer modes are single transfer, single-step transfer (DXSTEP register setting), and block transfer.

(7) Interrupt controller (INTC)

The interrupt controller processes the internal peripheral I/O (NPB) and external hardware interrupt requests (NMI, INTPZ0 to INTPZ31). The priorities of these interrupt requests can be specified in eight levels and multiple processing control can be performed for the interrupt sources.

(8) Clock generator (CG)

The clock generator can supply a clock of any multiplication factor and any SSCG setting as the internal system clock (CPCLK), because an internal PLL macro setting pin is set as an external pin (use it within the AC specifications). A VSB bus clock (VBCLK) can be supplied by setting the CLKDV0 and CLKDV1 pins, and dividing (by 2, 3, or 4) the pipeline clock (CPCLK).
Connect an external resonator to the XT1 and XT2 pins as an input clock.

(9) Counter/timer

A PFESiP/V850EP1 incorporates four 16-bit timer/event counter channels, six 16-bit interval timer channels, and two 16-bit 2-phase encoder input up/down counter/timer channels. It can measure pulse intervals and frequencies, and output programmable pulses.

(10) Serial interface (SIO)

A PFESiP/V850EP1 incorporates four asynchronous serial interface (UART5) channels and two clock-synchronous serial interface (CSI0) channels for the serial interface.
Furthermore, it incorporates a USB host controller and a USB function controller.

(11) A/D converter (ADC)

The A/D converter is a high-speed high-resolution 10-bit A/D converter that has eight analog input pins. It converts signals by using a successive conversion method.

(12) PWM

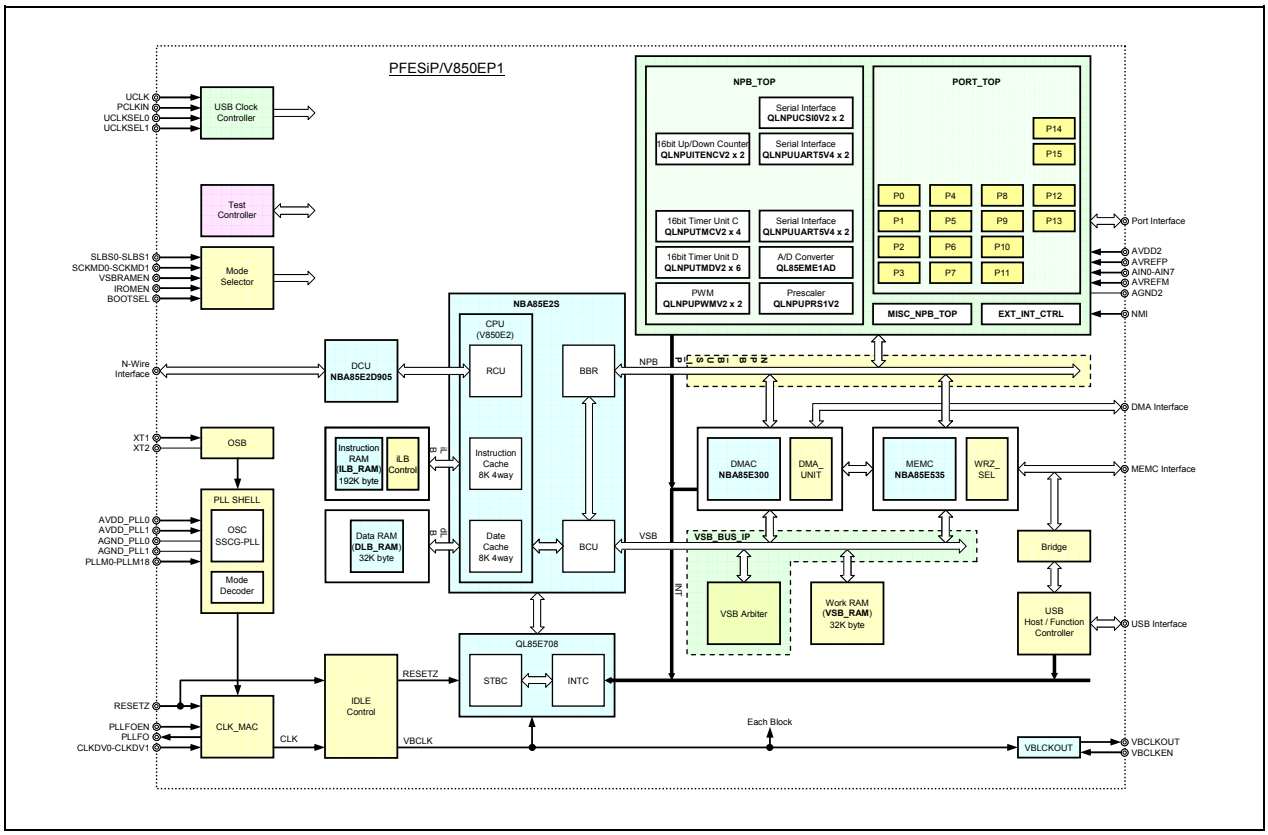
A PFESiP/V850EP1 is provided with two channels of PWM signal output with an 8-, 9-, 10-, or 12-bit resolution. The PWM output can be used as a digital-to-analog conversion output by connecting an external low-pass filter. It is optimal for actuator control signals of motors.

(13) Ports

The ports have functions which act as general-purpose ports and control pins, as shown below.

Port	I/O	Control Function
Port0(P00-P07)	8bit I/O	External interrupt input
Port1(P10-P17)	8bit I/O	External interrupt input
Port2(P20-P27)	8bit I/O	External interrupt input (SiP internal connection takes precedence)
Port3(P30-P37)	8bit I/O	Ansyncronous serial interface I/O
Port4(P40-P47)	8bit I/O	Timer CI/O
Port5(P50-P57)	8bit I/O	Timer C output, Timer ENC input
Port6(P60-P67)	8bit I/O	External address bus
Port7(P70-P77)	8bit I/O	External bus interface input (WAITZ), External bus interface output (chip select)
Port8(P80-P85)	6bit I/O	External bus interface I/O
Port9(P90-P97)	8bit I/O	External data bus
Port10(P100-P107)	8bit I/O	External data bus
Port11(P110-P116)	7bit I/O	Timer ENCI/O, Option N-Wire interface I/O, A/D conversion trigger input
Port12(P120-P127)	8bit I/O	DMA controller output (terminal count, acknowledgement)
Port13(P130-P133)	4bit I/O	DMA controller transfer request input
Port14(P140-P147)	8bit I/O	Clock synchronization serial interface, PWM output
Port15(P150-P157)	8bit I/O	External interrupt input

2.2 Internal Block Diagram



2.3 I/O Interface

P00 to P07	:Port 0
P10 to P17	:Port 1
P20 to P27	:Port 2
P30 to P37	:Port 3
P40 to P47	:Port 4
P50 to P57	:Port 5
P60 to P67	:Port 6
P70 to P77	:Port 7
P80 to P85	:Port 8
P90 to P97	:Port 9
P100 to P107	:Port 10
P110 to P116	:Port 11
P120 to P127	:Port 12
P130 to P133	:Port 13
P140 to P147	:Port 14
P150 to P157	:Port 15
TO0 to TO3	:TMC external pulse Outputs
TI0 to TI3	:TMC external clock Inputs
TCLR0 to TCLR3	:TMC clear request Inputs
ETIUD0 ,ETIUD1	:TMENC count pulse Inputs
ETCUD0 ,ETCUD1	:TMENC count pulse Inputs
ETCLR0 ,ETCLR1	:TMENC clear Inputs
ETO0, ETO1	:TMENC outputs
PWMO0 ,PWMO1	:PWM Outputs
TXD0 to TXD3	:UART transmit Outputs
RXD0 to RXD3	:UART receive Inputs
SCK0 ,SCK1	:Clocked Serial Interface Clock I/O
SI0 ,SI1	:Clocked Serial Interface Serial Input
SO0 ,SO1	:Clocked Serial Interface Serial Output
ADTRG	:A/D Trigger Input
NMI	:Non-Maskable Interrupt Request
INTPZ0 to INTPZ7	:Interrupt Request & TMC Capture Trigger
INTPZ8 to INTPZ11	:Interrupt Request & TMENC Capture Trigger
INTPZ12 to INTPZ15	:Interrupt Request
INTPZ16 to INTPZ23	:Interrupt Request for SiP Internal
INTPZ24 to INTPZ31	:Interrupt Request
DMARQZ0 to DMARQZ3	:DMA Request
DMAAKZ0 to DMAAKZ3	:DMA Acknowledge

CSZ0-CSZ7	:Chip Select
A0-A25	:Address Bus
D0-D31	:Data Bus
RDZ	:Read Strobe
WRZ0 to WRZ3	:Write Strobe
WRSTBZ	:Write Strobe
BENZ0 to BENZ3	:Byte Enable
IORDZ	:I/O Read Strobe
IOWRZ	:I/O Write Strobe
DQM0 to DQM3	:SDRAM DQ mask enable
SDWEZ	:SDRAM Write enable
SDCASZ	:SDRAM Column address strobe
SDRASZ	:SDRAM Row address strobe
SDCKE	:SDRAM Clock Enable Output
WAITZ	:Wait Input
HLDRQZ	:Hold Request
HLDAKZ	:Hold Acknowledge
BCYSTZ	:Bus Cycle Start Timing
BUSCLK	:SDRAM Clock / Bus Clock output
REFRQZ	:Refresh Request
SELFREFZ	:Self-refresh Request
AVDD_AD	:A/D Converter V_{DD} (3.3V)
AVREFP	:A/D Converter Reference Voltage +
AIN0 to AIN7	:Analog Input
AVREFM	:A/D Converter Reference Voltage -
AGND_AD	:A/D Converter GND
UCLK	:USB Clock Input
UHD0P	:USB Host Channel 0 D+
UHD0M	:USB Host Channel 0 D–
UHD1P	:USB Host Channel 1 D+
UHD1M	:USB Host Channel 1 D–
PPON0	:USB Host Channel 0 PPON
PPON1	:USB Host Channel 1 PPON
OCI0	:USB Host Channel 0 OCI
OCI1	:USB Host Channel 1 OCI
UFD0P	:USB Function D+
UFD0M	:USB Function D–
VBUSDET	:USB VBUS Detect
PCLKIN	:USB Bus Bridge Clock Input
UCLKSEL0, UCLKSEL1	:USB Clock Select

TCZ0 to TCZ3	:DMA Terminal Count Outputs
SDMARQZ0, SDMARQZ1	:DMA Request for SiP Internal
SDMAAKZ0, SDMAAKZ1	:DMA Acknowledge for SiP Internal
STCZ0, SCZ1	:DMA Terminal Count Outputs for SiP Internal
SCSZ0 to SCSZ3	:Chip Select for SiP Internal
SA0 to SA20	:Address Bus for SiP Internal
SD0 to SD15	:Data Bus for SiP Internal
SRDZ	:Read Strobe for SiP Internal
SWRZ0, SWRZ1	:Write Strobe for SiP Internal
SWRSTBZ	:Write Strobe for SiP Internal
SBENZ0, SBENZ1	:Byte Enable for SiP Internal
SIORDZ	:I/O Read Strobe for SiP Internal
SIOWRZ	:I/O Write Strobe for SiP Internal
SWAITZ	:Wait Input for SiP Internal
SHLDRQZ	:Hold Request for SiP Internal
SHLDAKZ	:Hold Acknowledge for SiP Internal
SBCYSTZ	:Bus Cycle Start Timing for SiP Internal
SBUSCLK	:Bus Clock output for SiP Internal (6mA)
SREFRQZ	:Refresh Request for SiP Internal
DDI	:Debug Data Input
DCK	:Debug Clock Input
DMS	:Debug mode
DDO	:Debug Data Output
DRSTZ	:Debug Reset
DBINT	:DCU Debug Interrupt Input
TRCCLK	:Trace Clock
TRCEND	:Trace End Status Output
TRCDATA0 to TRCDATA7	:Trace Data Output
EVTTRG	:DCU Event Trigger
RMODEZ	:DCU Reset Mode
EVIN	:DCU Event Trigger
TRCCE	:DCU Trace Complex Enable

SLBS0, SLBS1	:Local Bus Size Select
VBCLKEN	:VBCLK Output Enable
SCKMD0, SCKMD1	:BUSCLK Divide Control
CLKDV0, CLKDV1	:VBCLK Divide Control
VSBRAMEN	:VSB RAM Enable
BOOTSEL	:Boot Select
MODE0, MODE1	:Operation Mode
PLL0 to PLL6	:PLLM0-PLLM6:PLL Divider Select
PLL7 to PLL9	:PLLN0-PLLN2
PLL10 to PLL11	:PLLP0-PLLP1
PLL12	:SSMDL0:Modulation Frequency Range
PLL13	:SSMDL1
PLL14 to PLL16	:SSADJ0-:SSCG Jitter Select :SSADJ2
PLL17, PLL18	:PLLS0-PLLS1
TMODE0	:Test Mode Select
TMODE1	:Test Mode Select
TMODE2	:Test Mode Select
TMODE3	:Test Mode Select
TESTCLK	:Test Clock Input / Test Output
TMC1	:1 Chip Test Mode Select
TMC2	:1 Chip Test Mode Select
TMS	:TAP Controller Mode Select
TDI	:Register Data Input
TRST	:TAP Controller Reset
TCK	:TAP Controller Clock
TDO	:Register Data Output
IROMEN	:Instruction RAM for Test
RESETZ	:System Reset
VBRESTOZ	:System Reset Output
XT1, XT2	:Oscillator
VBCLKOUT	:System Clock Output
PLLFO	:PLL FO Output
AVDD_PLL0	:SSCG PLL Power Supply (1.5V)
AVDD_PLL1	:SSCG PLL Power Supply (1.5V)
AGND_PLL0	:SSCG PLL Ground
AGND_PLL1	:SSCG PLL Ground
EVDD	:I/O Power Supply (3.3V)
IVDD	:Internal Power Supply (1.5V)
EGND	:I/O Power Ground
IGND	:Internal Power Ground

2.4 Electrical Characteristics

2.4.1 Absolute maximum ratings

Item	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD15}	1.5 V system	−0.5 to +2.0	V
Power supply voltage	V_{DD33}	3.3 V system	−0.5 to +4.6	V
I/O Voltage	V_I/V_O	3.3 V buffer V_I/V_O < VD33+0.5 V	−0.5 to +4.6	V
Output current	I_O	3.3 V buffer, I_{OL} = 3 mA Type	11	mA
		3.3 V buffer, I_{OL} = 6 mA Type	21	mA
		3.3 V buffer, I_{OL} = 9 mA Type	29	mA
		3.3 V buffer, I_{OL} = 12 mA Type	45	mA
		3.3 V buffer, I_{OL} = 18 mA Type	58	mA
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2.4.2 Recommended operating range

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD15}	1.5 V system	1.35	1.5	1.65	V
	V_{DD33}	3.3 V system	3.0	3.3	3.6	V
Operating ambient temperature	T_A		40		85	°C
Negative trigger voltage	V_N	3.3 V Schmitt buffer	0.6		1.8	V
Positive trigger voltage	V_P	3.3 V Schmitt buffer	1.2		2.4	V
Hysteresis voltage	V_H	3.3 V Schmitt buffer	0.3		1.5	V
Low-level input voltage	V_{IL}	3.3 V buffer	0		0.8	V
High-level input voltage	V_{IH}	3.3 V buffer	2.0		V_{DD33}	V
Input rise time	trI	Normal input	0		200	ns
Input fall time	t_{fI}	Normal input	0		200	ns
Input rise time	t_{rI}	Schmitt input	0		10	ms
Input fall time	t_{fI}	Schmitt input	0		10	ms

2.4.3 DC characteristics (V_{DD15} = 1.5 V ±0.15 V, V_{DD33} = 3.3 V ±0.3 V, T_A = -40 to +85 °C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OFF-state current	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
Output short-circuit current[Note1]	I_{OS}				-250	μA
Input leakage current (3.3 V buffer)	I_I	VI = VD33 or GND (Normal input)		±10–1	±10	μA
		VI = GND(pull-up 50 kΩ)	-37	-103	-253	μA
		VI = GND(pull-up 5 kΩ)	-305	-827	-1947	μA
		VI = VD33(pull-down 50 kΩ)	26	73	175	μA
Analog input leakage current	I_{LWASN}	ANI0 to ANI7 pins			±10	μA
Pull-up resister (5 kΩ)	R_{PU}	3.3 V buffer	1.8	4.0	9.9	kΩ
Pull-up resister (50 k Ω)	R_{PU}	3.3 V buffer	14.2	31.9	80.7	kΩ
Pull-down resister (50 k Ω)	R_{PD}	3.3 Vbuffer	20.6	44.9	116.4	kΩ
Low-level output current	I_{OL}	V_{OL} = 0.4 V(I_{OL} = 3 mA Type, 3.3 V buffer)	3.0			mA
		V_{OL} = 0.4 V(I_{OL} = 6 mA Type, 3.3 V buffer)	6.0			mA
		V_{OL} = 0.4 V(I_{OL} = 9 mA Type, 3.3 V buffer)	9.0			mA
		V_{OL} = 0.4 V(I_{OL} = 12 mA Type, 3.3 V buffer)	12.0			mA
		V_{OL} = 0.4 V(I_{OL} = 18 mA Type, 3.3 V buffer)	18.0			mA
High-level output current	I_{OH}	V_{OH} = 2.4 V(I_{OL} = 3 mA Type, 3.3 V buffer)	-3.0			mA
		V_{OH} = 2.4 V(I_{OL} = 6 mA Type, 3.3 V buffer)	-6.0			mA
		V_{OH} = 2.4 V(I_{OL} = 9 mA Type, 3.3 V buffer)	-9.0			mA
		V_{OH} = 2.4 V(I_{OL} = 12 mA Type, 3.3 V buffer)	-12.0			mA
		V_{OH} = 2.4 V(I_{OL} = 18 mA Type,3.3V buffer)	-18.0			mA
Low-level output voltage	V_{OL}	I_{OL} = 0 mA (3.3 V buffer)			0.1	V
High-level output voltage	V_{OH}	I_{OH} = 0 mA (3.3 V buffer)	VD33–0.1			V
Differential input sensitivity	V_{DI}	|(D+) – (D–)|(USB buffer)	0.2			V
Common mode voltage range	V_{CM}	to Local GND reference (USB buffer)	0.8		2.5	V
Single-ended 0 reception threshold	V_{SE}	(**Note2**) (USB buffer)	0.8		2.0	V
High-level output voltage	V_{OH}	RL of 15 kΩ to GND (USB buffer)	2.8		3.6	V
Low-level output voltage	V_{OL}	RL of 1.5 kΩ to 3.6 V (USB buffer)	0		0.3	V
Data line Hi-Z leakage current	I_{LO}	0 V < V_{IN} < 3.3 V (USB buffer)	-10		+10	μA

Note 1. The output short-circuit time is 1 second or less per pin of the LSI.

2. V_{SE} is Single-ended receiver input level and comply with LVTTL Specifications. (V_{IL} = 0.8 V, V_{IH} = 2.0 V)

* The + and − signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by −.

2.4.4 AC characteristics (V_{DD15} = 1.5 V ±0.15 V, V_{DD33} = 3.3 V ±0.3 V, T_A = -40 to +85 °C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Toggle frequency (L Type)	f_{tog}	Internal toggle F/F(F/O = 1)		1.9		GHz
Toggle frequency (M Type)	f_{tog}	Internal toggle F/F(F/O = 1)		3.1		GHz
Propagation delay time	t_{PD}	3.3 V input buffer F/O = 1 Wiring length = 30 μ m, t_r = t_f = 0.1 ns		184		ps
		3.3 V output buffer (18 mA), C_L = 15 pF		903		ps
		3.3 V outputr buffer (24 mA), C_L = 15 pF		867		ps
Propagation delay time (L Type)	t_{PD}	Internal gate F/O = 1, standard wiring length		41.3		ps
		Internal gate (power gate) F/O = 1, standard wiring length		30.8		ps
Propagation delay time (M Type)	t_{PD}	Internal gate F/O = 1, standard wiring length		27.1		ps
		Internal gate (power gate) F/O = 1, standard wiring length		19.9		ps
Output rise time	t_r	3.3 V output buffer (18 mA) C_L = 15 pF: 10 to 90 %		944		ps
Output fall time	t_f	3.3 V output buffer (18 mA) C_L = 15 pF: 10 to 90 %		637		ps

CHAPTER 3 EP-1 SERIES EVALUATION AND GATE ARRAY DEVELOPMENT

When developing an LSI using EP-1 series, to implementing some or all of a system designed by the user, the specifications must be determined so that the circuit scale and the number of I/O pins of the gate arrays are optional.

Afterward, normally, gate array development is performed by using the following procedure.

(1) Estimate circuit scale and master size

↓

(2) Select package

↓

(3) Verify power consumption

↓

(4) Verify pin placement

↓

(5) Verify I/O interface level

↓

(6) Gate array development

↓

(7) Interface

↓

(8) Check using check item list

Hereinafter, the procedure is described in the order shown above.

3.1 Circuit Size and Master Size Estimation

3.1.1 Cell utilization rate, usable cell and pin pair number limits

The gate array uses a channelless architecture (sea-of-gates). This means that not all cells in the internal cell region can be used for function blocks such as gates, flip-flops, and memory. The number of cells actually used is the difference between the total number of cells and the routing cell region used by the number of wires between blocks (number of pin pairs).

The maximum cell utilization rates for the gate array are roughly as follows:

Table 3-1. Cell utilization rate

Wiring	Master Name	Number of Raw Cells	Usable Gate Number (Cell utilization rate)
3-layer wiring	MC-10501/10505	133380	80028 (60 %)
	MC-10502/10506	281636	160041 (60 %)
	MC-10503/10507	418953	242676 (60 %)

However, if a large-scale block, such as memory, is mounted, it may be that the total cell utilization rate is further limited, depending on the type of macro (see **3.1.3 Large-scale macro placement**).

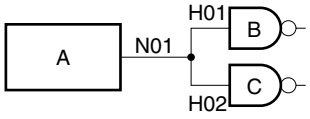
The pin-pair number is limited by the cell utilization rate and can be calculated by the following formula:

- 3-layer wiring product

  Pin-pair count = 112 × number of raw cells × {(100 – cell utilization rate)/100}^{2} /74.69

"Pin-pair count" is the number of wires connecting the output pins and input pins between blocks (see **Figure 3-1**).

Figure 3-1. Pin-pair Count



Block A N01-Block B H01
Block A N01-Block C H02

Total of 2 pairs (pin pair count = 2)

If many small-scale blocks such as inverters are used, routing between blocks increases compared with the number of cells used, which increases the number of routing channels.

Conversely, if many large-scale blocks such as memory are used, routing between blocks decreases compared with the number of cells used, which decreases the number of channels required.

Consequently, when placing large-scale blocks, such as memory, the cell utilization rate is further limited. Circuits that do not include memory are limited by the pin-pair count.

If the actual cell utilization rate and pin-pair count can be satisfied, placement and routing can be guaranteed in the standard schedule in most cases. On the other hand, in cases where the limits are exceeded, placement and routing requires a longer time and, in the worst case, becomes impossible.

Table 3-2 shows the number of usable gates and the corresponding pin-pair count with respect to the cell utilization rate.

Table 3-2. Usable Gates, Pin-pair Count

Product Name	35% Cell Utilization		40% Cell Utilization		45% Cell Utilization		50% Cell Utilization		60% Cell Utilization		70% Cell Utilization	
	Usable Gates	Pin-pair	Usable Gates	Pin-pair	Usable Gates	Pin-pair	Usable Gates	Pin-pair	Usable Gates	Pin-pair	Usable Gates	Pin-pair
MC-10501/10505	46683	84503	53352	72002	60021	60502	66690	50001	80028	32001	93366	18000
MC-10502/10506	98572	178431	112654	152035	126736	127752	140818	105580	168981	67571	197145	38008
MC-10503/10507	146633	265428	167581	226163	188528	190040	209476	157058	251371	100517	293267	56540

3.1.2 Notes on estimating number of cells used

(1) Input/output/bidirectional buffer blocks

Not only I/O cells but also internal cells are used to configure external interface blocks such as input, output, and bidirectional blocks. Therefore, add the number of internal cells used for input, output, and bidirectional buffer blocks described in **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)** when calculating the total number of cells used.

(2) Critical paths

If there is a path in which speed is a problem, measures can be taken in some cases to shorten the propagation delay of that path. However, routability drops dramatically when such measures are taken. In such a case, the cell utilization rate and maximum pin-pair count should be reduced by a further 10 to 20%.

(3) Macro configuration

Placement and routing are performed for each hierarchical macro (first hierarchy) in the circuit. Therefore, the hierarchical configuration calls for adequate consideration when a macro is created. Keep in mind the following points when performing hierarchical design.

(a) Because the routing between macros of the first hierarchy is long, avoid hierarchical design that implements one function between macros.

(b) If possible, avoid placing a small-scale macro that is used to facilitate circuit design in the first hierarchy.

3.1.3 Large-scale macro placement

Large-scale macro placeability is determined by whether or not it is possible to achieve the range (X × Y) of cells needed to implement the macros on the physical space of the internal cells indicated by (X × Y). For soft macros configured by small and medium-scale blocks, virtually no problems of placement arise as long as the cell utilization rate is satisfied. However, there are cases in which large-scale hard macros such as RAM blocks (basic macro) cannot be physically placed due to the size of the master.

Whether macros can be placed is determined by the range of the cells necessary for implementing each macro on the chip, and the range of cells that can be implemented on the master.

Table 3-3. Number of Raw Cells

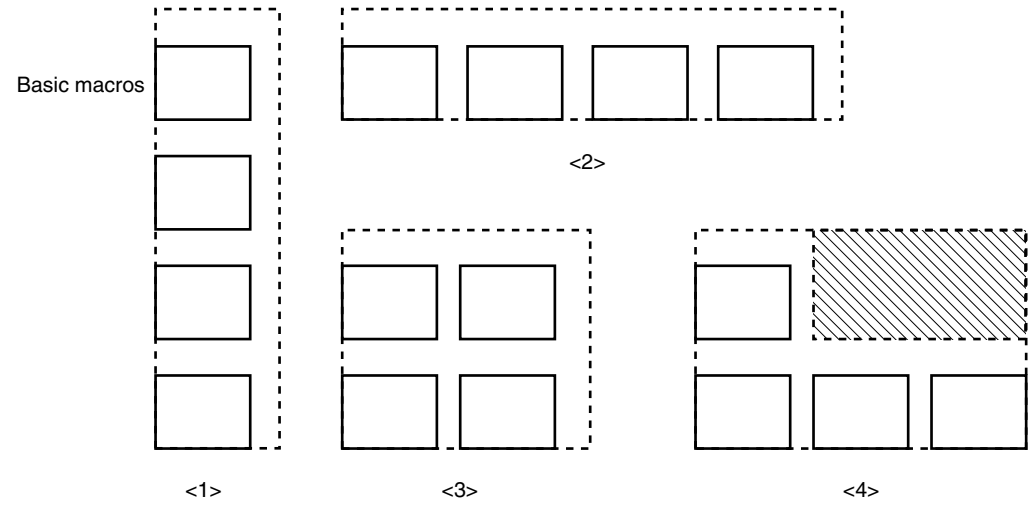
Wiring	Master Name	X	Y	Number of Raw Cells
3-layer Wiring	MC-10501/10505	494	270	133380
	MC-10502/10506	724	389	281636
	MC-10503/10507	1077	389	418953

(1) Range of cells occupied by each macro on chip

(a) Soft macro RAM

An NEC Electronics RAM is implemented by soft macros that consist of a basic macro and a logic area. The shape of the cell area occupied to implement a macro depends on how the basic macro is placed. The cell area occupied is limited by the master selected.

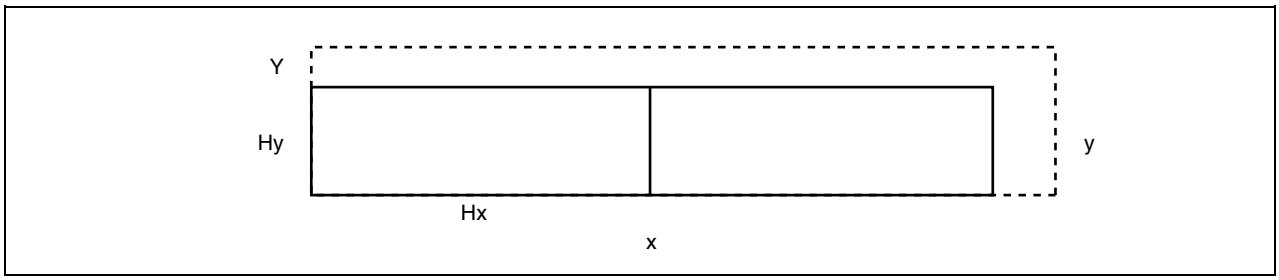
Figure 3-2. Shape of Cell Range Occupied by Macros (with 4 Basic Macros)



<1>: Limited by the number of vertical cells of the master.
<2>: Limited by the number of horizontal cells of the master.
<3>: Effective if the number of basic blocks used becomes large.
<4>: Physically possible but ineffective (because the placement range that can be specified during placement and routing is square or rectangular, the diagonally shaded area is wasted).

Table 3-5 lists examples of the cell ranges occupied by macros. However, it is possible to re-define cell ranges for a RAM outside those in Table 3-5.
To define cell ranges for soft macro RAM, first find the basic macro name and the number of cells required to configure the soft macro RAM in Table 3-5. Next, find the number of cells occupied by the basic macro (X and Y values) in Table 3-4. Then calculate the cell range by substituting in the variables in the following equation with the values from Tables 3-4 and 3-5.

Figure 3-3. Cell Range Occupied by Macro



$y = 2^n \times Hy + Y$

x = soft/uty/y

In the above equation, $\times \geq N/2n \times Hx$ must be satisfied.

soft :Number of cells in the soft macro RAM

uty : Apply the value shown in Table 3-1 for the cell utilization rate when the macro utilization rate is less than 50%.

Example In the case of MC-10501: 60 % = 0.60

Apply a value that is the value shown in Table 3-1 minus 5% when the macro utilization rate is more than 50%.

Example In the case of MC-10501: 60-5 % = 55 % = 0.55

Hx : Minimum number of cells occupied in the horizontal direction needed for placing basic macros.

Hy : Minimum number of cells occupied in the vertical direction needed for placing basic macros.

N : Number of basic macros used

n : When the number of basic macros is 1, n = 0

When the number of basic macros is 2, n = 0, 1

When the number of basic macros is 4, n = 0, 1, 2

When the number of basic macros is 8, n = 0, 1, 2, 3

When the number of basic macros is 16, n = 0, 1, 2, 3, 4

When the number of basic macros is 32, n = 0, 1, 2, 3, 4, 5

Y : Arbitrary integer (Y = 0, 1, 2, ...)

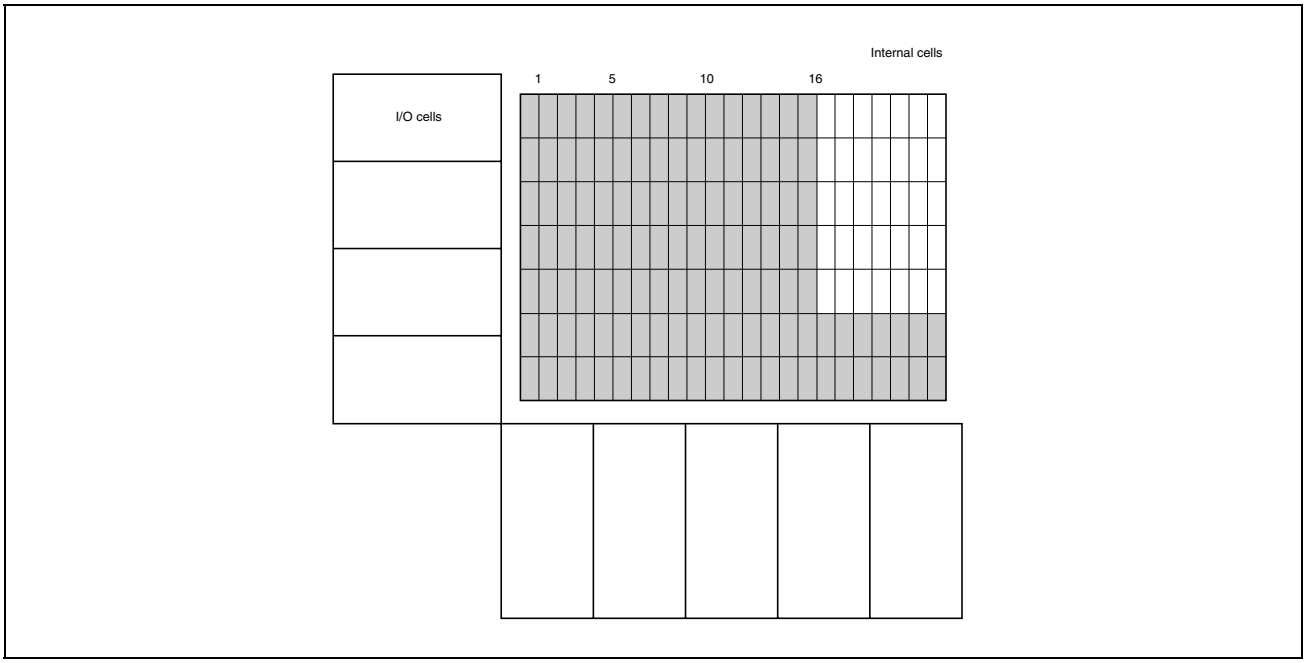
(b) Clock input drivers

The X × Y structure of cells used in a clock input driver differs from normal macros in its very long vertical dimensions. Because the vertical direction of some masters and place cells is much reduced compared with the horizontal direction, there are cases in which placement cannot be performed due to the master. Because the clock input driver requires a routing channel, it is necessary to consult with NEC Electronics if it is to be placed with other large-scale macros.

(2) Array of internal cells of master selected (see Table 3-3.)

Internal cells are also used for PFESiP/V850EP1 interface blocks and are limited as closely as possible to the I/O cell range. The area of internal cells used by the interface block is 16 internal cells from the left edge to the right edge and 2 cells from the top edge to the bottom edge. Therefore the cell area that the macro can placed in must be within the 16 × 2 range (blank part in Figure 3-4).

Figure 3-4. Area Where Macros Cannot Be Implemented



(3) Determining placeability

Macros are placeable if they can all be placed without overlapping, within the allowable area for implementing macros on the chip. If they are unplaceable, modification of the shape of the macro-occupied area must be considered. If more than one cell overlaps, consult NEC Electronics to determine placeability taking the pin configuration and macro placement position into consideration.

Table 3-4. Minimum Number of Cells Occupied by Basic Macro

(a) High-density 1-port RAM

Basic Macro	Words	Bits	X	Y
K147	16	4	48	9
K149	32	4	50	13
K18B	64	8	94	21
K1AB	64	10	116	21
K14D	128	4	82	21
K18F	256	8	160	37
K1AF	256	10	198	37
K18M	1024	8	316	69
K1AM	1024	10	392	69

(b) High-density 2-port RAM (W+R)

Basic Macro	Words	Bits	X	Y
K247	16	4	58	11
K249	32	4	106	11
K28B	64	8	208	15
K2AB	64	10	256	15
K24D	128	4	208	18
K28F	256	8	400	25
K2AF	256	10	496	25
K28M	1024	8	784	47
K2AM	1024	10	976	47

Table 3-5 shows the block names and cell ranges occupied by each RAM macro on the chip.

Table 3-5. Occupied Cell Ranges (1/8)

High-Density 1-Port RAM (55% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
RB47	16	4	K147	1	65	12						
RB49	32	4	K149	1	74	16						
RB4B	64	4	K149	2	74	32	148	16				
RB4D	128	4	K14D	1	130	24						
RB4F	256	4	K14D	2	130	48	261	24				
RB4H	512	4	K14D	4	130	96	261	48	522	24		
RB4M	1024	4	K14D	8	130	192	261	96	522	48	1044	24
RB4S	2048	4	K14D	16	130	384	261	192	522	96	1044	48
RB4U	4096	4	K14D	32	130	768	261	384	522	192	1044	96
RB87	16	8	K147	2	65	24	131	12				
RB89	32	8	K149	2	74	32	148	16				
RB8B	64	8	K18B	1	150	24						
RB8D	128	8	K14D	2	130	48	261	24				
RB8F	256	8	K18F	1	269	40						
RB8H	512	8	K18F	2	269	80	538	40				
RB8M	1024	8	K18M	1	551	72						
RB8S	2048	8	K18M	2	551	144	1101	72				
RBAB	64	10	K1AB	1	185	24						
RBAD	128	10	K1AB	2	185	48	369	24				
RBAF	256	10	K1AF	1	333	40						
RBAH	512	10	K1AF	2	333	80	666	40				
RBAM	1024	10	K1AM	1	683	72						
RBAS	2048	10	K1AM	2	683	144	1366	72				
RBC7	16	16	K147	4	65	48	131	24	262	12		
RBC9	32	16	K149	4	74	64	148	32	295	16		
RBCB	64	16	K18B	2	150	48	299	24				
RBCD	128	16	K14D	4	130	96	261	48	522	24		
RBCF	256	16	K18F	2	269	80	538	40				
RBCH	512	16	K18F	4	269	160	538	80	1076	40		
RBCM	1024	16	K18M	2	551	144	1101	72				
RBEB	64	20	K18B	2	150	48	299	24				
RBED	128	20	K1AB	4	185	96	369	48	738	24		
RBEF	256	20	K1AF	2	333	80	666	40				
RBEH	512	20	K1AF	4	333	160	666	80	1332	40		
RBEM	1024	20	K1AM	2	683	144	1366	72				
RBH7	16	32	K147	8	65	96	131	48	262	24	524	12
RBH9	32	32	K149	8	74	128	148	64	295	32	591	16
RBHB	64	32	K18B	4	150	96	299	48	598	24		
RBHD	128	32	K14D	8	130	192	261	96	522	48	1044	24
RBHF	256	32	K18F	4	269	160	538	80	1076	40		
RBHH	512	32	K18F	8	269	320	538	160	1076	80	2153	40
RBKB	64	40	K18B	4	150	96	299	48	598	24		
RBKD	128	40	K1AB	8	185	192	369	96	738	48	1476	24
RBKF	256	40	K1AF	4	333	160	666	80	1332	40		
RBKH	512	40	K1AF	8	333	320	666	160	1332	80	2664	40

Table 3-5. Occupied Cell Ranges (2/8)

High-Density 1-Port RAM (50% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
RB47	16	4	K147	1	72	12						
RB49	32	4	K149	1	81	16						
RB4B	64	4	K149	2	81	32	163	16				
RB4D	128	4	K14D	1	144	24						
RB4F	256	4	K14D	2	144	48	287	24				
RB4H	512	4	K14D	4	144	96	287	48	574	24		
RB4M	1024	4	K14D	8	144	192	287	96	574	48	1148	24
RB4S	2048	4	K14D	16	144	384	287	192	574	96	1148	48
RB4U	4096	4	K14D	32	144	768	287	384	574	192	1148	96
RB87	16	8	K147	2	72	24	144	12				
RB89	32	8	K149	2	81	32	163	16				
RB8B	64	8	K18B	1	165	24						
RB8D	128	8	K14D	2	144	48	287	24				
RB8F	256	8	K18F	1	296	40						
RB8H	512	8	K18F	2	296	80	592	40				
RB8M	1024	8	K18M	1	606	72						
RB8S	2048	8	K18M	2	606	144	1211	72				
RBAB	64	10	K1AB	1	203	24						
RBAD	128	10	K1AB	2	203	48	406	24				
RBAF	256	10	K1AF	1	366	40						
RBAH	512	10	K1AF	2	366	80	733	40				
RBAM	1024	10	K1AM	1	751	72						
RBAS	2048	10	K1AM	2	751	144	1503	72				
RBC7	16	16	K147	4	72	48	144	24	288	12		
RBC9	32	16	K149	4	81	64	163	32	325	16		
RBCB	64	16	K18B	2	165	48	329	24				
RBCD	128	16	K14D	4	144	96	287	48	574	24		
RBCF	256	16	K18F	2	296	80	592	40				
RBCH	512	16	K18F	4	296	160	592	80	1184	40		
RBCM	1024	16	K18M	2	606	144	1211	72				
RBEB	64	20	K18B	2	165	48	329	24				
RBED	128	20	K1AB	4	203	96	406	48	812	24		
RBEF	256	20	K1AF	2	366	80	733	40				
RBEH	512	20	K1AF	4	366	160	733	80	1465	40		
RBEM	1024	20	K1AM	2	751	144	1503	72				
RBH7	16	32	K147	8	72	96	144	48	288	24	576	12
RBH9	32	32	K149	8	81	128	163	64	325	32	650	16
RBHB	64	32	K18B	4	165	96	329	48	658	24		
RBHD	128	32	K14D	8	144	192	287	96	574	48	1148	24
RBHF	256	32	K18F	4	296	160	592	80	1184	40		
RBHH	512	32	K18F	8	296	320	592	160	1184	80	2368	40
RBKB	64	40	K18B	4	165	96	329	48	658	24		
RBKD	128	40	K1AB	8	203	192	406	96	812	48	1624	24
RBKF	256	40	K1AF	4	366	160	733	80	1465	40		
RBKH	512	40	K1AF	8	366	320	733	160	1465	80	2930	40

Table 3-5. Occupied Cell Ranges (3/8)

High-Density 1-Port RAM (45% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
RB47	16	4	K147	1	80	12						
RB49	32	4	K149	1	90	16						
RB4B	64	4	K149	2	90	32	181	16				
RB4D	128	4	K14D	1	159	24						
RB4F	256	4	K14D	2	159	48	319	24				
RB4H	512	4	K14D	4	159	96	319	48	638	24		
RB4M	1024	4	K14D	8	159	192	319	96	638	48	1276	24
RB4S	2048	4	K14D	16	159	384	319	192	638	96	1276	48
RB4U	4096	4	K14D	32	159	768	319	384	638	192	1276	96
RB87	16	8	K147	2	80	24	160	12				
RB89	32	8	K149	2	90	32	181	16				
RB8B	64	8	K18B	1	183	24						
RB8D	128	8	K14D	2	159	48	319	24				
RB8F	256	8	K18F	1	329	40						
RB8H	512	8	K18F	2	329	80	658	40				
RB8M	1024	8	K18M	1	673	72						
RB8S	2048	8	K18M	2	673	144	1346	72				
RBAB	64	10	K1AB	1	226	24						
RBAD	128	10	K1AB	2	226	48	451	24				
RBAF	256	10	K1AF	1	407	40						
RBAH	512	10	K1AF	2	407	80	814	40				
RBAM	1024	10	K1AM	1	835	72						
RBAS	2048	10	K1AM	2	835	144	1670	72				
RBC7	16	16	K147	4	80	48	160	24	320	12		
RBC9	32	16	K149	4	90	64	181	32	361	16		
RBCB	64	16	K18B	2	183	48	366	24				
RBCD	128	16	K14D	4	159	96	319	48	638	24		
RBCF	256	16	K18F	2	329	80	658	40				
RBCH	512	16	K18F	4	329	160	658	80	1316	40		
RBCM	1024	16	K18M	2	673	144	1346	72				
RBEB	64	20	K18B	2	183	48	366	24				
RBED	128	20	K1AB	4	226	96	451	48	902	24		
RBEF	256	20	K1AF	2	407	80	814	40				
RBEH	512	20	K1AF	4	407	160	814	80	1628	40		
RBEM	1024	20	K1AM	2	835	144	1670	72				
RBH7	16	32	K147	8	80	96	160	48	320	24	640	12
RBH9	32	32	K149	8	90	128	181	64	361	32	722	16
RBHB	64	32	K18B	4	183	96	366	48	731	24		
RBHD	128	32	K14D	8	159	192	319	96	638	48	1276	24
RBHF	256	32	K18F	4	329	160	658	80	1316	40		
RBHH	512	32	K18F	8	329	320	658	160	1316	80	2631	40
RBKB	64	40	K18B	4	183	96	366	48	731	24		
RBKD	128	40	K1AB	8	226	192	451	96	902	48	1804	24
RBKF	256	40	K1AF	4	407	160	814	80	1628	40		
RBKH	512	40	K1AF	8	407	320	814	160	1628	80	3256	40

Table 3-5. Occupied Cell Ranges (4/8)

High-Density 1-Port RAM (40% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
RB47	16	4	K147	1	90	12						
RB49	32	4	K149	1	102	16						
RB4B	64	4	K149	2	102	32	203	16				
RB4D	128	4	K14D	1	179	24						
RB4F	256	4	K14D	2	179	48	359	24				
RB4H	512	4	K14D	4	179	96	359	48	718	24		
RB4M	1024	4	K14D	8	179	192	359	96	718	48	1435	24
RB4S	2048	4	K14D	16	179	384	359	192	718	96	1435	48
RB4U	4096	4	K14D	32	179	768	359	384	718	192	1435	96
RB87	16	8	K147	2	90	24	180	12				
RB89	32	8	K149	2	102	32	203	16				
RB8B	64	8	K18B	1	206	24						
RB8D	128	8	K14D	2	179	48	359	24				
RB8F	256	8	K18F	1	370	40						
RB8H	512	8	K18F	2	370	80	740	40				
RB8M	1024	8	K18M	1	757	72						
RB8S	2048	8	K18M	2	757	144	1514	72				
RBAB	64	10	K1AB	1	254	24						
RBAD	128	10	K1AB	2	254	48	508	24				
RBAF	256	10	K1AF	1	458	40						
RBAH	512	10	K1AF	2	458	80	916	40				
RBAM	1024	10	K1AM	1	939	72						
RBAS	2048	10	K1AM	2	939	144	1878	72				
RBC7	16	16	K147	4	90	48	180	24	360	12		
RBC9	32	16	K149	4	102	64	203	32	406	16		
RBCB	64	16	K18B	2	206	48	411	24				
RBCD	128	16	K14D	4	179	96	359	48	718	24		
RBCF	256	16	K18F	2	370	80	740	40				
RBCH	512	16	K18F	4	370	160	740	80	1480	40		
RBCM	1024	16	K18M	2	757	144	1514	72				
RBEB	64	20	K18B	2	206	48	411	24				
RBED	128	20	K1AB	4	254	96	508	48	1015	24		
RBEF	256	20	K1AF	2	458	80	916	40				
RBEH	512	20	K1AF	4	458	160	916	80	1832	40		
RBEM	1024	20	K1AM	2	939	144	1878	72				
RBH7	16	32	K147	8	90	96	180	48	360	24	720	12
RBH9	32	32	K149	8	102	128	203	64	406	32	813	16
RBHB	64	32	K18B	4	206	96	411	48	823	24		
RBHD	128	32	K14D	8	179	192	359	96	718	48	1435	24
RBHF	256	32	K18F	4	370	160	740	80	1480	40		
RBHH	512	32	K18F	8	370	320	740	160	1480	80	2960	40
RBKB	64	40	K18B	4	206	96	411	48	823	24		
RBKD	128	40	K1AB	8	254	192	508	96	1015	48	2030	24
RBKF	256	40	K1AF	4	458	160	916	80	1832	40		
RBKH	512	40	K1AF	8	458	320	916	160	1832	80	3663	40

Table 3-5. Occupied Cell Ranges (5/8)

High-Density 2-Port RAM (W+R) (55% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
R947	16	4	K247	1	83	14						
R949	32	4	K249	1	151	14						
R94B	64	4	K249	2	151	28	303	14				
R94D	128	4	K24D	1	324	21						
R94F	256	4	K24D	2	324	42	648	21				
R94H	512	4	K24D	4	324	84	648	42	1297	21		
R94M	1024	4	K24D	8	324	168	648	84	1297	42	2593	21
R94S	2048	4	K24D	16	324	336	648	168	1297	84	2593	42
R94U	4096	4	K24D	32	324	672	648	336	1297	168	2593	84
R987	16	8	K247	2	83	28	166	14				
R989	32	8	K249	2	151	28	303	14				
R98B	64	8	K28B	1	315	18						
R98D	128	8	K24D	2	324	42	648	21				
R98F	256	8	K28F	1	649	28						
R98H	512	8	K28F	2	649	56	1299	28				
R98M	1024	8	K28M	1	1340	50						
R98S	2048	8	K28M	2	1340	100	2680	50				
R9AB	64	10	K2AB	1	388	18						
R9AD	128	10	K2AB	2	388	36	776	18				
R9AF	256	10	K2AF	1	761	28						
R9AH	512	10	K2AF	2	761	56	1523	28				
R9AM	1024	10	K2AM	1	1668	50						
R9AS	2048	10	K2AM	2	1668	100	3336	50				
R9C7	16	16	K247	4	83	56	166	28	331	14		
R9C9	32	16	K249	4	151	56	303	28	606	14		
R9CB	64	16	K28B	2	315	36	630	18				
R9CD	128	16	K24D	4	324	84	648	42	1297	21		
R9CF	256	16	K28F	2	649	56	1299	28				
R9CH	512	16	K28F	4	649	112	1299	56	2597	28		
R9CM	1024	16	K28M	2	1340	100	2680	50				
R9EB	64	20	K28B	2	315	36	630	18				
R9ED	128	20	K2AB	4	388	72	776	36	1552	18		
R9EF	256	20	K2AF	2	761	56	1523	28				
R9EH	512	20	K2AF	4	761	112	1523	56	3045	28		
R9EM	1024	20	K2AM	2	1668	100	3336	50				
R9H7	16	32	K247	8	83	112	166	56	331	28	663	14
R9H9	32	32	K249	8	151	112	303	56	606	28	1211	14
R9HB	64	32	K28B	4	315	72	630	36	1261	18		
R9HD	128	32	K24D	8	324	168	648	84	1267	42	2593	21
R9HF	256	32	K28F	4	649	112	1299	56	2597	28		
R9HH	512	32	K28F	8	649	224	1299	112	2597	56	5195	28
R9KB	64	40	K28B	4	315	72	630	36	1261	18		
R9KD	128	40	K2AB	8	388	144	776	72	1552	36	3103	18
R9KF	256	40	K2AF	4	761	112	1523	56	3045	28		
R9KH	512	40	K2AF	8	761	224	1523	112	3045	56	6091	28

Table 3-5. Occupied Cell Ranges (6/8)

High-Density 2-Port RAM (W+R) (50% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
R947	16	4	K247	1	91	14						
R949	32	4	K249	1	167	14						
R94B	64	4	K249	2	167	28	333	14				
R94D	128	4	K24D	1	357	21						
R94F	256	4	K24D	2	357	42	713	21				
R94H	512	4	K24D	4	357	84	713	42	1426	21		
R94M	1024	4	K24D	8	357	168	713	84	1426	42	2853	21
R94S	2048	4	K24D	16	357	336	713	168	1426	84	2853	42
R94U	4096	4	K24D	32	357	672	713	336	1426	168	2853	84
R987	16	8	K247	2	91	28	182	14				
R989	32	8	K249	2	167	28	333	14				
R98B	64	8	K28B	1	347	18						
R98D	128	8	K24D	2	357	42	713	21				
R98F	256	8	K28F	1	714	28						
R98H	512	8	K28F	2	714	56	1429	28				
R98M	1024	8	K28M	1	1474	50						
R98S	2048	8	K28M	2	1474	100	2948	50				
R9AB	64	10	K2AB	1	427	18						
R9AD	128	10	K2AB	2	427	36	853	18				
R9AF	256	10	K2AF	1	838	28						
R9AH	512	10	K2AF	2	838	56	1675	28				
R9AM	1024	10	K2AM	1	1835	50						
R9AS	2048	10	K2AM	2	1835	100	3670	50				
R9C7	16	16	K247	4	91	56	182	28	365	14		
R9C9	32	16	K249	4	167	56	333	28	666	14		
R9CB	64	16	K28B	2	347	36	693	18				
R9CD	128	16	K24D	4	357	84	713	42	1426	21		
R9CF	256	16	K28F	2	714	56	1429	28				
R9CH	512	16	K28F	4	714	112	1429	56	2857	28		
R9CM	1024	16	K28M	2	1474	100	2948	50				
R9EB	64	20	K28B	2	347	36	693	18				
R9ED	128	20	K2AB	4	427	72	853	36	1707	18		
R9EF	256	20	K2AF	2	838	56	1675	28				
R9EH	512	20	K2AF	4	838	112	1675	56	3350	28		
R9EM	1024	20	K2AM	2	1835	100	3670	50				
R9H7	16	32	K247	8	91	112	182	56	365	28	729	14
R9H9	32	32	K249	8	167	112	333	56	666	28	1333	14
R9HB	64	32	K28B	4	347	72	693	36	1387	18		
R9HD	128	32	K24D	8	357	168	713	84	1426	42	2853	21
R9HF	256	32	K28F	4	714	112	1429	56	2857	28		
R9HH	512	32	K28F	8	714	224	1429	112	2857	56	5714	28
R9KB	64	40	K28B	4	347	72	693	36	1387	18		
R9KD	128	40	K2AB	8	427	144	853	72	1707	36	3413	18
R9KF	256	40	K2AF	4	838	112	1675	56	3350	28		
R9KH	512	40	K2AF	8	838	224	1675	112	3350	56	6700	28

Table 3-5. Occupied Cell Ranges (7/8)

High-Density 2-Port RAM (W+R) (45% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
R947	16	4	K247	1	101	14						
R949	32	4	K249	1	185	14						
R94B	64	4	K249	2	185	28	370	14				
R94D	128	4	K24D	1	396	21						
R94F	256	4	K24D	2	396	42	792	21				
R94H	512	4	K24D	4	396	84	792	42	1585	21		
R94M	1024	4	K24D	8	396	168	792	84	1585	42	3170	21
R94S	2048	4	K24D	16	396	336	792	168	1585	84	3170	42
R94U	4096	4	K24D	32	396	672	792	336	1585	168	3170	84
R987	16	8	K247	2	101	28	203	14				
R989	32	8	K249	2	185	28	370	14				
R98B	64	8	K28B	1	385	18						
R98D	128	8	K24D	2	396	42	792	21				
R98F	256	8	K28F	1	794	28						
R98H	512	8	K28F	2	794	56	1587	28				
R98M	1024	8	K28M	1	1638	50						
R98S	2048	8	K28M	2	1638	100	3275	50				
R9AB	64	10	K2AB	1	474	18						
R9AD	128	10	K2AB	2	474	36	948	18				
R9AF	256	10	K2AF	1	931	28						
R9AH	512	10	K2AF	2	931	56	1861	28				
R9AM	1024	10	K2AM	1	2039	50						
R9AS	2048	10	K2AM	2	2039	100	4078	50				
R9C7	16	16	K247	4	101	56	203	28	405	14		
R9C9	32	16	K249	4	185	56	370	28	740	14		
R9CB	64	16	K28B	2	385	36	770	18				
R9CD	128	16	K24D	4	396	84	792	42	1585	21		
R9CF	256	16	K28F	2	794	56	1587	28				
R9CH	512	16	K28F	4	794	112	1587	56	3175	28		
R9CM	1024	16	K28M	2	1638	100	3275	50				
R9EB	64	20	K28B	2	385	36	770	18				
R9ED	128	20	K2AB	4	474	72	948	36	1896	18		
R9EF	256	20	K2AF	2	931	56	1861	28				
R9EH	512	20	K2AF	4	931	112	1861	56	3722	28		
R9EM	1024	20	K2AM	2	2039	100	4078	50				
R9H7	16	32	K247	8	101	112	203	56	405	28	810	14
R9H9	32	32	K249	8	185	112	370	56	740	28	1481	14
R9HB	64	32	K28B	4	385	72	770	36	1541	18		
R9HD	128	32	K24D	8	396	168	792	84	1585	42	3170	21
R9HF	256	32	K28F	4	794	112	1587	56	3175	28		
R9HH	512	32	K28F	8	794	224	1587	112	3175	56	6349	28
R9KB	64	40	K28B	4	385	72	770	36	1541	18		
R9KD	128	40	K2AB	8	474	144	948	72	1896	36	3793	18
R9KF	256	40	K2AF	4	931	112	1861	56	3722	28		
R9KH	512	40	K2AF	8	931	224	1861	112	3722	56	7444	28

Table 3-5. Occupied Cell Ranges (8/8)

High-Density 2-Port RAM (W+R) (40% Cell Utilization)

RAM Type	Words	Bits	Basic RAM	Quantity	Cell Area Occupied by RAM							
					TypeA		TypeB		TypeC		TypeD	
					X	Y	X	Y	X	Y	X	Y
R947	16	4	K247	1	114	14						
R949	32	4	K249	1	208	14						
R94B	64	4	K249	2	208	28	416	14				
R94D	128	4	K24D	1	446	21						
R94F	256	4	K24D	2	446	42	891	21				
R94H	512	4	K24D	4	446	84	891	42	1783	21		
R94M	1024	4	K24D	8	446	168	891	84	1783	42	3566	21
R94S	2048	4	K24D	16	446	336	891	168	1783	84	3566	42
R94U	4096	4	K24D	32	446	672	891	336	1783	168	3566	84
R987	16	8	K247	2	114	28	228	14				
R989	32	8	K249	2	208	28	416	14				
R98B	64	8	K28B	1	433	48						
R98D	128	8	K24D	2	446	42	891	21				
R98F	256	8	K28F	1	893	28						
R98H	512	8	K28F	2	893	56	1786	28				
R98M	1024	8	K28M	1	1842	50						
R98S	2048	8	K28M	2	1842	100	3685	50				
R9AB	64	10	K2AB	1	533	18						
R9AD	128	10	K2AB	2	533	36	1067	18				
R9AF	256	10	K2AF	1	1047	28						
R9AH	512	10	K2AF	2	1047	56	2094	28				
R9AM	1024	10	K2AM	1	2294	50						
R9AS	2048	10	K2AM	2	2294	100	4587	50				
R9C7	16	16	K247	4	114	56	228	28	456	14		
R9C9	32	16	K249	4	208	56	416	28	833	14		
R9CB	64	16	K28B	2	433	36	867	18				
R9CD	128	16	K24D	4	446	84	891	42	1783	21		
R9CF	256	16	K28F	2	893	56	1786	28				
R9CH	512	16	K28F	4	893	112	1786	56	3571	28		
R9CM	1024	16	K28M	2	1842	100	3685	50				
R9EB	64	20	K28B	2	433	36	867	18				
R9ED	128	20	K2AB	4	533	72	1067	36	2133	18		
R9EF	256	20	K2AF	2	1047	56	2094	28				
R9EH	512	20	K2AF	4	1047	112	2094	56	4188	28		
R9EM	1024	20	K2AM	2	2294	100	4587	50				
R9H7	16	32	K247	8	114	112	228	56	456	28	911	14
R9H9	32	32	K249	8	208	112	416	56	833	28	1666	14
R9HB	64	32	K28B	4	433	72	867	36	1733	18		
R9HD	128	32	K24D	8	446	168	891	84	1783	42	3566	21
R9HF	256	32	K28F	4	893	112	1786	56	3571	28		
R9HH	512	32	K28F	8	893	224	1786	112	3571	56	7143	28
R9KB	64	40	K28B	4	433	72	867	36	1733	18		
R9KD	128	40	K2AB	8	533	144	1067	72	2133	36	4267	18
R9KF	256	40	K2AF	4	1047	112	2094	56	4188	28		
R9KH	512	40	K2AF	8	1047	224	2094	112	4188	56	8375	28

3.1.4 Placement considerations for cell-based IC type memory

Refer to the **EA-9HD Series Memory Macro Design Manual (A13367E)** for the cell-based IC-type memory size.

Furthermore, since the cell-based IC-type memory is created from the base, examine the bit/word configuration (the memory size cannot be changed after the base is created).

Determine whether it is possible to include macros or not using the following formulas.

(Number of RAM macro X direction cells) ≤ (Number of base X direction cells before cutout) – (32 cells)

(Number of RAM macro Y direction cells) ≤ (Number of base Y direction cells before cutout) – (4 cells)

3.1.5 Usable cells and pin-pair count limit (outside large-scale macros (such as memory))

The number of usable logic gates is calculated by subtracting the gate count occupied by the cell-based IC-type RAM macros from the total number of gates available in the master.

(Number of gates that can be packed in the logic unit) = (Number of master on-chip gates) – Number of gates taken up by cell-based IC-type RAM macros

The number of logic unit usable gates is defined as shown below corresponding to the number of gates taken up by cell-based IC-type RAM macros.

	Macro Utilization Rate < 50 %	Macro Utilization Rate > 50 %
RAM BIST unit utilization rate	Standard cell utilization rate	Standard cell utilization rate –5%
Logic unit cell utilization rate		

Because routing over the memory blocks is not possible routing also depends on the total area occupied by the memory blocks. Routing resources decrease as the number of RAM blocks utilized increases. Also, the pin-pair limit changes accordingly.

Calculate the number of cells usable for gates other than the large-scale macros (such as memory) by using the following equations.

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.60

Because the total cell utilization rate changes when large-scale macros (such as memory) are placed, the pin-pair count limit also changes.

Cell utilization rate = (number of usable cells + number of cells used for all macros)/number of raw cells × 100

Pin-pair count = 112 × number of raw cells × {(100 – cell utilization rate)/100} ^{2} / 74.69

3.1.6 Notes on placing large-scale macros (such as memory)

The following points must be noted when using large-scale macros:

- External pin placement
- Block type used for circuits other than macros

(1) External pin placement

Place related external pins close to macros if two or more large-scale macros are placed. If no consideration is given to pin placement, the wiring of external pins is long, wasting routing channels. As a result, routing may not be completed. When placing two or more large-scale macros, consult NEC Electronics for macro placement method.

(2) Block type used for circuits other than macros

When the number of cells that can be used for logic is reduced because of large-scale macros, medium-scale macros, such as 8-bit latches, may not fit in the available space.

3.2 Package Selection

The EP-1 series provides a different package for each master. Select the best-suited package based on the number of I/O pins in the circuit specifications.

The number of I/O pins and power supply pins of the EP-1 Series may vary, depending on the master used.

Since the location of the power supply pins and the number of signal pins differs according to the package, please check with NEC Electronics. For a list of the packages, refer to **CHAPTER 11 PACKAGES**.

3.3 Verifying Power Consumption

Although the power consumption of the gate array block is low, a considerable amount of power will be consumed when it is operated at a high speed (for example, at 50 MHz or faster). Because the temperature of the LSI increases with the amount of power used and the functionality of the product is not guaranteed as the temperature increases beyond the maximum values specified here, it is necessary to hold the power consumption of the LSI below a maximum.

For an EP-1 Series LSI, the power consumption of both the PFESiP/V850EP1 and gate array must be taken into consideration. For the power consumption of the PFESiP/V850EP1, see the **PFESiP/V850EP1 Product Data User's Manual (A19069E)**. For the power consumption of the gate array, see **5.3 Power Consumption**.

The limit of power consumption is determined, according to the package used. Take the power consumption of both the PFESiP/V850EP1 and gate array into consideration and select an optimal package. For details, refer to **CHAPTER 11 PACKAGES**.

3.4 Pin Placement

The power supply pin positions and NC pin positions of the package, and the pins related to the PFESiP/V850EP1 are predetermined. The user pins of mainly the gate array block are to be determined by the customer. The points noted below must be considered in determining pin layout (pin placement).

There are cases where the power requirement will increase, depending on the results of investigating items such as the number of simultaneous operation output pins.

For details, refer to **CHAPTER 11 PACKAGES**.

3.4.1 Notes on pin placement

(1) Clock pins, control (set, reset) pins

Because these pins are subject to noise, they must be placed close to ground (GND) pins.

(2) Output pins

Because output pins are subject to clock pin noise, they should be isolated as much as possible. If a large group of output pins has many simultaneous operation pins, the group should be surrounded by V_{DD} and GND pins.

(3) NC pins (No Connection)

When an embedded array is mounted on a printed circuit board, do not use an NC (no connection) pin as a signal relay pin. Some NC pins are actually connected to the pads of the chip. Connect the NC pins to ground (GND) or V_{DD}.

(4) Scan path and boundary scan I/O pins

The boundary scan test is required in PFESiP/V850EP1. The placement of test pins for each package is predetermined.

If scan path test is used, the I/O pins can be shared with the pins for the boundary scan test.

For details, see **NEC SYSTEM LSI DESIGN Design For Test User's Manual (A15168E)**.

(5) Digital PLL (digital phase locked loop) pin placement

There are no physical limits for pin placement. However, to sufficiently draw out the capabilities of digital PLLs, it is necessary to study pin placement, including the placement of PLL macros. NEC Electronics should be consulted regarding pin placement.

Applicable blocks: F9E4, F9H2, F9H3, F9H4SSCG, FI0P, FI0Q

(6) Placing oscillator block

For the locations where the oscillation block can be placed, refer to **CHAPTER 11 PACKAGES**.

Do not place pins that may malfunction when noise is superimposed on them (such as a reset pin) in the vicinity of the oscillator pins.

(7) Mode setting pin

<R> TMC1_GA and TMC2_GA pins are reserved for the test of NEC Electronics. (It is not necessary to count the number of the user pins.)

Since the reserved pins are not required for customer circuit design, please keep the pins unconnected without processing them.

Please connect the pins to GND on the printed circuit board for actual use.

<R> **(8) Providing the files for pin placement evaluation**

NEC Electronics offers the following two files to evaluate the pin placement for the customer use. Please consult with NEC Electronics for your file.

- Padinfo files to evaluate pin placement for the customer (Excel)
- Padinfo files to generate gate array DIF (Pin Assignment information) (Excel)

3.5 Gate Array I/O Interface

Connect to the user pins of the gate array appropriate I/O blocks according to the desired I/O interface.

3.5.1 Input blocks

Signal Level
LVTTL
5 V tolerant
5 V full-swing

Function
Buffer
Fail Safe

Input Format
Normal
Schmitt trigger

Pull-Up/Pull-Down Resistor
No resistor
With 50 kΩ pull-up resistor
With 5 kΩ pull-up resistor
With 50 kΩ pull-down resistor

Signal Level	Function	Input Format
GTL+	Open-drain	Normal

Signal Level	Function	Input Format
LVTTL	Digital PLL	Special

There are four types of input interface blocks:

<1> LVTTL input level block

This block connects a 3.3 V input signal to the LSI. Blocks with fail-safe functions are also available. A block with a fail-safe function has a protection function against excess voltage. There is no continuity to the embedded array power supply when the embedded array power supply voltage is in the OFF state, even if a signal is applied.

<2> 5 V tolerant input block

This block connects a 5 V input signal to the LSI.

<3> 5 V full-swing input block

5 V output can be performed by providing a 5 V power supply.
Shared use with the 3.3 V interface is possible, allowing the realization of a dual power supply for the interface.

<4> GTL+

Because GTL+ (gunning transceiver logic; small amplitude interface) is a differential circuit, similar to ECL, it can accept super high-speed signals.

In addition, a digital PLL (digital phase locked loop) is also available for minimizing the clock skew between chips.

3.5.2 Output blocks

Signal Level	Function	Output Format	Pull-Up/Pull-Down Resistor	Load Drive Capability I_{OL}
LVTTL	Buffer	Normal	No resistor	1.0 mA
5 V tolerant	3-state	Low noise	With 50 kΩ pull-up resistor	2.0 mA
5 V full-swing	Open-drain	TTL/CMOS	With 5 kΩ pull-up resistor	3.0 mA
			With 50 kΩ pull-down resistor	6.0 mA
				9.0 mA
				12.0 m

Signal Level	Function	Output Format	Pull-Up/Pull-Down Resistor	Load Drive Capability I_{OL}
GTL+	Open-drain	Normal	No resistor	1.0 mA

There are four types of output interface-level blocks:

<1> LVTTL output interface block

This block connects a 3.3 V input signal to the LSI.

<2> 5 V tolerant output interface block

This block outputs a 5 V signal from the LSI. There are two types, CMOS and TTL. The CMOS block must be clamped with a pull-up resistor, the same as for an open-drain output. Also, the TTL block supports 5 and 3.3 V LSIs that drive the embedded array.

<3> 5 V full-swing output block

5 V output can be performed by providing a 5 V power supply.

<4> GTL+

The GTL+ output part is an open-drain buffer with enable function.

In addition, a low-noise type buffer for holding down generated noise is also available. The output drive capability I_{OL} is equal to I_{OH}. The following types of buffers are available:

- LVTTL output buffer (Normal type: 6 types, low-noise type: 5 types)
- TTL 5 V tolerant output buffer (Normal type: 8 types, low-noise type: 3 types)
- CMOS 5 V tolerant output buffer (Normal type: 6 types, low-noise type: 3 types)
- 5 V full-swing buffer for TTL (Normal type: 4 types, low-noise type: 2 types)
- 5 V full-swing buffer for CMOS (Normal type: 10 types, low-noise type: 5 types)

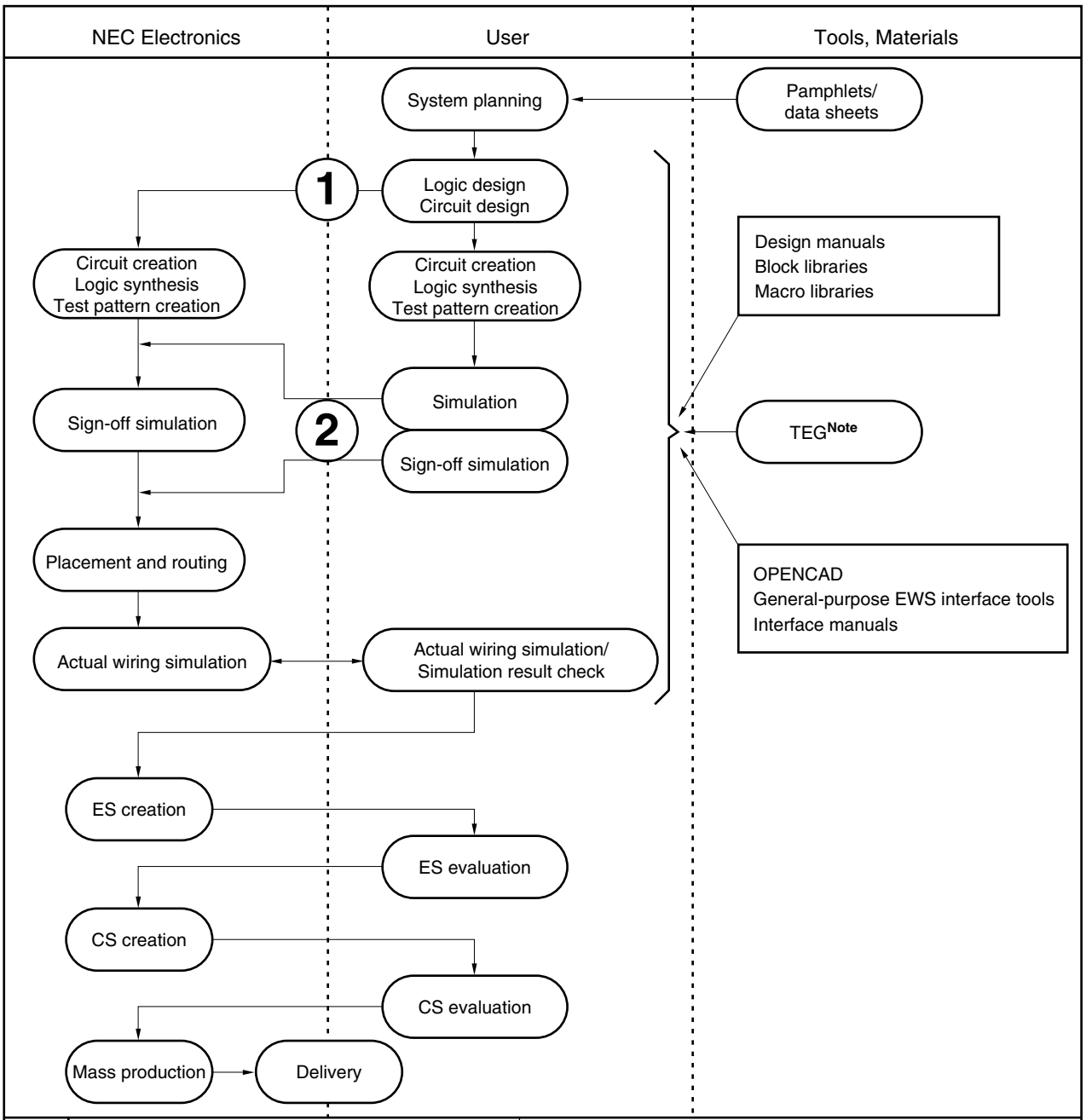
If an input signal is at a floating level in a CMOS circuit, excessive current will flow, and noise will affect the circuit, resulting in possible malfunction. A buffer with a pull-up or pull-down resistor must be used for pins whose level may float in the circuit board.

Use an 18 mA or a 24 mA type low-noise buffer as the output buffer of the EP-1 series gate array block.

3.6 Gate Array Development Flow

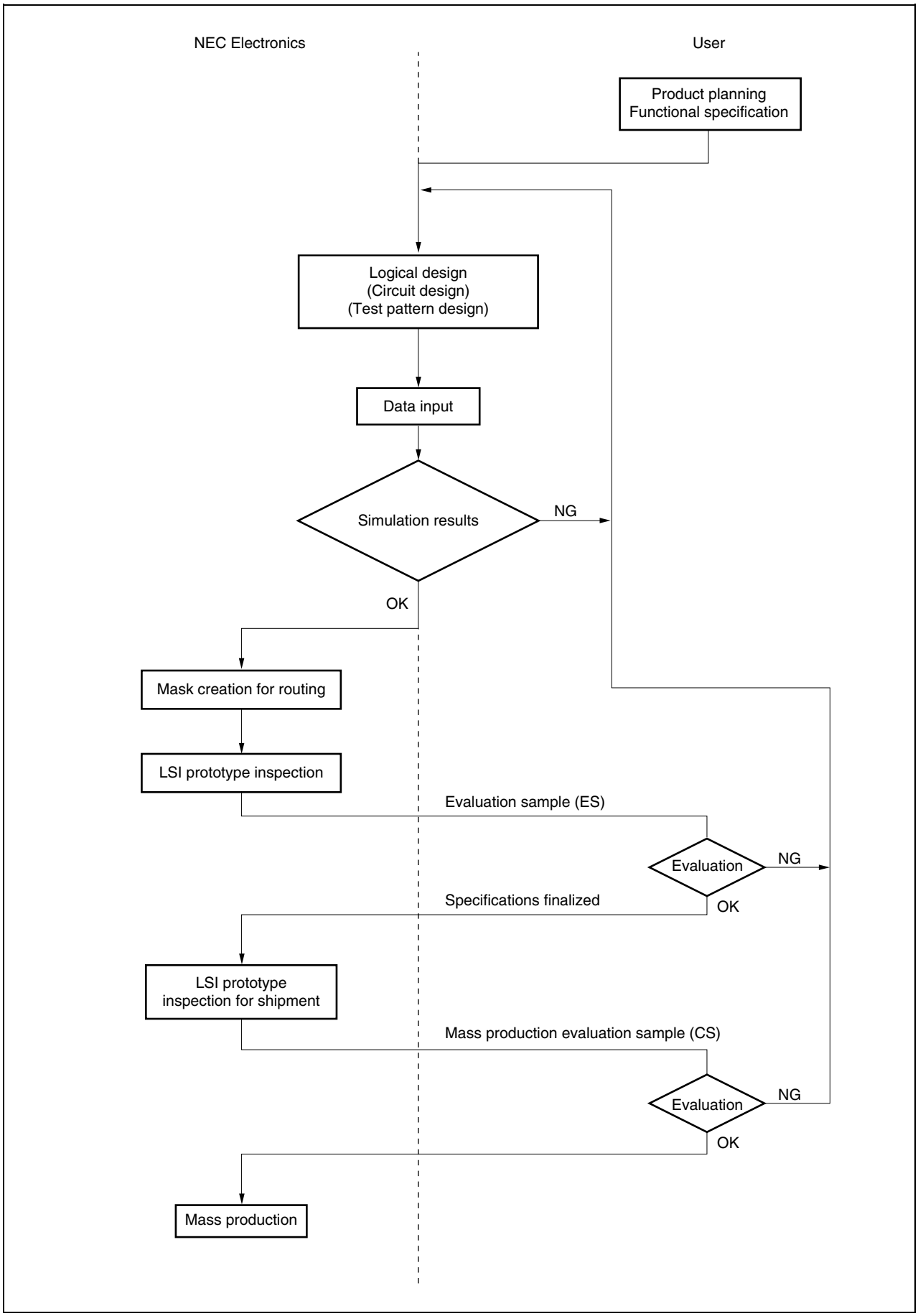
The following figure shows the development flow of a gate array.

Flow 1: Development procedure and interfacing

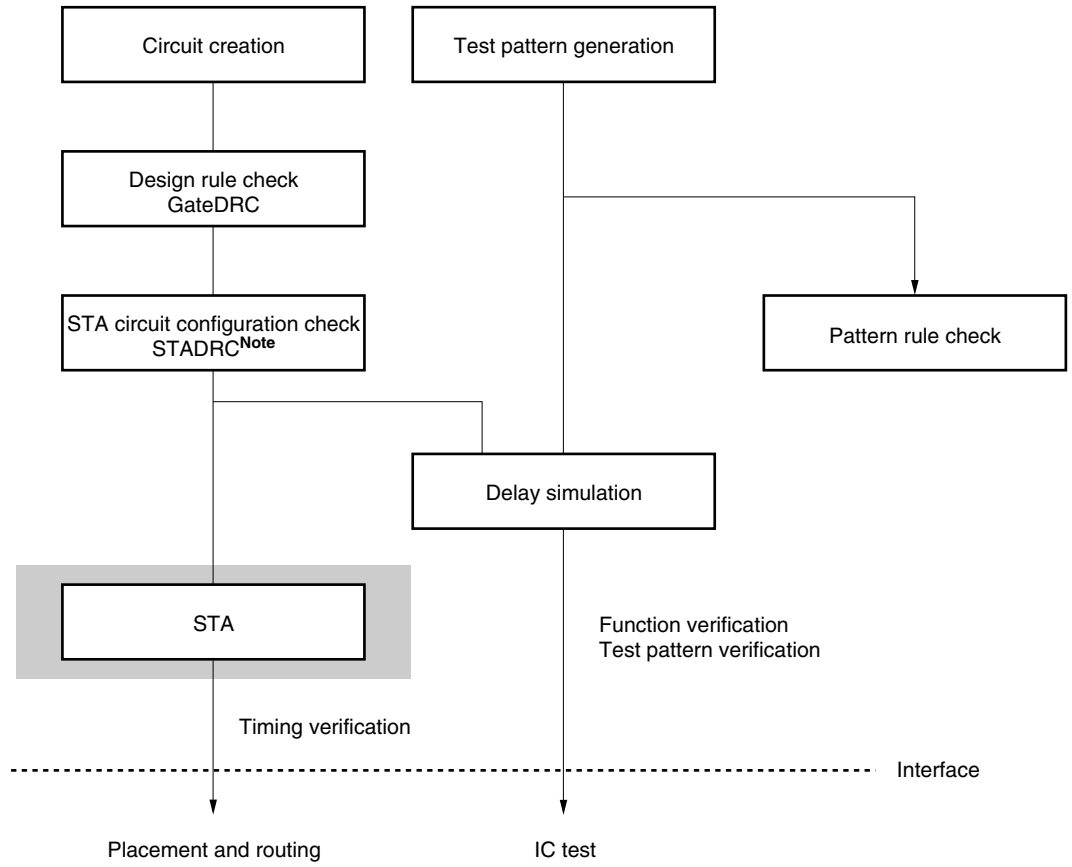


1	Circuit diagram level interface	
2	Simulation level interface	• When using NEC Electronics' sign-off simulator, placement and routing is performed immediately after user confirmation. If another simulator is used, simulation will be executed again by NEC Electronics.

Flow 2: Development flow



Flow 3: Front-end detailed flow



Note STADRC is required only when sign-off is performed by STA.

3.7 OPENCAD Configuration Tools

Caution Refer to the user's manuals in the OPENCAD Series for the latest versions of the OPENCAD configuration tools.

The following tools can be selected in accordance with the user environment.

Function	NEC Electronics Tools	I/F Data	Commercial Tool I/F
Function simulator	–	• Netlist PWC/EDIF(2.0.0)/ Verilog HDL • Test pattern ALBA • Delay data file • Constraint file	ModelSim™/Verilog-XL™/ NC-Verilog®/VCS®
Schematic editor	Vdraw		-
Logic synthesis	-		Design Compiler®
Gate level simulator Note 1	V.sim		ModelSim/Verilog-XL/ NC-Verilog/VCS
Formal verifier	-		Formality®/Tuxedo™-LEC /Conformal™-LEC
STA Note 1	Tiara		PrimeTime®
Fault simulator Note 2	C.FGRADE		-
Design for test	NEC_SCAN/NEC_BSCAN/ NEC_BIST/ TESTBUS		DFTCompiler/TetraMax®
Floor planner Note 3	CBIC:ace_floorplan GA:Galet		-
Placement and wiring Note 3	Galet		Silicon Ensemble™

Notes 1. Sign-off tool

2. Tool not supported in HPTM version

3. Stand-alone tool

Remark Platform: SUN™ (Solaris™)/HP (HP-UX™)/RedHat™ Enterprise Linux™
GUI : X11R5/Motif™1.2

Embedded array development is a cooperative effort by the user and NEC Electronics. The user is responsible for the steps from system and circuit design through simulation. NEC Electronics is responsible for providing design information, supporting the user in designing the circuit, and the steps after simulation.

The transfer of development work from the user to NEC Electronics is called interfacing. The interface level is divided into the following two depending on what data is to be provided from the user to NEC Electronics.

(1) Circuit diagram level interface

A circuit diagram designed with 74LS or NEC Electronics' embedded array blocks is submitted to NEC Electronics and NEC Electronics performs the steps after circuit simulation.
NEC Electronics will provide the user with the results of design rule checking and circuit simulation, which must be confirmed and approved by the user.

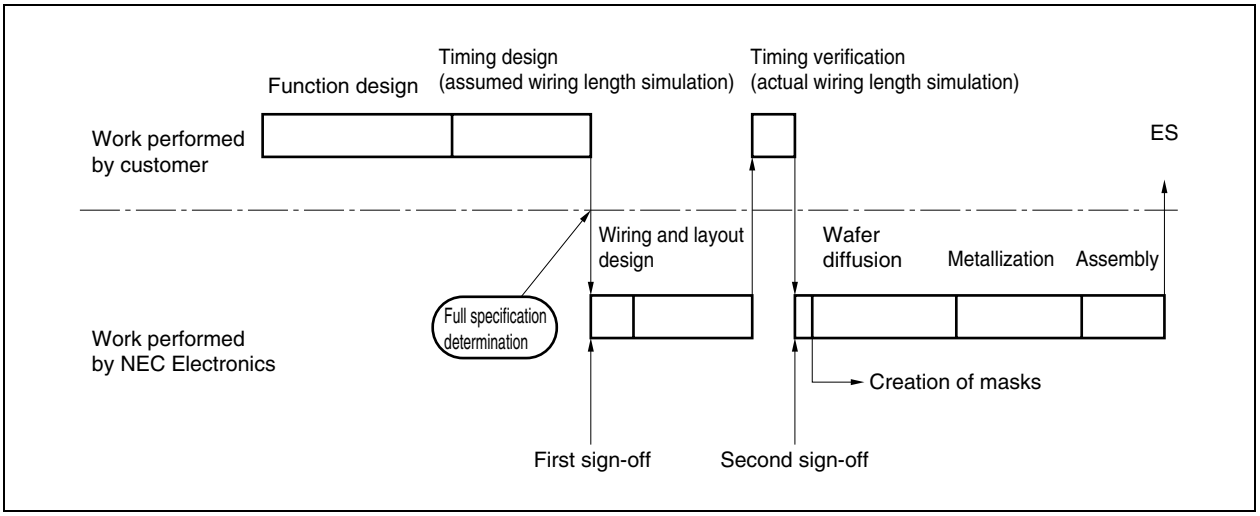
(2) Simulation level interface

The user performs circuit design and simulation work using various EWS (engineering work stations) and CAD system simulators, and NEC Electronics takes over the rest of the development work (such as automatic placement and routing and final simulation).

At either interface level, the user may consult NEC Electronics about items NEC Electronics has provided, as well as which tools are presently available.

3.8 Sign-off Conditions and Data to be Passed

Sign-off conditions are the conditions for accepting design data that is submitted to NEC after verification has been done via simulations. After the assumed wiring length delay simulation is completed, there is a first sign-off that comes immediately before wiring layout. After the actual wiring length simulation is completed, there is a second signoff that comes immediately before creation of masks. The design data that is submitted for the first sign-off is called the CF1 (clean file 1) data and the design data for the second sign-off is called the CF2 (clean file 2) data.



3.8.1 Basic conditions for sign-offs

The basic conditions for sign-offs are explained below.

[First sign-off]

(1) Make sure there are no critical errors in the design rule check program (except for pseudo errors, such as an all output operation error used when a dummy gate is implemented, which have already been confirmed as OK).

(2) Make sure that a netlist and test patterns have been prepared and checked the next item via a assumed wiring length delay simulation using the sign-off simulator.

<1> Make sure there were no mismatches with expected values or timing errors during simulations using maximum and minimum conditions (except for pseudo errors that have been confirmed as OK via actual operations and tests).

- Test patterns to be submitted to NEC should be prepared using a cycle period (rate) of 200 ns if possible without causing problems. Also, verification should also be done via simulation using actual operation conditions.

  [Check items]

  - Function check
  - Setup/hold time check
  - Release/removal time check
  - Minimum pulse width check
  - Bus conflict/bus float check

(3) If any cores have been implemented, perform a separate simulation for the cores and make sure there are no mismatches. If a RAM macro has been implemented, check access while in separate test mode to make sure there are no problems in the test circuit.

[Second sign-off]

(1) Check for the following items when performing an actual wiring length simulation using the sign-off simulator.

<1> Make sure that there were no mismatches with expected values or timing errors during the simulations using maximum and minimum conditions (except for pseudo errors that have been confirmed as OK via actual operations and tests).

- Also, be sure to perform simulations using actual operation conditions to confirm the test patterns to be submitted to NEC.

<2> When there is a critical path, confirm that the required values are met.

3.8.2 Data required for interface

(1) Data submitted for first sign-off

<1> Netlist that meets the conditions for the first sign-off

[Format]

- PWC [Note] or EDIF

<2> Design rule check confirmation results (LOG file)

<3> Test patterns that meet conditions for sign-off

[Format]

Use the following combination.

Test pattern	Timing data
NELPAT [Note]	Timing ALBATROSS file

Note This is NEC's original format.

[Test pattern types]

The following data from simulation under maximum conditions.

- Test patterns for separate test verification of user macro
- Total chip simulation patterns (chip level)
- Test patterns for confirming ROM code (when ROM macro has been implemented)
- Test patterns for separate test verification of cores (when a core has been implemented)
- Access patterns for verification of separate RAM macro (when RAM macro has been implemented)

Related register files

Remark Be sure to prepare either one test pattern for separate test verification of user macro or one test pattern for total chip simulation as a test pattern that meets the DC test conditions.

<4>ROM code data and support data for code and macro (when a ROM macro has been implemented)

[Format]

- NINCF [Note] or Verilog format (HEX display)

[Support information]

- ROM block name, instance name (such as CS00 **** for PWC format), ROM code file name, and ROM code header name

Note This is NEC's original format.

<5> Assumed wiring length simulation LOG file

- LOG file contains simulation results for various test patterns under maximum and minimum conditions (logging of execution under maximum conditions only is accepted for separate simulations of core and memory macro blocks, as long as there are no "Delay Over Period" errors).

<6> Other data

- ASIC product development information (checksheet) (contains items up until completion of CF1)
  Be sure to check with NEC Electronics whether the ASIC product development information (checksheet) you are planning to use is the latest version. For details, refer to **EA-9HD Series Design Manual (A13282E)**.
- Critical path instructions (only if required)
- Glitch/noise troubleshooting instructions (only if required)
- Simulation result confirmation instructions (before placement and routing)

- Results of investigation into special requirements (only if required)

(2) Data submitted for second sign-off

<1> LOG files of actual wiring length simulations

[Types]

- LOG file contains simulation results for various test patterns under maximum and minimum conditions (must conform to cycle periods of test patterns submitted to NEC).

<2> Other data

- Simulation result confirmation instructions (after placement and routing)
- Product requirement specifications (only if revisions were made after first sign-off)
- Check list (contains items up until completion of CF2)
- Critical path instructions (only if required)
- Glitch/noise troubleshooting instructions (only if required)
- Results of investigation into special requirements (only if additional investigation was done after first sign-off)

3.8.3 List of interface data

Caution There may be changes to the data depending on the edition of OPENCAD, so be sure to contact NEC Electronics before commencing design.

Rev.2.1 19 July '02

			File Type and Name	SIMULATOR							
				V.sim			Verilog				
NETLIST			PWC (.pwc)	√Note2			√Note2				
			VerilogHDL (.v)	–			√Note2				
			EDIF (.edif)	√Note2			√Note2				
TEST Pattern	Without IO Modulation specification		ALBATROSS (.alb)	√			√				
	With IO Modulation specification		ALBATROSS (.alb) Note1	√			√				
MACRO	RAM	BIST	RAMPIN file (.rpi)	▲			▲				
			BIST separate file (.bist.scn) (when used with SCAN)	▲			▲				
	ROM		NINCF (.nin)	▲			▲				
	Mega Macro		Megamacro Single Unit Test Specification	▲Note3			▲Note3				
			PINF file (.pinf)	▲Note3			▲Note3				
			Initial Pattern	▲			▲				
	Digital PLL		Initial Pattern	▲			▲				
DFT	BSCAN		SCAN+BSCAN Initial Pattern (scan.init.alb)	▲			▲				
			SET file (.set)	▲			▲				
			Circuit verification pattern (.bspat.alb)	√			√				
			Order file (.bsorder)	▲			▲				
			BSDL file (.bsdl)	▲			▲				
	SCAN		User macro separate file	▲			▲				
			Pin location file	▲			▲				
Other (Layout guideline)	Pin Assign		DIF (.dif)	√			√				
	CLITICAL PATH		tiara comand file	▲			▲				
			Critical Path Guidelines (Paper)	▲			▲				
	Floorplan		Floorplan specification document (Paper)	▲Note4			▲Note4				
			Def file (.floorplan.def)	▲Note4			▲Note4				
	CTS		CTS Check report (.rpt)	√			√				
	Power supply separation information		-	▲			▲				
	Delay adjustment request between clocks		-	▲			▲				
Check result file	Netlist rule check		(.gatedrc)	√			√				
	alb check (.ALBchk)		PIN check "NO ERR" screen copy	√			√				
	SCAN check (.scanchk)		BSCAN check (.bscanchk)	√			√				
	alb check (.ALBchk)		PIN check "NO ERR" screen copy	▲			▲				
	SCAN check (.scanchk)		BSCAN check (.bscanchk)	▲			▲				
	Sim result MIN. & MAX. (Fraction of pattern number)			.slg	.tpe	Note5	.log	.bus	.ovprd	Note5	.tpe
			DC test pattern (up to 32 K patterns)	√Note4	√Note4	√Note4	√Note4	√Note4	√Note4	√Note4	√Note4
			Function test pattern	▲	▲	▲	▲	▲	▲	▲	▲
			High-speed function test pattern	▲Note6	▲Note6	▲Note6	▲Note6	▲Note6	▲Note6	▲Note6	▲Note6
TESTACT	DFT database file		(dft_db)	▲			▲				
	DFT database file		(dft-set)	▲			▲				
	Test bus connection verification patterns		testbus.cpt	▲			▲				
	BSCAN circuit verification patterns		bspat.cpt	▲			▲				

Remark √: Required, ▲: When necessary

Note 1. Be aware that I/O Modulation is described on TIMING in ALBATROSS.

2, 3. Select one for each.

4, 6. Required if high-speed function test is requested. If the number of DC test patterns exceeds 32 K, the first 32 K patterns are for DC measurement and the rest are for function testing.

5. .iomoduchk

C3 I/F OPC V4.5	Metalization wafer	indef/OpenCAD.env/PIASS-E/PWCE/cts.pwc/nlef/embed.lef/merge.def/ outdef/po_psd2psd*.rpt/verify.jnl/ga_galetrc.pwc/ga_galet.lseq/ pathdelay.vsim.al (for V.sim)/verilog.sdf (for Verilog)/ eco.jnl (lapse FILE upon ECO execution)/CXPWC.eco (upon ECO execution)/ outdef.eco (upon ECO execution)/sim result (.trc)
	Base wafer	embed.lef/embed.def/embed.lsq/PROUTE.mac/OpenCAD.env/PWCE ga_embed.sum/nlef/indef
C3 I/F OPC V5.0 or later	Metalization wafer	to .route.pwc/ to .route.def/ to .route.rc.pwc/ to .route.netmerge.def/ to .route.netmerge.pwc/ to .route.merge_rc.pwc/ to .route.lseg/ to .hier.pr.Universal.sdf/ to .ctsinfor/OpenCAD.env/galet.nlef/ galet.verify.jnl/eco.jnl (upon ECO execution)/sim result (.trc)
	Base wafer	to .embed.def/ to .embed.gds/ to .embed.lef/galet_proute.mac/galet.nlef

Remarks 1. to CIRCUIT name

2. When the base wafer is ordered in advance, the metalization wafer data is unnecessary.

3. Contact NEC Electronics when usage conditions are as follows for the C3 I/F.

Usage conditions: When PFESiP/V850EP1 and cell-based IC are used with SCAN incorporated.

CHAPTER 4 PRODUCT SPECIFCATIONS

4.1 Terminology

Table 4-1. Terminology for Absolute Maximum Ratings

Item	Symbol	Definition
Power supply voltage	V_{DD} Note	Range of voltages which will not damage or reduce reliability when applied to the V_{DD} pin.
Input voltage	V_I	Range of voltages which will not damage or reduce reliability when applied to the input pin.
Output voltage	V_O	Range of voltages which will not damage or reduce reliability when applied to the output pin.
Input current	I_I	Maximum current which will not cause latchup when applied to the input pin.
Output current	I_O	Maximum DC current which will not cause damage or reduce reliability when flowing to or from the output pin.
Operating temperature	T_A	Range of ambient temperatures for normal logical operation.
Storage temperature	T_{stg}	Range of element temperatures which will not damage or reduce reliability in the state where neither voltage nor current is applied.

Note This is V_{DD33} for a 3.3 V power supply.

Table 4-2. Terminology for Recommended Operating Conditions

Item	Symbol	Definition
Power supply voltage	V_{DD} Note	Range of voltages for normal logical operation when V_{SS} = 0 V.
High-level input voltage	V_{IH}	For voltage applied to the input of gate array, this value indicates the voltage of the high-level state in which the input buffer operates normally. ● If voltage greater than the MIN. value is applied, the input voltage is assured to be high level.
Low-level input voltage	V_{IL}	For voltage applied to the input of the gate array, this value indicates the voltage of the low-level state in which the input buffer operates normally. ● If a voltage less than the MAX. Value is applied, the input voltage is assured to be low level.
Positive trigger voltage	V_P	Input level that inverts the output level when the input of gate array is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Input level that inverts the output level when the input of gate array is changed from the high-level side to the low-level side.
Hysteresis voltage	V_H	Difference between the positive- and negative-trigger voltage.
Input rise time	t_{ri}	Limit value for the rise time from 10% to 90% of the input voltage applied to the input of gate array.
Input fall time	t_{fi}	Limit value for the fall time from 90% to 10% of the input voltage applied to the input of gate array.

Note This is V_{DD33} for a 3.3 V power supply.

Table 4-3. Terminology for DC Characteristics

Item	Symbol	Definition
Static current consumption	I_{DDS}	In the state where there is no voltage change in the input and output pins, indicates the current that flows in from the power supply pin at the specified power supply voltage.
OFF state output current	I_{OZ}	For a 3-state output, this value indicates the current that flows through the output pin at the specified voltage when the output is at high impedance.
Output short-circuit current	I_{OS}	Current that flows out if the output pin is short-circuited to GND when output is at the high level.
Input leakage current	I_I	Current that flows through the input pin when voltage is applied to the input pin.
Low-level output current	I_{OL}	Current that flows to the output pin at the specified low-level output voltage.
High-level output current	I_{OH}	Current that flows from the output pin at the specified high-level output voltage.
Low-level output voltage	V_{OL}	Output voltage when output is open in the low-level state.
High-level output voltage	V_{OH}	Output voltage when output is open in the high-level state.

4.2 Product Specifcations (EP-1 Series)

This chapter describes the product specifications of the EP1 Series gate array.

See the **PFESiP/V850EP1 Product Data User's Manual (A19069E)** for the product standards of EP-1 Series-dedicated microcontroller PFESiP/V850EP1 which makes the EP-1 Series. See **4.3 Product Specifcations (Gate Array)** for the product standards of the gate array which makes the same EP-1 Series.

4.2.1 Absolute maximum rating value (EP-1 series)

Table 4-4. Absolute Maximum Rating Values

Item	Symbol	Conditions	Ratings	Unit
Power supply voltage	VD15	1.5 V system	-0.5 to +2.0	V
Power supply voltage	VD33	3.3 V system	-0.5 to +4.6	V
Power supply voltage	VD50	5.0 V system	-0.5 to +6.0	V
Input/Output voltage	V_I/V_O	3.3 V buffer, V_I/V_O < VD33 + 0.5 V	-0.5 to +4.6	V
Input/Output voltage	V_I/V_O	5 V tolerant buffer, V_I/V_O < VD33 + 3.0 V	-0.5 to +6.6	V
Input/Output voltage	V_I/V_O	5.0 V buffer, V_I/V_O < VD50 + 0.5 V	-0.5 to +6.0	V
Output current	I_O	I_{OL} = 1 mA Type	3	mA
Output current	I_O	I_{OL} = 2 mA Type	7	mA
Output current	I_O	I_{OL} = 3 mA Type	10	mA
Output current	I_O	I_{OL} = 6 mA Type	20	mA
Output current	I_O	I_{OL} = 9 mA Type	29	mA
Output current	I_O	I_{OL} = 12 mA Type	40	mA
Output current	I_O	I_{OL} = 18 mA Type	58	mA
Output current	I_O	I_{OL} = 24 mA Type	75	mA
Operating ambient temperature	T_A		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

4.2.2 Recommended operating range (EP-1 series)

Table 4-5. Recommended operating range

Item	Symbol	Conditions		MIN	TYP	MAX	Unit
Power supply voltage	VD15	1.5 V		1.35	1.5	1.65	V
Power supply voltage	VD33	3.3 V		3.0	3.3	3.6	V
Power supply voltage	VD50	5.0 V**Note**		4.5	5.0	5.5	V
High-level input voltage	V_{IH}	LVTTL input buffer		2.0		VD33	V
Low-level input voltage	V_{IL}	LVTTL input buffer with fail-safe function		0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.4		2.4	V
Negative trigger voltage	V_N			0.8		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	TTL 5 V tolerant input buffer		2.0		5.5	V
Low-level input voltage	V_{IL}			0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.4		2.4	V
Negative trigger voltage	V_N			0.8		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	5 V full-swing input buffer for CMOS		0.7 VD50		VD50	V
Low-level input voltage	V_{IL}			0		0.3 VD50	V
Positive trigger voltage	V_P		Schmitt input	1.8		4.0	V
Negative trigger voltage	V_N			0.6		3.1	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	TTL 5 V full-swing input buffer		2.2		VD50	V
Low-level input voltage	V_{IL}			0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.2		2.4	V
Negative trigger voltage	V_N			0.6		1.8	V
Hysteresis voltage	V_H			0.3		1.5	V
Input rise time	t_{ri}	Normal input		0		200	ns
Input fall time	t_{fi}			0		200	ns
Input rise time	t_{ri}	Schmitt input		0		10	ms
Input fall time	t_{fi}			0		10	ms

Note Only when 5 V full-swing buffer is provided.

Remark When inputting a slow signal with a long rise/fall time, noise on a signal line may affect the operation. Therefore, use a Schmitt trigger input buffer. Because fluctuation on the power supply line due to simultaneous operation of output buffers reduces the capability of the Schmitt trigger input buffer, carefully determine pin placement.

The EP-1 Series gate array has input/output interface blocks that can be connected not only to 3.3 V LSIs but also to conventional 5 V LSIs.

4.3 Product Specifcations (Gate Array)

4.3.1 Absolute maximum rating values (gate array)

Table 4-6. Absolute Maximum Rating Values

Item		Symbol	Conditions	Ratings	Unit
Power supply voltage		V_{DD33}	3.3 V	-0.5 to +4.6	V
		V_{DD50}	5.0 V Note	-0.5 to +6.0	V
Input voltage	LVTTL input buffer	V_I	$V_I < V_{DD33}$+0.5 V	-0.5 to +4.6	V
	LVTTL input buffer with fail-safe function		$V_I < V_{DD33}$+0.5 V	-0.5 to +4.6	V
	5 V tolerant input buffer		$V_I < V_{DD33}$+3.0 V	-0.5 to +6.6	V
	5 V full-swing buffer		$V_I < V_{DD50}$+0.5 V	-0.5 to +6.0	V
Output voltage	LVTTL output buffer	V_O	$V_O < V_{DD33}$+0.5 V	-0.5 to +4.6	V
	TTL 5 V tolerant output buffer		$V_O < V_{DD33}$+3.0 V	-0.5 to +6.6	V
	CMOS 5 V tolerant output buffer		$V_O < V_{DD33}$+3.0 V	-0.5 to +6.6	V
	5 V full-swing buffer		$V_O < V_{DD50}$+0.5 V	-0.5 to +6.0	V
Output current	I_{OL} = 1.0 mA	I_O	FV0A	3	mA
	I_{OL} = 2.0 mA		FV0B	7	mA
	I_{OL} = 3.0 mA		FO09, FV09, FY09	10	mA
	I_{OL} = 6.0 mA		FO04, FV04, FY04	20	mA
	I_{OL} = 9.0 mA		FO01, FV01, FY01	30	mA
	I_{OL} = 12.0 mA		FO02, FV02, FY02, FW02, FZ02	40	mA
	I_{OL} = 18.0 mA		FO03, FV03, FY03, FW03, FZ03	60	mA
	I_{OL} = 24.0 mA		FO06, FV06, FY06, FW06, FZ06	75	mA
Operating ambient temperature		T_A		-40 to +85	°C
Storage temperature		T_{stg}		-65 to +150	°C

Note Only when 5 V full-swing buffer is provided.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Except for buffers with a fail-safe function, 5 V or 3.3 V must be applied to the input pins only after applying the power supply voltage.

4.3.2 Recommended operating range (gate array)

Table 4-7. Recommended Operating Range

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD33}	3.3 V		3.0	3.3	3.6	V
	V_{DD50}	5.0 V[Note]		4.5	5.0	5.5	V
High-level input voltage	V_{IH}	LVTTL input buffer		2.0		V_{DD33}	V
Low-level input voltage	V_{IL}	LVTTL input buffer with fail-safe function		0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.4		2.4	V
Negative trigger voltage	V_N			0.8		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	5 V tolerant input buffer		2.0		5.5	V
Low-level input voltage	V_{IL}			0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.4		2.4	V
Negative trigger voltage	V_N			0.8		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	5 V full-swing input buffer for CMOS		0.7 V_{DD50}		V_{DD50}	V
Low-level input voltage	V_{IL}			0		0.3 V_{DD50}	V
Positive trigger voltage	V_P		Schmitt input	1.8		4.0	V
Negative trigger voltage	V_N			0.6		3.1	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	5 V full-swing input buffer for TTL		2.2		V_{DD50}	V
Low-level input voltage	V_{IL}			0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.2		2.4	V
Negative trigger voltage	V_N			0.6		1.8	V
Hysteresis voltage	V_H			0.3		1.5	V
Input rise time	t_{ri}	Normal input		0		200	ns
Input fall time	t_{fi}	(Data line)		0		200	ns
<R> Input rise time	t_{ri}	Normal input		0		4	ns
<R> Input fall time	t_{fi}	(Clock line)		0		4	ns
Input rise time	t_{ri}	Schmitt input		0		10	ms
Input fall time	t_{fi}			0		10	ms

Note Only when 5 V full-swing buffer is provided.

<R> **Remark** If a signal that rises or falls dully or a signal with noise exceeding the threshold value is to be input, use a Schmitt trigger input buffer because noise on the internal signal line of the chip may cause malfunctioning. Clock input in particular is easily influenced by noise, so that a separate recommended operating range is specified. If the rise or fall time increases beyond this range, likewise use a Schmitt trigger input buffer. Note that, if a noise exceeding the hysteresis voltage is input, malfunctioning may occur. Exercise care in laying out pins as fluctuation on the power supply due to simultaneous switching of output buffers degrades the capability of the Schmitt trigger input buffer.

4.3.3 DC characteristics (gate array)

Table 4-8. DC Characteristics (1/3)

Item			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption[Note1]	MC-10501/10505		I_{DDS}	$V_I = V_{DD33}$ or GND		1.0	200	μA
	MC-10502/10506			5 V full-swing buffer		2.0	400	μA
	MC-10503/10507			$V_I = V_{DD50}$ or GND		3.0	600	μA
OFF-state output current[Note 2]	LVTTL output		I_{OZ}	$V_O = V_{DD33}$ or GND			±10	μA
	TTL 5 V tolerant output						±10	μA
	CMOS 5 V tolerant output						±10	μA
	5 V full-swing output buffer for CMOS [Note 8]			$V_O = V_{DD50}$ or GND			±10	μA
	5 V full-swing output buffer for TTL[Note 8]						±10	μA
Output influx current[Note 3]	CMOS 5 V tolerant output		I_R	V_{PU} = 5.5 V, R_{PU} = 2 kΩ, V_O = 3.0 V			0.1	μA
Output short-circuit current[Note 4]			I_{OS}	V_O = GND			-250	mA
Input leakage current (3.3 V)	Normal input		I_I	$V_I = V_{DD33}$ or GND			±1.0	μA
	With pull-up resistor (50 kΩ)			V_I = GND	-28	-83	-190	μA
	With pull-up resistor (5 kΩ)			V_I = GND	-280	-700	-1900	μA
	With pull-down resistor (50 kΩ)			$V_I = V_{DD33}$	28	83	190	μA
Input leakage current (5.0 V) [Note 8]	Normal input			$V_I = V_{DD50}$ or GND			±10	μA
	With pull-up resistor (50 kΩ)			V_I = GND	-36	-145	-308	μA
	With pull-up resistor (5 kΩ)			V_I = GND	-300	-1163	-2750	μA
	With pull-down resistor (50 kΩ)			$V_I = V_{DD50}$	45	116	367	μA
3.3 V buffer	Pull-up resistor[Note5]	50 kΩ	R_{PU}	V_I = GND	18.9	39.8	107.1	kΩ
		5 kΩ		V_I = GND	1.9	4.7	10.7	kΩ
	Pull-down resistor[Note5]	50 kΩ	R_{PD}	$V_I = V_{DD33}$	18.9	39.8	107.1	kΩ
5 V full-swing buffer [Note 8]	Pull-up resistor[Note5]	50 kΩ	R_{PU}	V_I = GND	17.9	34.6	125.1	kΩ
		5 kΩ		V_I = GND	2.0	4.3	15.0	kΩ
	Pull-down resistor[Note5]	50 kΩ	R_{PD}	$V_I = V_{DD50}$	15.0	43.4	100.0	kΩ
Low-level output current[Note 6] (LVTTL output)	3.0 mA Type	FO09	I_{OL}	V_{OL} = 0.4 V	3.00[Note7]			mA
	6.0 mA Type	FO04			6.00			mA
	9.0 mA Type	FO01			9.00			mA
	12.0 mA Type	FO02			12.00			mA
	18.0 mA Type	FO03			18.00			mA
	24.0 mA Type	FO06			24.00			mA
Low-level output current[Note 6] (TTL 5 V tolerant output)	1.0 mA Type	FV0A		V_{OL} = 0.4 V	1.00			mA
	2.0 mA Type	FV0B			2.00			mA
	3.0 mA Type	FV09			3.00			mA
	6.0 mA Type	FV04			6.00			mA
	9.0 mA Type	FV01			9.00			mA
	12.0 mA Type	FV02			12.00			mA
	18.0 mA Type	FV03			18.00			mA
	24.0 mA Type	FV06			24.00			mA

Table 4-8. DC Characteristics (2/3)

Item			Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low-level output current[Note 6] (CMOS 5 V tolerant output)	3.0 mA Type	FY09	I_{OL}	V_{OL} = 0.4 V	3.00			mA
	6.0 mA Type	FY04			6.00			mA
	9.0 mA Type	FY01			9.00			mA
	12.0 mA Type	FY02			12.00			mA
	18.0 mA Type	FY03			18.00			mA
	24.0 mA Type	FY06			24.00			mA
Low-level output current[Note 6, 8] (5 V full-swing output buffer)	1.0 mA Type	FV0AAL		V_{OL} = 0.4 V	1.00			mA
	2.0 mA Type	FV0BAL			2.00			mA
	3.0 mA Type	FV09AL			3.00			mA
	6.0 mA Type	FV04AL			6.00			mA
	9.0 mA Type	FV01AL			9.00			mA
	12.0 mA Type	FV02AL			12.00			mA
	18.0 mA Type	FV03AL			18.00			mA
High-level output current[Note 6] (LVTTL output)	3.0 mA Type	FO09	I_{OH}	V_{OH} = 2.4 V	-3.00			mA
	6.0 mA Type	FO04			-6.00			mA
	9.0 mA Type	FO01			-9.00			mA
	12.0 mA Type	FO02			-12.00			mA
	18.0 mA Type	FO03			-18.00			mA
	24.0 mA Type	FO06			-24.00			mA
High-level output current[Note 6] (TTL 5 V tolerant output)	1.0 mA Type	FV0A		V_{OH} = 2.4 V	-1.00			mA
	2.0 mA Type	FV0B			-1.00			mA
	3.0 mA Type	FV09			-3.00			mA
	6.0 mA Type	FV04			-3.00			mA
	9.0 mA Type	FV01			-3.00			mA
	12.0 mA Type	FV02			-3.00			mA
	18.0 mA Type	FV03			-6.00			mA
	24.0 mA Type	FV06			-6.00			mA
High-level output current[Note 6, 8] (5 V full-swing output buffer)	1.0 mA Type	FV0AAL		V_{OH} = V_{DD50} - 0.4 V	-1.00			mA
	2.0 mA Type	FV0BAL			-2.00			mA
	3.0 mA Type	FV09AL			-3.00			mA
	6.0 mA Type	FV04AL			-6.00			mA
	9.0 mA Type	FV01AL			-9.00			mA
	12.0 mA Type	FV02AL			-12.00			mA
	18.0 mA Type	FV03AL			C18.00			mA
Low-level output voltage	LVTTL output Type		V_{OL}	**Note9**, I_{OL} = 6 mA (6 mA Type), V_{DD33} = min.			0.4	V
	TTL 5 V tolerant output						0.4	V
	CMOS 5 V tolerant output						0.4	V
	5 V full-swing output buffer[Note 8]			**Note9**, I_{OL} = 6 mA (6 mA Type), V_{DD50} = min.			0.4	V
High-level output voltage	LVTTL output type		V_{OH}	**Note9**, I_{OH} = -6 mA (6 mA Type), V_{DD33} = min.	2.4			V
	TTL 5 V tolerant output				2.4			V
	5 V full-swing output buffer[Note 8]			**Note9**, I_{OH} = -6 mA (6 mA Type), V_{DD50} = min.	V_{DD50}-0.4			V

Table 4-8. DC Characteristics (3/3)

Item		Symbol	Conditions	MIN	TYP	MAX	Unit
Low-level output voltage	LVTTL output type	V_{OL}	I_{OL} = 0 mA			0.1	V
	LVTTL output (with 5 kΩ pull-up resistor)					0.2	V
	TTL 5 V tolerant output					0.1	V
	CMOS 5 V tolerant output					0.1	V
	5 V full-swing output buffer[Note 8]					0.1	V
High-level output voltage	LVTTL output type	V_{OH}	I_{OH} = 0 mA	V_{DD33}-0.1			V
	TTL 5 V tolerant output			V_{DD33}-0.2			V
	5 V full-swing output buffer[Note 8]			V_{DD50}-0.1			V

Notes 1. Static current consumption increases when an I/O block with an on-chip pull-up/pull-down resistor is used (see **CHAPTER 5 ESTIMATING ELECTRICAL CHARACTERISTICS** for details).

2. For TTL 5 V tolerant and CMOS 5 V tolerant 3-state buffers and I/O buffers, the OFF state current of the output increases slightly in order to bias the 5 V protection circuit.

3. If the TTL 5 V tolerant and CMOS 5 V tolerant output buffers are pulled up at a voltage higher than the supply voltage of the LSI, a sink current flows from the output pins to the internal circuitry of the LSI.

4. The output short-circuit time is 1 second or less per pin of the LSI.

5. The pull-up and pull-down resistances vary depending on the input and output voltages.

6. All the buffers with the same output drive capability have the same specifications.

7. 2.00 mA for a buffer with a 5 kΩ pull-up resistor.

8. Only when 5 V full-swing buffer is provided.

9. Same for other drive capabilities (I_{OH}/I_{OL}) types.

Remark The + and − signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by −.

The CMOS 5 V tolerant output buffer structurally has no direct-current output high level.

4.3.4 AC characteristics (gate array)

Table 4-9 shows the AC characteristics.

The maximum operating clock frequency ($f_{MAX.}$) of the internal cell toggle flip-flop is the value of the toggle frequency (f_{tog}) in the table. Note that the maximum operating clock frequency ($f_{MAX.}$) varies in the actual circuit according to the circuit configuration.

Table 4-9. AC Characteristics (V_{DD33} = 3.3 ±0.3 V, V_{DD50} = 5.0 ±0.5 V, T_A = -40 to +85 °C)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Maximum toggle frequency	f_{tog}	Internal toggle F/F (Fan-outs = 2)		670			MHz
Propagation delay time	t_{PD}	Internal gate	Fan-outs = 1; Wiring length = 0 mm		94		ps
			Fan-outs = 1; Standard wiring length		131		ps
			Standard load		108		ps
		Internal gate (power gate)	Fan-outs = 1; Standard wiring length		107		ps
			Standard load		94		ps
		Input buffer	Fan-outs = 1; Standard wiring length		229		ps
			Standard load		222		ps
		Output buffer (FO01)	C_L = 15 pF		1396		ps
		5 V full-swing input buffer	Fan-outs = 2; Standard wiring length		690		ps
		5 V full-swing input buffer	C_L = 15 pF, I_{OL} = 18 mA		2045		ps
Output rise time	t_r	Output buffer (FO01)	C_L = 15 pF		2391		ps
		5 V full-swing output buffer	C_L = 15 pF, I_{OL} = 9 mA		1601		ps
Output fall time	t_f	Output buffer (FO01)	C_L = 15 pF		1872		ps
		5 V full-swing output buffer	C_L = 15 pF, I_{OL} = 9 mA		1583		ps

Remark Standard load : Fan-outs = 2; Wiring length = 0 mm
Standard wiring length : 145 μm/1 pin-pair

4.3.5 Pin Capacitance

Pin capacitance is the sum of the interface block capacitance and the package characteristic capacitance. Table 4-10 shows the capacitance (C_B) of the interface blocks. Table 4-11 shows the capacitance (C_P) of each package.

The pin capacitance is calculated by the following formula:

Pin capacitance (C_T) = interface block capacitance (C_B) + capacitance (C_P) of each package

Table 4-10. Capacitance of Interface Block (C_B)

(a) Input Buffer

Inteface level	$C_{B(MIN.)}$ (pF)		$C_{B(MAX.)}$ (pF)	
	Normal	with Failsafe	Normal	with Failsafe
LVTTL	3.25	2.84	3.97	3.48
5 V tolerant	6.25	–	6.97	–
5 V full-swing	8.00	–	10.00	–

Remark V_{DD} = 0 V, T_J = 25 °C, f = 1 MHz

(b) Output Buffer/I/O Buffer

Interface Level		C_B (pF)							
		1 mA	2 mA	3 mA	6 mA	9 mA	12 mA	18 mA	24 mA
LVTTL	MIN	-	-	3.25	3.25	3.25	3.25	3.25	3.25
	MAX	-	-	3.97	3.97	3.97	3.97	3.97	3.97
TTL5 V tolerant	MIN	6.25	6.25	6.25	6.25	6.25	6.25	6.25	6.25
	MAX	6.97	6.97	6.97	6.97	6.97	6.97	6.97	6.97
CMOS 5 V tolerant	MIN	-	-	6.25	6.25	6.25	6.25	6.25	6.25
	MAX	-	-	6.97	6.97	6.97	6.97	6.97	6.97
5 V full-swing	MIN	-	-	8.00	8.00	8.00	8.00	8.00	8.00
	MAX	-	-	10.00	10.00	10.00	10.00	10.00	10.00

Remark V_{DD} = 0 V, T_J = 25 °C, f = 1 MHz

Table 4-11. Capacitance of Packages (C_P)

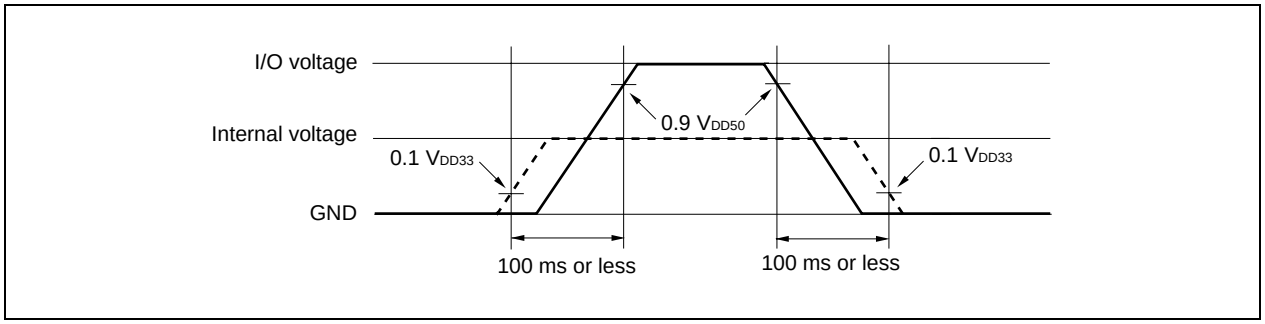
Package		Lead Pitch	Package Size	C_P (pF)
PBGA	464 pins	1.00 mm, perimeter	25 × 30 mm	0.8 to 2.0
	550 pins			
FPBGA	452 pins	0.80 mm, perimeter	22 × 22 mm	Under evaluation
	433 pins	0.65 mm, perimeter	17 × 17 mm	Under evaluation

4.4 Power Supply Application/Interruption Sequence

Regardless of power supply sequence, the time interval from the start of the rise of the first power supply until both the internal power supply and the I/O power supply stabilize should be 100 ms or less (recommended).

The voltage during time measurement is from 0.1 V_{DD} to 0.9 V_{DD} (see Figure 4-1).

Figure 4-1. Power Supply Application/Interruption Sequence Example (Recommended)



(1) When using 5 V full-swing buffer

When turning on 5 V power supplies, time interval after the internal power supply and the I/O power supply are turned on until each power supply stabilizes should be 100 ms or less (recommended).

When turning off the power supplies, at first turn off the 5V power supply and the other power supplies should be terminated in 100 ms or less.

CHAPTER 5 ESTIMATING ELECTRICAL CHARACTERISTICS

This chapter explains the methodology for calculating power consumption and propagation delay time. The current consumption values described in this chapter are only those of the EP-1 series gate array block. Note that the current consumption values of the EP-1 series as a whole are the total values of the CPU block and the gate array block.

5.1 Estimating Static Current Consumption

5.1.1 Estimating static current consumption

Only a minute leakage current flows from the power supply to GND in the standby state. If a 5 V output block or an I/O buffer with an on-chip pull-up/pull-down resistor is not used, the static current consumption is equal to the leakage current. On the other hand, if an I/O buffer with an on-chip pull-up/pull-down resistor is used, the static current consumption increases due to direct current flowing through that resistor according to the signal level.

Moreover, for TTL 5 V tolerant and CMOS 5 V tolerant output buffers, current flows from the output pin into the LSI if the output buffer is pulled up at the 5 V power supply, even if the output level is high.

To calculate static current consumption, use the following equation:

$$I_{DDS\,(max.)} = I_L + I_{U50} \times \lambda + I_{D50} \times m + I_{U5} \times n + I_{RT} \times p + I_{RC} \times q \quad (\mu A)$$

I_L: Gate array block leakage current: MC-10501/10505 (200 μA)
MC-10502/10506 (400 μA)
MC-10503/10507 (600 μA)

I_{U50}: Current consumption of 50 kΩ on-chip pull-up resistor (190 μA)

I_{D50}: Current consumption of 50 kΩ on-chip pull-down resistor (190 μA)

I_{U5}: Current consumption of 5 kΩ on-chip pull-up resistor (1900 μA)

I_{RT}: Current flowing into TTL 5 V tolerant output buffer output

Output level		
	Low level	(V_{PU}/R_{PU} A)
	High level	(see **5.1.2 Output influx current (I_R)**)
	High impedance	(14 μA)

I_{RC}: Current flowing into CMOS 5 V tolerant output buffer output

Output level		
	Low level	(VPU/RPU A)
	High level	(see **5.1.2 Output influx current (I_R)**)
	High impedance	(18 μA)

λ: Number of signal low levels in an I/O buffer with 50 kΩ on-chip pull-up resistor

m: Number of signal high levels in an I/O buffer with 50 kΩ on-chip pull-down resistor

n: Number of signal low levels in an I/O buffer with 5 kΩ on-chip pull-up resistor

p: Number of TTL 5 V tolerant output buffers pulled up by the 5 V power supply

q: Number of CMOS 5 V tolerant output buffers pulled up by the 5 V power supply

V_{PU}: 5 V pull-up voltage

R_{PU}: Pull-up resistance

If a 3-state circuit is included in the circuitry, the effect of the OFF-state output current must also be considered.

5.1.2 Output influx current (I_R)

The TTL 5 V tolerant and CMOS 5 V tolerant output buffers are blocks used when a 5 V output level is required. In a TTL 5 V tolerant output block, current flows into the LSI if pulled up at 5 V to make the output a direct-current flow. A direct-current high level cannot be implemented for the CMOS 5 V tolerant output buffer, but a small influx current is generated. (However, an influx current outside the OFF state leakage cannot flow if the output is at high impedance.)

Figure 5-1. Output Influx Current (I_R) Influx Route

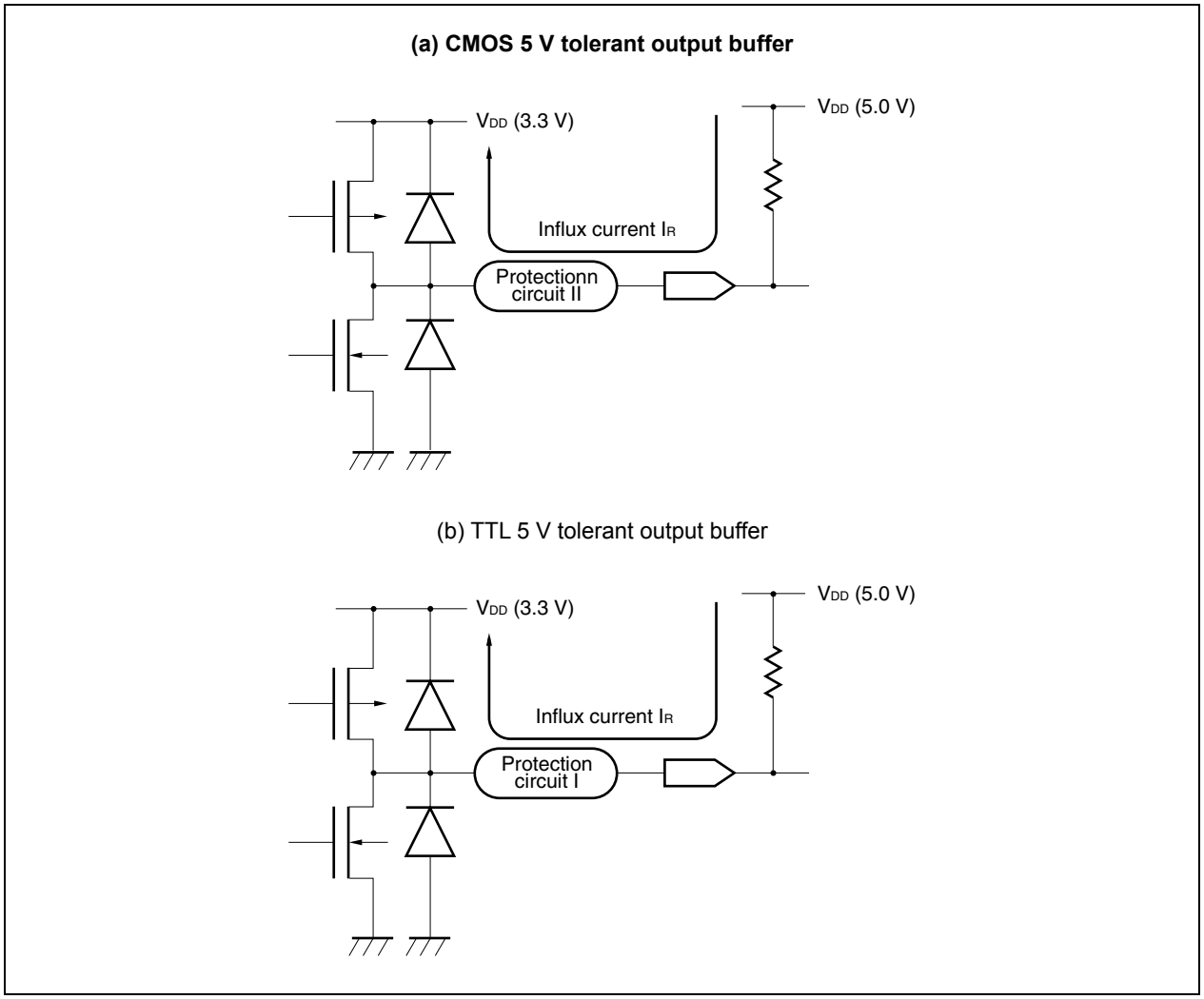
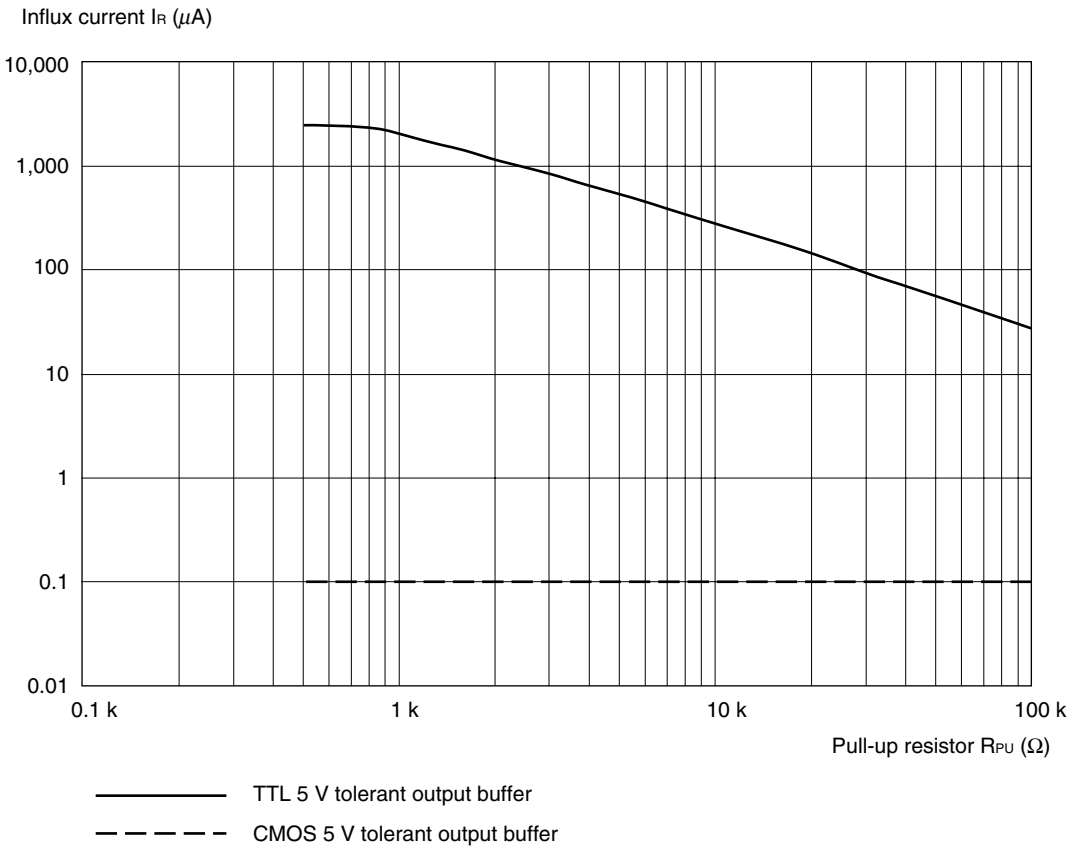


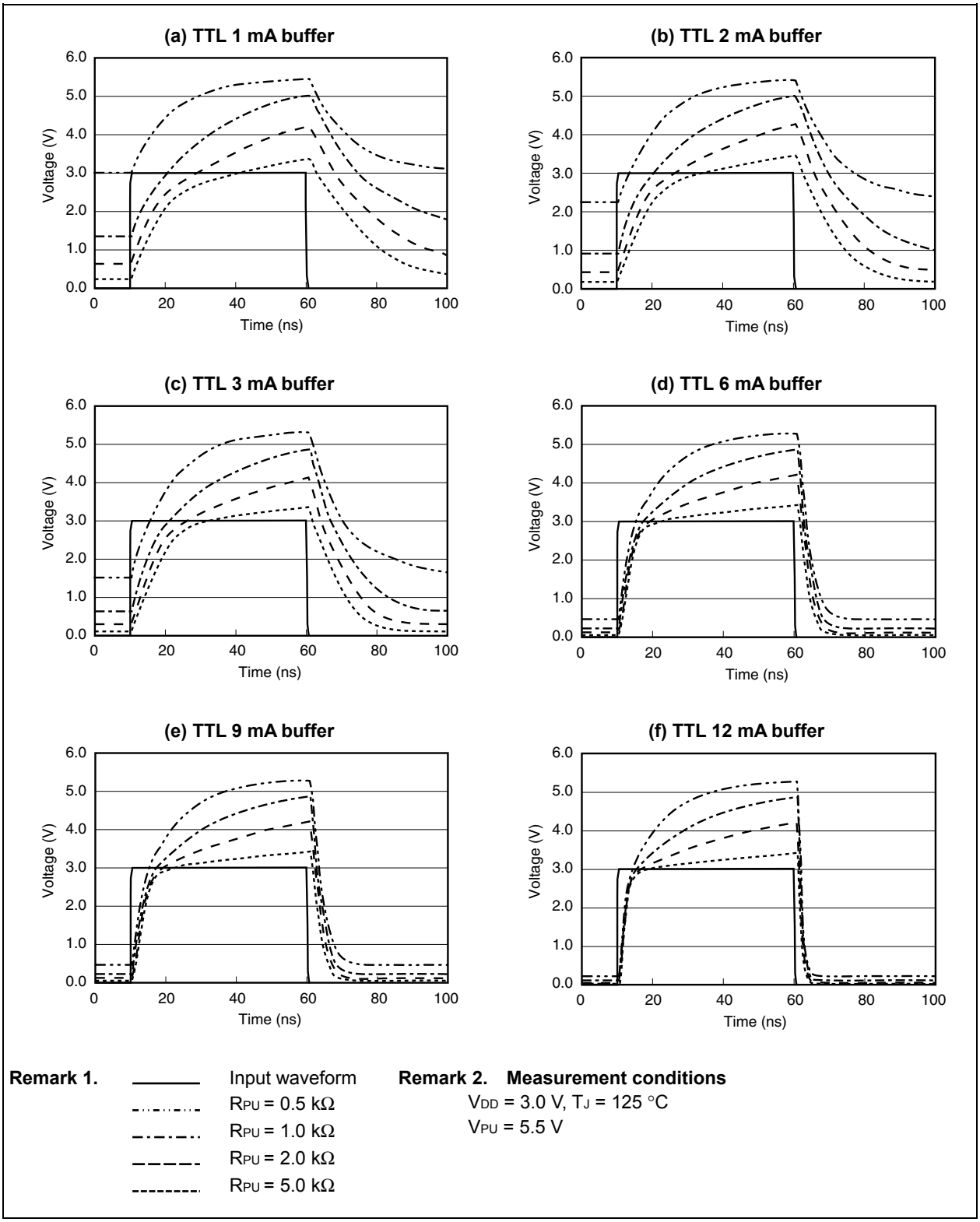
Figure 5-2 shows the influx current determined by the pull-up resistor. Figure 5-3 shows an output waveform based on a representative pull-up resistance value. The measurement circuit for the output waveform and the conditions on a representative pull-up resistance value are shown in Figure 5-4. Still more, Figure 5-5 shows an output waveform based on a 5 V full-swing buffer. The measurement circuit for the output waveform and the conditions on 5 V fullswing buffer are shown in Figure 5-6.

Figure 5-2. Output Influx Current



Conditions V_{DD} = 3.0 V, V_{PU} = 5.5 V
T_J = 125 °C
Worst case

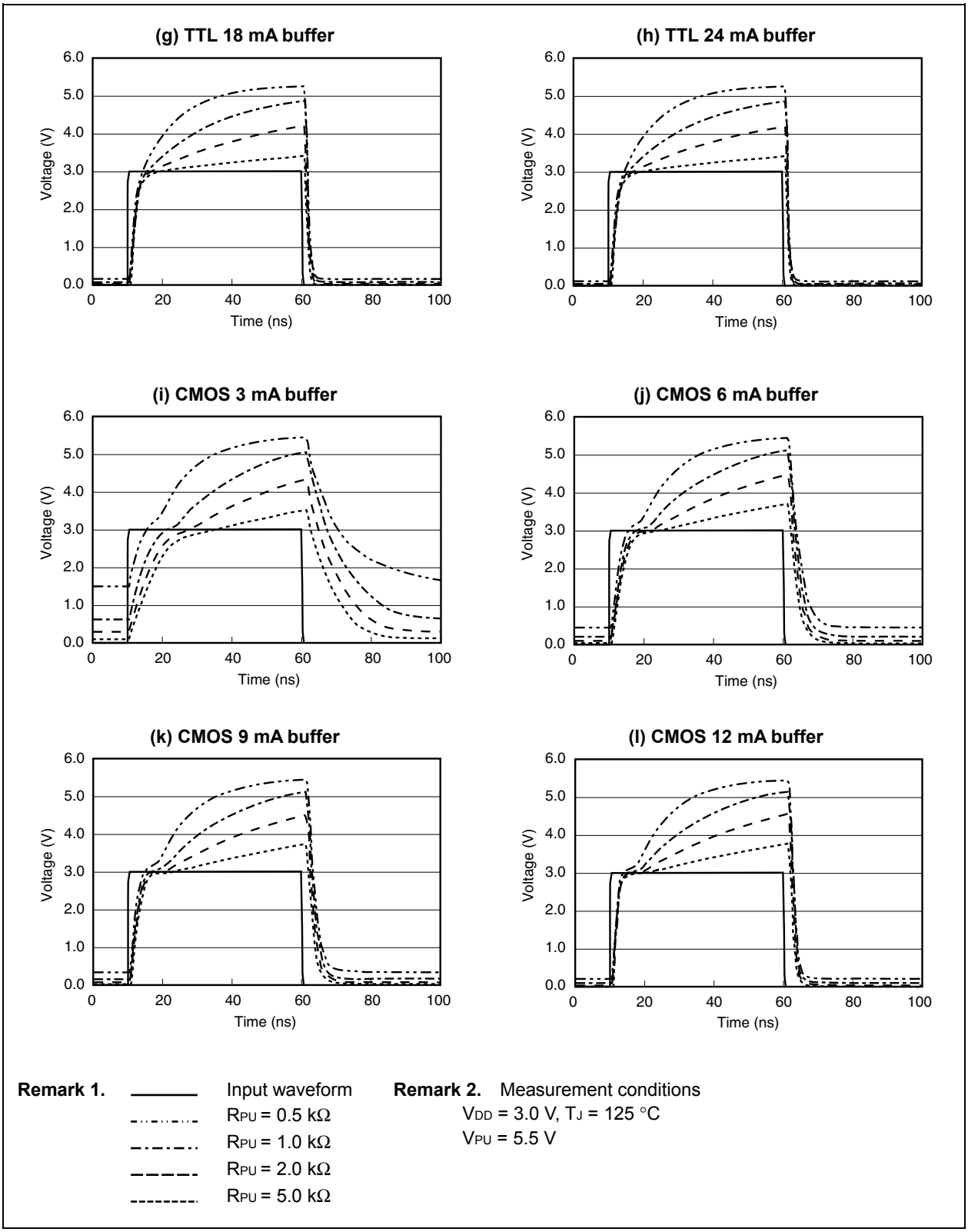
Figure 5-3. 5 V Tolerant Output Buffer Output Waveform (1/3)



Remark 1. Input waveform
R_{PU} = 0.5 kΩ
R_{PU} = 1.0 kΩ
R_{PU} = 2.0 kΩ
R_{PU} = 5.0 kΩ

Remark 2. Measurement conditions
V_{DD} = 3.0 V, T_J = 125 °C
V_{PU} = 5.5 V

Figure 5-3. 5 V Tolerant Output Buffer Output Waveform (2/3)



Remark 1. Input waveform
R_{PU} = 0.5 kΩ
R_{PU} = 1.0 kΩ
R_{PU} = 2.0 kΩ
R_{PU} = 5.0 kΩ

Remark 2. Measurement conditions
V_{DD} = 3.0 V, T_J = 125 °C
V_{PU} = 5.5 V

Figure 5-3. 5 V Tolerant Output Buffer Output Waveform (3/3)

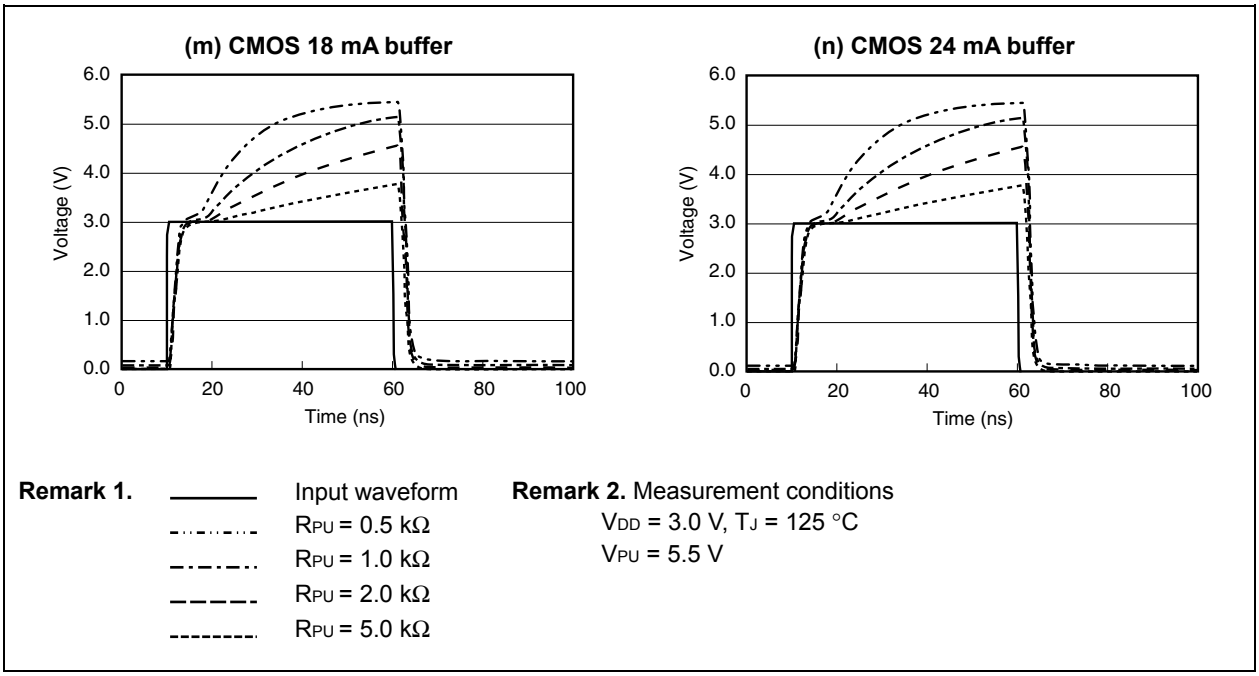


Figure 5-4. Measurement Circuit (5 V Tolerant Output Buffer)

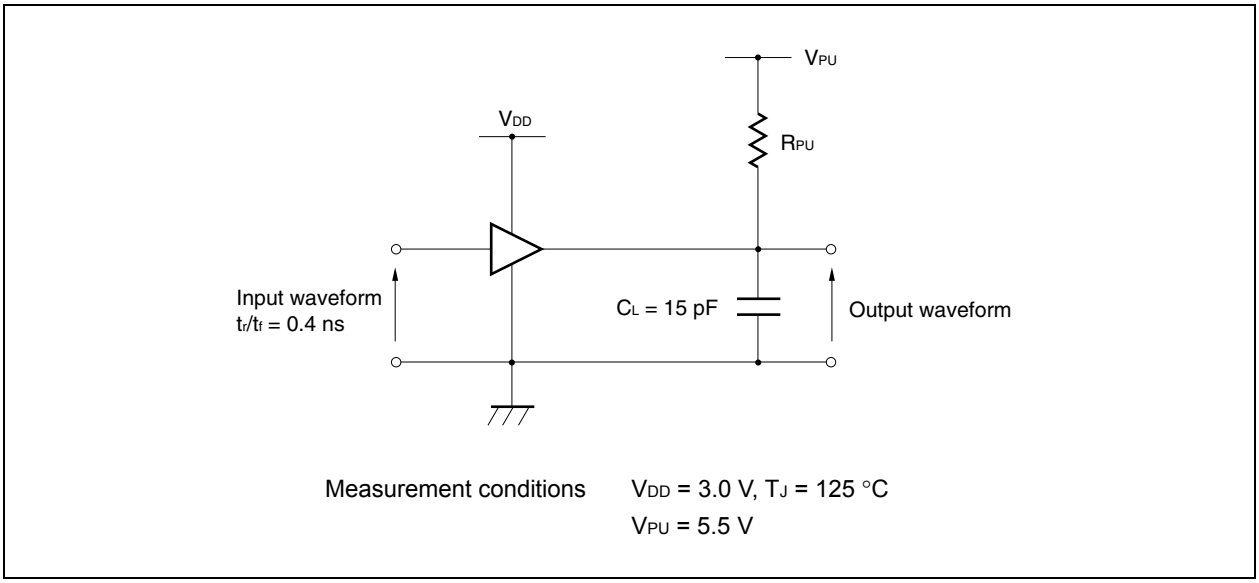


Figure 5-5. 5 V full-swing buffer output waveform

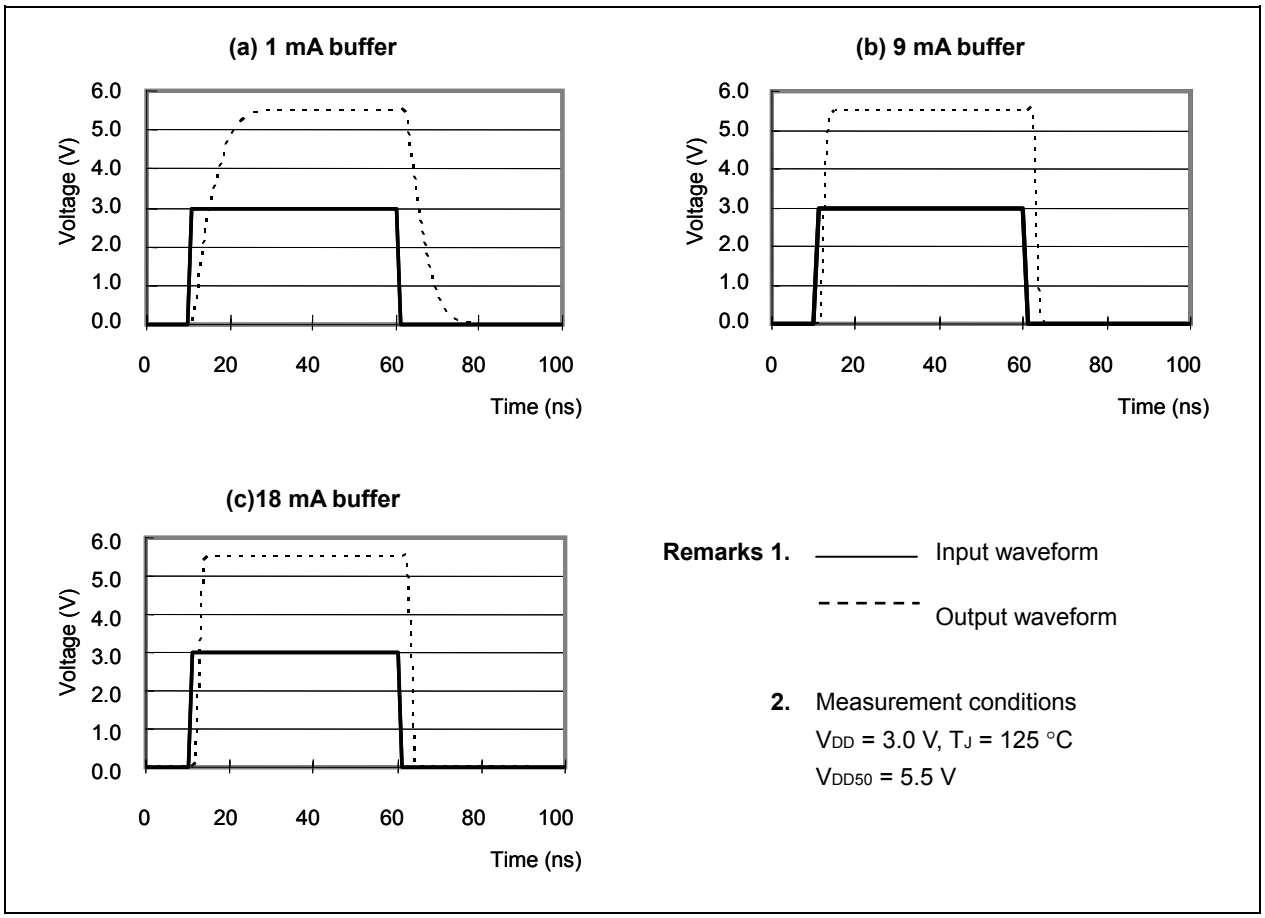
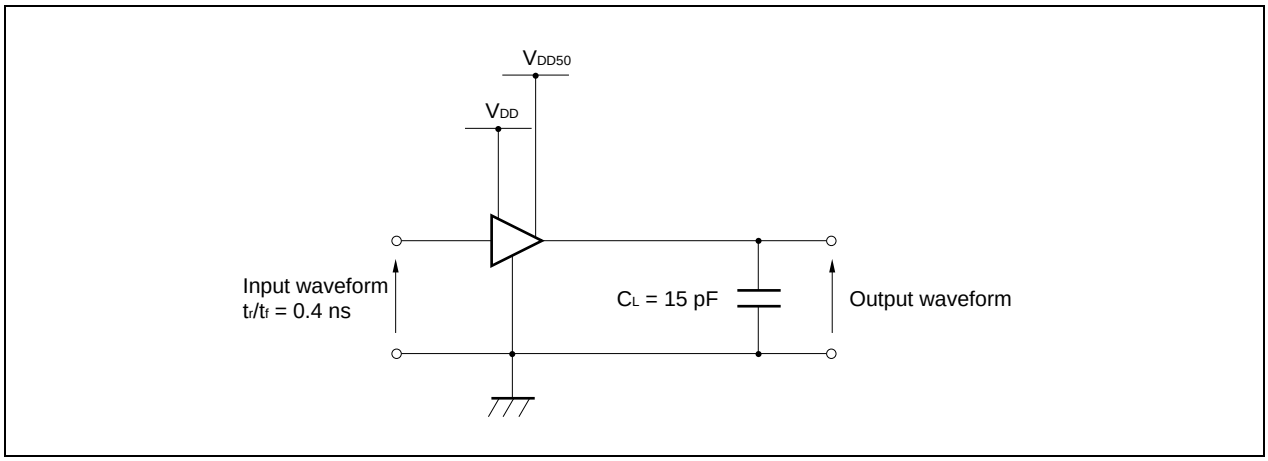


Figure 5-6. Measurement Circuit (5 V full-swing buffer)



5.2 Input Through Current

If the input voltage (VIN) is the same as the power supply voltage (V_{DD}), the input leakage current will be the same as the value listed in **CHAPTER 4 PRODUCT SPECIFICATIONS**. However, if the input voltage is lower than the power supply voltage, or if the input voltage is higher than the GND level, then a current will flow from the P-channel via the N-channel. This current is called the input through current. Figures 5-7 to 5-12 show the input through current (reference value) of each interface.

Figure 5-7. Input Through Current (3.3 V Input)

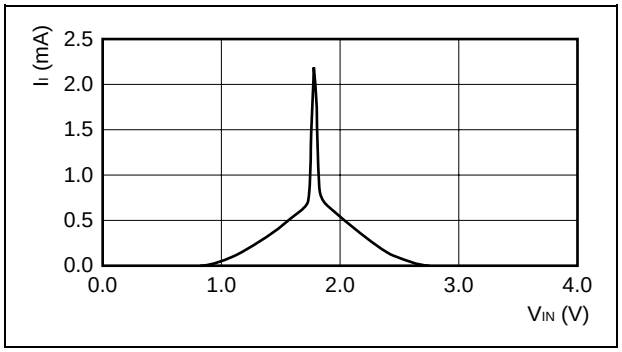


Figure 5-8. Input Through Current (3.3 V Schmitt input)

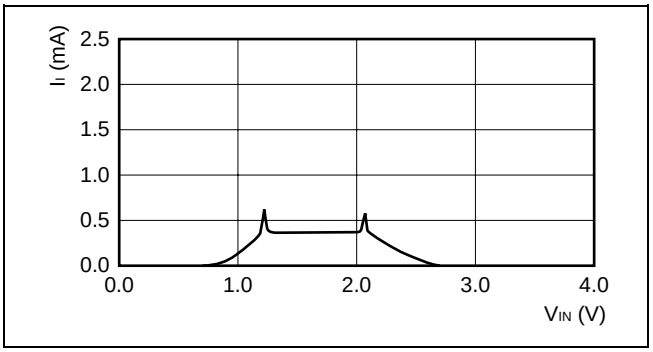


Figure 5-9. Input Through Current (5 V Input)

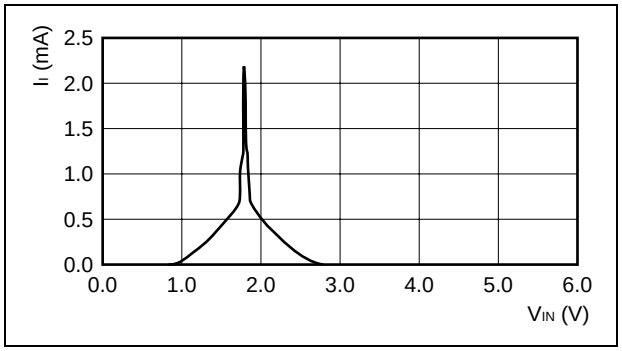


Figure 5-10. Input Through Current (5 V Schmitt input)

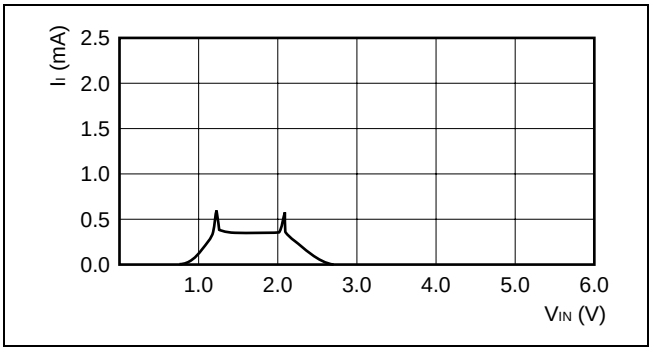


Figure 5-11. Input Through Current (5 V full-swing Input)

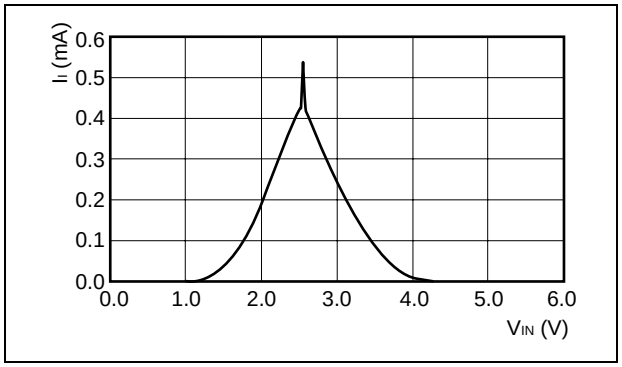
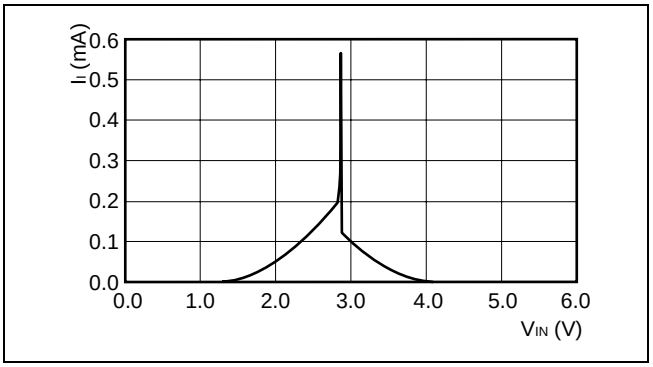


Figure 5-12. Input Through Current (5 V full-swing Schmitt input)



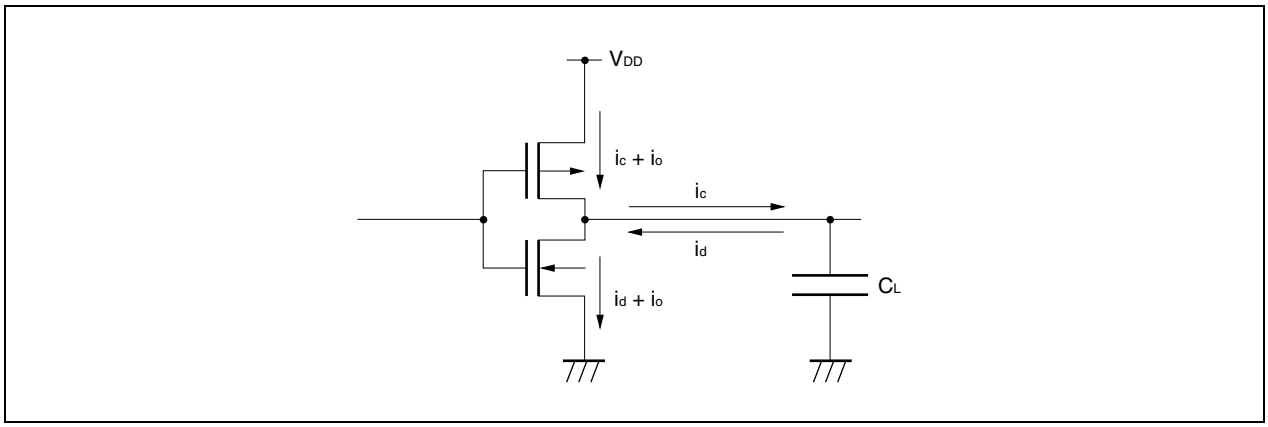
5.3 Power Consumption

Although CMOS device transistors consume less power than bipolar devices, they still consume a considerable amount of power if the circuit scale is large and the operating frequency is high. Because the temperature of an LSI (chip), which has a significant influence on the reliability (life) of the LSI, rises with power consumption, it is necessary to hold the power consumption of the LSI below a maximum.

5.3.1 Causes of power consumption

The current consumption is the sum of the following values, like the standard CMOS devices:

- Charge current of load capacitance connected to each transistor : ic
- Discharge current of load capacitance connected to each transistor : id
- Through current when each transistor is switching : io
- Leakage current of the device : IL



Because there is no charge, discharge, or through current when the LSI is not operating, the power consumption of the chip is determined by the leakage current of the entire device. Inasmuch as the charge, discharge, and through currents become extremely large compared with the leakage current when the LSI is operating, the effect of leakage current can be ignored in the chip power consumption. When the output rise (fall) time of each transistor is extremely fast compared with the input rise (fall) time, the through current increases greatly. However, through current is normally proportional to the charge and discharge currents.

5.3.2 Estimating power consumption

Power consumption is determined by the charge, discharge, and through currents of each transistor. However, as it is problematic to define each transistor state, a rough calculation of power consumption is made for each type of block.

The calculated results of the formulas shown below are values at V_{DD} = 3.3 V and T_A = 25°C; thus, adjustments must be made if the power supply or the temperature is different.

Total power consumed $P_D = \Sigma P_{DCELL} + \Sigma P_{RAM} + \Sigma P_{DI} + \Sigma P_{CTS} + \Sigma P_{PLL} + \Sigma P_{GTL} + \Sigma P_{DO} + \Sigma P_{OSC}$

(a) Σ P_{DCELL}… Internal cell power consumption
(Excluding the cells used by memory, clock tree synthesis, and interface block)

$\Sigma P_{DCELL} = \Sigma P_{DGate} + \Sigma P_{DLatch} + \Sigma P_{DF/F} + \Sigma P_{DT}$ (μW)

See **APPENDIX A POWER CONSUMPTION** for details.

(b) ΣP_{RAM}…Memory block power consumption

RAM block power consumption

$\Sigma P_{RAM} = \Sigma (P_{RM} \times f_{RM} \times R_{RM} + P_{WM} \times f_{WM} \times R_{WM})$ (mW)

P_{RM}: Unit power consumption during read (mW/MHz) Note 1
f_{RM}: Operating frequency during read
R_{RM}: Operating rate during read Note 2
P_{WM}: Unit power consumption during write (mW/MHz) Note 1
f_{WM}: Operating frequency during write
R_{WM}: Operating rate during write Note 2

(c) ΣP_{DI}…Input buffer and bidirectional buffer power consumption

$\Sigma P_{DI} = \Sigma (P_I \times f + P_{CONST}) \times Buffer$ (μW)

f: Operating frequency (MHz)
Buffer: Number of operating input buffers and bidirectional buffer inputs at frequency f
If input buffer operation is intermittent, use the average operating frequency (f_A) Note 3
P_I: Power consumption for each input buffer (μW/Buffer/MHz)
See Table 4-1.
P_{CONST}: Constant power consumption Note 4

Table 5-1. Power Consumption by Input Buffer

Representative Block Type	P_I
FI01, FIA1, FIV1, BP3I, BP5I, FI0P, FI0Q	3.95
FIS1, FIE1, FIF1	7.85

(d) Σ P_{CTS}…Clock tree synthesis power consumption

$$\Sigma P_{CTS} = \Sigma (28.32 + 0.786 \times 10^{-1} \times FF) \times f \times 10.86 \times 10^{-6} \quad (W)$$

f: Operating frequency (MHz)
FF: Flip-flop

(e) Σ P_{PLL}…Digital PLL power consumption

$$\Sigma P_{PLL} = \Sigma (P_{PL} \times f) \quad (mW)$$

f: Operating frequency (MHz)
P_{PL}: Digital PLL power consumption (See Table 5-2)

Table 5-2. Digital PLL Power Consumption

Block Type	P_{PL}
F9E4	1.18 mW

(f) ΣP_{DO}…Output and bidirectional buffer power consumption

$$\Sigma P_{DO} = \Sigma \{ (P_O + P_{CO} \times C_L) \times f + P_{CONST} \} \times Buffer \quad (mW)$$

P_O: Power consumption for each output buffer (without load) (mW/MHz). See Table 5-3.
P_{CO}: Power consumption for each output buffer (load dependent) (mW/MHz/pF). See Table 5-3.
C_L: Load capacitance (pF)
f: Operating frequency (MHz). Use the average operating frequency (f_A) when output buffers are operated intermittently**Note 3**.
Buffer: Number of output buffers and bidirectional buffers operating at frequency f (output part)
P_{CONST}: Constant power consumption**Note 4**.

Table 5-3. Output Buffer Power Consumption

Output Level	I_{OL} (mA)	Representative Block	P_O (mW/MHz)	P_{CO} (mW/MHz/pF)
LVTTL Output Normal Type	3.0	FO09	0.099	0.011
	6.0	FO04	0.117	0.012
	9.0	FO01	0.121	0.012
	12.0	FO02	0.124	0.012
	18.0	FO03	0.134	0.012
	24.0	FO06	0.144	0.011
LVTTL Output Low-noise Type	6.0	FE04	0.114	0.012
	9.0	FE01	0.117	0.012
	12.0	FE02	0.121	0.012
	18.0	FE03	0.128	0.012
	24.0	FE06	0.132	0.011
TTL 5 V Tolerant Output Normal Type	1.0	FV0A	0.277	0.011
	2.0	FV0B	0.252	0.011
	3.0	FV09	0.272	0.011
	6.0	FV04	0.295	0.011
	9.0	FV01	0.301	0.011
	12.0	FV02	0.310	0.011
	18.0	FV03	0.321	0.011
	24.0	FV06	0.332	0.011
TTL 5 V Tolerant Output Low-noise Type	12.0	FW02	0.310	0.011
	18.0	FW03	0.312	0.011
	24.0	FW06	0.317	0.011
CMOS 5 V Tolerant Output Normal Type	3.0	FY09	0.338	0.010
	6.0	FY04	0.346	0.011
	9.0	FY01	0.346	0.011
	12.0	FY02	0.359	0.012
	18.0	FY03	0.368	0.011
	24.0	FY06	0.381	0.011
CMOS 5 V Tolerant Output Low-noise Type	12.0	FZ02	0.350	0.011
	18.0	FZ03	0.354	0.011
	24.0	FZ06	0.360	0.011
5 V Full-Swing Output Normal Type	1.0	FV0AAL	0.2098	0.0246
	2.0	FV0BAL	0.2413	0.0259
	3.0	FV09AL	0.2518	0.0264
	6.0	FV04AL	0.2826	0.0272
	9.0	FV01AL	0.3147	0.0264
	12.0	FV02AL	0.3754	0.0257
	18.0	FV03AL	0.5340	0.0252
PCI Output	-	BP3O	0.134	0.012
	-	BP5O	0.332	0.011

The output level of TTL 5 V tolerant output is defined to be 3.3 V, and that of the CMOS 5 V tolerant output is defined to be 5.0 V.

The following equation should be used when 5 V are used to pull up the TTL 5 V output:

$$P_{DO\ (5.0\ V)} = 1.65 \times P_{DO} \quad (mW)$$

The following equation should be used when 3.3 V are used to pull up the CMOS 5 V tolerant output.

$$P_{DO\ (3.3\ V)} = P_{DO}/1.65 \quad (mW)$$

(g) Σ P_{GTL}…GTL+ power consumption

$$\Sigma P_{GTL} = \Sigma P_{GI} \times \text{Buffer} + \Sigma P_{GO} \times \text{Buffer} \quad (mW)$$

P_{GI}: Input part power consumption (mW/Buffer) (See Table 5-4.)

P_{GO}: Output part power consumption (mW/Buffer)

Table 5-4. Power Consumption of GTL+ Input

Condition	Supply Current (mA)	P_{GI} (mW/Buffer)
IEN = 1, A = 0	Under study	Under study
IEN = 1, A = 1	Under study	Under study
IEN = 0	Under study	Under study

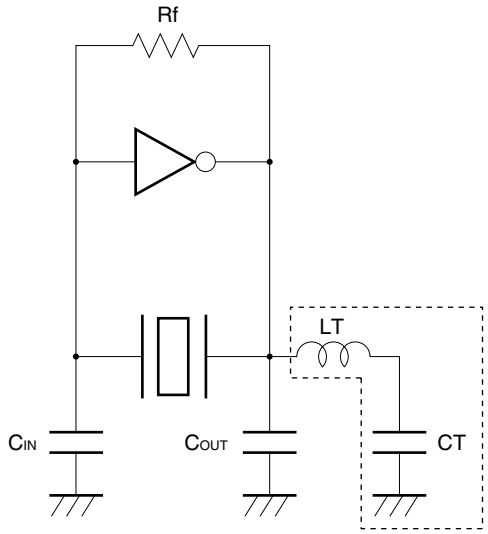
GTL+ output power consumption

P_{GO} = (Under study) (mW/Buffer)

(h)Σ P_{OSC}…Oscillator power consumption (Reference value)

The power consumption (reference value) is shown in Table 5-5, and circuit diagram is shown in Figure 5-13.

Figure 5-13. Oscillator Power Consumption Circuit Diagram



Remark The section within the broken lines is added when measuring at 32 MHz or 48 MHz.

Table 5-5. Oscillator Power Consumption (Reference Values)

Frequency	External Constant Used				Duty (%)	V_{start} (V)	V_{hold} (V)	P_{OSC} (mW)
	C_{IN} (pF)	C_{OUT} (pF)	L_T (μH)	C_T (μF)				
4 MHz	13	23	-	-	51.8	1.73	1.31	16.64
24 MHz	13	13	-	-	51.4	1.83	1.50	21.21
32 MHz	3	13	4.7	0.1	51.7	2.22	1.75	24.99
48 MHz	3	13	4.7	0.1	52.8	2.37	2.04	30.14

Caution The values in the table are for reference only because the actual values vary greatly depending on the resonator and constant.

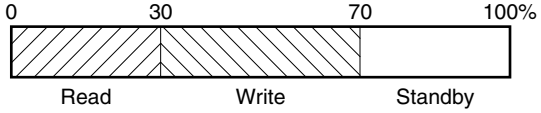
Remarks 1. The values indicated for Duty, Vstart, Vhold, and POSC (power consumption) are the worst-case values (V_{DD} = 3.6 V, T_A = 125°C).

2. The 32 MHz or 48 MHz resonator is used in overtone mode.

3. The values of external constants CIN and COUT include a jig capacitance of 3 pF.

Notes 1. Unit power consumption
(The numerical values are listed in **5.3.3 Unit power consumption of memory** and **CMOS-9HD Series Memory Block Library (A13071E)**.)

2. Write and read operating factors



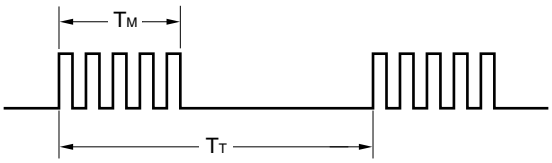
For example, if the RAM operating percentage is as shown in the figure above, then, RRM = 0.3 and RWM = 0.4

3. Average operating frequency (f_A)

(If operation is intermittent, the average operating frequency (fA) can be investigated.)

$f_A = f_M \times T_M \div T_T$

T_M: Actual operating interval
T_T: Intermittent operating cycle
f_M: Operating frequency of actual operating interval

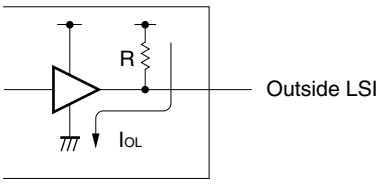


4. Constant power consumption
(If direct current is flowing through the input, output, and bidirectional buffers, a constant power consumption is added.)

Example 1. Direct current via the pull-up/pull-down resistor

$P_{CONST} = (V_{DD}^2/R) \times A$

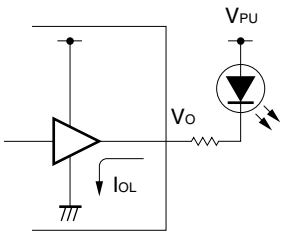
V_{DD}: Power supply voltage
R: Pull-up/pull-down resistance. Use a typical value if the resistor is on board the LSI
A: Operating factor
Low-level percentage when using a pull-up resistor, or high-level percentage when using a pull-down resistor The user should specify the operating factor based on the circuit specification



Example 2. To drive for items that require a large current, such as LEDs

$P_{CONST} = V_O \times I_O \times A$

A: Percentage of LED ON time



5.3.3 Unit power consumption of memory

(1) High-density 1-Port RAM

Refer to **Table 5-6 Unit Power Consumption of High-Density 1-Port RAM**.

Table 5-6. Unit Power Consumption of High-Density 1-Port RAM

RAM	Word	bit	P_{WM}	P_{RM}
RB47	16	4	0.018	0.014
RB49	32	4	0.019	0.015
RB4B	64	4	0.038	0.030
RB4D	128	4	0.023	0.018
RB4F	256	4	0.046	0.036
RB4H	512	4	0.092	0.072
RB4M	1024	4	0.184	0.144
RB4S	2048	4	0.368	0.288
RB4U	4096	4	0.736	0.576
RB87	16	8	0.036	0.028
RB89	32	8	0.038	0.030
RB8B	64	8	0.032	0.023
RB8D	128	8	0.046	0.036
RB8F	256	8	0.069	0.055
RB8H	512	8	0.138	0.110
RB8M	1024	8	0.097	0.068
RB8S	2048	8	0.194	0.136
RBAB	64	10	0.040	0.029
RBAD	128	10	0.080	0.058
RBAF	256	10	0.097	0.067
RBAH	512	10	0.194	0.138
RBAM	1024	10	0.118	0.082
RBAS	2048	10	0.236	0.164

RAM	Word	bit	P_{WM}	P_{RM}
RBC7	16	16	0.072	0.056
RBC9	32	16	0.076	0.060
RBCB	64	16	0.064	0.046
RBCD	128	16	0.092	0.072
RBCF	256	16	0.138	0.110
RBCH	512	16	0.276	0.220
RBCM	1024	16	0.194	0.136
RBEB	64	20	0.080	0.058
RBED	128	20	0.160	0.116
RBEF	256	20	0.194	0.134
RBEH	512	20	0.388	0.268
RBEM	1024	20	0.236	0.164
RBH7	16	32	0.144	0.112
RBH9	32	32	0.152	0.120
RBHB	64	32	0.128	0.092
RBHD	128	32	0.184	0.144
RBHF	256	32	0.276	0.220
RBHH	512	32	0.552	0.440
RBKB	64	40	0.160	0.116
RBKD	128	40	0.320	0.232
RBKF	256	40	0.388	0.268
RBKH	512	40	0.776	0.536

Remarks 1. P_{WM}: Power consumed during write
P_{RM}: Power consumed during read

2. Unit: mW/MHz

(2) High-density dual-port RAM

Refer to **Table 5-7 Unit Power Consumption of High-Density 2-Port RAM (W+R)**.

Table 5-7. Unit Power Consumption of High-Density 2-Port RAM (W+R)

RAM	Word	bit	P_{WM}	P_{RM}
R947	16	4	0.023	0.016
R949	32	4	0.030	0.020
R94B	64	4	0.060	0.040
R94D	128	4	0.040	0.028
R94F	256	4	0.080	0.056
R94H	512	4	0.160	0.112
R94M	1024	4	0.320	0.224
R94S	2048	4	0.640	0.448
R94U	4096	4	1.280	0.896
R987	16	8	0.046	0.032
R989	32	8	0.060	0.040
R98B	64	8	0.054	0.041
R98D	128	8	0.080	0.056
R98F	256	8	0.124	0.091
R98H	512	8	0.248	0.182
R98M	1024	8	0.159	0.105
R98S	2048	8	0.318	0.210
R9AB	64	10	0.065	0.050
R9AD	128	10	0.130	0.100
R9AF	256	10	0.147	0.109
R9AH	512	10	0.294	0.218
R9AM	1024	10	0.194	0.123
R9AS	2048	10	0.388	0.246
R9C7	16	16	0.092	0.064
R9C9	32	16	0.120	0.080
R9CB	64	16	0.108	0.082
R9CD	128	16	0.160	0.112
R9CF	256	16	0.248	0.182
R9CH	512	16	0.496	0.364
R9CM	1024	16	0.318	0.210
R9EB	64	20	0.130	0.100
R9ED	128	20	0.260	0.200
R9EF	256	20	0.294	0.218
R9EH	512	20	0.588	0.436
R9EM	1024	20	0.388	0.246
R9H7	16	32	0.184	0.128
R9H9	32	32	0.240	0.160
R9HB	64	32	0.216	0.164
R9HD	128	32	0.320	0.224
R9HF	256	32	0.496	0.364
R9HH	512	32	0.992	0.728
R9KB	64	40	0.260	0.200
R9KD	128	40	0.520	0.400
R9KF	256	40	0.588	0.436
R9KH	512	40	1.176	0.872

Remarks 1. P_{WM}: Power consumed during write

P_{RM}: Power consumed during read

2. Unit: mW/MHz

(3) Cell-based IC type memory

Refer to **EA-9HD Series Memory Macro Design Manual (A13367E)**.

5.3.4 Compensation method

The results calculated by the formulas in 5.3.2 Estimating power consumption are values for V_{DD} = 3.3 V and T_A = 25°C. If different power supply or temperature specifications are used, adjustments must be calculated using the following equation.

$$P_W = P_D \times K_1 + \Sigma P_{CONST} \times K_2$$

P_D: Calculated result of total power consumption (including constant power consumption)
ΣP_{CONST}: Sum of constant power consumption only
K1: Compensation coefficient (See Table 5-8)
K2: Compensation coefficient (See Table 5-8)

The TYP. value is usually used to determine the power consumption.

However, the MAX. value is used when high reliability is demanded.

The MAX. value can also be used to calculate the maximum power consumption value in each power supply and temperature specification range.

Table 5-8. Compensation Coefficient

(V_{DD} = 3.3 ±0.3 V, T_A = -40 to +85 °C)

Compensation Coefficient	TYP. Value	MAX. Value
K_1	1.00	1.28
K_2	0.00	0.15

5.3.5 Determining power consumption

The power consumption is determined on the basis of whether or not the calculated power consumption (P_D) is within the maximum allowable power consumption (P_{WL}) specified for each package and master. The maximum allowable power consumption and master is listed in **CHAPTER 11 PACKAGES** (Since packages under development are included, confirm that the package has been released).

$$P_D \leq P_{WL}$$

The values in **CHAPTER 11 PACKAGES** are for T_A = −40 to +85°C with natural convection. If a different maximum operating temperature is used, the maximum allowable power consumption for the environment used must be calculated by means of the maximum junction temperature (TJ (MAX.)), the maximum ambient temperature (T_A (MAX.)) and the thermal resistance (θ ja) specified for each package and master. The thermal resistance (θ_{ja}) for each package and master is listed in the tables concerning thermal resistance in **CHAPTER 11 PACKAGES** (Since packages under development are included, confirm that the package has been released). Thermal resistance was measured under the condition of a 90 × 90 mm by 1.6 mm thick sample mounted on a glass-epoxy circuit board.

$$P_{WL} = (T_{J\,(MAX)} - T_{A\,(MAX)}) / \theta_{ja} \quad (W)$$

Condition $T_{A\,(MAX.)} \geq 40$ °C

5.4 Estimating Propagation Delay Time

5.4.1 Accuracy of propagation delay time

The propagation delay time (t_{PD}) fluctuates due to I/O buffers, internal function blocks, and the following factors:

Factors fluctuating propagation delay time

- Load capacitance (number of fan-outs, routing capacitance)
- Power supply voltage
- Ambient temperature
- Manufacturing variation
- Other circuit-based factors

Circuit-based causes other than those related to power supply voltage, ambient temperature, and load capacitance include: fluctuation due to the input signal waveform, fluctuation in the equivalent input capacitance of the transfer gate, the Miller effect, and fluctuation in the input threshold voltage. NEC Electronics has introduced delay simulators and static delay calculators, taking these fluctuation factors into consideration as much as possible, so that a more precise propagation delay can be calculated.

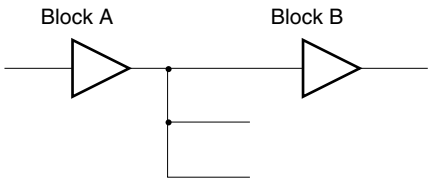
Thus, rough calculations of propagation delay time made by the user may not match the numerical values listed in the separately published **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

5.4.2 Calculation of propagation delay time

The calculation formula shown below is rough and simplified. The calculation results are comparatively accurate for a load range that satisfies the following conditions. The larger the load capacitance, the larger the error becomes and the smaller the calculated numerical result of the simulator becomes. With this prior understanding, this formula can be used as a guide.

Condition: The sum of the pre-stage F/I of the block, which is the object of the delay calculation, is within 15% of the F/O limit of the pre-stage drive block.

Example



Let Block B be the object of the propagation calculation. The accuracy of the simplified calculation formula is high when the sum of the F/I connected to the output of block A is within 15% of the block A F/O limit.

If these details or the above conditions are not applicable, see **APPENDIX B PROPAGATION DELAY TIME** for methods to improve the calculation accuracy. The propagation data for each block that is needed for the calculation is listed in the **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

(1) Input buffer and internal function block delay

The delay time of the internal function block and memory blocks can be calculated roughly from the load (number of fan-outs) connected to that output pin and the wiring length (routing capacitance).

$$t_{PD} = t_{LD0} + (\Sigma F/O + \lambda) \times t_1 \quad \text{(ns)}$$

t_{LD0}: Delay time of the block itself with F/O = 0 and λ = 0
Σ F/O: Number of fan-outs of the relevant output pins
λ: Routing capacitance connected to the relevant output pins
(see **5.4.3 Estimating routing capacitance**.)
t_1: Delay coefficient of the relevant output pins

Internal bus delay

$$t_{PD} = t_{LD0} + \{\Sigma F/O + \lambda + (N - 1) \times 0.96\} \times t_1 \quad \text{(ns)}$$

t_{LD0}: Delay time of the block itself with F/O = 0 and λ = 0
Σ F/O: Number of fan-outs connected to the bus
N: Sum of 3-state buffers (F531, F532) connected to the bus
λ: Routing capacitance connected to the relevant output pins
(see **5.4.3 Estimating routing capacitance**.)
t_1: Delay coefficient of the relevant output pins

Output buffer delay

Using the following equation, the output buffer delay can be roughly calculated from the load capacitance connected to the output pin.

$$t_{PD} = t_{LD0} + T \times C_L \quad \text{(ns)}$$

t_{LD0}: Delay time of the block itself with C_L = 0 pF
C_L: Load Capacitance connected to the relevant output pin
T: Delay Coefficient of the relevant output pin

The delay time of the I/O buffer is calculated based on the following conditions:

- LVTTL output: Threshold voltage = 1.5 V, output swing = 0 to V_{DD}
- 5 V tolerant output: Threshold voltage = 1.5 V, output swing = 0 to V_{DD}
- 5 V full-swing output: Threshold voltage = 2.5 V, output swing = 0 to V_{DD}

Even in the 5 V tolerant output, the delay time is specified based on the condition of no output pull-up.

5.4.3 Estimating routing capacitance

In embedded arrays, because the placement and routing is performed on the master based on circuit connection data, the physical length of the wiring to be connected as the function block load is not known at the preplacement/routing stage. The wiring length is therefore assumed and calculated so as to enable calculation of the propagation time before the placement and routing stage. When the actual layout results are statistically processed, the majority of the generated wiring lengths (about 70% of the total wiring) tend to be shorter than the values determined by the assumed wiring length calculation.

Table 5-9 shows the estimated values of the assumed wiring capacitance in the EP-1 series. Placement and routing are executed for each macro (in the top hierarchy only) within a determined placement range. Therefore there are considerable differences between intra- and inter-macro wiring lengths. The assumed wiring length in the pre-placement/routing stage is treated by the delay simulator in two categories: intra-macro and inter-macro. Therefore be aware that the values will differ slightly from those in Table 5-9.

Table 5-9. Routing Capacitance Estimate (Wiring Length Converted to F/I Value)

Master	Pin-Pair Count											
	1	2	3	4	5	6	7	8	9	10	15	20
MC-10501/10505	4.50	10.28	16.06	21.84	27.62	33.40	39.17	44.95	50.73	56.51	85.40	114.29
MC-10502/10506	5.10	12.18	19.27	26.36	33.44	40.53	47.62	4.70	61.79	68.87	104.31	139.74
MC-10503/10507												

5.4.4 Fluctuation in propagation delay time

The propagation delay time (t_{PD}) of I/O buffers and internal function block fluctuates for a variety of reasons as described in **5.4.1 Accuracy of propagation delay time**. The **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)** indicates the minimum and maximum values under the conditions:

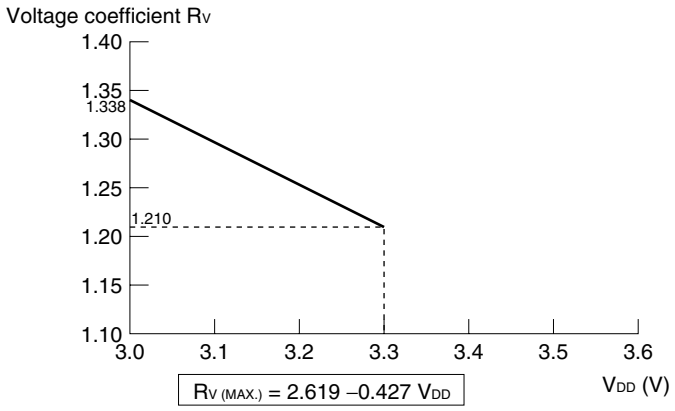
V_{DD} = 3.3 ±0.3 V and T_A = –40 to +85°C (T_J = –40 to +125°C)

The difference between the typical value and these values is called the absolute distribution. The propagation delay is listed for the minimum, typical, and maximum specifications.

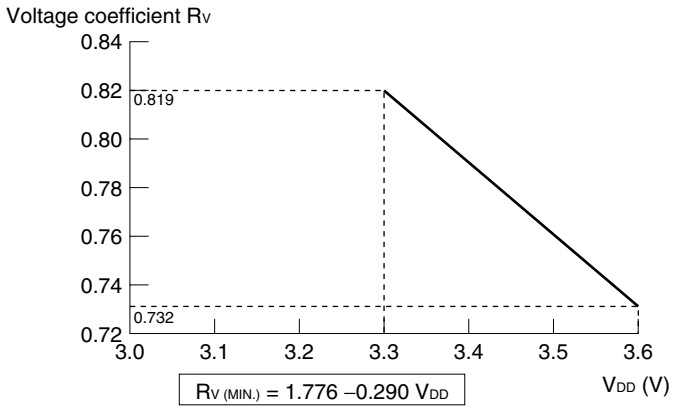
With the EA-9HD Series, the absolute distribution of each block is studied to improve the accuracy of calculation of the propagation delay time. Therefore, a uniform absolute distribution cannot be used unlike with conventional products. However, Figure 5-14 (a) through (c) shows, for reference, the dependency of the delay coefficient on power supply voltage and operating junction temperature.

Figure 5-14. Propagation Delay Time (Preliminary)

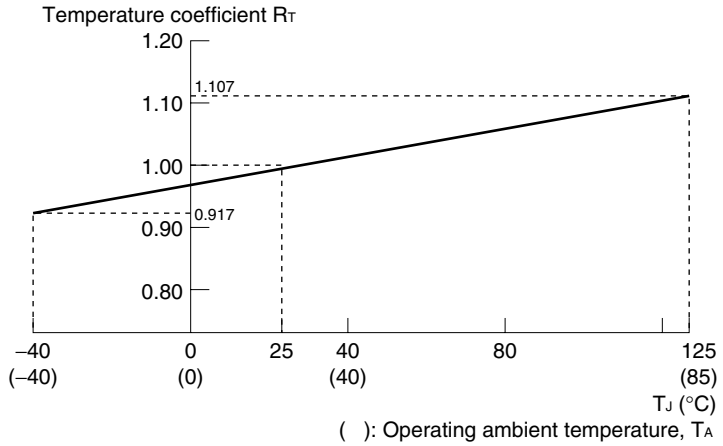
(a) V_{DD} dependency (MAX.)



(b) V_{DD} dependency (MIN.)



(c) T_J dependency



$-40 \leq T_J \leq 25°C$	$R_{T\,(MIN.)} = 0.968 + 0.00128T_J$
$25 \leq T_J \leq 125°C$	$R_{T\,(MAX.)} = 0.974 + 0.00106T_J$

The coefficient of the absolute distribution can be recalculated by limiting the operating ambient temperature and power consumption (for example, by limiting the temperature rise due to power consumption to about 10°C). The operating junction temperature when the operating ambient temperature or power consumption is limited can be calculated by the formula below. The lower the operating junction temperature, the closer to 1 the coefficient of the absolute distribution (if the operating junction temperature is limited to 100°C, the delay time is 5% shorter than when the temperature is limited to 125°C).

$T_J = T_{A(MAX)} + P_D \times \theta_{ja}$ (°C)

where: T_J : Operating junction temperature
$T_{A(MAX)}$: Maximum value of operating ambient temperature
P_D : Power consumption estimated by the calculation formula in 5.3.2 **Estimating power consumption**
θ_{ja} : Thermal resistance (See the tables concerning thermal resistance in **CHAPTER 11 PACKAGES**)

Please note that since Figure 5-14 (a) through (c) shows the average values of the delay distribution (variations in the process are already included in the value of the power supply voltage), the guaranteed values are the result of simulation.

Reference data

$R_{MAX} = R_{V(MAX)} \times R_{T(MAX)}$, $R_{MIN} = R_{V(MIN)} \times R_{T(MIN)}$, $t_{PD(MAX)} = t_{PD(TYP)} \times R_{MAX}$, $t_{PD(MIN)} = t_{PD(TYP)} \times R_{MIN}$

Standard specification: 3.3 V condition (V_{DD} = 3.3 ±0.3 V; T_A = –40 to +85°C; TJ = –40 to +125°C)

R_{MAX} = 1.48

R_{MIN} = 0.67

Calculation example 2

Derive $R_{MAX}./R_{MIN.}$ for V_{DD} = 3.3 ±0.3 V, T_J = -40 to +120 °C

(1) Derive R_V from Figure 5-14 (a) and (b):

$R_{V(MAX)}$= 1.34

$R_{V(MIN)}$= 0.73

(2) Next, derive R_T from Figure 5-14 (c):

$R_{T(MAX)}$= 1.10

$R_{T(MIN)}$= 0.92

(3) Accordingly, it follows that,

$R_{MAX} = R_{V(MAX)} \times R_{T(MAX)} = 1.34 \times 1.10$

$R_{MIN} = R_{V(MIN)} \times R_{T(MIN)} = 0.73 \times 0.92$

R_{MAX} = 1.474

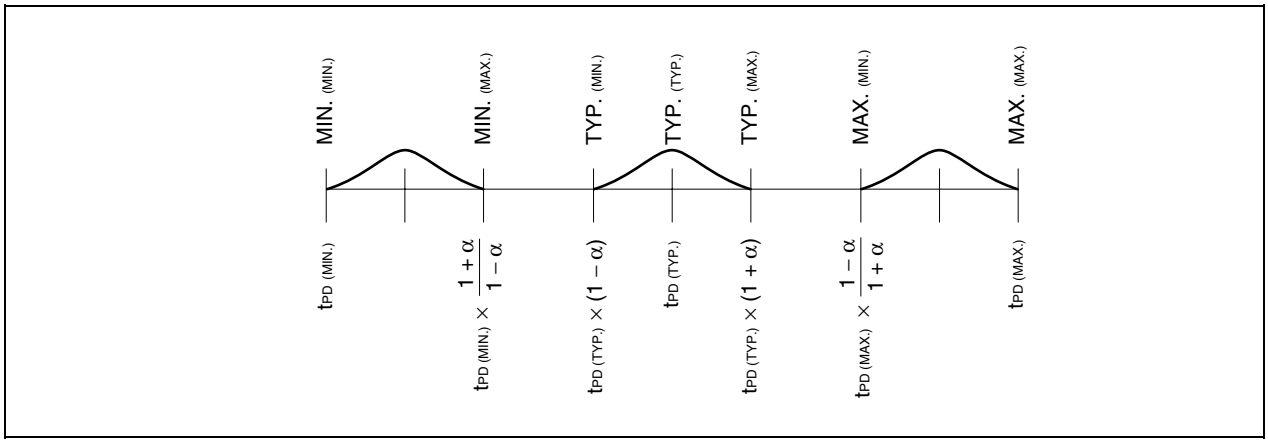
R_{MIN} = 0.672

In addition to the absolute distribution applicable from the device specification, there is also the relative distribution generated by the chip's internal paths and by the manufacture of the P-ch and N-ch transistors. This relative distribution is an important factor in verifying the timing of the circuit. The PFESiP/V850EP1 relative distribution is as follows.

Relative distribution α = 10 %

Figure 5-15 shows the distribution with t_{PD} (TYP.) as the median.

Figure 5-15. t_{PD} Distribution



5.5 Output Buffer Characteristics

5.5.1 Rise/fall times of output buffer

The rise and fall times of the output buffer vary greatly by differences in the drive capability due to the output level and by the connected load capacitance. The output buffer rise/fall times, tr and tf, can be calculated as follows:

$$t_r = t_{r0} + F_{tr} \times C_L \quad \text{(ns)}$$
$$t_f = t_{f0} + F_{tf} \times C_L \quad \text{(ns)}$$

t_{r0} : Reference rise time (load capacitance, C_L = 0 pF)
t_{f0} : Reference fall time (load capacitance, C_L = 0 pF)
F_{tr}, F_{tf} : Load capacitance coefficient
C_L : Load capacitance ($0 < C_L \leq 300$ pF)

See Tables 5-10 through 5-13 for output buffer coefficients.

Table 5-10. t_r and t_f Calculation Coefficients of LVTTL Output Buffer

(a) Output level = V_{DD} × 10% to V_{DD} × 90%

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal Type	FO09	I_{OL} = 3.0 mA	2.68	0.312	2.26	0.261
	FO04	I_{OL} = 6.0 mA	1.43	0.170	1.08	0.138
	FO01	I_{OL} = 9.0 mA	1.02	0.117	0.77	0.098
	FO02	I_{OL} = 12.0 mA	0.73	0.092	0.66	0.074
	FO03	I_{OL} = 18.0 mA	0.53	0.060	0.45	0.051
	FO06	I_{OL} = 24.0 mA	0.48	0.046	0.38	0.036
Low-noise Type	FE04	I_{OL} = 6.0 mA	2.93	0.181	3.71	0.140
	FE01	I_{OL} = 9.0 mA	2.58	0.125	3.30	0.100
	FE02	I_{OL} = 12.0 mA	2.45	0.093	3.12	0.077
	FE03	I_{OL} = 18.0 mA	2.40	0.065	2.97	0.053
	FE06	I_{OL} = 24.0 mA	2.37	0.033	2.93	0.040

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

(b) Output level = 0.8 to 2.0 V

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal Type	FO09	I_{OL} = 3.0 mA	0.85	0.105	0.87	0.101
	FO04	I_{OL} = 6.0 mA	0.42	0.056	0.41	0.055
	FO01	I_{OL} = 9.0 mA	0.30	0.039	0.29	0.038
	FO02	I_{OL} = 12.0 mA	0.23	0.029	0.23	0.028
	FO03	I_{OL} = 18.0 mA	0.18	0.019	0.16	0.019
	FO06	I_{OL} = 24.0 mA	0.14	0.014	0.13	0.015
Low-noise Type	FE04	I_{OL} = 6.0 mA	2.13	0.087	3.18	0.101
	FE01	I_{OL} = 9.0 mA	1.99	0.061	2.96	0.069
	FE02	I_{OL} = 12.0 mA	1.92	0.046	2.82	0.053
	FE03	I_{OL} = 18.0 mA	1.96	0.031	2.74	0.037
	FE06	I_{OL} = 24.0 mA	1.96	0.024	2.69	0.030

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Table 5-11. t_r and t_f Calculation Coefficients of TTL 5 V Tolerant Output Buffer

(a) Output level = V_{DD} × 10% to V_{DD} × 90%

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal Type	FV0A	I_{OL} = 1.0 mA	9.65	0.482	9.90	0.473
	FV0B	I_{OL} = 2.0 mA	7.18	0.371	7.05	0.349
	FV09	I_{OL} = 3.0 mA	7.15	0.319	5.45	0.275
	FV04	I_{OL} = 6.0 mA	2.75	0.124	1.95	0.100
	FV01	I_{OL} = 9.0 mA	2.17	0.095	1.55	0.075
	FV02	I_{OL} = 12.0 mA	1.34	0.064	0.87	0.042
	FV03	I_{OL} = 18.0 mA	1.35	0.064	0.70	0.035
	FV06	I_{OL} = 24.0 mA	1.40	0.065	0.60	0.028
Low-noise Type	FW02	I_{OL} = 12.0 mA	1.83	0.074	1.95	0.042
	FW03	I_{OL} = 18.0 mA	2.10	0.074	1.85	0.035
	FW06	I_{OL} = 24.0 mA	1.93	0.074	1.85	0.028

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

(b) Output level = 0.8 to 2.0 V

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal Type	FV0A	I_{OL} = 1.0 mA	2.90	0.130	3.85	0.181
	FV0B	I_{OL} = 2.0 mA	2.41	0.116	2.87	0.143
	FV09	I_{OL} = 3.0 mA	2.49	0.111	2.48	0.111
	FV04	I_{OL} = 6.0 mA	0.88	0.041	0.79	0.042
	FV01	I_{OL} = 9.0 mA	0.66	0.030	0.59	0.031
	FV02	I_{OL} = 12.0 mA	0.37	0.018	0.34	0.018
	FV03	I_{OL} = 18.0 mA	0.37	0.017	0.27	0.014
	FV06	I_{OL} = 24.0 mA	0.38	0.017	0.22	0.011
Low-noise Type	FW02	I_{OL} = 12.0 mA	0.61	0.015	0.70	0.016
	FW03	I_{OL} = 18.0 mA	0.67	0.016	0.64	0.013
	FW06	I_{OL} = 24.0 mA	0.63	0.016	0.58	0.011

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Table 5-12. t_r and t_f Calculation Coefficients of CMOS 5 V Tolerant Output Buffer

(c) Output level = 0.8 to 2.0 V

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal Type	FY09	I_{OL} = 3.0 mA	1.52	0.085	3.45	0.140
	FY04	I_{OL} = 6.0 mA	0.70	0.035	0.65	0.048
	FY01	I_{OL} = 9.0 mA	0.55	0.027	0.45	0.035
	FY02	I_{OL} = 12.0 mA	0.35	0.021	0.30	0.018
	FY03	I_{OL} = 18.0 mA	0.35	0.015	0.25	0.016
	FY06	I_{OL} = 24.0 mA	0.34	0.015	0.23	0.012
Low-noise Type	FZ02	I_{OL} = 12.0 mA	2.55	0.026	3.40	0.026
	FZ03	I_{OL} = 18.0 mA	2.56	0.026	3.51	0.024
	FZ06	I_{OL} = 24.0 mA	2.58	0.018	3.61	0.016

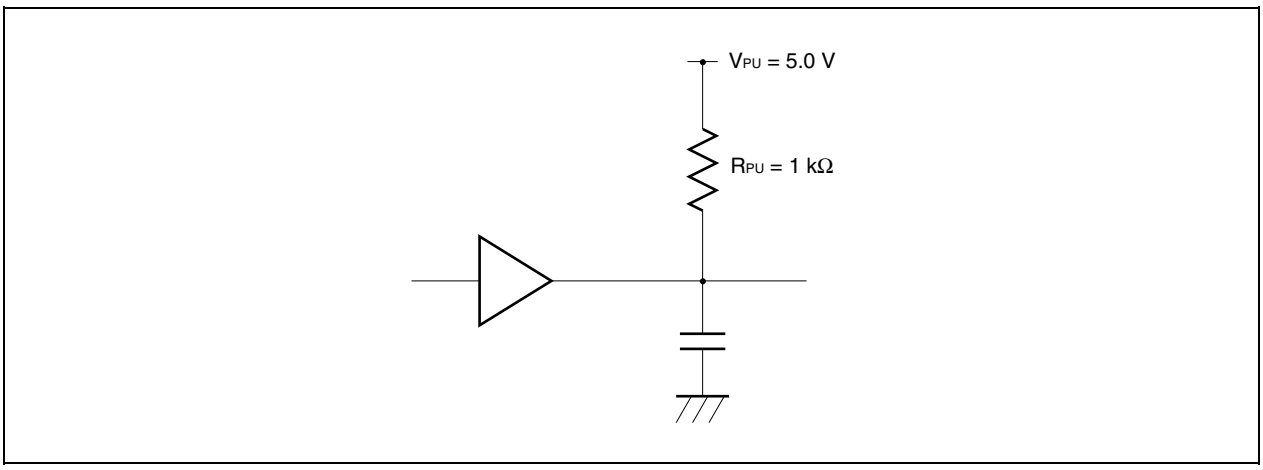
Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Table 5-13. t_r and t_f Calculation Coefficients of 5 V Full-Swing output Buffer

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal Type	FV0AAL	I_{OL} = 1.0 mA	4.72	0.877	4.76	0.894
	FV0BAL	I_{OL} = 2.0 mA	2.42	0.439	2.46	0.447
	FV09AL	I_{OL} = 3.0 mA	1.70	0.292	1.73	0.298
	FV04AL	I_{OL} = 6.0 mA	1.08	0.144	1.20	0.163
	FV01AL	I_{OL} = 9.0 mA	0.97	0.107	1.07	0.114
	FV02AL	I_{OL} = 12.0 mA	0.90	0.076	1.07	0.083
	FV03AL	I_{OL} = 18.0 mA	0.90	0.052	1.09	0.055
Low-noise Type	FW09AL	I_{OL} = 3.0 mA	2.11	0.288	2.50	0.290
	FW04AL	I_{OL} = 6.0 mA	1.67	0.140	2.06	0.160
	FW02AL	I_{OL} = 12.0 mA	1.62	0.078	1.94	0.093
	FW03AL	I_{OL} = 18.0 mA	1.64	0.058	1.92	0.070

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD33} = 3.3 V / V_{DD50} = 5.0 V. t_i = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Evaluation circuit



5.5.2 Recommended load capacitance range for output buffers

The maximum allowable load capacitance C_L (MAX.) of the output buffer should be C_L (MAX.) ≤ 300 pF. In addition, Table 5-14 shows the recommended load capacitance range for each drive capability of the output buffer. The optimal output buffer based on Table 5-14 should be selected.

The recommended load capacitance range of the 5 V tolerant buffers for CMOS depends on the pull-up resistance value.

In particular, if a load capacitance outside the recommended range is used, it must be noted that the overshoot and undershoot generated in the output signal increases if a lower load capacitance is used.

Table 5-14. Recommended Load Capacitance Ranges for Output Buffers

Buffer Type	Example	Drive Capability	Recommended Load Capacitance Range (pF)
LVTTL Normal Type	FO09	I_{OL} = 3.0 mA	0 to 40
	FO04	I_{OL} = 6.0 mA	0 to 80
	FO01	I_{OL} = 9.0 mA	10 to 110
	FO02	I_{OL} = 12.0 mA	20 to 155
	FO03	I_{OL} = 18.0 mA	100 to 230
	FO06	I_{OL} = 24.0 mA	120 to 300
LVTTL Low-noise Type	FE04	I_{OL} = 6.0 mA	0 to 90
	FE01	I_{OL} = 9.0 mA	0 to 135
	FE02	I_{OL} = 12.0 mA	20 to 180
	FE03	I_{OL} = 18.0 mA	25 to 200
	FE06	I_{OL} = 24.0 mA	35 to 250
TTL 5 V tolerant Normal Type	FV0A	I_{OL} = 1.0 mA	0 to 20
	FV0B	I_{OL} = 2.0 mA	0 to 35
	FV09	I_{OL} = 3.0 mA	0 to 40
	FV04	I_{OL} = 6.0 mA	0 to 75
	FV01	I_{OL} = 9.0 mA	15 to 110
	FV02	I_{OL} = 12.0 mA	20 to 155
	FV03	I_{OL} = 18.0 mA	100 to 230
	FV06	I_{OL} = 24.0 mA	120 to 300
TTL 5 V tolerant Low-noise Type	FW02	I_{OL} = 12.0 mA	20 to 170
	FW03	I_{OL} = 18.0 mA	20 to 170
	FW06	I_{OL} = 24.0 mA	20 to 170
5 V full-swing Normal Type	FV0AAL	I_{OL} = 1.0 mA	0 to 25
	FV0BAL	I_{OL} = 2.0 mA	0 to 50
	FV09AL	I_{OL} = 3.0 mA	0 to 85
	FV04AL	I_{OL} = 6.0 mA	0 to 150
	FV01AL	I_{OL} = 9.0 mA	5 to 230
	FV02AL	I_{OL} = 12.0 mA	20 to 290
	FV03AL	I_{OL} = 18.0 mA	50 to 300
5 V full-swing Low-noise Type	FW09AL	I_{OL} = 3.0 mA	0 to 87
	FW04AL	I_{OL} = 6.0 mA	0 to 160
	FW02AL	I_{OL} = 12.0 mA	0 to 200
	FW03AL	I_{OL} = 18.0 mA	0 to 200

5.5.3 Maximum operating frequency for output buffers

The maximum operating frequency of the output buffer is determined by the drive capability and the load capacitance. As explained in **5.5.2 Recommended load capacitance range for output buffers**, there are recommended ranges for load capacitance. The diagonally shaded parts of the graphs in Figures 5-16 through 5-21 correspond to these ranges. Use the buffer types described in **7.1** for the interface for SiP internal connections. (Operation assuming the use of SBUSCLK = 66.6 MHz has been confirmed.)

The right sides of the diagonally shaded parts can be used if there are no problems with the propagation delay time, rise time, and fall time. On the other hand, there is large overshoot and undershoot in the left sides.

Moreover, the output maximum operating frequencies shown in Figures 5-16 through 5-21 are specified assuming that only capacitances are connected to the output pins. Consequently, there is a slight fluctuation if inductance is taken into consideration. In addition, because the waveform of the CMOS 5 V tolerant interface changes greatly according to the pull-up resistance value, the output waveform is shown for stated conditions.

Caution Calculate tr and tf of the output signal to confirm that the output pulse width satisfies the input specifications of the other device.

Figure 5-16. Restrictions for f_{MAX} vs. C_L (LVTTL Output, Normal Type) (1/2)

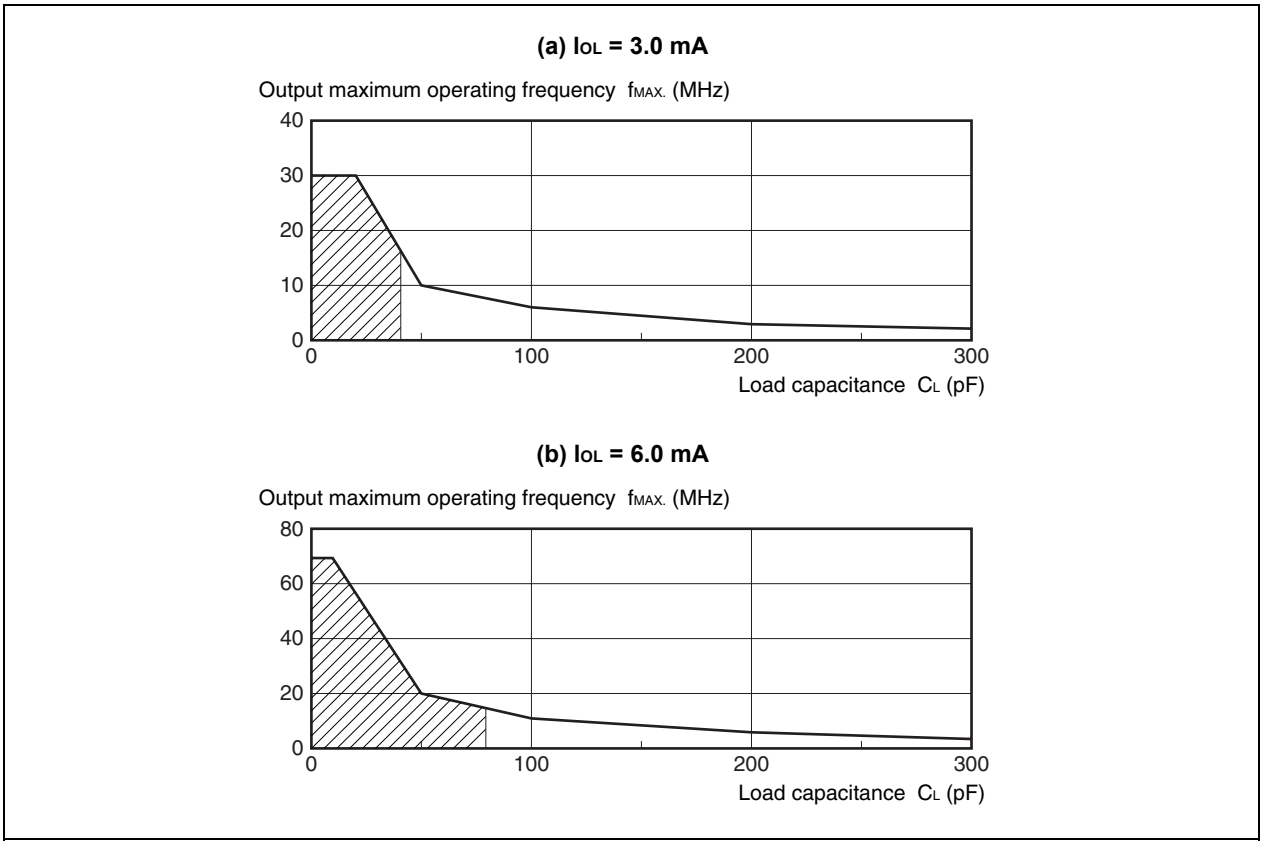
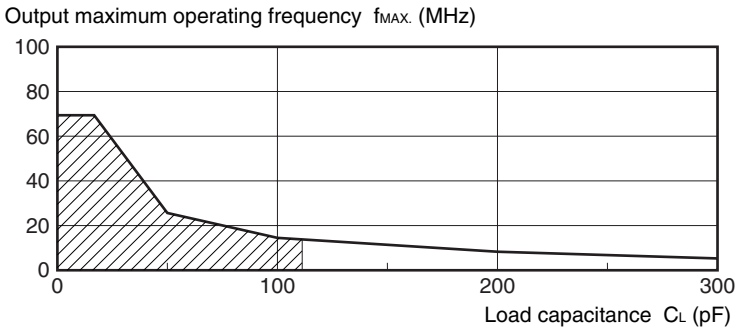
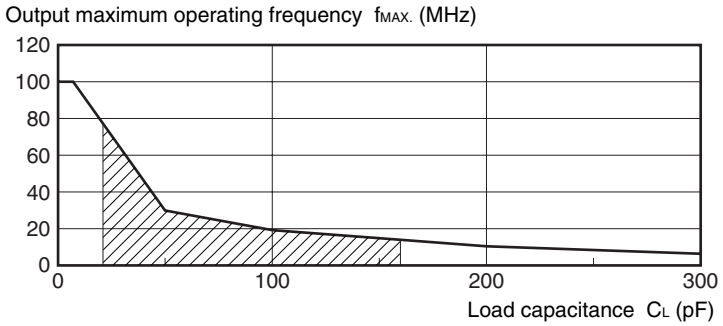


Figure 5-16. Restrictions for f_{MAX} vs C_L (LVTTL Output, Normal Type) (2/2)

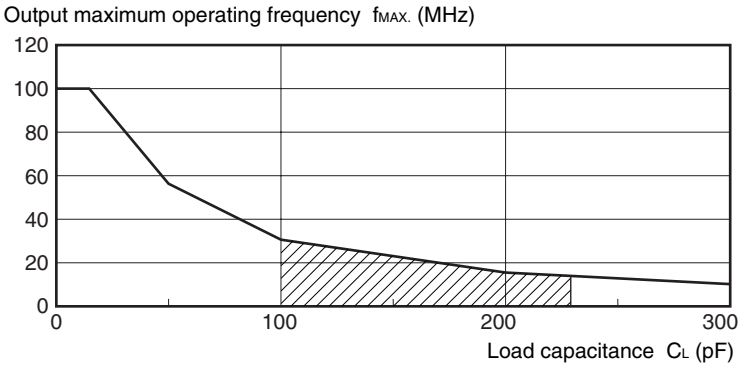
(c) I_{OL} = 9.0 mA



(d) I_{OL} = 12.0 mA



(e) I_{OL} = 18.0 mA



(f) I_{OL} = 24.0 mA

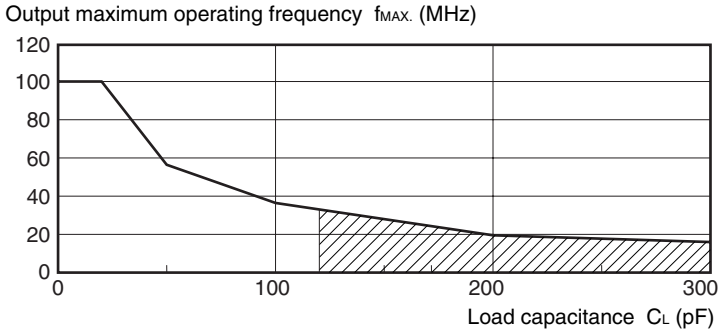
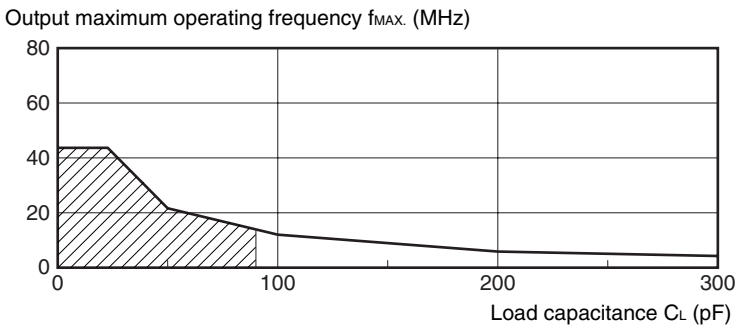
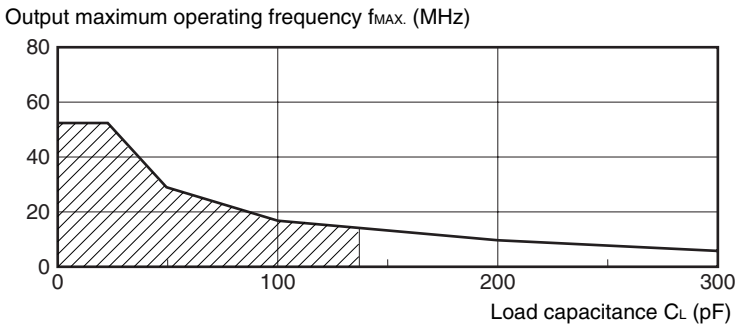


Figure 5-17. Restrictions for f_{MAX} vs. C_L (LVTTL Output, Low-Noise Type) (1/2)

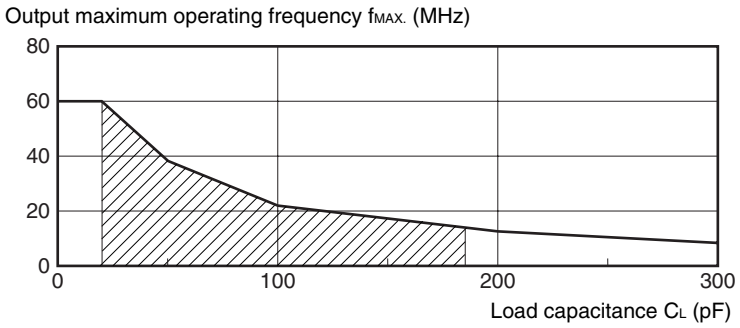
(a) I_{OL} = 6.0 mA (FE04)



(b) I_{OL} = 9.0 mA (FE01)



(c) I_{OL} = 12.0 mA (FE02)



(d) I_{OL} = 18.0 mA (FE03)

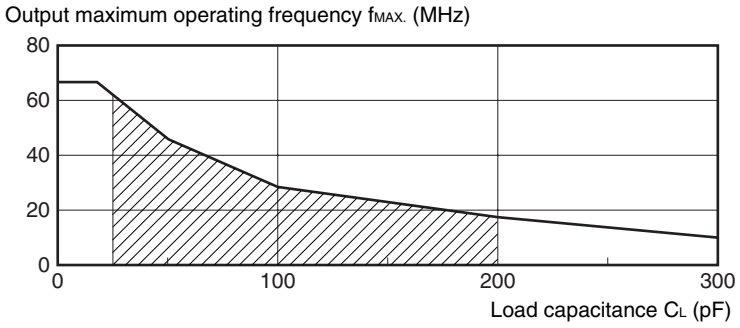


Figure 5-17. Restrictions for f_{MAX} vs. C_L (LVTTL Output, Low-Noise Type) (2/2)

(e) I_{OL} = 24.0 mA (FE06)

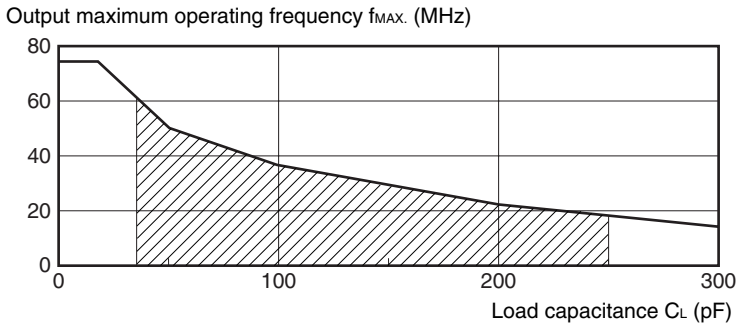
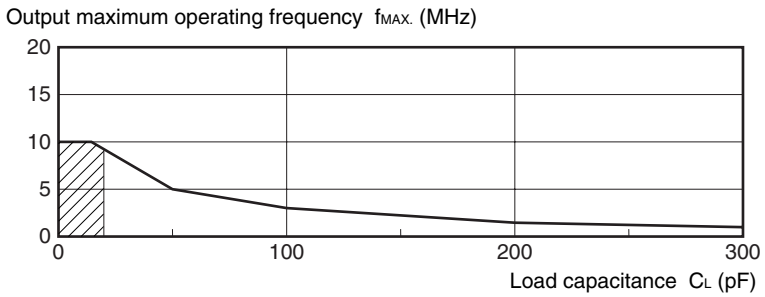
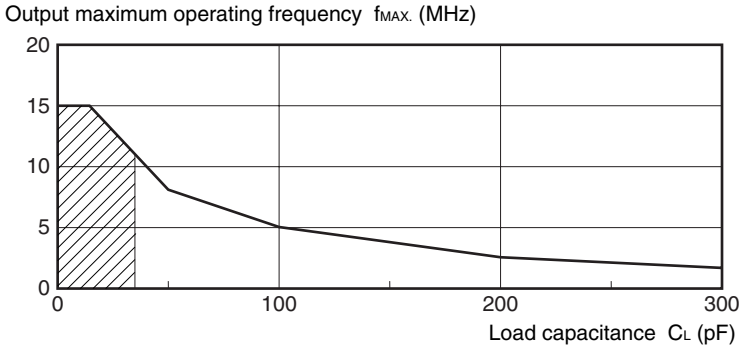


Figure 5-18. Restrictions for f_{MAX} vs. C_L (TTL 5 V Tolerant Output, Normal Type) (1/2)

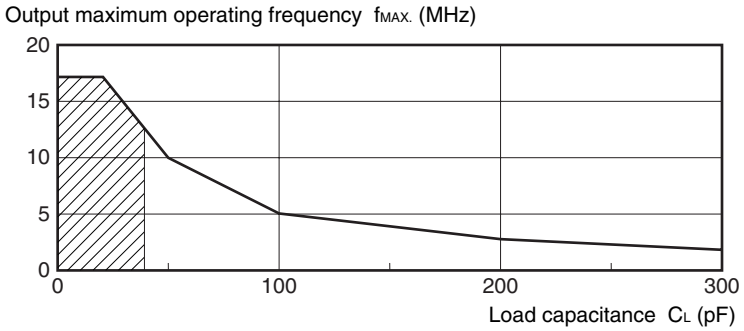
(a) I_{OL} = 1.0 mA



(b) I_{OL} = 2.0 mA



(c) I_{OL} = 3.0 mA



(d) I_{OL} = 6.0 mA

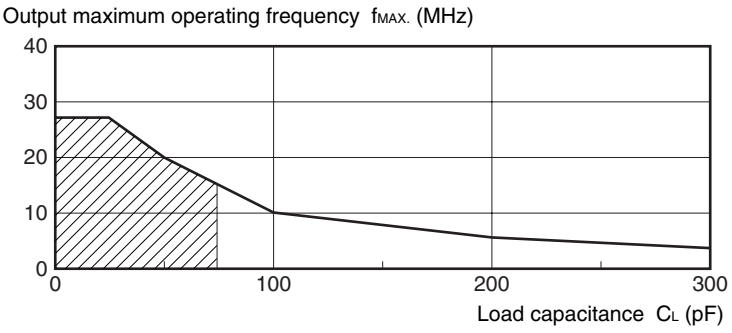
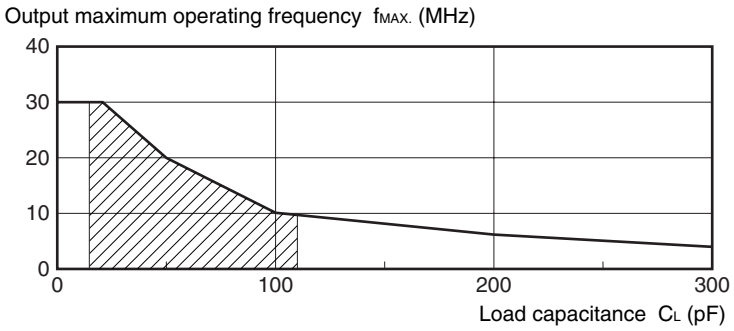
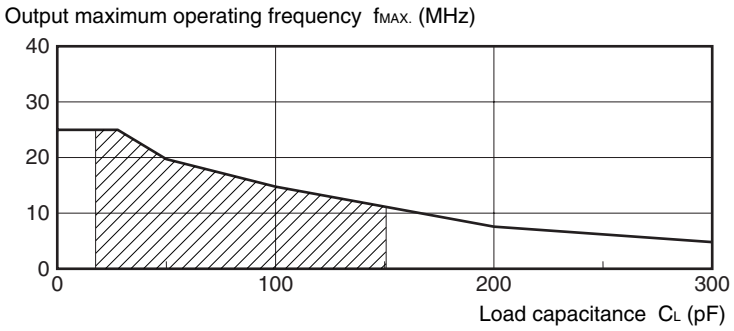


Figure 5-18. Restrictions for f_{MAX} vs. C_L (TTL 5 V Tolerant Output, Normal Type) (2/2)

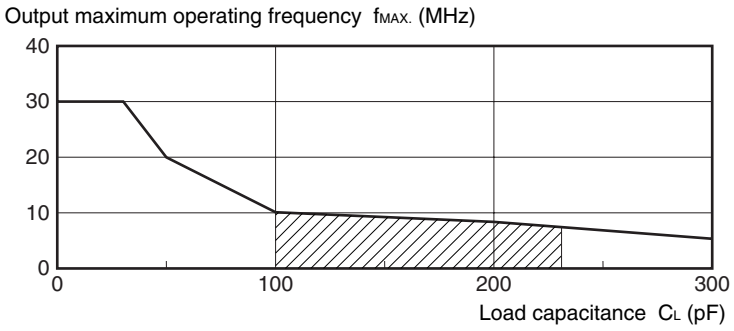
(e) I_{OL} = 9.0 mA



(f) I_{OL} = 12.0 mA



(g) I_{OL} = 18.0 mA



(h) I_{OL} = 24.0 mA

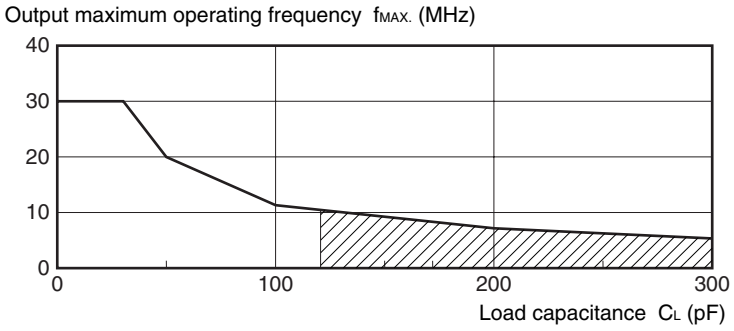
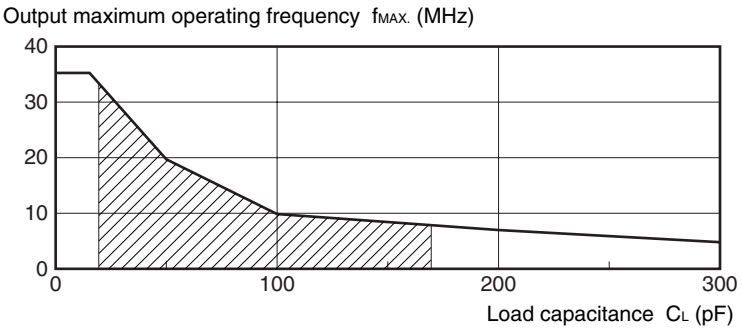
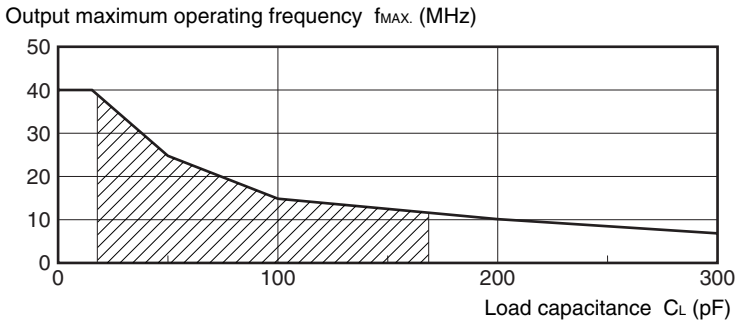


Figure 5-19. Restrictions for f_{MAX} vs. C_L (TTL 5 V Tolerant Output, Low-Noise Type)

(a) I_{OL} = 12.0 mA



(b) I_{OL} = 18.0 mA



(c) I_{OL} = 24.0 mA

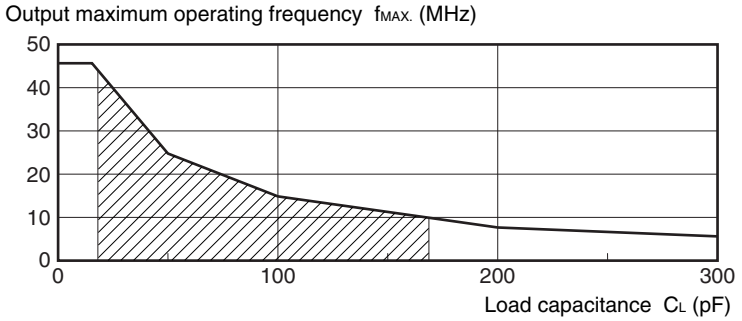
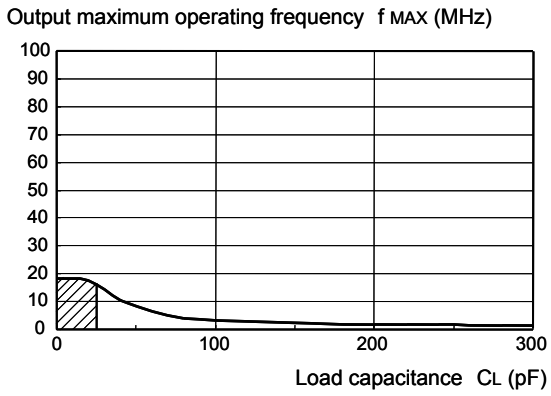
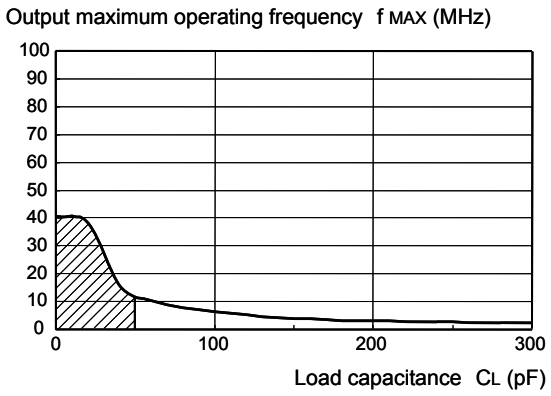


Figure 5-20. Restrictions for f_{MAX} vs. C_L (5 V Full-Swing, Normal Type) (1/2)

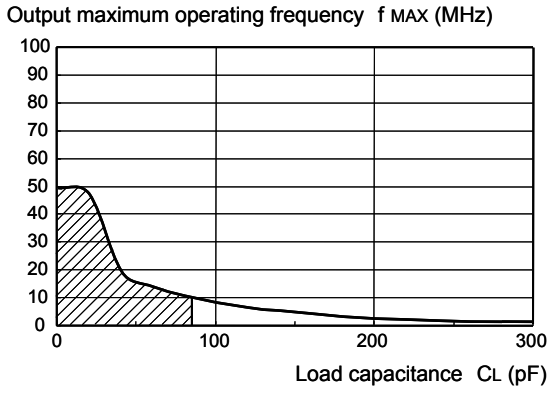
(a) FV0AAL (I_{OL} = 1.0 mA)



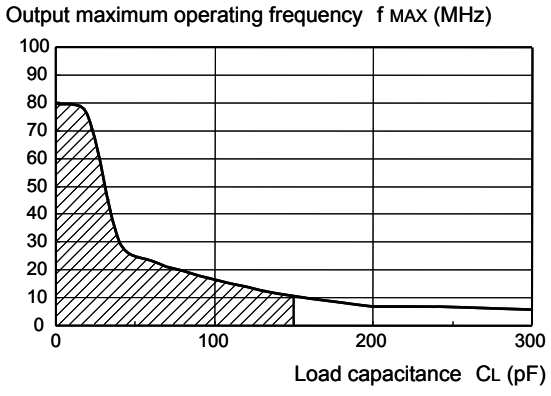
(b) FV0BAL (I_{OL} = 2.0 mA)



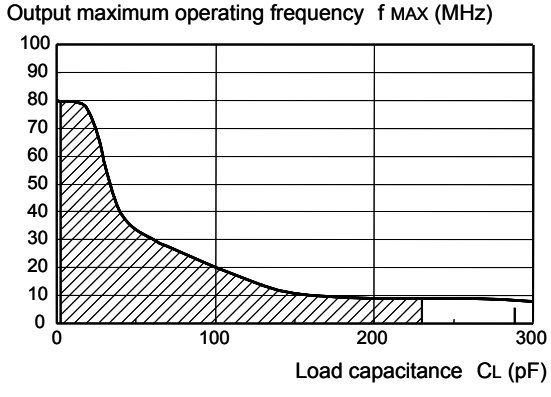
(c) FV09AL (I_{OL} = 3.0 mA)



(d) FV04AL (I_{OL} = 6.0 mA)



(e) FV01AL (I_{OL} = 9.0 mA)



(f) FV02AL (I_{OL} = 12.0 mA)

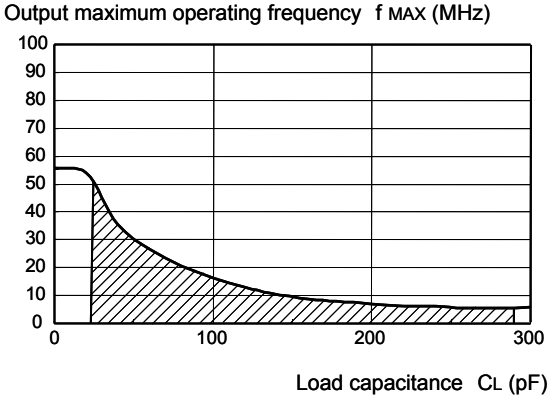


Figure 5-20. Restrictions for f_{MAX} vs. C_L (5 V Full-Swing, Normal Type) (2/2)

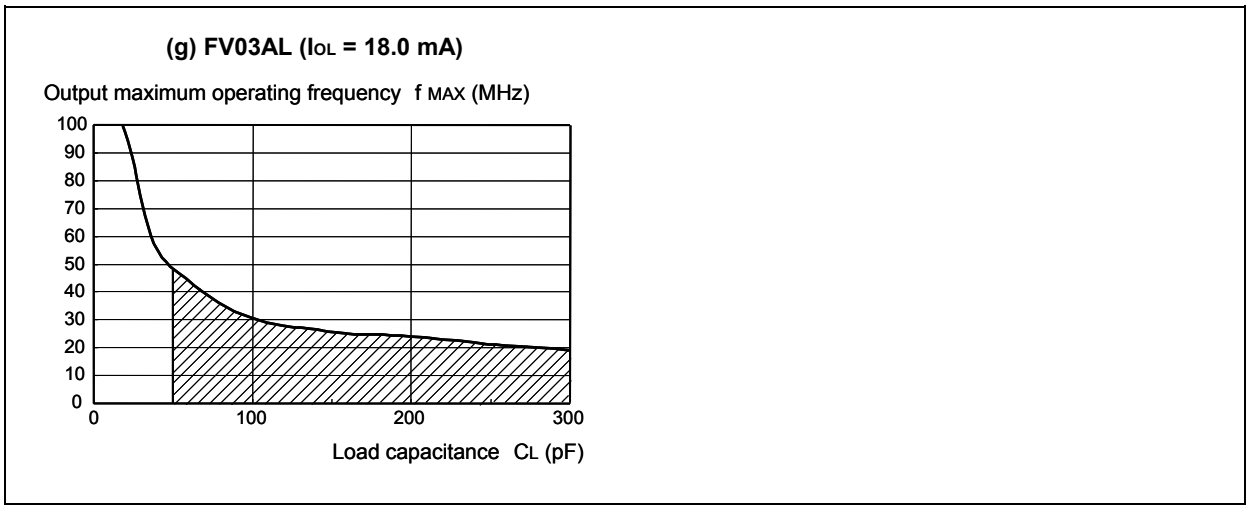
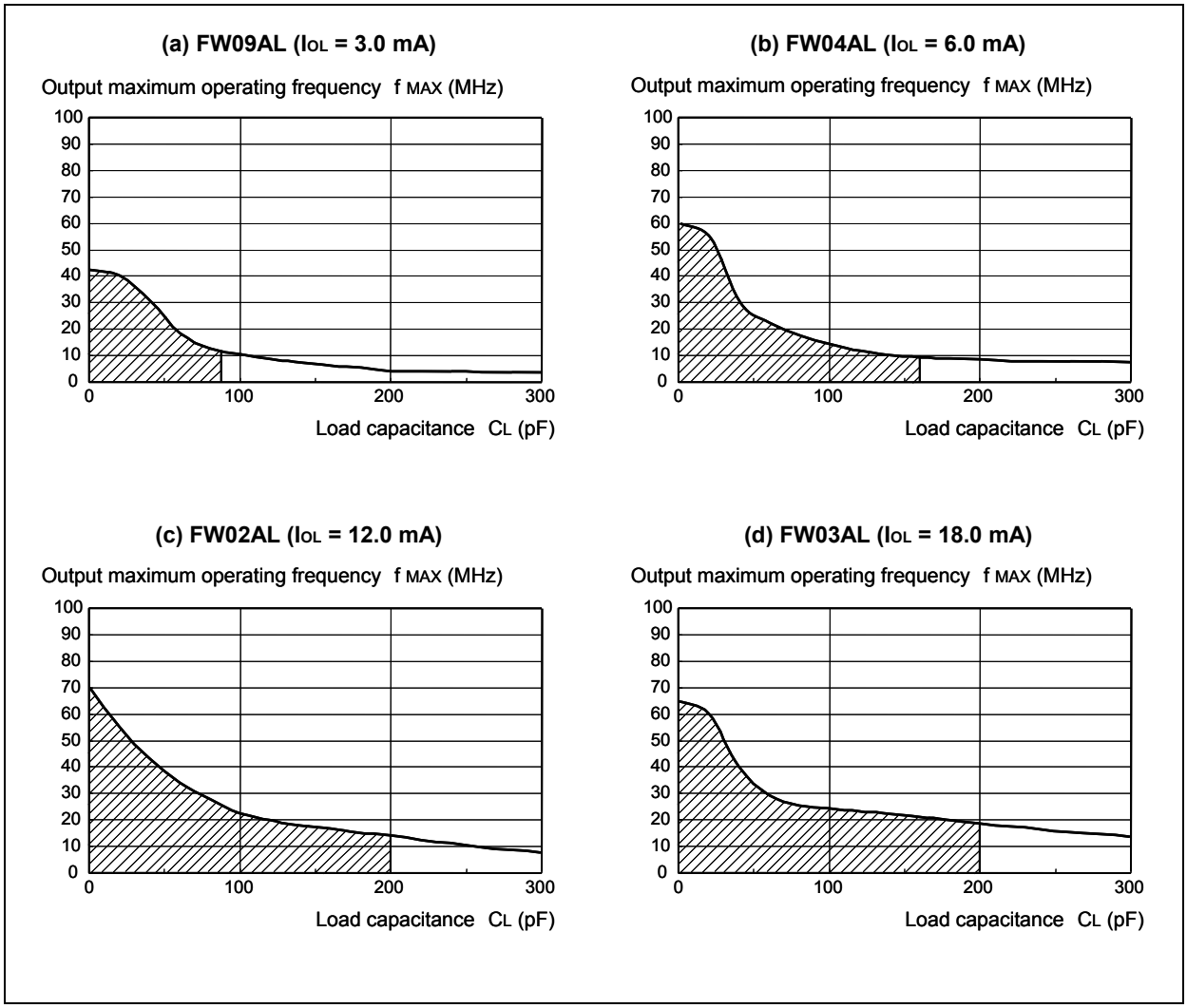


Figure 5-21. Restrictions for f_{MAX} vs. C_L (5 V Full-Swing, Low-Noise Type)



The CMOS 5 V tolerant output waveforms shown in Figures 5-22 and 5-23 show the output waveform for the following conditions:

V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Evaluation circuit

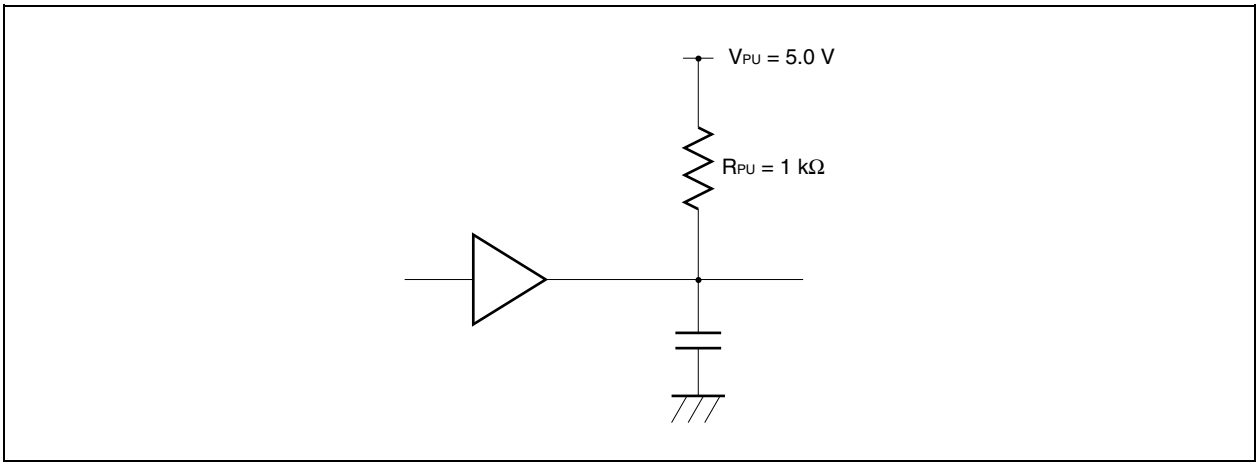
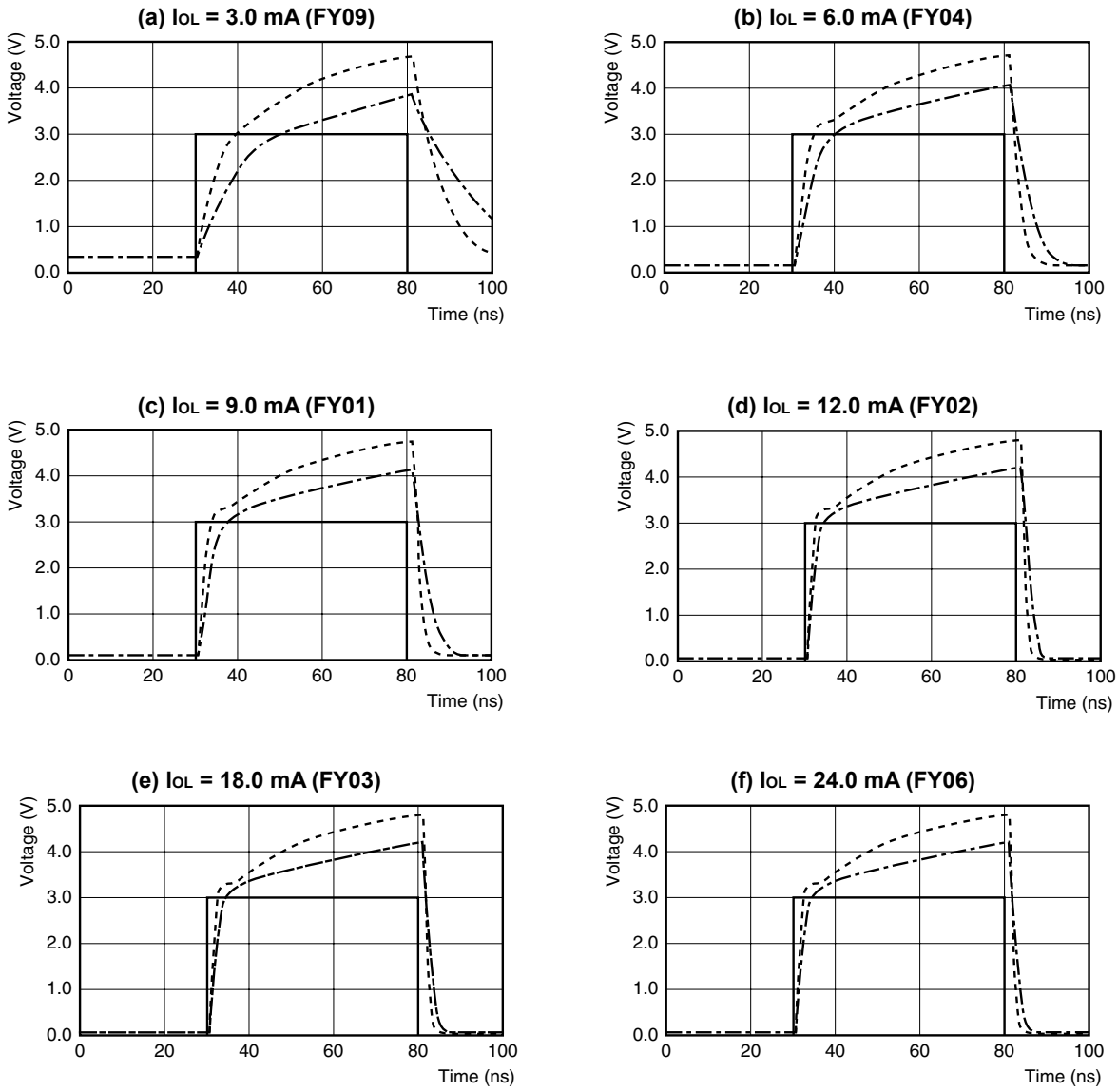


Figure 5-22. Output Waveforms (CMOS 5 V Tolerant Output, Normal Type)



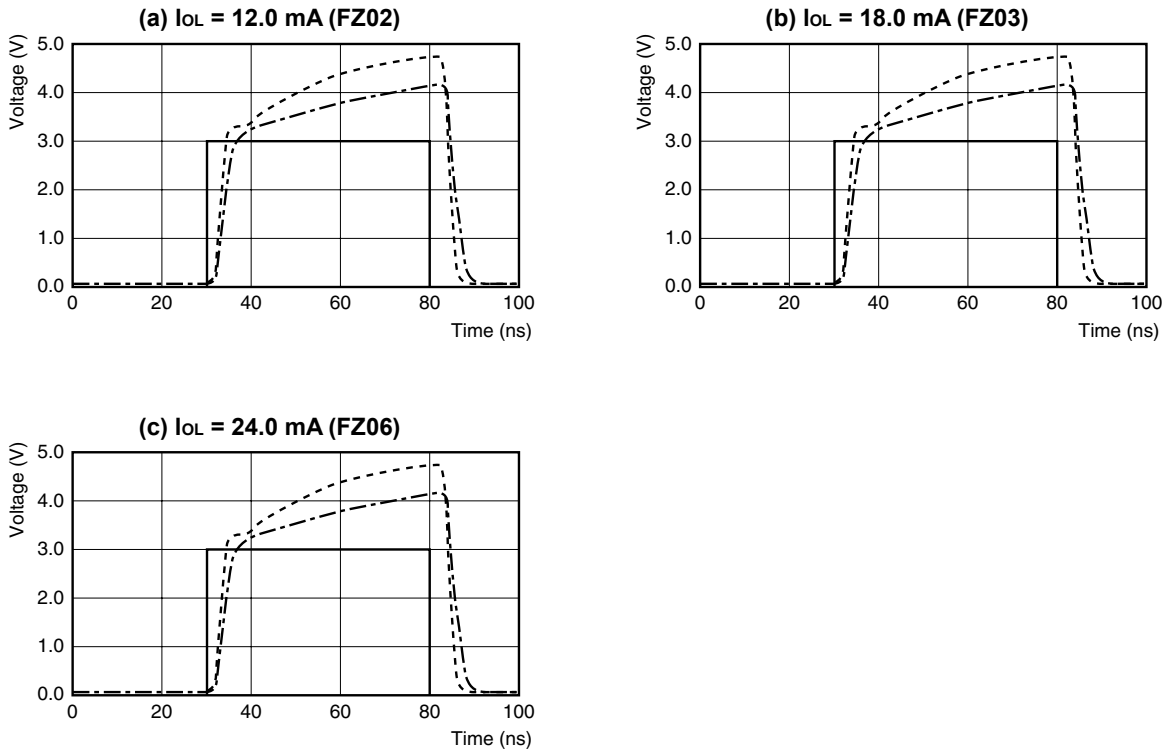
Remark Each line in the above figures shows the following waveform.

——————— : Input signal

- - - - - - - - - - - - - : with load capacitance (output for 15 pF)

—·—·—·—·—·— : with load capacitance (output for 50 pF)

Figure 5-23. Output Waveforms (CMOS 5 V Tolerant Output, Low-Noise Type)



Remark Each line in the above figures shows the following waveform.

——————— : Input signal

- - - - - - - - - - - - - : with load capacitance (output for 15 pF)

—·—·—·—·—·— : with load capacitance (output for 50 pF)

5.5.4 Output buffer output current (I_{OL}, I_{OH})

NEC Electronics defines the output current of EP-1 series at V_{OL} = 0.4 V and V_{OH} = 2.4 V. However, there are cases in which the V_{OL} and V_{OH} used differ for actual applications. In such cases, the coefficients shown below should be used in estimating the I_{OL} and I_{OH} characteristics in accordance with the actual conditions.

• Dependency on output voltage

V_{OL} = 0.4 to 0.6 V, V_{OH} = (V_{DD} – 0.4 V) to (V_{DD} – 0.6 V)

Because I_{OL} and I_{OH} vary almost proportionately to the output voltage, a direct approximation is possible. However, this excludes the I_{OH} of the TTL level output buffer.

Equations for estimating the output buffer current

$I_{OL}' = I_{OL} \times V_{OL}/0.4$ (mA)

$I_{OH}' = I_{OH} \times (V_{DD} - V_{OH})/0.6$ (mA)

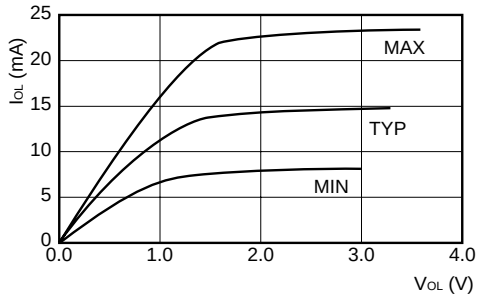
I_{OL} : I_{OL} specification when V_{OL} = 0.4 V
V_{OL} : V_{OL} value used
I_{OH} : I_{OH} specification when V_{OH} = 2.4 V
V_{OH} : V_{OH} value used

The I_O vs. V_O curves are shown from Figure 5-24. The MIN. curve is shown for the conditions V_{DD} = 3.0 V and T_J = 125°C. The TYP. curve is shown for the conditions V_{DD} = 3.3 V and T_J = 25°C. The MAX. curve is shown for the conditions V_{DD} = 3.6 V and T_J = –40°C. The direct currents I_{OH} and I_{OL} that can actually be used should be within the absolute maximum ratings. Furthermore, the CMOS 5 V output buffer is configured to cut off the direct current I_{OH}, and the V_O vs. I_O curve cannot be shown for the MIN. and MAX. conditions.

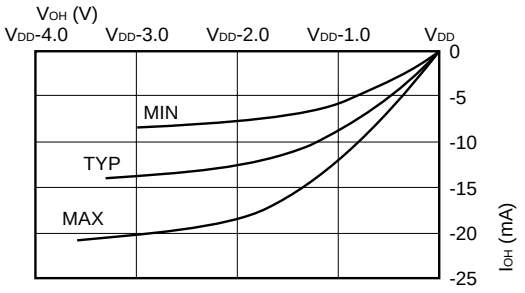
Figure 5-24. I_O vs V_O (1/9)

(1) LVTTL output type; I_{OL} = 3 mA (Representative block type: FO09)

(a) I_{OL} vs V_{OL}

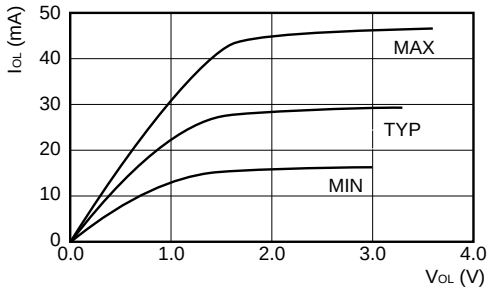


(b) I_{OH} vs V_{OH}

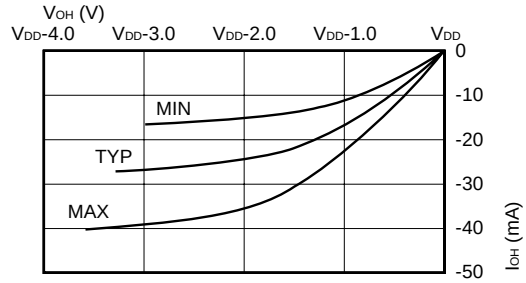


(2) LVTTL output type; I_{OL} = 6 mA (Representative block type: FO04, FE04)

(a) I_{OL} vs V_{OL}

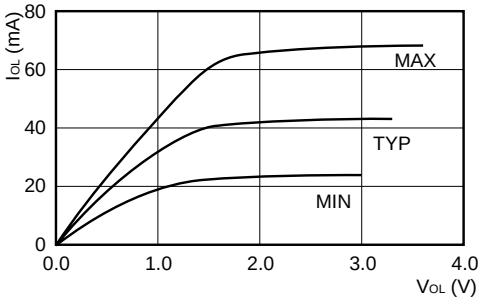


(b) I_{OH} vs V_{OH}

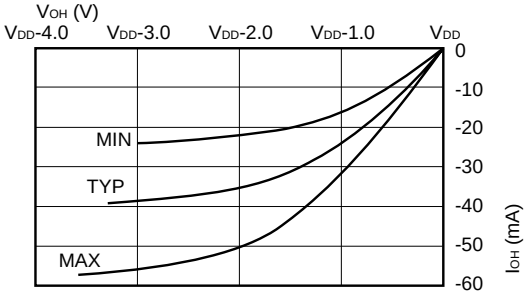


(3) LVTTL output type; I_{OL} = 9 mA (Representative block type: FO01, FE01)

(a) I_{OL} vs V_{OL}

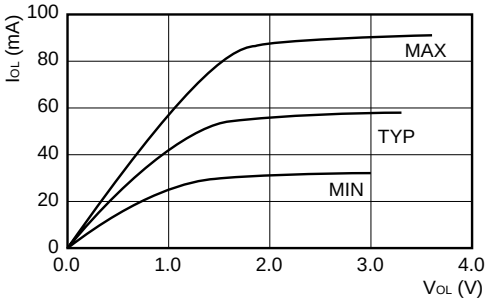


(b) I_{OH} vs V_{OH}



(4) LVTTL output type; I_{OL} = 12 mA (Representative block type: FO02, FE02)

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

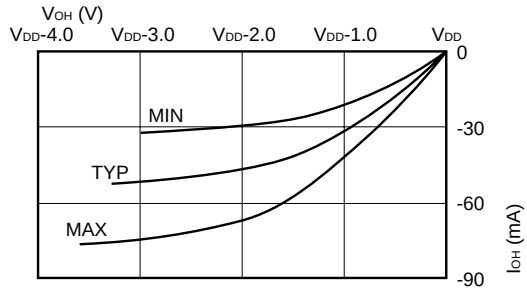
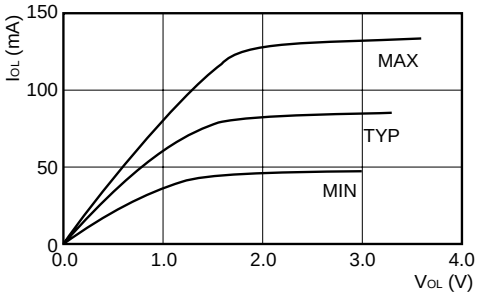


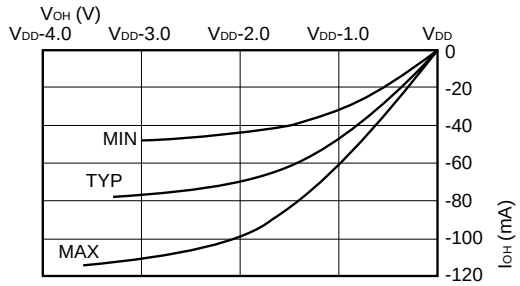
Figure 5-24. I_O vs V_O (2/9)

(5) LVTTL output type; I_{OL} = 18 mA(Representative block type: FO03, FE03)

(a) I_{OL} vs V_{OL}

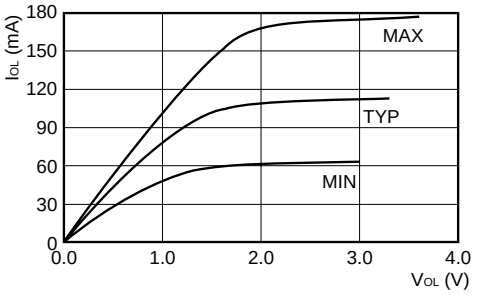


(b) I_{OH} vs V_{OH}

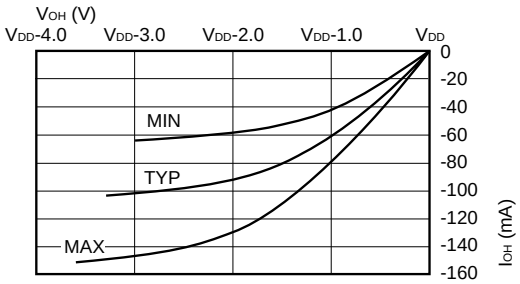


(6) LVTTL output type; I_{OL} = 24 mA (Representative block type: FO06, FE06)

(a) I_{OL} vs V_{OL}

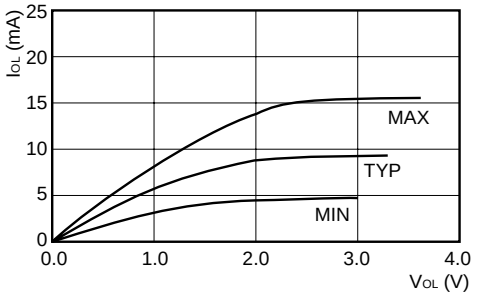


(b) I_{OH} vs V_{OH}

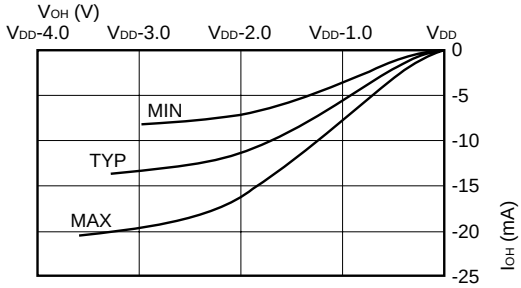


(7) TTL 5 V tolerant output, normal type; I_{OL} = 1 mA (Representative block type: FV0A)

(a) I_{OL} vs V_{OL}

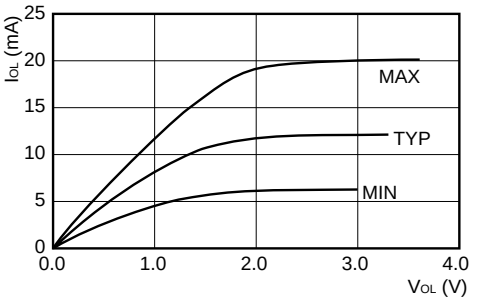


(b) I_{OH} vs V_{OH}



(8) TTL 5 V tolerant output, normal type; I_{OL} = 2 mA (Representative block type: FV0B)

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

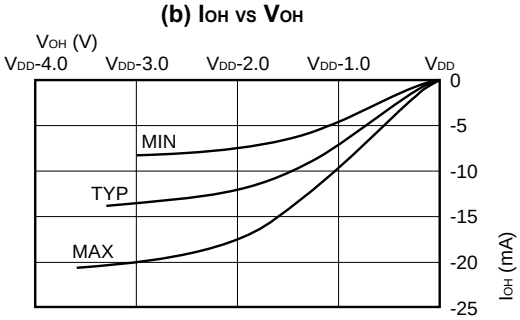
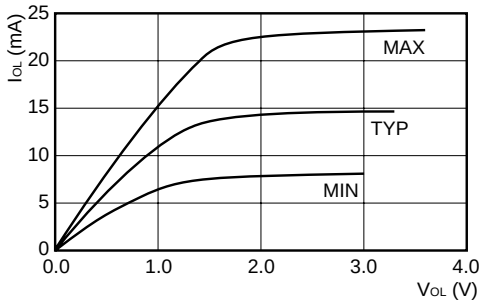


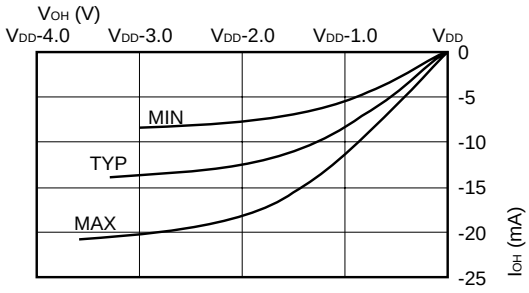
Figure 5-24. I_O vs V_O (3/9)

(9) TTL 5 V tolerant output, normal type; I_{OL} = 3 mA (Representative block type: FV09)

(a) I_{OL} vs V_{OL}

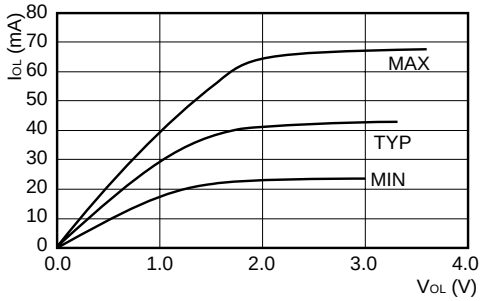


(b) I_{OH} vs V_{OH}

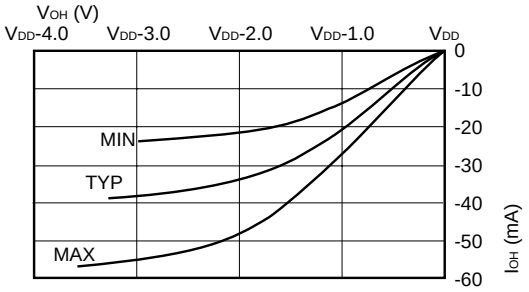


(10) TTL 5 V tolerant output, normal type; I_{OL} = 6 mA (Representative block type: FV04)

(a) I_{OL} vs V_{OL}

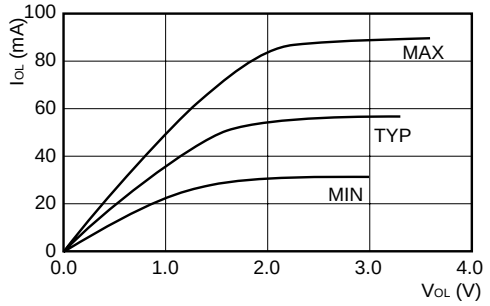


(b) I_{OH} vs V_{OH}

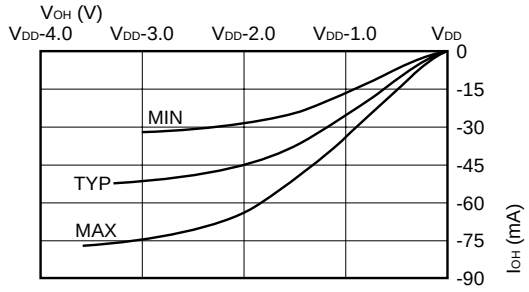


(11) TTL 5 V tolerant output, normal type; I_{OL} = 9 mA (Representative block type: FV01)

(a) I_{OL} vs V_{OL}

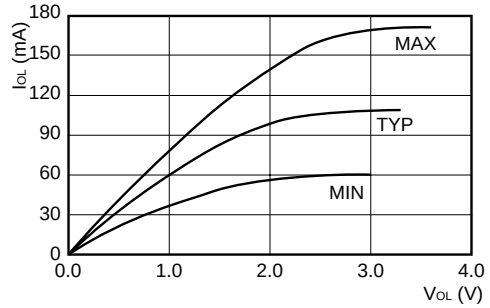


(b) I_{OH} vs V_{OH}



(12) TTL 5 V tolerant output, normal type; I_{OL} = 12 mA (Representative block type: FV02)

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

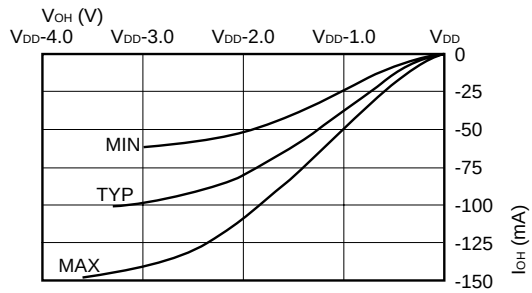
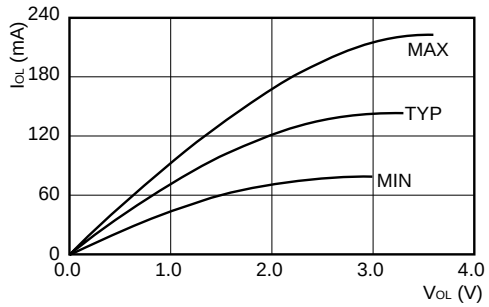


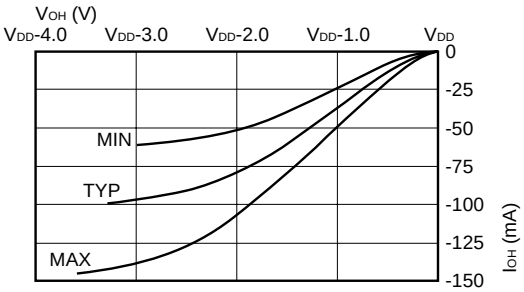
Figure 5-24. I_O vs V_O (4/9)

(13) TTL 5 V tolerant output, normal type; I_{OL} = 18 mA (Representative block type: FV03)

(a) I_{OL} vs V_{OL}

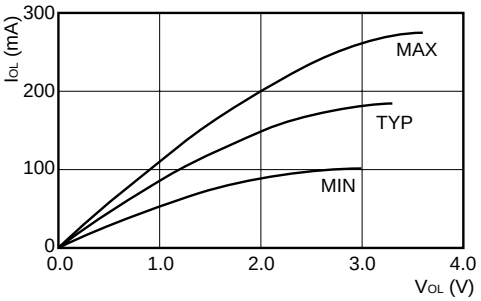


(b) I_{OH} vs V_{OH}

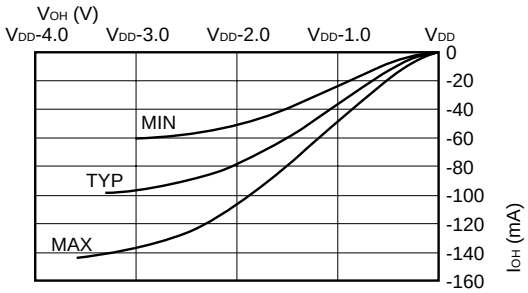


(14) TTL 5 V tolerant output, normal type; I_{OL} = 24 mA (Representative block type: FV06)

(a) I_{OL} vs V_{OL}

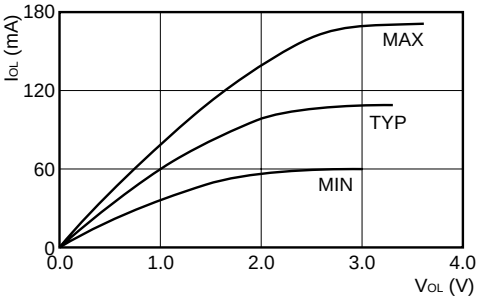


(b) I_{OH} vs V_{OH}

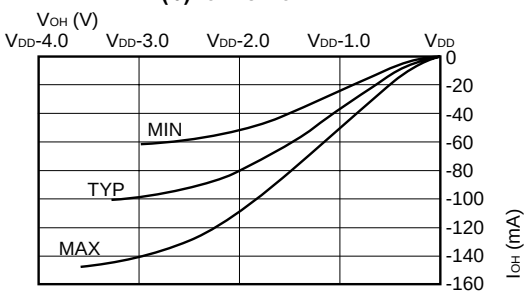


(15) TTL 5 V tolerant output, low noise type; I_{OL} = 12 mA (Representative block type: FW02)

(a) I_{OL} vs V_{OL}

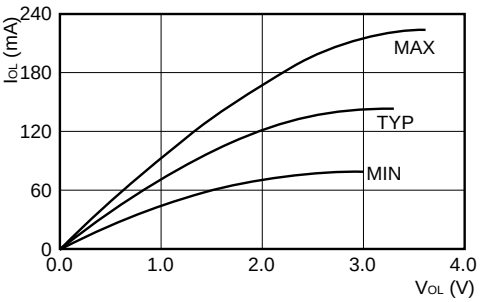


(b) I_{OH} vs V_{OH}



(16) TTL 5 V tolerant output, low noise type; I_{OL} = 18 mA (Representative block type: FW03)

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

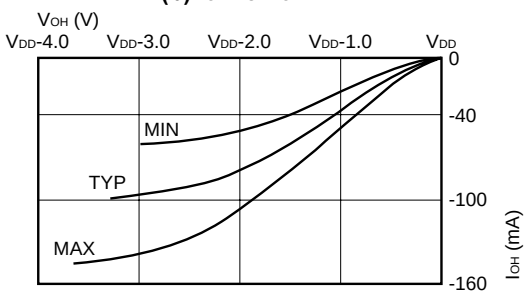
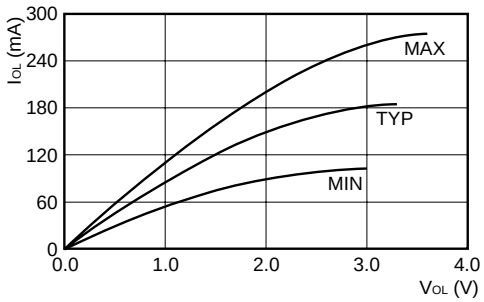


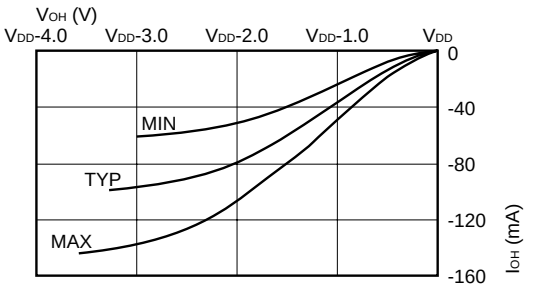
Figure 5-24. I_O vs V_O (5/9)

(17) TTL 5 V tolerant output, low noise type; I_{OL} = 24 mA (Representative block type: FW06)

(a) I_{OL} vs V_{OL}

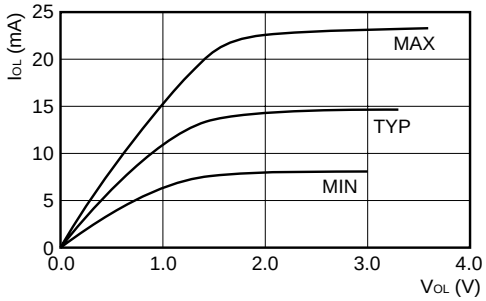


(b) I_{OH} vs V_{OH}

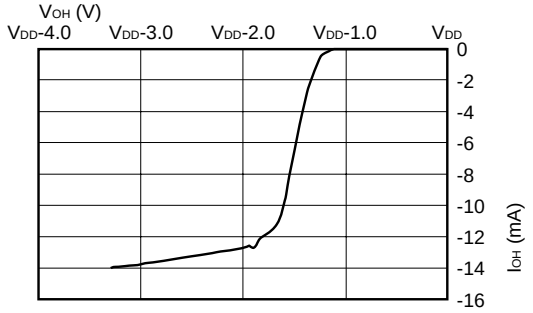


(18) CMOS 5 V tolerant output, normal type; I_{OL} = 3 mA (Representative block type: FY09)

(a) I_{OL} vs V_{OL}

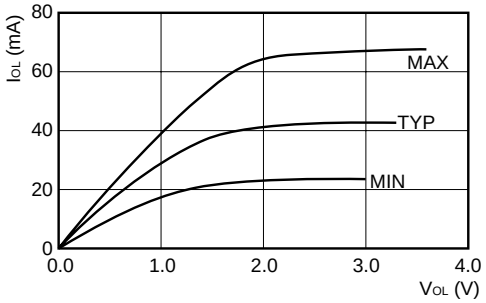


(b) I_{OH} vs V_{OH}

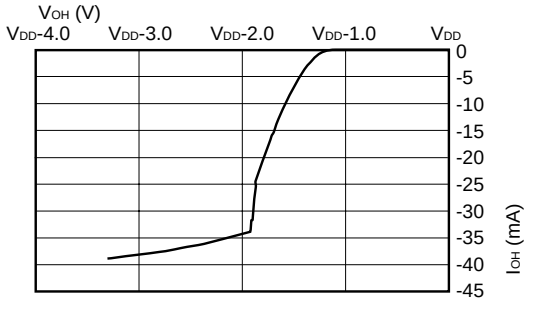


(19) CMOS 5 V tolerant output, normal type; I_{OL} = 6 mA (Representative block type: FY04)

(a) I_{OL} vs V_{OL}

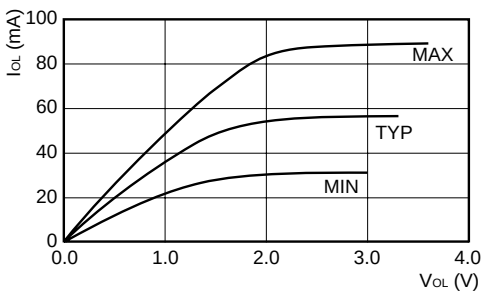


(b) I_{OH} vs V_{OH}



(20) CMOS 5 V tolerant output, normal type; I_{OL} = 9 mA (Representative block type: FY01)

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

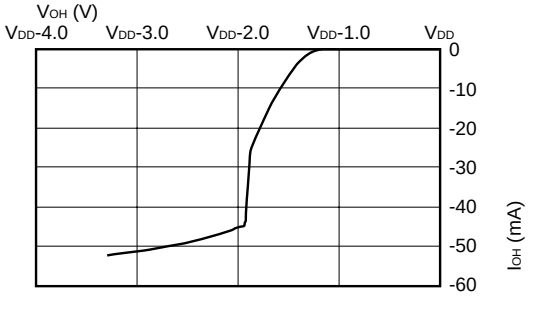
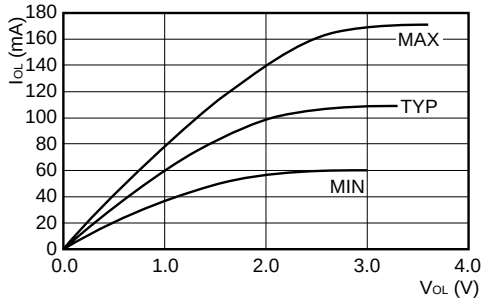


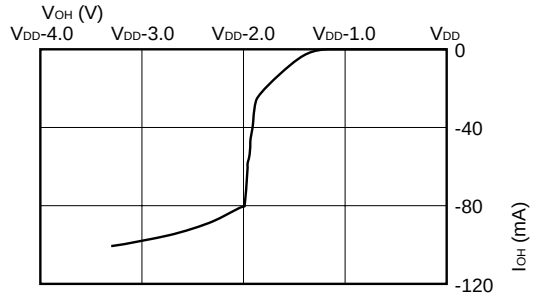
Figure 5-24. I_O vs V_O (6/9)

(21) CMOS 5 V tolerant output, normal type; I_{OL} = 12 mA (Representative block type: FY02)

(a) I_{OL} vs V_{OL}

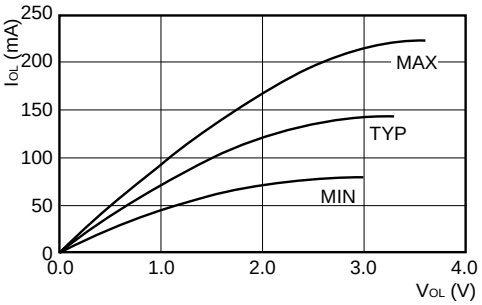


(b) I_{OH} vs V_{OH}

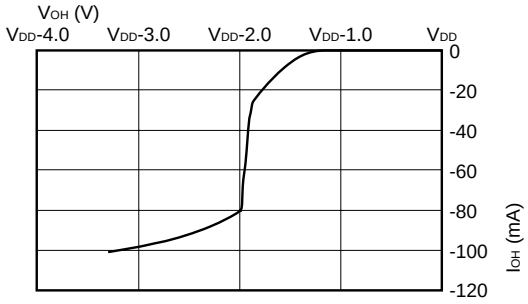


(22) CMOS 5 V tolerant output, normal type; I_{OL} = 18 mA (Representative block type: FY03)

(a) I_{OL} vs V_{OL}

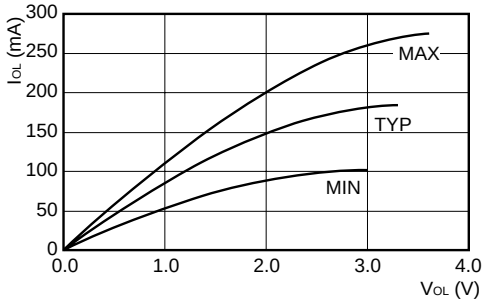


(b) I_{OH} vs V_{OH}

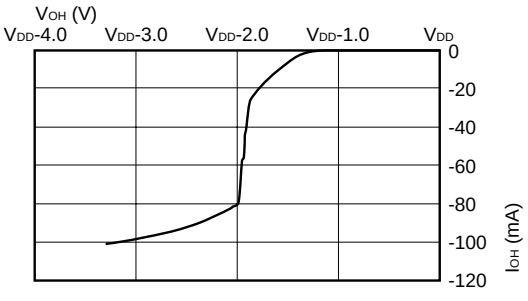


(23) CMOS 5 V tolerant output, normal type; I_{OL} = 24 mA (Representative block type: FY06)

(a) I_{OL} vs V_{OL}

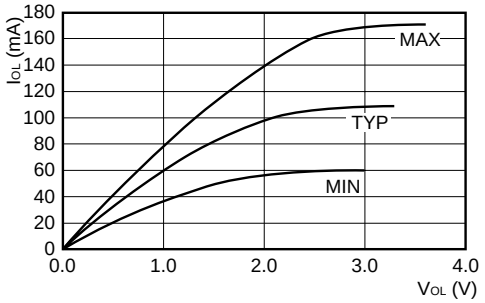


(b) I_{OH} vs V_{OH}



(24) CMOS 5 V tolerant output, low noise type; I_{OL} = 12 mA (Representative block type: FZ02)

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

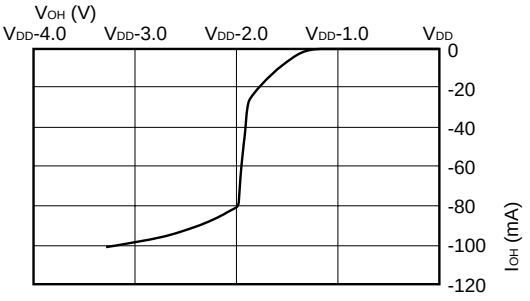
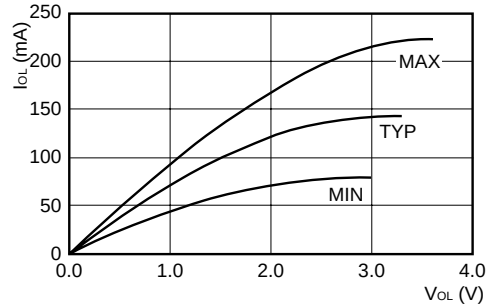


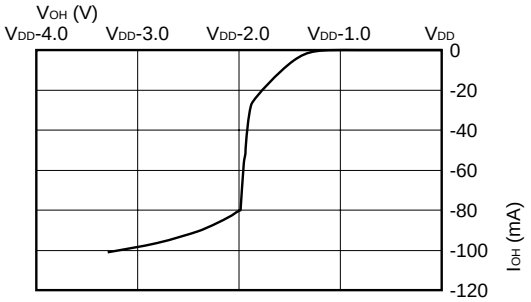
Figure 5-24. I_O vs V_O (7/9)

(25) CMOS 5 V tolerant output, low noise type; I_{OL} = 18 mA (Representative block type: FZ03)

(a) I_{OL} vs V_{OL}

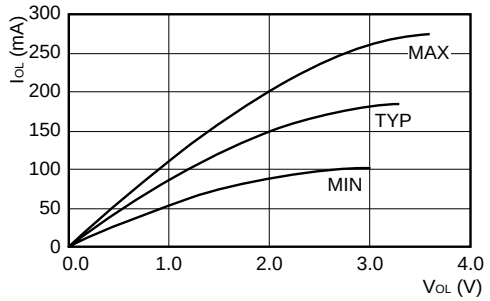


(b) I_{OH} vs V_{OH}

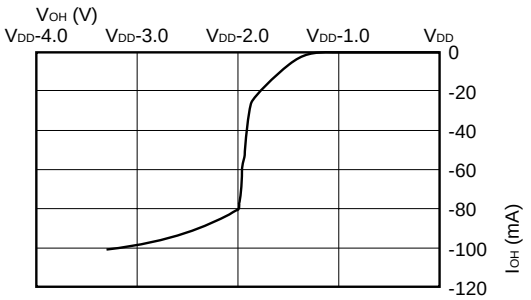


(26) CMOS 5 V tolerant output, low noise type; I_{OL} = 24 mA (Representative block type: FZ06)

(a) I_{OL} vs V_{OL}

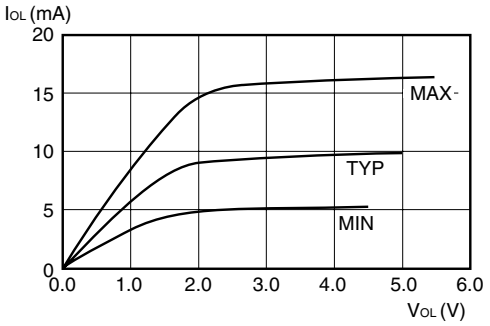


(b) I_{OH} vs V_{OH}

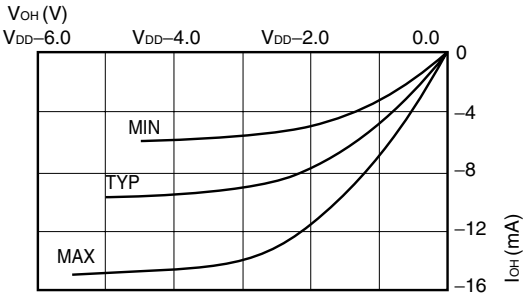


(27) 5 V full-swing output, I_{OL} = 1 mA (Representative block type: FV0AAL (normal type))

(a) I_{OL} vs V_{OL}

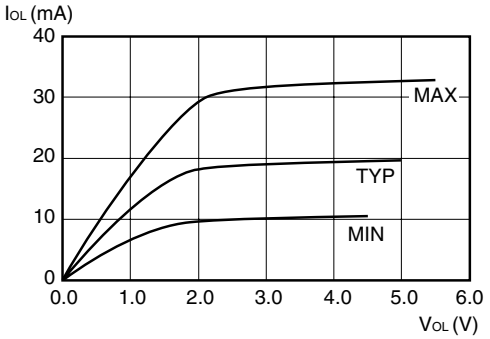


(b) I_{OH} vs V_{OH}



(28) 5 V full-swing output, I_{OL} = 2 mA (Representative block type: FV0BAL (normal type))

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

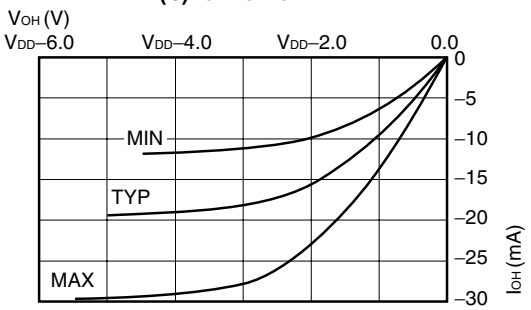
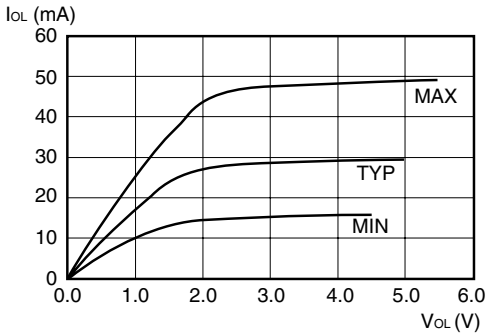


Figure 5-24. I_O vs V_O (8/9)

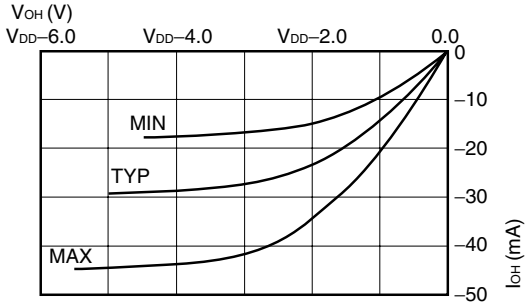
(29) 5 V full-swing output, I_{OL} = 3 mA

(Representative block type: FV09AL (normal type), FW09AL(low noise type))

(a) I_{OL} vs V_{OL}



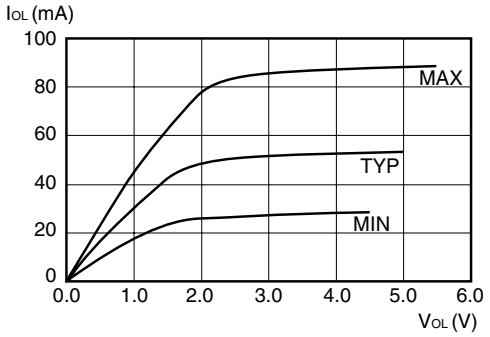
(b) I_{OH} vs V_{OH}



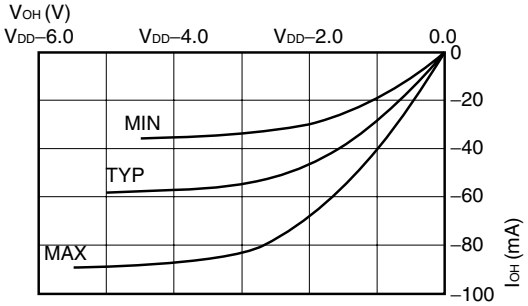
(30) 5 V full-swing output, I_{OL} = 6 mA

(Representative block type: FV04AL(normal type), FW04AL(low noise type))

(a) I_{OL} vs V_{OL}



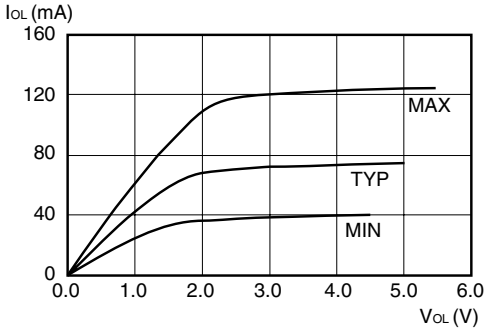
(b) I_{OH} vs V_{OH}



(31) 5 V full-swing output, I_{OL} = 9 mA

(Representative block type: FV01AL(normal type), FW01AL(low noise type))

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}

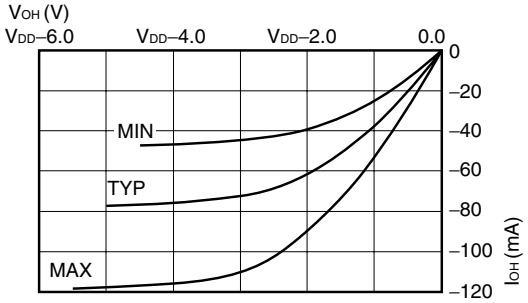
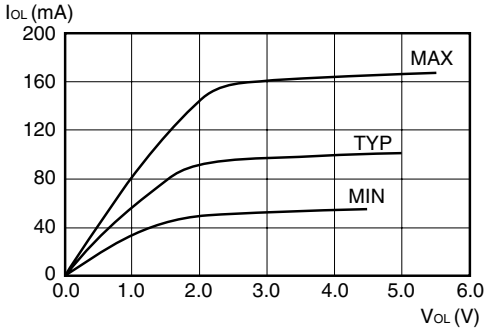


Figure 5-24. I_O vs V_O (9/9)

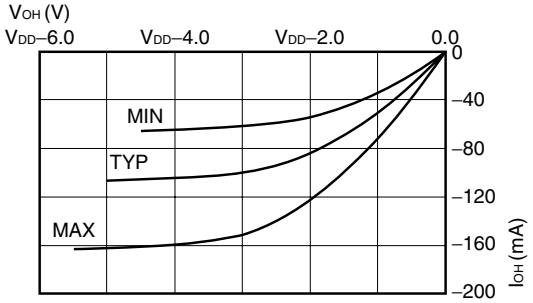
(32) 5 V full-swing output, I_{OL} = 12 mA

(Representative block type: FV02AL (normal type), FW02AL (low noise type))

(a) I_{OL} vs V_{OL}



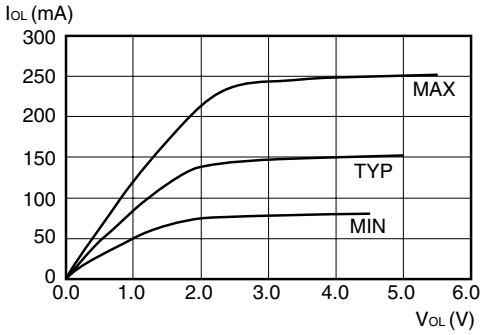
(b) I_{OH} vs V_{OH}



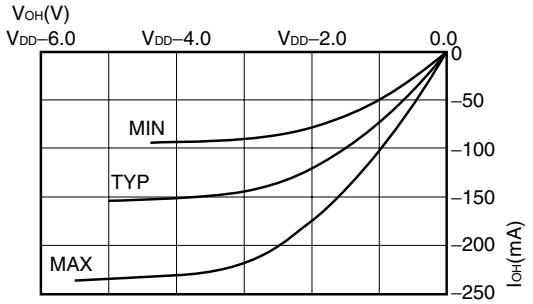
(33) 5 V full-swing output, I_{OL} = 18 mA

(Representative block type: FV03AL(normal type), FW03AL (low noise type))

(a) I_{OL} vs V_{OL}



(b) I_{OH} vs V_{OH}



5.6 Limits of Simultaneous Operation of Output Buffers

When the output buffer switches from low to high or from high to low, the current that charges/discharges the output load capacitance flows instantaneously to the power supply or GND line via the output buffer. Let i be charge/discharge currents and L the power supply inductance, then, the generated noise is expressed by $-L \times \Delta i/\Delta t$. It can be seen from this that the generated noise increases proportionately with changes in the charge/discharge currents and with the power supply inductance. The value of $\Delta i/\Delta t$ is determined by the output buffer type, and generally is larger for output buffers with large drive capability (more accurately, because the low-noise buffer $\Delta i/\Delta t$ value is determined by the drive capability of the large output transistors and by the input rise time (t_r) and input fall time (t_f) to those transistors, the value is smaller than for an output buffer that has the same drive capability). As the number of pins that switch simultaneously increases, the excessive charge/discharge currents increase, and sizable noise is generated in the power supply or GND line. This results in malfunction of the system.

There are two types of malfunctions as follows:

<1> The LSI malfunctions due to fluctuation of the LSI input threshold level
<2> The next stage circuit malfunctions due to noise appearing at the LSI output pin

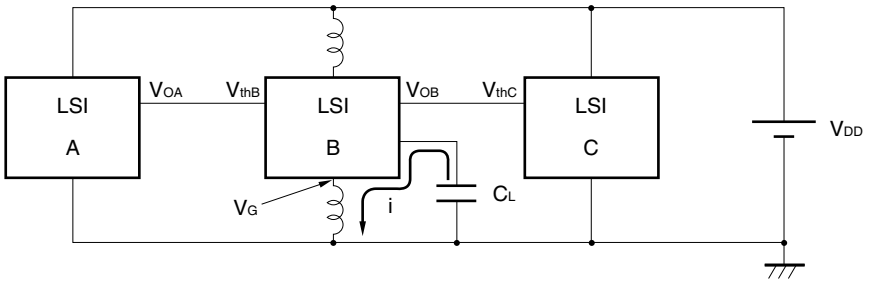
The circuit in Figure 5-25 (a) can be considered when the LSI's B output buffer is switched from H → L. When this happens, the load discharge current flows to the GND line on the mounted circuit board via the LSI B output buffer and the LSI internal GND line. As a result of this discharge current, inverse power arises in the inductance of the GND line, and the LSI internal GND level V_G rises, causing the malfunctions shown in Figure 5-25 (b) and (c). Furthermore, if the output buffer switches from L → H, charge current flows to the load capacitance, noise is generated in the power supply line, and the LSI internal V_{DD} level drops momentarily.

(1) In case when not using 18 mA or 24 mA type buffer, 9 mA or 12mA type 5 V tolerant buffer, and 9mA, 12mA, 18mA type 5V full-swing buffer (except low-nosie buffer), SSO checking do not need to be checked, because of sufficient placemnet of V_{DD}/GND PADS.

(2) In case when using 18 mA or 24 mA type buffers (normal type), 9 mA or 12mA type 5 V tolerant buffer (normal type), or 9mA, 12mA, 18mA type 5V full-swing buffer (normal type), SSO checking need to be checked, because if this is not done, there is the possibility that the SSO error will be occurred. However, in case when using low-noise buffer, SSO checking do not need to be checked. In case when using normal type above, consult NEC Electronics.

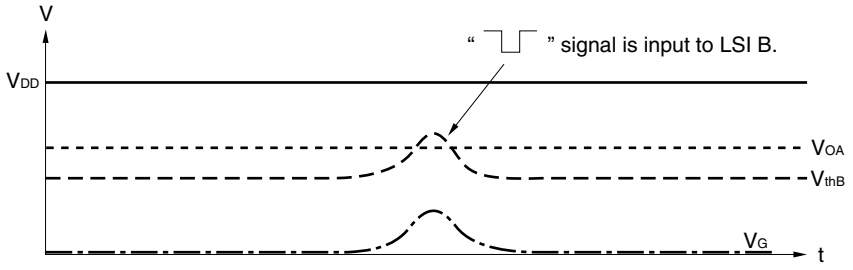
Figure 5-25. Malfunction Caused by Simultaneous Operation

(a) Circuit diagram

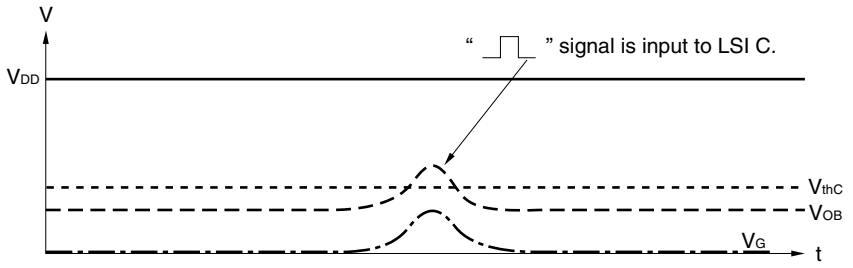


V_{OA}: Output level of LSI A
V_{OB}: Output level of LSI B
V_{thB}: Input threshold level of LSI B
V_{thC}: Input threshold level of LSI C
V_G: GND level of LSI B

(b) Fluctuation in input threshold level of LSI B



(c) Noise generated to the output pin of LSI B



CHAPTER 6 CIRCUIT DESIGN GUIDELINES

This chapter explains the points to be noted and limits to be applied in designing a circuit.

When designing an LSI using the EP-1 series, once a circuit has been designed it cannot be easily modified, unlike when designing a circuit using standard TTL or CMOS ICs.

Therefore, take care to design your LSI without errors by observing the limits and following the design rules described in this design manual.

If an LSI is designed without observing the design rules, not only is the development period after interfacing with NEC Electronics extended, but also the product you develop may need to be reworked.

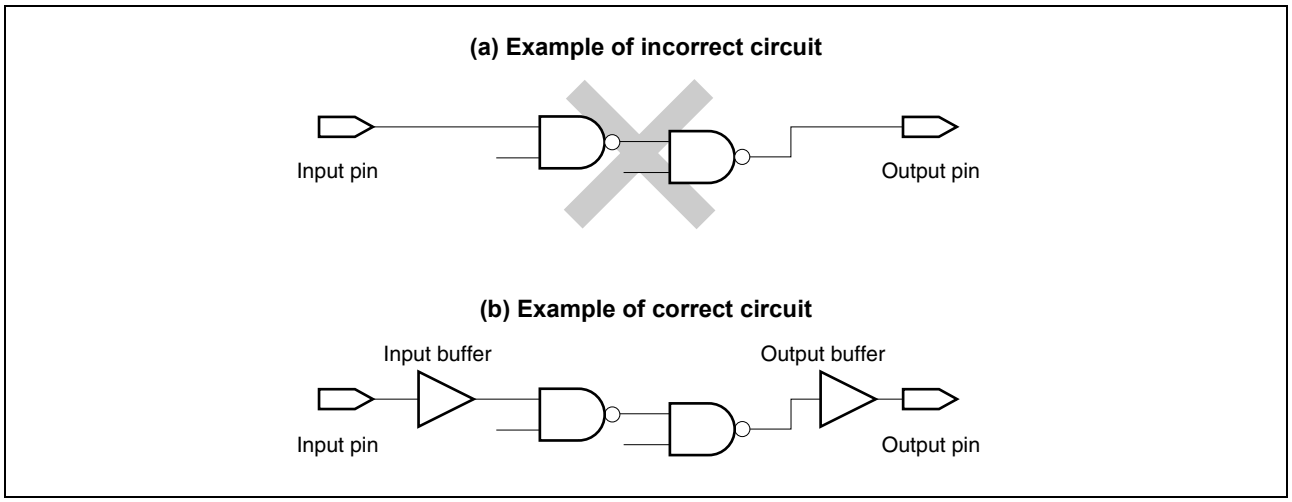
6.1 Basic Circuit Configuration

6.1.1 Using Input/output buffers

When designing an LSI with EP-1 series, place input/output buffers between the LSI and the I/O pins (see Figure 6-1).

Reasons: <1> To protect the LSI from destruction due to static electricity
<2> To obtain sufficient output drive capability

Figure 6-1. Basic Circuit Configuration



6.1.2 Unused pins

With EP-1 series, unused input pins cannot be left open (the state where they are not connected to anything). The pins must be input at either a high or low level by using F091 (H- and L-level generator). If a block's input pins are open, it cannot function correctly since the input level is undetermined. This condition also becomes a source of leakage current (I_{IL}). In addition, large fan-outs should be avoided when F091 is used. If several blocks are clamped to a single block, the wiring becomes concentrated, making placement and routing difficult. Avoid wiring concentrations for the sake of circuit simplification. A warning error will be posted by the tester during a design rule check if the block's output pins are open. Discard unnecessary blocks.

6.1.3 Fan-out limitations

There are limitations on the fan-out capacitance that can be connected to a block's output pins (the fan-out number). The allowable load capacitance for each block is given in **CMOS-9HD Series, EA-9HD Series Block Library (A13052E**).

Because signal rise and fall times increase (accompanied by a deterioration of accuracy) when the load capacitance to be driven increases, propagation delay time has to be reevaluated. Moreover, if rise and fall times become very long, data-through develops in the flip-flops causing abnormal logic operation.

Therefore, do not exceed the fan-out capacitance limit when designing.

Finally, design with a load capacitance that is 1/3 of the limit in circuits that have strict speed specifications.

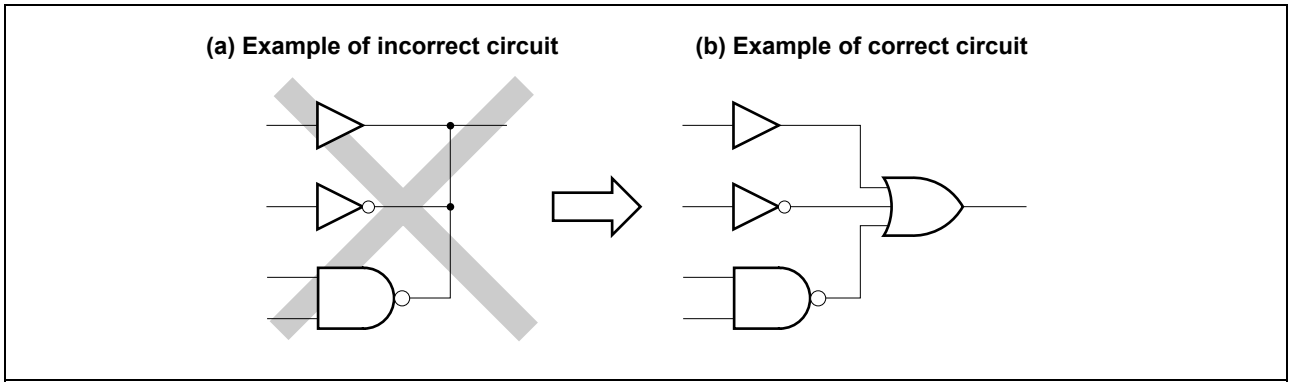
Caution Note that not only the fan-in capacitance of the block connected in the subsequent stage, but also the wiring capacitance is included in the load capacitance.

6.1.4 Wired logic prohibitions

Other than the case for the bus, do not configure wired logic as mutually connected block outputs.

The P-channel transistors and the N-channel transistors become conductive at the same time as a function of the logic state regardless of the outputs that are connected. Pay attention to this since the steady low-power characteristics can be lost for feature CMOS circuits when the output is at an intermediate level because current can flow from V_{DD} to ground.

Figure 6-2. Wired Logic Prohibitions



6.1.5 Notes on using bidirectional buffer

If an output signal is input as is to the internal circuit with a bidirectional buffer, the internal circuit that receives this input signal may malfunction due to distortion of the output waveform and ringing as shown in Figure 6-3. In the output mode, make sure that the signal immediately before the output buffer is input to the internal circuit as shown in Figure 6-4. In particular, do not employ the design method in which the input signal is input to the flip-flop clock.

Figure 6-3. Ringing

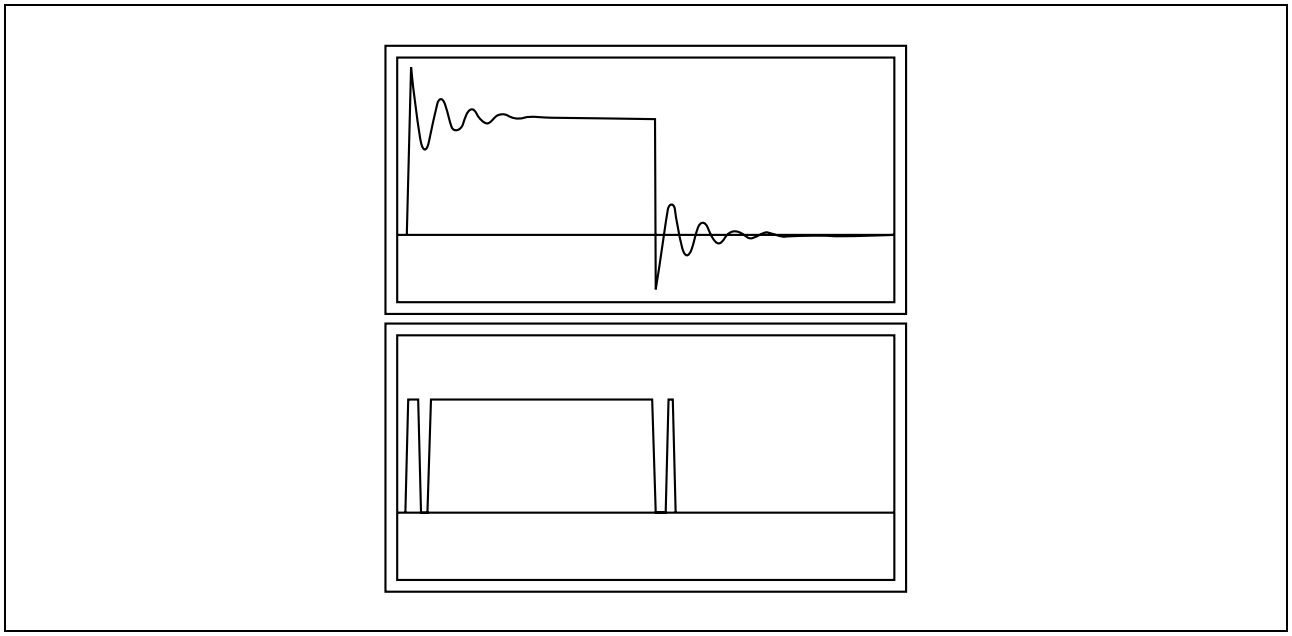
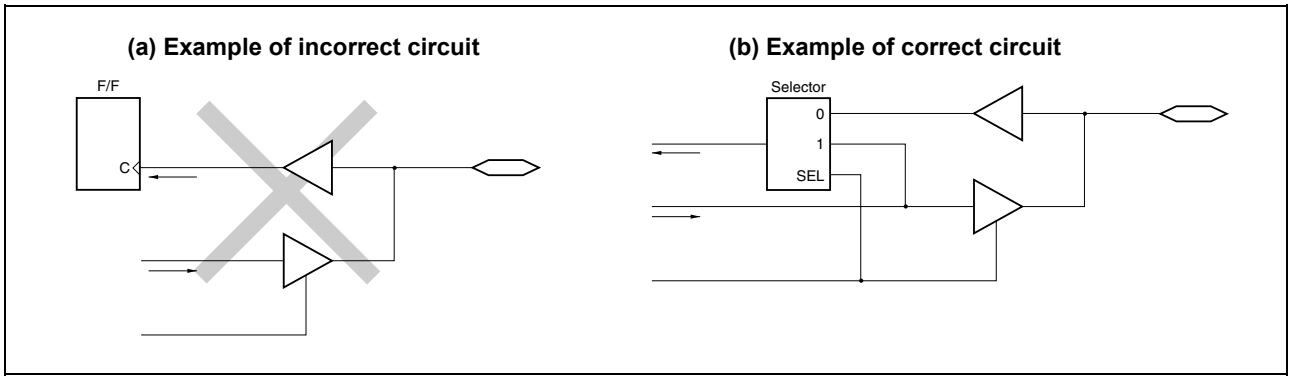


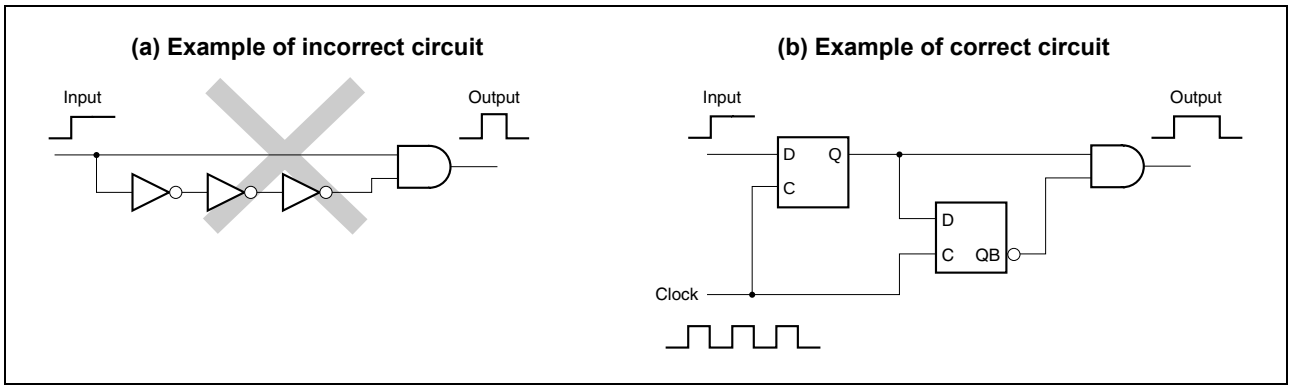
Figure 6-4. Example of Preventive Circuit



6.2 Differential Circuits Prohibitions

As a rule, differential circuits should not be configured from EP-1 series. Since embedded-array placement and routing design is done automatically, the range of waveforms that are internally generated cannot be guaranteed with embedded arrays, and the desired functions will not materialize. Therefore, avoid structuring the circuit shown in Figure 6-5 (a), and structure the circuit as shown in Figure 6-5 (b).

Figure 6-5. Differential Circuit Prohibitions

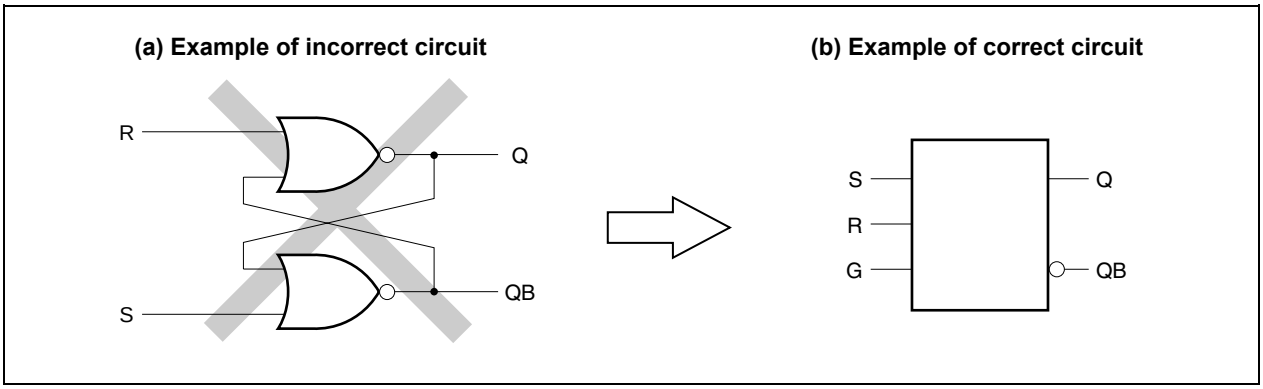


6.3 RS Latch and Loop Circuits

6.3.1 RS latch

Gate-configured asynchronous RS latches should not be used with embedded arrays. This is due to cases when initialization cannot take place via simulation or high variation in circuit path speed due to routing location effects.

Figure 6-6. Asynchronous RS Latches

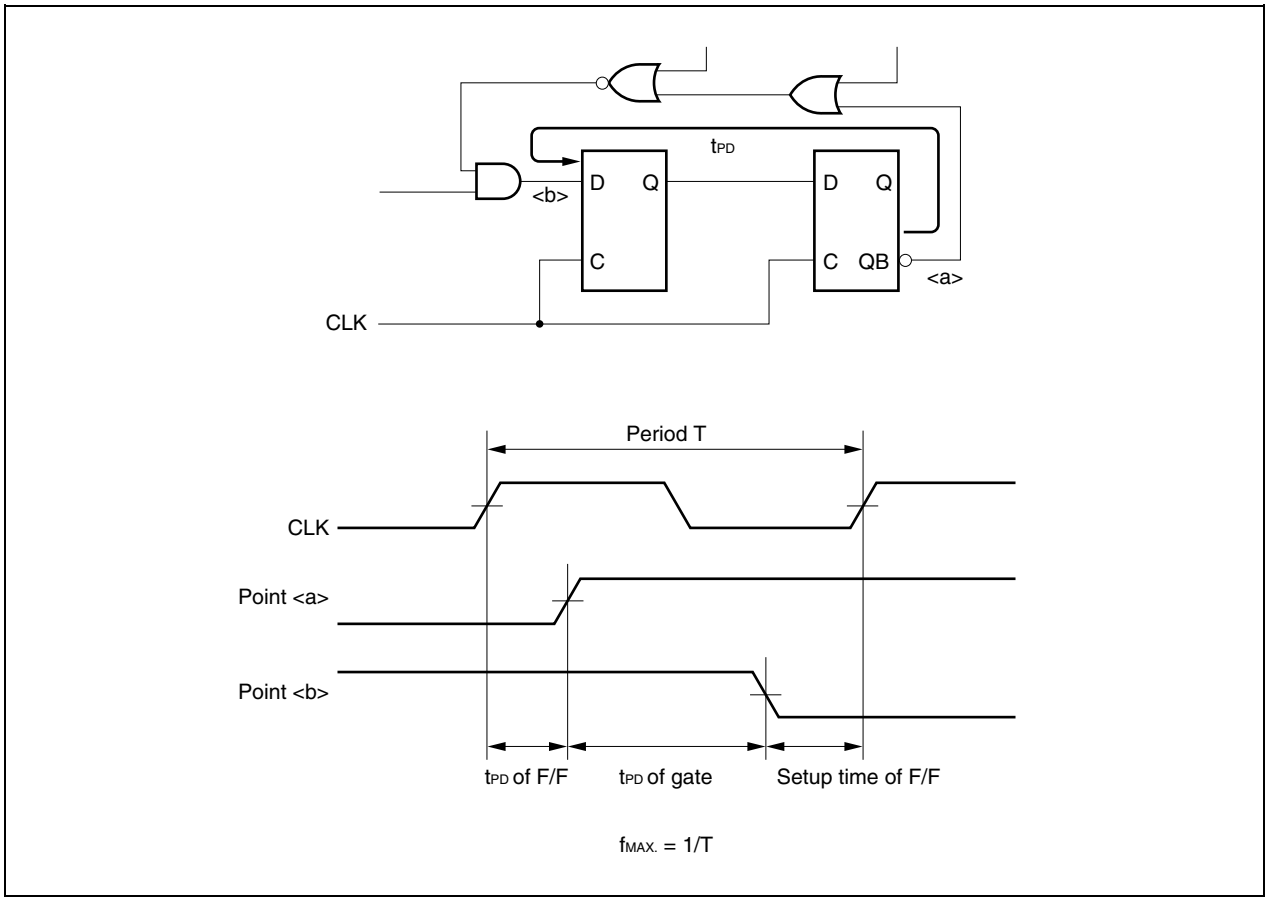


6.3.2 Loop circuit

The following points must be noted when loop circuits, such as feedback loops, are used.

(1) As shown in Figure 6-7, if gates lie between feedback loops in divider circuits, the frequency characteristics will drop due to the delay time caused by these gates. The delay times of these loops must be determined beforehand and the frequency characteristics must be verified (see **6.6 Delay Time Margin for the verification method**).

Figure 6-7. Loop Circuit



(2) A loop circuit cannot be formed when the scan path is formed.
In this case, isolate the loop circuit by using gates as a countermeasure.

6.3.3 Prohibited state (use prohibited) of flip-flops

The state in which both the set and reset inputs of an RS latch or flip-flop are enabled at the same time is prohibited (Use prohibited). This is because the retained data becomes unstable if both the set and reset inputs are disabled simultaneously. What value the retained data will take is influenced by delicate timing such as the timing of the set and reset signal input and delay of the internal signal of the flip-flop and cannot be guaranteed.

Consequently, be aware of the following when using flip-flops with set/reset inputs.

<1> Do not enable set and reset inputs at the same time.

<2> When it is necessary to enable set and reset inputs simultaneously, disable one side first and then disable the other side. By doing this, the state that the flip-flop was in when it was disabled will be maintained.

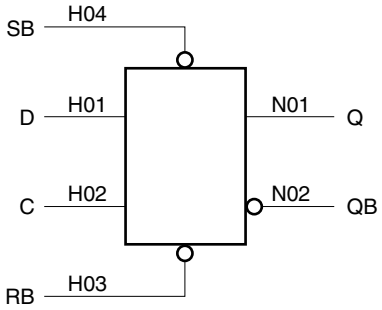


Table 6-1. F617(D-F/F with SB, RB)

D	C	RB	SB	Q	QB	
0	↑	1	1	0	1	
1	↑	1	1	1	0	
X	↓	1	1	Hold	Hold	
X	X	0	1	0	1	
X	X	1	0	1	0	
X	X	0	0	0	0	← Use prohibited

X : Irrelevant

6.4 Clock Line Design

6.4.1 Asynchronous circuits and synchronous circuits

Circuit design methods can be divided into 3 types, single-phase synchronous circuit design, which is ordinarily used for designing circuits used in general-purpose LSI, Multi-phase synchronous circuit design and asynchronous circuit design, which are used often in designing CPU and similar devices. The features of each of these circuit design methods are shown below.

Table 6-2. Features of Circuit Design

	Advantages	Disadvantages
Asynchronous circuit design	Circuit scale becomes smaller. Power consumption becomes lower.	Malfunction due to spikes can occur easily. Defects can occur easily due to post delay simulation.
Single-phase synchronous circuit design	The circuit is simple. It is appropriate for high speed circuits.	It is necessary to consider clock signal wiring skew.
Multi-phase synchronous circuit design	It is easy to assure flip-flop hold time. (circuit design which does not depend on technology is possible)	Not appropriate for high speed operations.

Of these methods, malfunctions due to wiring skew occur easily in circuits which use an asynchronous circuit, so this method is not appropriate for design of the EP-1 series. Design with a synchronous circuit with a single-phase clock which uses multi-phase clock or clock tree synthesis.

(1) Asynchronous circuit design

Asynchronous circuit design is a design method in which control uses circuits which combine clock, reset and similar control signals. Since there are fewer control signals compared to data signals, circuits which control the control signals result in a smaller circuit scale than circuits which control data. Thus, the circuit is easier to see and circuits which have smaller power consumption can be realized.

However, when control is carried out in circuits which combine control signals, (basically, a decoder or selector), the possibility of spike noise being generated in control signals becomes extremely high and these circuits are easily influenced by wiring delay.

Therefore, in a process which are susceptible to the influences of wiring delay such as the EP-1 series, there are phenomena where simulation results differ between before placement and routing and after placement and routing, and this becomes a cause of defects. In the design of EP-1 series, as a rule, please do not create asynchronous circuits.

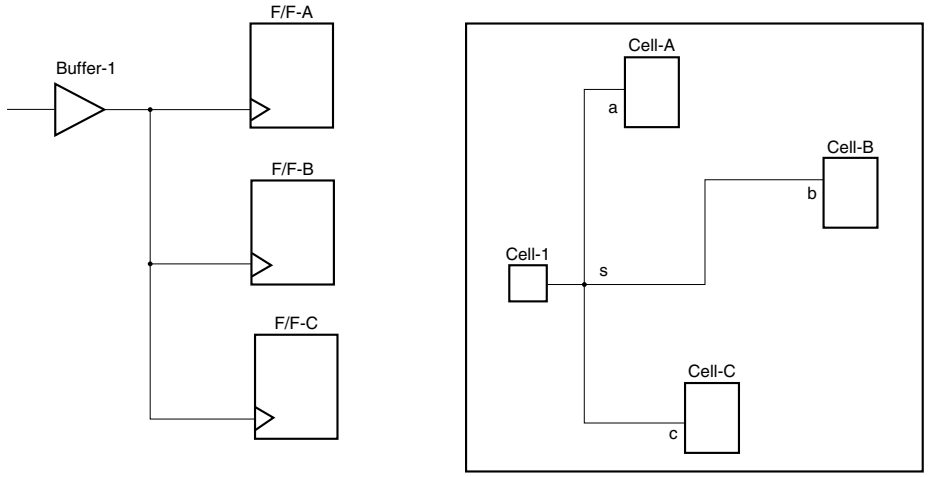
However, in the case of circuits which are sure to operate regardless of the wiring length delay, creation of such circuits does not matter.

Also, when it comes to circuit specifications, if the circuit is an asynchronous circuit, operation can be guaranteed by specifying the critical path. However, only 6 critical paths can be set, so exercise caution.

(2) Single-phase synchronous circuit design

Single-phase synchronous circuit design is a method where sequential circuits are made to run by one type of clock signal. With this design method, the circuit configuration becomes comparatively simple, but it is necessary to adjust the timing due to clock skew between sequential circuits.

Figure 6-8. Clock Skew



The delay timing to a, b and c differs depending on the wiring resistance.

Deviation of the clock signal between sequential circuits is called clock skew (for details, refer to **6.4.2 Clock skew**).

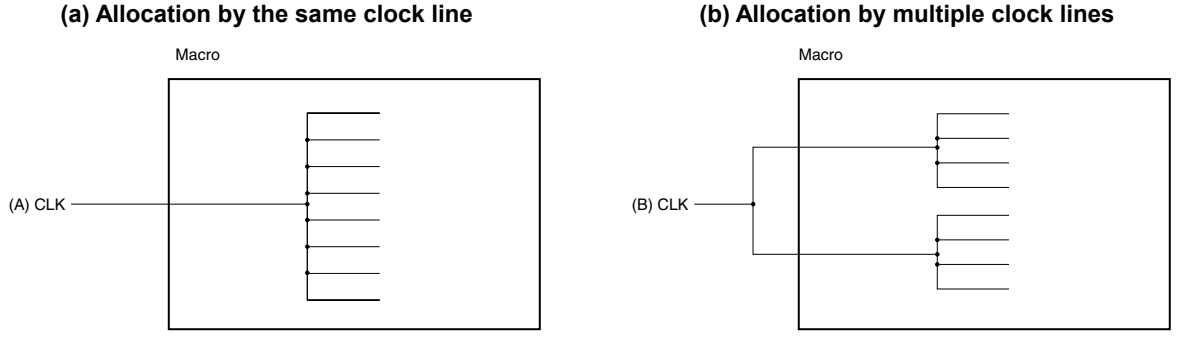
Clock skew increases as the wiring resistance gets higher. Also, it is dependent on wiring lengths from branch points. If single-phase circuit design is carried out, please consider the clock skew and take countermeasures by the following methods.

(A) Within the same macro, as much as possible, distribute with the same clock line (refer to **Figure 6-9 Clock Distribution**).

(B) If distributing in multiple clock lines, do it so that malfunctions do not occur due to clock skew between the clock lines.

(C) Use clock tree synthesis (refer to **6.4.4 Clock tree synthesis**).

Figure 6-9. Clock Distribution



(3) Synchronous circuit design using a multi-phase clock

If processing speed is not a problem, a synchronous circuit configuration using a multi-phase clock is recommended. However, in realizing a single function, design in a multi-phase synchronous circuit has many difficult points when compared with the design in an asynchronous circuit, so designs with synchronous circuits is not so common.

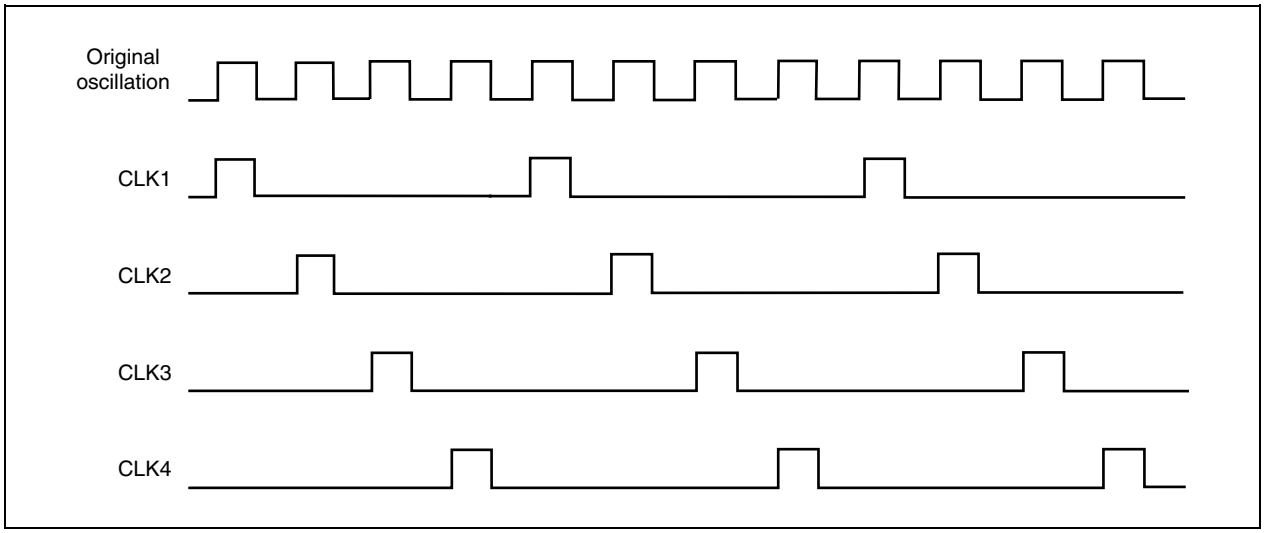
Here, an ordinary method used widely by LSI makers in designing synchronous circuits which use multi-phase clocks is introduced.

A multi-phase clock is as shown in **Figure 6-10 Example of Multi-Phase Clock** (example of a 4-phase clock).

A multi-phase clock is the most commonly used method for designing general purpose LSI (such as CPU).

For example, if there are 3 clocks for 1 state in a CPU, then that CPU uses a 3-phase clock.

Figure 6-10. Example of Multi-Phase Clock



Furthermore, if a multi-phase clock is used, the following points are effective.

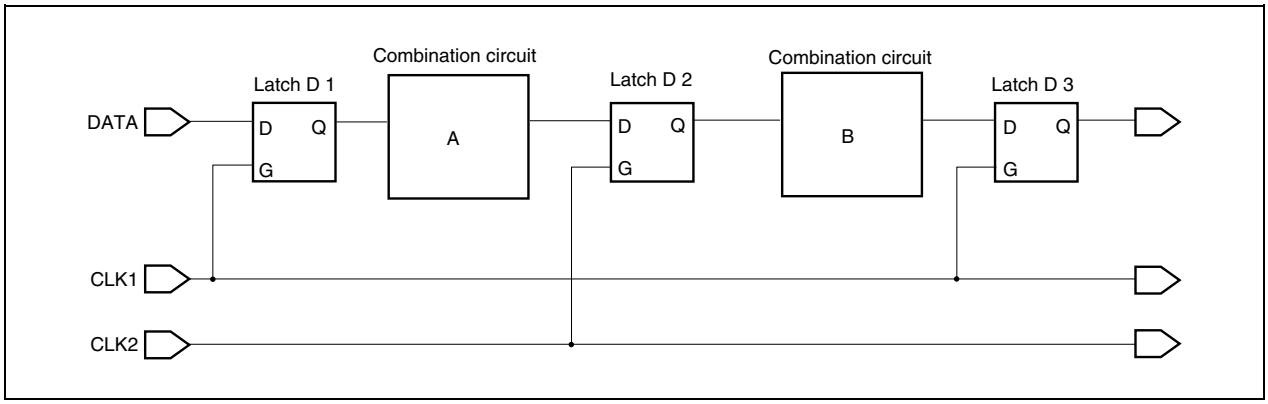
(a) It is easy to assure the setup time and hold time of a latch or F/F.

By using CLK1 and CLK2 alternately as shown below, assuring the latch's setup time and hold time becomes easy.

For example, in the case of the circuit in Figure 6-11, it is as follows.

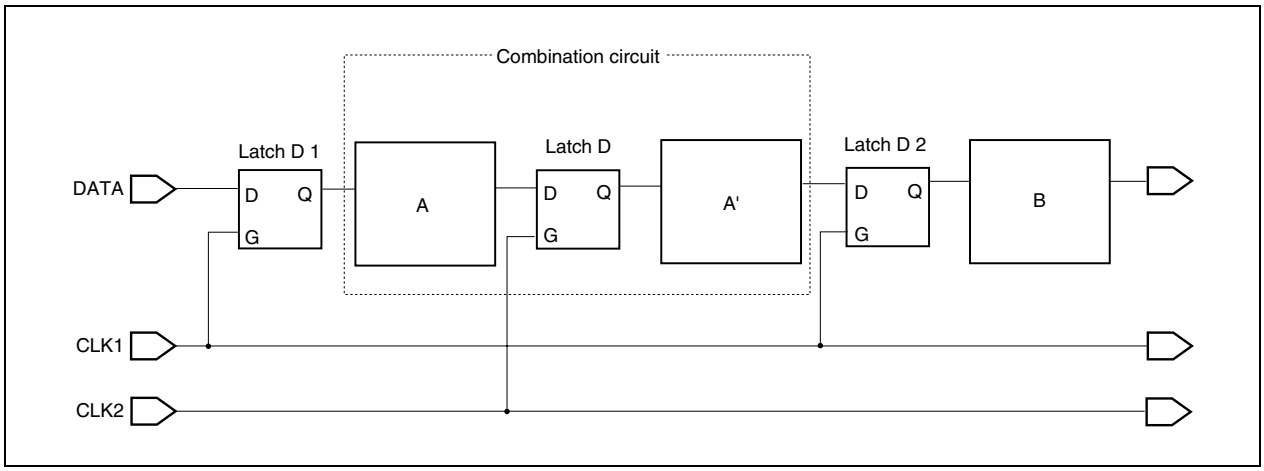
(Latch 2 Setup Time) = (Original oscillation frequency period) – (Delay timing of combination circuit A)

Figure 6-11. Assuring Latch Setup Time and Hold Time



If the delay time of combination circuit A is long and the latch 2 setup timing cannot be assured, combination circuit A is divided by 2 as in Figure 6-12 and one more latch is inserted in the interval to assure the setup time of latch 2. It is the same for the hold time.

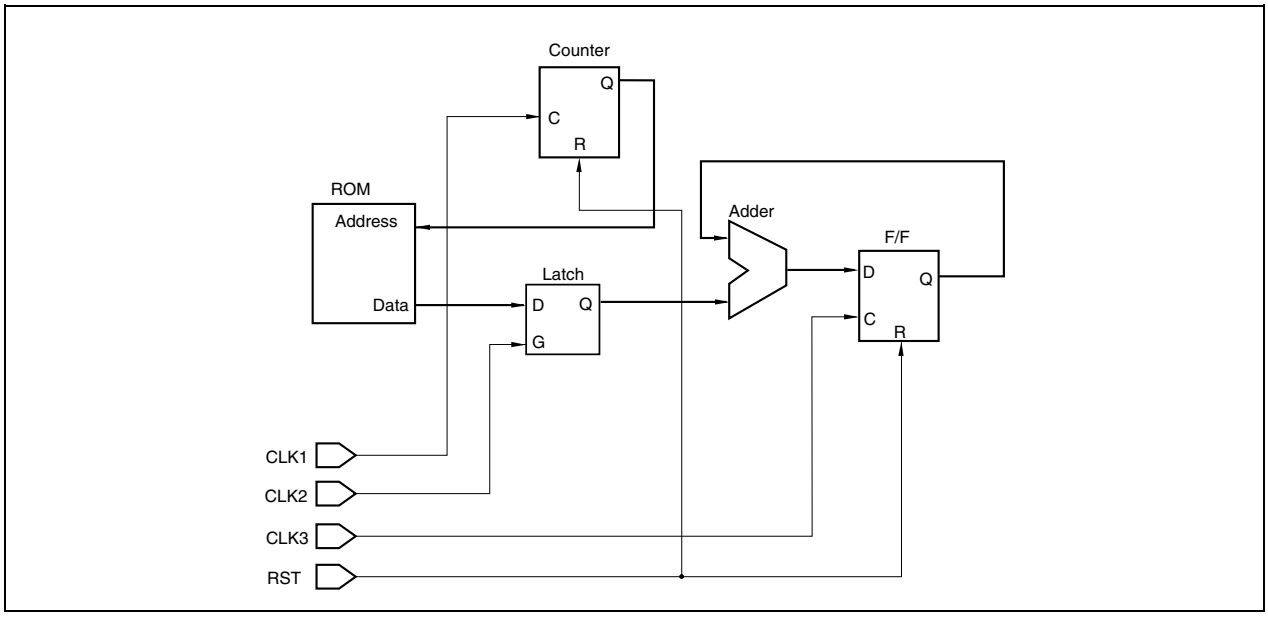
Figure 6-12. Division of Combination Circuit



(b) If you are creating a complex synchronous circuit, the circuit can be simplified by distributing tasks among the different clocks.

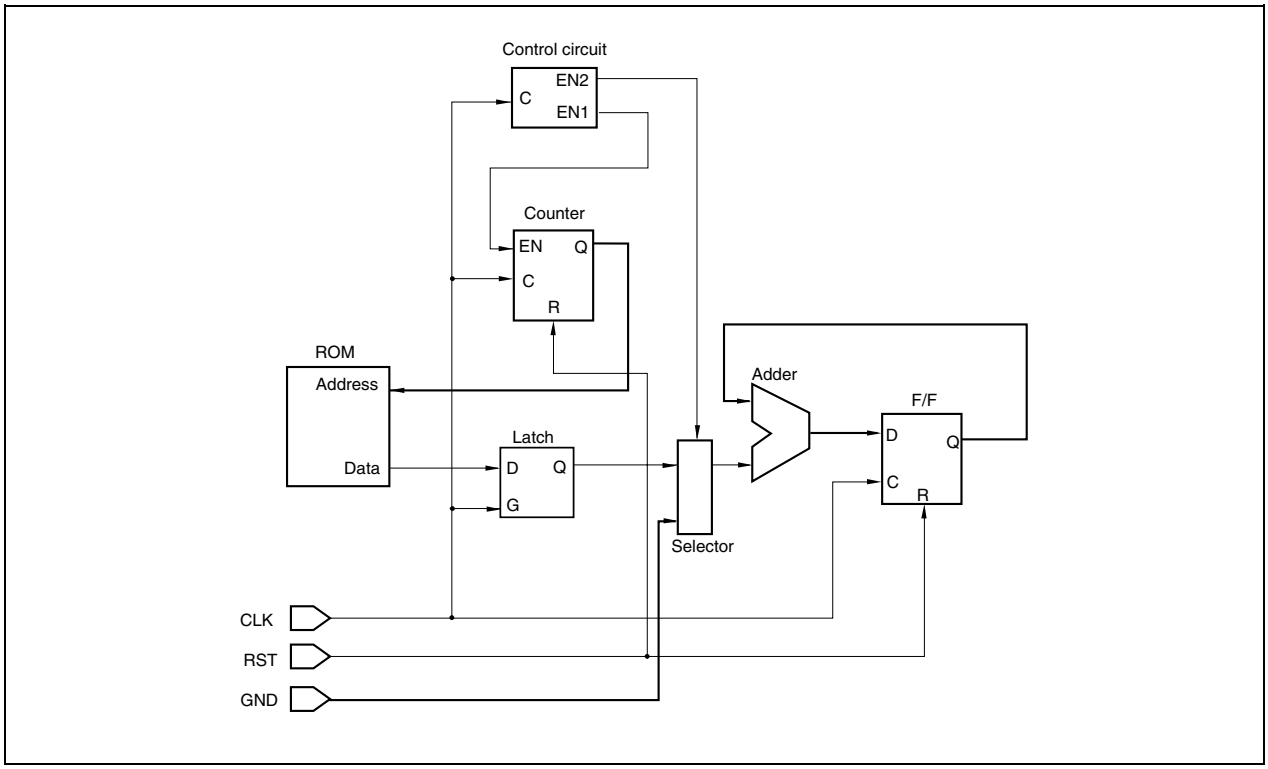
As a result, the number of gates becomes fewer than in the case where a single-phase clock is used. For example, let's make a circuit which inputs data from ROM serially and adds them each time t data which are accumulating. If this is designed with synchronous circuits using a 3-phase clock, it is simplified as shown in Figure 6-13.

Figure 6-13. Add Circuit (Using 3-Phase Clock)



If this is designed using a single-phase clock, the circuit becomes more complex as compared to the use of a 3-phase clock, as shown in **Figure 6-14 Add Circuit (Using Single-Phase Clock)**, and thus the number of gates tends to increase.

Figure 6-14. Add Circuit (Using Single-Phase Clock)

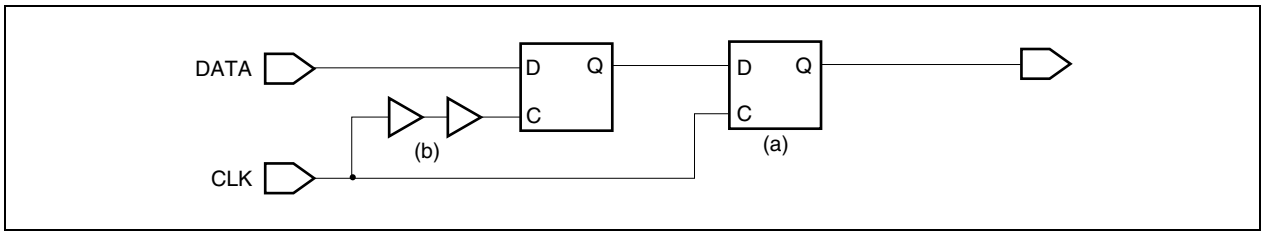


(c) Design that is not dependent on the process is possible.

If a circuit is designed using a multi-phase clock, the only influence that the process has is basically the maximum clock frequency only, and since F/F hold time is assured without using a delay gate, etc., design can be accomplished without awareness of the process.

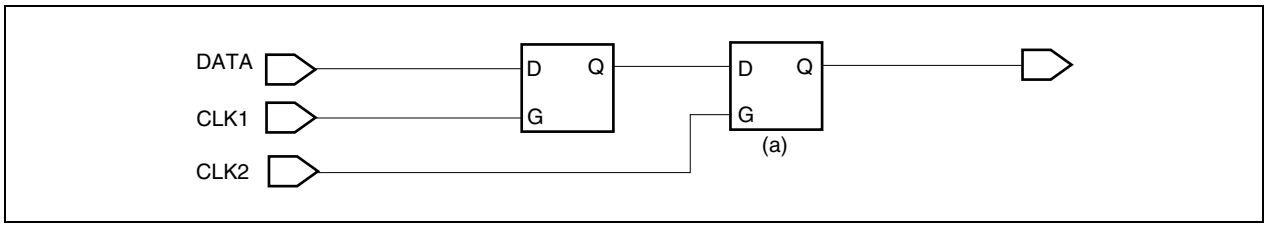
In the case of a circuit like that in Figure 6-15, which is frequently seen in 74LS circuit diagrams designed with a single-phase clock, the F/F (a) hold time is assured with a delay gate (b). In this case, if the process changes, the delay value of delay gate (b) changes, so there is a possibility that it will be impossible to assure the F/F hold time.

Figure 6-15. Frequently Seen Circuit in 74LS Circuit Diagram



In the case of the circuit in Figure 6-16 where a multi-phase clock is used, the F/F (a) hold time is assured by “(CLK2 clock rise) – (CLK1 clock rise)”, so it is not dependent on the process.

Figure 6-16. Circuit When 2-Phase Clock Is Used



Caution The more the clock phases increase, the easier the circuit design becomes, although the processing speed slows down. Therefore, realize the desired function with as few phases as possible.

6.4.2 Clock skew

Clock skew is generated by wiring length variations as a function of macro placement. Hold timing errors in sequential circuits can result from clock skew. Usually, however, it is impossible to take any errors due to these variations into consideration in the simulation before placement and routing. Therefore, the following guidelines are provided to minimize this problem.

(1) Clock line design in a macro

One clock line should be supplied in single-phase synchronous circuit design.

It is basically not necessary to test for clock skew in multiphase synchronous circuit design.

However, it is necessary to check operating frequency.

(2) Clock line design between macros

There are special clock skew problems between macros associated with synchronous design. Examples of a countermeasure are shown in Figure 6-17.

Figure 6-17. Clock Line Countermeasure

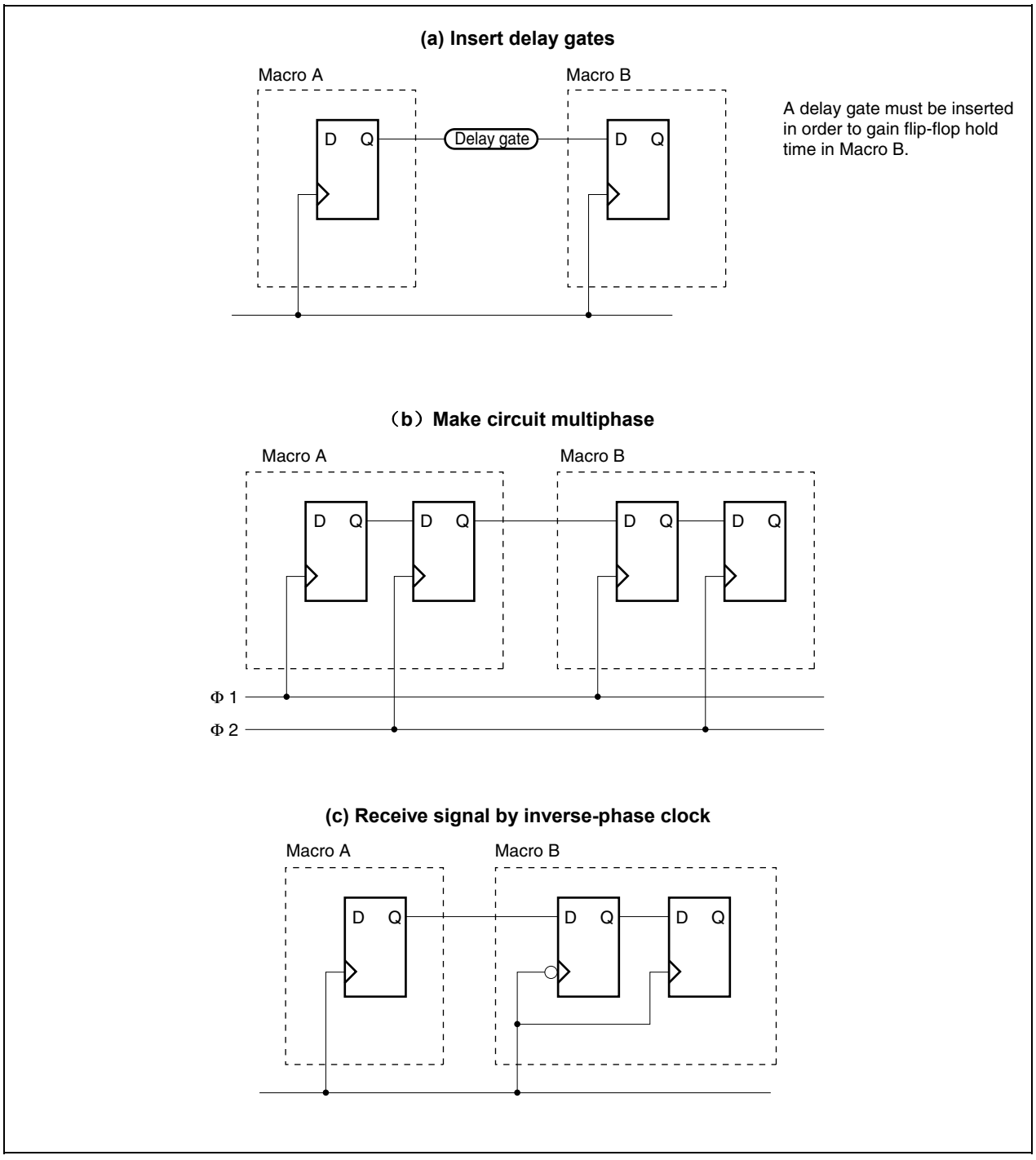


Figure 6-17 (b) is a measure using a multiphase clock. In this case, it is necessary to keep the clock frequency in mind.

Figure 6-17 (c) uses inverse phase so that there is a hold time margin. With this method, it is necessary to keep the clock frequency and duty cycle in mind.

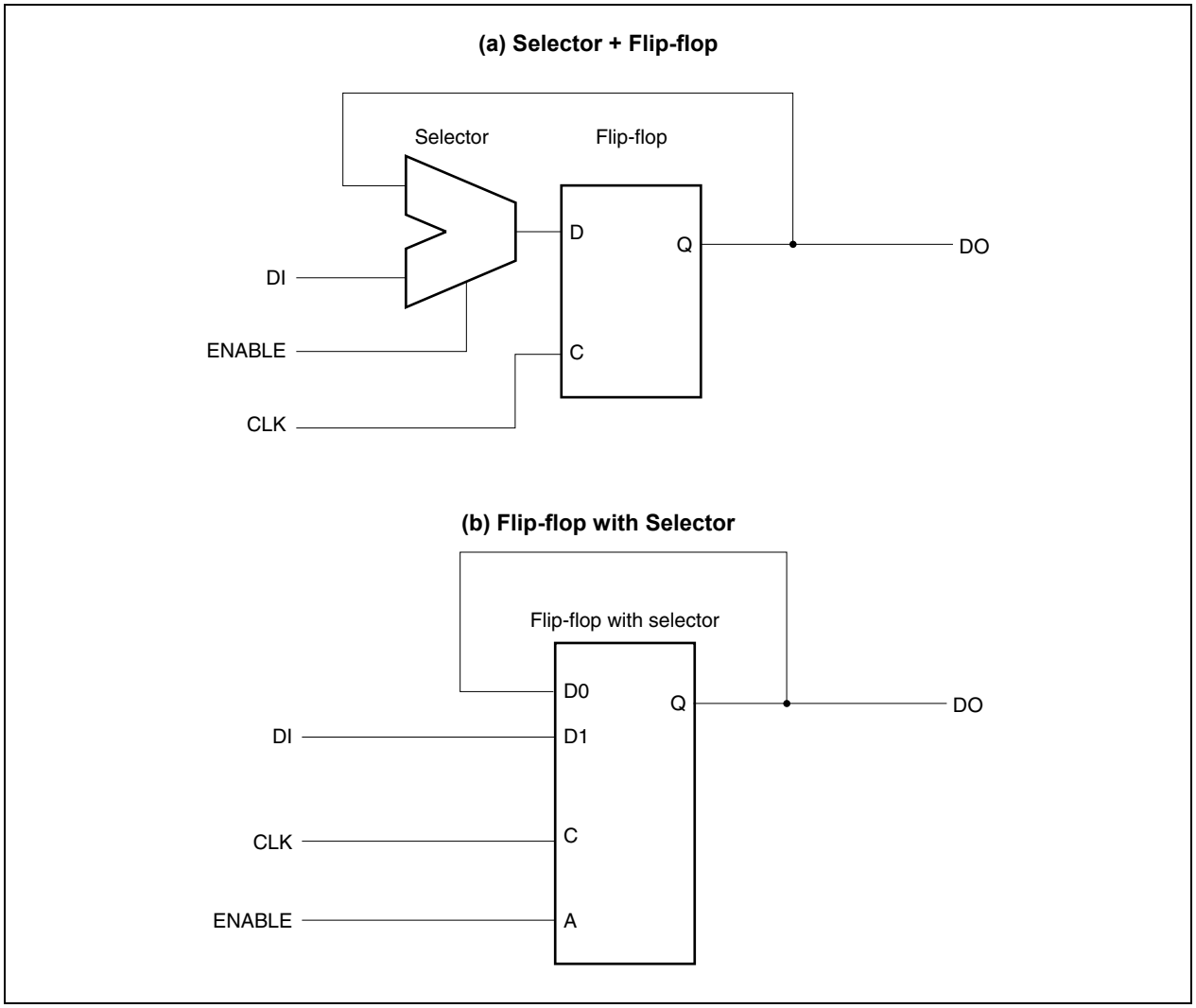
6.4.3 Enable control

If it is necessary to stop a system operation, create an enable signal and design the circuit so that system internal flip-flops do not operate. There are two types of enable signal, data enable and clock enable.

(1) Data enable

Design is carried out so that feedback of output signals prevents the signals from changing. To change the enable signal, use the reverse edge of the flip-flop. This is the most common method and is appropriate for synchronize design.

Figure 6-18. Data Enable Flip-Flop



(2) Clock enable

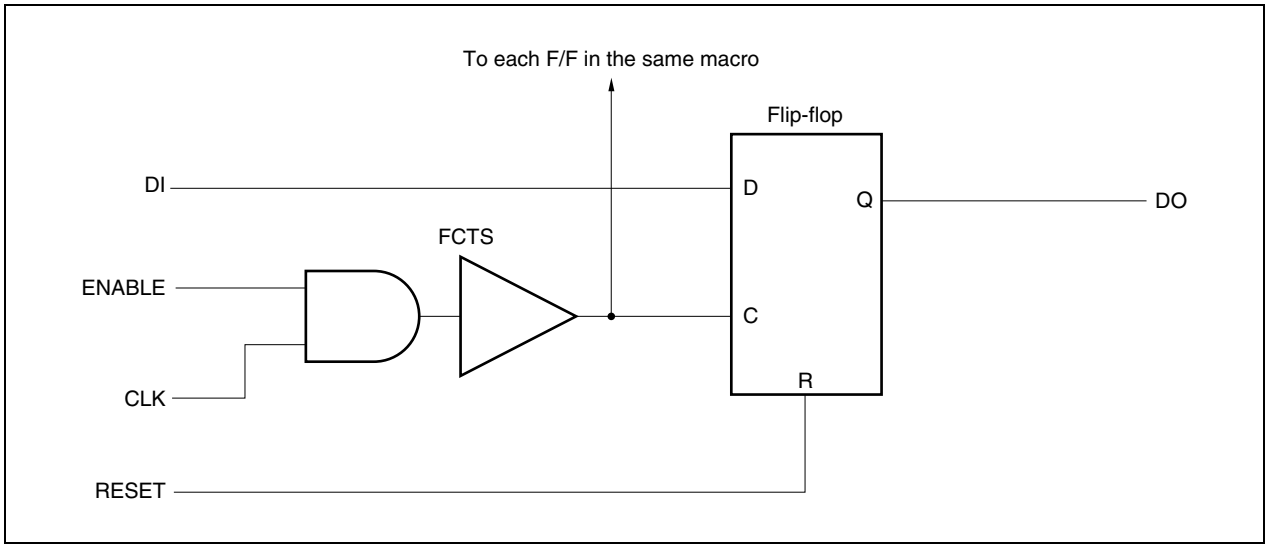
In data enable, even after the flip-flop has stopped, the clock signal continues to be supplied to the flip-flop. For that reason, in systems with a sleep mode (in which clock signal supply is stopped to the circuits to reduce power consumption), there are cases where power consumption becomes a problem. Clock enable is one method of treatment in such a case.

Concretely, by inserting a logic gate such as an AND in the clock input as in Figure 6-19, supply of the clock signal to the flip-flop is prevented.

However, with this method, the spike noise generated at the inserted logic gate is input to the clock, so malfunction can occur easily. Malfunctions due to such a cause can be prevented by initializing the flip-flop when recovering from the sleep mode.

Furthermore, in ordinary systems, it is recommended that design be carried out with data enable.

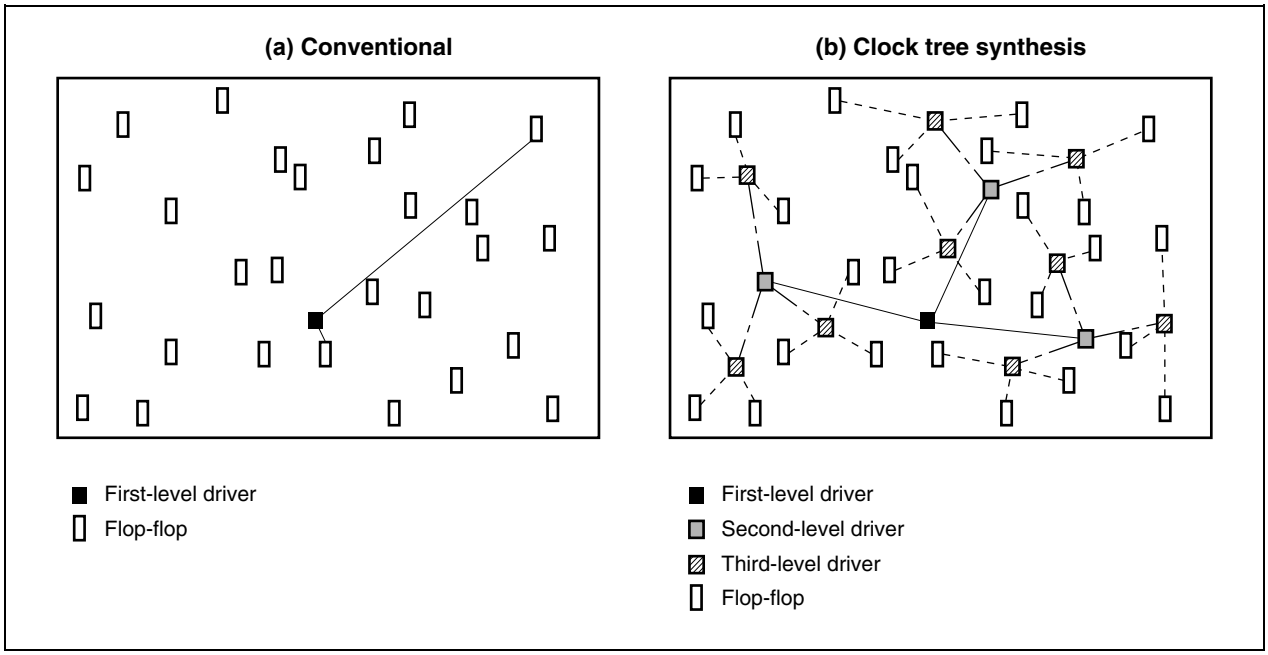
Figure 6-19. Example of Configuration Using Clock Enable



6.4.4 Clock tree synthesis

Clock tree synthesis is a technique that minimizes clock skew between flip-flops that are connected to the clock line. As shown in Figure 6-20 (a), the distance between the clock driver and each flip-flop is not constant. In addition, wiring resistance increases due to shrink processing. Because of this, the variations in wiring length are linked to clock skew. With clock tree synthesis, a buffer is inserted in the clock line. This uniformly distributes the clock line, as shown in Figure 6-20 (b).

Figure 6-20. Concept of Clock Tree Synthesis



(1) How to use clock tree synthesis

In clock tree synthesis, a clock tree synthesis block is substituted for the clock drivers that are usually used. The block names and the number of inserted stages are shown in Table 6-3. The selection of the blocks to be used is based on the number of clock line branches.

Caution The recommended number of CTSs used is one per chip. Two or more CTSs can be used, however, there is a risk of lowering the cell utilization rate and causing clock skew to increase due to the increase in the number of CTSs used. The more CTSs are used the more time is required for clock tree synthesis and routing. Therefore, take this into account when determining the schedule.

Table 6-3. Reference List of Buffer Type CTS Delay, Skew Values (with 1 CTS Incorporated)

Block Name	Layer	Input Block	Number of Clock Line Branches				
			32 to 128 [127]	129 to 1280 [560]	1281 to 2560 [1978]	2561 to 5120 [3854]	Maximum Number of Branches
FC52	2	F154	(0.43 to 1.29) 0.05 ns	▲	×	×	139 to 256
FC53	3	F154	(0.45 to 1.49) 0.15 ns	(0.56 to 1.85) 0.19 ns	(0.91 to 2.92) 0.28 ns	▲	2653 to 5035
FC54	4	F154	(0.54 to 1.76) 0.10 ns	(0.54 to 1.86) 0.23 ns	(0.97 to 3.03) 0.27 ns	(0.98 to 3.11) 0.38 ns	50412 to 95664
FC92	2	F158BR	(0.29 to 0.98) 0.05 ns	▲	×	×	176 to 334
FC93	3	F158BR	(0.37 to 1.21) 0.08 ns	(0.38 to 1.31) 0.12 ns	▲	▲	2111 to 4007
FC94	4	F158BR	(0.44 to 1.46) 0.08 ns	(0.45 to 1.57) 0.13 ns	(0.62 to 2.10) 0.21 ns	(0.71 to 2.37) 0.34 ns	25340 to 48086

Cautions 1. The values in the above list are for reference only, and may change depending on the master and number of cells, and the circuit configuration (presence/absence of macros), etc.

2. It does not necessarily follow that the number of clock branches increases proportionately to FC52 to FC94.

3. The maximum number of clock branches differs depending on the master.

4. The maximum number of clock branches is the value when flip-flops at fan-in 1:0 are used.

Remark This expansion block differs from the conventional inverter type CTS block.
The meanings of the symbols in the table are as follows.
×: Disabled
▲: Can be used depending on the master and circuit configuration.
Values in parentheses ( ) in the table indicate the minimum delay time (left) and maximum delay time (right) of when the number of branches is the number in the brackets [ ], and the number underneath indicates the maximum clock skew time.

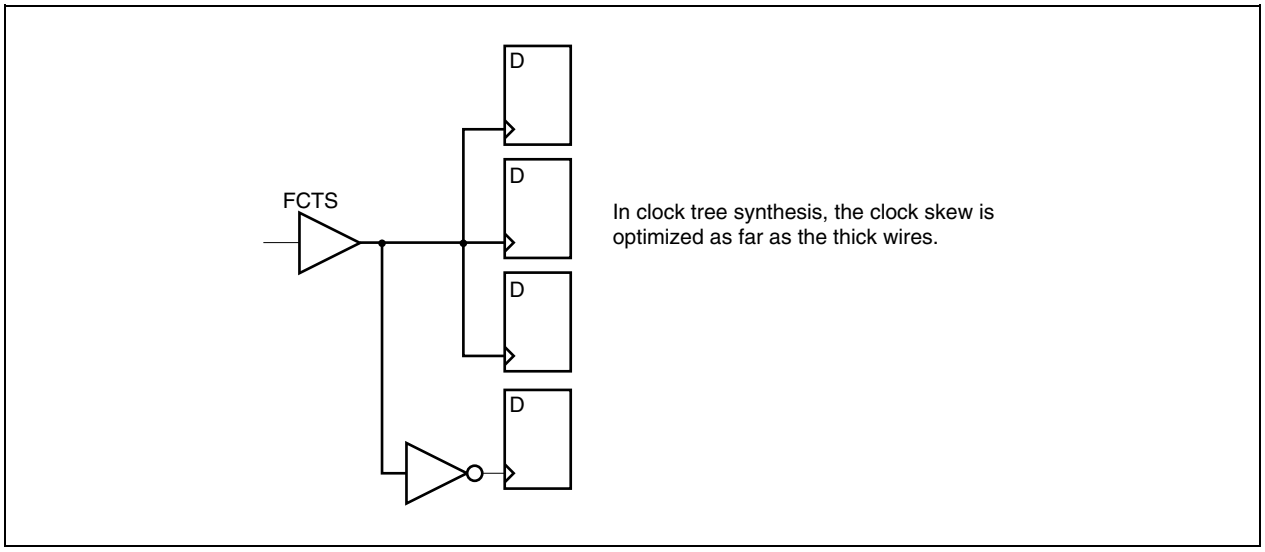
(2) Clock tree synthesis guidelines

The following precautions apply when using clock tree synthesis.

(a) The section from the output of the clock tree synthesis block (FCTS) to the block that requires optimized clock skew must be written by one net.

If a function block is inserted in the path, the clock skew up to the function block is optimized.

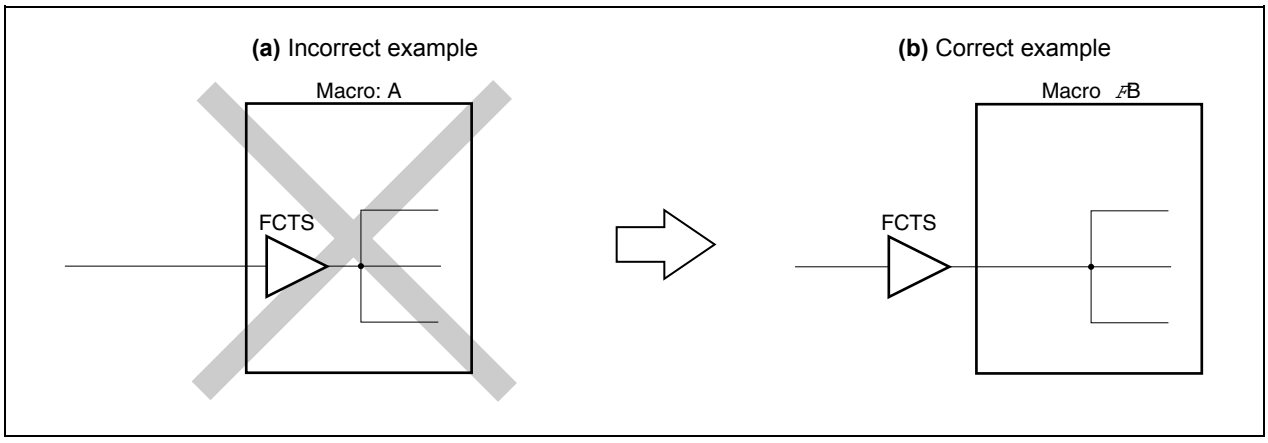
Figure 6-21. Clock Skew Optimization



(b) Write the FCTS to the TOP layer.

The FCTS can be written in the macro if the FCTS does not return to the higher layer.

Figure 6-22. Example of CTS Block Writing



(c) Routing detours increase with large macros and high use rates, and there are cases where clock skew cannot be sufficiently optimized.

(d) Since delay times increase, use a digital PLL (see **9.6 Digital PLL**) when there are timing problems between chips.

6.4.5 Setting and resetting of latches and flip-flops

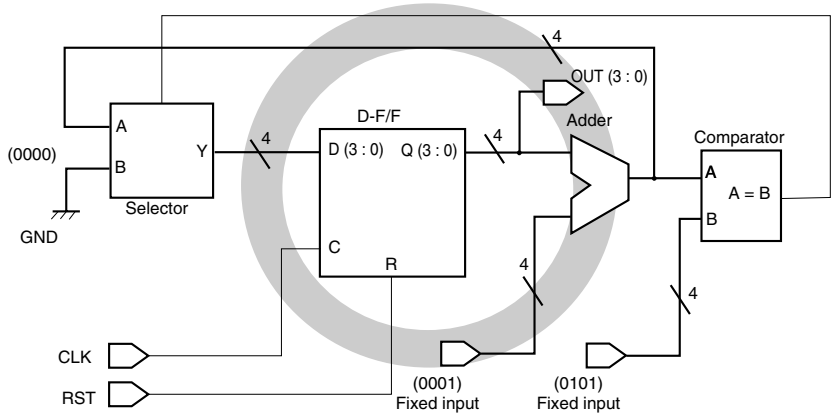
Use setting and resetting of latches and flip-flops only for initializing (except RS latches). If used for other purposes, the following problems occur.

(1) An ATG (test pattern auto generation) such as a scan path cannot be used effectively.
(2) Signal paths become complex, so circuit verification becomes complicated and results in verification delays. In order to reduce verification time and eliminate verification delays in large scale circuit design, it is recommended that the previously described method be used.
(3) It becomes easy to fall back into a circuit configuration that is dependent on the process (such as a delay gate to assure the minimum pulse width in a reset).

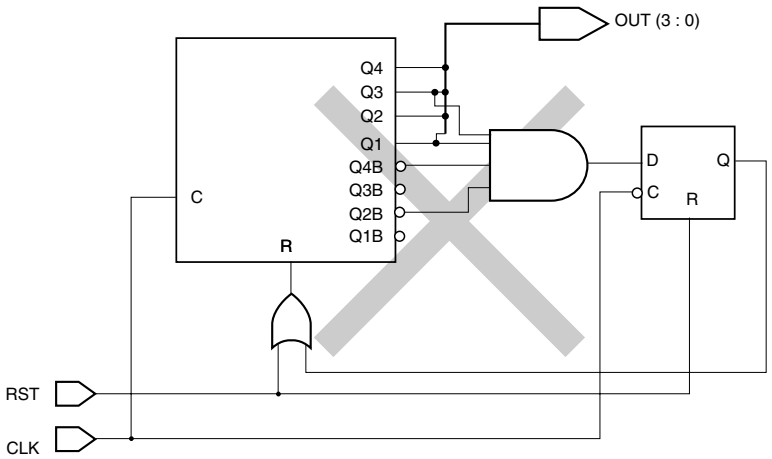
Therefore, avoid circuits such as the frequently seen example of the 74LS circuit in Figure 6-23 (b) and use the more commonly seen circuit configuration in Figure 6-23 (a).

Figure 6-23. Examples of Base 5 Counter

(a) Example of correct circuit



(b) Example of incorrect circuit



6.5 Notes on Configuring High-Speed Circuits

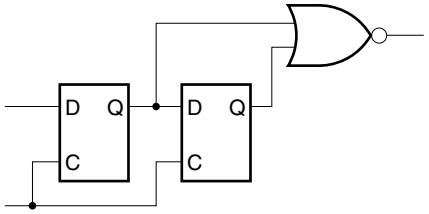
Generally, an N-channel transistor can pass a higher current than a P-channel transistor. Therefore, a NOR gate consisting of P-channel transistors connected in series has a reduced load drive capability at the rising of the output. For example, a NOR block in a CMOS embedded array is slower than a NAND block, and has poor fan-out characteristics.

The guidelines for structuring a circuit that will run at high speed are shown below.

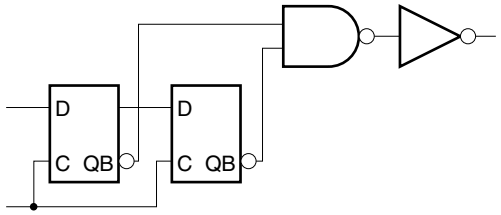
(1) Structure the circuit by using logic conversion techniques and standard NAND blocks.

- The circuit's speed will improve, as will the circuit's stability.

Circuit not well suited to high-speed (stable) operation



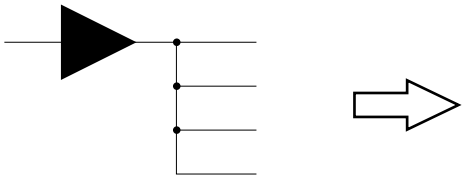
Circuit well suited to high-speed (stable) operation



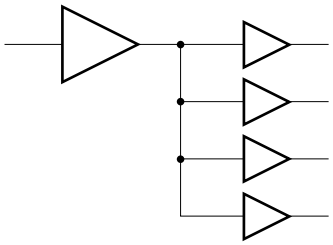
(2) Structure the circuit so that the fan-out is as small as possible to lighten the load.

- As a rule of thumb, stick to 1/3 to 1/2 the fan-out limit.

Circuit not well suited to high-speed (stable) operation



Circuit well suited to high-speed (stable) operation



(3) Convert from low-power blocks to standard blocks.

(4) Use complex blocks.

(5) Closely place macros between which high-speed signals are transferred.

(6) Execute a test run once in advance if possible.

(7) Designing in Modules (Piecemeal)

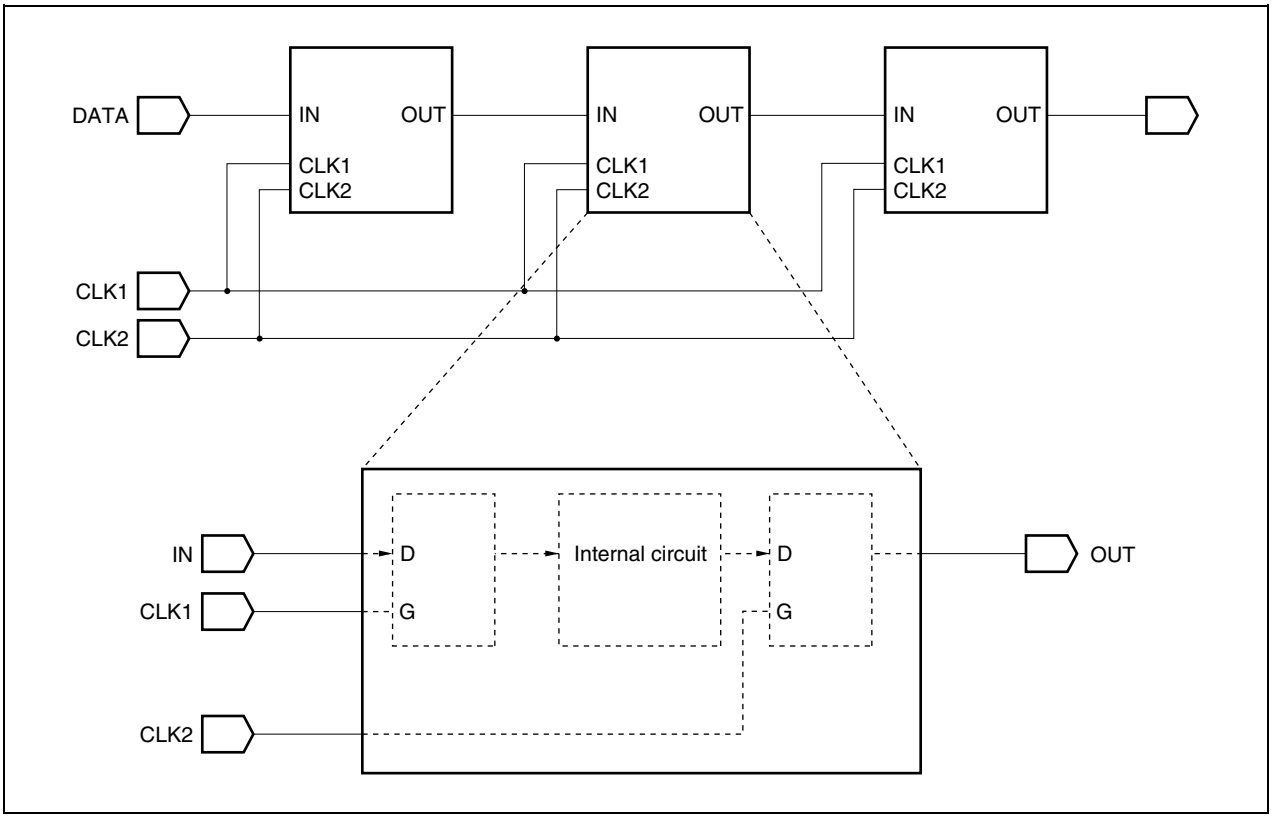
When designing high-speed, large scale circuits, it is generally possible to improve efficiency by dividing the device into several modules and designing in layers.

Standardization of inter-macro interfaces

The largest obstacle to overcome in layer designing is the inability to complete circuit design due to the lack of compatibility between inter-macro interfaces when macros are joined on a single chip.
The solution to this problem lies in the standardization of the inter-macro interfaces.

A simple example of this is shown in Figure 6-24 below. In this example, it has been decided to first latch all the output data of the respective macros with CLK2 before being output, and latch all the input data with CLK1 before being received. As a result, it has been possible to avoid contention when receiving inter-macro data, and at the same time standardize the interfaces related to this process.

Figure 6-24. Standardization of Inter-Macro Interfaces



6.6 Delay Time Margin

The logic circuits consist of combination circuits whose output is determined uniquely by the state at their inputs and sequential circuits whose output is determined by the state at their inputs and their previous state. Specifically, sequential circuits consist of gate circuits that have feedback, flip-flops, and latches.

Taking into consideration the testability and delay times, it is clear that individual combination and sequential circuits can not be too large. Also, a majority of the sequential circuits are operated in synchronization with the system clock which has an adequate margin with respect to the delay times of the combination circuits.

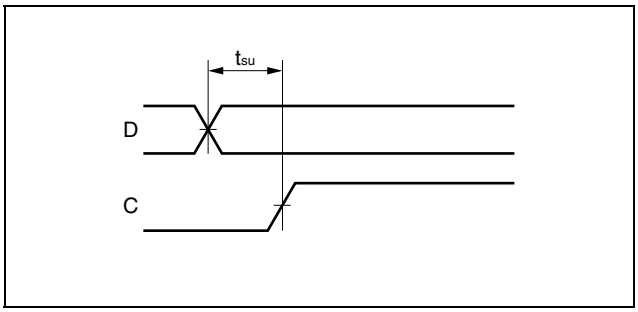
At the portion where adequate margin cannot be secured by the clock, timing of the entry of the sequential circuit, ie., each input of flip-flops and latches, must be secured.

6.6.1 Timing definitions

(1) Setup time (t_{su})

In latches or flip-flops, the data setup time needed to read in data by the active edge of the clock.

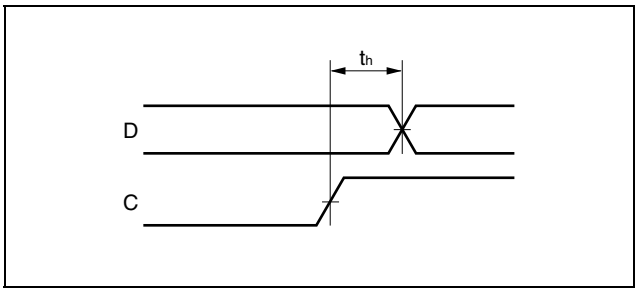
Figure 6-25. Setup Time



(2) Hold time (t_h)

In latches or flip-flops, the data hold time needed to read in data by the active edge of the clock.

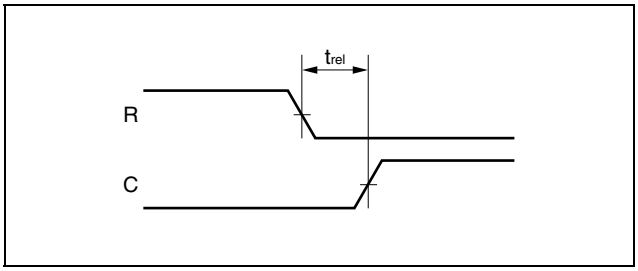
Figure 6-26. Hold Time



(3) Release time (t_{rel})

In latches and flip-flops, release time is the time needed from release of the reset (or set) until the active edge of the next clock becomes valid.

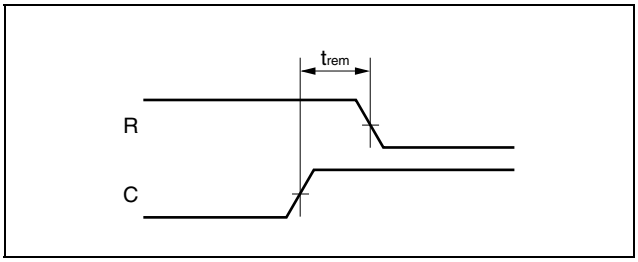
Figure 6-27. Release Time



(4) Removal time (t_{rem})

In latches and flip-flops, removal time is the time needed to make the active edge of the clock invalid when the reset (or set) is cancelled.

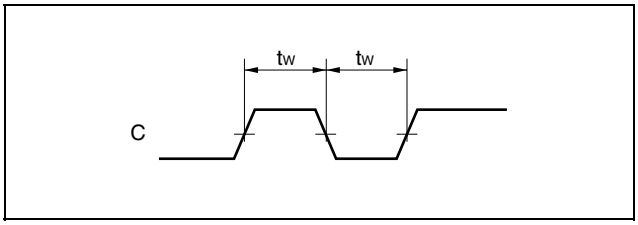
Figure 6-28. Removal Time



(5) Minimum pulse width (t_w)

In latches or flip-flops, minimum pulse width is the minimum time of the clock (or reset and set) pulse width needed in order to read in data correctly

Figure 6-29. Minimum Pulse Width



6.6.2 Delay time margin (asynchronous circuits)

As an example of calculating the delay time margin, we will look at the set up time and the hold time for the circuit in Figure 6-30. Here, the variation and wiring length establish the specifications for decreasing the margin. If the fixed standard values that are determined by each block (t_{su} and t_h) are satisfied, decisions about normal operation can be ascertained.

Figure 6-30. Delay Time Margin Calculation

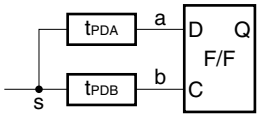
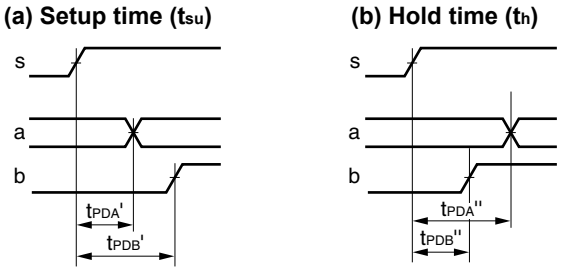


Figure 6-31. Timing Estimate



Calculation equations:

$t_{su} < t_{PDB}' - t_{PDA}'$

$= t_{PDB(MIN)} - t_{PDA[MIN(max)]}$

$= t_{PDB(MIN)} - t_{PDA(MIN)} \times \frac{1+\alpha}{1-\alpha}$

$t_h < t_{PDA}'' - t_{PDB}''$

$= t_{PDA(MIN)} - t_{PDB[MIN(max)]}$

$= t_{PDA(MIN)} - t_{PDB(MIN)} \times \frac{1+\alpha}{1-\alpha}$

α: Distribution coefficient (0.1)

6.6.3 Delay time margin (high-speed circuits)

In circuits operating at high frequencies, the operating margin for an internal functional block's delay time is small since the single-cycle time is short. Here, we show the delay time margin calculation for both in-phase and inverse-phase circuits.

(1) In-phase clock

Consider the shift register operation containing delay A between flip-flops F1 and F2 in Figure 6-32. As shown in Figure 6-33, the points at which this circuit is inspected are where the output data (Q of F1) passes through delay A to F2 (sampling timing <1>) and at sampling timing <2>, where a check is made to see if the data is read normally.

Therefore, the value resulting from adding the maximum delay at point a to the setup time of F2 must be obtained within one time period T.

Figure 6-32. In-Phase Clock Circuit

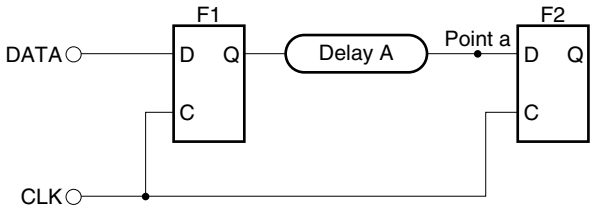
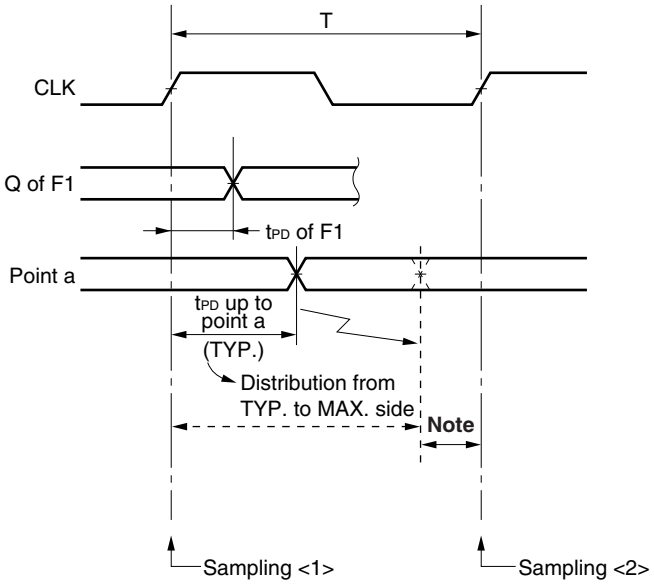


Figure 6-33. In-Phase Clock Timing



Note In consideration of the F2 setup time, do not cross into the next sampling timing.

Calculation equation:

$T - (t_{PD(F1)(MAX)} + t_{PDA(MAX)}) > t_{SU(F2)}$

The following countermeasures are necessary if this relationship is not satisfied:

- Reduce the amount of delay of delay A
- Lower the operating frequency (lengthen period T)

(2) Inverse-phase clock

Figure 6-34 is an inverse modification of the F2 clock's active edge shown in Figure 6-32. Since both the rise and fall edges are used, the operating margin varies as a function of the clock's duty cycle. The circuit normally operates under the following conditions.

Figure 6-34. Inverse-Phase Clock Circuit

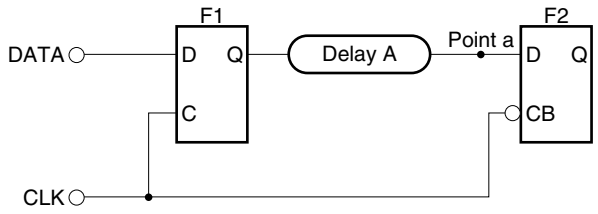
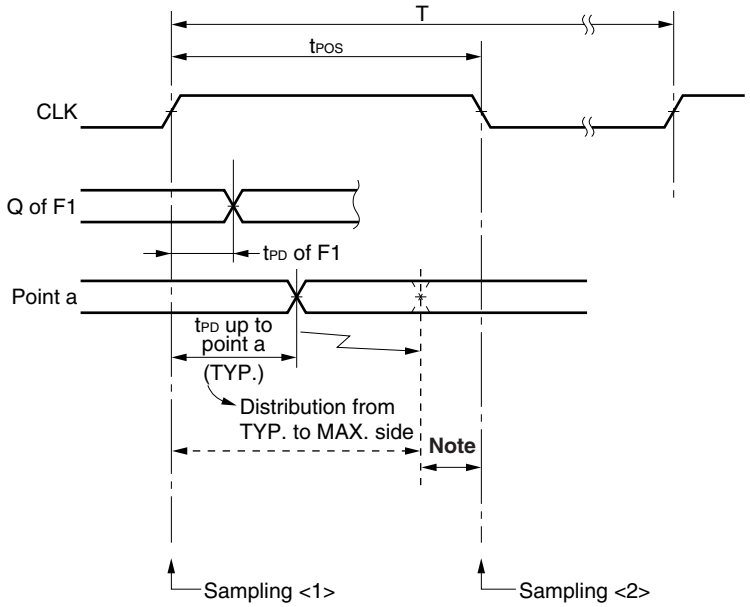


Figure 6-35. Inverse-Phase Clock Timing



Note In consideration of the F2 setup time, do not cross into the next sampling timing.

Calculation equation:

$t_{POS} - (t_{PD(F1)(MAX)} + t_{PDA(MAX)}) > t_{SU(F2)}$

The following countermeasures are necessary if this relationship is not satisfied:

- Reduce the amount of delay of delay A
- Lower the operating frequency (lengthen period T)
- Increase the CLK duty

6.6.4 Minimum pulse width

With circuits operating at high speed, there are cases when the minimum pulse width for a flip-flop input block is not satisfied due to the delay difference between the rise of the signal and its fall and the relative variation of identical pulses.

For example, in Figure 6-36, the signal input by the clock passes through delay B and is input to the flip-flop. The timing is shown in Figure 6-37. In regard to delay B, when the fall time delay t_{PDB} (LL) is greater than the rise time delay t_{PDB} (HH), t_{NEG} becomes greater than t_{NEG} (MIN.), and the pulse becomes narrow. t_{NEG} (MIN.) is estimated by specifications established by the relative variation between the maximum t_{PDB} (LL) and t_{PDB} (HH).

Figure 6-36. Minimum Pulse Width

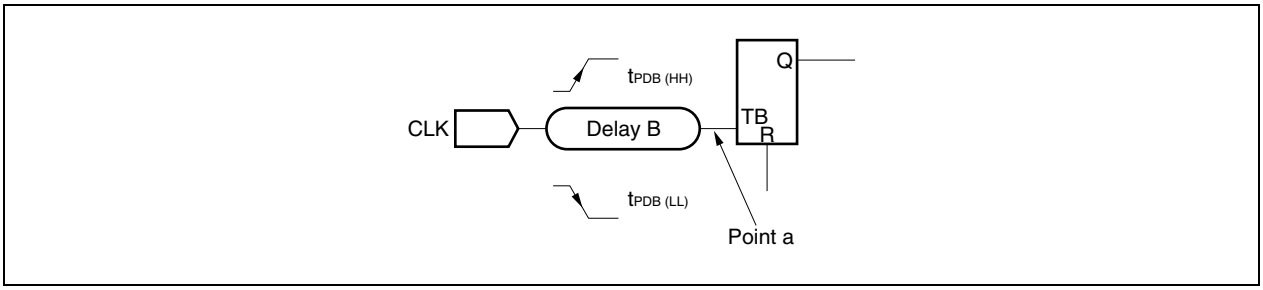
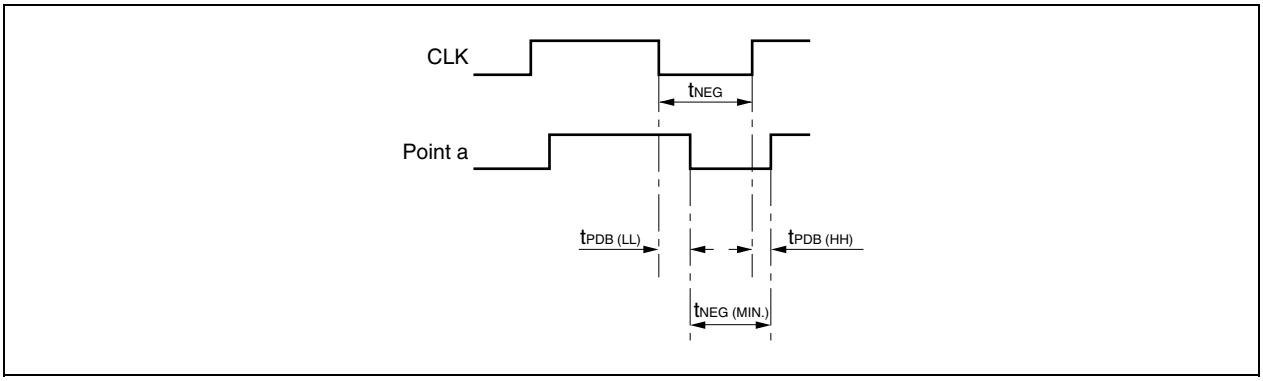


Figure 6-37. Pulse Narrowing



Calculation equations:

$$t_{NEG(MIN)} = t_{NEG} + (t_{PDB(HH)(MAX)} - t_{PDB(LL)[MAX(min)]}) > t_W$$

$$\rightarrow t_{NEG(MIN)} = t_{NEG} + (t_{PDB(HH)(MAX)} - t_{PDB(LL)(MAX)} \times \frac{1-\beta}{1+\beta}) > t_W$$

β: Distribution coefficient (0.1)

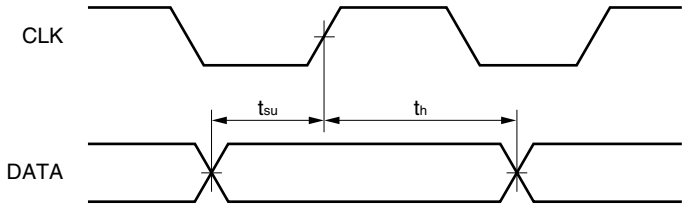
The ratio t_{PDB} (HH)/t_{PDB} (LL) is controlled in order to regulate the minimum pulse width of the signal that is input to the flip-flop. This increases the duty cycle. In the example above, the fall is at the functional block that contains delay B and the delay t_{PDB} (LL) is short. If the rise delay t_{PDB} (HH) is converted to be slow, t_{NEG} (MIN.) increases. In addition, be aware that a high-level pulse width standard must be satisfied.

6.6.5 Metastability

If the set up and hold time standards are satisfied, an output is generated at the flip-flop and latch if a block and data as well as a block and set/reset are changed simultaneously. It then becomes possible to obtain an intermediate level that is neither high nor low. This unstable condition is called metastability.

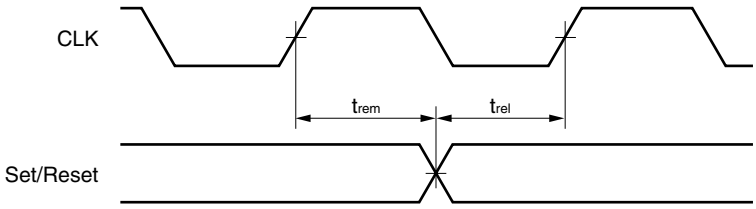
The metastable state is finalized after a certain time, and the output settles into a high or low level. However, an unstable state results since the level that is defined has no relationship to the data input level. In the cases where the set up, hold, release and removal times cannot be satisfied, take the countermeasures shown below to prevent this unstable state from spreading over the entire circuit.

Remark Setup time (t_{su}) … Time that the data signal must secure before the clock changes
Hold time (t_h) ……Time that the data signal must be held after the clock changes



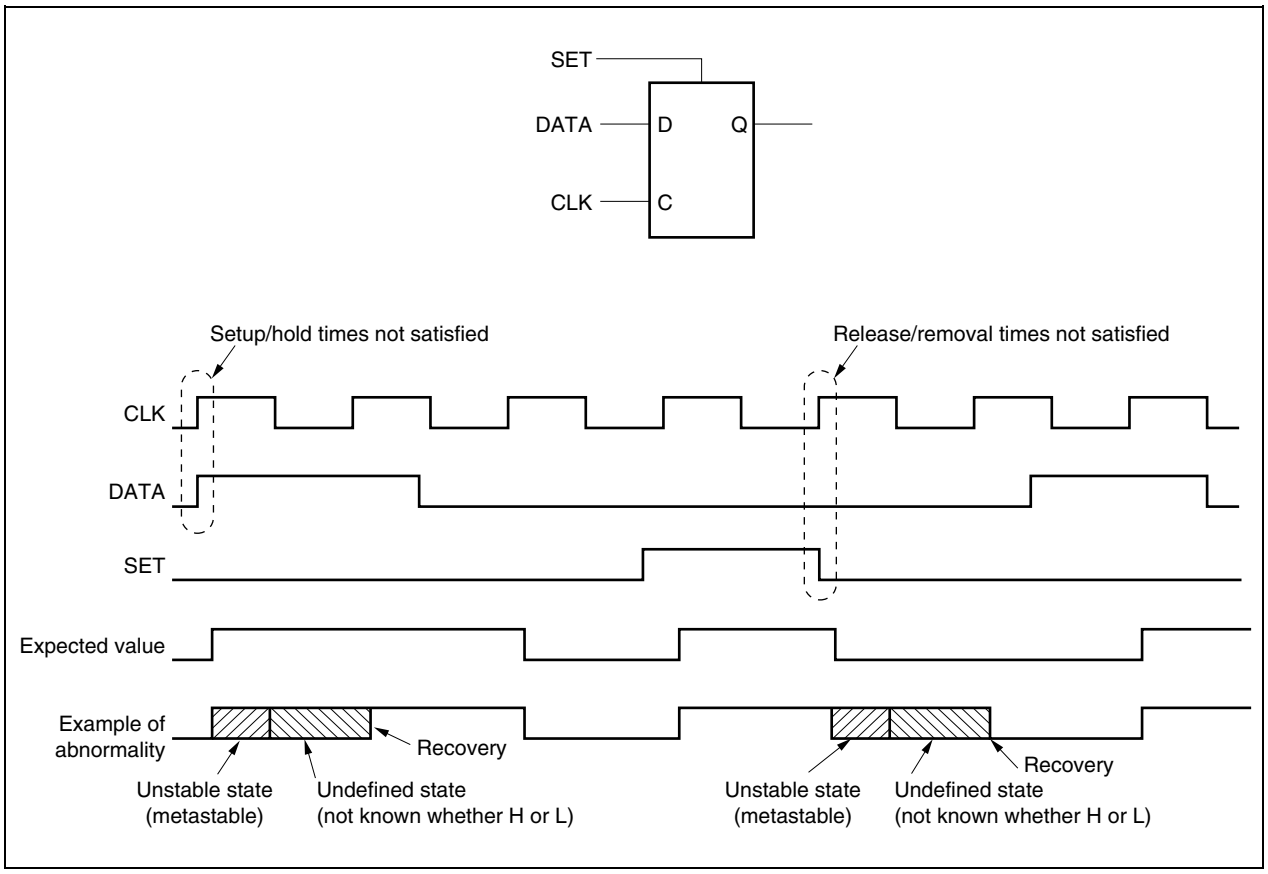
Caution The specified time must be satisfied (see CMOS-9HD Series, EA-9HD Series Block Library (A13052E)) for t_{su} and t_h.

Release time (t_{rel}) .....Time after the set/reset signal changes until the clock becomes valid
Removal time (t_{rem}) ...Time needed in order to make the clock invalid



Caution The set or reset signals must not be cancelled in the vicinity of the active edge of the clock.

(1) Metastability and recovery time



In the EP-1 Series, the time of the metastable state is specified as shown below. After this time, it is not clear whether the state is H or L, but it is one of them (it is shown as “Undefined” in the above figure).

Metastable time = $t_{PD(MAX)} \times 6$

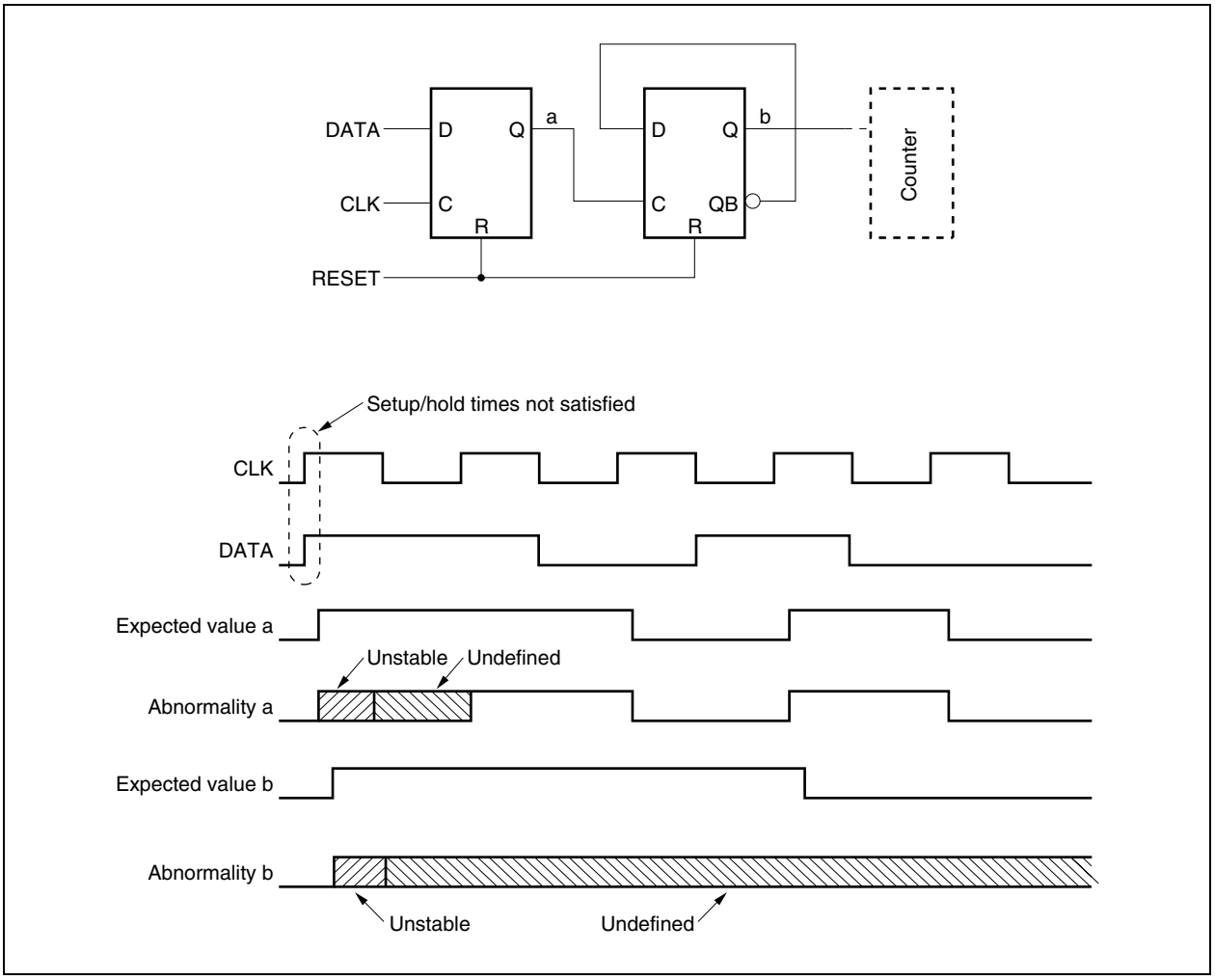
$t_{PD(MAX)}$ ... Maximum value of the delay time from the active edge of the clock until the output changes (when the ratings of the setup/hold times could not be satisfied); or, release/removal time (when the ratings of the release/removal times could not be satisfied).
There is no problem even if t_{PD0} (MAX.) is used in FXXX-type sequential circuits. Their respective values are listed in **CMOS-9HD Series, EA-9HD Series Block Library** (**A13052E**).

(2) Avoiding metastability

When the stipulated times cannot be satisfied (asynchronous input signals), take the following steps to avoid abnormalities.

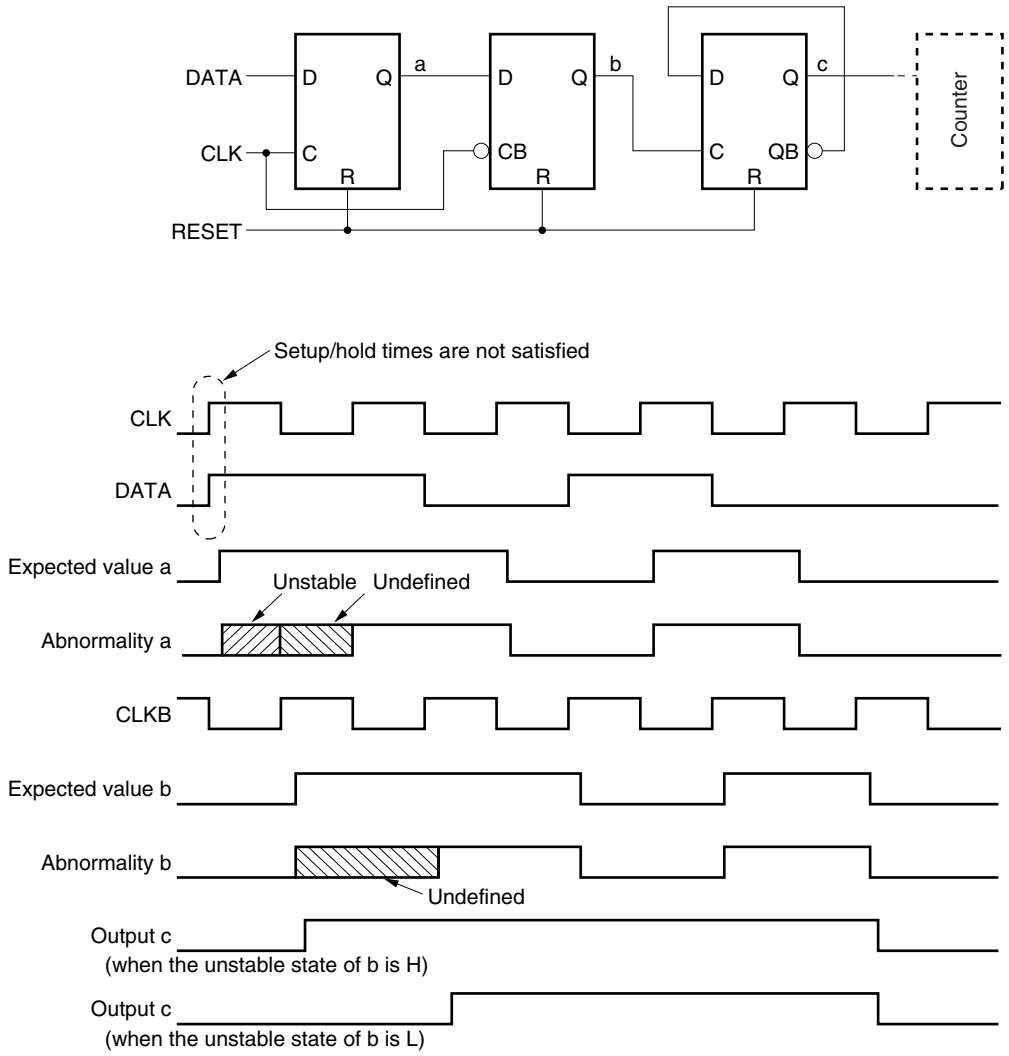
Example of an abnormality

When the output from b in the figure below is input to the counter there is an excess number of counts.



Example of avoiding abnormality

Output c is stable due to the insertion of a 1-step flip-flop. However, although the initial clock at c can have two values as a function of the instability of b, there is no effect on the counter in the following example.



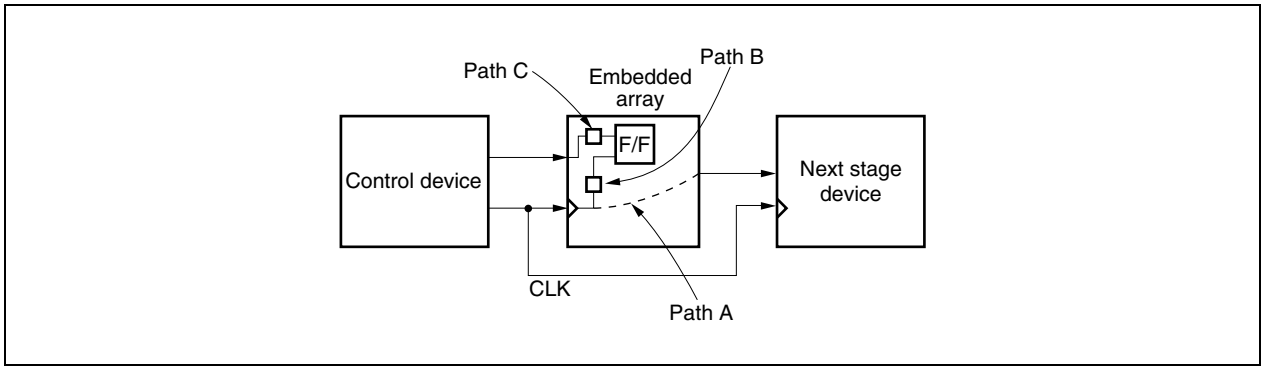
Remark Clock width > t_{PD} (MAX.) × 6 + (t_{su} or t_h)

6.6.6 Critical path guidelines

A critical path relates to the system timing contained in the embedded array. It is the path that establishes the delay time for the embedded array (see Figure 6-38). In this example, a detailed investigation of the path (the critical path) is necessary.

- Path A: Is the timing of the device in the next stage satisfied for embedded array output sampling by the clock?
- Path B, C: Is the sampling timing satisfied in the embedded array by the controlling device's output timing?

Figure 6-38. System with Critical Path



The following are the three types of critical paths:

<1> Input to output
<2> Input to input
<3> Output to output

The inspection and specification methods for these critical paths are explained in the following sections.

(1) Calculating and designing a critical path

As described in **5.4.3 Estimating routing capacitance**, placement and routing are executed by determining the placement range for each macro hierarchy (first hierarchy only). Consequently, the intra-macro and intermacro wiring lengths differ significantly.

The following points must be noted when the propagation delay time of the critical path is estimated using the assumed routing capacitance listed in Table 5-9.

<1> The critical path can be terminated in one macro hierarchy (first hierarchy) (excluding the I/O buffer).
<2> The load connected to the path can be reduced by making the critical path as simple as possible (limiting the fan-out value to 1/3).
<3> Except as given above, the input and output pins should be placed as close together as possible in regard to critical paths from the input to output pins.
<4> Circuits other than critical paths should not be included within macro hierarchies.

(2) Critical path between input and output

Path A in the circuit example of Figure 6-38 is not influenced by the other inputs. The maximum t_{PD} value is designed to be smaller than that required by the system.

In addition, keep in mind the large dependency of the output buffer's propagation delay time on the external load capacitance (C_L).

Calculation equation:

t_{PD} (MAX.) < System specification value

(3) Critical path between two inputs

We will look at calculations for the circuit in Figure 6-39 by studying the input sampling timing. In inspecting this timing, we are assuming the input signal timing shown in Figure 6-40 since the relative timing specifications between the input pins must be well-defined in order to make the calculation.

Figure 6-39. Example of Input-Input Critical Path

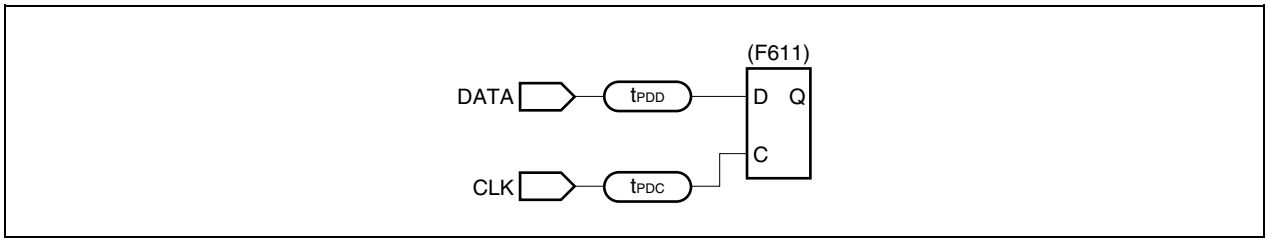
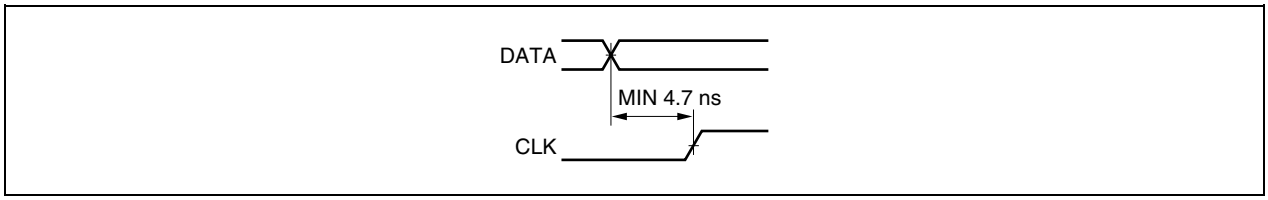


Figure 6-40. Inspection of Setup Time



The following points must be taken into consideration with respect to the conditions used:

- Absolute distribution is in the direction of the smaller margin
- Relative distribution is in the direction of the largest t_{PDD} and the smallest t_{PDC}

The method for making these decisions is shown below.

Calculation equations:

DATA is assumed to be a time differential of 4.7 ns (MIN.) from the clock, as shown in Figure 6-40. $t_{PDC(MIN)} - t_{PDD[MIN(max)]} + 4.7 > t_{SU}$

$$\rightarrow t_{PDC(MIN)} - t_{PDD(MIN)} \times \frac{1+\alpha}{1-\alpha} + 4.7 > t_{SU}$$

α: Distribution coefficient (0.1)

6.6.7 Ensuring operating margin

When the operating margin of a circuit is found to be insufficient from the results of a delay margin check and a critical path check, there are several things that can be done, depending on the circuit configuration.

Generally, the following methods are taken.

<1> Reassess input and output specifications
- Decrease the input f_{MAX}. and lower the input f_{MAX}. duty distribution
- Relax the input and output timing and decrease the output capacitive load

<2> Reassess pin placement
- Shorten the wiring length to decrease the delay between input and output (adjacent placement of pins)

<3> Modify the circuit
- Decrease delay time by simplifying the circuit
- Decrease delay time by decreasing the load on the circuit
- Obtain the margin by inserting a delay gate

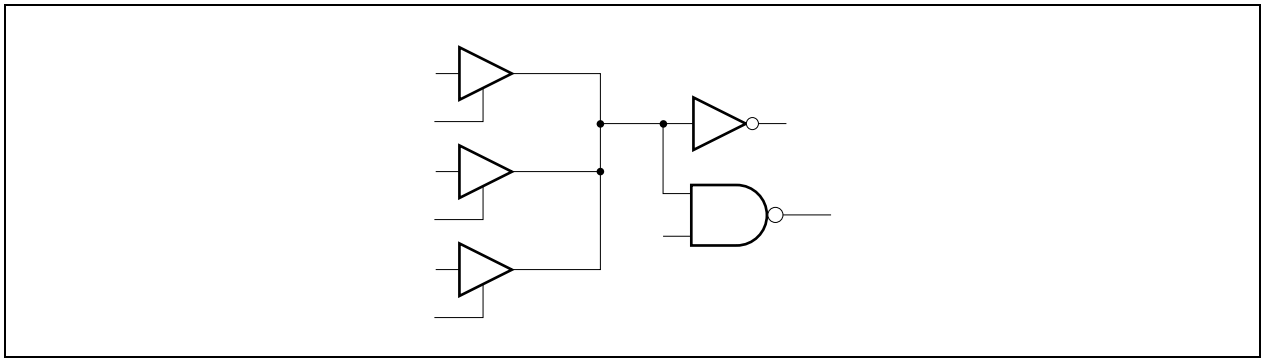
Delay calculations (or recalculations) are necessary when modifying a circuit.

6.7 Internal Bus Structure

6.7.1 Configuring internal bus

Typical data selection techniques include the data selector format and the bus selector format. The circuit structure of a selector (multiplexer) can become very complex. On the other hand, the bus format is comparatively simpler than the circuit structure so it is easier to understand. Further, the propagation delay time increases although there may not be an increase in the number of cells used. Therefore it is important to select the optimum circuit structure.

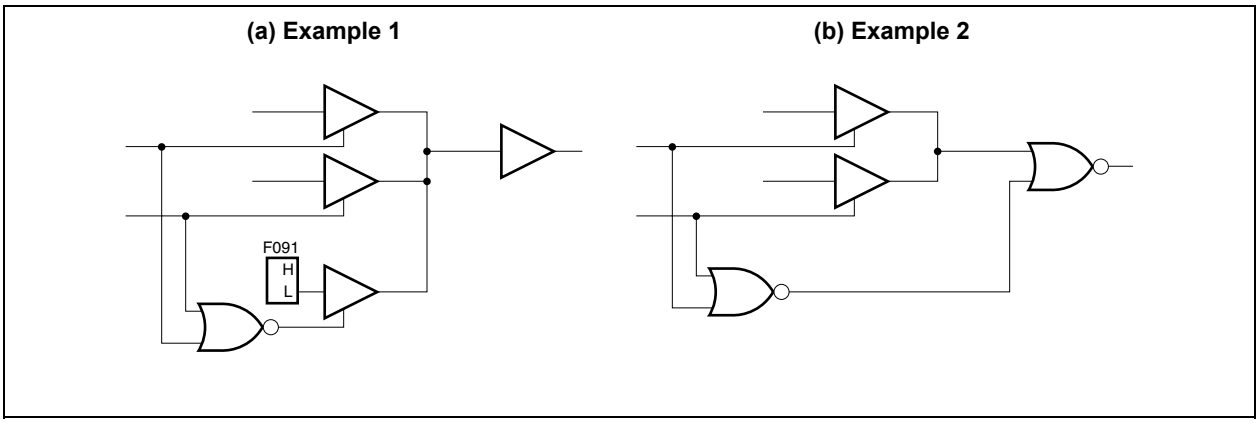
Figure 6-41. Internal Bus Configuration



6.7.2 Preventing internal bus floating

As a basic rule when using an internal bus, a block configured on the same bus line should be in only one output enable state. This is necessary to avoid a floating state in the input of the next stage block. Examples of a good internal bus circuit structure are shown in Figure 6-42.

Figure 6-42. Examples of Internal Bus Floating Prevention Circuit



6.7.3 Precautions

Although several connected blocks can operate on the same bus line when using an internal bus, the signal rise and fall times may increase due to an increase in wiring length and an increase in the fan-in loading of the previous block. Since problems such as operating stability and reliability may result, the following constraints must be observed. For further information, see **6.8 External Bus Contention**.

(1) Observe the bus constraints in the following formula:

$$F/O + N \leq 50$$

$$(1.4 \times F/O + 1.1 \times N + 1.9) \times f < 410$$

F/O … Sum of the fan-in loading (F/I) of the gates connected to the bus
N … Sum of the 3-state buffers (F531, F532) connected to the bus
f … Operating frequency (MHz) of the bus

Contact NEC Electronics when you wish to use a device under conditions that exceed the above restrictions.

(2) Basically, the following states are prohibited for the bus line.

(a) More than two outputs are enabled on the same bus line.
(b) All outputs are disabled on the same bus line.

Consider enable-signal skew such as that which occurs when the signals converge, even though the conditions lie within the 20 ns maximum.

6.8 External Bus Contention

In addition to the explanation in **6.7.3 Precautions**, the following two items should be noted when connecting to a bus in a system that uses EP-1 series and other LSIs.

(1) Bus contention
(2) Bus floating

Take measures with timing design and pull-up/pull-down resistors in order to avoid these problems.

In addition, in order to avoid external bus floating, there are I/O blocks with pull-up and pull-down resistors. For further information, see **CHAPTER 9 MULTI-FUNCTION BLOCKS.**

6.9 Testability

There is more than just logic design when designing a gate array. Test circuits are also necessary. Consider the points shown below when designing the circuit and when making a test pattern. Take the following items into consideration when designing a circuit or test pattern.

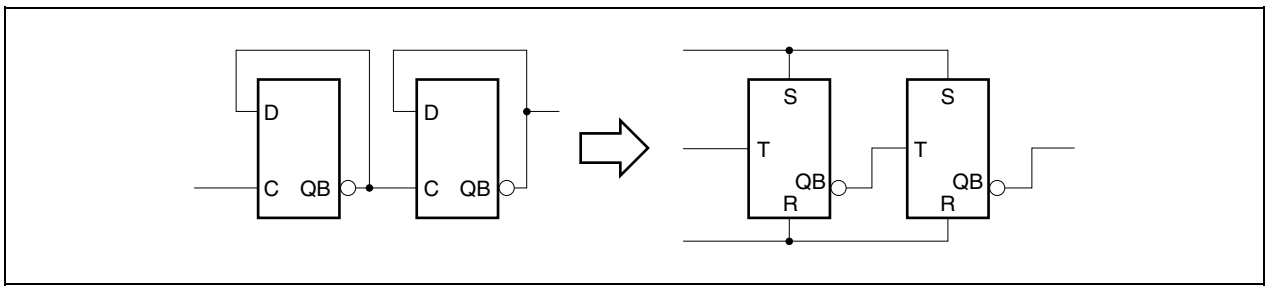
- Flip-flop initialization.
- Division of counters.
- Addition of test pins.
- Division (modularization) of internal circuits by test pins.

6.9.1 Flip-flop initialization

When the device is powered up, it is not known whether the output state of a block, such as a flip-flop or counter, is high level or low level. Consequently, initialization must be performed during the first few patterns when simulating.

In the design stage, the circuit should be configured so that an initialization pattern is not too long, and blocks with reset inputs should be used as much as possible so that the initial state of the internal circuit can be reset to a known state.

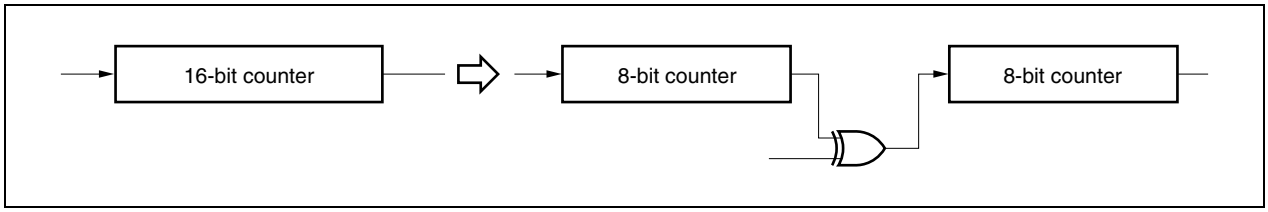
Figure 6-43. Initializing Flip-Flops



6.9.2 Division of counters

With multi-bit counters, the effective test method is to divide the counters to reduce the number of test patterns. For example, the number of pulses necessary until the final stage of a 16-bit counter operates is 2^{16} pulses. By dividing the 16-bit counter into two 8-bit counters as shown in Figure 6-44, however, the number of pulses can be cut by 1/100 to 1/200.

Figure 6-44. Dividing Counters



6.9.3 Adding test pins and dividing circuits

As explained in 6.9.2 Division of counters, there are cases where the number of test patterns increases even when the LSI test is simplified. This is done rather than setting up test pins in multibit counters and large-scale macros so that an operating mode can be externally operated.

(1) A test mode is specially set up when operation is divided into several modes. This is an effective technique for establishing the test-mode pins (test pins).

(2) With large-scale circuits, the several macros (modules) are divided. In this case, test pins are specially set up for partitioning the modules. This is an effective technique for testing LSIs in a partitioned condition.

6.10 Signal Racing and Spike Noise

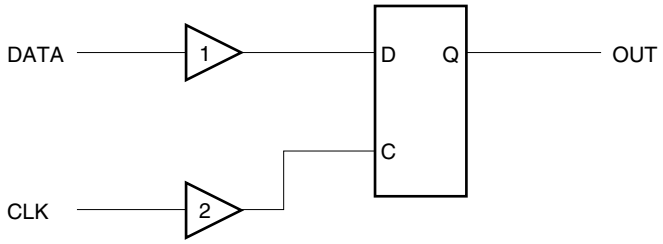
6.10.1 Signal racing (contention)

The condition where the timing changes when there are more than two input signals in a logic block is called racing.

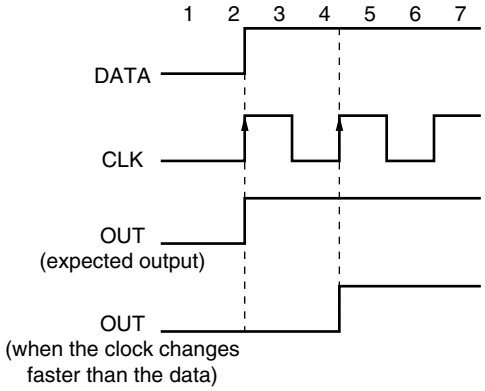
If the test pattern shown in Figure 6-45 (b) is added to a circuit such as that in Figure 6-45 (a), a shift in flip-flop data and clock timing occurs due to the difference between the two delays in buffer 1 and the routing delay difference. The result of this is that the expected operation does not occur. In the case of Figure 6-45 (a), data is first set in the flip-flop, making it necessary to consider a change in the clock. The test pattern for this is shown in Figure 6-45 (c).

Figure 6-45. Racing

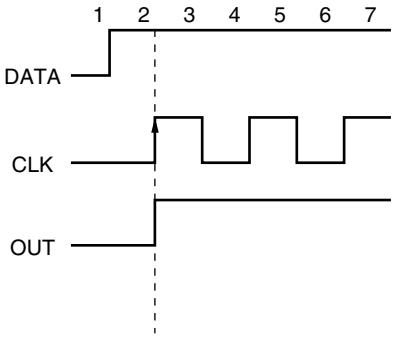
(a) Circuit with potential for racing



(b) Test patterns with potential for racing



(c) Test patterns that do not cause racing



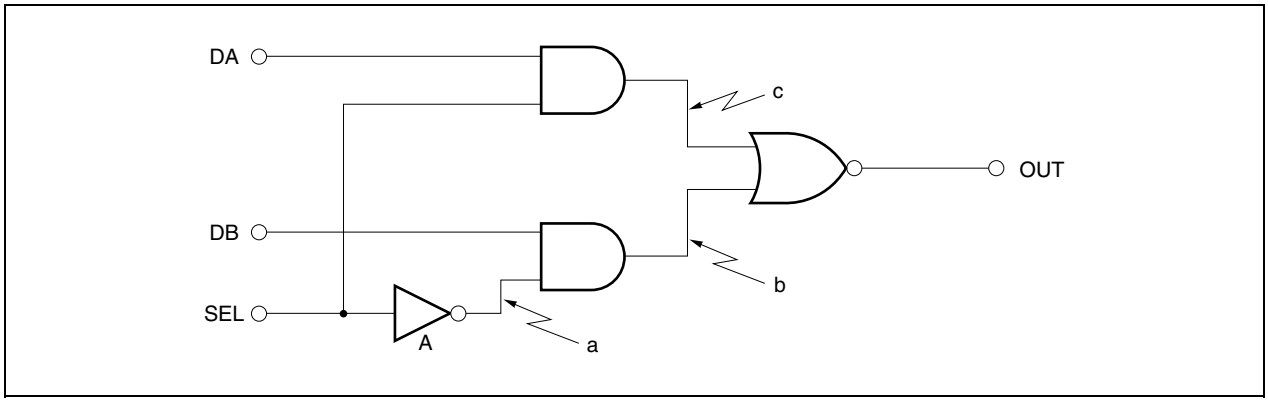
6.10.2 Spike noise

Spike noise is noise in a circuit that employs two or more gate inputs and is caused by a small input timing shift when the input signal timing changes. The time interval of this spike noise changes as a function of the size of the shift in timing. If the spike noise is input to the next-stage flip-flop block and the set/reset, the affected signal path related to the flip-flop's output signal can generate errors in operation.

Consequently, when gates with two or more inputs are used, it must be determined if an influence is exerted on the next-stage gates and the output signals by spikes generated by changes occurring when the multiple inputs change simultaneously. It must also be confirmed whether or not operating errors are occurring. If the spike noise cannot be observed in the following stage, it does not influence that stage, and the test pattern and circuit need not be modified.

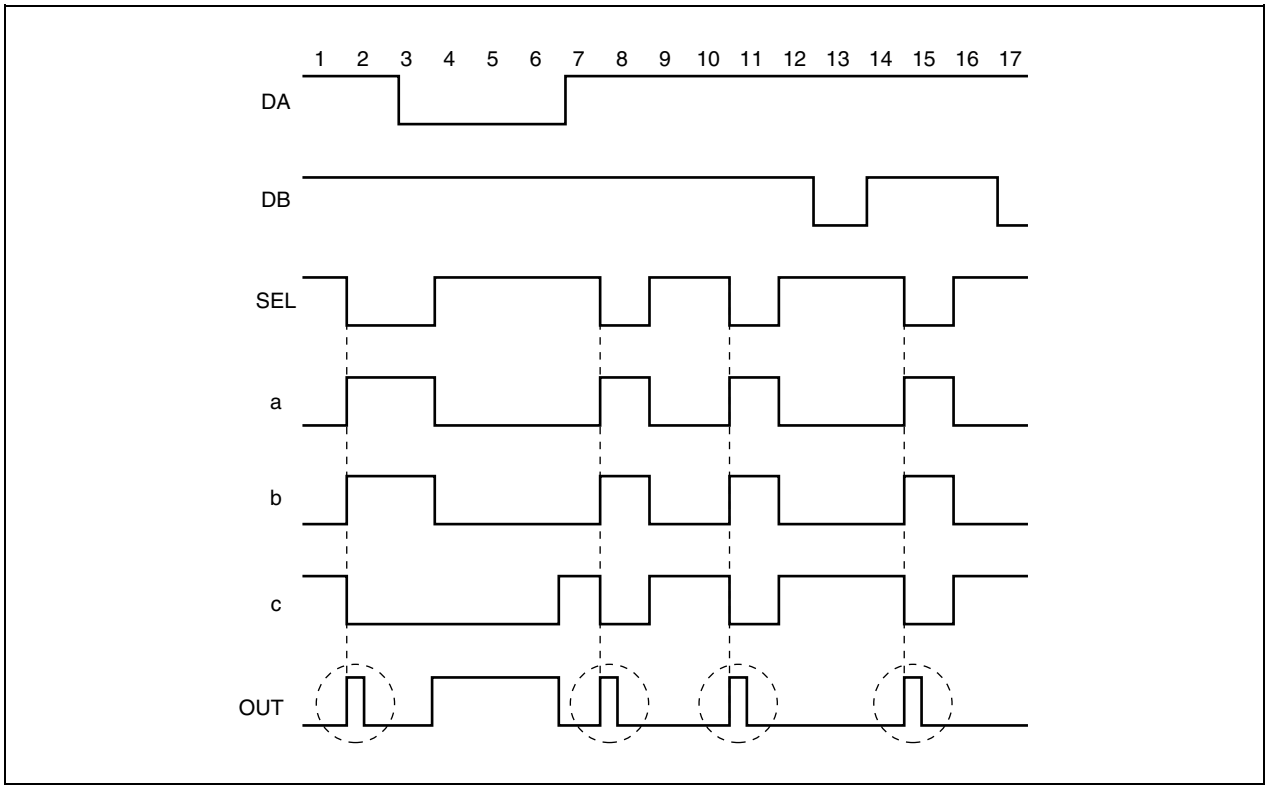
The following is an example of the generation of spike noise and measures that can be taken against it.

Figure 6-46. Data Selector Circuit



The AND-NOR data selector circuit shown in Figure 6-46 will generate the test pattern shown in Figure 6-47.

Figure 6-47. Test Pattern Example (Before Improvement)



In this case, when both the DA and DB input data signals are in a high-level state, spike noise is generated at the output signal OUT since the SEL (select signal) changes from H to L. The pattern in Figure 6-47 generates spikes at pattern locations 2, 8, 11, and 15.

As is clear from the circuit diagram, when DA and DB are in the high-level state, the state of b and c are determined by the state of SEL. In addition, when SEL changes from H to L, b changes from L to H and c changes from H to L in the same pattern. Moreover, a changes when it goes through inverter A and the delay through A is greater than that of SEL. Because of this, b is delayed more than c. Consequently, the state of b and c are simultaneously L and L at 2, 8, 11, and 15 of the test pattern, and L-to-H-to-L spike noise is generated.

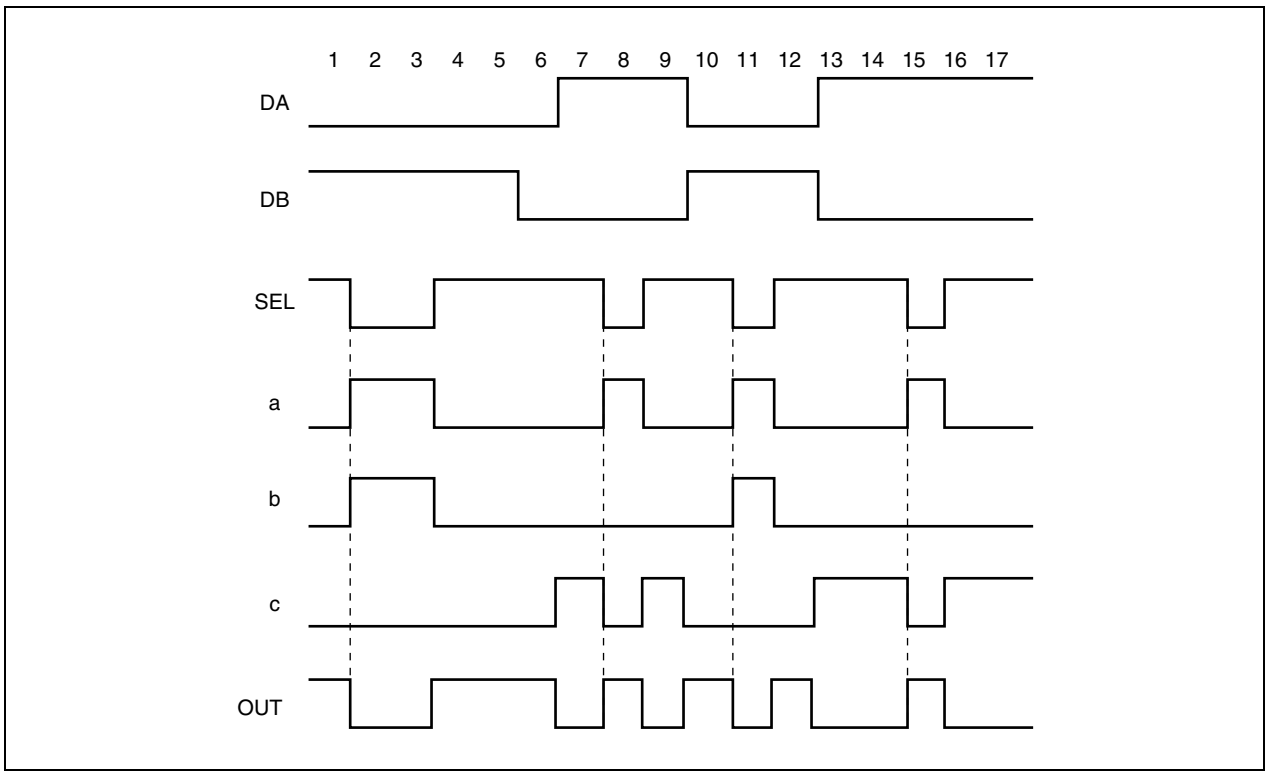
Consider the following two measures if this spike noise is input to the flip-flop block or the set/reset.

<1> Design so that data is not changed, i.e. the output of flip-flops are not changed, due to spike noise at the timing where spike noise occurs.

<2> Modify the test pattern.

In the case of this example, when SEL changes from H to L, make at least one of DA and DB change to L. There is no spike noise at the output OUT if the timing is designed as shown in Figure 6-48.

Figure 6-48. Test Pattern Example (After Improvement)

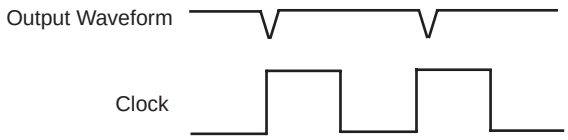


<R> 6.11 Output Waveform Noise

The DC characteristics of the low or high level of the output voltage are as described in **CHAPTER 4 PRODUCT SPECIFICATIONS**; however, noise may occur in the output waveform due to charge and discharge currents of the internal circuit operation.

To minimize the noise in the output waveform, externally add a smoothing bypass capacitor.

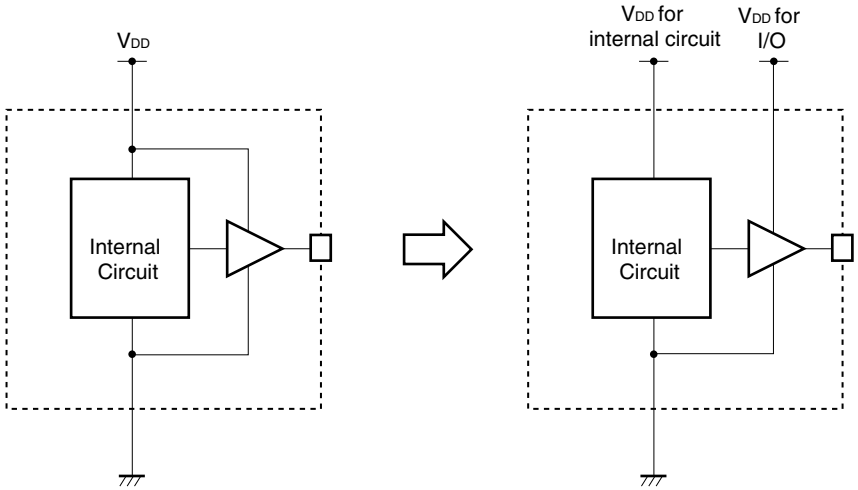
Figure 6-49. Output Waveform Noise



To completely suppress the noise in the output waveform, separate the power supply to V_{DD} for the internal circuit and V_{DD} for I/O.

The separation of the power supply is supported by CMOS-10HD 2-power supply products and EA-9HD 2-power supply products

Figure 6-50. Power Supply Separation



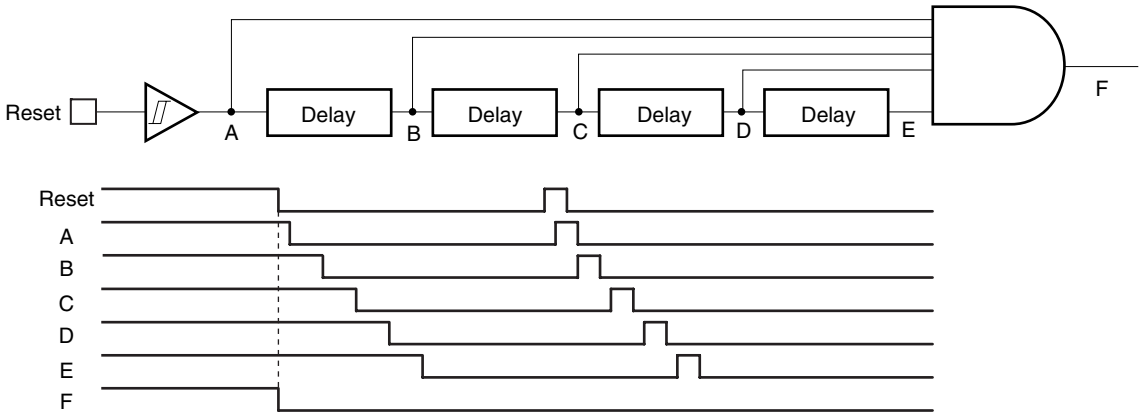
<R> 6.12 Reset Pin

Handle the reset pin as follows in order to prevent a reset operation from occurring when the input level changes momentarily due to noise.

(1) Use as a Schmitt input buffer.
(2) Insert a filter circuit that eliminates momentary pulses.

Figures 6-51 and 6-52 show examples of countermeasure circuits used when a reset (active high) occurs.

Figure 6-51. Countermeasure Circuit Example 1

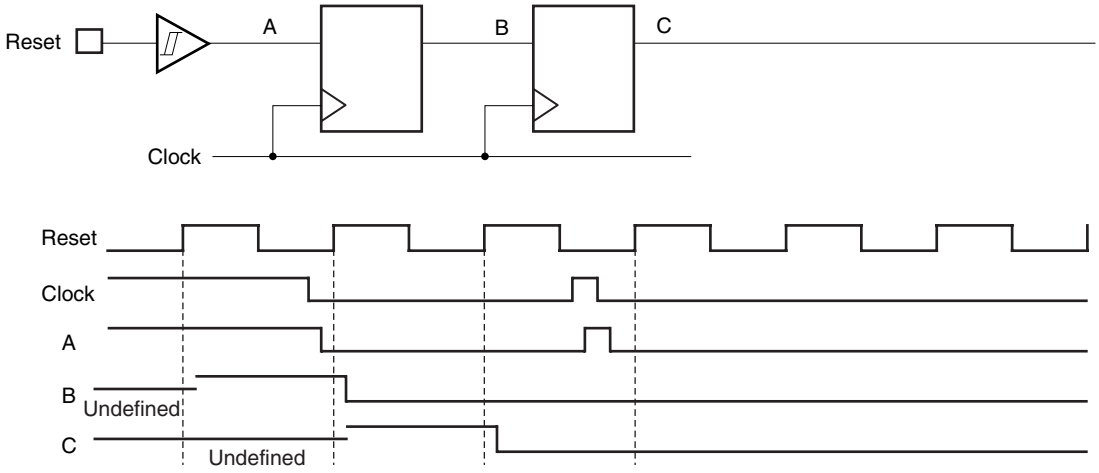


The countermeasure circuit in Figure 6-51 prevents a reset from being activated by a pulse, after a reset has been released.

The reset circuit is released, depending on the input reset.

This circuit is a differential circuit and requires caution regarding the layout. When using the circuit, contact NEC Electronics, because group placement and forcible placement may be required during layout.

Figure 6-52. Countermeasure Circuit Example 2



The countermeasure circuit in Figure 6-52 is configured of two F/F stages, in order to handle metastability that is caused by a conflict between a reset and the clock.

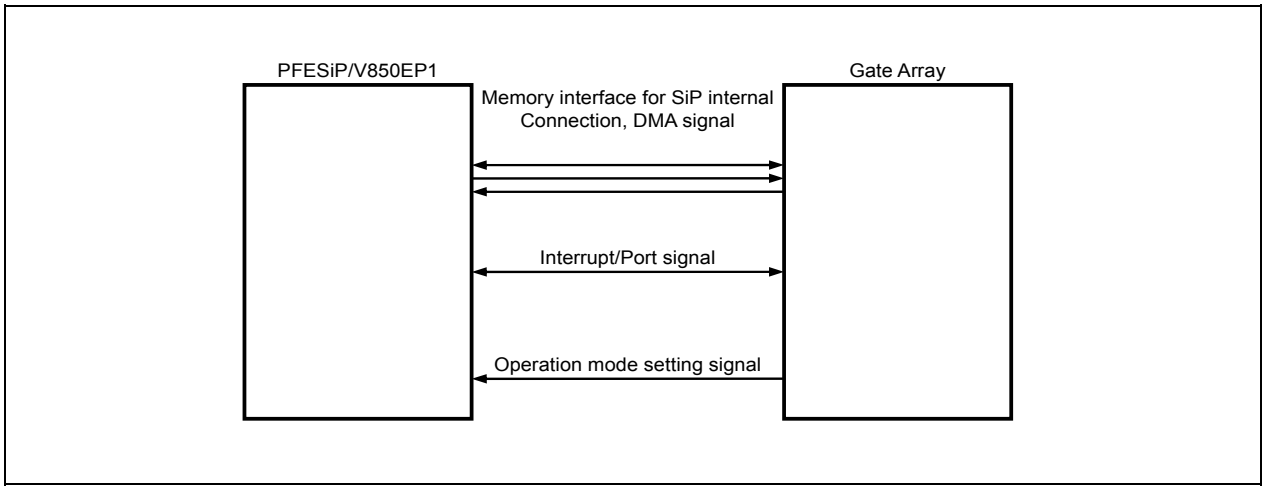
CHAPTER 7 EP SERIES-SPECIFIC CIRCUIT DESIGN

7.1 Connections Between the PFESiP/V850EP1 and Gate Array

Figure 7-1 shows 3 types of the configuration of the connections between the PFESiP/V850EP1 and gate array.

- Memory interface for SiP internal connection, DMA signal (refer to **7.1.1**)
- Interrupt/port signal (refer to **7.1.1**)
- Operation mode setting signal (refer to **7.1.2**)

Figure 7-1. Configuration of Connections Between the PFESiP/V850EP1 and Gate Array



7.1.1 Pins for connections between PFESiP/V850EP1 and gate array (memory interface for SiP internal connection, DMA signal)

As part of the PFESiP mass-production test, bidirectional-bus conflicts between the PFESiP/V850EP1 and gate array must be prevented when testing the PFESiP/V850EP1. Furthermore, caution must be exercised for the gate array I/Os, so that unnecessary steady currents do not flow through the pull-up and pull-down resistors of the I/O buffers on the PFESiP/V850EP1 side.

Consequently, use predetermined buffer types for the memory interface signals for SiP internal connection of the gate array, DMA I/O signals for SiP internal connection, and interrupt and port signals. In addition, the pin name must require the same name as the PFESiP/V850EP1 SiP internal connection pin to prevent a connection mistake.

<R> Please control the I/O of SD0 to SD15 by 8-bit of SD0 to SD7 or SD8 to SD15.

Table 7-1, 7-2, and 7-3 list buffers in detail, and Figure 7-2 shows signal connection with buffers.

Table 7-1. Memory Interface Signals for SiP Internal Connection (54 pins)

Pin Name	Buffer Type	Function
SCSZ0 to SCSZ3	FI01B1	Memory controller chip select
SA0 to SA20	FI01B1	Address bus (20 bit width)
SD0 to SD15	B00UBB	Data bus (16 bit width)
SRDZ	FI01B1	Read strobe signal
SBENZ0, SBENZ1	FI01B1	Bite enable (shared with SWRZ0-1: SiP internal dedicated write strobe signal)
SIOWRZ	FI01B1	Write strobe signal for external I/O
SIORDZ	FI01B1	Read strobe signal for external I/O
SWRSTBZ	FI01B1	Write strobe output (WRZ [3:0] OR)
SWAITZ	FO09B2	Wait signal
SHLDRQZ	FO09B2	Bus hold request
SHLDAKZ	FI01B1	External bus hold request acknowledge
SBCYSTZ	FI01B1	Bus cycle start status
SBUSCLK	FIS1B1	Bus clock
SREFRQZ	FI01B1	Refresh status
SRESTOZ	FIS1B1	Bus reset

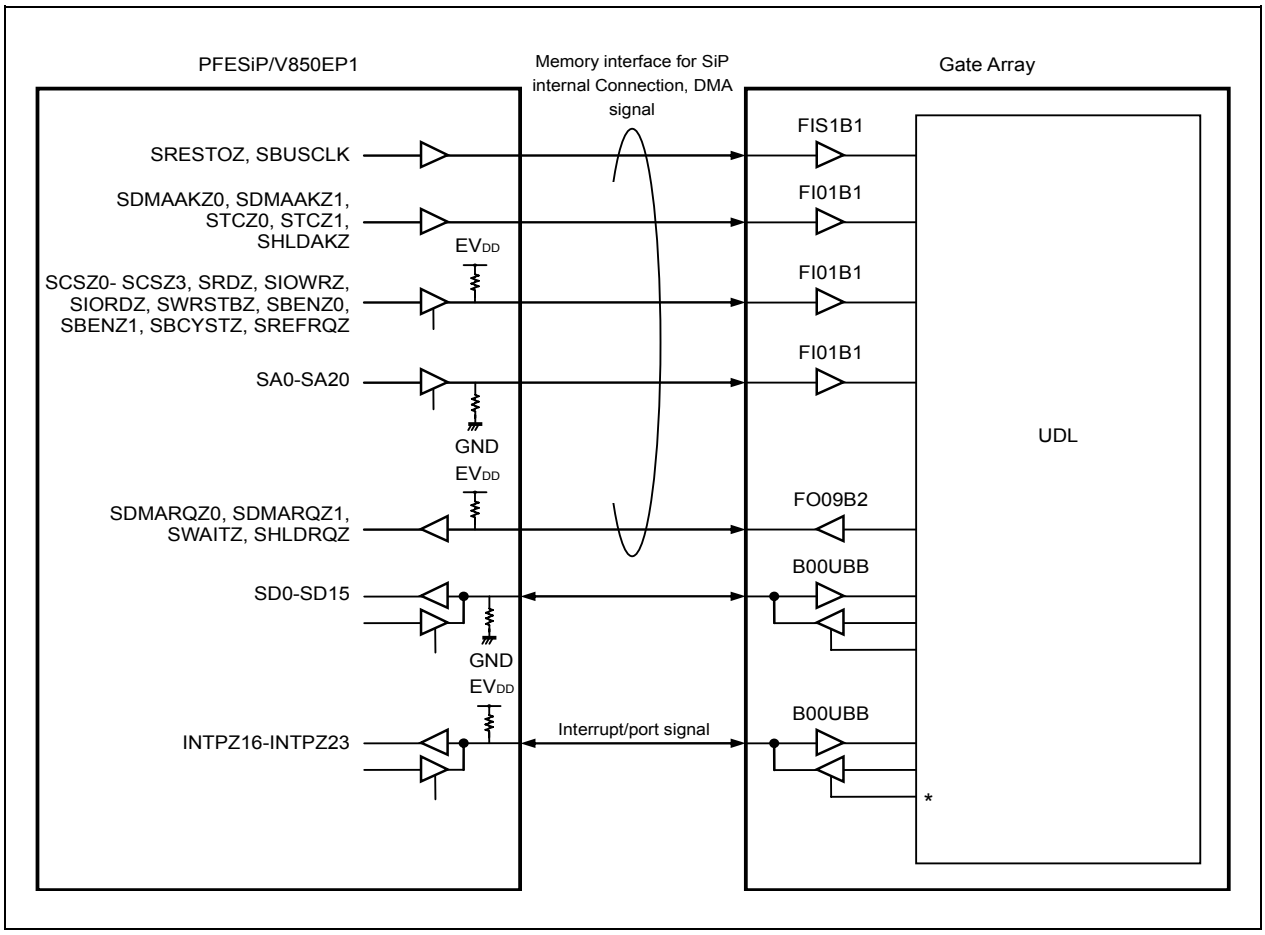
Table 7-2. DMA I/O Signal for SiP Internal Connection (6 pins)

Pin Name	Buffer Type	Function
SDMARQZ0, SDMARQZ1	FO09B2	DMA transfer request
SDMAAKZ0, SDMAAKZ1	FI01B1	DMA acknowledge
STCZ0, STCZ1	FI01B1	Terminal count (DMA transfer completed)

Table 7-3. Interrupt/Port Signals (8 pins)

Pin Name	Buffer Type	Function
INTPZ16 to INTPZ23	B00UBB	Maskable external interrupt (shared with PORT20 to PORT27: port)

Figure 7-2. Connections Between the PFESiP/V850EP1 and Gate Array (1)



Use the buffers shown in Tables 7-1 to 7-3, even if the pins are not being used.

Connect the input buffer output pin to a function block (such as F101 or F111) shown in E.2 on page 315, and leave its output open.

Use F091 to clamp the output buffer so that its signal is deasserted.

In the case of a bidirectional buffer, deassert the control signal and set it to be high impedance as a pin on the PFESiP/V850EP1 side.

When using an interrupt/port signal as an interrupt, fix the control signal (signal marked with an asterisk (“*”) in Figure 7-2) to high level.

7.1.2 Pins for connection between PFESiP/V850EP1 and gate array (operation mode setting signal)

Design a circuit which can be used to set values in the gate array block for the following operation mode setting pins (28) of the PFESiP/V850EP1.

To use the operation mode settings by completely fixing them, determine the logic by performing pull-up or pull-down processing for the desired logic in the gate array block.

To change the operation mode settings after production, externally determine the desired logic by assigning the logic to the external pins of the gate array block. Note, however, that dynamically changing these settings during operation is not assumed.

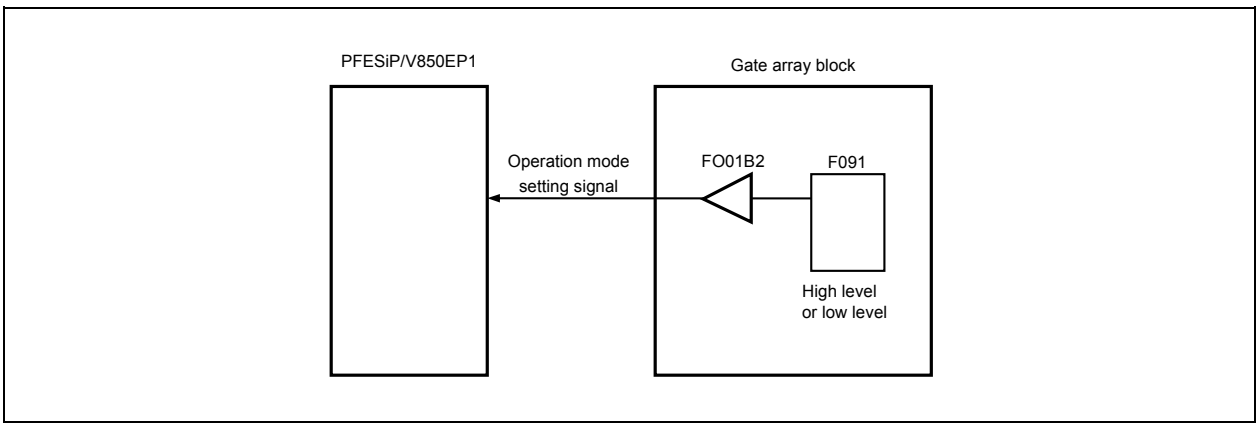
For the details on the operation mode settings, refer to **PFESiP/V850EP1 Hardware (CPU Function) User's Manual (A19070E)**.

Be sure to use the buffer (FO01B2) shown in table 7-4. In addition, the pin name must require the same name as the PFESiP/V850EP1 SiP internal connection pin to prevent a connection mistake.

Table 7-4. PFESiP/V850EP1 Operation Mode Setting Signals (28 pins)

Pin Name	Buffer Type	Function
SLBS1 to SLBS0	FO01B2	Input for selecting the MEMC external bus width 00: 32 bit, 01: 16 bit, 10: 8 bit, 11: 8 bit
VBCLKEN	FO01B2	Input for enabling or disabling the VBCLKOUT output 0: low level output, 1: enabled
SCKMD1 to SCKMD0	FO01B2	nput for selecting the ratio between VBCLK and BUSCLK of NBA85E535 00: VBCLK/1, 01: VBCLK/2, 10: setting prohibited, 11: setting prohibited
VSBRAMEN	FO01B2	Input for enabling the work RAM (VSB_RAM) 0: invalid, 1: valid
CLKDV1 to CLKDV0	FO01B2	Input for selecting the division ratio between CPCLK and VBCLK 00: setting prohibited, 01: CPCLK/2, 10: CPCLK/3, 11: CPCLK/4
BOOTSEL	FO01B2	Boot selection 0: SCSZ0 area (from internal SiP), 1: CSZ0 area (from external bus)
PLL6 to PLL0	FO01B2	(PLLM6 to PLLM0) Input for setting the multiplication factor for the internal PLL
PLL9 to PLL7	FO01B2	(PLLN2 to PLLN0) Input for setting the multiplication factor for the internal PLL
PLL11 to PLL10	FO01B2	(PLLP1 to PLLP0) Input for setting the multiplication factor for the internal PLL
PLL13 to PLL12	FO01B2	(SSMDL1 to SSMDL0) Input for setting the SSCG modulation range
PLL16 to PLL14	FO01B2	(SSADJ2 to SSADJ0) Input for setting the SSCG frequency diffusion mode and corresponding range
PLL18 to PLL17	FO01B2	(PLLS1 to PLLS0) S selector input of SSCG

Figure 7-3. Connections Between the PFESiP/V850EP1 and Gate Array (2)



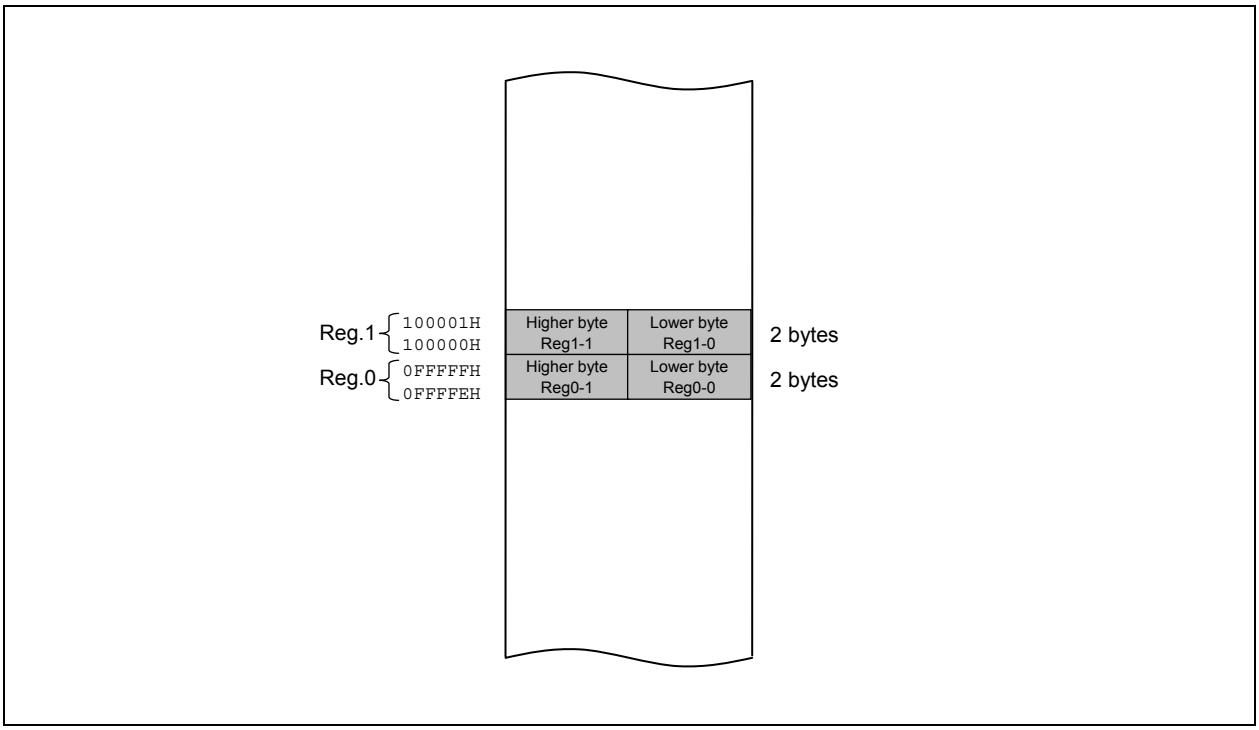
For the details of pins for connection between PFESiP/V850EP1 and gate array, refer to **PFESiP/V850EP1 Hardware (CPU Function) User's Manual (A19070E).**

7.2 Memory Interface for PFESiP/V850EP1

The memory interface for SiP internal connection must be noted regarding the logic design with regard to the AC timing for the connection between the PFESiP/V850EP1 and gate array. To design a memory interface circuit for SiP internal connection, see the **PFESiP/V850EP1 Hardware (CPU Function) User's Manual (A19070E)**.

Provide a test register that can be read- or write-accessed from the PFESiP, via the memory interface for SiP internal connection. It must be visible as a part of the CPU memory map of the PFESiP and provide it for the following fixed addresses. (Provide it at a 16-bit width for each 0FFFFEH and 100000H.)

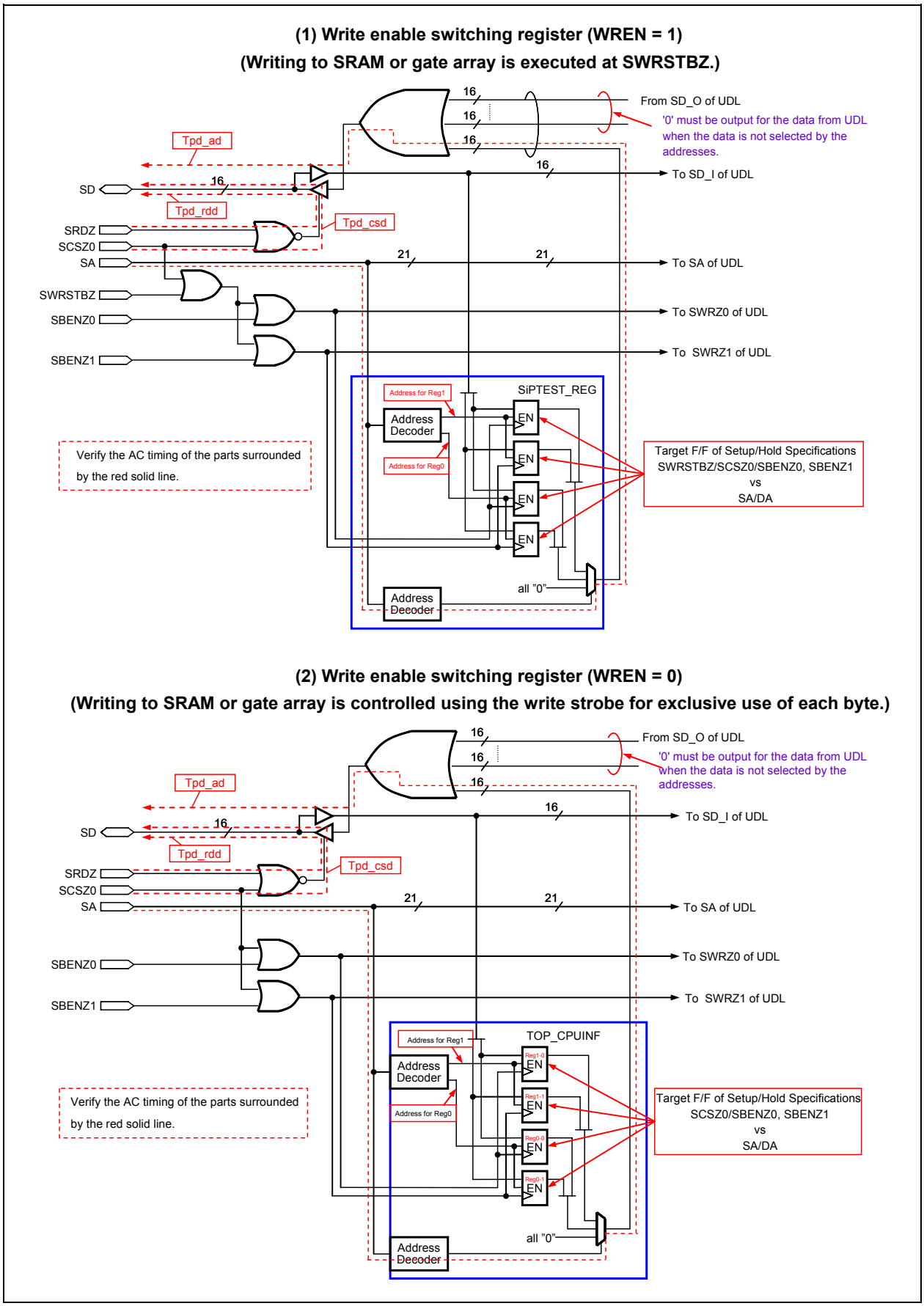
<R> **Figure 7-4. Test Register That Can Be Read- or Write-Accessed from PFESiP/V850EP1**



To access these registers via the memory interface for SiP internal connection, please inform NEC Electronics of the memory controller settings of the PFESiP/V850EP1.

For reference, the following figure shows an example of the connections between the PFESiP/V850EP1 and gate array.

<R> **Figure 7-5. Example of the Connections Between the PFESiP/V850EP1 and Gate Array**



7.3 Design for Test (DFT)

7.3.1 Boundary-Scan test (NEC_BSCAN) application

Use a Boundary-Scan test to test the connection between the PFESiP and gate array.

It is therefore required to apply a BoundaryScan test circuit for the gate array block.

A circuit design using a dedicated interface block and processing for inserting a TAP controller macro is required. Use the above-mentioned interface block and TAP controller as markers to automatically generate a Boundary-Scan circuit by using a dedicated tool.

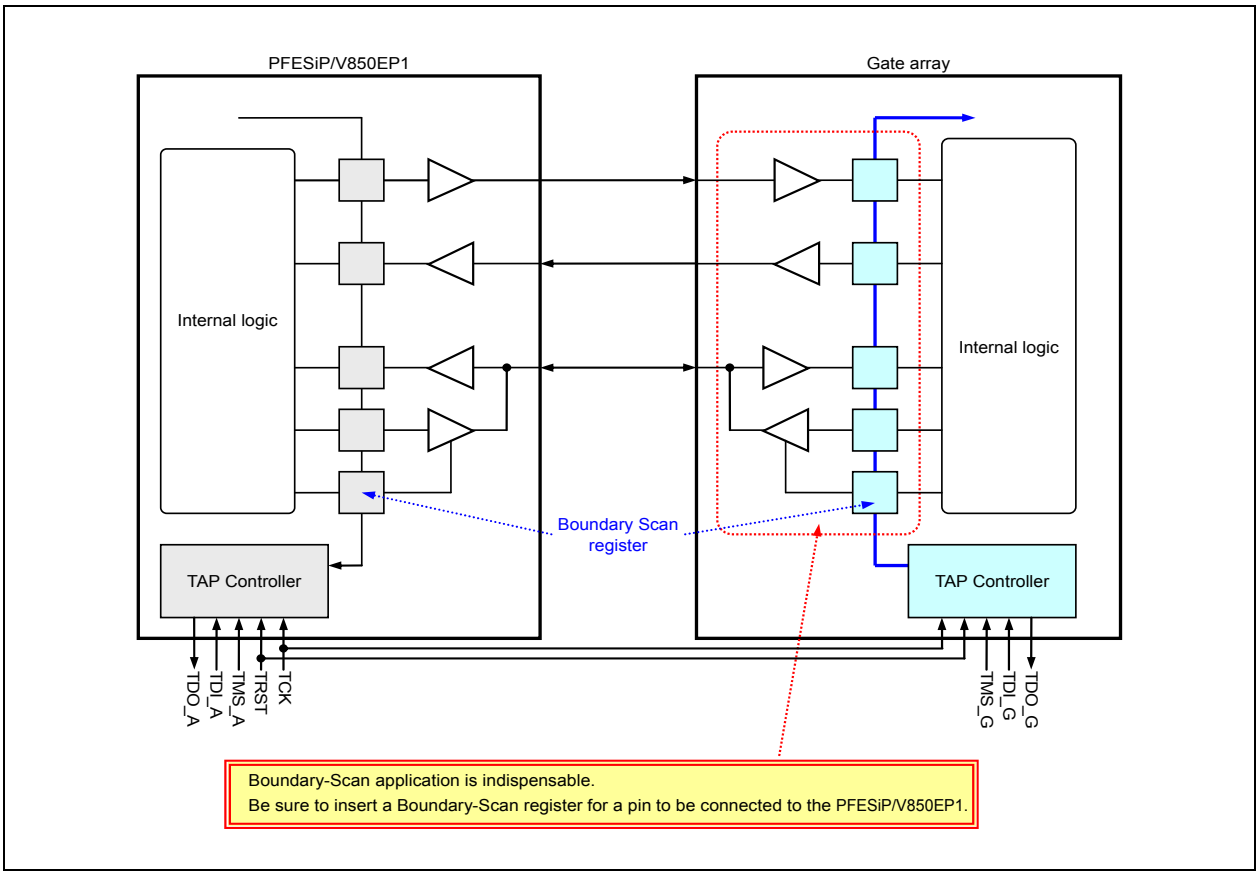
Note that inserting a BoundaryScan register for a dedicated test pin (such as a TEB of a BIST circuit or a test mode pin of a mega macro) in order to prevent the mounted macro to be set to the test mode during the BoundaryScan mode is prohibited. (A BoundaryScan register can be inserted for a test pin that is shared with a user pin.)

A specific pin can be excluded from a BoundaryScan register being inserted by designing the circuit by using a normal interface block, instead of a dedicated interface.

For details of the procedure, see **5.3 NEC_BSCAN Design Method** in the Design For Test User's Manual.

<R> TCK and TRST are shared by the PFESiP/V850EP1 and gate array. In addition, do not count TDI_G, TDO_G, and TMS_G pins of the gate array in the number of user pins because these pins are secured separately from user pins.

<R> **Figure 7-6. Boundary-Scan Test (NEC_BSCAN)**



7.3.2 Combined use with scan test (NEC_SCAN2)

NEC_BSCAN mentioned above and NEC_SCAN2 can be used together for designing.

Scan tests can be controlled via the TAP controller and the required number of test pins can be reduced by using them together for designing. To apply a Scan test for the logic block, a BoundaryScan test must be used together for designing. For details, see **6. DESIGN WITH TWO DFTs** in the Design For Test User's Manual.

7.3.3 Test design when mega macro is mounted

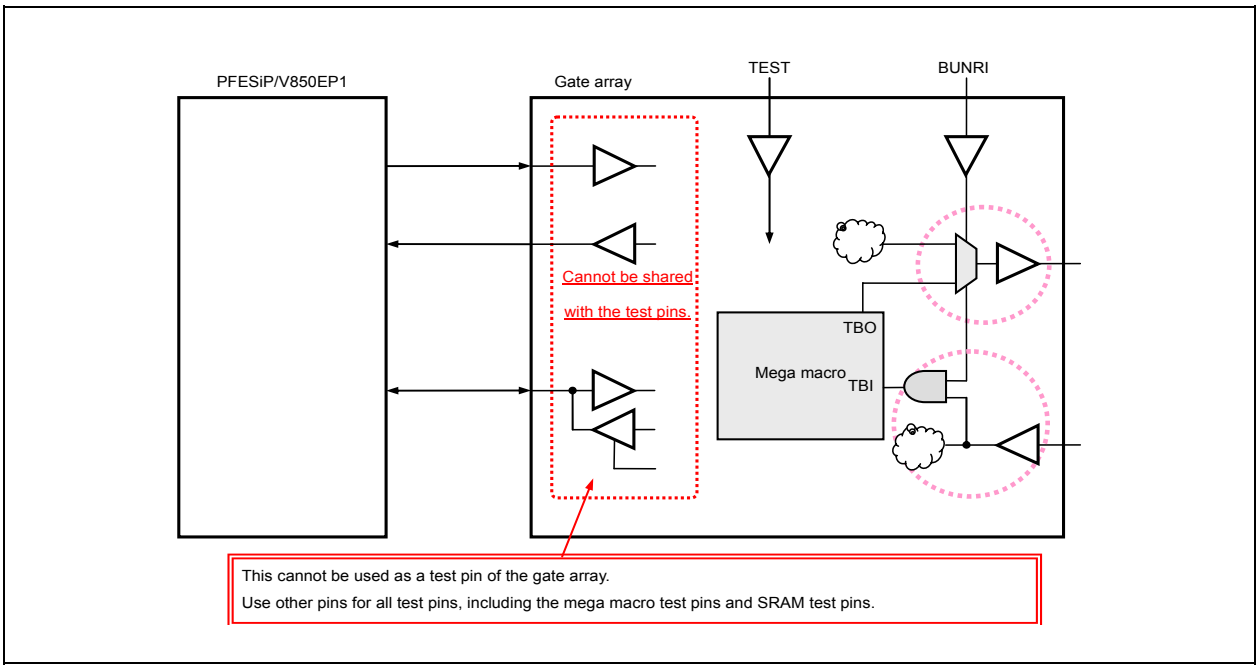
Design a test by referring to the edition on mega macros.

The test pins of a mega macro can be shared with user pins, except for the mode control pins.

To share the test pins with user pins, perform designing by noting the following cautions and the cautions described in the edition on mega macros.

- The mega macro test pins cannot be shared with the user pins to be connected to the PFESiP. With SRAMBIST, the same constraint is applied for test pins that can be shared with user pins.

Figure 7-7. Test Design When a Mega Macro Is Mounted



CHAPTER 8 TEST PATTERN GENERATION

When designing with gate arrays, the circuit's expected function and performance are verified through simulation on a computer. To execute the simulation, the user is requested to prepare a circuit diagram and test patterns.

These test patterns are also used for product inspection before shipment. During shipment inspection, the functions of the LSI are verified (test function) and the DC characteristics (such as power supply leakage current, input leakage current, and output current) are tested. Unless adequate consideration is given to the shipment inspection, therefore, the product is not thoroughly tested when shipped. Therefore, generate test patterns with which fault detection and DC testing can be performed.

During simulation, the conditions under which the LSI is actually used by the user can be realized relatively easily. The LSI tester, which tests the actual LSI, however, cannot completely reproduce the conditions under which the user actually uses the LSI, in many cases. Therefore, generate the test patterns in accordance with the capability of the LSI tester and by observing specified limits.

This chapter describes the points to be noted when generating test patterns.

8.1 Test Pattern Types

The types of test patterns available are shown in Table 8-1.

One DC test pattern is essential, but other test patterns may also be necessary depending on circuit or user requirements. When the LSI tester is used to perform DC measurement, the measurement is carried out using up to the first 32,000 patterns of the DC test pattern.

Table 8-1. Test Pattern Types

Pattern Name	Purpose	Pattern Generator
DC test pattern	DC measurement, logic verification	User
Function test pattern	Logic verification	User
High-speed function test pattern	Logic verification (real time)	User
Megamacro initialization pattern	Initialization	NEC Electronics (inserted by user)
Megamacro single-unit test setting pattern	Setting megamacro peripheral values	User
Megamacro test pattern	Logic verification (megamacro single unit)	NEC Electronics
Scan test pattern	Fault detection	User or NEC Electronics
RAM test pattern	Logic verification (RAM single unit)	NEC Electronics
Digital PLL initialization pattern	Initialization	User
Boundary scan test pattern	Logic verification (boundary scan circuit)	User

Although the pattern length per pattern is not restricted (except for the high-speed function test), the total pattern length is. For details, refer to **8.2.2 Limitations on test pattern length**.

8.2 Notes from Viewpoint of Product Test (LSI Tester)

8.2.1 I/O pin naming conventions

(1) Maximum number of characters for I/O pins

64 characters MAX.

(2) Data submitted for first sign-off

Some characters must not be used when specifying a pin name.

The characters that can be used are listed in the table below.

Table 8-2. Restrictions on Pin Names

Usable characters	Alphabetic uppercase letters Numeric characters “_” (underscore)
Unusable characters	“ / ” (slash) and all other special characters other than the underscore Alphabetic lowercase letters

8.2.2 Limitations on test pattern length

The length of a test pattern is limited by the size of the LSI tester’s memory.

The minimum and maximum lengths of test patterns (for DC test and for the function test) are listed in Table 8-3.

Table 8-3. Limitations on Number of Test Patterns

Number of Patterns / Package[Note 1]	Minimum Number of Test Patterns (Applicable to DC Test Patterns)	Maximum Number of Test Patterns[Note 2]
144 pins or less (with SCAN)	150 patterns	128 K patterns
144 pins or less (without SCAN)		256 K patterns
145 pins or more		512 K patterns

Notes 1. The number of package pins includes the number of power supply pins (GND, V_{DD}, etc.).

2. The maximum length of test pattern does not need to be considered for the RAM test pattern, scan test pattern generated by NEC Electronics, and high-speed function test pattern.
Examine each length of test pattern for the user-generated test pattern and megamacro boundary scan, taking the limited pattern length above into consideration.

8.2.3 Number of test patterns

There can be more than one test pattern. The maximum number of patterns is 20, including all interface test patterns such as those for DC test and function test. In this case, the RAM test pattern, scan test pattern generated by NEC Electronics, and high-speed function test pattern do not need to be considered.

However, the number of test patterns should be minimized as far as possible in order to increase efficiency. Even if the test pattern is divided for the sake of convenience of design, in principle, submit one test pattern to NEC Electronics (the test patterns can be easily combined by using the wave editor of the pattern utility or OPENCAD).

To divide the test pattern, initialize each pattern (see **8.3.1 Initializing circuit**). If this is not possible, be sure to inform NEC Electronics of the sequence of the test patterns (in writing).

The test pattern must be divided in the following cases.

- If the time conditions (input delay and pulse width) and output judge time (strobe time) of the input signals differ. For details, see **8.3 Notes on Generating Test Pattern for Function Test**.

8.3 Notes on Generating Test Pattern for Function Test

8.3.1 Initializing circuit

Whether the output state of blocks, such as flip-flops and counters, is at the high level or low level immediately after power application is unknown (see **6.9.1 Flip-flops initialization**). Consequently, the initial status of sequential circuits such as flip-flops and counters is “X” (undefined) during simulation. To verify operation of the circuit, it is necessary to change the internal function block state from an indeterminate state to a determinate state (circuit initialization).

When designing a circuit, prepare a pattern that can initialize the circuit at the beginning of the test pattern, and at the same time, consider use of a reset pin, so that the circuit can be easily initialized.

When preparing divided test patterns, in principle, initialization is necessary for each pattern (see **Figure 8-4 Test Pattern Example**).

8.3.2 Test period (test rate)

The test rate is referred to as the cycle of one test pattern.

Currently, the test period limitation at NEC Electronics for a general function test is as follows:

Test period: 200 ns

If a higher-speed test period than above is desired, perform the high-speed function test. For the high-speed function test pattern, refer to **8.9 High-Speed Function Test (Real-Time Test)**.

8.3.3 Output determination time (strobe time)

The output determination time (strobe time) refers to the time during which the output value of the product is referenced with the expected value on the test pattern. In the current normal function test pattern, this time is always the final time (199.99 ns) of the period, and anything outside of this becomes a high-speed function.

For details of the high-speed function test pattern, see **8.9 High-Speed Function Test (Real-Time Test)**.

8.3.4 Specification of timing phase

For the specification of timing phases currently supported, refer to Table 8-4 (including the basic timing).

The skew among the pins of the LSI tester (specified as ±5 ns) must be considered, and the time differential of each phase must be set to 10 ns or greater.

The basic timing phase indicates the NRZ signal when Δt_D = 0 ns. NRZ signals with an equal delay time (Δt_D) are considered as in-phase and counted as one phase no matter how many input pins there are with the same timing.

Likewise, RZ signals with an equal delay time (Δt_D) and pulse width (Δt_W) are also considered as in phase.

Positive clocks and negative clocks with an equal Δt_D and Δt_W are also counted as one phase. However, NRZ signals and RZ signals with an equal Δt_D are in-phase.

Table 8-4. Timing Phase Number

PKG	Timing Phase Number[Note]
All packages	6

Note Including basic timing phases.

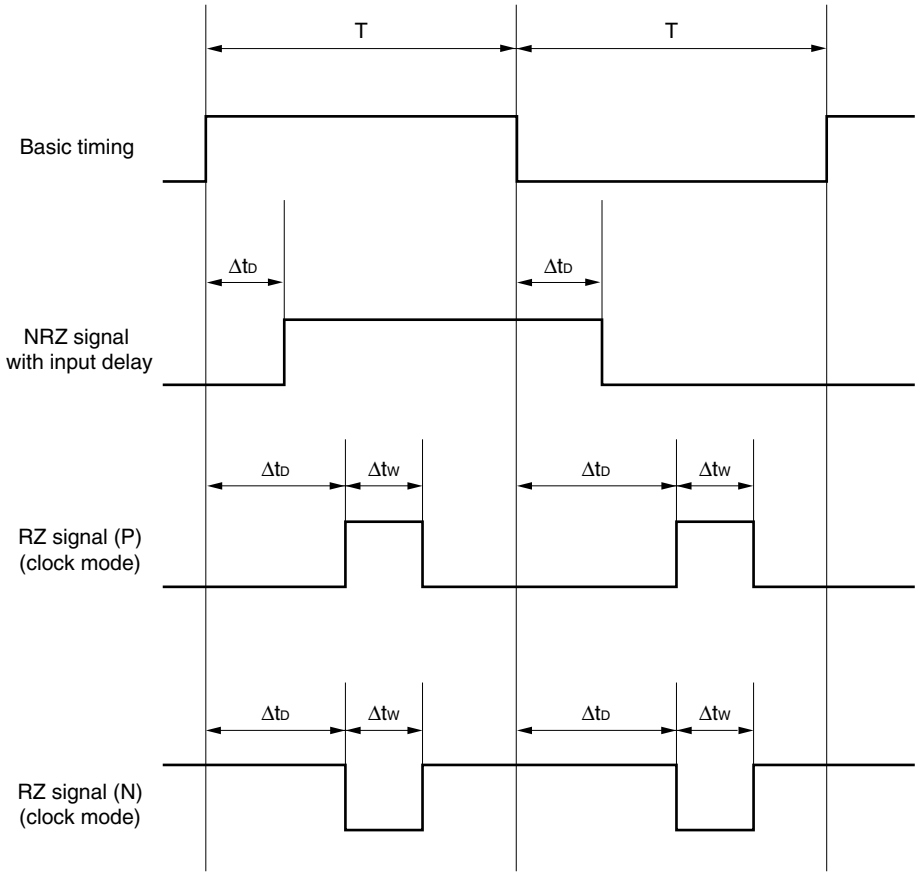
Table 8-5. Timing Constraints

Timing Limit / Signal Type	Input Delay (Δt_D)		Input Pulse Width (Δt_W)	
	MIN.	MAX.	MIN.	MAX.
Basic timing	0 ns		–	
NRZ signal	10 ns	T – 10 ns	–	
RZ signal (clock mode)	10 ns	T – Δt_W – 10 ns	145 pins or more: 10 ns 144 pins or less: 15 ns	T – Δt_D – 15 ns

Remarks 1. NRZ (Non-Return to Zero) signal: Indicates there is only one change within one test pattern (1 test rate).

2. RZ (Return to Zero) signal: A signal with a change of 0 → 1 → 0 or 1 → 0 → 1 within one test pattern.

Figure 8-1. Timing Phase



Cautions 1. At least 10 ns must remain between changes of each signal.

2. RZ signal input to bidirectional pins is prohibited.

Remark T: Test period (test rate)

The clock mode (RZ) signal of the input has two polarities, which determine how it is used.

Table 8-6. Clock Mode

Input Pattern	Definition	Operation	
		Positive Clock (P)	Negative Clock (N)
1 (H)	Clock generation	0 → 1 → 0(positive clock generation)	1 → 0 → 1(negative clock generation)
0 (L)	Clock stop	0 hold	1 hold

8.3.5 Skew

When two or more input signals are changed at the same time during simulation, no skew occurs between input signals. With an LSI tester that is used to check the quality of products, however, the input signals do not change at exactly the same time because of a skew of several ns that exists between input pins, even if it is specified that the signals change at the same time. Consequently, even if no problem is found during simulation, the product may not pass a quality test because of the skew between pins.

Therefore, take the following measures so that the product will operate normally even if there is an input skew when generating a test pattern.

(1) Do not change a flip-flop's data input and clock at the same time

→ Instead, alternate by one pattern.

(2) Use a clock signal (RZ signal) and an input delay signal (NRZ signal).

→ Stagger the input.

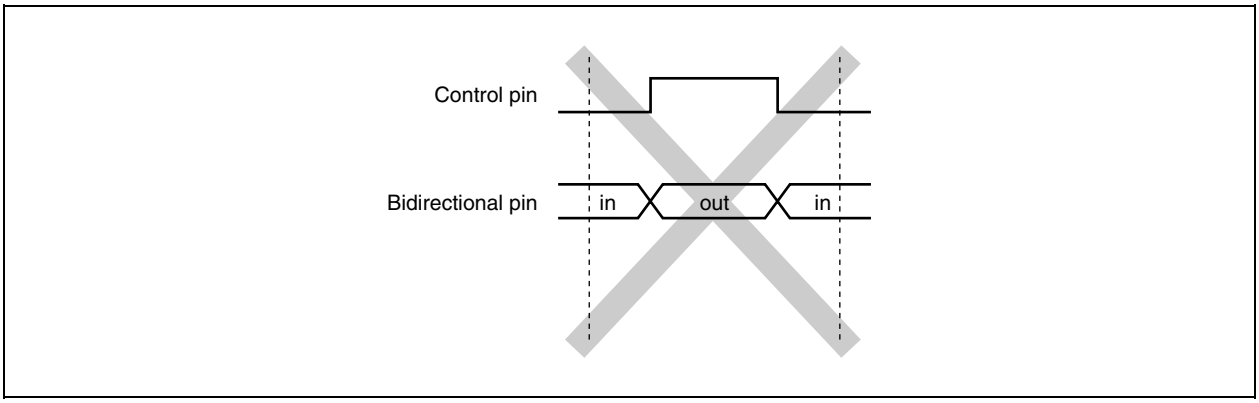
If it is assumed that the input skew is 10 ns and the setup time between data and clocks is 5 ns, then a 15 ns delay time is needed, as shown below.

LSI test input skew	+	Setup time	=	Input delay time specified to clock signal
10 ns	+	5 ns	=	15 ns

8.3.6 Notes on switching I/O mode of bidirectional pin

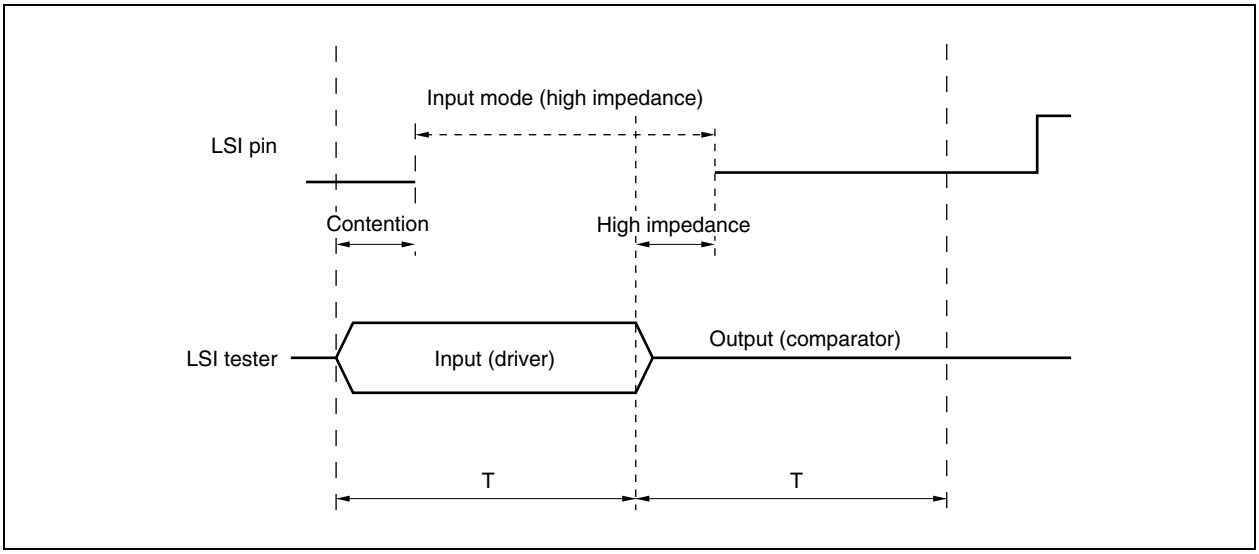
(1) Although the switching of the bidirectional pins' I/O mode is generally carried out at the basic timing, for the DC test pattern and function test pattern, it is possible to shift the I/O switch timing of a single set. This is known as the I/O modulation function (refer to **8.3.7 I/O modulation function** for details).
Note, however, that the bidirectional pin I/O mode cannot be switched using the RZ signal (because the mode will change twice within 1 rate: input → output → input. See Figure 8-2.)

Figure 8-2. Example of Incorrect Bidirectional Pin Switch Timing

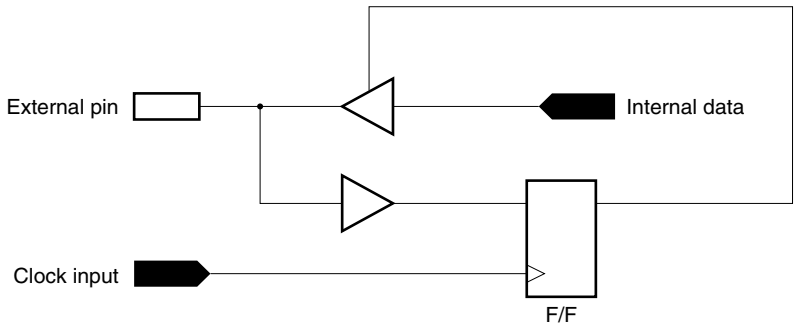


(2) In cases when an input delay has been added to the control pin in the bidirectional pin I/O mode, or when the I/O mode switch timing is different to the basic timing because there is a delay until the internal circuit is enabled, ensure that the input and output values match when switching the I/O mode. This processing prevents a current from flowing when the device's output signal conflicts with the LSI tester's driver (input), and is used to avoid power supply modulation or other such causes of malfunction. If it is not possible to match the input and output values, ensure that the conflict does not exceed 20 ns (see **8.3.8 I/O conflict**).
Note that it is prohibited to input the RZ signal (clock waveform) to a bidirectional pin.

Figure 8-3. Contention During Input/Output Switching

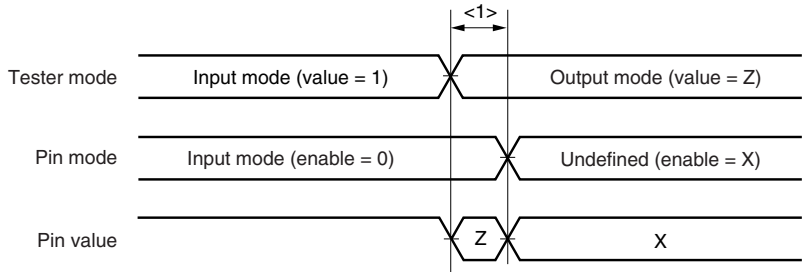


(3) Although the switching of the bidirectional pins' I/O mode is generally carried out at the basic timing, for the DC test pattern and function test pattern, it is possible to shift the I/O switch timing of a single set. This is known as the I/O modulation function (refer to **8.3.7 I/O modulation function**).

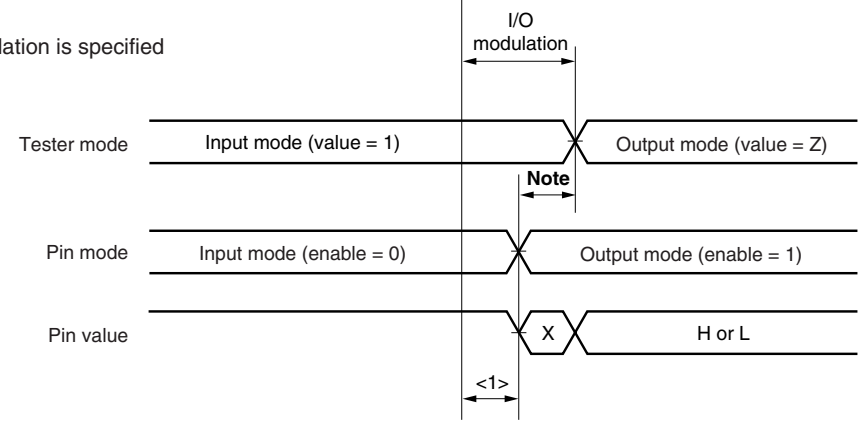


(a) Pattern example for PCI bus circuit I/O modulation

• When I/O modulation is not specified



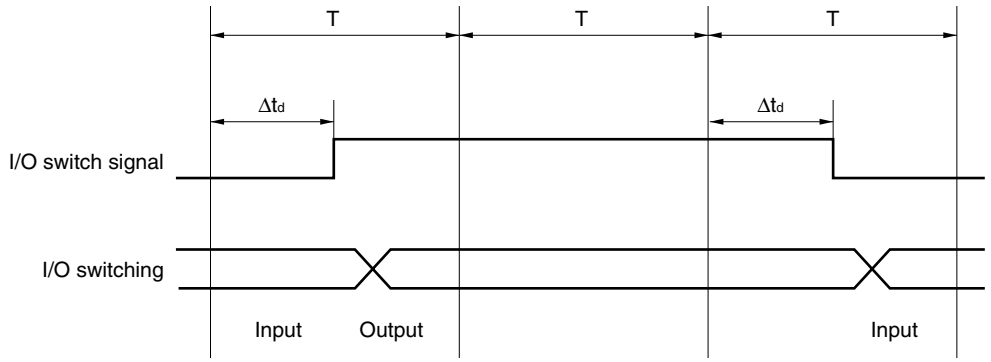
• When I/O modulation is specified



Note During this period, signals conflict. Be sure not to exceed the time limit.
Time limit: 5 ns ≤ Conflict ≤ 20 ns
During <1> (enable switching time)
When I/O modulation is not specified:
Floating occurs. Since pins become undefined (X) after that, testing cannot be performed correctly.
When I/O modulation is specified:
Since the tester remains in input mode, input mode value "1" is retained for pins. Due to that, the enable value becomes "1" after enable switching, and switching can be performed correctly.

8.3.7 I/O modulation function

Although in the case of the DC test pattern and function test pattern it is possible to shift the I/O switch timing of a single set, the following restrictions apply.



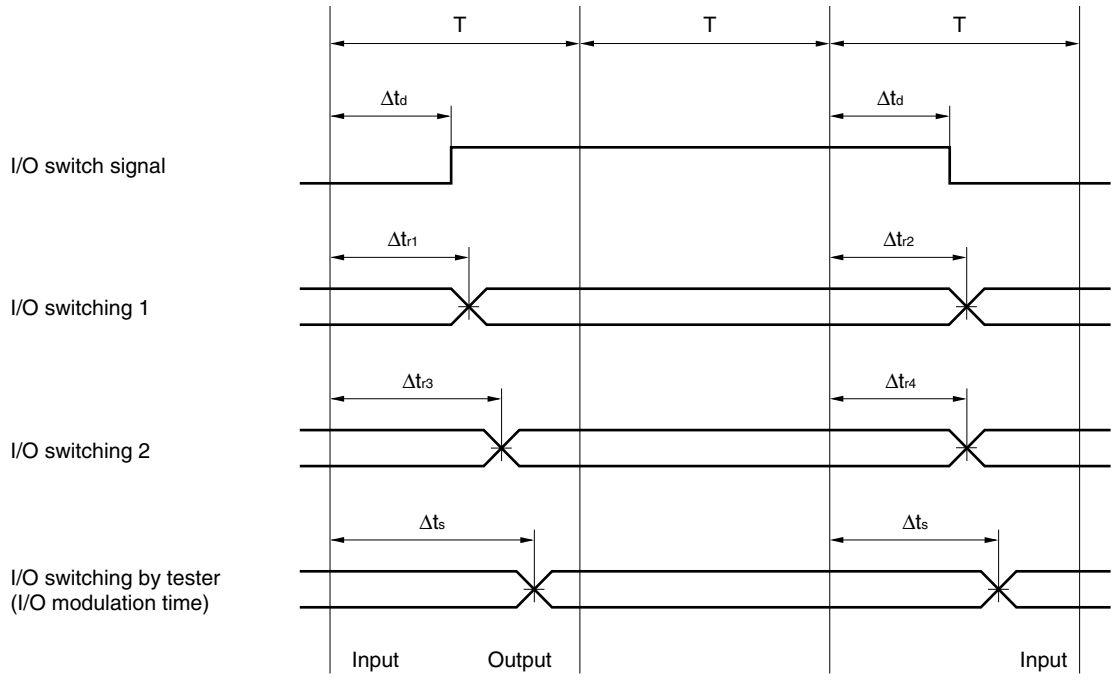
Remark T: Pattern period
Δt_d: Input delay of I/O switch signal

When shifting the I/O switch timing from the basic timing, the I/O switch time on the tester side is set as the I/O modulation.

The following expression must be satisfied, assuming Δt_{rmax} is the slowest time of all the pins and patterns among the bidirectional pin (simulation result) I/O switch times, and Δt_s is the I/O modulation time.

$\Delta t_s \geq \Delta t_{rmax} + 5$ ns

The reason for this is that in cases when the bidirectional mode is switched after the pre-switching value is fetched inside circuits such as a PCI bus circuit, because it is necessary to hold the external (LSI tester) value until the pin's I/O mode has been switched, the circuit must be driven longer (I/O mode switching delayed longer) than in the simulation result: 5 ns of the skew between the LSI tester pins.



Remark T: Pattern period

Δt_d: Input delay of I/O switch signal

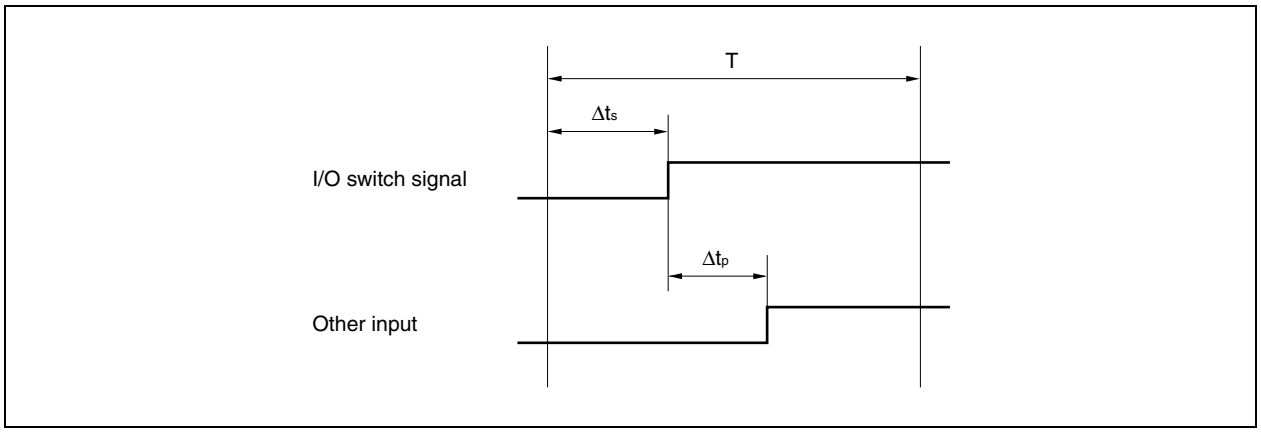
Δt_{r1} to Δt_{r4}: Bidirectional pins' I/O switch times

(Δt_{r3} in the above figure corresponds to Δt_{rmax} in the aforementioned equation.)

Δt_s: I/O modulation (I/O switching on the tester side) time

In addition to satisfying the above conditions, the following restrictions must be observed.

Item	I/O Modulation (Δt_s)		Interval Between I/O Modulation and Other Input Delay (Δt_p)
	MIN.	MAX.	MIN.
Restriction	10 ns	T – 10 ns	10 ns



When setting both the input delay (Δt_d) and I/O modulation (Δt_s) for the same pin, ensure that either of the following is satisfied:

$\Delta t_s = \Delta t_d$, or $\Delta t_s + 10$ ns $\leq \Delta t_d$.

Note that the I/O conflict time must be kept within 20 ns, even when using the I/O modulation function.
Also note that the I/O modulation function cannot be used in the high-speed function test.

8.3.8 I/O conflict

If it is not possible to match the bidirectional pins' input and output values, the I/O conflict must not exceed 20 ns.
The reference for judging I/O conflict is shown below.

Simulation Result	Expected Value	
	Input	Mode Undefined
Output 1	0, X	0, X
Output 0	1, X	1, X
Output X	0, 1, X	0, 1, X, Z

8.3.9 Testing multifunction I/O circuits

(1) Oscillators

Oscillators cannot be actually oscillated and tested with a simulator and LSI tester. Input a dummy signal to the input pin of the oscillator.

Use the inverted signal of the input signal as the expected value of the output of the oscillator.

The oscillator input signal is equivalent to the clock signal. Because a stable test cannot be performed due to conflict if this input signal and external data or set/reset input signals are changed at the same timing, be sure to stagger the timing.

Because the test pattern is not modeled in an oscillating state, the external timing of data or reset signals related to the clock in an oscillating state (oscillator input signals) is not tested.

(2) Open-drain output

The expected output value in the case of output disable must be high impedance (Z).

8.4 Notes on Generating DC Test Patterns

Restrictions for DC test patterns are basically same as those for function test patterns. The test pattern is not only used to test the functions but also used to test DC characteristics during shipment inspection. Therefore, the following points must be noted in generating a test pattern.

<1> If possible, prepare a dedicated test pattern set for the DC test pattern.

<2> The length of the DC test pattern should be more than 150 patterns. If the length of the pattern exceeds 32,000, perform the DC test between 1st and 32000th pattern.

<3> If possible, make input pins change at least two times (except for oscillation stop control pin).

<4> Output pins must output a high level and a low level at least once each.

<5> The output pin of a 3-state output buffer must output a high-impedance state (off state).

<6> When a bidirectional buffer is used, make sure that the input state and output state are switched at least once.

<7> Although the basic test period is 200 ns, set the test period to be sufficiently longer than the delay time (operating time) of the circuit.
Be sure to set the output determination time (strobe time) towards the end of the cycle (this is so the output is determined after the circuit has entered the stable state).

<8> If an RZ (Return to Zero) signal is input to an input pin, make sure that the RZ signal is not output as is. The output value of the output pin that outputs the RZ signal is always either one of two values at output determination time, and the other value cannot be tested.

<9> Bus fighting and bus floating for the internal bus is prohibited.

<10> Initialize the circuit until 50th pattern.

<11> The IDDq test is performed in the DC measurement pattern. The measurement pattern is selected automatically. If possible, operate the internal circuit to improve coverage.

<12> Be sure to set to oscillation mode when an oscillator block is mounted.

<13> In the test pattern in oscillation mode, input the same pattern as normal clock pattern for the input pin (XT1) and expected value of output pin (XT2) should be its inverse.

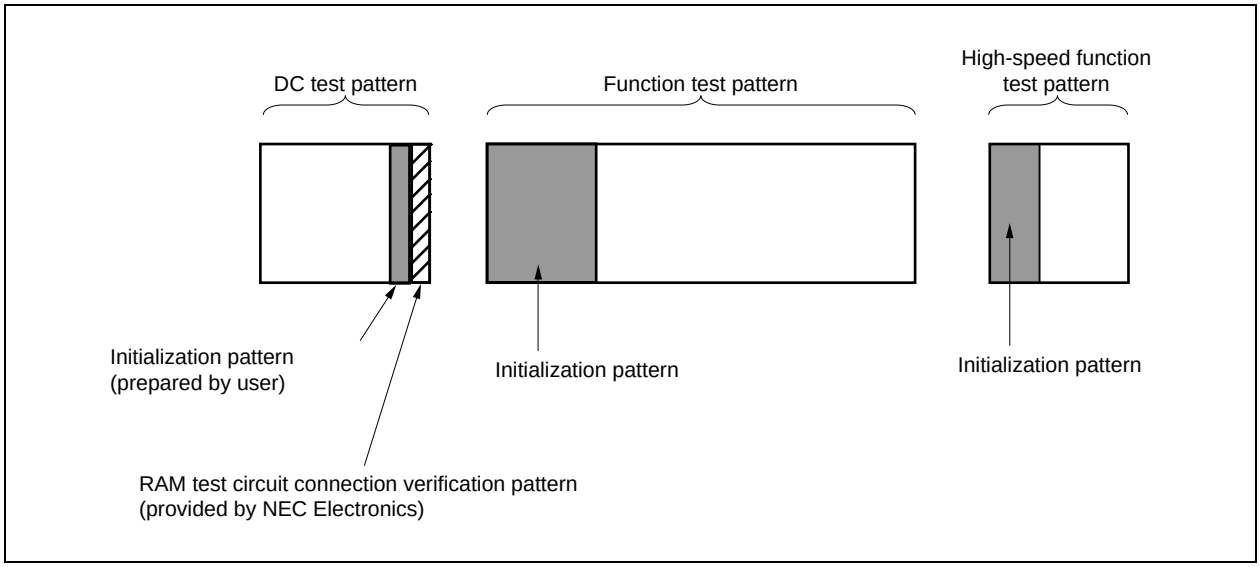
The RZ signal has changes of “0 → 1 → 0” and “1 → 0 → 1” in one test pattern (1 test rate). By contrast, the NRZ signal has only one change in one test pattern (1 test rate).

8.5 Test Pattern for Incorporating RAM

NEC Electronics supplies a test pattern for RAM, and the user does not have to consider RAM tests. However, the following limitations are applied if NEC Electronics supplies the test pattern for RAM. (For details, see **9.11 Memory**).

(1) Additional RAM pins (TIN, TEB, and TOUT) are needed in order to test the RAM.
(2) If there are multiple RAMs or connections between RAM and logic circuits, the connection to each RAM must be tested by the user test patterns.
(3) Be sure to set the TEB pin to user mode (high) for each of the user test patterns.

Figure 8-4. Test Pattern Example



8.6 Test Patterns for Separate Testing of User Logic

- These test patterns are required when the target chip includes a CPU or CPU peripheral macro and a user logic function block.
- These test patterns are used to separate the user logic part from the other cores (CPU and CPU peripheral) to verify the operation.
- If the target chip includes a ROM macro or a RAM macro, these test patterns should include a test pattern to access that macro.
  Note with caution that a dummy model[Note] is normally used for separate simulation of user logic when the target chip includes a CPU or CPU peripheral core, so the core cannot be accessed.

  Note Before starting simulation, you may choose between using a dummy model or a full function model, but a dummy macro is selected when user macro simulation has been specified. A dummy macro is a simple model created to check a macro's I/O connections; it is not the macro's original operation model.

- These test patterns are used for shipment inspections.

8.7 Test Patterns for Separate Test Circuit Verification of Cores

(1) Test patterns for reading ROM macro code data

- These test patterns are required only when the target chip includes a ROM macro.
- These test patterns are used to verify the ROM code by directly reading all ROM code from the ROM macro while in separate test mode.
- These test patterns are used for shipment inspections.

(2) Test pattern for built-in RAM

NEC Electronics supplies a test pattern for RAM, and the user does not have to consider RAM tests. However, the following limitations are applied if NEC Electronics supplies the test pattern for RAM. (For details, refer to **9.11 Memory**).

- Additional RAM test pins (TIN, TEB, and TOUT) are needed in order to test the RAM.
- Be sure to make the user mode of the TEB pin high at the first pattern of each test pattern.
- Eight test patterns for inspecting the connection with the RAM test circuit must be inserted following the test patterns for the DC test. Also, a correct test circuit connection must be verified.
- If there are multiple RAMs or connections between RAM and logic circuits, the connection to each RAM must be tested by the user test patterns.
- Consult NEC Electronics when using the BIST circuit together with a test bus.

(3) Test patterns for separate test circuit verification of CPU or CPU peripheral macro

- These test patterns are required only when the target chip includes a CPU or CPU peripheral macro.
- Before starting simulation, choose a dummy model[Note] for the CPU or CPU peripheral macro, then set separate test mode for each macro and perform a simulation using the test patterns for separate test verification that are provided by NEC Electronics. Afterward, check for errors.
  The test mode settings and the correspondences between the core pins and the external pins while in test mode should be submitted to NEC Electronics.

  Note Before starting simulation, you may choose between using a dummy model or a full function model. A dummy macro is a simple model created to check a macro's I/O connections; it is not the macro's original operation model. A dummy model is normally used, except when performing a total chip simulation.

- These test patterns are used to verify whether or not cores are efficiently connected to the separate test circuit. To enable confirmation, the simulation pattern for verification of the test circuit should be submitted to NEC Electronics along with a simulation run log. Also, during shipment inspections, the same function test pattern that is used for NEC Electronics' standard devices is used to verify operations.

8.8 Test Patterns for Total Chip Simulations

(1) If the target chip does not include a CPU or if there is no simulation that operates the CPU using an assembler program

- These test patterns activate the entire chip (in actual operation mode) and verify various functions. If the chip includes a CPU peripheral macro, generate these test patterns to verify mutual connections between cores and user logic.
- These test patterns are used in shipment inspections.

(2) If performing total chip simulation in which the CPU is operated using an assembler program

> Although total chip simulation that includes testing the CPU is required for function verification, it is difficult to generate test patterns that completely avoid conflicts among input patterns, so the customer must determine whether or not such conflicts are reflected in the LSI tester.
> In some cases, application of these test patterns may be delayed since pattern conflicts that are reflected in the tester may not be resolved completely and timing adjustments may be needed in the tester. NEC Electronics asks for your cooperation in providing information required for such timing adjustments.

The operation of core blocks can be verified by using the test patterns provided by NEC Electronics to test the megafunction blocks, and user logic blocks can be verified via user logic simulations. Consequently, this combination provides adequate confirmation of testability and therefore the results need not be reflected in a tester.

[Test patterns to be used when using a tester]

- These test patterns activate the entire chip (in actual operation mode) and verify only the connections between macros and between macros and user logic.
- Generate test patterns via the following steps.

  <1> Perform simulations via an assembler program, using the gate array circuit diagram as well as the added ROM and RAM macros.

  <2> Extract a test pattern from the start of the gate array chip circuit diagram, make skew adjustments, etc., make sure the test pattern avoids input pattern conflicts, and then perform another simulation of the gate array as a discrete device. Next, eliminate any remaining pattern conflict and submit the test pattern to NEC Electronics.

The flow of creating total chip simulation patterns for interface uses is shown in Figure 8-5.

- Pattern conflict causes and countermeasures
  When the test pattern of a single gate array is extracted, there is a possibility of pattern conflict due to normalization of the detailed skew timing.
  As a countermeasure to prevent pattern conflict, a skew setting that takes the tester's setting restrictions into account is needed. For details of these setting restrictions for input skew, etc., refer to **8.3 Notes on Generating Test Pattern for Function Test**.

<Reference>

When using external memory for a total chip simulation, note that the following signals entail a high risk of generating pattern conflict when test patterns of an gate array are used.

- Memory addresses, CSB and OEB signals, and read data input during memory read operation

  ↓

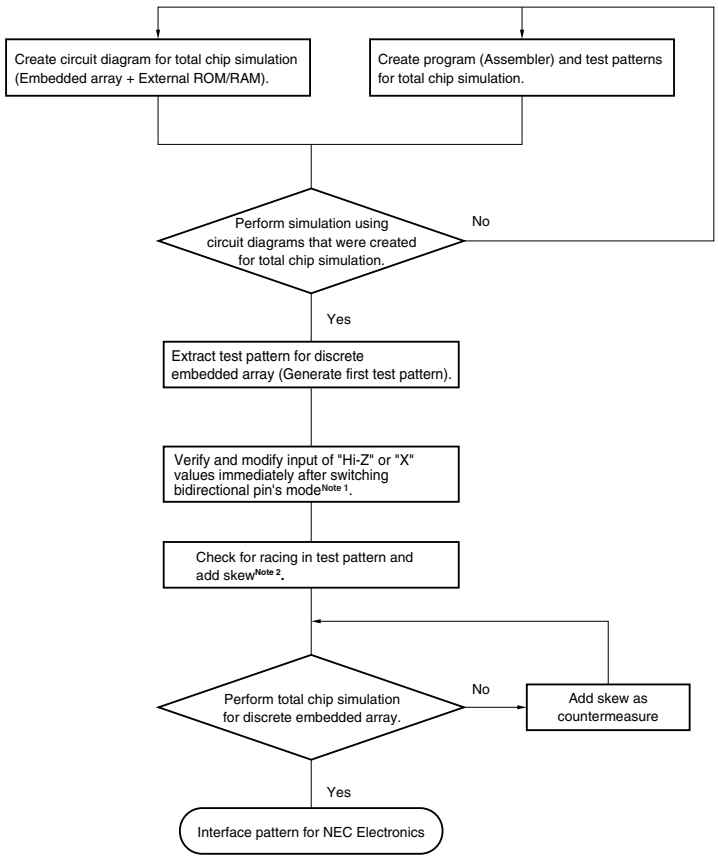
  Skew can be added to the read data as a countermeasure.
  Since the same model is used for external memory and internal memory, this could be due to an access time that is too short.

- We recommend using an RZ signal as the clock signal to avoid conflict between clock and data signals and to reduce the number of test patterns.

[When used only for function verification simulations]

These test patterns activate the entire chip (in actual operation mode) and verify various functions. An assembler program is used to perform the simulation. Since the results are not reflected in the tester, there is no need to perform a simulation specifically for gate array to check for input pattern conflicts.

Figure 8-5. Flow for Generating Total Chip Simulation Patterns



Notes 1. Immediately after switching from output mode to input mode, if a “Hi-Z” or “X” status exists, enter the same value (“1” or “0”) that appears in the output pattern that is one pattern before the pattern where the output-input mode switch occurred.

2. Note that there are restrictions related to skew settings. For details of these restrictions, refer to **8.3 Notes on Generating Test Pattern for Function Test**.

8.9 High-Speed Function Test (Real-Time Test)

Checking the designed circuit through simulation at the actual operating frequency is a very effective technique for checking the actual operation of the LSI. In this way, problems concerning the timing of the circuit during actual operation that may have been overlooked by the designer can be found.

During the shipment inspection of the product, the actual operating conditions cannot be always simulated because the performance of the LSI tester may be limited. The high-speed function test, however, can simulate conditions very close to the actual operating conditions.

This section describes the following limits of the high-speed function test. Generate a test pattern observing these limits.

8.9.1 Limitation of the test pattern length

The length per test pattern must consist of 32,000 patterns MAX.

8.9.2 Test period (test rate)

The test rate is referred to as the period of one test pattern.

Currently, the test rate limitation at NEC Electronics for a general high-speed function test is as follows:

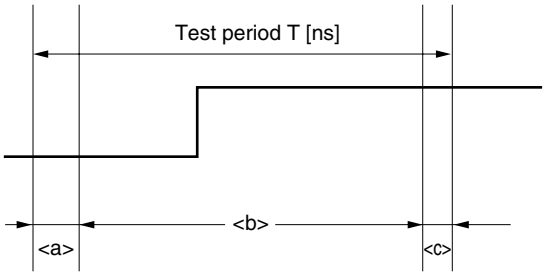
Test period: 50 ns MIN.

8.9.3 Output determination time (strobe time)

The output determination time (strobe time) indicates the time required to verify the output value of the product against the expected value on the test pattern. Currently, up to two strobe times can be assigned per test pattern. However, only one strobe time can be assigned per pin. If three or more strobe times or several strobe times per pin must be established, each one must have its own test pattern.

Setting strobe time within 15 ns the beginning of the basic timing or with 10 ns before the end of the timing is prohibited.

Figure 8-6. Strobe Time



<a> <b> <c>

15 ns ≤ strobe time ≤ T – 10 ns

Caution Open-drain, GTL+, and HSTL buffers are not real-time test targets.

8.9.4 Notes on high-speed function testing

To conduct the high-speed function test, execute MIN./MAX. simulations under the following conditions. The results of both the simulations must match.

Confirm these simulations before and after placement and routing.

Note with caution that I/O modulation cannot be used.

> Ask NEC Electronics for the delay data (path delay file) after placement and routing.
> At this time, the load capacitance data file (DIF FILE) for the output pins used for simulation is necessary. Submit this file to NEC Electronics.
> For the format of the DIF file, see **APPENDIX C ALBATROSS AND DIF FILE FORMATS**.

The purpose of these simulations is to detect the possibility of occurrence of problems when inspection is performed with an LSI tester. Therefore, conditions different from the actual operating conditions must sometimes be set.

Specify settings of the time condition for input signals, the output determination time (strobe time), and the test period (test rate) for each phase in “High-speed function test guidelines”.

<1> MAX. simulation conditions

Test period (T):	User-specified value
Load capacitance (C_L):	Bidirectional pin: 125 pF, MAX. value of load capacitance with LSI tester Output pin: 90 pF
Strobe time:	Set to specified value –5 ns with skew of strobe time assumed to be –5 ns

<2> MIN. simulation conditions

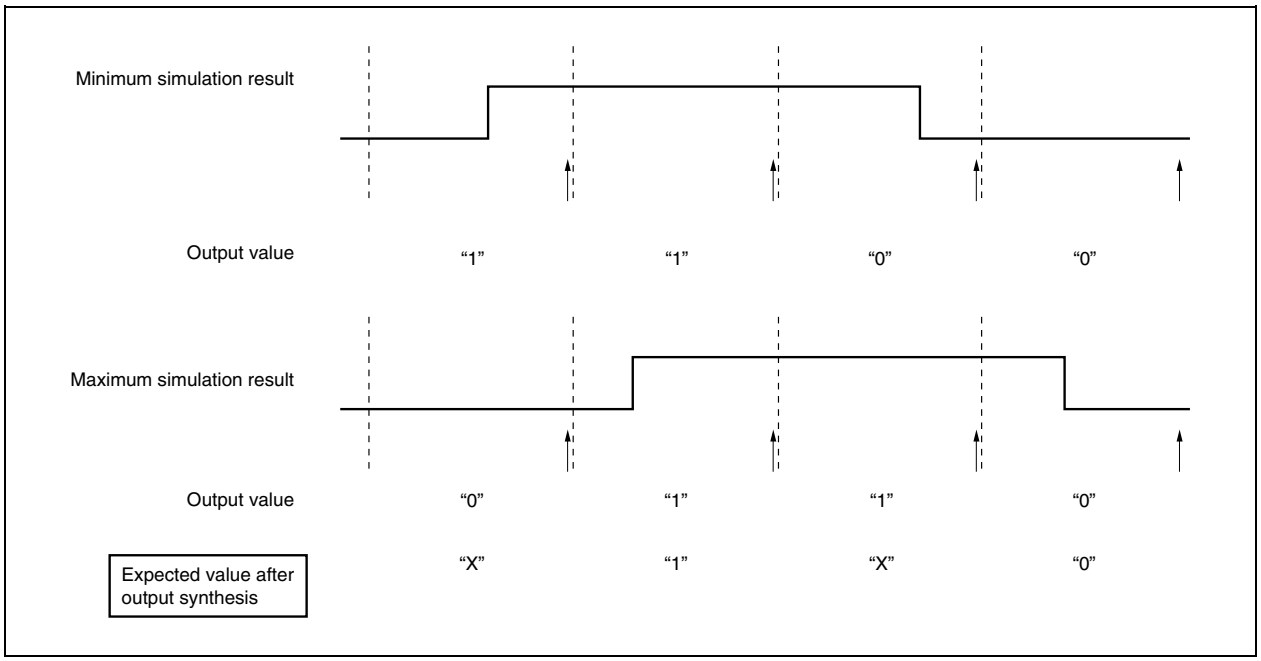
Test period (T):	User-specified value
Load capacitance (C_L):	60 pF, MIN. value of load capacitance with LSI tester
Strobe time:	Set to specified value +5 ns with skew of strobe time assumed to be +5 ns

During real-time simulation, the simulation result may not converge in one pattern and the output may change at the next pattern, as shown in Figure 8-7.

If the simulation result is different between the MAX. simulation and MIN. simulation, take the following measures:

- Change the expected output value of the test pattern, which differs between the two test patterns, to “X” (Don’t care). Synthesize the test patterns (see **Figure 8-7**).
- Alternatively, include only the timing actually requiring inspection as the system, as the expected values.

Figure 8-7. Real-Time Simulation Results



8.10 Testability (Fault Coverage)

8.10.1 Consideration of testability (fault coverage)

Fault simulation is a way to verify the testability (fault coverage) when an ASIC is developed. In other words, it diagnoses the validity of a test pattern generated to test the functions of logic circuits and detects the faults that are not detected by that test pattern.

During the ASIC manufacturing process, various faults may arise. These faults are broadly classified into dynamic faults and static faults.

Dynamic faults create long delay paths, spikes, and timing violations. Such faults are caused by the operating environment or design errors.

Static faults are represented by physical damage to the chip such as routing shorts and opens. In most of the cases, the production process is responsible for these faults. Logic simulation verifies the functions and timing of a created circuit. However, it does not verify the test efficiency of a test pattern for detecting static faults in the chip actually produced. Fault simulation defines static faults in the circuit and verifies whether faults have been accurately detected by the input test pattern from the output pins of the ASIC developed.

The purpose of fault simulation is to inspect how efficiently test patterns can detect a fault at the boundary of the function blocks of the created circuit. The test efficiency of these test patterns is called testability (fault coverage) and is expressed as a percentage to indicate how well the test patterns can detect the faults in the circuit.

$$\text{Testability (fault coverage)} = \frac{\text{Number of faults detectable by given test input pattern}}{\text{Total number of faults in circuit tested}} \times 100\ (\%)$$

If the testability (fault coverage) is low, the LSI may not be tested well and defective products may be shipped.

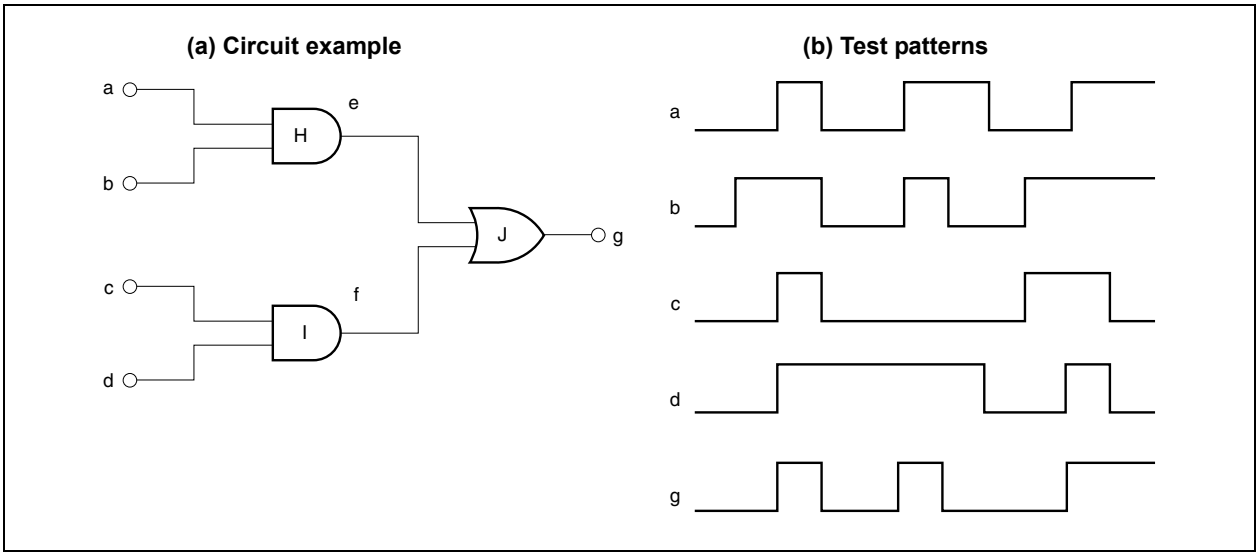
NEC Electronics recommends that the fault coverage, as far as possible, be made at least 90% in order to raise the quality of the product.

To improve testability (fault coverage), it is recommended to provide a test circuit at the circuit design stage and to employ the scan path test method.

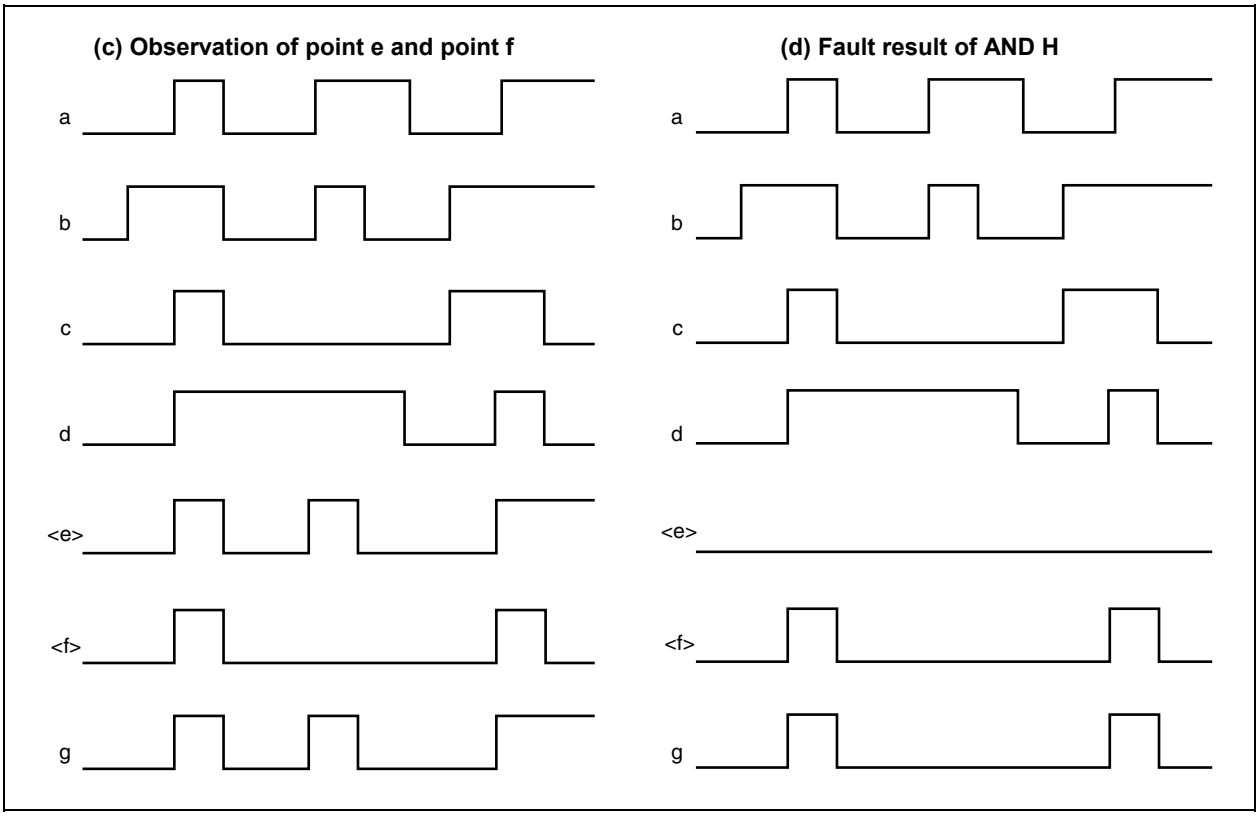
8.10.2 Principle of fault simulation

Fault simulation generally operates by the same algorithm as the logic simulation that tests the logical functions. In the execution of fault simulation, however, the faults can be set in the circuit. Figure 8-8 shows examples of fault simulation.

Figure 8-8. Concept of Fault Simulation (1/2)



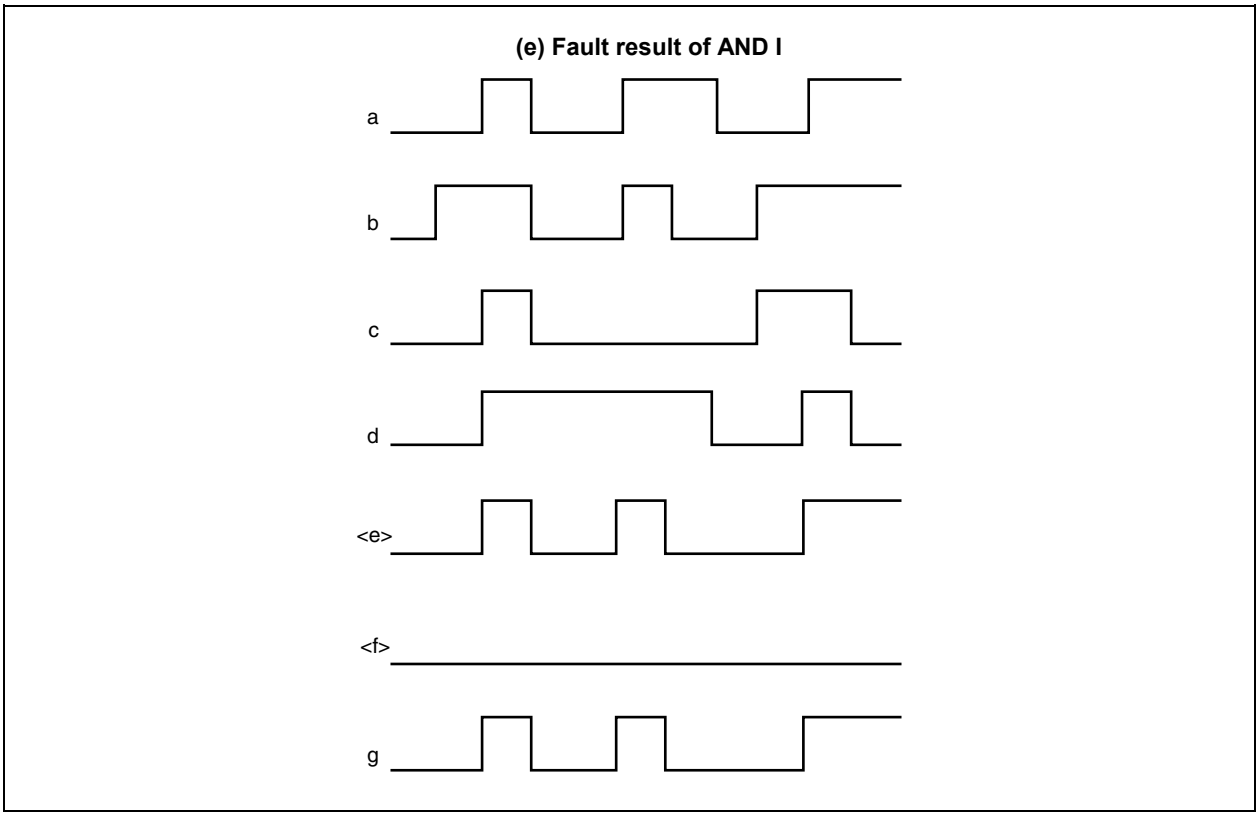
It is assumed that this circuit has a fault and that the output of the 2-input AND gate H is always at the low level. If an input signal the same as Figure 8-8 (c) is input in this case, it can be seen that the result of output “g” will be different (see **Figure 8-8 (c)** and **(d)**). Accordingly, this fault can be detected by these test patterns.



There may also be cases of a fault in which the output of the 2-input AND gate I is always at the low level.

As shown in Figure 8-8 (e), this input signal (test pattern) becomes the same as the test pattern in Figure 8-8 (c), which shows that they are ineffective in detecting this fault.

Figure 8-8. Concept of Fault Simulation (2/2)



Fault simulation defines these types of faults one by one with respect to the internal circuit and checks whether the defined faults can be detected at the output pin by performing simulation.

The types of faults that can generally be defined by fault simulation are called single degenerate faults.

The following two types of single degenerate faults are defined in circuits:

<1> Stuck-at-1: Fault where a given part is fixed at the high level (“1”)

<2> Stuck-at-0: Fault where a given part is fixed at the low level (“0”)

CHAPTER 9 MULTI-FUNCTION BLOCKS

The EP-1 series offers the following multifunction blocks, in addition to the normal function blocks. This chapter explains the functions and usage of each multifunction block.

- LVTTL and 5 V tolerant blocks, 5 V full-swing buffer
- Buffer with on-chip pull-up/pull-down resistors
- Clock driver
- GTL+
- Digital PLL
- Memory block
- Compiled memory
- Megamacros

9.1 LVTTL and 5 V Tolerant Blocks, 5 V Full-Swing Buffer

The EP-1 series offers the following interface blocks.
This section describes the features of each block. For the name of each block, consult NEC Electronics.

Input blocks
- LVTTL input block
- LVTTL input block (with fail-safe function)
- 5 V tolerant input block
- 5 V full-swing input buffer

Output blocks
- LVTTL output block
- TTL 5 V tolerant output block
- CMOS 5 V tolerant output block
- 5 V full-swing output buffer

Use low noise type for 18mA/24mA-buffers.

9.1.1 Input buffers

The LVTTL input block receives 3.3 V signals only; it cannot receive 5 V signals. A 5 V signal is received by a 5 V tolerant input block which can also receive 3.3 V signals. Therefore, note that the input characteristics (V_{IL} and V_{IH}) comply with the LVTTL standard.

A normal input buffer is provided with a protection diode. When an input voltage is applied while the power supply is turned off, therefore, a leakage current occurs and may cause a failure. The LVTTL input block with a fail-safe function can apply the input voltage to the input block even when the supply voltage is off. It can therefore be used for hot insertion and removal as long as the specified static voltage condition is satisfied.

Figure 9-1. Equivalent Circuit Diagrams for LVTTL Input and TTL 5 V Tolerant Input Buffers

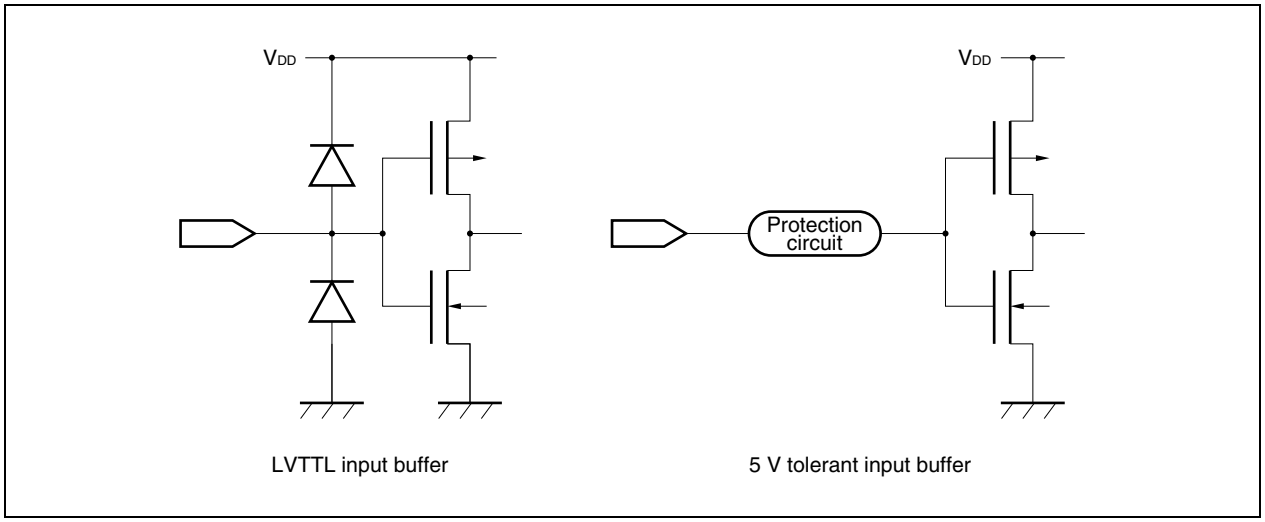
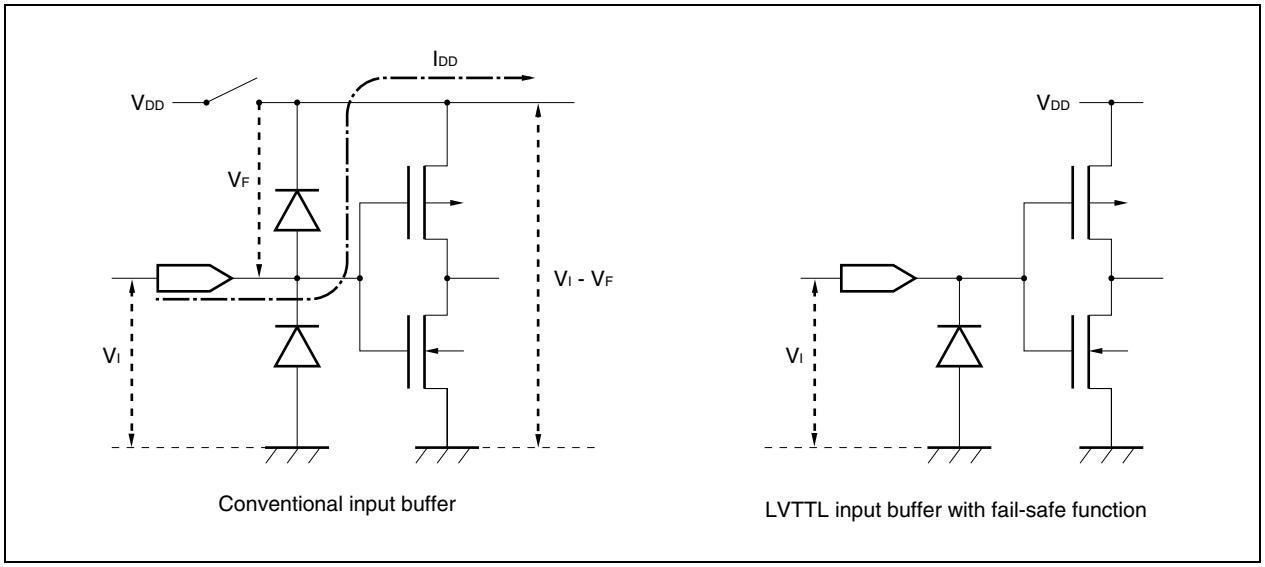


Figure 9-2. Equivalent Circuit Diagram for LVTTL Input Buffer with Fail-Safe Function



9.1.2 Output buffers

The EP-1 series offers TTL 5 V tolerant output blocks and 5 V full-swing output buffers in addition to the LVTTL output blocks.

<1> TTL 5 V tolerant output buffer

This buffer is used when the LSI at the next stage is of 5V TTL logic. The output level is also compatible with a LVTTL output buffer. The TTL 5 V output buffer, however, has a 5 V protection circuit, considering that connection with a 5 V line is necessary. This block can also be pulled up at 5 V.

However, the TTL 5 V tolerant output buffer allows a slight influx current to flow to the embedded array when the buffer is pulled up at 5 V. Therefore, the output signal may not rise to 5 V depending on the pull-up resistance. Please Count in drop the voltage for IR × RPU (see **5.1.2 Output influx current (I_R)**).

With a 3-state output buffer and bidirectional buffer, the off-state current slightly increases due to the bias voltage of the 5 V protection circuit when the 3-state circuit is in the off state.

<2> 5 V full-swing output buffer

There are two types of 5 V full-swing output buffers, CMOS 5 V output buffers and TTL output buffers. They can be connected to 5 V TTL and 5 V CMOS level LSI, respectively.

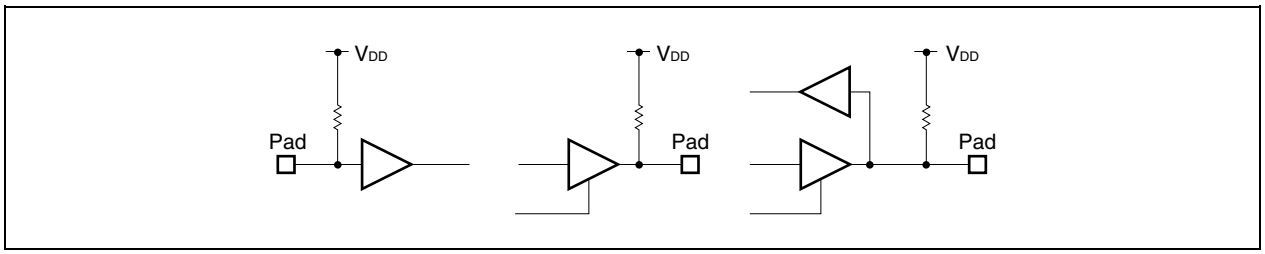
These buffers can be made to perform 5 V full-swing output by applying 5 V power supply to the LSI.

9.2 Input/Output/Bidirectional Buffers with On-Chip Pull-up/Pull-down Resistors

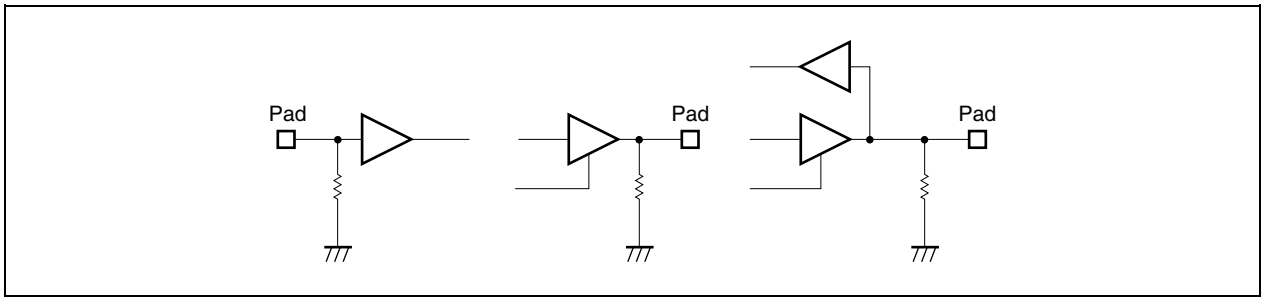
The EP-1 series has input buffers, Schmitt-input buffers, 3-state output buffers, P-ch open-drain output buffers, N-ch open-drain output buffers, bidirectional buffers, Schmitt-input bidirectional buffers, and I/O blocks with on-chip pull-up/pull-down resistors. By using these, a more compact system can be created.

For the name of each block, refer to **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

Pull-up resistor



Pull-down resistor



During simulation, undefined (X) or high-impedance (Z) values cannot be input to the input pins of the input buffers and bidirectional buffers with on-chip pull-up/pull-down resistors.

The expected output value must be set to “Hi-Z” (high-impedance) or “don’t care” when the output pins of 3-state output buffer and bidirectional buffers with on-chip pull-up/pull-down resistors are not active.

9.3 Clock Input Drivers (Reference)

Below is an introduction of EA-9HD local clock distribution methodology.

Generally, it is recommended 'clock tree synthesis' technique that minimizes clock skew between flip-flops that are connected to the clock line. (For details, see **6.4 Clock Line Design**.)

The clock signal input from an external source to the LSI must be supplied to the many on-chip flip-flops of the LSI, and the blocks used require the following features:

(1) High drive capability (fan-out)
(2) High-speed operation

Therefore, the EP-1 series offers the dedicated internal blocks listed in Table 9-1 to satisfy this requirement. These clock input driver-dedicated blocks have the following features:

(1) Fan-out: 82 to 83 per output pin
(2) Low dependency of propagation delay time on fan-out

Because a clock input driver-dedicated block requires a lot of wiring, only one can be used in the LSI, regardless of the type of the block.

If the limits of **Table 9-1 Clock Input Driver Dedicated Block** are to be exceeded, consult NEC Electronics.

Table 9-1. Clock Input Driver Dedicated Block

Block Name	Number of Allowable Fan-Outs	Number of Cells Used
FIB1	664	56
FDB1	664	56
FUB1	664	56
FWB1	664	56
FIH1	656	56
FDH1	656	56
FIG1	664	56
FDG1	664	56

9.4 Oscillator

9.4.1 Configuration of oscillator

Three types of oscillator blocks are available for configuring an oscillator: one using external feedback resistors, one with internal feedback resistors, and another with an oscillation stop function. Using any of these blocks, an oscillator can be configured simply by connecting a resonator, a capacitor, and limiting resistor to the external pins. However, only up to two oscillator-dedicated blocks can be used. When two blocks are used, one of them must be placed at the polarity opposite to the other to prevent mutual interference between the two, and each circuit must operate on a separate clock. Three or more oscillator blocks must not be used. If it is necessary to use more than one block, consult NEC Electronics.

Table 9-2 shows the recommended oscillation frequency range of the oscillator and the combination of blocks configuring the oscillator.

For the locations where the oscillation block can be placed, see **CHAPTER 11 PACKAGES**. When using the oscillator block with stop function, control stopping of the oscillator block from an external source. The stop control pin can be placed anywhere, but it should be placed as close to the oscillator block as possible.

For the oscillator block (OSBx), however, see **9.4.3 Notes on oscillator block (OSBx)**.

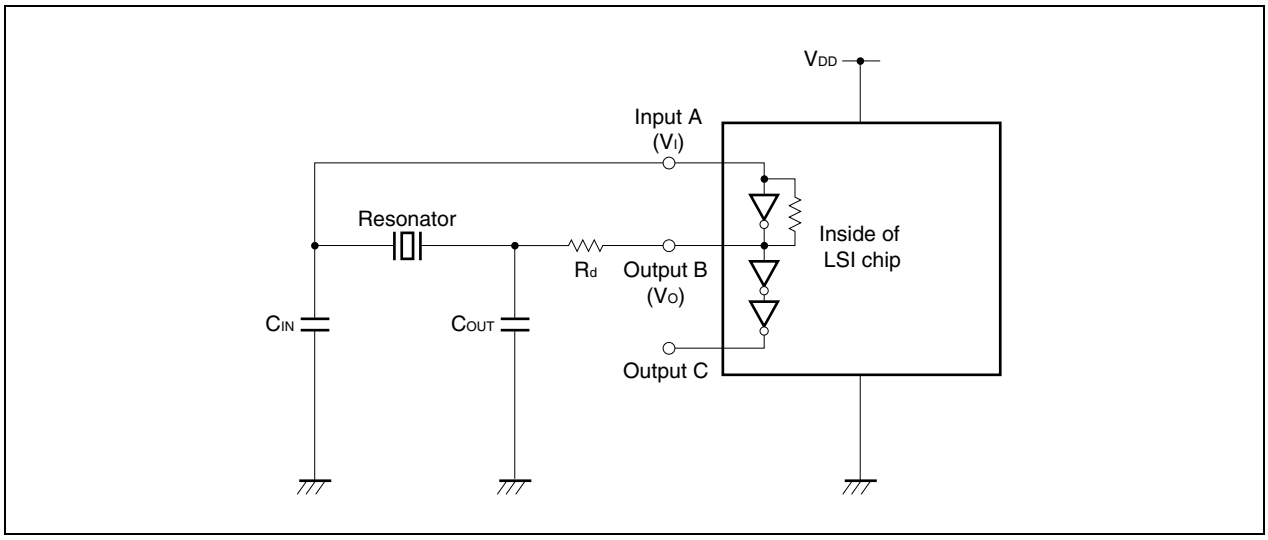
Table 9-2. Recommended Oscillation Frequency Range and Configuration

Feedback Resistor		Stop Function	Configuration		Frequency	Placement
			Input	Output		
External	1 MΩ	No	OSI1	OSO9	MHz band	Arbitrary
Internal		No	OSI1	OSO1	MHz band	Fixed
			OSI1	OSO3 (formerly OSO0)		
		Yes	OSI2	OSO7		
		Yes	OSBx		kHz to MHz band	Restricted[Note]

<R>

Note For the restrictions, see **9.4.3 Notes on oscillator block (OSBx)**.

Figure 9-3. Example of Oscillator Configuration



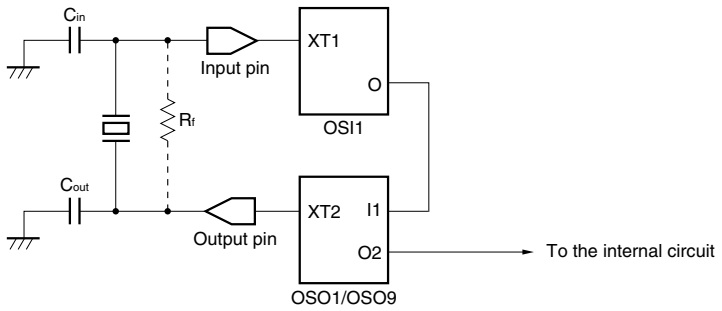
Remark To determine capacitors C_{IN} and C_{OUT}, limiting resistor R_d, and current consumption, evaluation is necessary with an evaluation sample (ES or CS).

9.4.2 Description of oscillator

Describe as follows when using an oscillator.

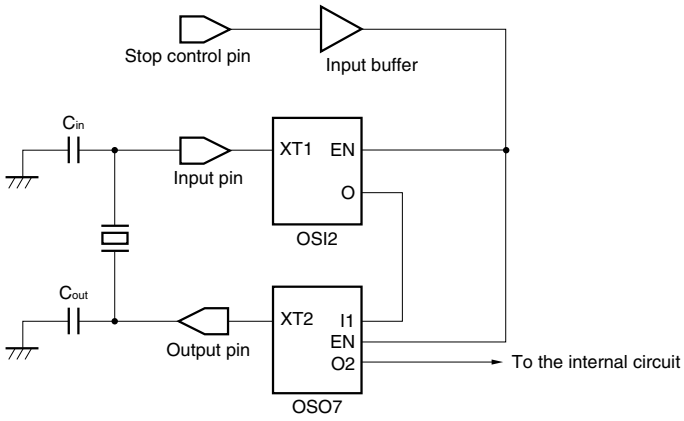
Figure 9-4. Oscillator Configuration (1/3)

(a) OSI1+OSO1, OSI1+OSO9



Remark When using OSO9, external feedback resistor Rf with a value of 1 MΩ or so is necessary.

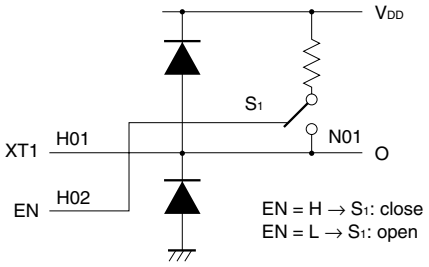
(b) OSI2+OSO7



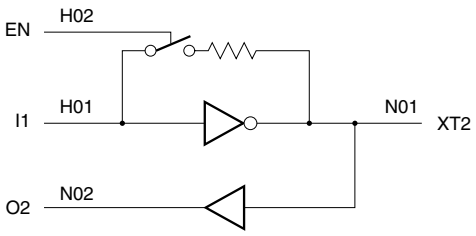
Remark The O2 output when oscillation is stopped is low level.

The equivalent circuits of OSI2 and OSO7 are shown below.

<1> OSI2 equivalent circuit



<2> OSO7 equivalent circuit



Truth table

XT1	EN	O
0	0	0
1	0	1
1	1	1
0	1	X

← Use prohibited

Truth table

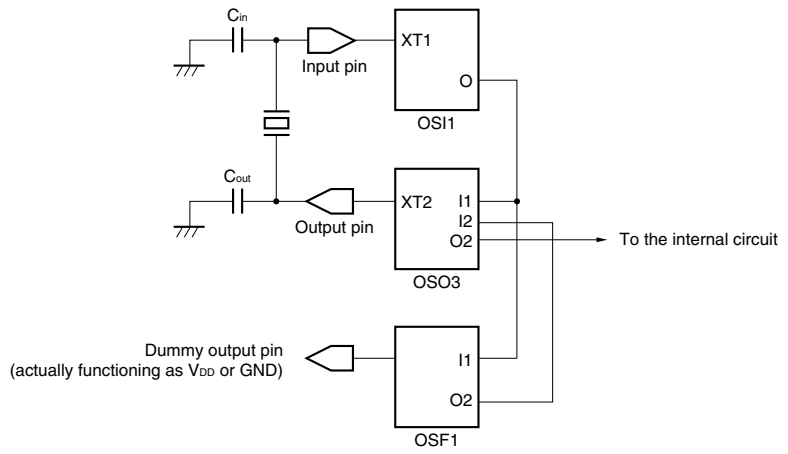
I1	EN	XT2	O2
0	0	1	1
1	0	0	0
1	1	0	0
0	1	X	X

← Use prohibited

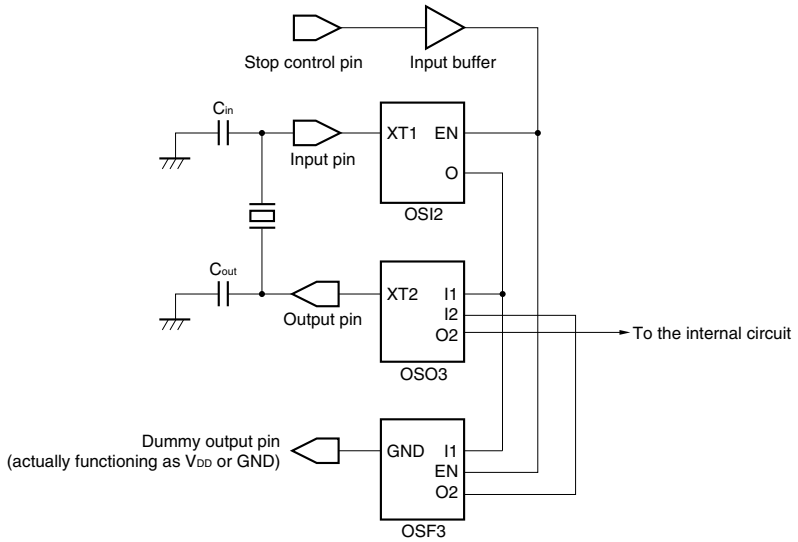
Caution When not connecting a resonator, fix the input pin (XT1) to the H level.

Figure 9-4. Oscillator Configuration (2/3)

(c) OSI1+OSO3+OSF1



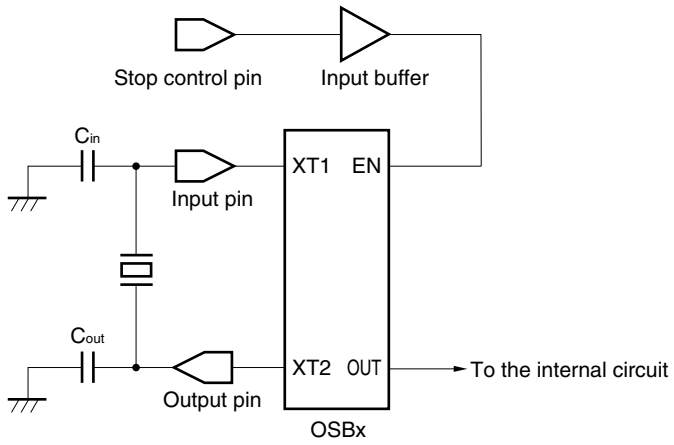
(d) OSI2+OSO3+OSF3



<R>

Figure 9-4. Oscillator Configuration (3/3)

(e) OSBx



Truth table

H01 (XT1)	H02 (EN)	N01 (OUT)	N02 (XT2)	
0	1	0	1	
1	1	1	0	
0	0	0	1	
1	0	0	X	← Use prohibited

Remark The OUT output when oscillation is stopped is low level.

Describe the test pattern of an oscillator as follows:

- Use the inverse of the pattern transmitted to the internal circuit as the input pattern of the input pins (XT1) of OSIx and OSBx.
- Use the same pattern as that transmitted to the internal circuit as the output pattern of the output pins (XT2) of OSOx and OSBx.
- Always input 0 to the stop control pins of OSO7 and OSBx in the DC test pattern.
- The output pins of OSF1 and OSF3 are dummy pins. The actual function of these pins is V_{DD} or GND, depending on the package.
  However, all the output patterns should be zero (low level), regardless of whether the dummy pin is GND or V_{DD}.

The pattern transmitted to the internal circuit and the pattern output to the output pins (XT2) of OSOx and OSBx are the inverted input pattern.

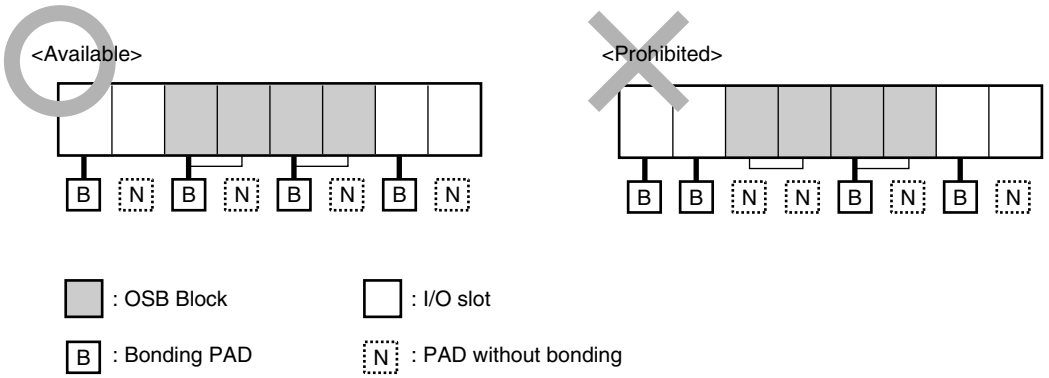
<R> 9.4.3 Notes on oscillator block (OSBx)

The oscillator block (OSBx) uses four I/O slots.

One pin is provided to the two I/O slots on the left and one pin is provided to the two I/O slots on the right. These pins are N02 and H01 pins, respectively.

Bear in mind the following points when placing the oscillator block.

- The four I/O slots cannot be separated from each other.
- The N02 pin is on the left and the H01 pin is on the right. These pins are not interchangeable.
- Place the two pins (N02 and H01 pins) at positions where they can be connected, on a pad that can be bonded.



When using the oscillator block, note the following points.

- When the stop function is not used, clamp the stop control signal so that an actual operation can be performed (EN = 1). Note, however, that a special request is needed.
- To use the stop function, be sure to provide a stop mode to a pattern created by the user.
- To set the stop mode (EN = 0) during simulation, be sure to give a low level to the external input pin (XT1), and make the expected value of the external output pin (XT2) high level.
- To control stopping of the oscillator block from the core, confirm each active level and do not use a wrong level.
- Design a circuit, taking the oscillation stabilization time when the stop function is canceled into consideration.
- Inserting a limiting resistor in series with the output side (XT2) is effective for lowering the unwanted radiation noise.

  To use the OSB3-OSBA, use an oscillator block with as low a gain as possible to lower the radiation noise.

9.4.4 Notes on configuring oscillator

Because the EP-1 series has an internal oscillator block, it can be used to configure an oscillator by connecting a resonator and constants outside the package. Although an oscillator can be easily configured, certain differences from logic circuits must be noted because an oscillator is an analog circuit that operates at a high frequency.

In order for the oscillator to operate stably, it is necessary to optimize the external constants (input capacitor, output capacitor, and limiting resistor). In addition, because the oscillator is an analog circuit, the following points must also be noted.

<1> Oscillator (oscillation circuit) pin placement is determined by package. For the placement, see **CHAPTER 11 PACKAGES**.

<2> Place the clock pin or reset pin, etc. as far away as possible from oscillator pins (oscillator) because these pins may cause a malfunction if noise occurs on them even momentarily.

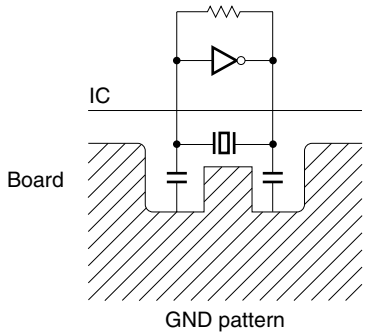
<3> Place the output buffer as far away as possible from oscillator pins (oscillator) because it is a source of noise.

<4> The following points must be noted for the printed circuit board.

- Place the input and output pins, and the resonator of the oscillator as closely as possible, and keep the length of the wiring between them as short as possible.
- Also keep the length of the wiring between the ground of the capacitors and the GND of the embedded array as short as possible. Use as thick a wiring line as possible.
- Keep the leads of the resonator and capacitors as short as possible. Secure the resonator and capacitors onto the printed circuit board to minimize the influence of mechanical vibration.
- As far as possible, enclose the external constants by GND patterns.

<5> To input the clock generated by an external oscillator from the input pins (OSI1, OSI2) of the oscillation block, perform connection to XIN (OSI1, OSI2) side and leave the XOUT (OSO1) side open. Also, since the oscillator is an inverter in logical terms, an inverted signal of input enters the internal circuit.

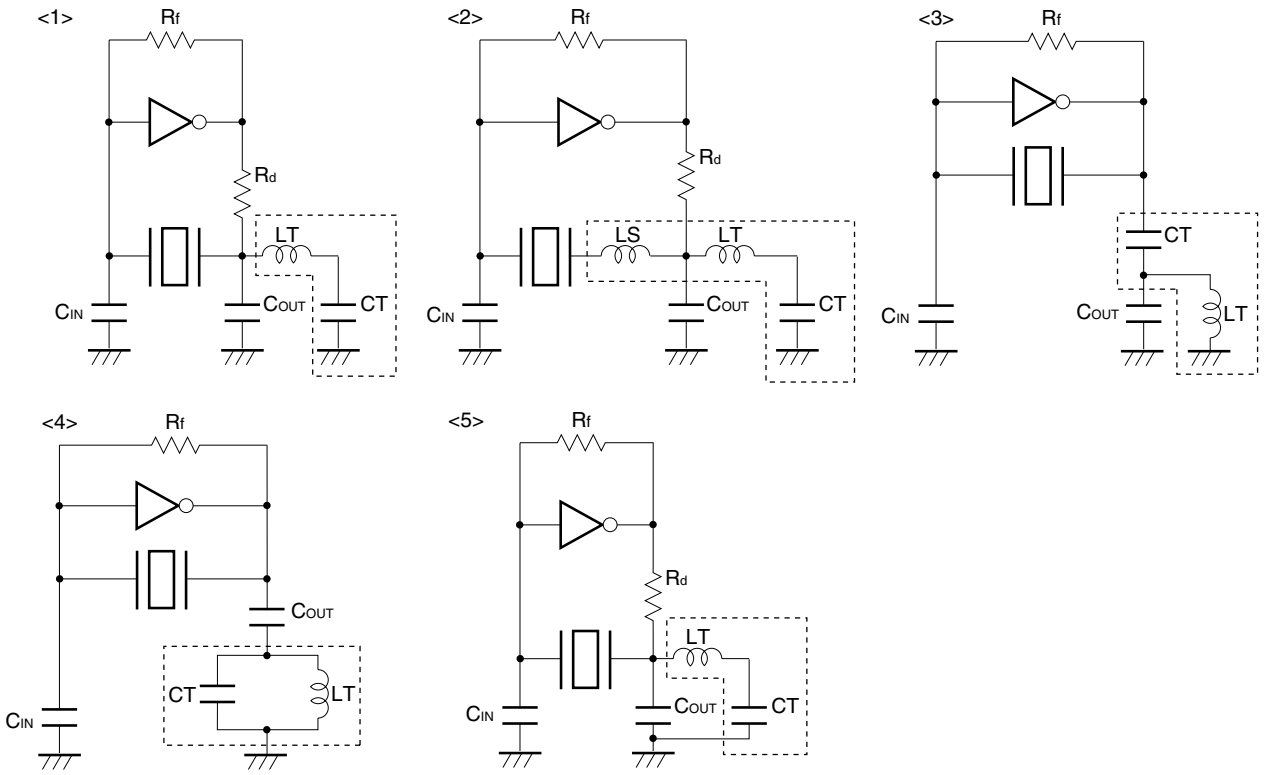
Figure 9-5. Example of GND Pattern on Board



The following points must be noted during evaluation to determine the external constants.

- Use the printed circuit board that is to be actually used (because the oscillation operation range may fluctuate due to the difference in the dielectric constant of the board).
- Check with the developed EP-1 series (ES or CS) and the resonator to be actually used.

Figure 9-6. Example of Overtone Circuit



Remark The dotted lines indicate the overtone circuit.

9.4.5 Constants of external circuit

To generate a clock signal, evaluation of matching with the resonator is necessary. Table 9-3 shows an example of criteria for this evaluation. Determine the parameters to be measured through consultation with the resonator manufacturer.

Table 9-3. Example of Criteria

Item	Criteria
<1> Oscillation frequency	Frequency must be within accuracy of resonator.
<2> Oscillation start voltage (V_s)	2.0 V or less
<3> Oscillation hold voltage (V_h)	$V_h \leq V_S$
<4> Operation on power application	Check oscillation by repeatedly turning ON/OFF power.
<5> Current consumption	As low as possible.
<6> Peak value of oscillated waveform	2.2 V ≤ V_{IH}, $V_{OH} \leq V_{DD}$ 0 V ≤ V_{IL}, $V_{OL} \leq$ 0.5 V
<7> Duty factor	50 ±10 %

Oscillation is evaluated with the ES or CS model. Because all the embedded array, resonator, and external constants are subject to variations due to production conditions and operating conditions, take these variations into consideration during evaluation.

To evaluate parameters <4> through <7> above, fluctuations in power supply and temperature must be also taken into consideration. Measure these parameters under the following MIN., TYP., and MAX. conditions.

Example When fluctuations in power supply and temperature are taken into consideration:
T_A = –40 to +85°C
V_{DD} = 3.3 V ±10%
Measure these parameters under the following MIN., TYP., and MAX. conditions.

	MIN	TYP	MAX
T_A(°C)	-40	25	+85
V_{DD}(V)	3.6	3.3	3.0

Remark The values in this table indicate the conditions of the MIN., TYP., and MAX. values of the propagation delay time (t_{PD}) of the embedded array, and do not refer to the MIN., TYP., and MAX. values of the resonator.

9.4.6 Resonators and circuit configuration

Table 9-4 lists the external resonators that can be added to the OSO7 (OSO1) and OSO9 and their recommended external constants. This data has been evaluated by the resonator manufacturers. For the frequency and external constants and circuit configuration other than those in the table, please contact to each manufacturer.

Table 9-4. Resonator Evaluation (1/2)

(a) 3.3 ±0.3 V

Material	Manu facturer	Frequency (MHz)	Part Number		Capacitor	Recommended External Constant		
			Old	New		C_{IN}(pF)	C_{OUT}(pF)	R_d(Ω)
Ceramic	TDK Corp.	16.93	FCR16.93M2G	-	External	5	5	330
		33.86	FCR33.86M2G	-		10	10	-
		4.00	FCR4.0MC5	-	Internal	-	-	3300
		8.00	FCR8.0MC5	-		-	-	1500
		50.80	FCR50.8M2G	-		-	-	-
	Murata Mfg. Co., Ltd.	25.00	CSALS25M0X53-B0	-	External	10	10	0
		25.00	CSACW2500MX01 Note1	CSACW25M0X51-R0 Note1		10	10	0
		33.86	CSALS33M8X51-B0	-		7	7	0
		50.00	CSALS50M0X51-B0	-		3	3	0
		50.00	CSACW5000MX01 Note1	CSACW50M0X51-R0 Note1		3	3	0
		60.00	CSA60.00MXZ040	-		Open	3	0
		2.00	CSTLS2M00G56-B0	-	Internal	-	-	1500
		2.00	CSTCC2.00MG0H6 Note1	CSTCC2M00G56-R0 Note1		-	-	1500
		4.00	CSTS0400MG06	CSTLS4M00G56-B0		-	-	680
		4.00	CSTCR4M00G55-R0 Note1	-		-	-	680
		8.00	CSTS0800MG06	CSTLS8M00G56-B0		-	-	220
		8.00	CSTCC8.00MG0H6 Note1	CSTCC8M00G56-R0 Note1		-	-	220
		16.00	CSTLS16M0X54-B0	-		-	-	0
		16.00	CSTCV16.00MXJ0C3 Note1	CSTCV16M0X53J-R0 Note1		-	-	0
		33.86	CSTCW3386MX01 Note1	CSTCW33M8X51-R0 Note1		-	-	0
		40.00	CSTLS40M0X51-B0	-		-	-	0
		40.00	CSTCW4000MX01 Note1	CSTCW40M0X51-R0 Note1		-	-	0
	Kyocera Corporation	4.00	PBRC4.00HR Note1	-	Internal	-	-	1500
		8.00	PBRC8.00HR Note1	-		-	-	0
		16.00	SSR16.00BR-MN1 Note1	-		-	-	0
		20.00	SSR20.00BR-H8S Note1	-		-	-	0
		33.86	SSR33.86 BR-ALP Note2	-		-	-	0
		48.00	SSR48.00 BR-AN05 Note3	-		-	-	0

Note 1. Surface mount type

2. Surface mount type. A 6.8 kΩ external feedback resistor is required for OSO7 (OSO1).

3. Surface mount type. A 4.7 kΩ external feedback resistor is required for OSO7 (OSO1).

Remark Oscillation environment: V_{DD} = 3.3 ±0.3 V, T_A = −40 to +85°C,
External feedback resistor of OSO9 = 1 MΩ

Table 9-4. Resonator Evaluation (2/2)

(b) 3.0 ±0.3 V

Material	Manu facturer	Frequency (MHz)	Part Number		Capacitor	Recommended External Constant		
			Old	New		C_{IN}(pF)	C_{OUT}(pF)	R_d(Ω)
Ceramic	Murata Mfg. Co., Ltd.	2.00	CSTCC2.00MG0H6 Note	CSTCC2M00G56-R0 Note	Internal	-	-	1500
		4.00	CSTCR4M00G55-R0 Note	-		-	-	680
		4.00	CSTS0400MG06	CSTLS4M00G56-B0		-	-	680
		8.00	CSTCE8M00G55-R0 Note	-		-	-	220
		8.00	CSTS0800MG06	CSTLS8M00G56-B0		-	-	220
		16.00	CSTCE16M0V53-R0 Note	-		-	-	100
		25.00	CSTCG25M0V51-R0 Note	-		-	-	100
		25.00	CSTCW2500MX01 Note	CSTCW25M0X51-R0 Note		-	-	0
		33.86	CSTCG33M8V53-R0 Note	-		-	-	68
		33.86	CSTCW3386MX01 Note	CSTCW33M8X51-R0 Note		-	-	0
		40.00	CSACW4000MX01 Note	CSACW40M0X51-R0 Note	External	3	3	0
		50.00	CSACW5000MX01 Note	CSACW50M0X51-R0 Note		Open	Open	0

Note Surface mount type

Remark Oscillation environment: V_{DD} = 3.0 ±0.3 V, T_A = −40 to +85°C,
External feedback resistor of OSO9 = 1 MΩ

(c) OSBx, 3.3 ±0.3 V

Material	Manu-facturer	Frequency (MHz)	Part Number	Block Name	Capacitor	Recommended External Constant			
						C_{IN} (pF)	C_{OUT} (pF)	R_d (Ω)	R_f (Ω)
Ceramic	Murata Mfg. Co., Ltd.	1	CSB1000J	OSB3	External	100	100	–	–
		2	CSA2.00MG			30	30	–	–
			CST2.00MG		Internal	(30)	(30)	–	–
		4	CSA4.00MGU		External	30	30	–	–
			CST4.00MGWU		Internal	(30)	(30)	–	–
		8	CSA8.00MTZ093		External	30	30	–	–
			CST8.00MTW093		Internal	(30)	(30)	–	–
		12	CSA12.0MTZ	OSB4	External	30	30	–	–
			CST12.0MTW		Internal	(30)	(30)	–	–
		16	CSA16.00MXZ040	OSB5	External	5	5	–	–
			CST16.00MXW0C1		Internal	(5)	(5)	–	–
		20	CSA20.00MXZ040	OSB6	External	3	3	–	–
		25	CSA25.00MXZ040	OSB7		3	3	–	–
		32	CSA32.00MXZ040			–	3	–	8.2 k
		40	CSA40.00MXZ040	OSB9		–	3	–	6.8 k
		50	CSA50.00MXZ040	OSBA		–	–	–	5.6 k
	TDK Corp.	28	CCR28.0MSC6	OSB6	External	–	–	10	–

Remark Oscillation environment: V_{DD} = 3.3 ±0.3 V, T_A = –40 to +85°C
External circuit constants L and C are necessary when a resonator of 24 MHz or more and of the third-order overtone is used.

Table 9-5. Crystal Resonator Evaluation

Material	Manu-facturer	Frequency (kHz)	Part Number	Block Name	Capacitor	Recommended External Constant				
						C_{IN} (pF)	C_{OUT} (pF)	R_d (kΩ)	LT (μH)	CT (μF)
Crystal	Seiko Instruments Inc.	32.768	VT-200 [Note] SP-T Series SSP-T Series	OSB1	External	12	15	100	–	–

Note Oscillation environment: V_{DD} = 3.3 ±0.3 V, T_A = –10 to +60°C

9.5 GTL+

Gunning transceiver logic (GTL+) is a new interface standard that implements high-speed signal transmission with a small amplitude signal. The GTL+ interface input consists of a CMOS differential circuit, similar to that of an ECL interface. However, the GTL+ interface output consists of an N-ch open-drain buffer with an enable pin attached. This enable pin controls the GTL+ output in the same manner as a conventional 3-state buffer. A small amplitude signal below 1.0 V is implemented by terminating the GTL+ output pin with a lower voltage than the power supply voltage.

When a GTL+ interface is used, it is necessary to optimally terminate the output to match the characteristic impedance of the wire and prevent reflection of the signal. In addition, because the amplitude is extremely small, fluctuation of the GND line must be minimized.

Caution When using this interface block, consult NEC Electronics in advance.

9.5.1 Electrical specifications

Table 9-6 shows the electrical specifications of GTL+.

Table 9-6. GTL+ Electrical Specifications

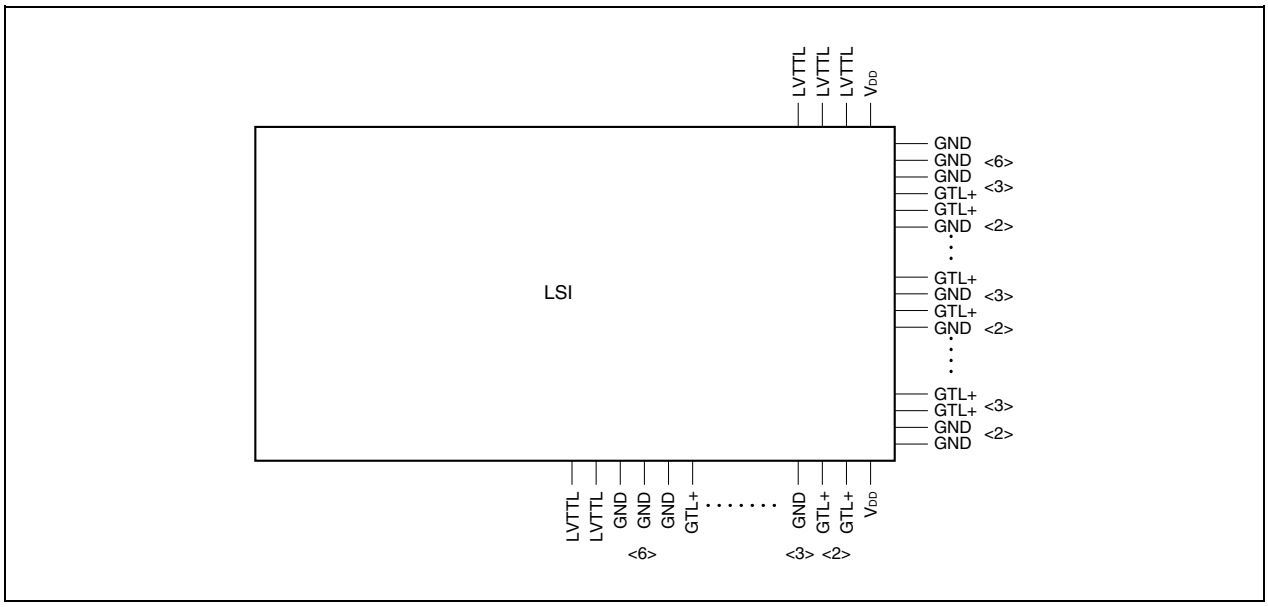
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Termination voltage	V_{TT}		1.35	1.5	1.65	V
Reference voltage	V_{REF}		(2/3) V_{TT} – 2%	1.0	(2/3) V_{TT} + 2%	V
High-level input voltage	V_{IH}		V_{REF} + 0.1			V
Low-level input voltage	V_{IL}				V_{REF} – 0.1	V
High-level output voltage	V_{OH}			1.5		V
Low-level output voltage	V_{OL}				0.55	V

9.5.2 GTL+ pin placement

The following pin placement guidelines must be observed to stabilize GTL+ interface operation when using the GTL+ interface blocks:

<1> Place a GTL+ buffer at allowable pins only.
<2> Add GND pins at the rate of one pin for every two GTL+ buffers (there are cases where the physical ratio is one GND pin for every GTL+ buffer, depending on the package and master).
<3> Place the added GND pins adjacent to a GTL+ buffer.
<4> Place the GTL+ buffers together between GND pins.
<5> Non-GTL+ buffers (even input buffers) must not be placed between the GND and V_{DD} pins between which GTL+ buffers are inserted.
<6> There should be 3 GND pins surrounding the entire set of GTL+ buffers.

Figure 9-7. Example of GTL+ Pin Placement



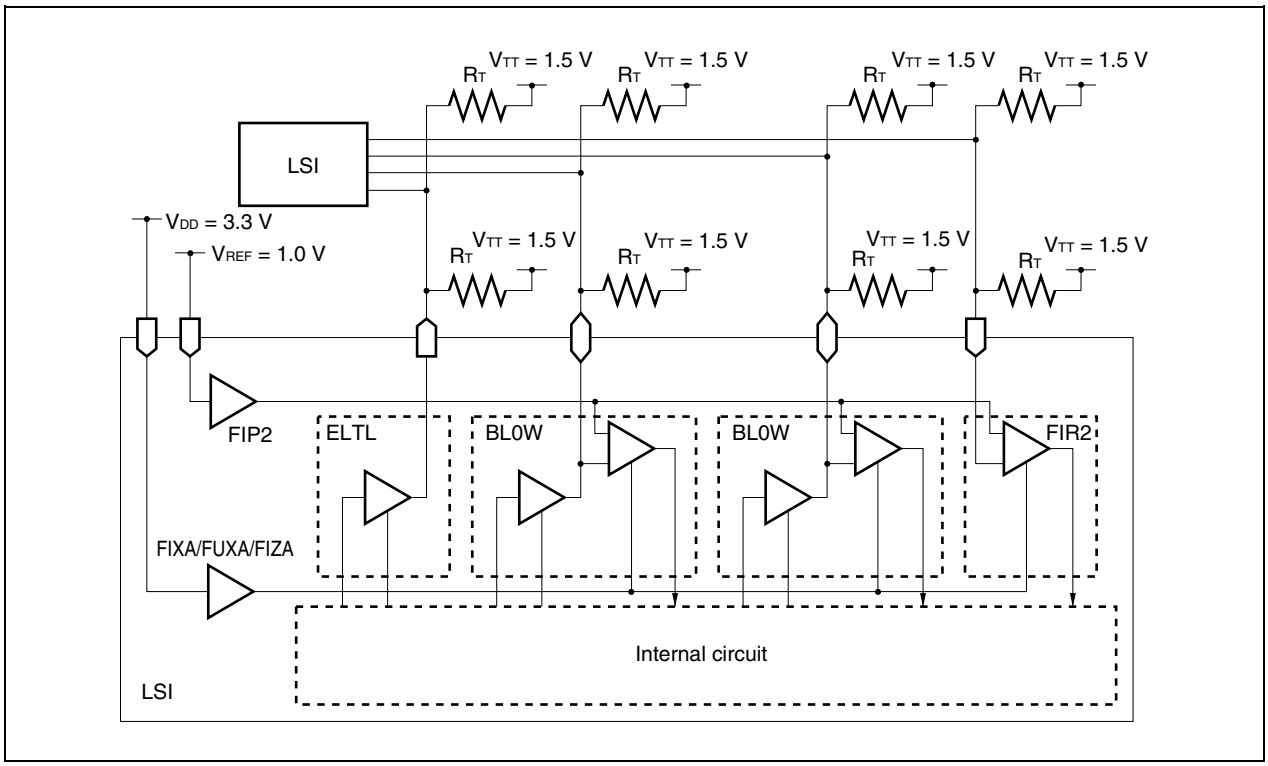
The simultaneous operation limits still apply even if there are multiple types of interfaces on the chip.

9.5.3 Connection rules

The GTL+ interface requires two external pins. One for applying the reference voltage and another for the control enable to stop operation current of input block. In addition, a terminating resistor optimized to prevent reflection of the signal is also required.

The pin that applies the reference voltage must be connected to the RFV pin of the GTL+ input buffer via an FIP2. The control pin of the GTL+ input buffer must also be connected to the IEN pin of the GTL+ input buffer via FIXA, FUXA, or FIZA.

Figure 9-8. Example of Using GTL+ Interface



9.5.4 Generating test pattern

To use the GTL+ interface, generate a test pattern according to the following rules:

<1> Apply a constant high level to the test pattern at the reference voltage input pin.

<2> Make sure that the test pattern at the input control pin is at low level in at least one of the patterns from pattern 51 to the end.

<3> If there are bidirectional pins, including an interface level other than that of GTL+, input a low-level signal to the input control pin when the input/output direction of the bidirectional buffer is determined.

9.6 Digital PLL

To implement a high-speed circuit that synchronizes two or more chips, the internal clock skew of each chip must be reduced and the phases of the clock signals of the chips must be synchronized as much as possible. However, the load of the clock line of one chip may differ from that of the other chip. It is therefore almost impossible to synchronize the phases of the clock signals with all the related F/F in the system by an ordinary method (see Figure 9-9). Therefore, NEC Electronics offers a digital PLL to improve the skew. A PLL (Phase Locked Loop) is used to minimize the phase difference between the clocks of the respective chips by synchronizing the clocks with a basic clock supplied from an external source (see Figure 9-10). In this case, the phase difference of the clocks between the respective F/F of each chip must be kept lower than CTS (Clock Tree Synthesis). For details, see **6.4 Clock Line Design**. This method cannot improve the phase difference of the basic clock, but can relatively easily lower the skew between chips.

Figure 9-9. Clock Skew

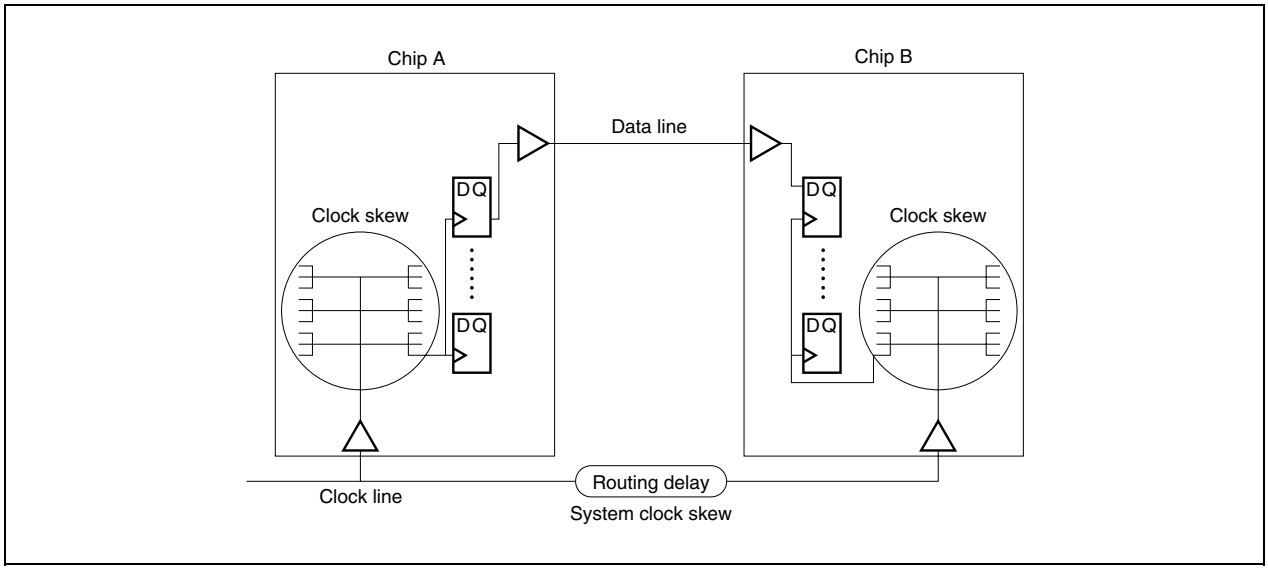
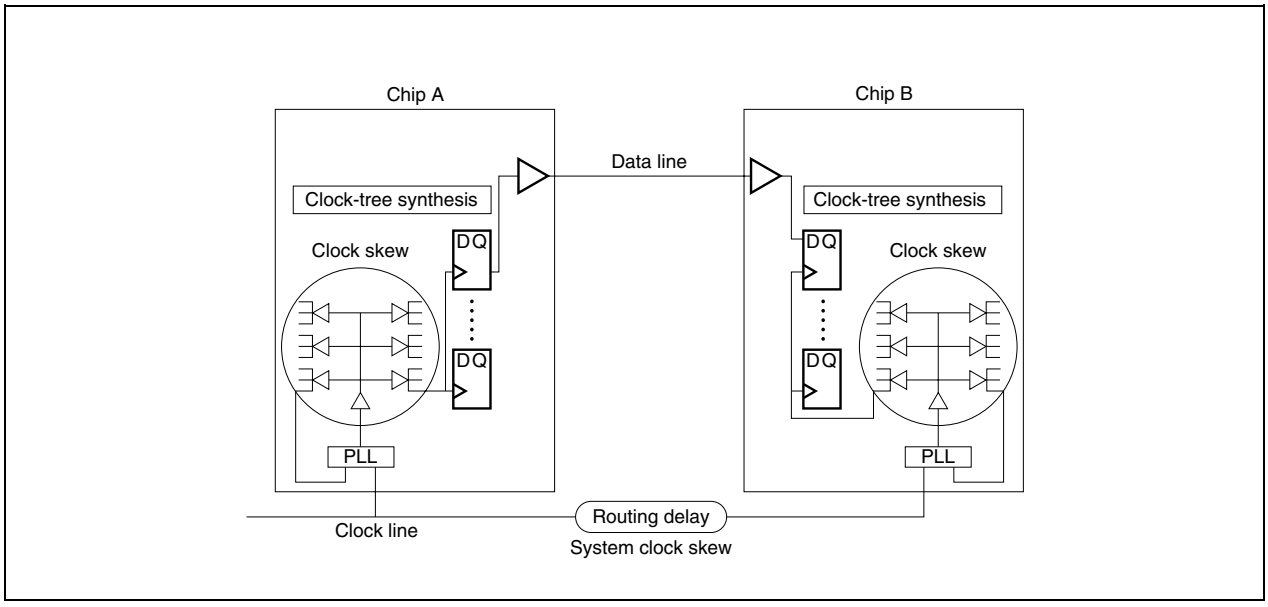


Figure 9-10. Clock Skew Countermeasures

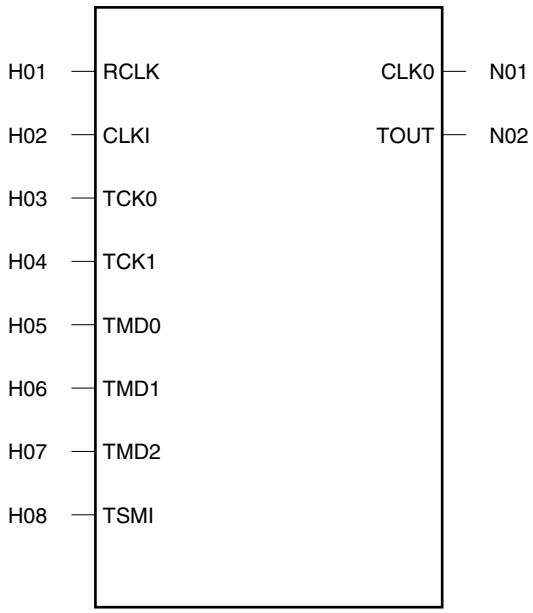


9.6.1 Digital PLL (F9E4)

(1) Function and operation mode

This section explains the functions and operation modes of the digital PLL (F9E4).

Block Name	Function	Number of cells
F9E4	Digital PLL (wide range: 33 to 80 MHz)	3770



F9E4

(a) Pin function list

Pin Name	Signal Name	Attribute	Function
H01	RCLK	IN	Reference clock signal
H02	CLKI	IN	Feedback clock signal
H03	TCK0	IN	Test clock signal (in NEC test mode)
H04	TCK1	IN	Test clock signal (in NEC test mode)
H05	TMD0	IN	Test mode select signal
H06	TMD1	IN	Test mode select signal
H07	TMD2	IN	Test mode select signal
H08	TSMI	IN	NEC test mode-dedicated input pin
N01	CLK0	OUT	Clock output signal
N02	TOUT	OUT	Lock signal and NEC test mode output signal

(b) Operation truth table

RCLK	CLKI	TCK0	TCK1	TMD0	TMD1	TMD2	TSMI	CLK0	TOUT	Mode
A	○	X	X	0	0	0	X	A	LOCK	PLL mode
A	X	X	X	1	0	0	X	0	0	Reset mode
A	X	X	X	0	1	0	X	A	0	Through path mode
A	X	X	X	0	0	1	X	0	0	Stop mode
A	X	○	○	1	1	0	○	0	TEST	NEC test mode
A	X	○	○	1	0	1	○	0	TEST	
A	X	○	○	1	1	1	○	0	TEST	

Remark A, ○: Indicates that the selected mode can be used.

(2) Electrical specifications

The electrical specifications of the digital PLL (F9E4) are shown in Tables 9-7 and 9-8.

Table 9-7. DC Characteristics

Specification V_{DD} = 3.3 ±0.3 V, T_A = -40 to +85 °C (T_J = -40 to +125 °C)

Item	Symbol	MIN	TYP	MAX	Unit
RCLK high-level input voltage	V_{IH}	2.0		V_{DD}	V
RCLK low-level input voltage	V_{IL}	0		0.8	V

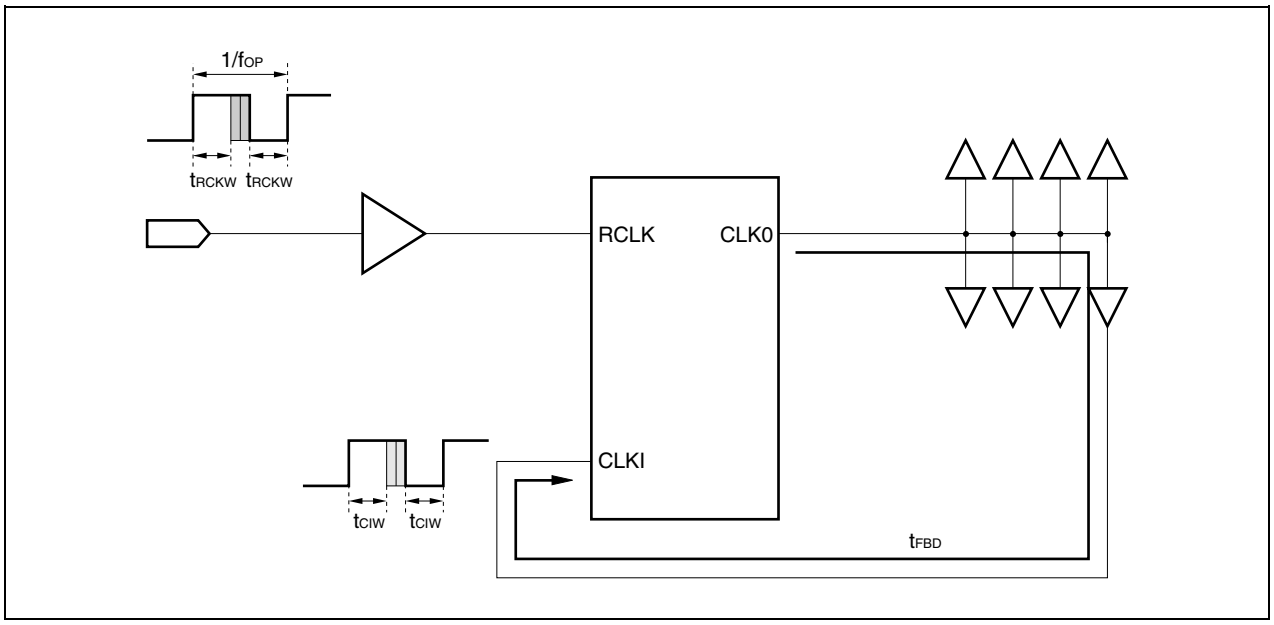
Table 9-8. AC Characteristics

Specification V_{DD} = 3.3 ±0.3 V, T_A = -40 to +85 °C (T_J = -40 to +125 °C)

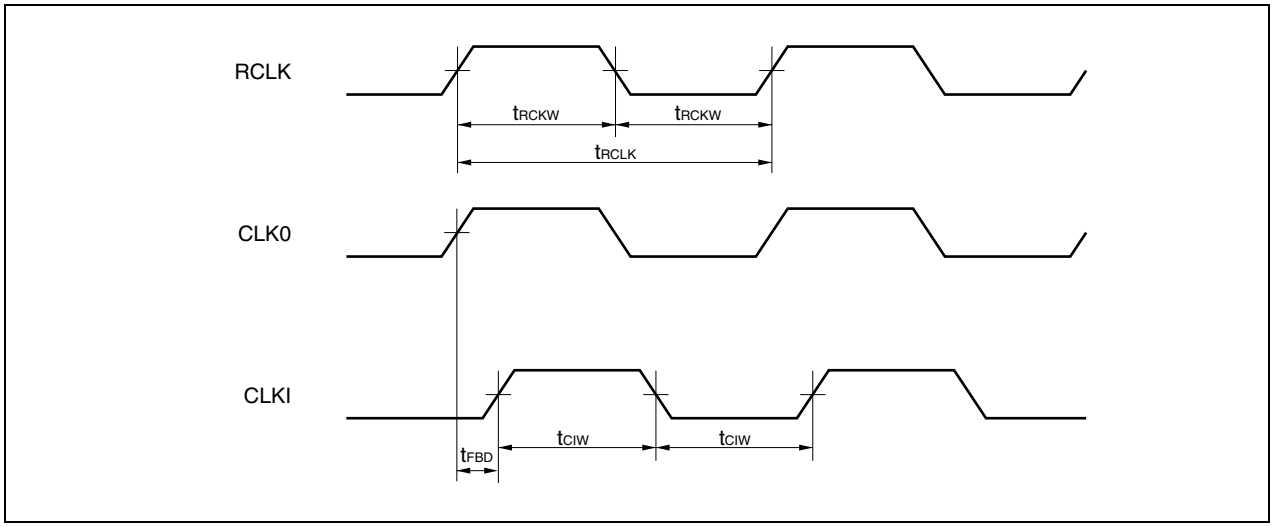
Item		Symbol	MIN	TYP	MAX	Unit
Operating frequency		f_{OP}	33		80	MHz
Reference clock (RCLK) cycle		t_{RCLK}	12.5		33.3	ns
Input minimum pulse width (H/L) (vs. RCLK)		t_{RCKW}	4.3			ns
Input minimum pulse width (H/L) (vs. CLKI)		t_{CIW}	3.3			ns
Clock tree delay		t_{FBD}	0		$2t_{RCLK}$ - 8.0	ns
Steady phase error		t_{OFF}			±0.1	ns
Output jitter[Note]		t_{JITT}			±0.18	ns
Lead-in time		t_{LOCK}			1325	t_{RCLK}
Reset mode setup time		t_{RSTW}	5			ns
Through path mode delay	LL	t_{THR}	0.60	0.90	1.40	ns
V_{DD} = 3.3 V ±5 %	HH		0.40	0.70	1.10	ns
	LL		0.60		1.30	ns
	HH		0.40		1.00	ns
Output stop time		t_{STOP}	0		4	t_{RCLK}

Note If an input signal includes jitter, the jitter of the digital PLL is the sum of the value shown in the above table and the jitter of the input signal.

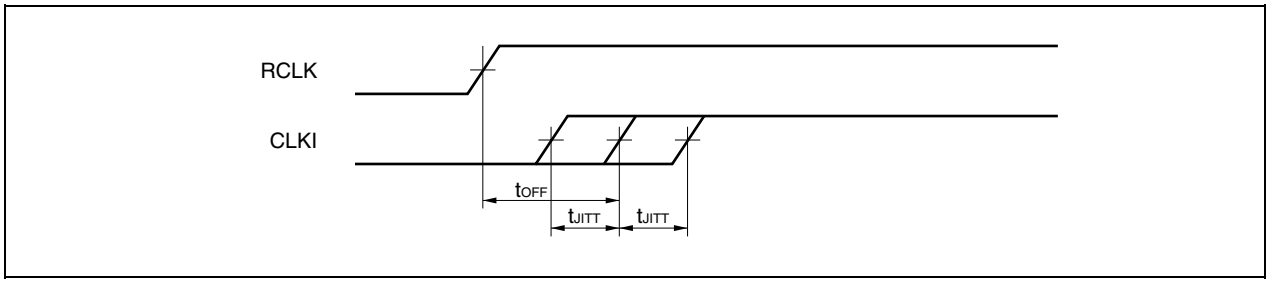
Figure 9-11. Digital PLL Timing (F9E4)



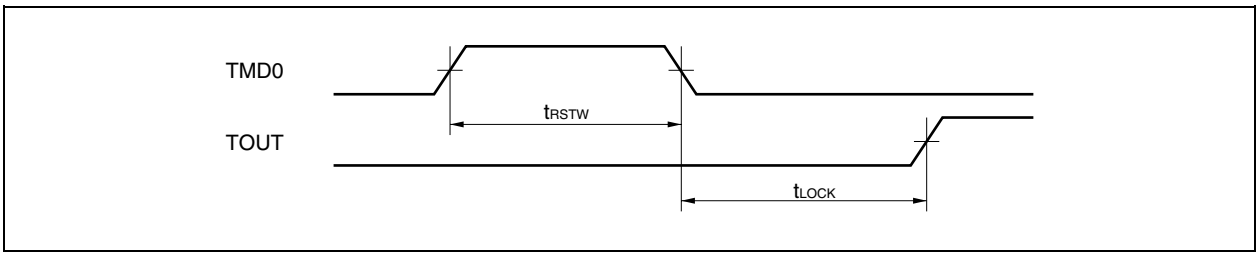
- Input and output waveforms



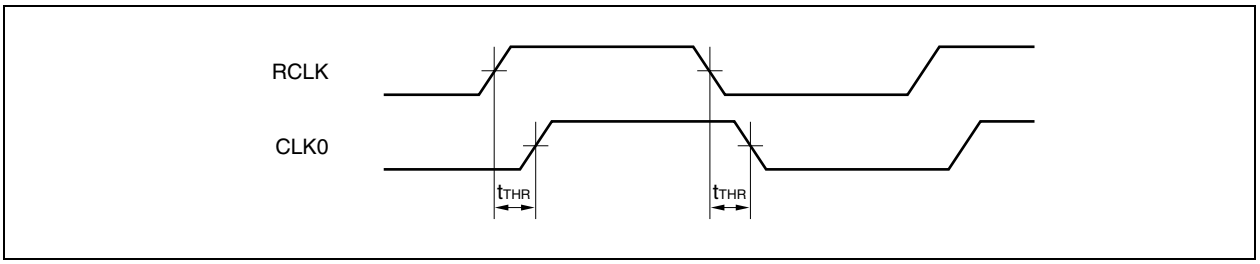
- Jitter and steady phase error



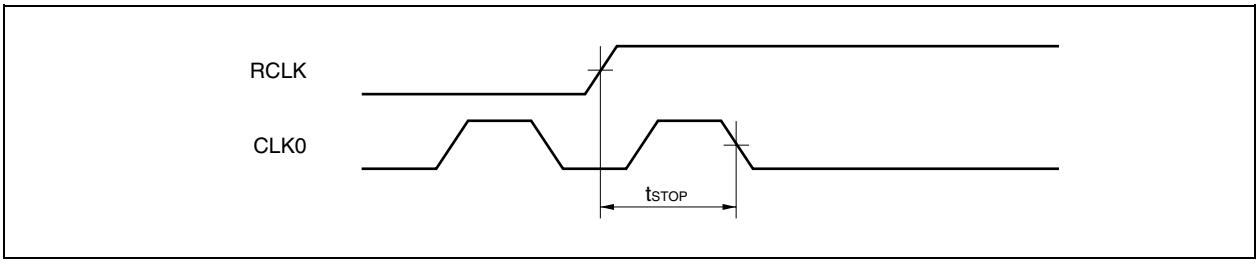
• Lead-in time and reset mode



• Through path mode



• Stop mode



(3) Connection rules

When using the digital PLL, seven input pins must be directly controlled from the external pins of the LSI. Moreover, one output pin must be directly output to an external pin. Therefore, the external input pins are connected via the input buffer of the digital PLL block, and the external output pin is also connected via the output buffer to the output pin of the digital PLL block.

Use the dedicated input buffer “FI0P (3.3 V I/F level)” or “FI0Q (5 V I/F level)” for the input pin of RCLK. Do not share its signal lines with the general signal lines.

Use Schmitt buffers (FIS1) as the input buffers of the TMD0, TMD1, and TMD2 pins to prevent malfunctioning due to noise. Input signals directly from external pins to these buffers, and do not share the signal lines of these buffers with general signal lines. Do not locate an input/output buffer with a high driving capability in the vicinity of these pins, and locate GND pins near these pins as far as possible to prevent malfunctioning due to noise.

Configure the circuits of the TCK0, TCK1, and TSMI input pins, and TOUT output pins so that these pins can be directly controlled or output by an external circuit in the NEC test mode shown in the table below. When these pins are shared with general signal lines, their wiring length tends to be long. Therefore, do not multiplex these pins with the pins that must operate at high speeds.

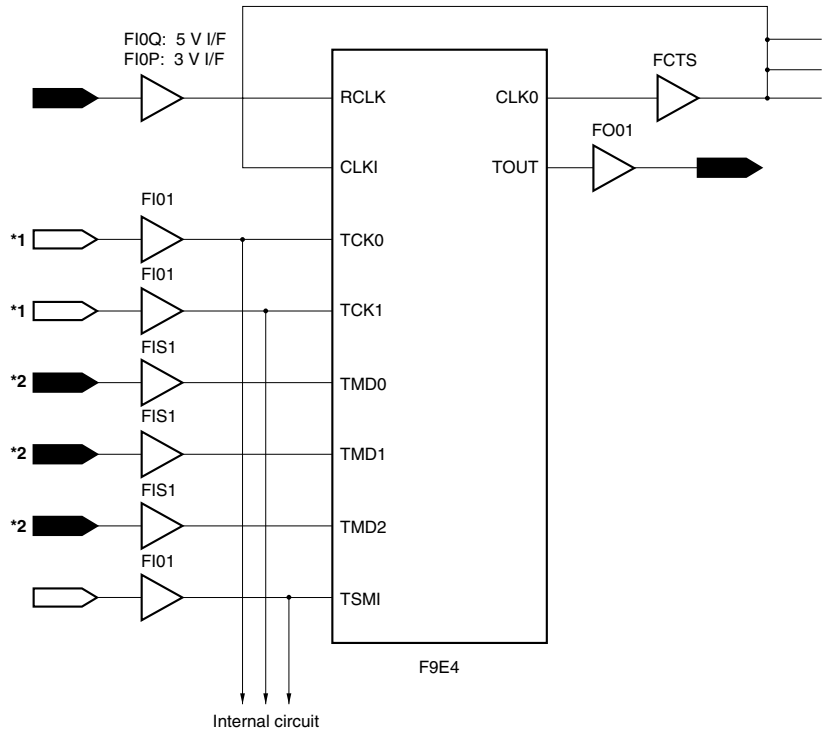
Figure 9-12 shows an example.

NEC test mode

TMD0	TMD1	TMD2
1	1	0
1	0	1
1	1	1

Figure 9-12. Digital PLL Connection Example (1/2)

(a) When digital PLL is used as single unit



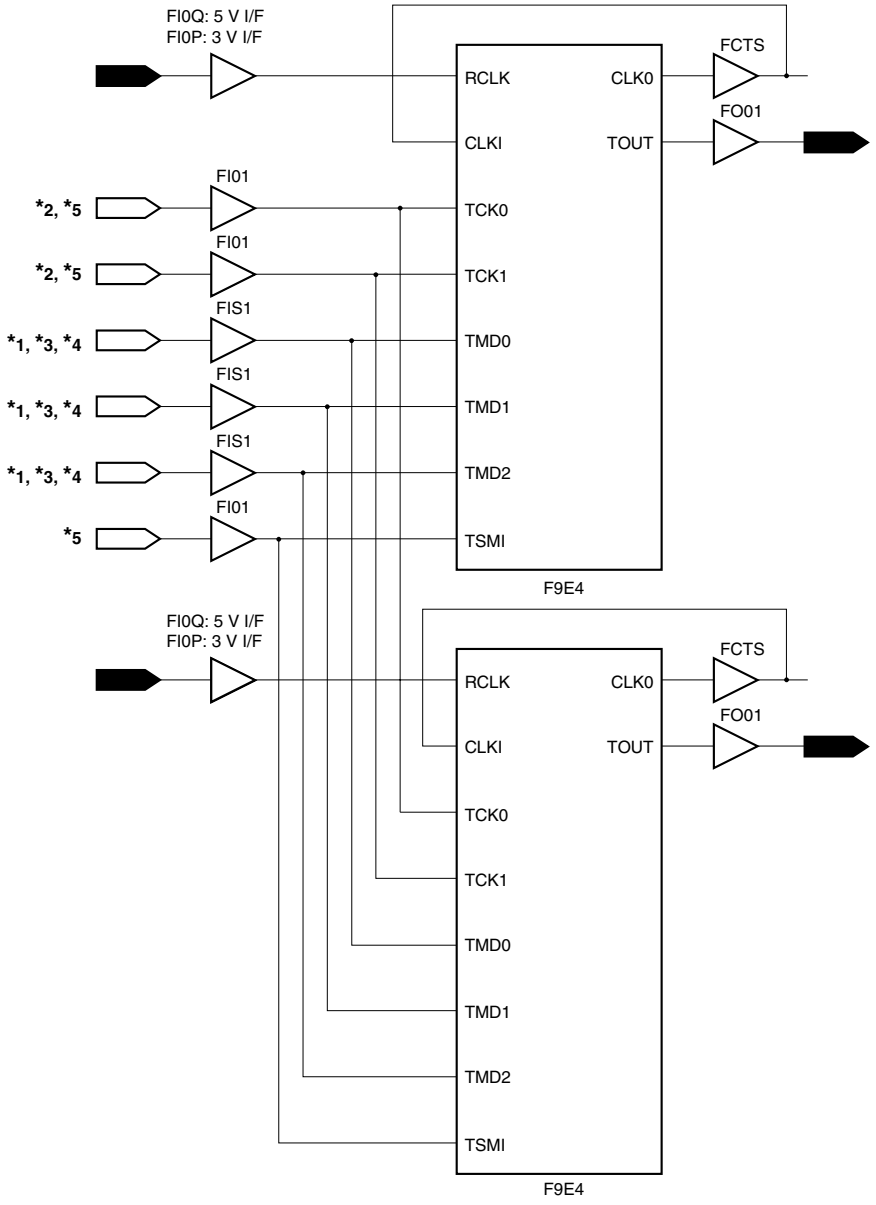
Cautions 1. ▬▶: Pin that cannot be shared with other general function pins, except for TMD0, which is shared with power-on reset. In the same way, the pin connected to the TOUT pin cannot be shared.

2. Pin *1 cannot be shared by using a bidirectional buffer.

3. Use a Schmitt buffer for the pin marked *2.

Figure 9-12. Digital PLL Connection Example (2/2)

(b) When two digital PLLs are used separately



Cautions 1. Use a Schmitt buffer for pin *1.

2. Pin *2 cannot be shared with general pins using a bidirectional buffer.

3. Pin *3 cannot be shared with general pins except for power-on reset at TMD0.

4. Pin *4 can be shared with pins with the same pin function only when multiple digital PLLs are used.

5. Pin *5 cannot be shared with pins a using a GTL+ interface buffer, N-ch open-drain buffer, or CMOS 5 V tolerant output buffer.

6. ▬▶ pins cannot be shared with other pins.

(4) Digital PLL operation

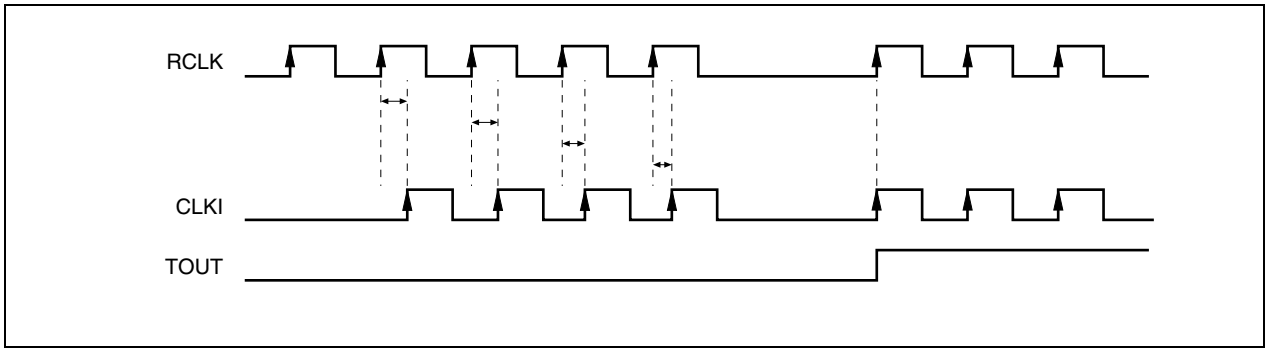
Digital PLLs have a number of operation modes other than the PLL mode. This section explains the operation modes necessary for designing embedded arrays with a PLL.

Be sure to reset the digital PLL (by executing the reset mode) before using the digital PLL (on power application). Execute reset when the voltage of the embedded array has reached the switching voltage and the clock with the desired frequency has been input to the RCLK pin.

(a) PLL mode

This mode is set when both the TMD0 and TMD1 pins are low. In this mode, the digital PLL synchronizes the phases of an external reference clock with the phase of the internal clock of the LSI. The TOUT pin goes high when the clock signals are synchronized. Exercise care in using this pin because it may generate spike noise.

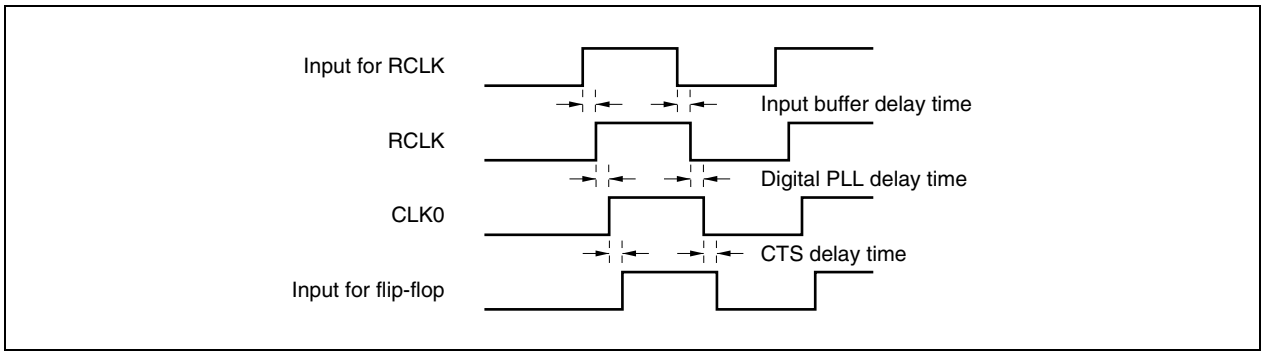
Figure 9-13. PLL Mode Timing



(b) Through path mode

This mode is set when the TMD0 pin is low and the TMD1 pin is high. Because simulation cannot be executed in the PLL mode which is the normal operation mode of the digital PLL, generate a test pattern for simulation in this mode. Give thorough consideration to the delay of the clock line, including the delay of the digital PLL.

Figure 9-14. Through Path Mode Timing



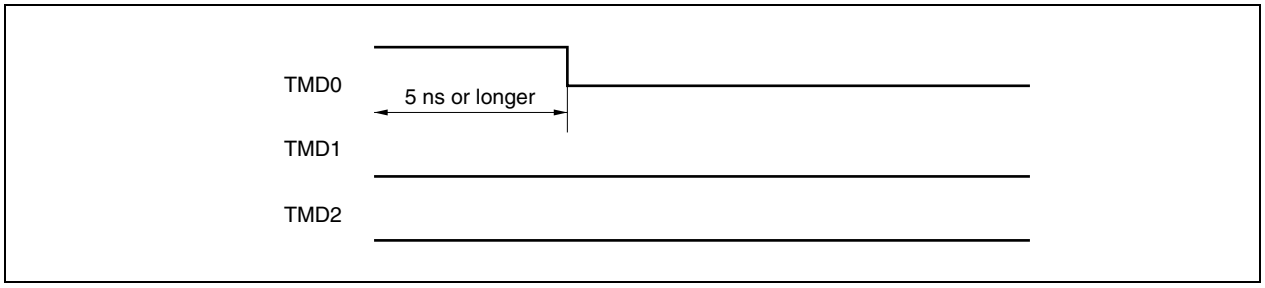
(c) Reset mode

This mode is for resetting the entire digital PLL.

After power application, execute the reset mode when the power supply of the EP-1 series is at the voltage at which it is to be used and the frequency of RCLK has stabilized at the frequency at which it is to be used.

Although the timing of setting reset mode is not prescribed, take sufficient care not to input noise to the TMD0, TMD1, or TMD2 pins, and set the reset mode for at least 5 ns. Also, because the output clock will be unstable until the digital PLL locks after reset mode is released, reset the user circuit after the digital PLL has locked.

Figure 9-15. Reset Mode Timing



The reset mode is necessary in the following cases:

<1> After power application

<2> If the frequency of the reference clock (RCLK) constantly fluctuates. Be sure to input stable clock (of constant frequency) to RCLK in the PLL mode. If the frequency of the clock input to RCLK constantly fluctuates (i.e., if the following permissible frequency fluctuation range is exceeded), be sure to execute the reset mode.

Permissible frequency fluctuation: Frequency fluctuation = ±1 ns

<3> When the clock signal stop mode is executed and released

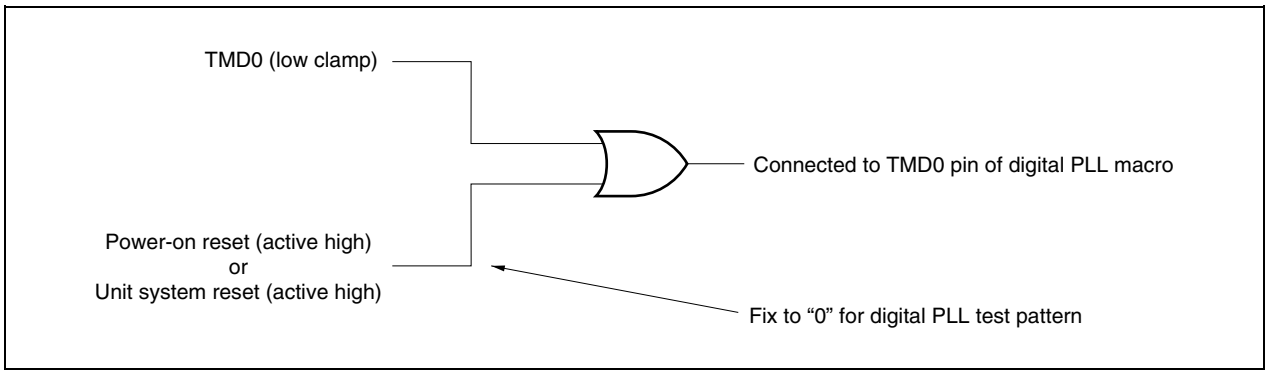
Example of using TMD0 related to reset mode

If the reset signal used when testing (simulating) the embedded array is different from the signal for actual use (when the active level differs or when the logic of the reset signal is organized in the embedded array), use the following circuit.

In this circuit configuration, clamp the TMD0 pin to the low level for actual use and fix the reset signal to “0” for testing.

At this time, make sure that noise is not superimposed on the TMD0 pin of the digital PLL. Consult NEC Electronics when inserting a gate between the dedicated pin and PLL as shown in the following figure.

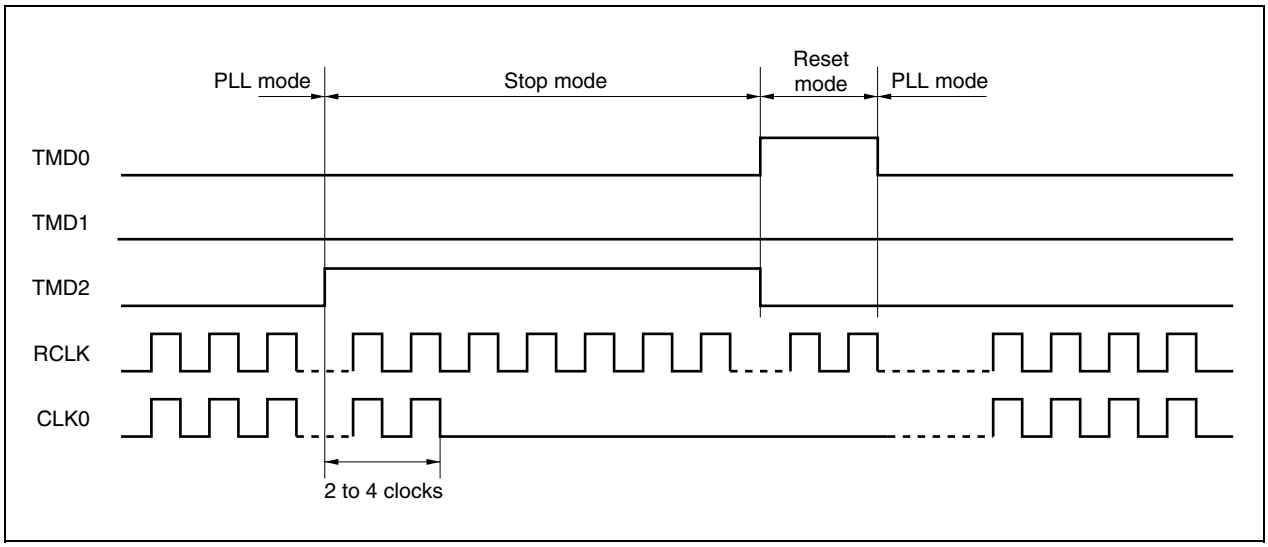
Figure 9-16. Example of Using TMD0



(d) Stop mode

This mode is set when the TMD0 and TMD1 pins are low and the TMD2 pin is high. In this mode, the internal clock signal of the embedded array is stopped 2 to 4 clocks after TMD2 has gone high. When releasing the stop mode or when stopping the basic clock input to the RCLK pin, be sure to input the basic clock again and execute the reset mode.

Figure 9-17. Stop Mode Timing

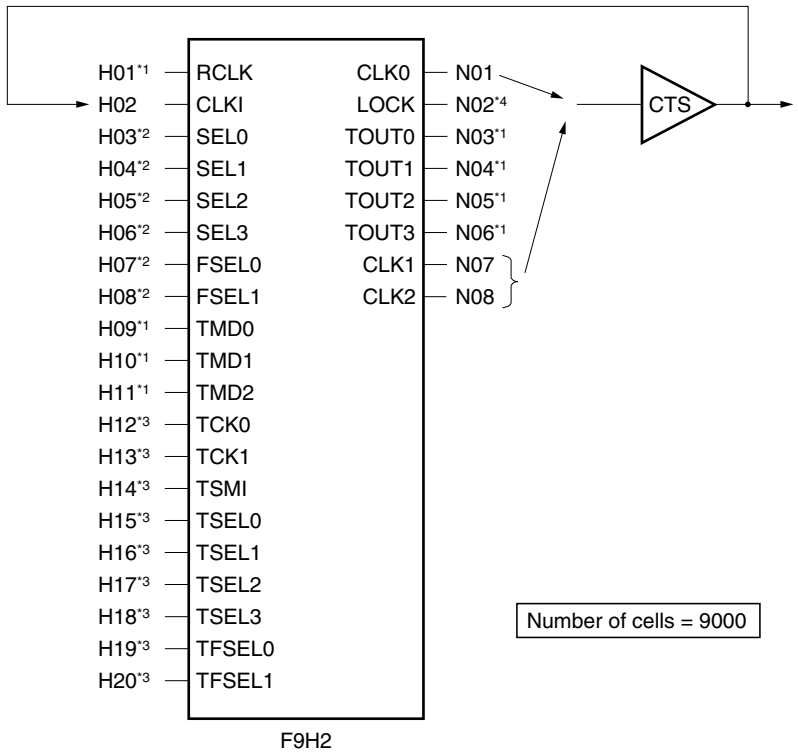


9.6.2 Digital PLL (F9H2)

(1) Function and operation mode

This section explains the functions and operation modes of the multiplication digital PLL (F9H2).

Figure 9-18. Digital PLL Connection Example (F9H2)



Cautions 1. Pins marked *1 cannot be shared with other LSI pins (dedicated pins).

2. Pins marked *2 do not need to be connected with external pins.

3. Pins marked *3 can be shared with other LSI pins.

4. Pins marked *4 do not need to be connected with external pins.

5. Be sure to connect one of the CLK0 to CLK2 outputs to the CLKI input. (Never divide the outputs by an F/F or input a divided output to CLKI.) If multiple CLKn are used, the phases are not synchronized.

6. Clamp the SEL3, FSEL0, and FSEL1 pins to either the high level or low level by using F091.

(a) Pin function list

Pin Name	Signal Name	Attribute	Function
H01	RCLK	IN	Reference clock signal
H02	CLKI	IN	Feedback clock signal
H03	SEL0	IN	Multiplication factor setting signal
H04	SEL1	IN	
H05	SEL2	IN	
H06	SEL3	IN	
H07	FSEL0	IN	Frequency setting signal
H08	FSEL1	IN	
H09	TMD0	IN	Test mode select signal
H10	TMD1	IN	
H11	TMD2	IN	
H12	TCK0	IN	Test mode clock input signal
H13	TCK1	IN	
H14	TSMI	IN	Test mode switching signal
H15	TSEL0	IN	Test mode multiplication factor setting signal
H16	TSEL1	IN	
H17	TSEL2	IN	
H18	TSEL3	IN	
H19	TFSEL0	IN	Test mode setting signal
H20	TFSEL1	IN	
N01	CLK0	OUT	Multiplication clock output signal
N02	LOCK	OUT	Lock signal
N03	TOUT0	OUT	NEC test mode output signal
N04	TOUT1	OUT	
N05	TOUT2	OUT	
N06	TOUT3	OUT	
N07	CLK1	OUT	Multiplication clock output signal (2-division output)
N08	CLK2	OUT	Multiplication clock output signal (4-division output)

(b) Operation truth table

RCLK	TCKn	SELn	TSELn	TFSEL1	TFSEL0	TMD2	TMD1	TMD0	TSMI	CLKn	LOCK	TOUTn	Mode
A	X	√	X	X	X	0	0	0	X	A	LOCK[Note1]	0	PLL mode[Note2]
X	X	√	X	X	X	0	0	1	X	0	0	0	Reset mode
A	X	√	X	X	X	0	1	0	X	A	0	0	Through path mode[Note3]
X	X	√	X	X	X	1	0	0	X	0	0	0	Stop mode
A	√	X	√	0	0	1	0	1	√	0	TEST	TEST	NEC test mode
A	√	X	√	0	1	1	0	1	√	0	TEST	TEST	
A	√	X	√	1	0	1	0	1	√	0	TEST	TEST	
A	√	X	√	1	1	1	0	1	√	0	TEST	TEST	
A	√	X	√	0	0	1	1	0	√	0	TEST	TEST	
A	√	X	√	0	1	1	1	0	√	0	TEST	TEST	
A	√	X	√	1	0	1	1	0	√	0	TEST	TEST	
A	√	X	√	1	1	1	1	0	√	0	TEST	TEST	
A	√	X	√	0	0	1	1	1	√	0	TEST	TEST	
A	√	X	√	0	1	1	1	1	√	0	TEST	TEST	
A	√	X	√	1	0	1	1	1	√	0	TEST	TEST	
A	√	X	√	1	1	1	1	1	√	0	TEST	TEST	

Note 1. This is 1 when the phase is locked (when the phase of RCLK and CLKI is synchronized).

2. Multiplied A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

3. A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

Remark A, √: Indicates that the selected mode can be used

(c) Multiplication factor settings

Set the multiplication factor by SELn (SELn, FSELn can also be clamped to F091).

Multiplication factor	FSELn[Note]	SEL3[Note]	SEL2	SEL1	SEL0	Usable Frequency Band (RCLK)
1	X	X	0	0	0	33 to 80 MHz
2	X	X	0	0	1	33 to 50 MHz, 66 to 100 MHz
3	X	X	0	1	0	33 MHz, 44.3 to 66.6 MHz
4	X	X	0	1	1	33 to 50 MHz

Note Fix FSELn and SEL3 to either 1 or 0 using F091.

Caution Can only be used within the above shown frequency band; other frequencies cannot be used.

(2) Electrical specifications

The electrical specifications of the digital PLL (F9H2) are shown in Table 9-9.

Table 9-9. AC Characteristics (F9H2)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remark
RCLK frequency Note 1	t_{RCKT}	33.0		80.0	MHz	When × 1 is set
		33.0		100.0	MHz	When × 2 is set
		33.0		66.6	MHz	When × 3 is set
		33.0		50.0	MHz	When × 4 is set
Power supply allowable fluctuation width				V_{DD} ±0.3	V	peak-to-peak
Input duty	t_{CIW}			50 ±5	%	
RCLK pulse width	t_{RCKW}	2.8			ns	
CLKI pulse width	t_{SIW}	2.0			ns	
Output jitter	t_{JITT}			600 Note 2	ps	Fluctuation of the power supply caused by noise: 300 mV (peak-to-peak) or less
				Note 2, 3	ps	Fluctuation of the power supply caused by noise: 300 to 600 mV (peak-topeak)
Output duty	t_{COW}	45		55	%	
Through path mode delay	t_{THR}	1.10		2.70	ns	CLK0 output
	t_{THL}	1.15		2.70	ns	CLK0 output
	t_{THR}	1.10		2.70	ns	CLK1 output
	t_{THL}	1.15		2.70	ns	CLK1 output
	t_{THR}	1.10		2.70	ns	CLK2 output
	t_{THL}	1.15		2.70	ns	CLK2 output
CTS delay restriction	t_{FBD}			20.42	ns	
Lead-in time	t_{LOCK}			2116	RCLK	
Steady phase error	t_{OFF}			±0.1	ns	No input jitter
Reset pulse width	t_{RSTW}	5			ns	
Output stop time	t_{STOP}	2		4	t_{COW}	
Power consumption Note 4	P_{PLL}		65		mW	V_{DD} = 3.3 V, T_A = 85 °C, RCLK = 50 MHz, CLK0 = 100 MHz

Notes 1. The usable frequency range for each multiplication factor is as follows. Note that other frequencies cannot be used.
× 1: 33 to 80 MHz
× 2: 33 to 50 MHz, 66 to 100 MHz
× 3: 33 MHz, 44.3 to 66.6 MHz
× 4: 33 to 50 MHz

2. The output jitter when the input jitter is 80 ps or less. If the input jitter exceeds 80 ps, add the input jitter to the output jitter value.

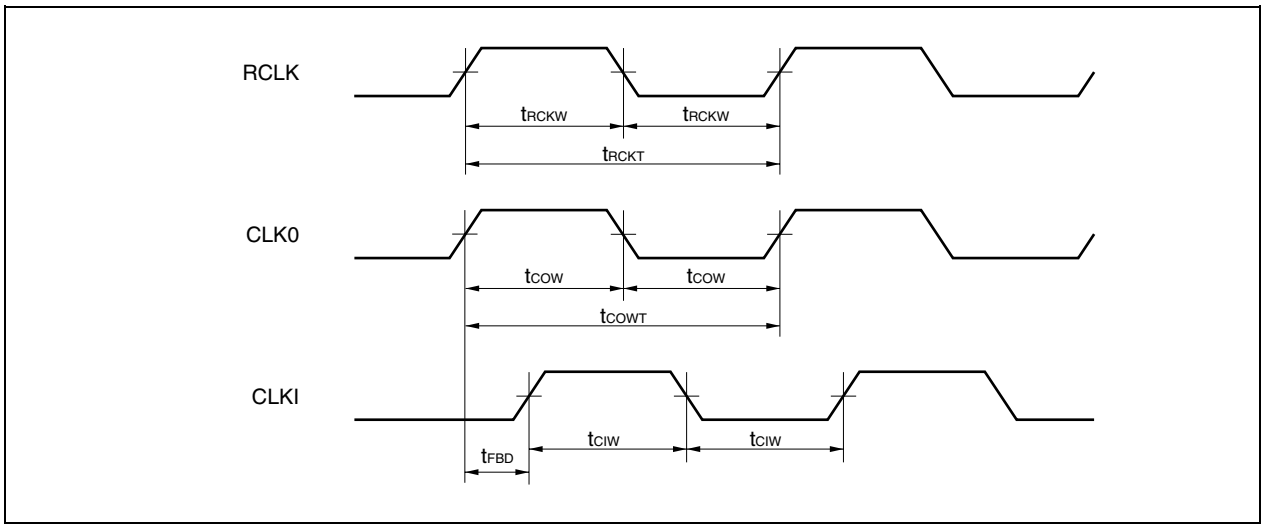
3. Jitter [ps] = fluctuation of the power supply [mV] × 2 [ps/mV]

4. The power consumption is calculated by using the following formula.

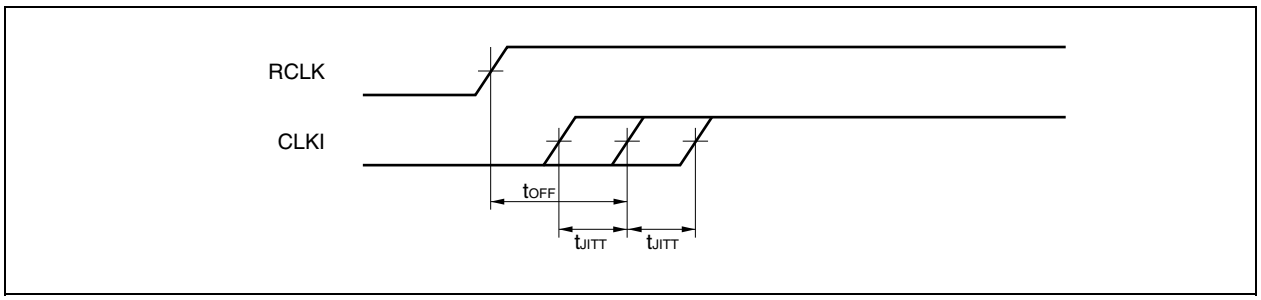
$$P_{PLL} = \{RCLK \times 900 \times 1.09+(RCLK/8)\times 100 \times 1.09+(RCLK/12)\times 80 \times 1.09+CLK0 \times 130 \times 1.09\} /1000 \text{ [mW]}$$

Remark RCLK: RCLK frequency [MHz], CLK0: Multiplication clock frequency [MHz],
1.09: Value when V_{DD} = 3.3 V, T_A = 85°C

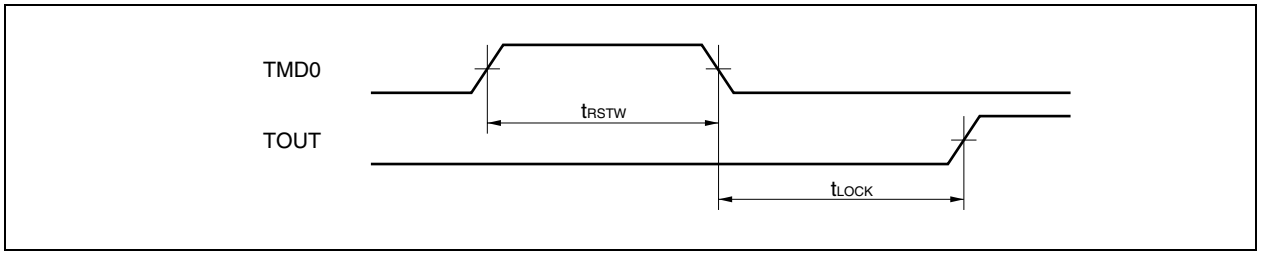
• Input and output waveforms



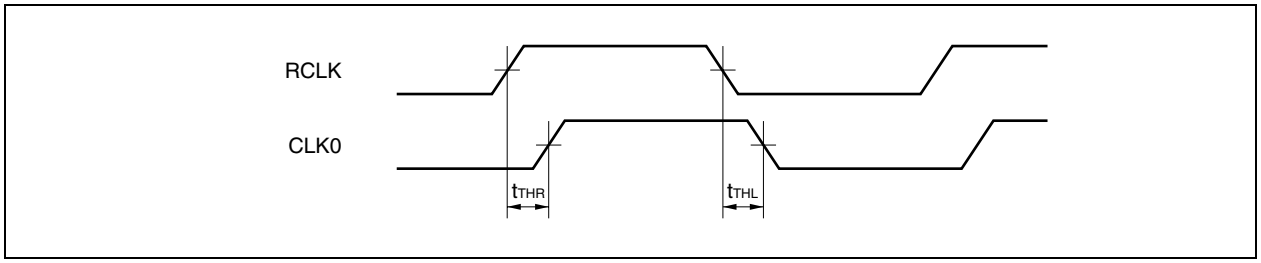
• Jitter and steady phase error



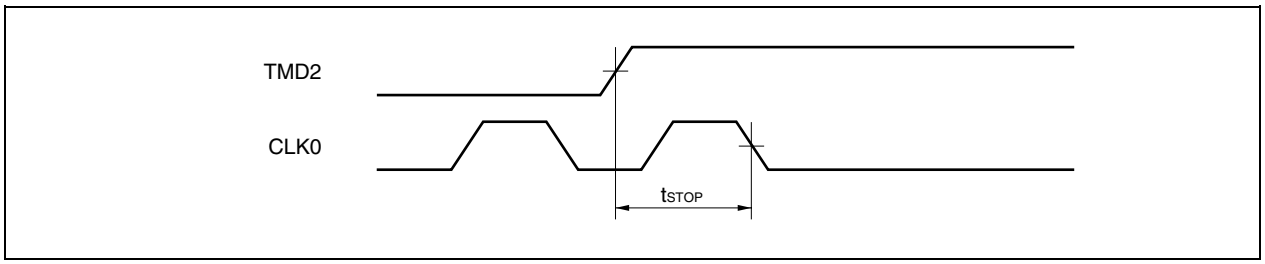
• Lead-in time and reset mode



• Through path mode



• Output stop mode

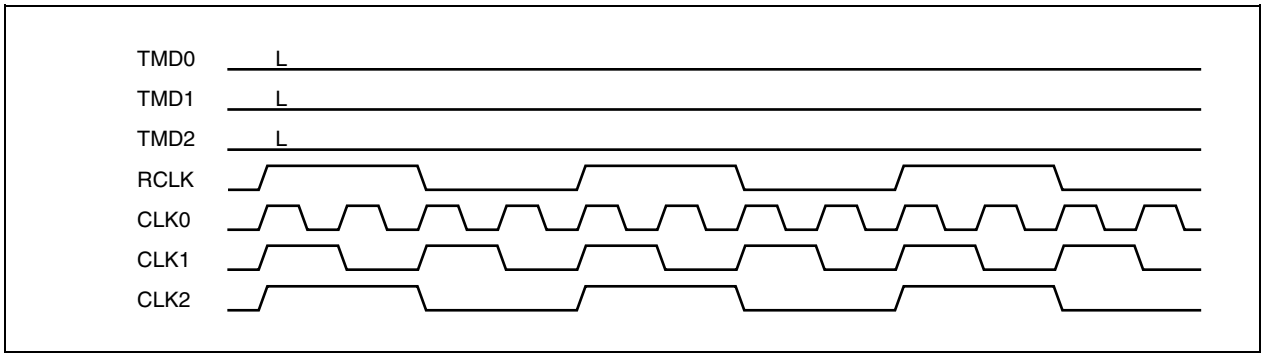


(3) Digital PLL operation mode

(a) PLL mode

In this mode, the phase of RCLK is synchronized with the phase of CLKn, and the clock set by the multiplication factor setting signal (SELn) is output.

[Waveform when × 4 is set in PLL mode]



(b) Reset mode

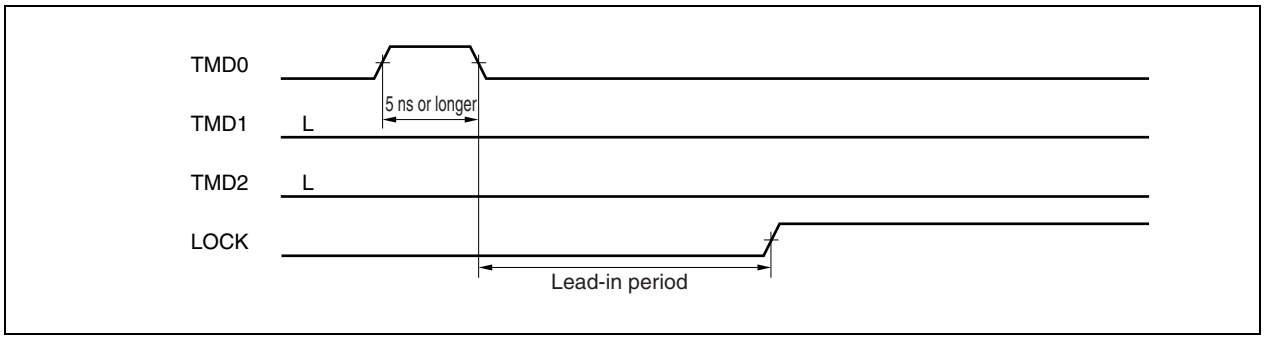
This mode is used to reset the entire digital PLL. Be sure to execute the reset mode after power application.

Although the timing of setting reset mode is not prescribed, set the reset mode for at least 5 ns.

Whether inputting RCLK or not during reset mode does not affect the operation.

The digital PLL locks within the lead-in period after reset mode is released.

[Waveform at reset mode]

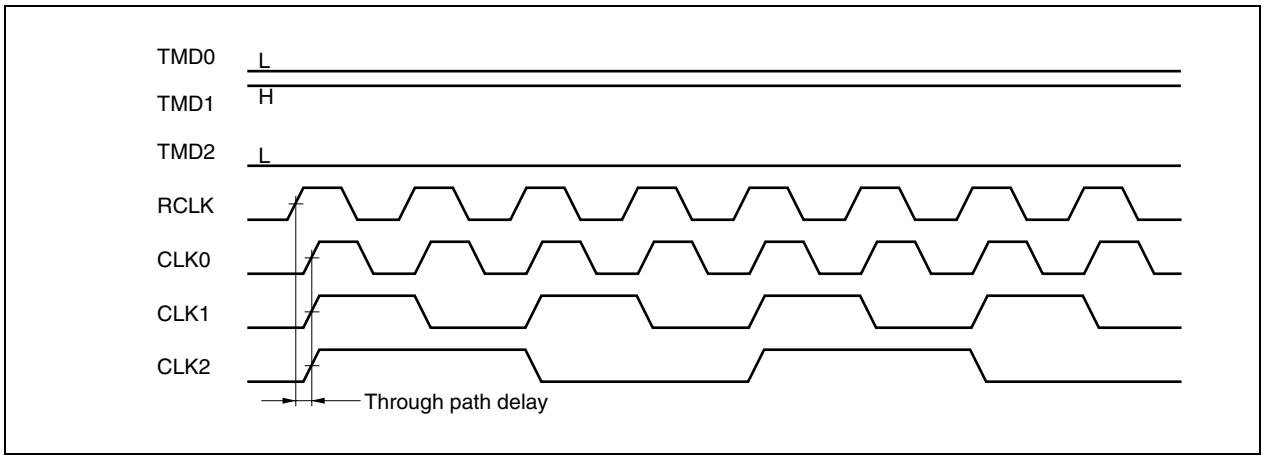


(c) Through path mode

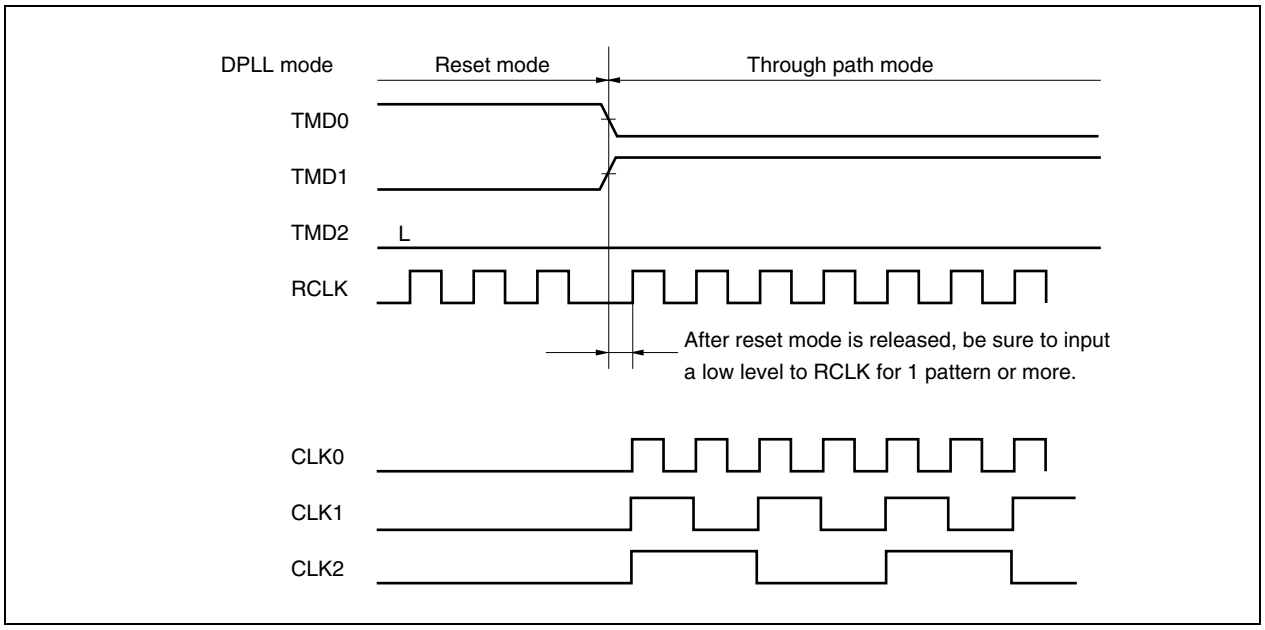
This mode is used to test the user circuit that is placed in the stage following the digital PLL. CLK0 is output later than RCLK by the amount of through path delay (In through path mode, RCLK = CLK0 regardless the multiplication factor).

The delay time in the AC ratings does not include the delay value of the clock tree, etc.

[Waveform of through path output]



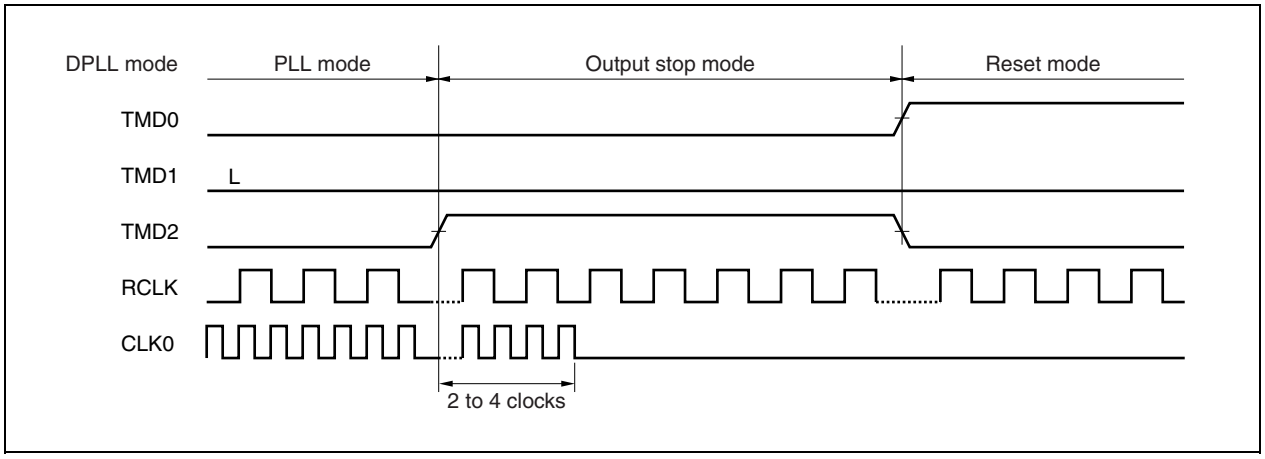
- Caution when setting the F9H2 type to through path mode
  Always set through path mode from reset mode.



(d) Output stop mode

This mode is used to fix the CLK0 output to low. When 2 to 4 clocks have elapsed after the output stop mode is set, CLK0 is fixed to low level without generating a spike.

Although the timing of setting stop mode is not prescribed, be sure to execute the reset mode after the output stop mode is released.



(4) Connection rules

- The external input buffer FI0P or FI0Q must be used for RCLK input. Use FI0P for the 3 V interface and FI0Q for the 5 V interface.
- Allocate the digital PLL at the corner (any of the four corners is acceptable).
- Do not place RAM or ROM near the digital PLL.
- Place GNDs for both pins next to the pin at which RCLK is placed.
- Place additional GNDs to reduce external buffer noise and do not place a high driving buffer (e.g. GTL+) near the digital PLL.
- Be sure to connect a clock driver or CTS to the CLK0 to CLK02 outputs, and either of the outputs to the CLKI input of the digital PLL (F9H2) (unused CLKn outputs can be left open). However, when the output of CLKn is divided by a F/F, etc., do not connect the divided output to the CLKI input of the digital PLL (F9H2).
- Connect Schmitt buffers to directly input TMD0 to TMD2 from external pins. Make sure that no spike noise is input to the TMD0 to TMD2 pins.
- Because the digital PLL (F9H2) is tested as a standalone unit, design the connection so that pins other than CLKI, SEL0 to SEL2 and CLK0 to CLK2 can be input/output from an external pin (TCK0, TCK1, TSMI, TSEL0 to TSEL3, TFSEL0 and TFSEL1 can be shared with another external pin). RCLK, TCK0, and TCK1 cannot be shared by using a bidirectional buffer.
- Set the reset mode for at least 5 ns.
- After power application, release the reset mode when the power supply voltage, input clock pulse width, duty, and frequency are stabilized at 3.3 ±0.3 V, 2.8 ns or more, 50 ±5%, and ±1 ns of the frequency to be used, respectively.
- Be sure to execute the reset mode when the output stop mode is released.
- Perform a test in the through path mode before executing simulation.
- The waveform of the CLK1 output is equal to 1/2 the CLK0 output waveform.
- The waveform of the CLK2 output is equal to 1/4 the CLK0 output waveform.
- In PLL mode, the output clock is unstable until the digital PLL (F9H2) locks (TOUT changes from L to H).

Consequently, operation cannot be guaranteed.

- After reset mode is released, be sure to input a ±1 ns cyclic variation with a 2.8 ns or longer pulse width at a duty of 50 ±5%. If an unstable clock exceeding this range is input to RCLK, the PLL is automatically shifted to reset mode, and the output clock may be unstable until the PLL locks.
- Be sure to execute the reset mode when the multiplication factor is changed.
- When reset mode is set or released, spike noise may be generated at the output clock.
- Supply the power supply voltage within the specifications (3.3 ±0.3 V) so that the fluctuation of the power supply caused by noise is 600 mV (peak-to-peak) or less. The correct operation of the digital PLL (F9H2) cannot be guaranteed if the fluctuation of the power supply caused by noise exceeds 600 mV.
- Supply the power supply voltage within the specifications (3.3 ±0.3 V) so that the fluctuation of the power supply caused by noise is 300 mV (peak-to-peak) or less. If the fluctuation of the power supply caused by noise is 300 to 600 mV, calculate the jitter using the following formula.

Jitter [ps] = fluctuation of the power supply [mV] × 2 [ps/mV]

The correct operation of the digital PLL (F9H2) cannot be guaranteed if the fluctuation of the power supply caused by noise is 600 mV or more.

- A special request is needed when a circuit (e.g. power-on-reset circuit) is placed between an input buffer and TMD0 to TMD2.
- Cautions on setting feedback clocks
  - Be sure to connect CTS to the CLK0 to CLK2 outputs, and that output to the CLKI input of the digital PLL (F9H2).
  - Do not divide outputs such as CLK0 by a F/F or input a divided output to CLKI.
  - Feed back a clock to the CLKI input that is an integral multiple of the reference clock.
  - Do not feed back a clock to the CLKI input that has a frequency lower than the reference clock [Note].

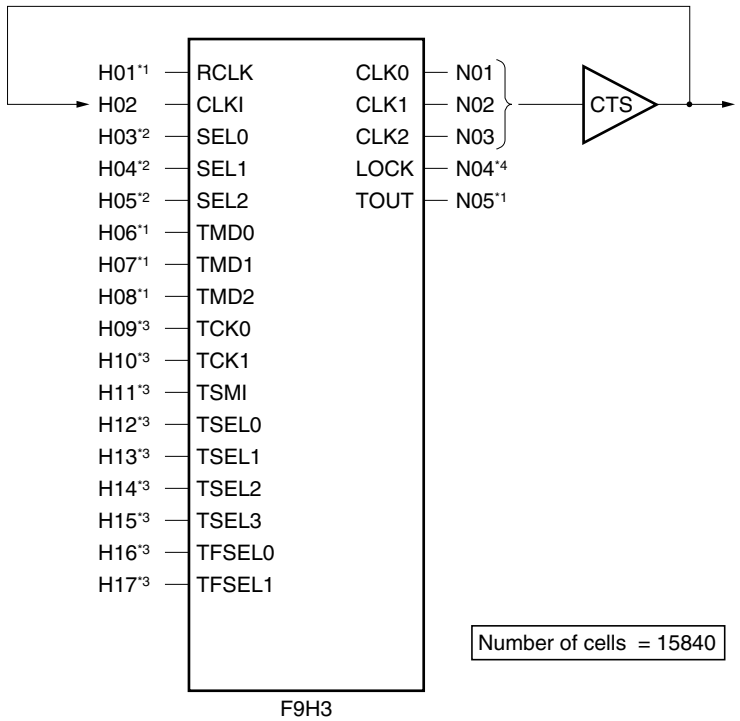
Note The feedback clock cannot be used in such a way that CLK1 is fed back in the ×3 multiplication mode, or CLK2 is fed back in the ×2 multiplication mode.

9.6.3 Digital PLL (F9H3)

(1) Function and operation mode

This section explains the functions and operation modes of the multiplication digital PLL (F9H3).

Figure 9-19. Digital PLL Connection Example (F9H3)



Cautions 1. Pins marked *1 cannot be shared with other LSI pins (dedicated pins).

2. Pins marked *2 do not need to be connected with external pins.

3. Pins marked *3 can be shared with other LSI pins.

4. Pins marked *4 do not need to be connected with external pins.

5. Be sure to connect one of the CLK0 to CLK2 outputs to the CLKI input. (Never divide the outputs by a F/F or input a divided output to CLKI.) If multiple CLKn are used, the phases are not synchronized.

(a) Pin function list

Pin Name	Signal Name	Attribute	Function
H01	RCLK	IN	Reference clock signal
H02	CLKI	IN	Feedback clock signal
H03	SEL0	IN	Multiplication factor setting signal
H04	SEL1	IN	
H05	SEL2	IN	
H06	TMD0	IN	Test mode select signal
H07	TMD1	IN	
H08	TMD2	IN	
H09	TCK0	IN	Test mode clock input signal
H10	TCK1	IN	
H11	TSMI	IN	Test mode switching signal
H12	TSEL0	IN	Test mode multiplication factor setting signal
H13	TSEL1	IN	
H14	TSEL2	IN	
H15	TSEL3	IN	
H16	TFSEL0	IN	Test mode setting signal
H17	TFSEL1	IN	
N01	CLK0	OUT	Multiplication clock output signal
N02	CLK1	OUT	Multiplication clock output signal (2-division output)
N03	CLK2	OUT	Multiplication clock output signal (4-division output)
N04	LOCK	OUT	Lock signal
N05	TOUT	OUT	NEC test mode output signal

(b) Operation truth table

RCLK	TCKn	SELn	TSELn	TFSEL1	TFSEL0	TMD2	TMD1	TMD0	TSMI	CLKn	LOCK	TOUT	Mode
A	X	√	X	X	X	0	0	0	X	A	LOCK[Note 1]	0	PLL mode[Note 2]
X	X	√	X	X	X	0	X	1	X	0	0	0	Reset mode
A	X	√	X	X	X	0	1	0	X	A	0	0	Through path mode[Note 3]
X	X	√	X	X	X	1	0	0	X	0	0	0	Stop mode
A	√	X	√	0	0	1	0	1	√	0	X	TEST	NEC test mode
A	√	X	√	0	1	1	0	1	√	0	X	TEST	
A	√	X	√	1	0	1	0	1	√	0	X	TEST	
A	√	X	√	1	1	1	0	1	√	0	X	TEST	
A	√	X	√	0	0	1	1	0	√	0	X	TEST	
A	√	X	√	0	1	1	1	0	√	0	X	TEST	
A	√	X	√	1	0	1	1	0	√	0	X	TEST	
A	√	X	√	1	1	1	1	0	√	0	X	TEST	
A	√	X	√	0	0	1	1	1	√	0	X	TEST	
A	√	X	√	0	1	1	1	1	√	0	X	TEST	
A	√	X	√	1	0	1	1	1	√	0	X	TEST	
A	√	X	√	1	1	1	1	1	√	0	X	TEST	

Note 1. This is 1 when the phase is locked (when the phase of RCLK and CLKI is synchronized).

2. Multiplied A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

3. A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

Remark A, √: Indicates that the selected mode can be used.

Reset mode setting

Set reset mode by setting TMD2 = 0, TMD1 = X, and TMD0 = 1 (X is either 0 or 1). To change the reset mode to PLL mode, set TMD (2:0) as follows.

Reset mode

TMD2	TMD1	TMD0
0	0	1

PLL mode

TMD2	TMD1	TMD0
0	0	0

To change the reset mode to through path mode, set TMD (2:0) as follows.

Reset mode

TMD2	TMD1	TMD0
0	1	1

Through path mode

TMD2	TMD1	TMD0
0	1	0

By setting as shown above, only one pin needs to be used to change the mode.

(c) Multiplication factor settings

Set the multiplication factor by SELn (SELn can also be clamped to F091).

Multiplication factor	SEL2	SEL1	SEL0	Usable Frequency Band (RCLK)
1	0	0	0	25 to 100 MHz
2	0	0	1	25 to 100 MHz
3	0	1	0	25 to 66.6 MHz
4	0	1	1	25 to 50 MHz
5	1	0	0	25 to 40 MHz
6	1	0	1	25 to 33.3 MHz
7	1	1	0	25 to 28.5 MHz
8	1	1	1	25 MHz

Caution Can only be used within the above shown frequency band; other frequencies cannot be used.

(2) Electrical characteristics

The electrical specifications of the digital PLL (F9H3) are shown in Table 9-10.

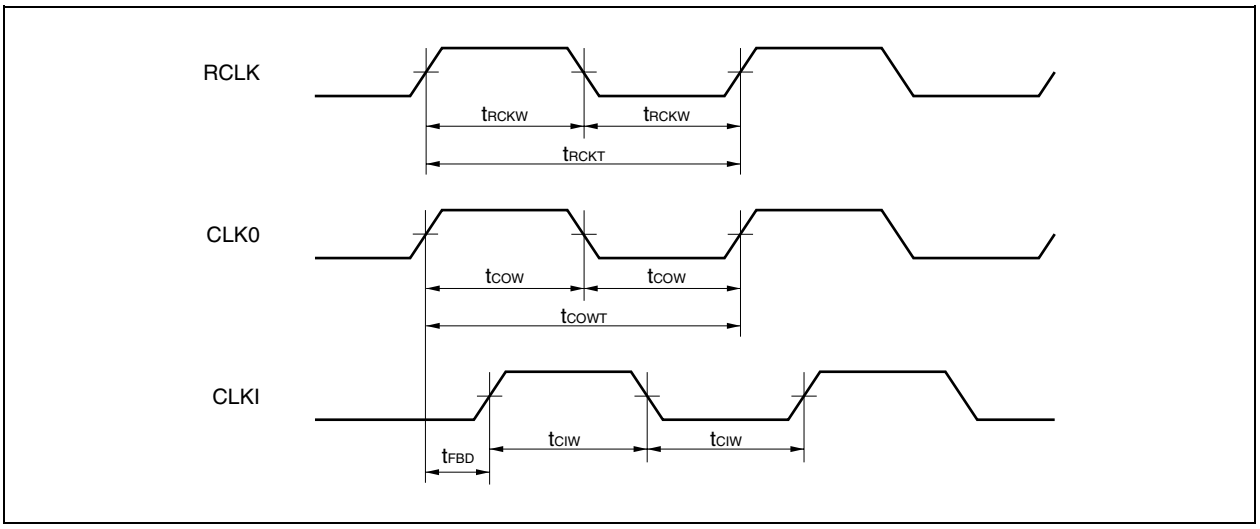
Table 9-10. AC Characteristics (F9H3)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
RCLK frequency	t_{RCKT}	25.0		100.0	MHz	When × 1 is set
		25.0		100.0	MHz	When × 2 is set
		25.0		66.6	MHz	When × 3 is set
		25.0		50.0	MHz	When × 4 is set
		25.0		40.0	MHz	When × 5 is set
		25.0		33.3	MHz	When × 6 is set
		25.0		28.5	MHz	When × 7 is set
		25.0		-	MHz	When × 8 is set
RCLK input allowable jitter	t_{RCKJ}			700	ps	
Power supply allowable fluctuation width				V_{DD} ±0.3	V	Peak- to-peak
Input duty	t_{CIW}			50 ±5	%	
RCLK pulse width	t_{RCKW}	2.8			ns	
CLKI pulse width	t_{SIW}	2.0			ns	
Output jitter	t_{JITT}			600[Note]	ps	Fluctuation of the power supply caused by noise: 200 mV (peak-topeak) or less
Output duty	t_{COW}	45		55	%	
Through path mode delay	t_{THR}	0.886		1.958	ns	CLK0 output
	t_{THL}	0.893		1.979	ns	CLK0 output
	t_{THR}	0.845		1.853	ns	CLK1 output
	t_{THL}	0.845		1.909	ns	CLK1 output
	t_{THR}	0.845		1.853	ns	CLK2 output
	t_{THL}	0.845		1.909	ns	CLK2 output
CTS delay restriction	t_{FBD}			8.22	ns	
Lead-in time	t_{LOCK}			2116	RCLK	
Steady phase error	t_{OFF}			±0.1	ns	No input jitter
Reset pulse width	t_{RSTW}	5			ns	
Output stop time	t_{STOP}	2		4	t_{COW}	
Power consumption	P_{PLL}		50		mW	

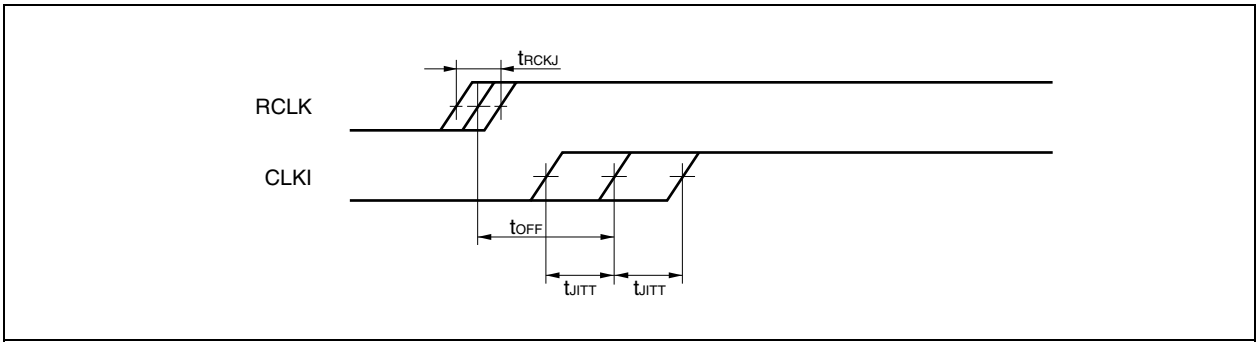
Note The output jitter when the input jitter is 80 ps or less

If the input jitter exceeds 80 ps, add the input jitter to the output jitter value.

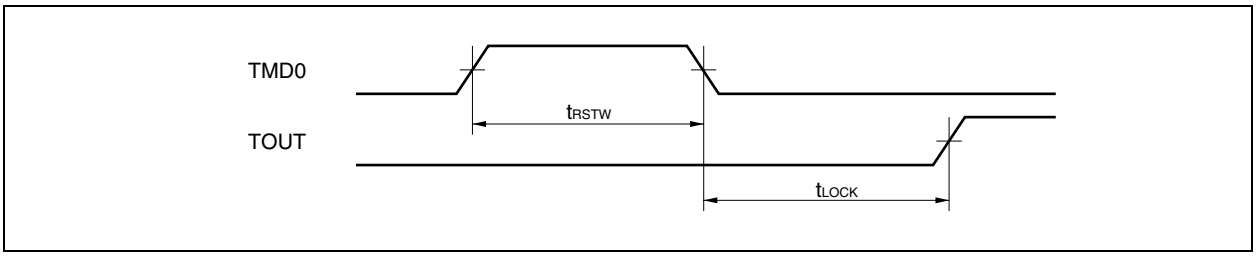
• Input and output waveforms



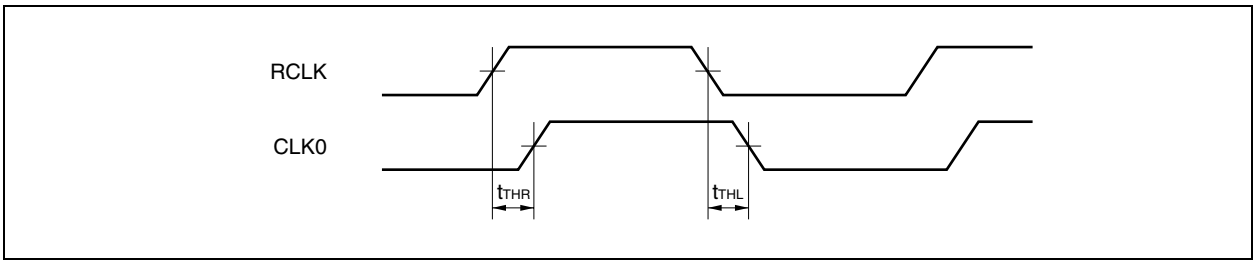
• Jitter and steady phase error



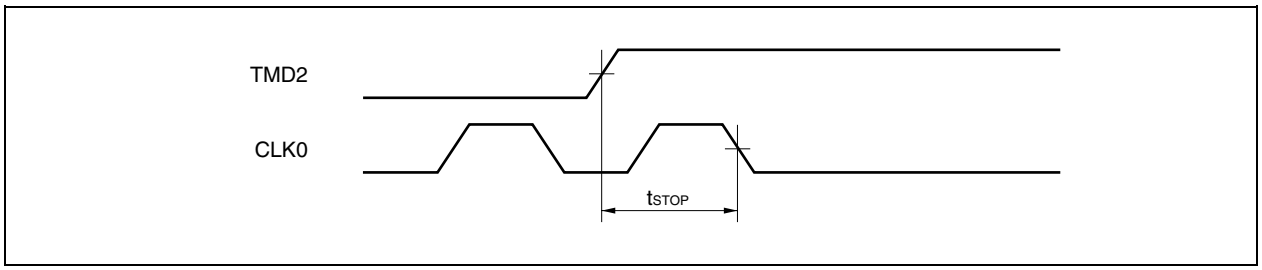
• Lead-in time and reset mode



• Through path mode



• Output stop mode

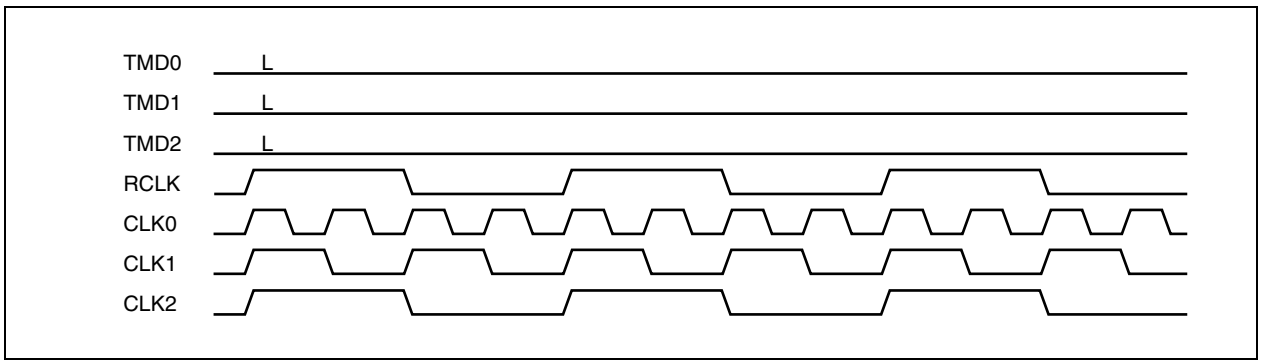


(3) Digital PLL operation

(a) PLL mode

In this mode, the phase of RCLK is synchronized with the phase of CLKn, and the clock set by the multiplication factor setting signal (SELn) is output.

[Waveform when x4 is set in PLL mode]



(b) Reset mode

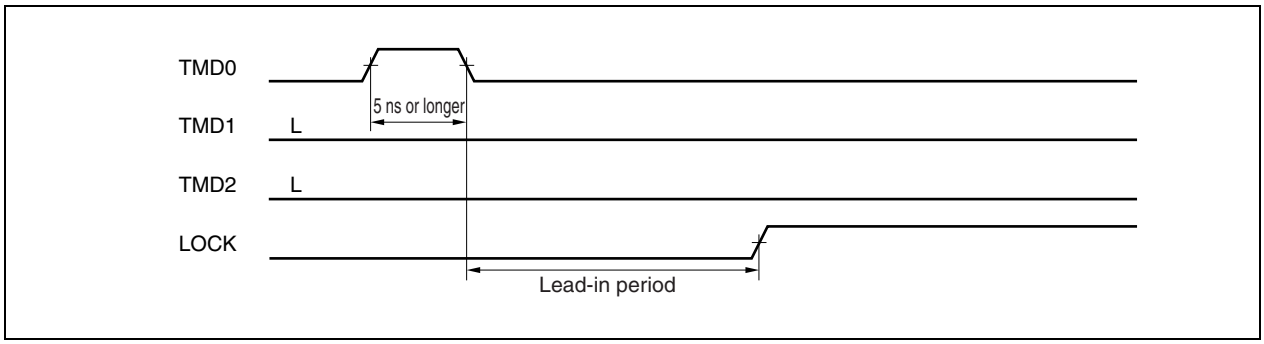
This mode is used to reset the entire digital PLL. Be sure to execute the reset mode after power application.

Although the timing of setting reset mode is not prescribed, set the reset mode for at least 5 ns.

Whether inputting RCLK or not during reset mode does not affect the operation.

The digital PLL locks within the lead-in period after reset mode is released.

[Waveform at reset mode]

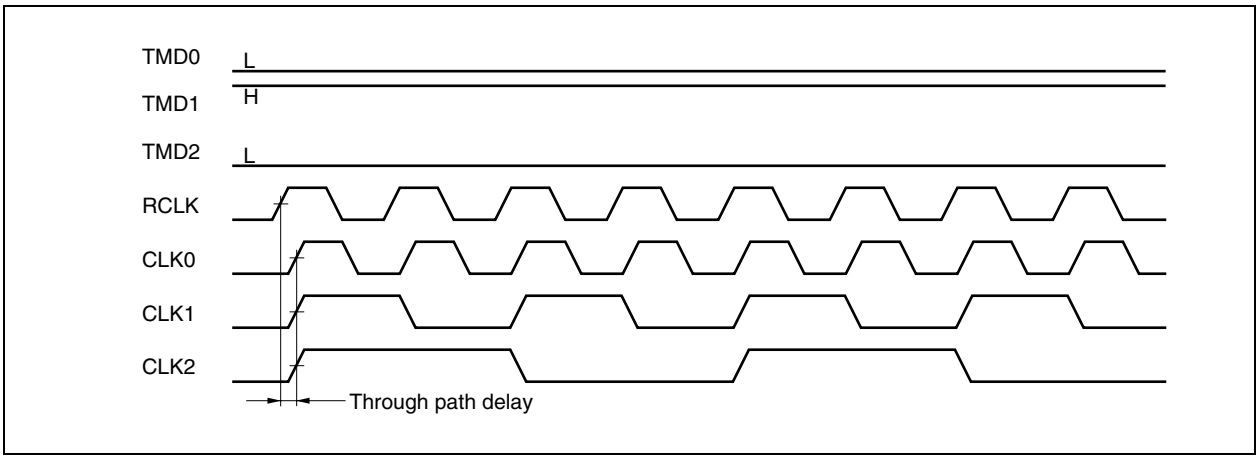


(c) Through path mode

This mode is used to test the user circuit that is placed in the stage following the digital PLL. CLK0 is output later than RCLK by the amount of through path delay (In through path mode, RCLK = CLK0 regardless the multiplication factor).

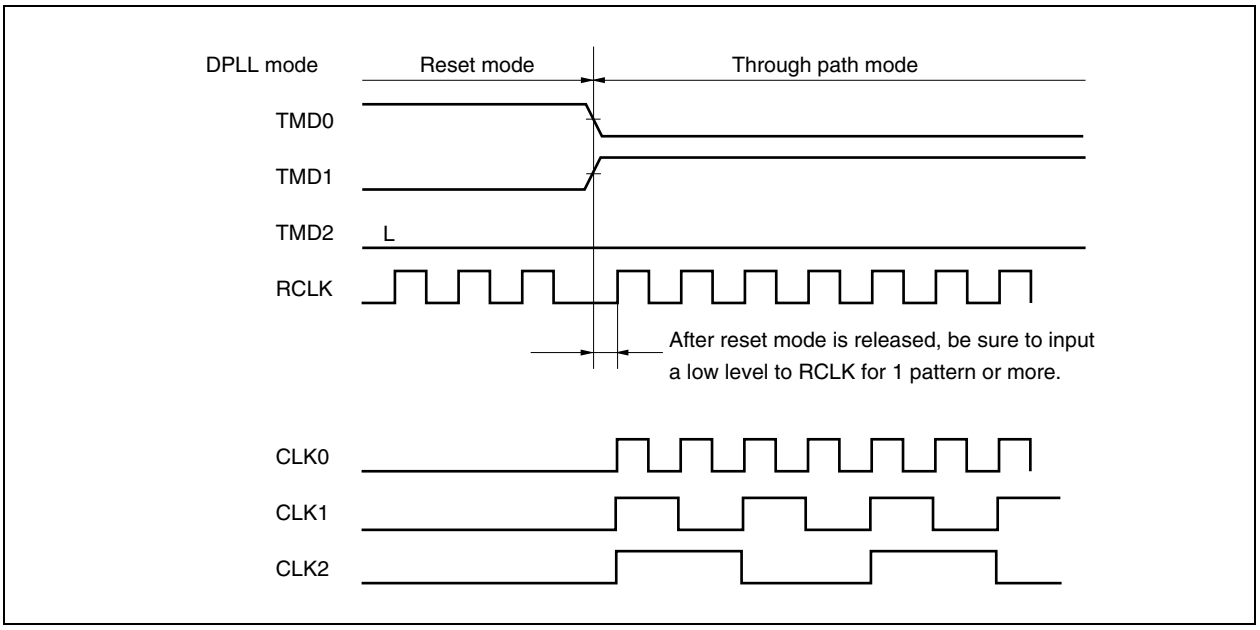
The delay time in the AC ratings does not include the delay value of the clock tree, etc.

[Waveform of through path output]



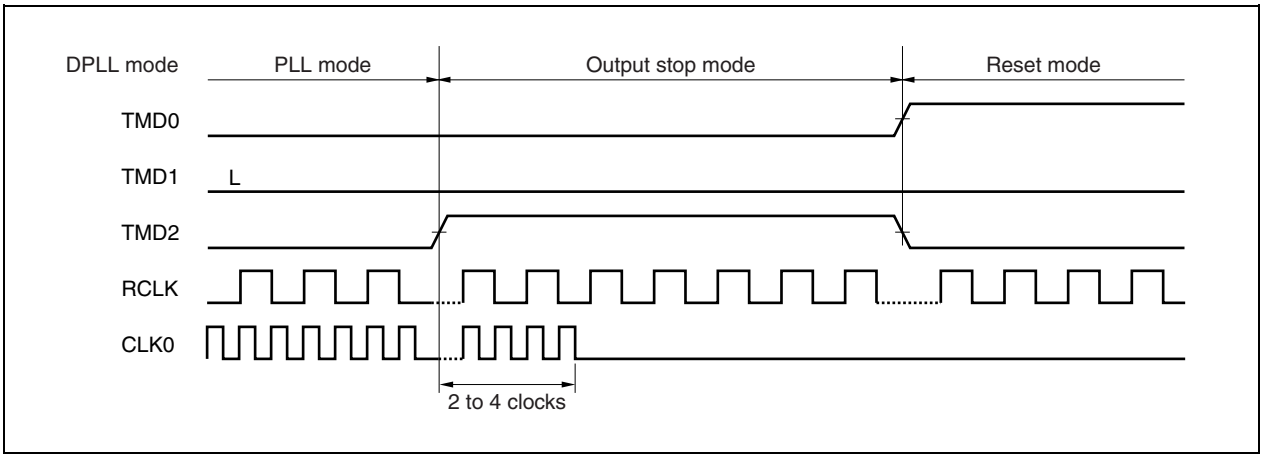
• Caution when setting the F9H3 type to through path mode

Always set through path mode from reset mode.



(d) Output stop mode

This mode is used to fix the CLK0 output to low. When 2 to 4 clocks have elapsed after the output stop mode is set, CLK0 is fixed to low level without generating a spike. Although the timing of setting stop mode is not prescribed, be sure to execute the reset mode after the output stop mode is released.



(4) Connection rules

- Be sure to set through path mode and confirm the connection before executing simulation. Take care with the setting and connection of each pin since this is not simulation under the actual usage conditions.
- The external input buffer FI0P or FI0Q must be used for RCLK input. Use FI0P for the 3 V interface and FI0Q for the 5 V interface.
- Make sure that no spike noise is input to the RCLK, TMD0 to TMD2 input pins.
- Allocate the digital PLL at the corner (any of the four corners is acceptable).
- Do not place RAM or ROM near the digital PLL.
- Place GNDs for both pins next to the pin at which RCLK is placed.
- Place additional GNDs to reduce external buffer noise and do not place a high driving buffer (e.g. GTL+) near the digital PLL.
- Be sure to connect a clock driver or CTS to the CLK0 to CLK02 outputs, and either of the outputs to the CLKI input of the digital PLL (F9H3) (unused CLKn outputs can be left open). However, when the output of CLKn is divided by a F/F, etc., do not connect the divided output to the CLKI input of the digital PLL (F9H3).
- Feed back a clock that is an integral multiple of the reference clock to the CLKI input. Do not feed back a clock to the CLKI input that has a frequency lower than the reference clock.
- Connect Schmitt buffers to directly input TMD0 to TMD2 from external pins. Make sure that no spike noise is input to the TMD0 to TMD2 pins.
- Because the digital PLL (F9H3) is tested as a standalone unit, design the connection so that pins other than CLKI, SEL0 to SEL2 and CLK0 to CLK2 can be input/output from an external pin (TCK0, TCK1, TSEL0 to TSEL3, TFSEL0 and TFSEL1 can be shared with another external pin). RCLK, TCK0, and TCK1 cannot be shared by using a bidirectional buffer.
- The output clock cannot be guaranteed if any of the following conditions apply. Be sure to execute the reset mode.
  - After power application
  - Power supply is out of the rated range (3.3 ±0.3 V)
  - When mode is shifted between PLL mode, through path mode, and output STOP mode
  - When the multiplication factor setting (SELn) is changed

  - When the input AC ratings in **Table 9-10 AC Characteristics (F9H3)** are not satisfied

- Set the reset mode for at least 5 ns.
- After power application, release the reset mode when the power supply voltage, input clock pulse width, duty, and frequency are stabilized at 3.3 ±0.3 V, 2.8 ns or more, 50 ±5%, and ±0.5 ns of the frequency to be used, respectively.
- Be sure to execute the reset mode when the output stop mode is released.
- The waveform of the CLK1 output is equal to 1/2 the CLK0 output waveform.
- The waveform of the CLK2 output is equal to 1/4 the CLK0 output waveform.
- In PLL mode, the output clock is unstable until the digital PLL (F9H3) locks (TOUT changes from L to H). Consequently, operation cannot be guaranteed.
- Supply the power supply voltage within the specifications (3.3 ±0.3 V) so that the fluctuation of the power supply caused by noise is 200 mV (peak-to-peak) or less. Attach a bypass capacitor of 22 μF or more between V_{DD} and GND for the power supply block on a board on which an LSI is mounted.
- After reset mode is released, be sure to input a ±0.5 ns cyclic variation with a 2.8 ns or longer pulse width at a duty of 50 ±5%. If an unstable clock exceeding this range is input to RCLK, the PLL is automatically shifted to reset mode, and the output clock may be unstable until the PLL locks.
- When reset mode is set or released, spike noise may be generated at the output clock.
- A special request is needed when a circuit (e.g. power-on-reset circuit) is placed between an input buffer and TMD0 to TMD2.
- The output clock cannot be guaranteed if RCLK stops. Be sure to input RCLK continuously.
- Cautions on setting feedback clocks
  - Be sure to connect CTS to the CLK0 to CLK2 outputs, and that output to the CLKI input of the digital PLL (F9H3).
  - Do not divide outputs such as CLK0 by an F/F or input a divided output to CLKI.
  - Feed back a clock to the CLKI input that is an integral multiple of the reference clock.
  - Do not feed back a clock to the CLKI input that has a frequency lower than the reference clock[Note].

Note The feedback clock cannot be used in such a way that CLK1 is fed back in the ×3 multiplication mode, or CLK2 is fed back in the ×2 multiplication mode.

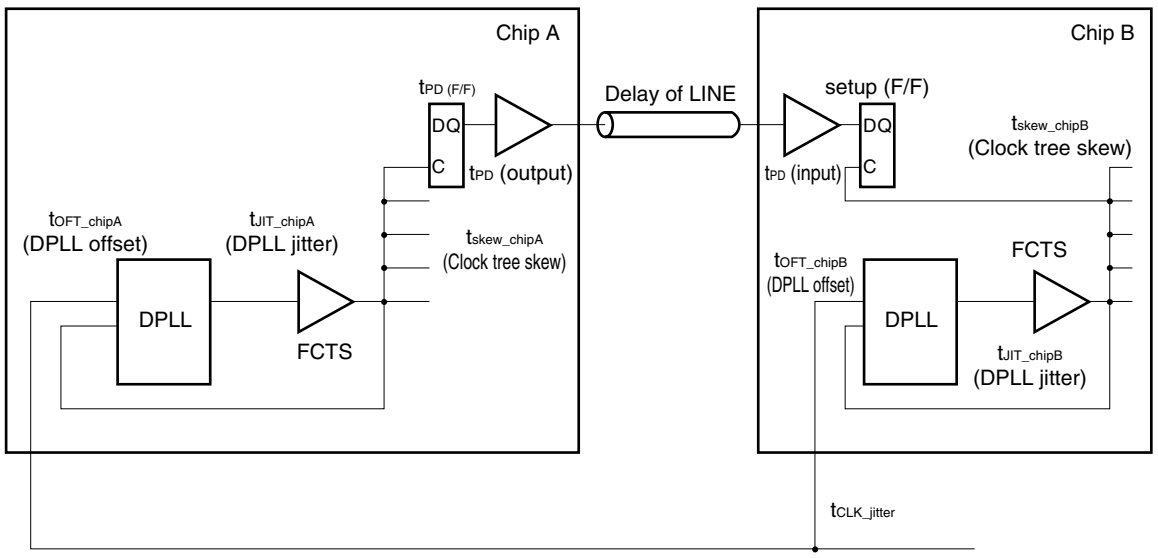
9.6.4 Signal transfer between devices

When signals are transmitted between devices with an on-board digital PLL, the maximum operating frequency is determined by taking the clock skew and jitter into consideration. This section explains the calculation of the maximum operating frequency. If shift registers are configured between devices, as shown in the circuit in Figure 9-20, the minimum period of the clock signal is expressed as follows:

Calculation equation:

$$T_{CLK} = t_{CLK\_\ jitter} + 0.5 \times t_{JIT\_chipA} + 0.5 \times t_{skew\_chipA}$$
$$+ t_{PD}(F/F) + t_{PD}(output) + Delay\ of\ LINE + t_{PD}(input) + setup(F/F)$$
$$+ 0.5 \times t_{JIT\_chipB} + 0.5 \times t_{skew\_chipB} + t_{OFT\_chipA} + t_{OFT\_chipB}$$

Figure 9-20. Signal Transfer Between Device



Remark DPLL: Digital PLL

9.6.5 Generating test pattern

The PLL operation cannot be reproduced by normal delay simulation. For shipment inspection of embedded arrays with a digital PLL, therefore, the operations of the circuits other than the digital PLL are checked with the digital PLL bypassed, and the operation of the digital PLL is checked separately. The test pattern for the digital PLL is prepared by NEC Electronics. The user is requested to observe the connection rules of the digital PLL and notes on generating the test pattern.

Be sure to inform NEC Electronics of the names of the pins to which the digital PLL is to be connected. NEC Electronics supplies 4 K of test patterns for checking the digital PLL. Therefore, the maximum test pattern length the user can use is the difference between the maximum test pattern length and 4 K.

The RCLK pin must not be specified as a clock pin.

(1) Normal simulation

The signals of the TMD0, TMD1, and TMD2 pins must be as follows. The user can use these signals only in the through path and reset modes.

Operation Mode	TMD0	TMD1	TMD2
Through path	0	1	0
Reset	1	0	0

(2) Digital PLL initial pattern[Note 1]

To check the operation of the digital PLL alone, use the digital PLL test pattern file available from NEC Electronics. However, when there are gates (logic) between the digital PLL test pins and the digital PLL main unit[Note 2], the patterns for checking direct access to the digital PLL test pins and main body and the test patterns (initialization patterns) for determining the expected output values of the blocks other than the digital PLL (such as flip-flops and I/O buffers) must be prepared by the user.

Note 1. • Use only in the through path and reset modes.
- Ensure that only the final pattern of output buffers other than that of TOUT is “don’t care”.
- Depending on the test to be performed, RCLK is directly output to TOUT (the only monitor pin), so do not specify the RCLK pin for the clock.
- Do not describe timing relationships.

2. In this case, please contact NEC Electronics.

9.6.6 Static timing analysis of circuits using digital PLL

The digital PLL STA model is currently only available for the through mode, so care is needed when verifying the timing between external inputs and flip-flops, flip-flops and flip-flops, and flip-flops and external outputs in lock mode.

For the verify

Figure 9 21. Example of Circuit Configuration When PLL Used

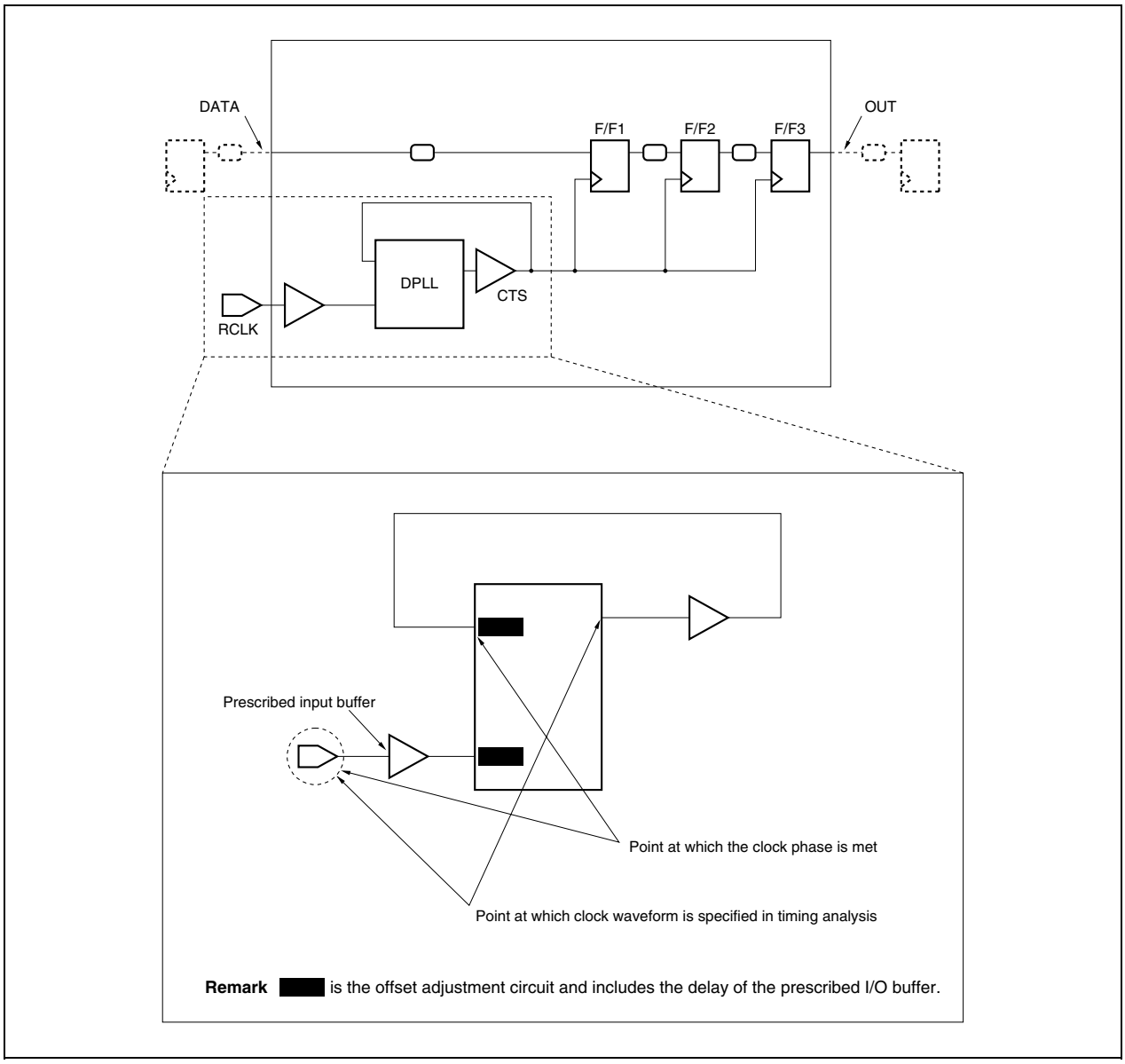


Table 9-11. Delay Values of Digital PLL Offset Adjustment Circuit (F9E4)

Type	Maximum Delay Value
F9E4H	-580
F9E4G	-483
F9E4F	-390
F9E4E	-309
F9E4D	-233
F9E4C	-146
F9E4B	-58
F9E4A	26
F9E4I	110
F9E4J	198
F9E4K	285
F9E4L	361
F9E4M	442
F9E4N	535
F9E4O	632

Remark The unit is 1 ps/unit.

Table 9-12. Delay Values of Digital PLL Offset Adjustment Circuit (F9H2)

Type	Maximum Delay Value
F9H2O	-562
F9H2N	-466
F9H2M	-383
F9H2L	-305
F9H2K	-217
F9H2J	-125
F9H2I	-37
F9H2A	45
F9H2B	127
F9H2C	215
F9H2D	307
F9H2E	395
F9H2F	473
F9H2G	556
F9H2H	652

Remark The unit is 1 ps/unit.

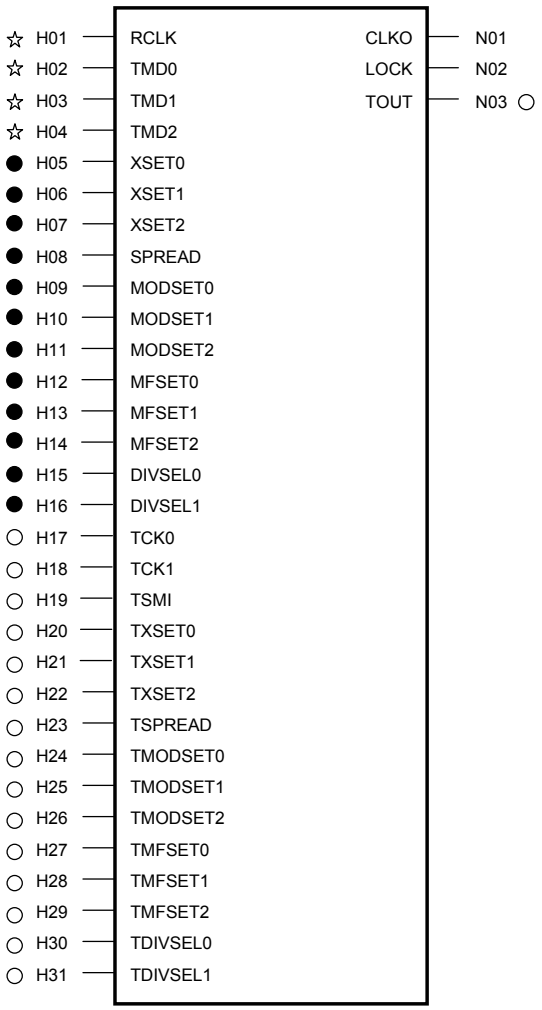
9.7 SSCG

9.7.1 F9H4SSCG

(1) Functions and operation modes

This macro has a multiplication function and SSCG (Spread Spectrum Clock Generation) function.
The SSCG function supplies a frequency modulated clock. By using this modulated clock, it is possible to reduce the EMI (Electromagnetic Interference) generated by the LSI. This macro cannot be used to obtain a constant modulation frequency. For other cautions, see **(4) Cautions**.

Block name: F9H4SSCG
Number of cells: 17550



F9H4SSCG

Cautions 1. The ☆pins are dedicated pins. Configure the system so that input can be performed directly from outside the LSI.

2. The ●pins are mode setting pins. Clamping these pins with F091 is not a problem.

3. The ○pins can be shared with other user pins, but in the NEC test mode, use a configuration such that input and output can be performed directly from outside the LSI.

(a) Pin function list

Pin Name	Symbol	IN/OUT	Function
H01	RCLK	IN	Reference clock signal
H02	TMD0	IN	Mode setting signal
H03	TMD1	IN	
H04	TMD2	IN	
H05	XSET0	IN	Internal multiplication setting signal
H06	XSET1	IN	
H07	XSET2	IN	
H08	SPREAD	IN	Modulation method setting signal (D-S = 0, C-S = 1)
H09	MODSET0	IN	Modulation degree setting signal
H10	MODSET1	IN	
H11	MODSET2	IN	
H12	MFSET0	IN	Modulation frequency multiplier setting signal
H13	MFSET1	IN	
H14	MFSET2	IN	
H15	DIVSEL0	IN	Output frequency division setting signal
H16	DIVSEL1	IN	
H17	TCK0	IN	Test input signal
H18	TCK1	IN	
H19	TSMI	IN	
H20	TXSET0	IN	Test multiplication setting signal
H21	TXSET1	IN	
H22	TXSET2	IN	
H23	TSPREAD	IN	Test modulation method setting signal
H24	TMODSET0	IN	Test modulation degree setting signal
H25	TMODSET1	IN	
H26	TMODSET2	IN	
H27	TMFSET0	IN	Test modulation frequency multiplier setting signal
H28	TMFSET1	IN	
H29	TMFSET2	IN	
H30	TDIVSEL0	IN	Test output frequency division setting signal
H31	TDIVSEL1	IN	
N01	CLKO	OUT	Multiplied output clock signal
N02	LOCK	OUT	Lock signal
N03	TOUT	OUT	Test output signal l

(b) Operation truth table

Input Pin Name / Mode	RCLK	TMD [2:0]	XSET [2:0]	DIVSEL [1:0]	SSCG Setting	Test Setting
SSCG mode	Fref Note1	000	N1 Note2	N2 Note3	B Note4	X
Reset mode	X	0X1 Note5	X	X	X	X
Through path mode	A Note6	010	X	X	X	X
NEC test mode	TIN Note7	TIN Note7	X	X	X	TIN Note7

output Pin Name / Mode	CLKO	LOCK	TOUT
SSCG mode	Fref × N1 × N2	LOCK Note8	0
Reset mode	0	0	0
Through path mode	A Note6	0	0
NEC test mode	0	0	TOUT Note7

Notes 1. Indicates the input clock frequency.

2. This is the internal multiplier setting value. For details, refer to **(c) Internal multiplier setting**.

3. This is the output frequency division setting value. For details, refer to **(d) Output frequency division setting**.

4. This is the SSCG setting value (SPREAD, MODSET [2:0], MFSET [2:0]).
For details, refer to **(e) Modulation method**, **(f) Modulation degree setting**, and **(g) Modulation frequency multiplier setting**.

5. During reset mode setting, set TMD1 to "0" or "1".

6. Indicates a signal. In the through path mode, the signal input to RCLK is output to CLKO with a delay that corresponds to the through path delay.

7. Indicates the test input signal (TIN) and the test output signal (TOUT).
The test setting pins indicate TCK0, TCK1, TSMI, TXSET [2:0], TSPREAD, TMODSET [2:0], TMFSET [2:0], and TDIVSEL [1:0].

8. In the unlocked state, LOCK = "0", and in the locked state (output of set frequency), LOCK = "1".

9. Input either "0" or "1" for "X" of the input pin.

(c) Internal multiplier setting

The internal multiplier is set with the XSET [2:0] pins. This value becomes the internal oscillation multiplier.
Set this value so that 45 MHz ≤ (RCLK input frequency × internal multiplier) ≤ 100 MHz.
CLKO output frequency = Internal oscillation frequency × Output frequency division.

XSET [2:0]	Internal Multiplier [N1]
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

(d) Output frequency division setting

The output frequency division is set with the DIVSEL [1:0] signals.

DIVSEL [1:0]	Frequency Division Value [N2]
0X	1/1
10	1/2
11	1/4

If the internal multiplier is 4 and the output frequency division is 1/2, the output clock's multiplier in relation to the input clock is $4 \times 1/2 = 2$.

(e) Modulation method

The modulation method is set with the SPREAD signal.

SPREAD	Modulation Method
0	Down-Spread
1	Center-Spread

Down-spread performs modulation so that the frequency does not exceed the output clock during nomodulation.

Center-spread performs modulation so that the output clock frequency during no-modulation is middlecentered.

(f) Modulation degree setting

The modulation degree is set with the MODSET [2:0] signals. The set value is the peak-to-peak value.

MODSET [2:0]	Modulation Degree
000	No modulation
001	Approx. 0.5% of output frequency
010	Approx. 1.0% of output frequency
011	Approx. 1.5% of output frequency
100	Approx. 2.0% of output frequency
101	Approx. 3.0% of output frequency
110	Approx. 4.0% of output frequency
111	Approx. 5.0% of output frequency

Note that synchronization with RCLK is not done even during no-modulation.

(g) Modulation frequency multiplier setting

The modulation frequency multiplier is set with the MFSET [2:0] signals.

MFSET [2:0]	n	Modulation Frequency Multiplier
000	0	1/1
001	1	1/2
010	2	1/3
011	3	1/4
100	4	1/5
101	5	1/6
110	6	1/7
111	7	1/8

The EMI reduction effect varies according to this setting value.
The modulation frequency used as reference is determined by the reference clock frequency, the internal multiplier, and the modulation degree.

[Recommended modulation frequency setting]

$$(5.24E - 4) \times (\text{Reference clock frequency [MHz]})^2 \times (\text{Internal multiplier})/\text{Modulation degree [\%]} - 1$$

Perform this setting with MFSET [2:0] so as to approximate the value of n. However, ($0 \leq n \leq 7$)

Example When RCLK = 25 MHz, internal multiplier = 4, modulation degree = 2%
$5.24E - 4 \times 25^2 \times 4/2 - 1 = -0.345$,
so set n = 0 (MFSET [2:0] = "000").

(2) Electrical specifications

Table 9-13. Recommendation for Using Condition (F9H4SSCG)

Parameter	Symbol	MIN	TYP	MAX	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Junction temperature	T_J	–40		+125	°C
RCLK input duty	t_{RCKD}	30		70	%
Reset pulse width	t_{RSTW}	5.0			ns

Table 9-14. AC Speciation (F9H4SSCG) (No Power Supply Noise)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Internal oscillation frequency	f_{CLK0}	45		100	MHz	Input clock frequency × internal multiplier
Output duty	t_{CLKD}	45		55	%	–
Multiplication cycle error	t_{CKTERR}			±100	ps	During no modulation: No output frequency division
				±150		During no-modulation: 1/2 output frequency division
				±200		During no-modulation: 1/4 output frequency division
Output cycle jitter Note1	t_{CLKPJ}			±100	ps	During no modulation: No output frequency division
				±120		During no-modulation: 1/2 output frequency division
				±140		During no-modulation: 1/4 output frequency division
Output cycle-to-cycle jitter	t_{CLKCJ}			±100	ps	No output frequency division
				±120		1/2 output frequency division
				±140		1/4 output frequency division
Lead-in time Note3	t_{LOCK}			34784	RCLK	–
Through path delay	t_{SIM}	742		2816	ps	HH
		804		3182		LL
Modulation degree error	t_{DERR}			+0.5	%	Value subtracting jitter during no-modulation
Current consumption	P_{OW}			**Note 2**	mA	–

Note 1. If noise is present in V_{DD} or GND, jitter is added with the following equation.
t_{CLKNJ} [ps] = 0.33 × Output cycle [ns] × Noise amplitude [mV] (ps)

2. The current consumption is expressed by the following equations.
Worst condition: Current consumption [mA] = f_{IN} [MHz] × 0.199 + f_{OSC} [MHz] × 0.278 (mA)
Typical condition: Current consumption [mA] = f_{IN} [MHz] × 0.170 + f_{OSC} [MHz] × 0.237 (mA)
f_{IN} = RCLK input frequency, f_{OSC} = Internal oscillation frequency

3. Lead-in time
The lead-in time indicates 34784 clock signals are input for RCLK.

<R> **(a) Calculating the modulation frequency**

Number of modulation STEPs = oscillation frequency [kHz] × modulation degree [%]/100/STEP value [PS]

STEP value [PS]: MAX = 9.82, MIN = 3.60, TYP = 6.71

Modulation frequency [kHz] =
input RCLK [kHz]/(16/3 × number of modulation STEPs × 2 × n + 1 value of MFSET)

Example: Number of modulation STEPs
(oscillation frequency = 32,000 [kHz], modulation degree = 0.5 [%], STEP value = 9.82 [PS] (MAX))
32000 × 0.5/100/9.82 = 16.293
Modulation frequency (input RCLK = 16,000 [kHz], n + 1 value of MFSET = 1)
16000/ (16/3 × 16.293 × 2 × 1) = 92.06

<R> **(b) Calculating various frequencies**

The various frequencies are calculated as described below.
To know long-term frequencies, eliminate the output cycle jitter (t_{CLKPJ}) and power supply noise (t_{CLKNJ}).

Ideal output cycle (t_{IDEAL})
= 1/{input frequency (f_{RCLK}) × internal multiplier (N1) × output frequency division value (N2)}

Remark The meanings of the symbols in the expression are as follows:

- t_{CKTERR}: Multiplication cycle error
- t_{CLKPJ}: Output cycle jitter
- mod: Modulation degree
- t_{DERR}: Modulation degree error
- t_{CLKNJ}: Power supply noise

[During no-modulation]

Maximum output cycle (T_{MAX}) = (t_{IDEAL}) + (t_{CKTERR}) + (t_{CLKPJ}) + (t_{CLKNJ})

Minimum output cycle (T_{MIN}) = (t_{IDEAL}) – (t_{CKTERR}) – (t_{CLKPJ}) + (t_{CLKNJ})

[During down-spread modulation]

Maximum output cycle (T_{MAX}) = (t_{IDEAL}) + (t_{CKTERR}) + (t_{CLKPJ}) + (t_{CLKNJ}) + (t_{IDEAL}) × (mod + t_{DERR}) / 100

Minimum output cycle (T_{MIN}) = (t_{IDEAL}) – (t_{CKTERR}) – (t_{CLKPJ}) – (t_{CLKNJ})

[During center-spread modulation]

Maximum output cycle (T_{MAX}) = (t_{IDEAL}) + (t_{CKTERR}) + (t_{CLKPJ}) + (t_{CLKNJ}) + (t_{IDEAL}) × {(mod/2) + t_{DERR}} / 100

Minimum output cycle (T_{MIN}) = (t_{IDEAL}) – (t_{CKTERR}) – (t_{CLKPJ}) – (t_{CLKNJ}) – (t_{IDEAL}) × {(mod/2) + t_{DERR}} / 100

Example: Maximum output cycle (T_{MAX}) during no-modulation under the following conditions

Input frequency (f_{RCLK}) = 33 [MHz]
Internal multiplier (N1) = 2
Output frequency division (N2) = 0.5
Modulation degree (mod) = 4 [%]
Multiplication cycle error (t_{CKERR}) = 150 [ps]
Output cycle jitter (t_{CLKPJ}) = 120 [ps]
Modulation degree error (t_{DERR}) = 0.5 [%]
Power supply noise (t_{CLKNJ}) = 1 [ps]

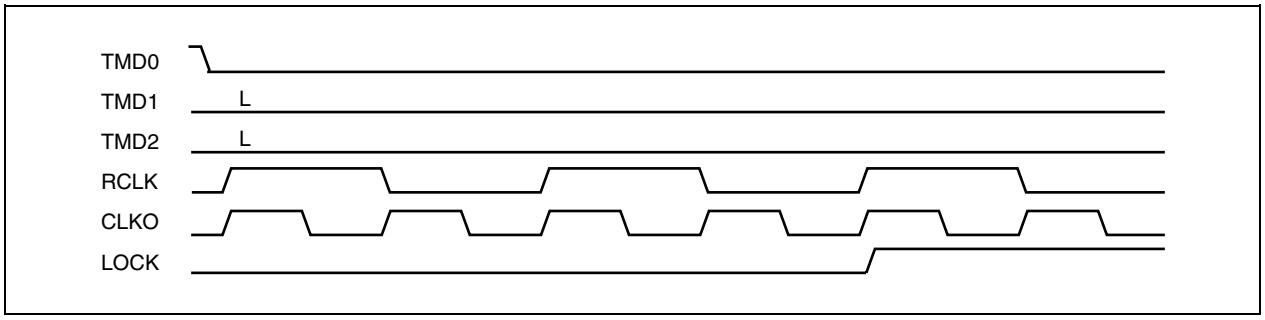
The ideal output cycle (t_{IDEAL}) is $1/0.000033 \times 2 \times 0.5 = 30303.0303$ [ps],
so the maximum output cycle (T_{MAX}) is
30303.0303 + 150 + 120 + 1 = 30574.0303 [ps].
When converted into frequency, it is 32.71 [MHz].

(3) Operation modes

(a) SSCG mode

This mode generates a multiplied output clock in relation to the RCLK frequency. To select this mode, the reset mode must be set and LOCK = "1" is set when the multiplication frequency is generated.

Example When XSET [2:0] = "011", DIVSEL [1:0] = "10" in the SSCG mode



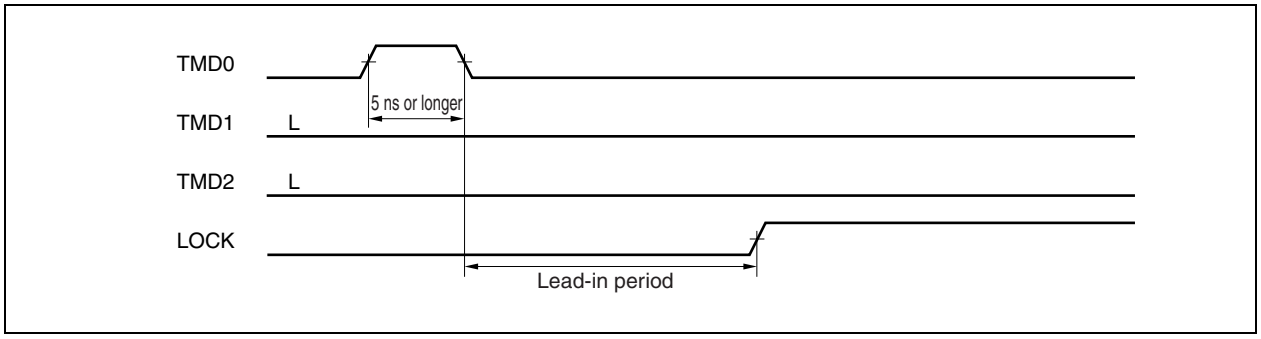
(b) Reset mode

This mode is used to reset the entire macro.

Although the timing of setting reset mode is not prescribed, set the reset mode for at least 5 ns.

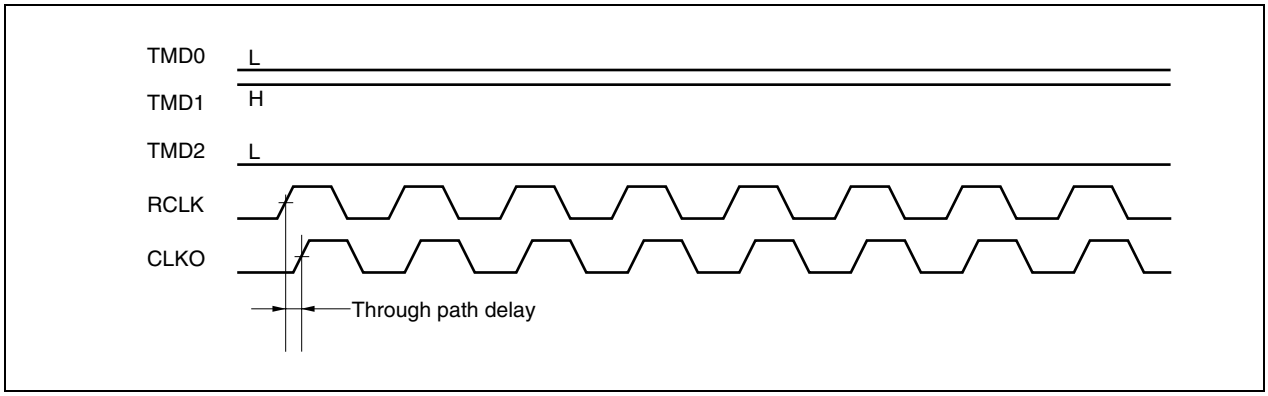
Whether inputting RCLK or not during reset mode does not affect the operation.

LOCK = "1" is set within the lead in time after reset mode has been released.



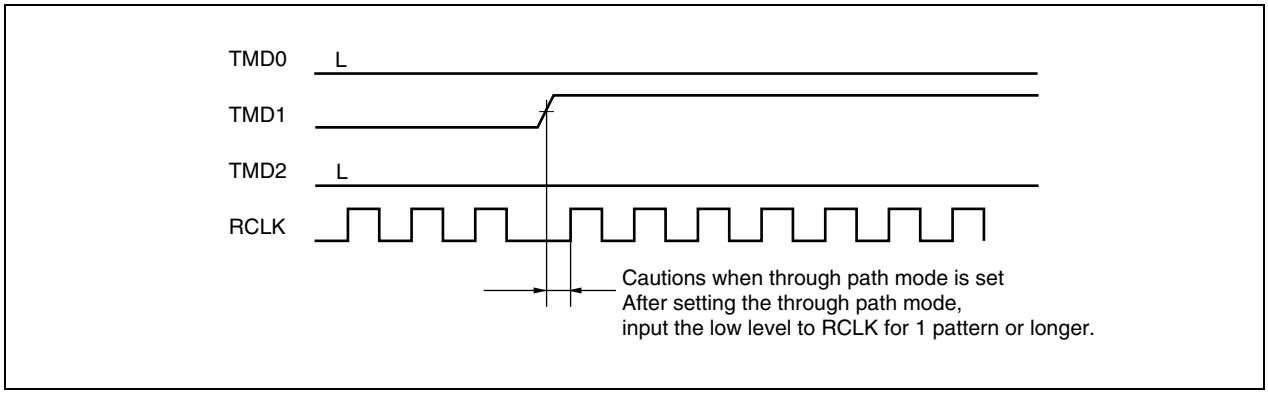
(c) Through path mode

This mode is used to test the user circuit in the stage after the macro or during simulation. RCLK is output to CLKO with a delay that corresponds to the through path delay (output frequency division setting is disabled). The user must perform design in this mode. In this mode, the internal circuits other than the output clock are in the same status as the reset mode.



• Cautions when through path mode is set

After setting the through path mode, input the low level to RCLK for 1 pattern or longer.



(4) Cautions

<R> • The macro is intended for frequency modulation and is not synchronized with the reference clock (RCLK), because the effects of multiplication cycle errors accumulate also during a no-modulation setting. Also, the average frequency does not match with the reference clock.

• As the clock to be used for the LSI, use only one CLKO output.

• During simulation, be sure to perform verification after setting the through path mode. However, since such verification is not done under actual use conditions, carefully perform the various pin settings and connections.

• Take precautions to prevent spike noise from being input to input pins RCLK and TMD [2:0].

• Directly input TMD [2:0] from external pins and connect a Schmitt buffer.

• This macro is to be placed in a chip corner. Do not place RAM or ROM near this macro.

• Place GNDs for both pins next to the pin at which RCLK is placed.

• Place an additional GND as a countermeasure against external buffer noise and do not place a buffer with high drive capability (GTL+, etc.) in the vicinity of this macro.

• To allow stand-alone testing of this macro, make it possible to perform input/output to/from TCK0, TCK1, TSMI, TXSET [2:0], TSPREAD, TMODSET [2:0], TMFSET [2:0], TDIVSEL [1:0], and TOUT pins from external. Sharing with other external pins is possible.

• Shared use through the use of bidirectional buffers is prohibited for RCLK, TCK0, and TCK1.

• If any one of the following conditions is met, be sure to execute the reset mode.

  - After power application
  - If the conditions listed in **Table 9-13 Recommendation for Using Condition (F9H4SSCG)** are not met
  - Before mode is set to SSCG mode
  - When the setting values of XSET [2:0], DIVSEL [1:0], SPREAD, MODSET [2:0] and MFSET [2:0] are changed in the SSCG mode

• Set the reset mode for at least 5 ns when the power supply voltage is 3.3 ±0.3 V and after RCLK has stabilized, following power application.

• Spikes in the output clock may occur when the mode is set to the reset mode and also when the reset mode <R> is released. Configure the circuit so that there are no problems even if spikes occur.

• Since the output clock is unstable until lock occurs (LOCK = L → H) in the SSCG mode, the operation cannot be guaranteed.

• Keep the power supply voltage within the rated range (3.3 ±0.3 V) and keep power supply fluctuations due to noise within 100 mV (peak-to-peak).

• Use a configuration such that RCLK and TMD [2:0] can be directly input from external. (If a circuit (power-on reset circuit, etc.) is inserted between the input buffer and TMD [2:0], a special request is required.)

• Since macro testing is required, when setting the NEC test mode, use a configuration so that test pin input and output can be performed directly from external.

• If RCLK is stopped, the CLKO clock is not guaranteed. Be sure to continuously input RCLK.

<R> • When RCLK is switched from reset mode to through path mode while it is at high level, a short high-pulse width is output to CLKO.

<R> 9.8 Analog PLL

9.8.1 ABPLWFB (Inside Placement Type)

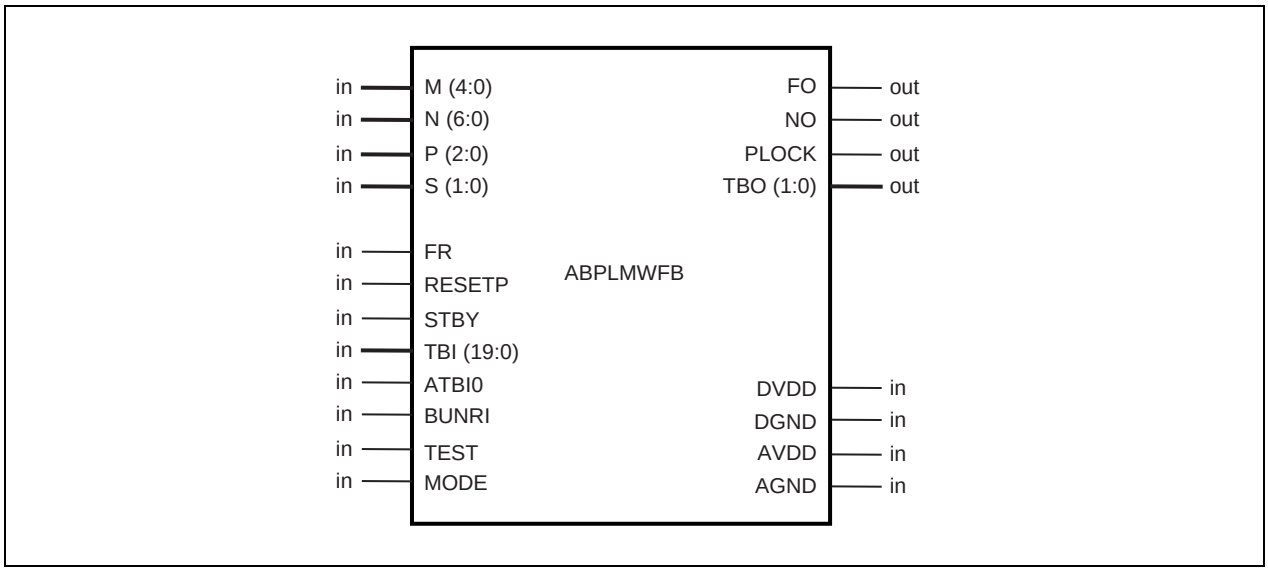
(1) Overview

This macro is analog PLL (hereinafter called APLL) with multiplication function.
The low frequency clock (from 4 MHz on up) can be input to it.
The output clock frequency up to 230 MHz can be output by this macro (APLL). In contrast, the maximum input frequency of the EA-9HD Series internal cells is 100 MHz. If the output clock frequency of the APLL exceeds 100MHz, therefore, please consult NEC Electronics.
There is no skew adjustment function between an input FR pin and output FO pin.

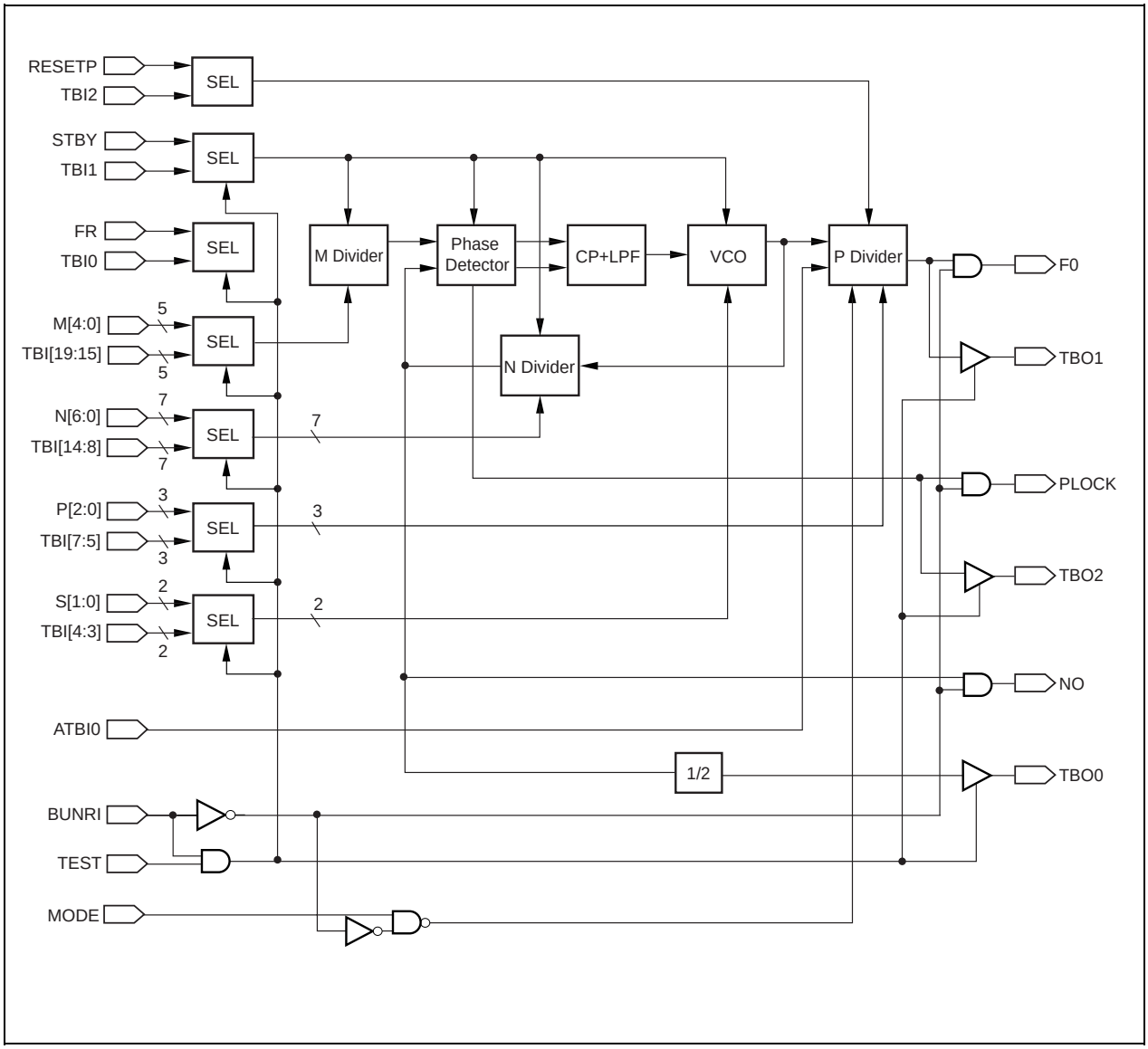
(2) Typical Characteristics and Features

- Macro name: ABPLMWFB (Inside Placement Type)
- Number of cells: 16320
- Supply voltage: 3.3 ±0.3 V
- Operating temperature: –40 to +85°C
- VCO output frequency range: 50 to 230 MHz
- Multiplication ratio: 2 to 128 (N divider)
- Output period jitter: 0.4 ns (peak to peak)
- Output long term jitter: 2.0 ns (peak to peak)
- No external device is needed
- Phase Lock-in indicator output

(3) Symbol diagram



(4) Block diagram



(a) Phase Detector

It outputs a pulse to show progress or delay by detecting the phase difference between two input signals.

(b) CP+LPF (Charge Pump + Low Pass Filter)

It converts the signal from Phase Detector to DC voltage.

(c) VCO (Voltage Control Oscillator)

It outputs the oscillation frequency depending to the LPF output voltage.

(5) Electrical specifications

(a) Absolute maximum ratings (T_A = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{STG}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

(b) Recommended Operating Range (T_A = –40 to +85°C)

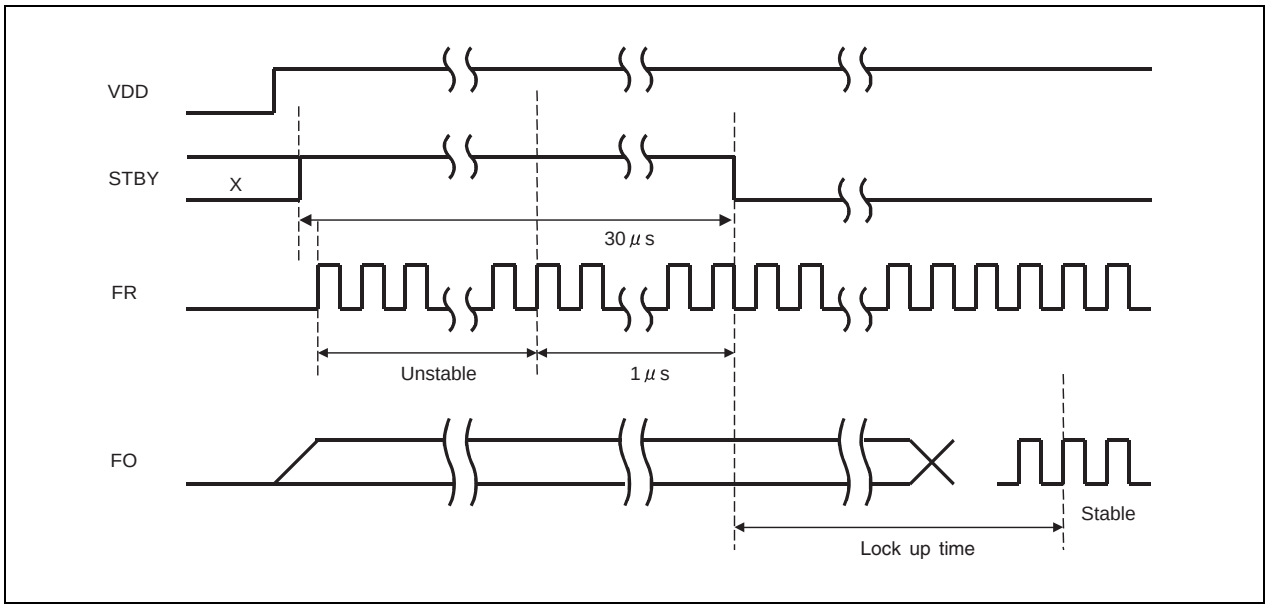
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AV_{DD}		3.0	3.3	3.6	V
Input frequency	f_{std}		4		160	MHz
PFD input frequency	f_{pfd}	f_{std} / m	2		80	MHz
Input duty ratio	I_{duty}		30		70	%
Input rise time	t_r	From 10% to 90% of V_{DD}			1.6	ns
Input fall time	t_f	From 90% to 10% of V_{DD}			1.6	ns
Input high pulse width	t_{pwh}		1.4			ns
Input low pulse width	t_{pwl}		1.4			ns
Divided ratio	m	Multiplication rate = n / (m x p)	2		32	
	n		2		128	
	p		1		8	

(c) Electrical Specifications (T_A = –40 to +85°C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	Operation			20	mA
	I_{DDS}	Standby		10	30	μA
VCO Output frequency	f_{vco}	Selected frequency range using S(1:0)	50		230	MHz
output duty ratio	duty	P(2:0) = 1, 3 or 7	45		55	%
Output period jitter	t_{pj}	peak to peak			0.4	ns
Output long term jiter	t_{lj}	peak to peak			2.0	ns
Lock up time	t_{lo}			300	1000	μs

(6) Timing diagram

The timing of power on and signal input is as follows:



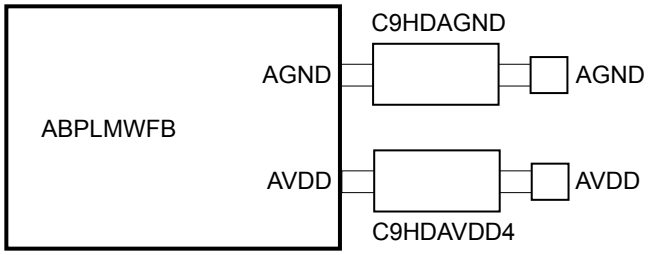
Maintain the status of STBY = 1 for at least 30 μs and make sure that the reference clock lasts for at least 1 μ sec with stability at that time. Then FO will be stabilized after lock up time.

(7) Pin functions

Pin Name	I/O	Function	Connection	C_{IN}/C_{MAX}
FR	I	Reference clock input	Internal	0.02 pF
M (4:0) Note1	I	M value for the M-counter	Internal	0.02 pF
N (6:0) Note1	I	N value for the N-counter	Internal	0.02 pF
P (2:0) Note1	I	P value for the P-counter	Internal	0.02 pF
S (1:0) Note1	I	Selected frequency range	Internal	0.40 pF
STBY	I	Standby mode control input	Internal	0.02 pF
RESETP	I	P-counter reset input	Internal	0.02 pF
MODE	I	Mode control input	Internal	0.03 pF
ATBI0	I	External clock input	Internal	0.02 pF
FO	O	Frequency output		
NO	O	Test output of N counter		
PLOCK	O	This pin dosen't use	Open	
AVDD Note2	I	Analog power supply	Internal Note2	–
AGND Note2	I	Analog ground	Internal Note2	–
DVDD Note2	I	Digital power supply	Internal Note2	–
DGND Note2	I	Digital ground	Internal Note2	–
TBI (19:0)	I	Test bus input	Internal	0.02 pF
TEST	I	Test mode setting input	Internal	0.02 pF
BUNRI	I	Separation test setting input	Internal	0.03 pF
TBO (2:0)	O	Test bus output	Internal	0.85 pF

Notes 1. Divided ratio M (4:0), N (6:0), P (2:0) and frequency range select S (1:0) should be set by F091 block. Switch of this ratio in operation is not recommended.

2. These pins should be wired directly to C9HDAVDD4 and C9HDAGND blocks without using I/O buffers.



(8) Divider tables

(a) M-Counter Table

The M-values are set using the combinations of M-Value (M4 to M0).

However, setting M-value = 0 is prohibited.

M4	M3	M2	M1	M0	M-Value	m-Value
0	0	0	0	0	Invalid	Invalid
0	0	0	0	1	1	2
0	0	0	1	0	2	3
0	0	0	1	1	3	4
–	–	–	–	–	–	–
1	1	1	1	0	30	31
1	1	1	1	1	31	32

(b) N-Counter table

The N-values are set using the combinations of N-Value (N6 to N0).

However, setting N-value = 0 is prohibited.

N6	N5	N4	N3	N2	N1	N0	N-Value	n-Value
0	0	0	0	0	0	0	Invalid	Invalid
0	0	0	0	0	0	1	1	2
0	0	0	0	0	1	0	2	3
–	–	–	–	–	–	–	–	–
1	1	1	1	1	1	0	126	127
1	1	1	1	1	1	1	127	128

(C) P-Counter table

The P-Counter is used to set the VCO output frequency in order to get a 50% duty cycle.

When all three values of P (2:0) are 0, then the VCO output frequency (f_{VCO}) is the same as the PLL output frequency, Fout.

The combinations of P (2:0) values and P values are given in the table below. Note that there are only 4 valid states.

P2	P1	P0	P-Value	p-Value	Fout
0	0	0	0	1	f_{VCO}
0	0	1	1	2	$f_{VCO}/2$
0	1	1	3	4	$f_{VCO}/4$
1	1	1	7	8	$f_{VCO}/8$
0	1	0	Invalid	Invalid	–
1	0	0	Invalid	Invalid	–
1	0	1	Invalid	Invalid	–
1	1	0	Invalid	Invalid	–

(9) Frequency selection table

The S-Counter (S0-S1) is used after the target output is selected by the user. The S-Counter table that can be selected is shown below.

S1	S0	f_{VCO}
0	0	50 to 90 MHz
0	1	90 to 130 MHz
1	0	130 to 170 MHz
1	1	170 to 230 MHz

The value that is selected by S1 and S0 is the VCO output frequency (f_{VCO}). The PLL output frequency (Fout) will become a value of VCO output frequency that was divided by P-divider. The improper setting of the S1 and S0 will result in an increase of PLL jitter.

(10) Operation table

There are five test modes in PLL macro as shown below.

(a) Normal mode (BUNRI = 0, STBY = 0, MODE = 0)

In this mode, input clock signal is multiplied and output to FO pin. Output clock signal from VCO can be divided by one, two, four or eight by controlling P (2:0).

Since the duty of output clock is not always 50% at P (2:0) = 0, if the 50% duty output is required, the divider is recommended to use.

(b) Stand by mode (TEST = 0, BUNRI = 0, STBY = 1)

Power consumption of PLL can be reduced in this mode by stopping clock signal.

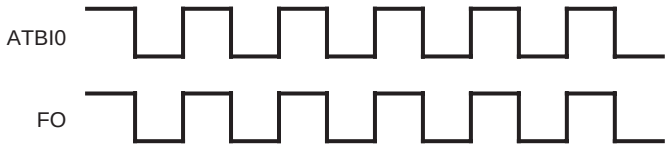
The lock up time is required until the output frequency is stabilized since release of this mode.

(c) PLL macro test mode (TEST = 1, BUNRI = 1)

This mode is test mode for PLL itself. Multiplied clock is output to TBO1

(d) Through mode (BUNRI = 0, MODE = 1)

This mode is used to compress the test pattern. In this mode, input clock signal from ATBI0 is output to FO directly for testing.



(e) Idd test mode (BUNRI = 0, MODE = 1, STBY = 1)

This mode is used to perform the Idd test for user logic.

The status of the pins during each test mode is shown below.

Pin Name / Test Mode	Input							
	FR	STBY	RESETP	S (1:0)	TBI0	TBI1	TBI2	TBI (19:3)
Normal mode	Fref	0	0	Valid	X	X	X	X
Standby mode	X	1	1	Valid	X	X	X	X
PLL macro test mode	X	X	X	X	Fref	0	0	Valid
Through mode	X	X	X	X	X	X	X	X
Idd test mode	X	1	X	X	X	X	X	X

Pin Name / Test Mode	Input				Output		
	TEST	BUNRI	MODE	ATBI0	FO	TBO0	TBO1
Normal mode	X	0	0	X	Fref x (n/m/p)	Hi-z	Hi-z
Standby mode	X	0	0	X	Fixed 1 or 0	Hi-z	Hi-z
PLL macro test mode	1	1	X	X	1	Fref / 2m	Fref x (n/m/p)
Through mode	X	0	1	Fop	Fop	Hi-z	Hi-z
Idd test mode	X	0	1	X	Fixed 1 or 0	Hi-z	Hi-z

Remarks 1. X means Don't care.
Fref means actual input frequency.
Fop means input frequency in simulation.

2. S (1:0) should be set by F091.

3. M (4:0), N (6:0) and P (2:0) should be set by F091.

4. Please care for maximum VCO frequency.

(11) Cautions

(a) There is some case which occurs some of non-connect pins, according to combination of master size and package.
(b) Input frequency and multiplication ratio should be set to keep consistent with VCO frequency range.
(c) This PLL should not be located nearby high drivability buffer or oscillation block.
(d) ON/OFF switch timing of power supply should be the same as the timing of total chip.
(e) NEC recommends separate V_{DD}/GND supply line on the PCB board, in order to have an immunity from noise.
(f) This PLL needs some lock up time after stand-by mode release.

(12) Example of the division number of M and N counter to obtain 220 MHz operation (Normal mode)

The following is an example of the Division Number of M and N counter to obtain 220 MHz operation using the equation for determining Fout. A calculation program is available so that the user can input the reference frequency, the target PLL frequency and it will give optimal Division Number for the M, N, and P counters so that the PLL output is the closest possible to the target output frequency. To program the counter values, they should be m = –1, n = –1 and p = –1.

m = 8, n = 123, and p = 1. That means M = 7, N = 122, and P = 0.
From Fout = (Fr × n) / (m × p),
Fout = (14.31818 × 123)/8 = 220 MHz

9.8.2 ADPLSHFB

(1) Overview

This macro is APLL with multiplication function.

The low frequency clock (from 10 MHz on up) can be input to it.

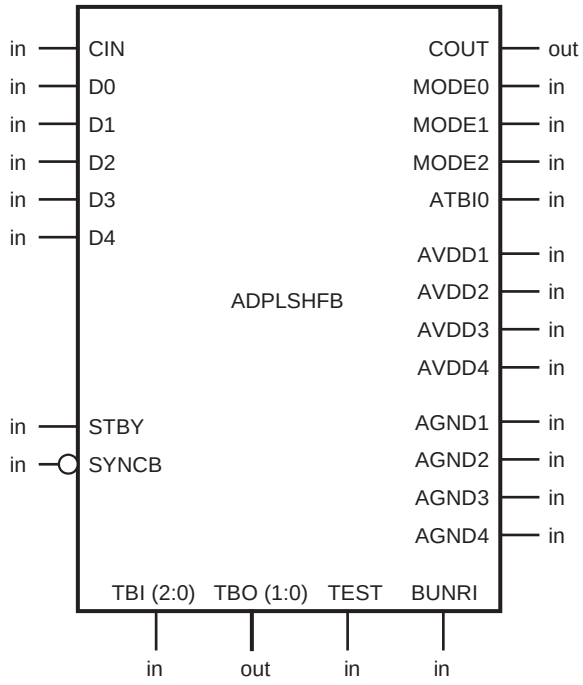
The output clock frequency up to 250 MHz can be output by this macro (APLL). In contrast, the maximum input frequency of the EA-9HD Series internal cells is 100 MHz. If the output clock frequency of the APLL exceeds 100MHz, therefore, please refer to NEC Electronics.

There is no skew adjustment function between an input FR pin and output FO pin.

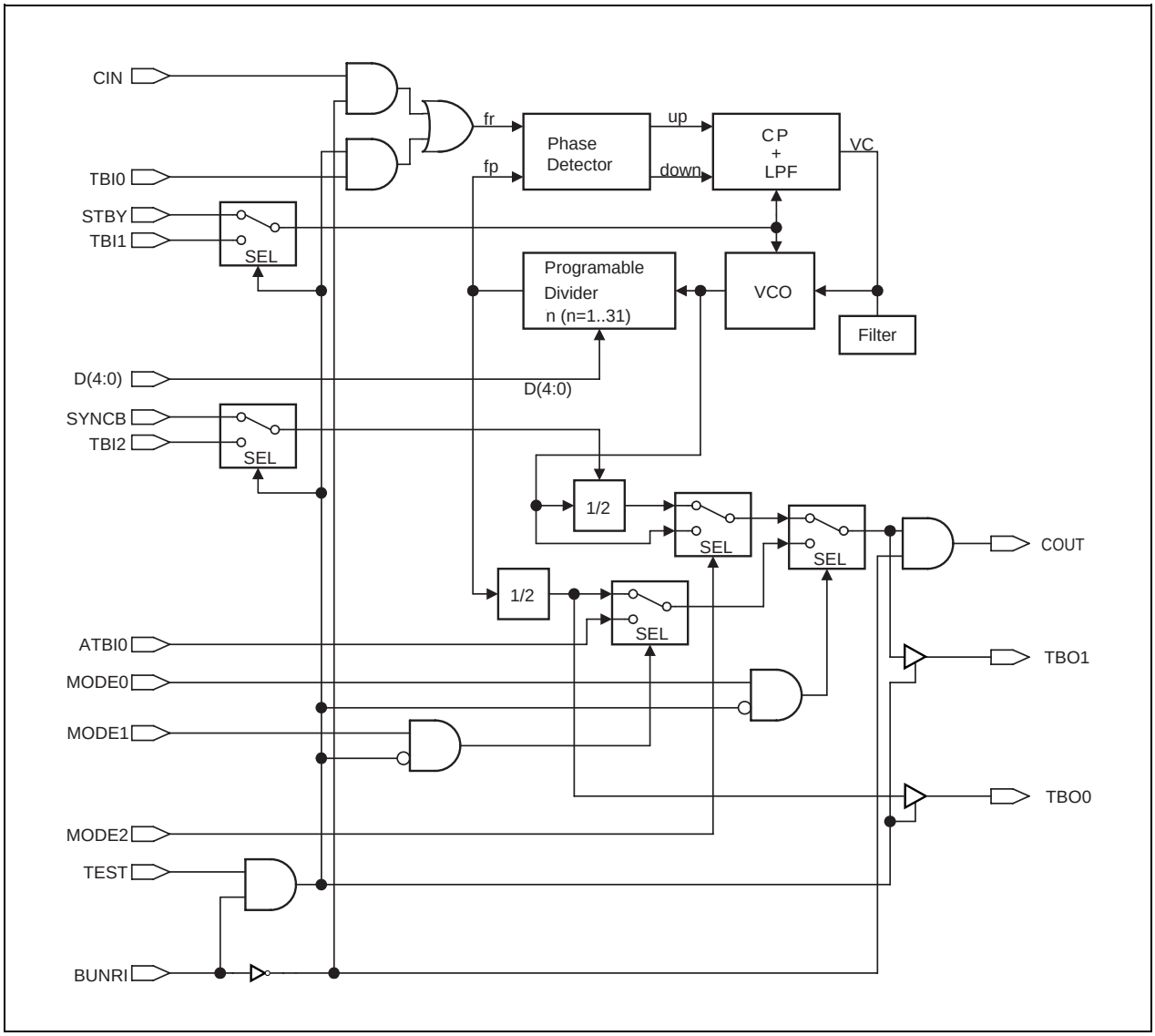
(2) Typical Characteristics and Features

- Macro name: ADPLSHFB
- Number of cells: 5400
- Supply voltage: 3.3 ±0.3 V
- Operating temperature: –40 to 85°C
- VCO output frequency range: 160 to 250 MHz
- Multiplication ratio: 2 to 16
- Output jitter: 0.5 ns (peak to peak)
- No external device is needed

(3) Symbol diagram



(4) Block diagram



(a) Phase Detector

It outputs a pulse to show progress or delay by detecting the phase difference between two input signals.

(b) CP+LPF (Charge Pump + Low Pass Filter)

It converts the signal from Phase Detector to DC voltage.

(c) VCO (Voltage Control Oscillator)

It outputs the oscillation frequency depending to the LPF output voltage.

(5) Electrical specifications

(a) Absolute maximum ratings (T_A = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{STG}	–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

(b) Recommended Operating Range (T_A = –40 to +85°C)

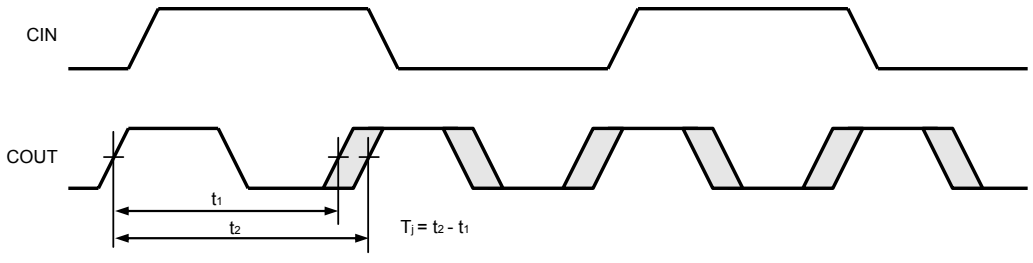
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AV_{DD}		3.0	3.3	3.6	V
Input frequency	f_{std}		10		125	MHz
Input rise time	t_r	From 10% to 90% of V_{DD}			2.0	ns
Input fall time	t_f	From 90% to 10% of V_{DD}			2.0	ns
Input high pulse width	t_{pwh}		2.0			ns
Input low pulse width	t_{pwl}		2.0			ns
Multiplication rate	n		2		16	

(c) Electrical Specifications (T_A = –40 to +85°C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	Operation			12.0	mA
	I_{DDS}	Standby			10.0	μA
VCO output frequency	f_{vco}		160		250	MHz
Output jitter	t_j	peak to peak			0.5	ns
Lock up time	t_{lo}				100	μs

(6) Timing diagram

Output jitter value is shown below.

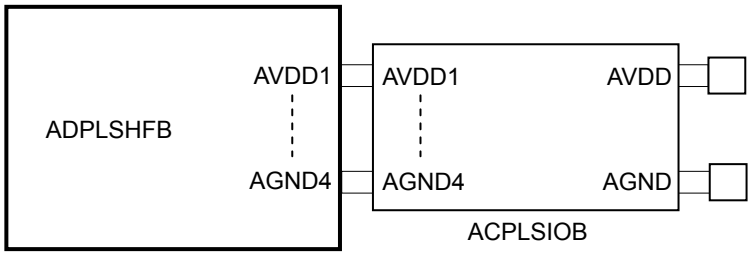


(7) Pin functions

Pin Name	I/O	Function	Connection	C_{IN}/C_{MAX}
CIN	I	Reference clock input	Internal	0.03 pF
D (4:0) Note1	I	Multiplication ratio data input	Internal	0.02 pF
STBY	I	Standby mode control input	Internal	0.03 pF
SYNCB	I	Divider reset input	Internal	0.03 pF
COUT	O	Clock output	Internal	2.68 pF
MODE0	I	Mode control input	Internal	0.02 pF
MODE1	I	Mode select input	Internal	0.02 pF
MODE2	I	Duty cycle control input (1/2 divider control)	Internal	0.06 pF
ATBI0	I	External clock input	Internal	0.03 pF
AVDD1	I	Analog power supply	Internal Note2	-
AVDD2	I	Analog power supply	Internal Note2	-
AVDD3	I	Analog power supply	Internal Note2	-
AVDD4	I	Analog power supply	Internal Note2	-
AGND1	I	Analog ground	Internal Note2	–
AGND2	I	Analog ground	Internal Note2	–
AGND3	I	Analog ground	Internal Note2	–
AGND4	I	Analog ground	Internal Note2	–
TBI (2:0)	I	Test bus input	Internal	0.03 pF
TEST	I	Test mode setting input	Internal	0.02 pF
BUNRI	I	Separation test setting input	Internal	0.04 pF
TBO0	O	Clock output (Used for core test mode)	Internal	2.69 pF
TBO1	O	Clock output (Used for core test mode)	Internal	2.69 pF

Notes 1. Multiplication ratio should be set by F091 block. Switch of this ratio in operation is not recommended.

2. These pins should be wired directly to ACPLSIOB block without using I/O buffers.



(8) Operation table

There are six test modes in PLL macro as shown below.

(a) Normal mode (TEST = 0, BUNRI = 0, STBY = 0, MODE0 = 0)

In this mode, input clock signal is multiplied and output to COUT pin. Output clock signal from VCO can be divided by two, controlling MODE2 signal. Since the duty of output clock is not always 50% when MODE2=1. If the 50% duty output is required, the divider is recommended to use.

(b) Stand by mode (TEST = 0, BUNRI = 0, STBY = 1, MODE0 = 0)

Power consumption of PLL can be reduced in this mode by stopping clock signal.

(c) PLL core test mode (TEST = 1, BUNRI = 1)

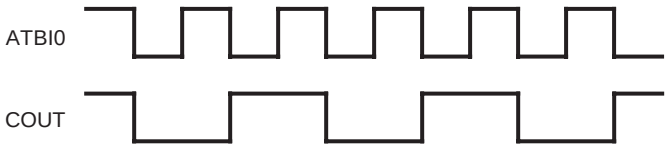
This mode is test mode for PLL itself. Half frequency clock of input clock is output to TBO0 and multiplied clock is output to TBO1.

(d) Other core test mode (TEST = 0, BUNRI = 1)

This mod030221e is other core test mode for other connected TBO0 or TBO1. In this mode, COUT is 0, TBO0 and TBO1 are hi-impedance.

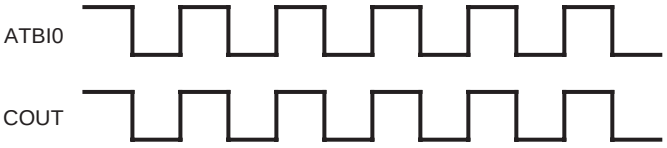
(e) Simulation mode (TEST = 0, BUNRI = 0, MODE0 = 1, MODE1 = 0)

This mode is test and simulation mode for internal user logic. Half frequency of input clock is output to COUT.



(f) Test pattern compression mode (TEST = 0, BUNRI = 0, MODE0 = 1, MODE1 = 1)

This mode is also test and simulation mode for internal user logic, in order to shorten test pattern. Input clock signal from ATBI0 is output to COUT directly.



The status of the pins during each test mode is shown in the following table.

Pin Name / Test Mode	Input									
	CIN	D(4:0)	STBY	SYNCB	ATBI0	TEST	BUNRI	MODE0	MODE1	MODE2
Normal mode	Fref	n	0	1	X	0	0	0	X	1
	Fref	n	0	1	X	0	0	0	X	0
Standby mode	X	X	1	X	X	0	0	0	X	X
PLL macro test mode	X	n	X	X	X	1	1	X	X	1
	X	n	X	X	X	1	1	X	X	0
Other core test mode	X	X	X	X	X	0	1	X	X	X
Simulation mode	Fop	n	0	1	X	0	0	1	0	X
Test pattern compression mode	X	X	X	1	Fop	0	0	1	1	X

Pin Name / Test Mode	Input			Output		
	TBI0	TBI1	TBI2	COUT	TBO0	TBO1
Normal mode	X	X	X	Fref x n	Hi-z	Hi-z
	X	X	X	Fref x n/2	Hi-z	Hi-z
Standby mode	X	X	X	X	Hi-z	Hi-z
PLL macro test mode	Fref	0	1	0	Fref/2	Fref x n
	Fref	0	1	0	Fref/2	Fref x n/2
Other core test mode	X	X	X	0	Hi-z	Hi-z
Simulation mode	X	X	X	Fop/2	Hi-z	Hi-z
Test pattern compression mode	X	X	X	Fop	Hi-z	Hi-z

Remarks 1. X means Don't care.
Fref means actual input frequency.
Fop means input frequency in simulation.

2. D(4:0) should be set by F091.

3. MODE2 should be set by F091.

(9) Cautions

(a) There is some case which occurs some of non-connect pins, according to combination of master size and package.

(b) Input frequency and multiplication ratio should be set to keep consistent with VCO frequency range.

(c) AVDD1-AVDD4 pins should be connected with AVDD1-AVDD4 pins of AAPLSIOB or ACPLSIOB block and AGND1-AGND4 pins should be connected with AGND1-AGND4 pins of AAPLSIOB or ACPLSIOB without any buffer.

(d) This PLL should not be located nearby high drivability buffer or oscillation block.

(e) Input clock into this PLL and output clock signal don't synchronize, because test circuit is inserted.

(f) Supply voltage of this PLL should be the same as supply voltage of total chip.

(g) ON/OFF switch timing of power supply should be the same as the timing of total chip.

(h) NEC recommends separate VDD/GND supply line on the PCB board, in order to have an immunity from noise.

(i) This PLL needs some lock up time after stand-by mode release.

(j) Create a user pattern in test pattern compression mode.

9.8.3 ADPLSMFB

(1) Overview

This macro is APLL with multiplication function.

The low frequency clock (from 7.5 MHz on up) can be input to it.

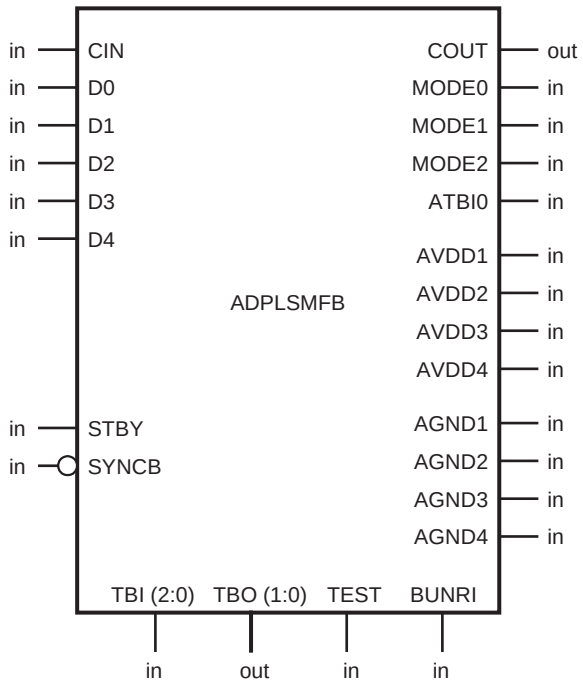
The output clock frequency up to 170 MHz can be output by this macro (APLL). In contrast, the maximum input frequency of the EA-9HD Series internal cells is 100 MHz. If the output clock frequency of the APLL exceeds 100MHz, therefore, please refer to NEC Electronics.

There is no skew adjustment function between an input FR pin and output FO pin.

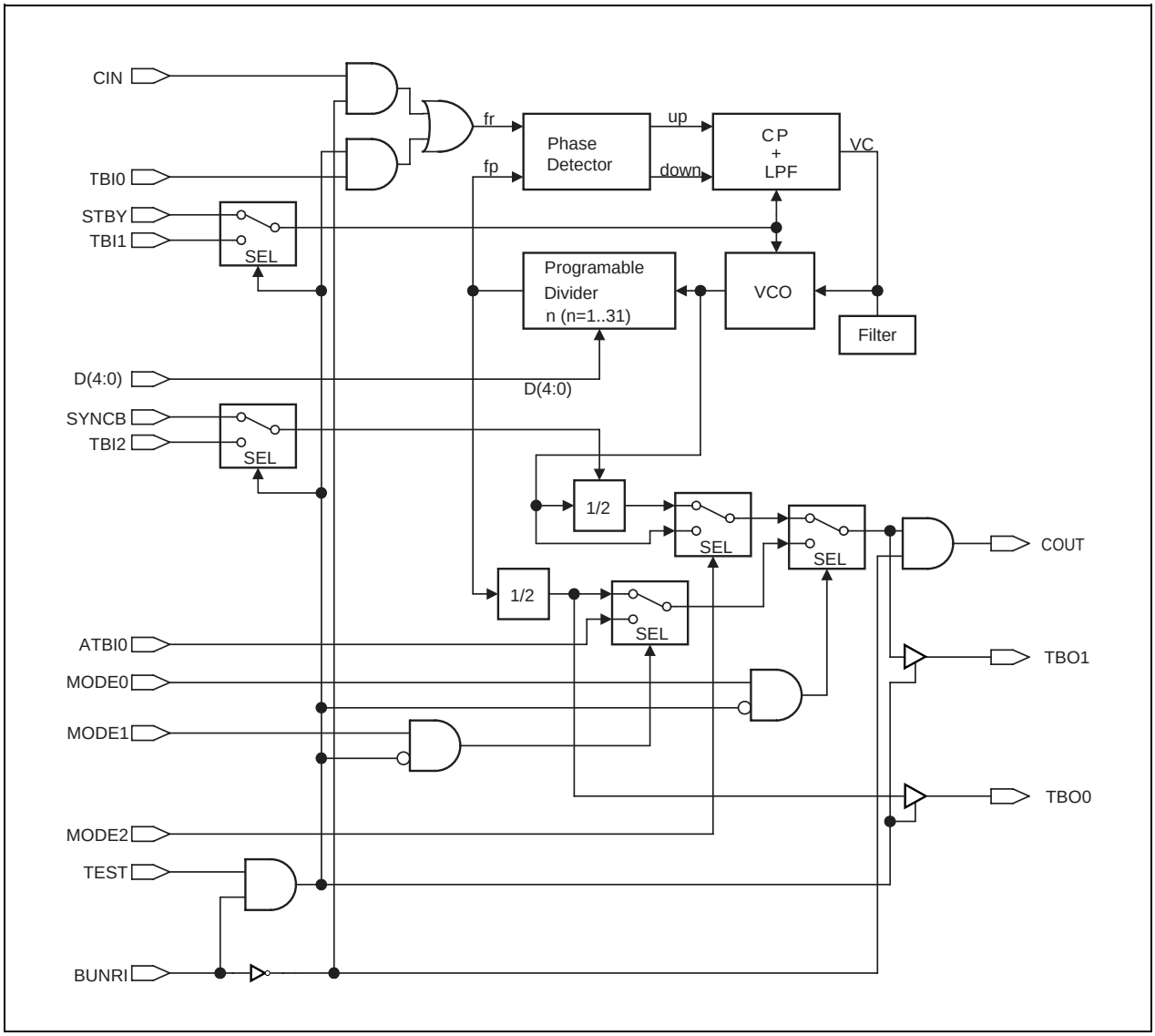
(2) Typical Characteristics and Features

- Macro name: ADPLSMFB
- Number of cells: 5400
- Supply voltage: 3.3 ± 0.3 V
- Operating temperature: –40 to 85°C
- VCO output frequency range: 120 to 170 MHz
- Multiplication ratio: 2 to 16
- Output jitter: 1.0 ns (peak to peak)
- No external device is needed

(3) Symbol diagram



(4) Block diagram



(a) Phase Detector

It outputs a pulse to show progress or delay by detecting the phase difference between two input signals.

(b) CP+LPF (Charge Pump + Low Pass Filter)

It converts the signal from Phase Detector to DC voltage.

(c) VCO (Voltage Control Oscillator)

It outputs the oscillation frequency depending to the LPF output voltage.

(5) Electrical specifications

(a) Absolute maximum ratings (T_A = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{STG}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

(b) Recommended Operating Range (T_A = −40 to +85°C)

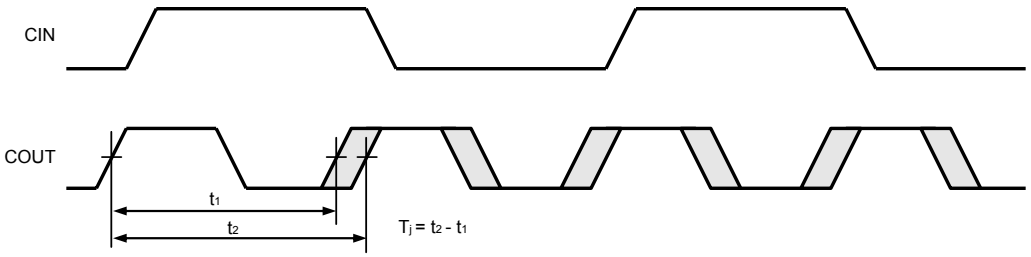
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AV_{DD}		3.0	3.3	3.6	V
Input frequency	f_{std}		7.5		85	MHz
Input rise time	t_r	From 10% to 90% of V_{DD}			2.0	ns
Input fall time	t_f	From 90% to 10% of V_{DD}			2.0	ns
Input high pulse width	t_{pwh}		2.0			ns
Input low pulse width	t_{pwl}		2.0			ns
Multiplication rate	n		2		16	

(c) Electrical Specifications (T_A = −40 to +85°C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	Operation			9.5	mA
	I_{DDS}	Standby			10.0	μA
VCO output frequency	f_{vco}		120		170	MHz
Output jitter	t_j	peak to peak			1.0	ns
Lock up time	t_{lo}				100	μs

(6) Timing diagram

Output jitter value is shown below.

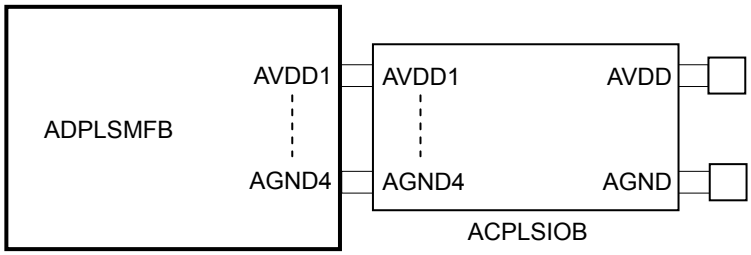


(7) Pin functions

Pin Name	I/O	Function	Connection	C_{IN}/C_{MAX}
CIN	I	Reference clock input	Internal	0.03 pF
D(4:0) Note1	I	Multiplication ratio data input	Internal	0.02 pF
STBY	I	Standby mode control input	Internal	0.03 pF
SYNCB	I	Divider reset input	Internal	0.03 pF
COUT	O	Clock output	Internal	2.68 pF
MODE0	I	Mode control input	Internal	0.02 pF
MODE1	I	Mode select input	Internal	0.02 pF
MODE2	I	Duty cycle control input (1/2 divider control)	Internal	0.06 pF
ATBI0	I	External clock input	Internal	0.03 pF
AVDD1	I	Analog power supply	Internal Note2	-
AVDD2	I	Analog power supply	Internal Note2	-
AVDD3	I	Analog power supply	Internal Note2	-
AVDD4	I	Analog power supply	Internal Note2	-
AGND1	I	Analog ground	Internal Note2	–
AGND2	I	Analog ground	Internal Note2	–
AGND3	I	Analog ground	Internal Note2	–
AGND4	I	Analog ground	Internal Note2	–
TBI(2:0)	I	Test bus input	Internal	0.03 pF
TEST	I	Test mode setting input	Internal	0.02 pF
BUNRI	I	Separation test setting input	Internal	0.04 pF
TBO0	O	Clock output (Used for core test mode)	Internal	2.69 pF
TBO1	O	Clock output (Used for core test mode)	Internal	2.69 pF

Notes 1. Multiplication ratio should be set by F091 block. Switch of this ratio in operation is not recommended.

2. These pins should be wired directly to ACPLSIOB block without using I/O buffers.



(8) Operation table

There are six test modes in PLL macro as shown below.

(a) Normal mode (TEST = 0, BUNRI = 0, STBY = 0, MODE0 = 0)

In this mode, input clock signal is multiplied and output to COUT pin. Output clock signal from VCO can be divided by two, controlling MODE2 signal. Since the duty of output clock is not always 50% when MODE2=1. If the 50% duty output is required, the divider is recommended to use.

(b) Stand by mode (TEST = 0, BUNRI = 0, STBY = 1, MODE0 = 0)

Power consumption of PLL can be reduced in this mode by stopping clock signal.

(c) PLL core test mode (TEST = 1, BUNRI = 1)

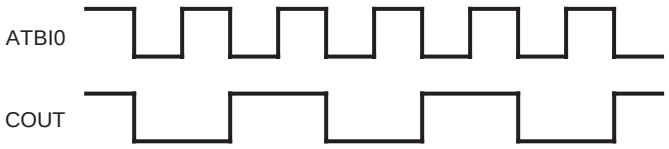
This mode is test mode for PLL itself. Half frequency clock of input clock is output to TBO0 and multiplied clock is output to TBO1.

(d) Other core test mode (TEST = 0, BUNRI = 1)

This mode is other core test mode for other connected TBO0 or TBO1. In this mode, COUT is 0, TBO0 and TBO1 are hi-impedance.

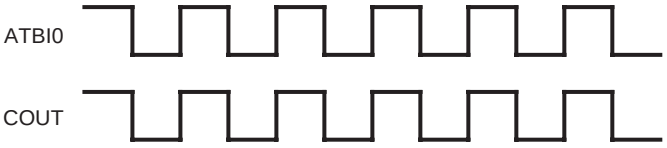
(e) Simulation mode (TEST = 0, BUNRI = 0, MODE0 = 1, MODE1 = 0)

This mode is test and simulation mode for internal user logic. Half frequency of input clock is output to COUT.



(f) Test pattern compression mode (TEST = 0, BUNRI = 0, MODE0 = 1, MODE1 = 1)

This mode is also test and simulation mode for internal user logic, in order to shorten test pattern. Input clock signal from ATBI0 is output to COUT directly.



The status of the pins during each test mode is shown in the following table.

Pin Name / Test Mode	Input									
	CIN	D(4:0)	STBY	SYNCB	ATBI0	TEST	BUNRI	MODE0	MODE1	MODE2
Normal mode	Fref	n	0	1	X	0	0	0	X	1
	Fref	n	0	1	X	0	0	0	X	0
Standby mode	X	X	1	X	X	0	0	0	X	X
PLL macro test mode	X	n	X	X	X	1	1	X	X	1
	X	n	X	X	X	1	1	X	X	0
Other core test mode	X	X	X	X	X	0	1	X	X	X
Simulation mode	Fop	n	0	1	X	0	0	1	0	X
Test pattern compression mode	X	X	X	1	Fop	0	0	1	1	X

Pin Name / Test Mode	Input			Output		
	TBI0	TBI1	TBI2	COUT	TBO0	TBO1
Normal mode	X	X	X	Fref x n	Hi-z	Hi-z
	X	X	X	Fref x n/2	Hi-z	Hi-z
Standby mode	X	X	X	X	Hi-z	Hi-z
PLL macro test mode	Fref	0	1	0	Fref/2	Fref x n
	Fref	0	1	0	Fref/2	Fref x n/2
Other core test mode	X	X	X	0	Hi-z	Hi-z
Simulation mode	X	X	X	Fop/2	Hi-z	Hi-z
Test pattern compression mode	X	X	X	Fop	Hi-z	Hi-z

Remarks 1. n means multiplication rate set by F091.
Fref means actual input frequency.
Fop means input frequency in simulation.

2. D(4:0) should be set by F091.

3. MODE2 should be set by F091.

(9) Cautions

(a) There is some case which occurs some of non-connect pins, according to combination of master size and package.

(b) Input frequency and multiplication ratio should be set to keep consistent with VCO frequency range.

(c) AVDD1-AVDD4 pins should be connected with AVDD1-AVDD4 pins of AAPLSIOB or ACPLSIOB block and AGND1-AGND4 pins should be connected with AGND1-AGND4 pins of AAPLSIOB or ACPLSIOB without any buffer.

(d) This PLL should not be located nearby high drivability buffer or oscillation block.

(e) Input clock into this PLL and output clock signal don't synchronize, because test circuit is inserted.

(f) Supply voltage of this PLL should be the same as supply voltage of total chip.

(g) ON/OFF switch timing of power supply should be the same as the timing of total chip.

(h) NEC recommends separate VDD/GND supply line on the PCB board, in order to have a immunity from noise.

(i) This PLL needs some lock up time after stand-by mode release.

(j) Create a user pattern in test pattern compression mode.

9.8.4 ACPLSLFB

(1) Overview

This macro is APLL with multiplication function.

The low frequency clock (from 4.375 MHz on up) can be input to it.

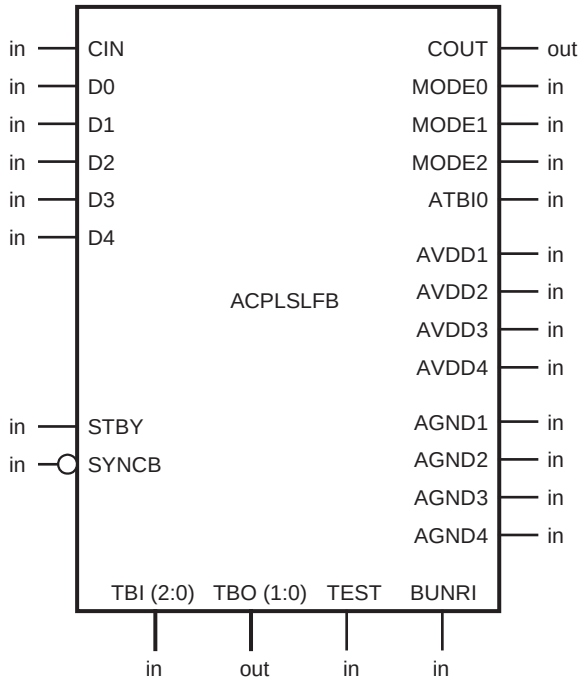
The output clock frequency up to 120 MHz can be output by this macro (APLL). In contrast, the maximum input frequency of the EA-9HD Series internal cells is 100 MHz. If the output clock frequency of the APLL exceeds 100MHz, therefore, please refer to NEC Electronics.

There is no skew adjustment function between an input FR pin and output FO pin.

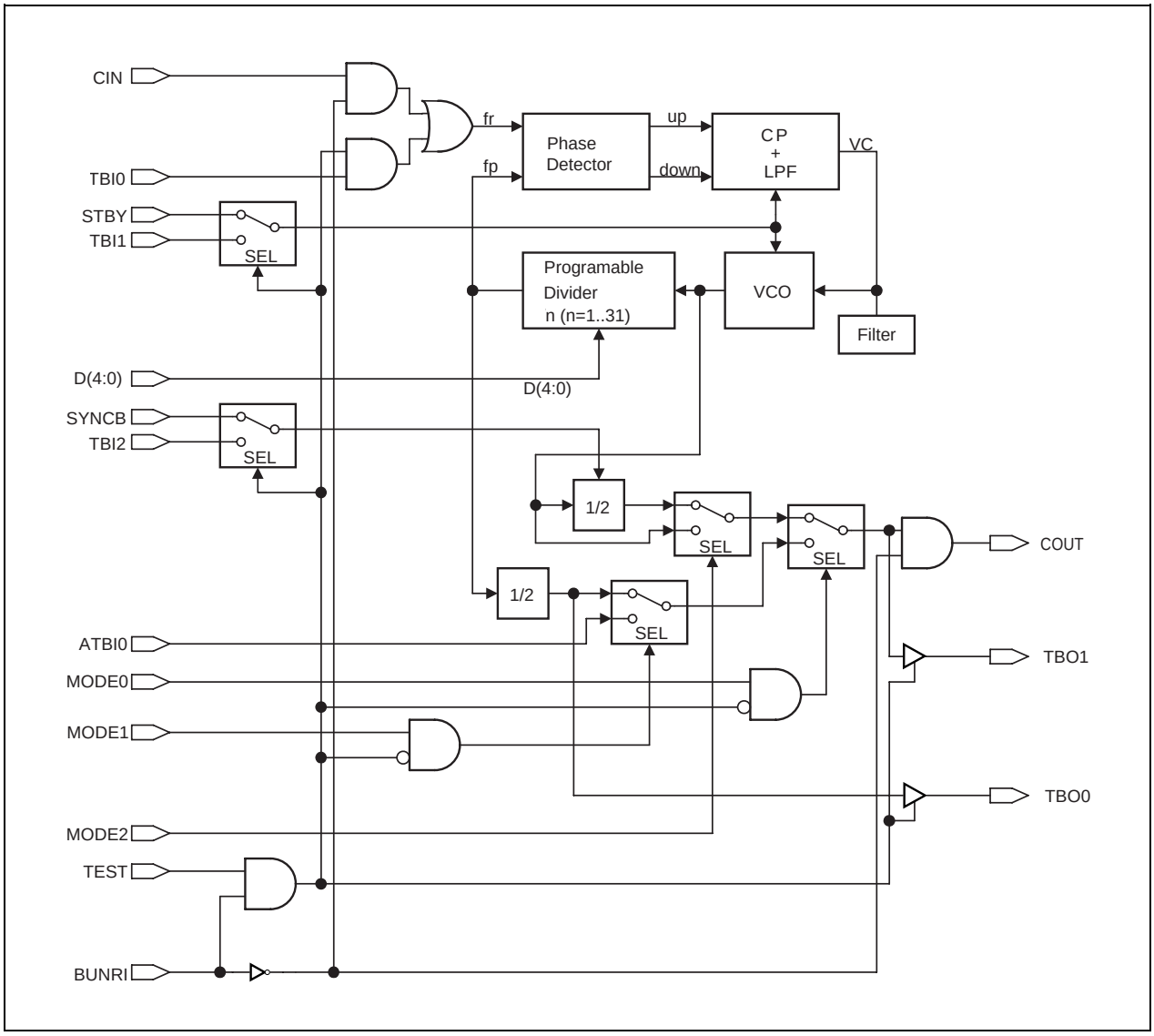
(2) Typical Characteristics and Features

- Macro name: ACPLSLFB
- Number of cells: 5400
- Supply voltage: 3.3 ± 0.3 V
- Operating temperature: –40 to 85°C
- VCO output frequency range: 70 to 120 MHz
- Multiplication ratio: 2 to 16
- Output jitter: 1.0 ns (peak to peak)
- No external device is needed

(3) Symbol diagram



(4) Block diagram



(a) Phase Detector

It outputs a pulse to show progress or delay by detecting the phase difference between two input signals.

(b) CP+LPF (Charge Pump + Low Pass Filter)

It converts the signal from Phase Detector to DC voltage.

(c) VCO (Voltage Control Oscillator)

It outputs the oscillation frequency depending to the LPF output voltage.

(5) Electrical specifications

(a) Absolute maximum ratings (T_A = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.5 to +4.6	V
Operating ambient temperature	T_A	−40 to +85	°C
Storage temperature	T_{STG}	−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

(b) Recommended Operating Range (T_A = −40 to +85°C)

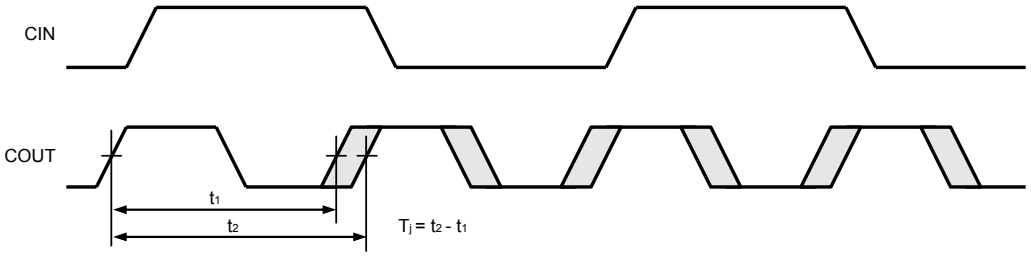
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AV_{DD}		3.0	3.3	3.6	V
Input frequency	f_{std}		4.375		60	MHz
Input rise time	t_r	From 10% to 90% of V_{DD}			2.0	ns
Input fall time	t_f	From 90% to 10% of V_{DD}			2.0	ns
Input high pulse width	t_{pwh}		2.0			ns
Input low pulse width	t_{pwl}		2.0			ns
Multiplication rate	n		2		16	

(c) Electrical Specifications (T_A = −40 to +85°C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	Operation at 100 MHz			4.2	mA
	I_{DD2}	Operation at 120 MHz			5.0	mA
	I_{DDS}	Standby			10.0	μA
VCO output frequency	f_{vco}		70		120	MHz
Output jitter	t_j	peak to peak			1.0	ns
Lock up time	t_{lo}				100	μs

(6) Timing diagram

Output jitter value is shown below.

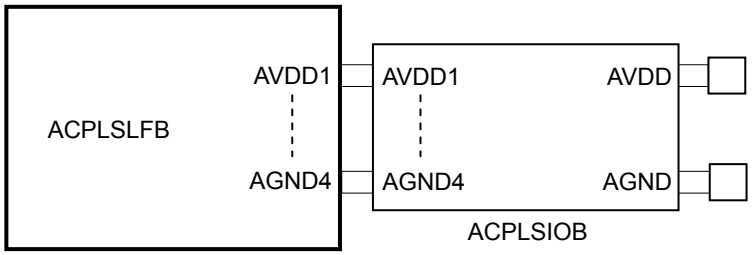


(7) Pin functions

Pin Name	I/O	Function	Connection	C_{IN}/C_{MAX}
CIN	I	Reference clock input	Internal	0.03 pF
D(4:0) Note1	I	Multiplication ratio data input	Internal	0.02 pF
STBY	I	Standby mode control input	Internal	0.03 pF
SYNCB	I	Divider reset input	Internal	0.03 pF
COUT	O	Clock output	Internal	2.68 pF
MODE0	I	Mode control input	Internal	0.02 pF
MODE1	I	Mode select input	Internal	0.02 pF
MODE2	I	Duty cycle control input (1/2 divider control)	Internal	0.06 pF
ATBI0	I	External clock input	Internal	0.03 pF
AVDD1	I	Analog power supply	Internal Note2	-
AVDD2	I	Analog power supply	Internal Note2	-
AVDD3	I	Analog power supply	Internal Note2	-
AVDD4	I	Analog power supply	Internal Note2	-
AGND1	I	Analog ground	Internal Note2	–
AGND2	I	Analog ground	Internal Note2	–
AGND3	I	Analog ground	Internal Note2	–
AGND4	I	Analog ground	Internal Note2	–
TBI(2:0)	I	Test bus input	Internal	0.03 pF
TEST	I	Test mode setting input	Internal	0.02 pF
BUNRI	I	Separation test setting input	Internal	0.04 pF
TBO0	O	Clock output (Used for core test mode)	Internal	2.69 pF
TBO1	O	Clock output (Used for core test mode)	Internal	2.69 pF

Notes 1. Multiplication ratio should be set by F091 block. Switch of this ratio in operation is not recommended.

2. These pins should be wired directly to ACPLSIOB block without using I/O buffers.



(8) Operation table

There are six test modes in PLL macro as shown below.

(a) Normal mode (TEST = 0, BUNRI = 0, STBY = 0, MODE0 = 0)

In this mode, input clock signal is multiplied and output it to COUT pin. Output clock signal from VCO can be divided by two, controlling MODE2 signal. Since the duty of output clock is not always 50% when MODE2=1. If the 50% duty output is required, the divider is recommended to use.

(b) Stand by mode (TEST = 0, BUNRI = 0, STBY = 1, MODE0 = 0)

Power consumption of PLL can be reduced in this mode by stopping clock signal.

(c) PLL core test mode (TEST = 1, BUNRI = 1)

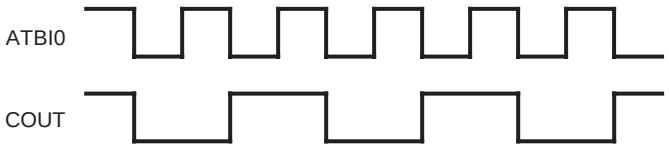
This mode is test mode for PLL itself. Half frequency clock of input clock is output to TBO0 and multiplied clock is output to TBO1.

(d) Other core test mode (TEST = 0, BUNRI = 1)

This mode is other core test mode for other connected TBO0 or TBO1. In this mode, COUT is 0, and TBO0 and TBO1 are hi-impedance.

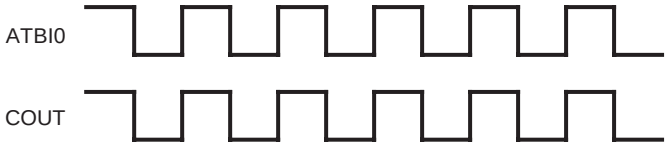
(e) Simulation mode (TEST = 0, BUNRI = 0, MODE0 = 1, MODE1 = 0)

This mode is test and simulation mode for internal user logic. Half frequency of input clock is output to COUT.



(f) Test pattern compression mode (TEST = 0, BUNRI = 0, MODE0 = 1, MODE1 = 1)

This mode is also test and simulation mode for internal user logic, in order to shorten test pattern. Input clock signal from ATBI0 is output to COUT directly.



The status of the pins during each test mode is shown in the following table.

Test Mode \ Pin Name	Input									
	CIN	D(4:0)	STBY	SYNCB	ATBI0	TEST	BUNRI	MODE0	MODE1	MODE2
Normal mode	Fref	n	0	1	X	0	0	0	X	1
	Fref	n	0	1	X	0	0	0	X	0
Standby mode	X	X	1	X	X	0	0	0	X	X
PLL macro test mode	X	n	X	X	X	1	1	X	X	1
	X	n	X	X	X	1	1	X	X	0
Other core test mode	X	X	X	X	X	0	1	X	X	X
Simulation mode	Fop	n	0	1	X	0	0	1	0	X
Test pattern compression mode	X	X	X	1	Fop	0	0	1	1	X

Test Mode \ Pin Name	Input			Output		
	TBI0	TBI1	TBI2	COUT	TBO0	TBO1
Normal mode	X	X	X	Fref x n	Hi-z	Hi-z
	X	X	X	Fref x n/2	Hi-z	Hi-z
Standby mode	X	X	X	X	Hi-z	Hi-z
PLL macro test mode	Fref	0	1	0	Fref/2	Fref x n
	Fref	0	1	0	Fref/2	Fref x n/2
Other core test mode	X	X	X	0	Hi-z	Hi-z
Simulation mode	X	X	X	Fop/2	Hi-z	Hi-z
Test pattern compression mode	X	X	X	Fop	Hi-z	Hi-z

Remarks 1. n means multiplication rate set by F091.
Fref means actual input frequency.
Fop means input frequency in simulation.

2. D(4:0) should be set by F091.

3. MODE2 should be set by F091.

(9) Cautions

(a) There is some case which occurs some of non-connect pins, according to combination of master size and package.

(b) Input frequency and multiplication ratio should be set to keep consistent with VCO frequency range.

(c) AVDD1-AVDD4 pins should be connected with AVDD1-AVDD4 pins of AAPLSIOB or ACPLSIOB block and AGND1-AGND4 pins should be connected with AGND1-AGND4 pins of AAPLSIOB or ACPLSIOB without any buffer.

(d) This PLL should not be located nearby high drivability buffer or oscillation block.

(e) Input clock into this PLL and output clock signal don't synchronize, because test circuit is inserted.

(f) Supply voltage of this PLL should be the same as supply voltage of total chip.

(g) ON/OFF switch timing of power supply should be the same as the timing of total chip.

(h) NEC recommends to have separate VDD/GND supply line on the PCB board, in order to have a immunity from noise.

(i) This PLL needs some lock up time after stand-by mode release.

(j) Create a user pattern in test pattern compression mode.

<R> 9.9 Power on Reset

9.9.1 Overview

This Analog Core is EA9HD Power on Clear Circuit. When the power supply is turned on, it can be used as a signal to initialize a digital circuit. However, the Power-on-Clear function does not support a temporary blackout of the power supply.

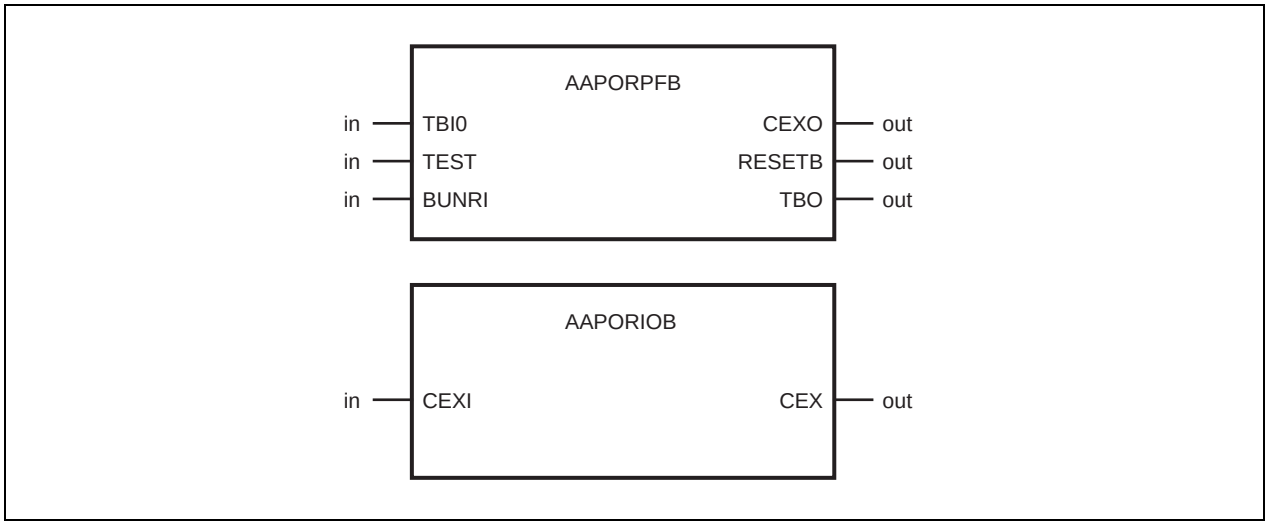
9.9.2 Typical Characteristics and Features

- Operating Junction Temperature (Tj): –40 to +125°C
- Power supply Voltage (V_{DD}): 1.8 to 3.6 V
- Detection voltage Hi: 2.15 to 2.35 V
- Detection voltage Lo: 1.90 to 2.10 V
- Hysteresis voltage Width: 0.2 to 0.3 V
- Reset Width 1: 20 ms (typ, CL = 0.1 μF)
- Reset Width 2: 10 μs (min. CL is not present)
- Current Consumption (Idd): 10 μA (max. V_{DD} = 3.6 V)
- External Capacitor (CL): 0 to 0.1 μF

9.9.3 Cell count

AAPORPFB: 2940 cells
AAPORIOB: 1 I/O

9.9.4 Symbol diagram



9.9.5 Pin information

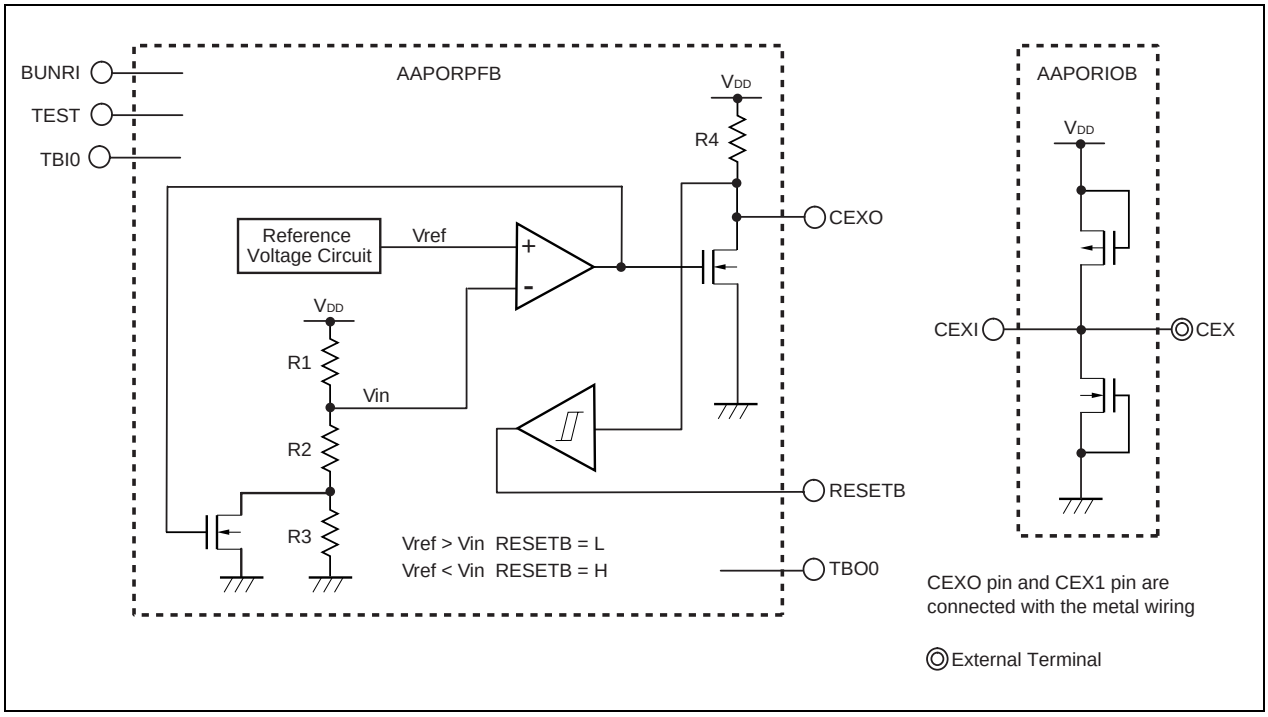
(1) AAPORPFB

Pin Name	I/O	Connection	Cin(pF)	Cmax(pF)
RESETB	O	internal	–	1.476
CEXO	O	internal	–	1.476
TBI0	I	internal	0.19	–
TBO0	O	internal	0.19	1.476
TEST	I	internal	0.19	–
BUNRI	I	internal	0.19	–

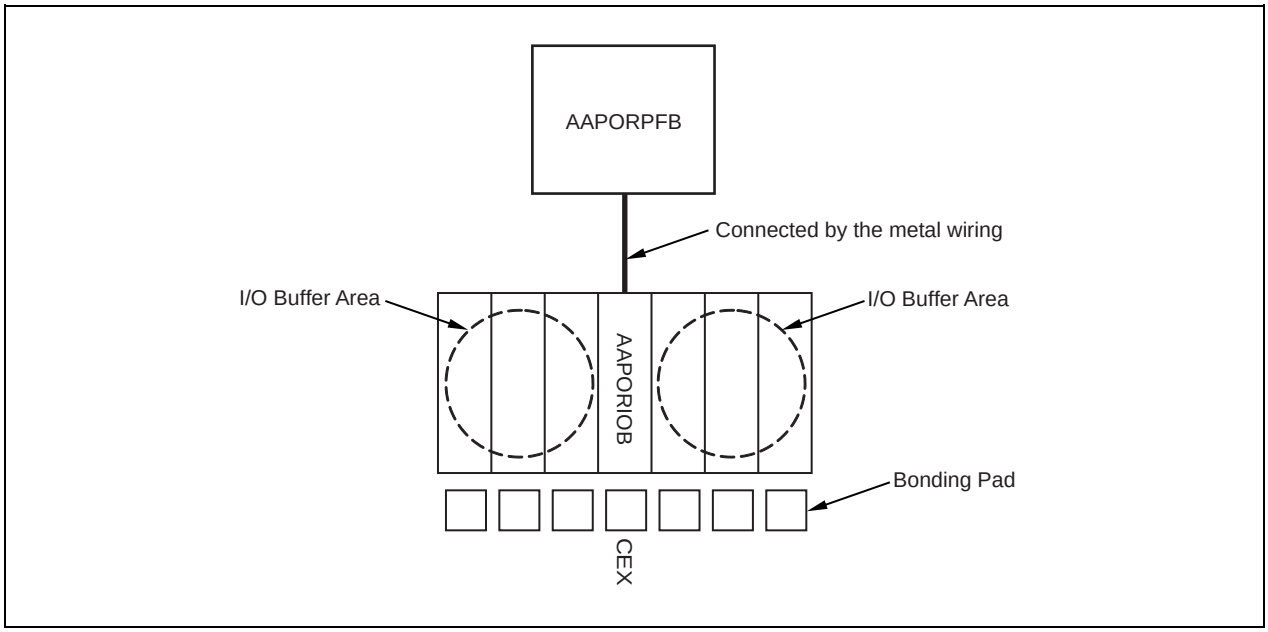
(2) AAPORIOB

Pin Name	I/O	Connection	Cin(pF)	Cmax(pF)
CEXI	I/O	internal	0.19	–
CEX	I/O	external	–	–

9.9.6 Block diagram



9.9.7 Layout image



9.9.8 Operation Table

The operation (Operation Table) of the simulation model in this core is a model that valued connected check. Please note it is different from the real operation.

The Operation table of the simulation model is shown below.

(1) AAPORPFB

Input			Output		
BUNRI	TEST	TBI0	RESETB	CEXO	TBO0
0	X	X	1	1	Hi-Z
1	0	X	1	1	Hi-Z
1	1	0	1	1	1
1	1	1	0	0	0

(2) AAPORIOB

Input	Output
CEXI	CEX
0	0
1	1

9.9.9 Electrical Characteristics (Preliminary)

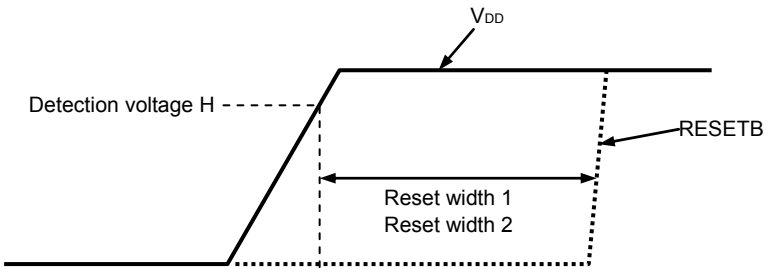
(1) Absolute maximum rating (Compliant with standard of EA9HD)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Power supply Voltage	V_{DD}		-0.5		4.6	V
Operating Junction Temperature	T_j		-40		125	°C
Storage Temperature	T_{stg}		-65		150	°C

(2) Power on reset characteristics

T_j = –40 to + 125°C

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Power supply Voltage	V_{DD}		1.8		3.6	V
Power supply slew rate	V_{SR}		0.033		1000	V/mS
Detection voltage Hi	V_{trip-H}		2.15		2.35	V
Detection voltage Lo	V_{trip-L}		1.90		2.10	V
Hysteresis voltage Width	V_{his}		0.2		0.3	V
Reset Width 1 (Refer to the figure below)	T_{pd1}	External Capacitor = 0.1 μF		20		mS
Reset Width 2 (Refer to the figure below)	T_{pd2}	External Capacity = 0	10			μS
Current Consumption	I_{DD}				10	μA



9.9.10 Pin function

(1) AAPORPFB

Pin Name	Description
RESETB	Reset signal output terminal (Active = Lo)
CEXO	Internal output of external capacitor connection terminal
TBI0	Test input terminal, Power down input (Normal: Lo, Power down: Hi)
TBO0	Test bus output, Reset signal output terminal (Active = Lo)
TEST	Test enable input terminal
BUNRI	Test mode control input terminal

(2) AAPORIOB

Pin Name	Description
CEXI	Internal input of external capacitor connection terminal
CEX	External output of external capacitor connection terminal

9.9.11 Cautions when using core

(1) The external capacitor connected with the CEX pin in this core is assumed to be 0.1 μF or less. Please reduce the wiring resistance on the substrate.

(2) This Power on Clear does not support a temporary blackout of the power supply.

(3) Be sure to use AAPORPFB and AAPORIOB in a pair.

(4) Design a circuit to become BUNRI=L when the power supply is started up. The reset pulse might not be output when becoming BUNRI=H momentarily.

9.10 PCI Local Bus Buffers

The PCI (Peripheral Component Interconnect) local bus is an integrated standard for local bus architecture that improves the speed of bus lines where bottlenecks would otherwise occur as signals are arbitrated between the PC and its peripheral components. Since this bus standard has signal transfers performed mainly by reflected waves, standards must be specified for a wide array of factors, including not only the bus protocol but also the bus driver's electrical specifications, the types of wire patterns and connectors used on the PC board, and even the shape of the PC board.

This section describes the EP-1 series bus driver that complies with PCI LOCAL BUS SPECIFICATION REVISION 2.0/3 V.

Before creating PCI components for the EP-1 series, be sure to join the "PCI Special Interest Group" (PCISIG) since vendor ID and specific support will be needed.

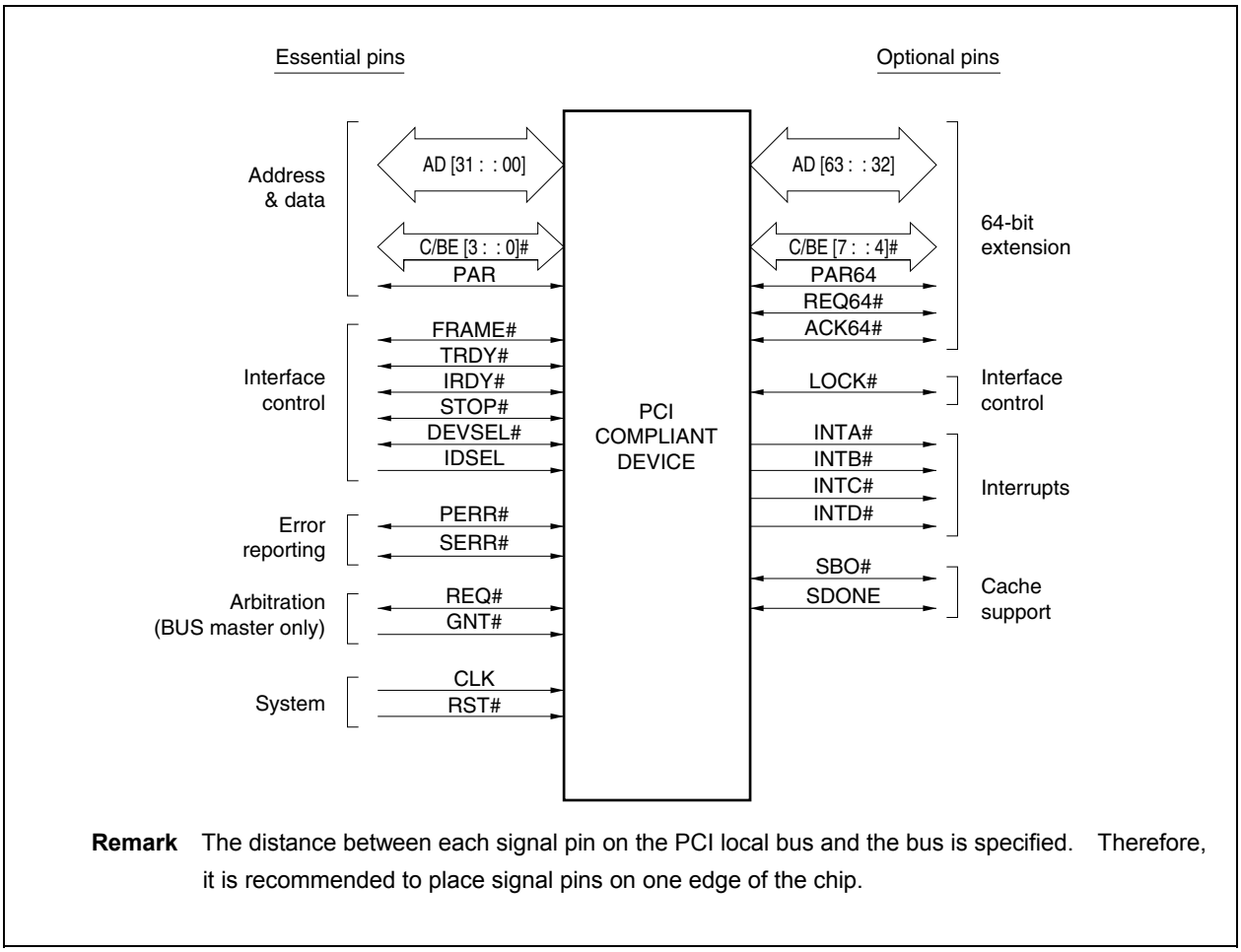
Specifications (standards) and other important documents can also be obtained from the PCISIG.

9.10.1 Signal specification of PCI local bus

The PCI interface requires that the target device have at least 47 pins that can be used as signal pins and that the bus master have at least 49 pins that can be used as signal pins in order to support implementation of an address/data line, interface control line, system signal line, and arbitration control line.

The pin list for the PCI local bus is shown below. For block list, refer to **Table 9-15 PCI Block**.

Figure 9-22. PCI Pin List



Remark The distance between each signal pin on the PCI local bus and the bus is specified. Therefore, it is recommended to place signal pins on one edge of the chip.

Table 9-15. PCI Block

(a) Blocks for 3.3 V PCI

3.3 V PCI Bus Driver	Full Type	Half Type
Input	BP3I	
Output	BP3O	FO01
3-state	BP3T	B008
Bidirectional	BP3B	B003
Open-drain	EXT5	

(b) Blocks for 5 V PCI

5 V PCI Bus Driver	Full Type
Input	BP5I
Output	BP5O
3-state	BP5T
Bidirectional	BP5B

Remark Full type: Blocks used with pin-to-bus (1-to-multiple)
Half type: Blocks used with pin-to-pin (1-to-1)

Notes on using 5 V PCI

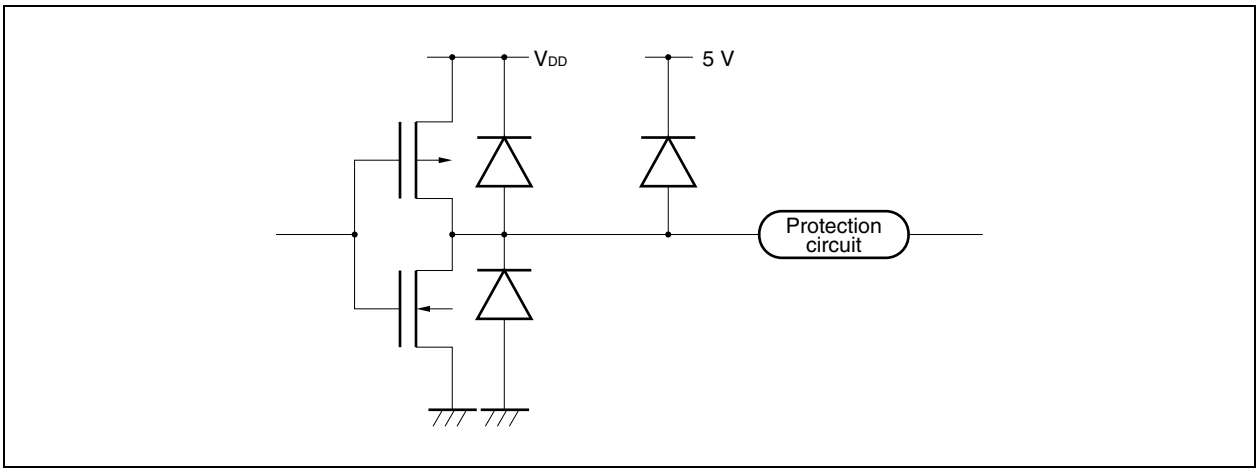
The 5 V PCI buffer has a clamping diode to protect the device from a reflection wave of 11 V (see **Figure 9-23 Equivalent Circuit Diagram of 5 V PCI Buffer**).
When using this buffer, therefore, a dedicated 5 V power supply pin for the clamping diode needs to be added.

The 5 V power supply is an additional power supply, and at least one must be located on the side of the chip on which the PCI buffer is located.
An additional 5 V power supply pin can be located anywhere on the side on which the PCI buffer is located. 5 V.

- Even if there are several PCI buffers on a side, at least one additional 5 V power supply can be located on that side (more than one is also possible).
- When there is a PCI buffer located on every side, a total of at least four additional 5 V power supply pins can be located; one (or more) on each side.

Caution The addition of a power supply is not related to reinforcing the power supply to prevent simultaneous operation.

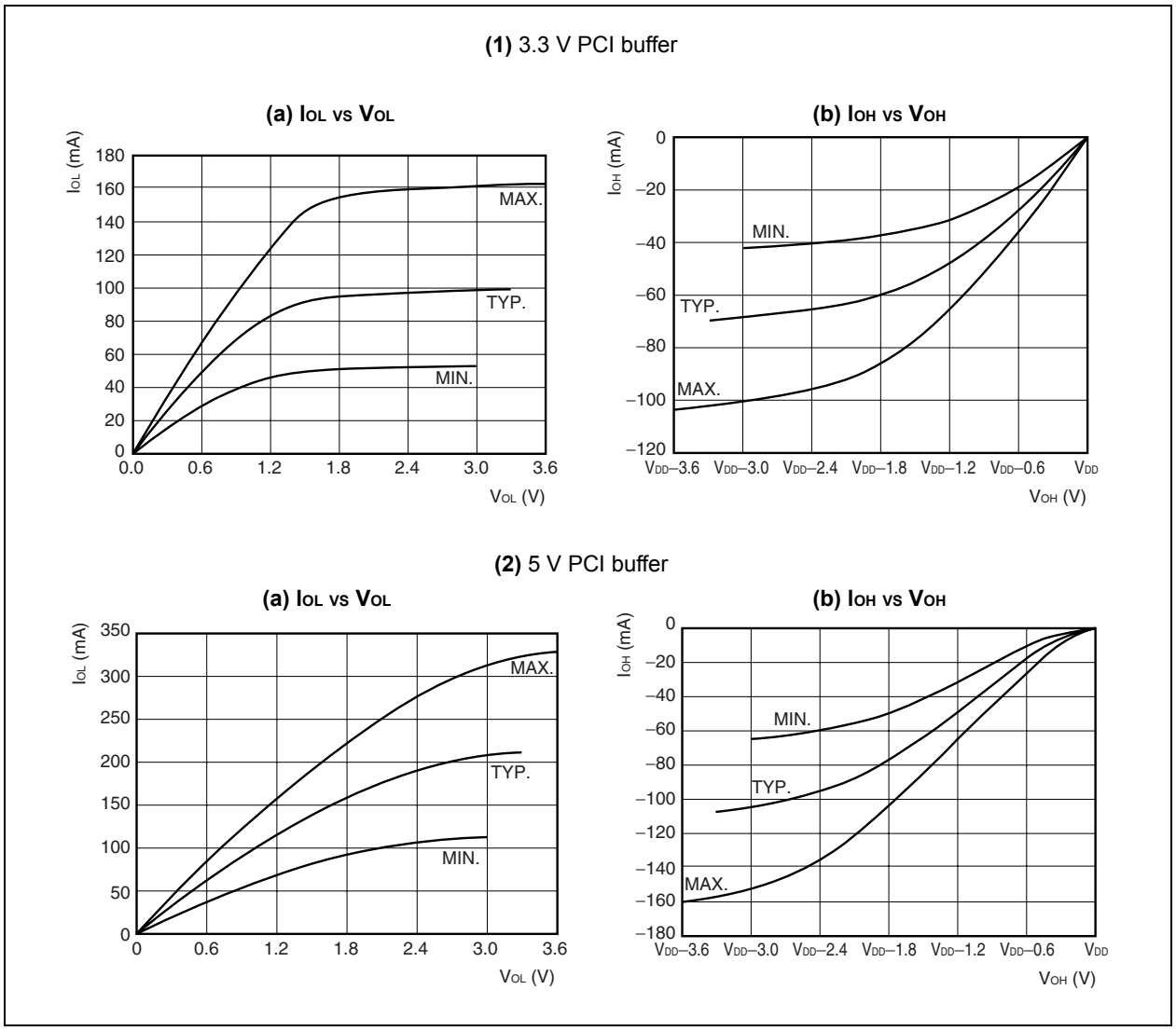
Figure 9-23. Equivalent Circuit Diagram of 5 V PCI Buffer



9.10.2 PCI buffer output current

The curve of I_O vs. V_O is shown in Figure 9-24.

Figure 9-24. I_O vs. V_O (PCI Buffer)



9.10.3 Electrical specifications

To use the PCI buffer, signal flow in the transmission path must be evaluated in advance. It requires some knowhow to do this.

The DC characteristics and pin capacitance, etc. conform to PCI LOCAL BUS SPECIFICATION REVISION 2.0/3 V.

9.11 Memory

In the EP-1 series, the gate array type memory block and cell-based IC-type memory macros can be included. This section explains the types of memory blocks and the points to be noted in using the memory blocks.

9.11.1 Gate array type memory

The gate array type memory blocks listed in Table 9-16 are available in the EP-1 series.

Table 9-16. List of Memory Blocks

(a) High-density 1-port RAM

	16	32	64	128	256	512	1024	2048	4096 [word]
4	RB47	RB49	RB4B	RB4D	RB4F	RB4H	RB4M	RB4S	RB4U
8	RB87	RB89	RB8B	RB8D	RB8F	RB8H	RB8M	RB8S	
10			RBAB	RBAD	RBAF	RBAH	RBAM	RBAS	
16	RBC7	RBC9	RBCB	RBCD	RBCF	RBCH	RBCM		
20			RBEB	RBED	RBEF	RBEH	RBEM		
32	RBH7	RBH9	RBHB	RBHD	RBHF	RBHH			
40 [bit]			RBKB	RBKD	RBKF	RBKH			

(b) High-density 2-port RAM (W+ R)

	16	32	64	128	256	512	1024	2048	4096 [word]
4	R947	R949	R949	R94D	R94F	R94H	R94M	R94S	R94U
8	R987	R989	R989	R98D	R98F	R98H	R98M	R98S	
10			R9A9	R9AD	R9AF	R9AH	R9AM	R9AS	
16	R9C7	R9C9	R9C9	R9CD	R9CF	R9CH	R9CM		
20			R9E9	R9ED	R9EF	R9EH	R9EM		
32	R9H7	R9H9	R9H9	R9HD	R9HF	R9HH			
40 [bit]			R9K9	R9KD	R9KF	R9KH			

(c) ROM

	128	256	512	1024	2048 [word]
4	J14DK	J14FK	J14HK	J14MK	J14SK
8	J18DK	J18FK	J18HK	J18MK	J18SK
16	J1CDK	J1CFK	J1CHK	J1CMK	J1CSK
32		J1HFK	J1HHK		
2048 [bit]				J1HMK	J1HSK

9.11.2 Cell-based IC type memory

- Compiled RAM

In cell-based IC type memory, the following range of bit/word combinations can be selected.

Table 9-17. Cell-Based IC-Type Compiled RAM Correspondence List

Access Method	Type	Number of Bits/Words
Synchronous	High-speed 1-port RAM	1 to 32/32 to 2 K
	High-speed 2-port RAM (RW + R)	1 to 32/32 to 2 K
	High-density 1-port RAM	1 to 32/16 to 2 K
	High-density 2-port RAM (W + R)	1 to 32/32 to 1 K

Refer to the **EA-9HD Series Memory Macro Design Manual (A13367E)** concerning calculation of the macro size.

- High-speed ROM (synchronous type)

For details of the High-speed ROM (synchronous type), see **EA-9HD Series Memory Macro Design Manual (A13367E).**

9.11.3 Gate array type RAM

As shown in Figure 9-25 and Figure 9-26, the high-density RAMs have a bit/word architecture based on basic macros (hard macros). The test circuit BIST: Built-in Self Test and built-in selector are configured by soft macros. This architecture eases restrictions on placement and routing, and reduces complexity when multiple RAMs are placed.

The memory test is included in the BIST soft macro. Only 3 pins are necessary for the test and there is no need of taking the trouble to directly input to and output from all the pins.

When RAM of NEC Electronics is used, be sure to use the NEC Electronics standard test circuit (BIST).

Figure 9-25. 1-Port RAM Circuit Configuration

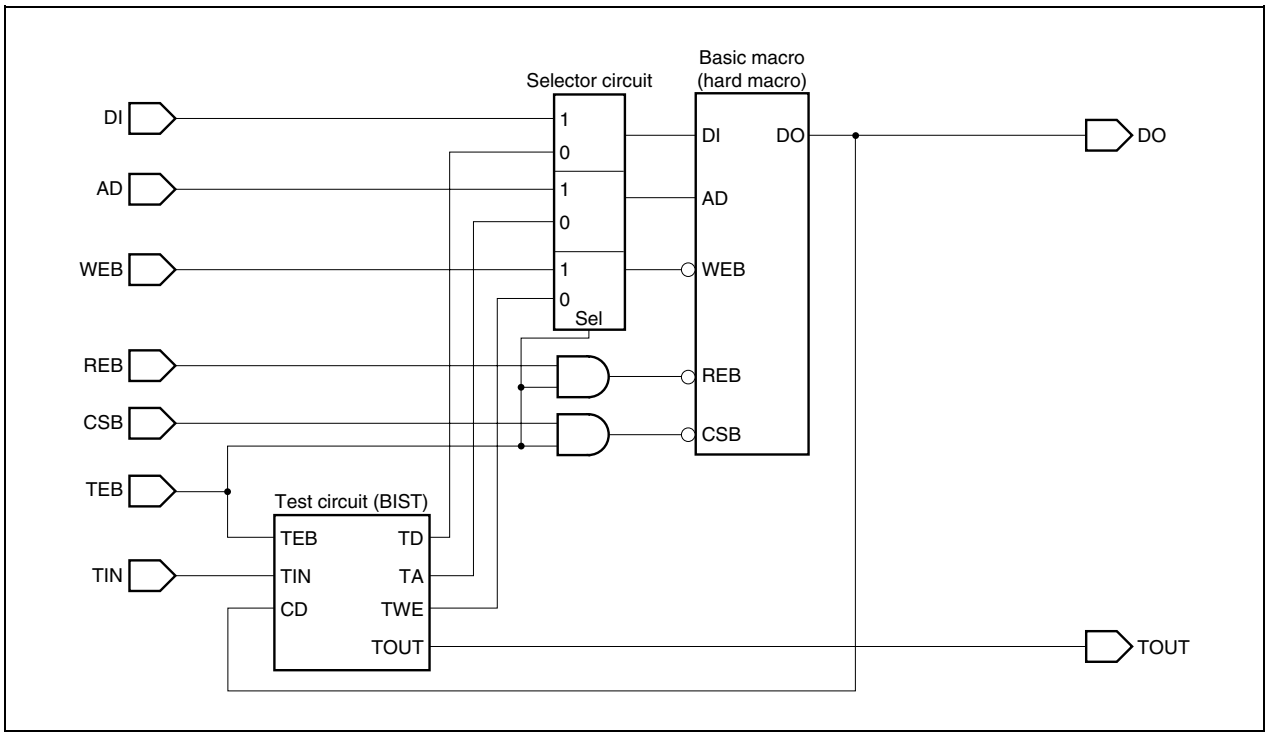
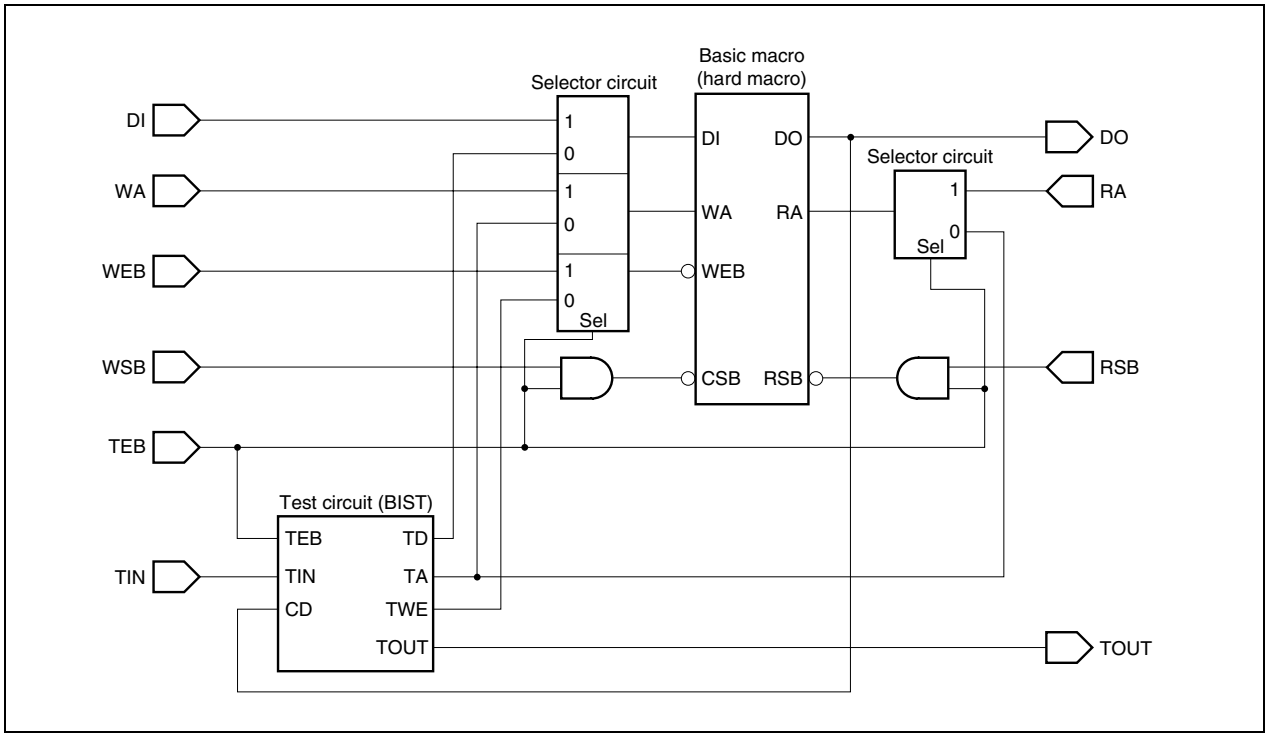


Figure 9-26. 2-Port RAM (W+ R) Circuit Configuration



9.11.4 Cell-based IC type RAM

Refer to the **EA-9HD Series Memory Macro Design Manual** (**A13367E**) for EA-9HD Series cell-based IC type memory macro.

9.11.5 Selection of gate array type memory

In the EA-9HD Series, gate array type RAM blocks are configured as soft macros. Therefore, RAM blocks with any bit/word configuration can be freely placed by combining the basic memory cells. However, certain frequently used blocks have already been registered as a simulation model (refer to **EA-9HD Series Memory Macro Design Manual** (**A13367E**)). Therefore, you should select and use blocks among these representative models whose size is closest to the desired bit/word size.

If there is no memory block in the desired size, such as when there are too many bits (RAM: 40 bits, ROM: 32 bits), consider connecting in parallel blocks having the same word size but different bit sizes.

Conversely, if there are too many words, use a decoder or other component to create a chip select signal as is done for ordinary memory circuits, then allocate the addresses.

When using memory in which the number of bits does not match the number of words, use soft macros instead, as described above. Contact NEC Electronics concerning the circuit configuration and test circuit (BIST) configuration.

9.11.6 Using gate array type memory

As with other function blocks, there are rules concerning fan-in (F/I) and fan-out (F/O) (refer to **EA-9HD Series Memory Macro Design Manual** (**A13367E**)). Make sure that the connections do not exceed fan-out limits, etc.

9.11.7 Using cell-based IC type memory

Since the EA-9HD Series cell-based IC type RAM block is made of a base wafer, the bit/word configuration can be changed as long as it does not exceed the limit. For details, refer to the **EA-9HD Series Memory Macro Design Manual** (**A13367E**).

9.11.8 Gate array type RAM test

Using the BIST function to test RAM blocks in the EA-9HD Series eases the restriction on the number of test patterns and makes it easier for users to perform memory checks.

As shown in Figure 9-27, the BIST function includes test signal generators that generate test addresses, test data, and test enable signals as well as a comparator that compares the output of the signal generators against the output of the expected value generator. User set up to perform RAM tests is done by simply connecting three pins: TIN, TEB, and TOUT, to external pins. When several RAM blocks have been mounted, the test inputs (TIN and TEB) can be shared with corresponding pins on other RAM blocks. The test output (TOUT) cannot be shared. It must be connected to a different external pin. Figure 9-28 shows a connection example.

When performing RAM tests, the basic idea is to send data directly from external input pins to the test inputs (TIN and TEB) and to retrieve the data from the test output (TOUT) via a direct connection to an external pin. If inverters or flip-flops are used instead of direct connections, the configuration must then include signal inversion, clocking, and the like, which makes it impossible to use the basic test pattern. The final state of any user-provided test pattern must be usable for RAM testing (i.e., the TIN, TOUT, and TEB pins must be able to handle RAM test signals sent directly from external pins). NEC Electronics will provide the RAM test patterns.

Figure 9-27. Test Circuit (BIST) Block Diagram

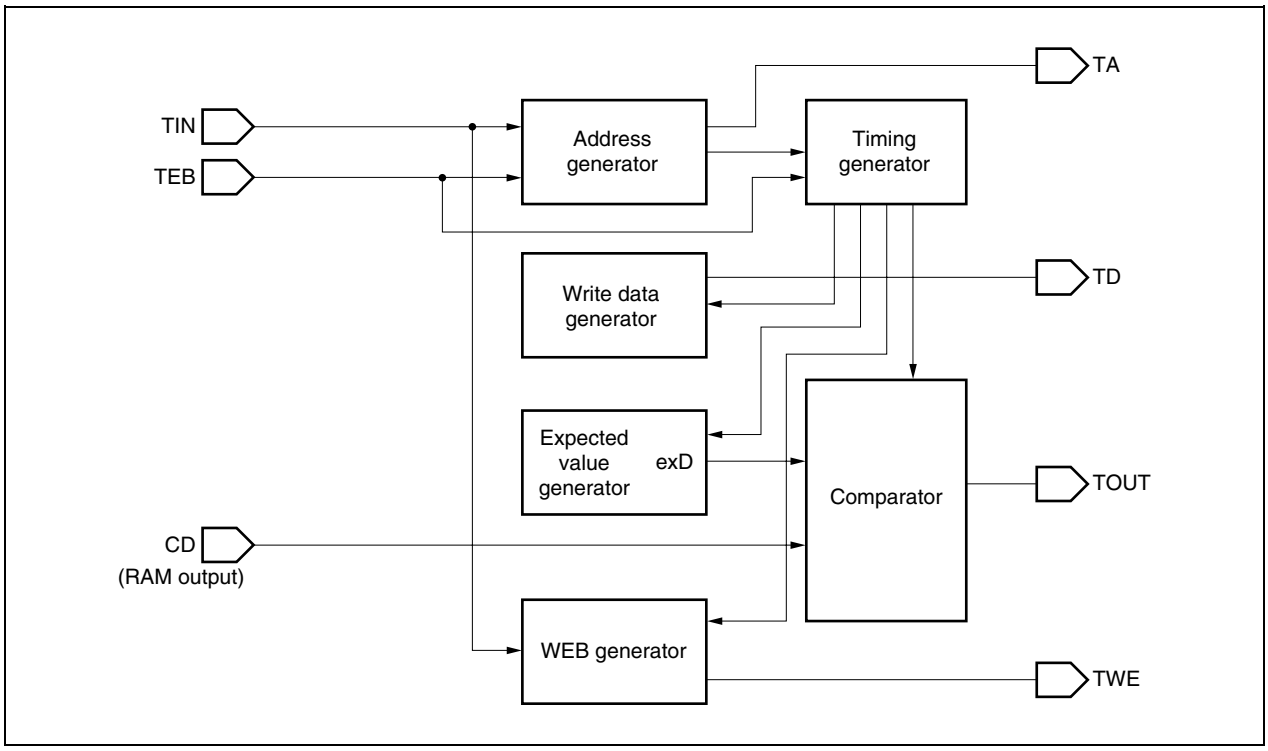
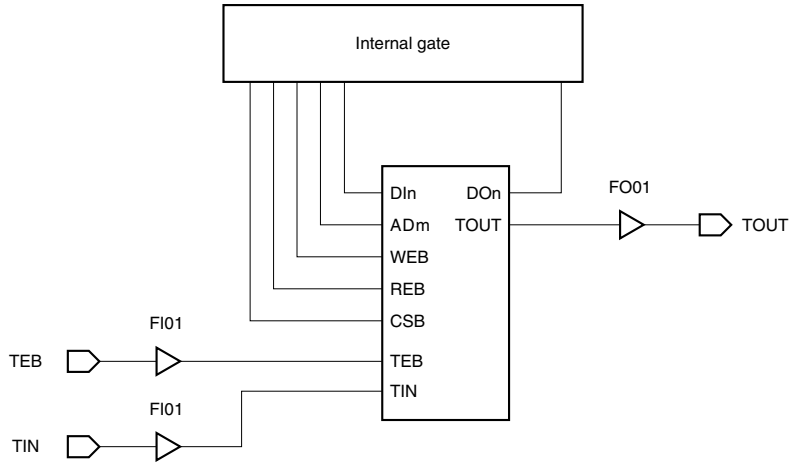
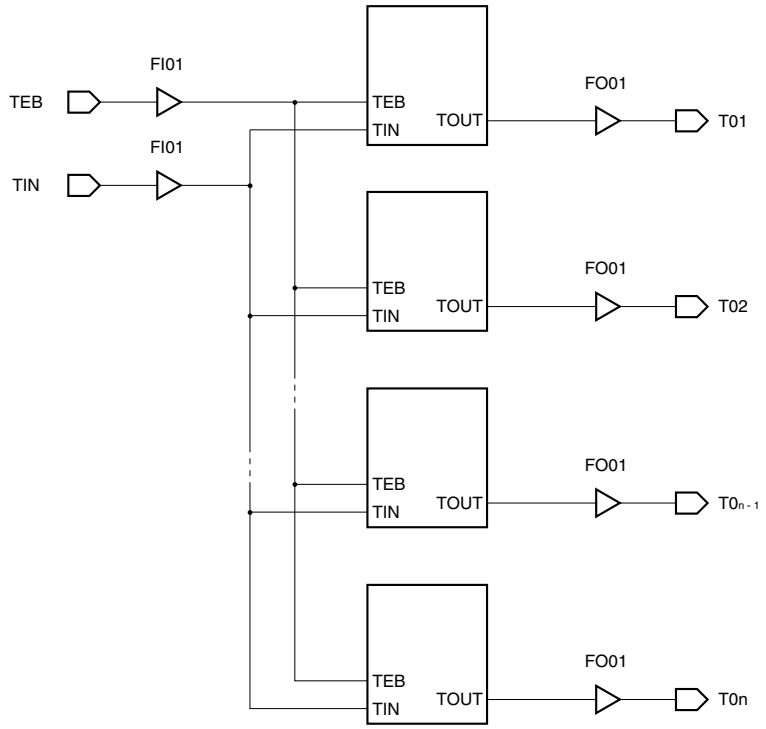


Figure 9-28. Example of RAM Test Circuits

(a) Connection example for placing one RAM block



(b)Connection example for placing multiple RAM blocks



(1) Integrate the TEB input and TIN input as one pin and connect it to the respective RAM. Even when the RAM blocks have different capacities, each TEB input and TIN input is shared with the other TEB inputs and TIN inputs.

(2) Each TOUT pin outputs to a separate external pin.

9.11.9 Cell-based IC type RAM test

Cell-based IC type RAM testing can be carried out with BIST. However, cell-based IC type RAM does not include BIST. It is necessary, therefore, to connect BIST at the circuit design stage.

For the connection between RAM and BIST, refer to the **EA-9HD Series Memory Macro Design Manual** (**A13367E**). Consult NEC Electronics when using BIST together with a test bus.

9.11.10 Setup of test I/O pins (TIN, TEB, and TOUT)

(1) Gate array type memory

(a) If there are unused pins

If there are any unused pins other than power supply pins or NC pins, use those pins for testing.

(b) If there are no unused pins

Certain pins that are already being used can be shared as test pins. Note the following when deciding which pins to set up as shared pins. Note that the TEB pin cannot be shared and another pin must be set up as a dedicated pin.

<1> Shared TIN pin: This pin can be shared with ordinary input pins or ordinary output pins. When sharing a TIN pin with an ordinary output pin, use the pin as a bidirectional pin for the TEB signal as the enable signal, use it as an output pin for normal usage, and as an input pin for testing. In addition, fix test pattern terminal to low level in this case. Figure 9-29 shows a connection example.

<2> Shared TOUT pin: This pin can also be shared with ordinary input pins or ordinary output pins. When sharing a TOUT pin with an ordinary input pin, use the pin as a bidirectional pin for the TEB signal as the enable signal, use it as an input pin for normal usage, and as an output pin for testing. When sharing this pin with an ordinary output pin, use an internal selector circuit for switching via the TEB signal. Figure 9-30 shows a connection example.

Caution The test I/O pins cannot be alternately used as pins that use the GTL+ interface buffer, Nch open-drain buffer, or CMOS 5 V tolerant output buffer.

(c) Handling on board

Select one method from the following for handling the TEB and TIN pins.

Handling of TEB pin[Note 1]

- Use a pull-up buffer
- Pull it up externally
- Connect it to V_{DD} externally

Handling of TIN pin[Note 2]

- Use a pull-up buffer
- Use a pull-down buffer
- Connect it to V_{DD} externally
- Connect it to GND externally

Notes 1. Not in test mode

2. Handling is required when the TIN pin does not have an alternate function as a normal pin.

(2) Cell-based IC type memory

For setup of the TIN, TEB, and TOUT pins of the cell-based IC type memory macro, refer to **EA-9HD Series Memory Macro Design Manual** (**A13367E**).

Consult NEC Electronics when using BIST together with a test bus.

Figure 9-29. Making TIN Pin Alternate Function

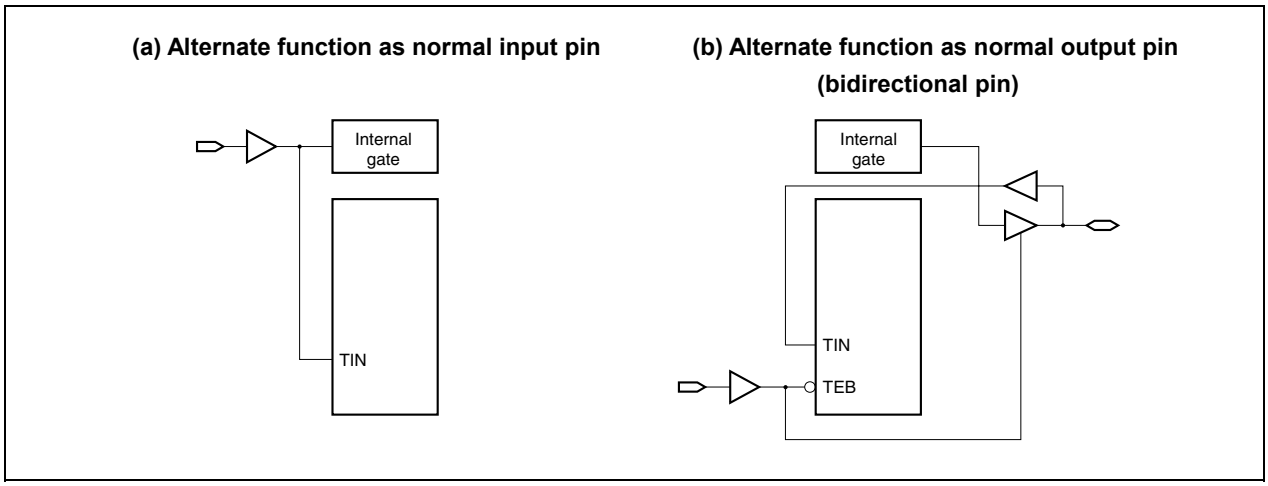
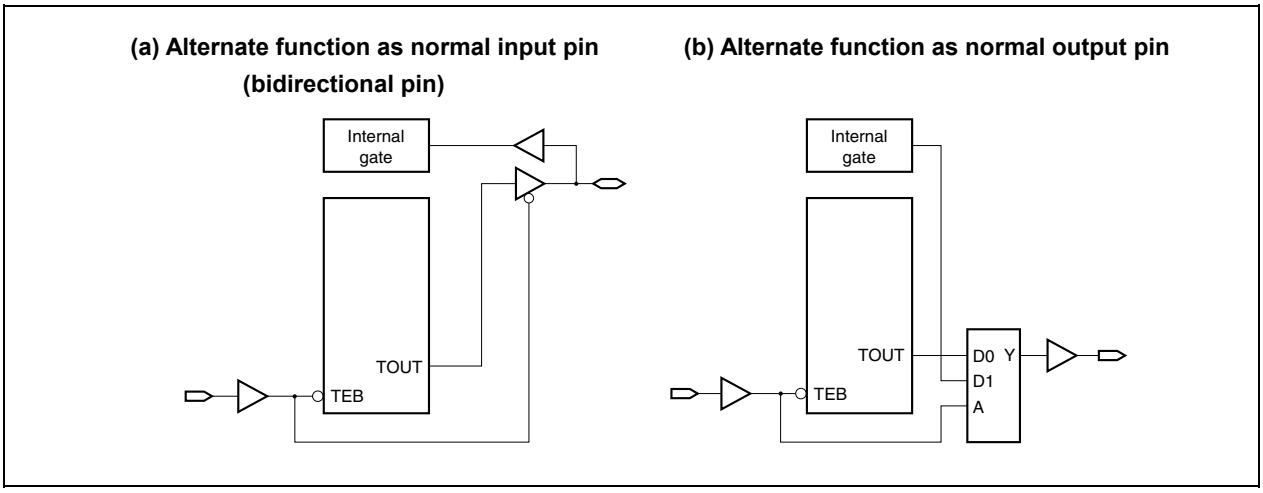


Figure 9-30. Making TOUT Pin Alternate Function

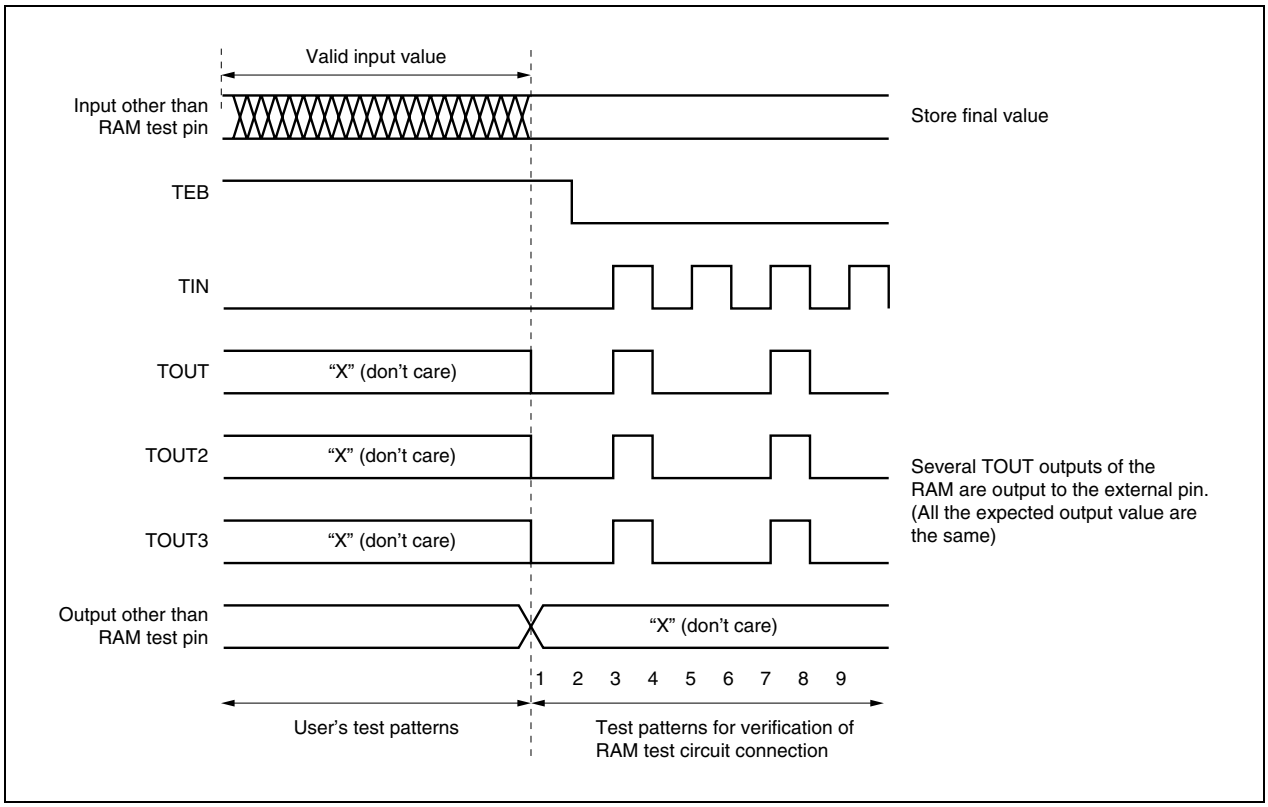


9.11.11 RAM test circuit connection check

To check whether or not the BIST circuit is properly connected, carry out checking by RAMCHK flow on OPENCAD generating and adding the connection confirmation patterns (nine patterns) as shown in Figure 9-31 to the end of the user-provided test pattern (Test pattern for DC check: if the DC pattern is independent, then it is this pattern) by using OPENCAD RAMCHK. Be sure to perform RAMCHK before submitting the test pattern to NEC Electronics. In addition, set the status in which input and output for the pin signals required to the BIST test (TEB, TIN, and TOUTx) can be executed at the end of the test pattern (Test pattern for DC check: if the DC pattern is independent, then it is this pattern.) When sharing a TIN pin with an ordinary output pin, fix test pattern terminal to low level.

The RAM-BIST test pattern is provided by NEC Electronics and thus the user does not need to generate it.

Figure 9-31. Example of Test Patterns



(1) Input other than RAM test pin: Input 9 patterns in such a way that the final value of the user test pattern is preserved.

(2) TEB: First input a high level for 1 pattern and then input a low level for 8 patterns.

(3) TIN: First input a low level for 1 pattern and then input 8 patterns of repetitive 01 signal.

(4) TOUT: Set the expected output value to 001000100. When multiple RAM is placed, several TOUT outputs of the RAM must be output to the external pins (the RAM test is executed completely in parallel).

(5) Output other than RAM test pin: Set the expected output value to "X" (don't care).

Remark The connection check pattern of BIST is automatically generated by RAMCHK and thus it is not necessary to add it to the user's patterns in advance.
In addition, simultaneous checking can be carried out by connecting TIN and TEB in common in the gate array type RAM and cell-based IC type RAM.
For more information, refer to the **EA-9HD Series Memory Macro Design Manual (A13367E)**.

9.11.12 ROM tests

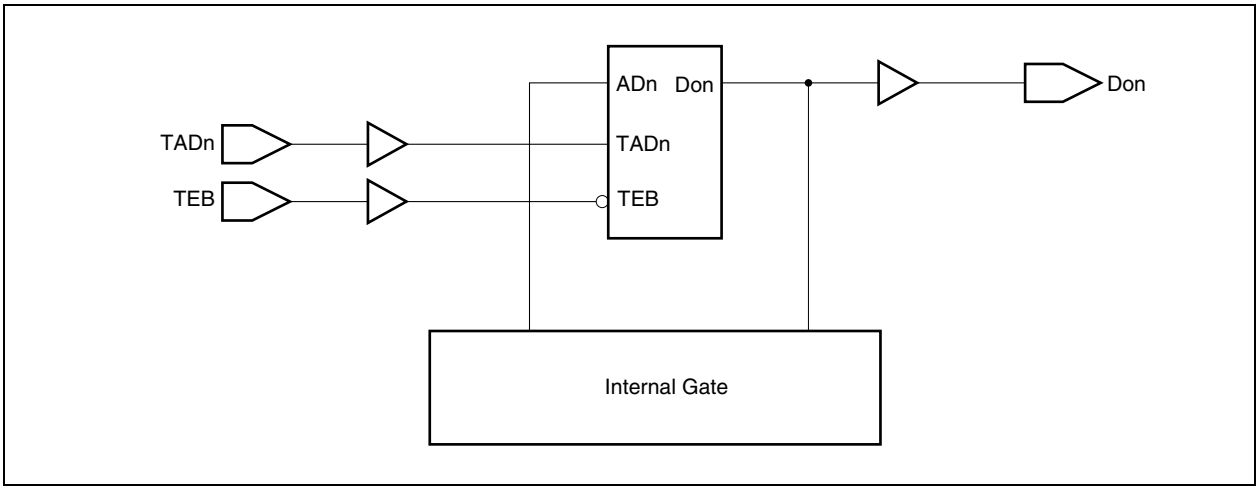
The ROM block has the test address. Turning on and off the test enable signal (TEB) switches between the real and test modes. If it is difficult to conduct ROM tests within the user-designed circuit, design a scheme that enables ROM tests to be conducted directly from external pins, as shown in Figure 9-32.

The user should prepare ROM test patterns.

ROM tests should read and check all memory contents with ROM codes. NEC Electronics does not check the ROM codes. The user should include this check in the test patterns.

See Section **9.11.13 ROM code format** for ROM code generation.

Figure 9-32. ROM Test Circuit Example



9.11.13 ROM code format

Either NINCF or extended Intel hex can be used as the interface data format for the ROM code.

> All ROM code bits must be defined as either input or output pins.
> For example, if an area of 990 bytes are used in a 1K byte ROM, the user should specify also the remaining 34 bytes in the interface data file.

NINCF format :	NEC Electronics-defined format, handling data of undefined length
Extended Intel hex format :	World-standard ROM code, only applicable to byte data. Extended Intel hex format can handle 16-bit data.

(1) Incorporating the ROM code into a simulation system

Merely registering a ROM in a simulation library does not make it usable. The ROM code must be incorporated into the simulator before staring simulation.

The method for ROM code incorporation depends on the simulator. An example follows.

V.sim : NINCF format only.
The ROM code is incorporated at the beginning of simulation using the mr command.

Verilog : The ROM code is converted from the extended Intel hex or NINCF format to the Verilog format. The Verilog format allows both hex and binary descriptions. In the ROM macro library, the ROM code is specified by $READMEMH (hex format) or $READMEMB (binary format).

(2) NINCF

The NINCF file is a text file with a fixed format shown in Figure 9-33.

Although ASCII codes can be entered using a text editor, have the NINCF file created automatically to avoid chances of error.

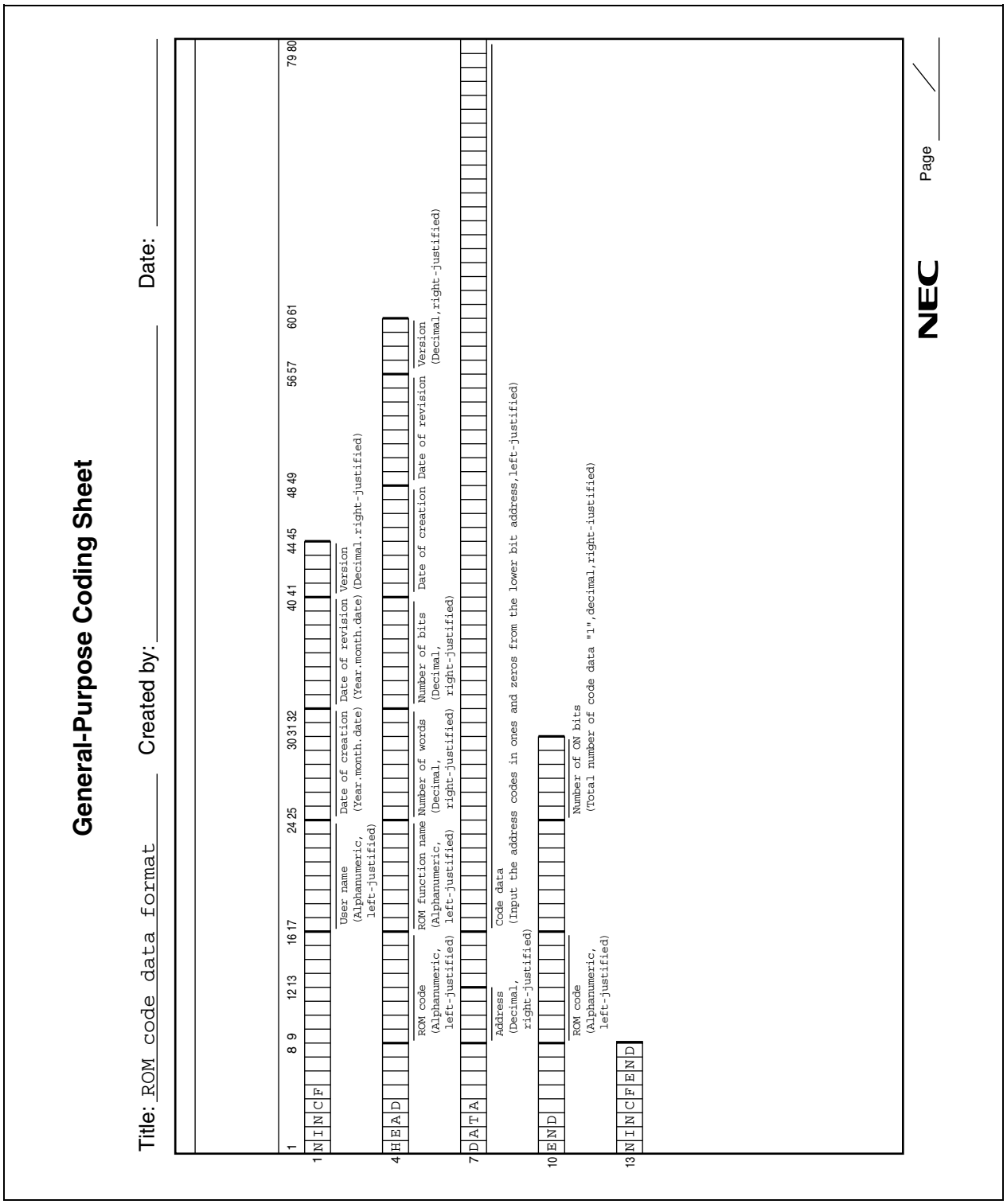
A utility program is available for automatic conversion from the extended Intel hex format.

(3) ROM code generation

Describe ROM code in the format shown in Figure 9-33 below.

Note that because this is a fixed-column format, the columns must not be shifted when describing.

Figure 9-33. Format of ROM Code Data

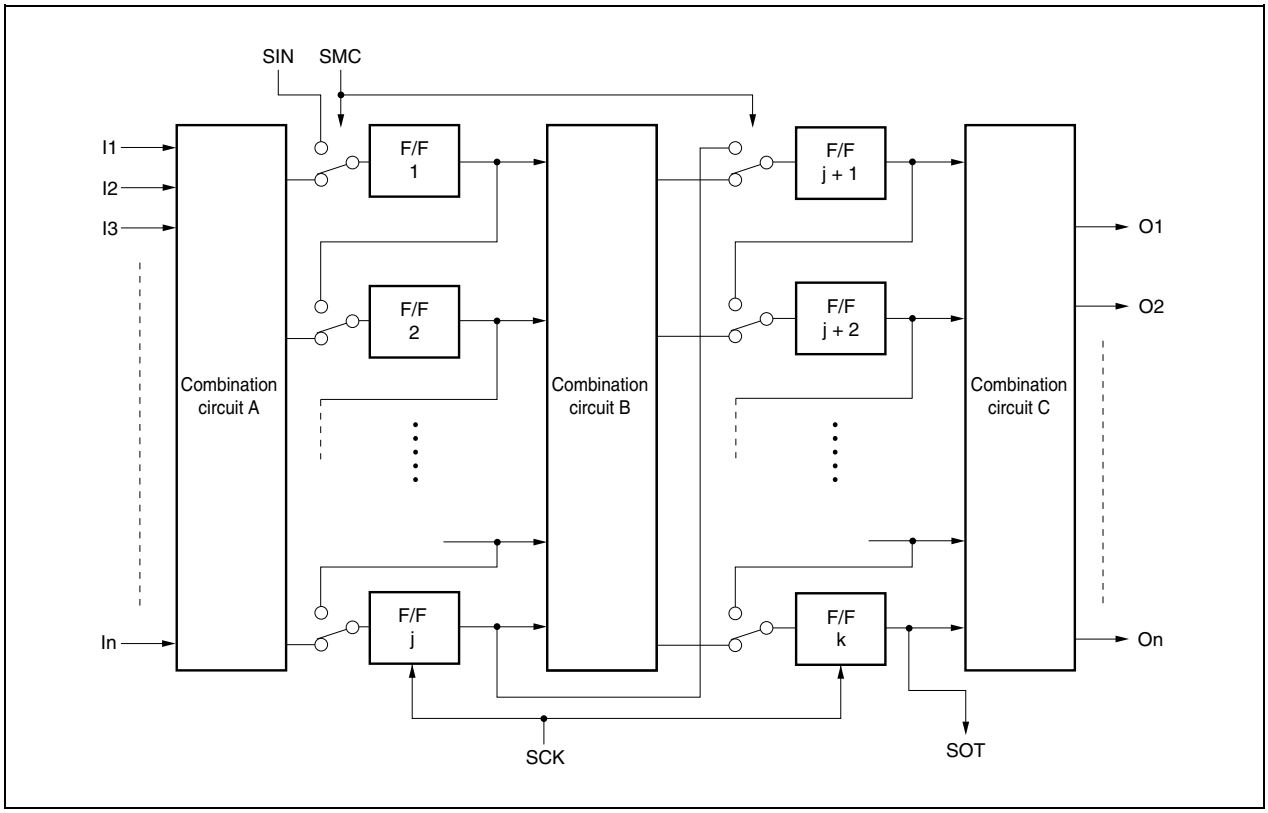


9.12 Scan Path Test

It is extremely difficult to generate a test pattern that checks the operation of an LSI efficiently with a circuit that frequently uses flip-flops (F/F) and that has a deep logical depth. Scan path testing can change the connections of all the internal flip-flops of LSI-like shift registers. Therefore, the circuit can be tested efficiently by easily initializing all the flip-flops of a circuit with a deep logical depth and reading all the flip-flop states in a certain state.

For details, see **NEC SYSTEM LSI DESIGN Design For Test User's Manual**.

Figure 9-34. Theory of Scan Path Test Method



Remark In: Input signal when testing a combination circuit, or normal input
On: Diagnostic output when testing a combination circuit, or normal output
SIN: Input signal when testing a sequential circuit
SMC: Mode switching signal
SCK: Test clock
SOT: Diagnostic output when testing a sequential circuit

9.13 Boundary Scan Test

In recent years, connections among LSIs on boards have become very complex due to the trend towards multilayer boards, more pins per LSI chip, etc., which has had the effect of making LSI-related testing more complex.

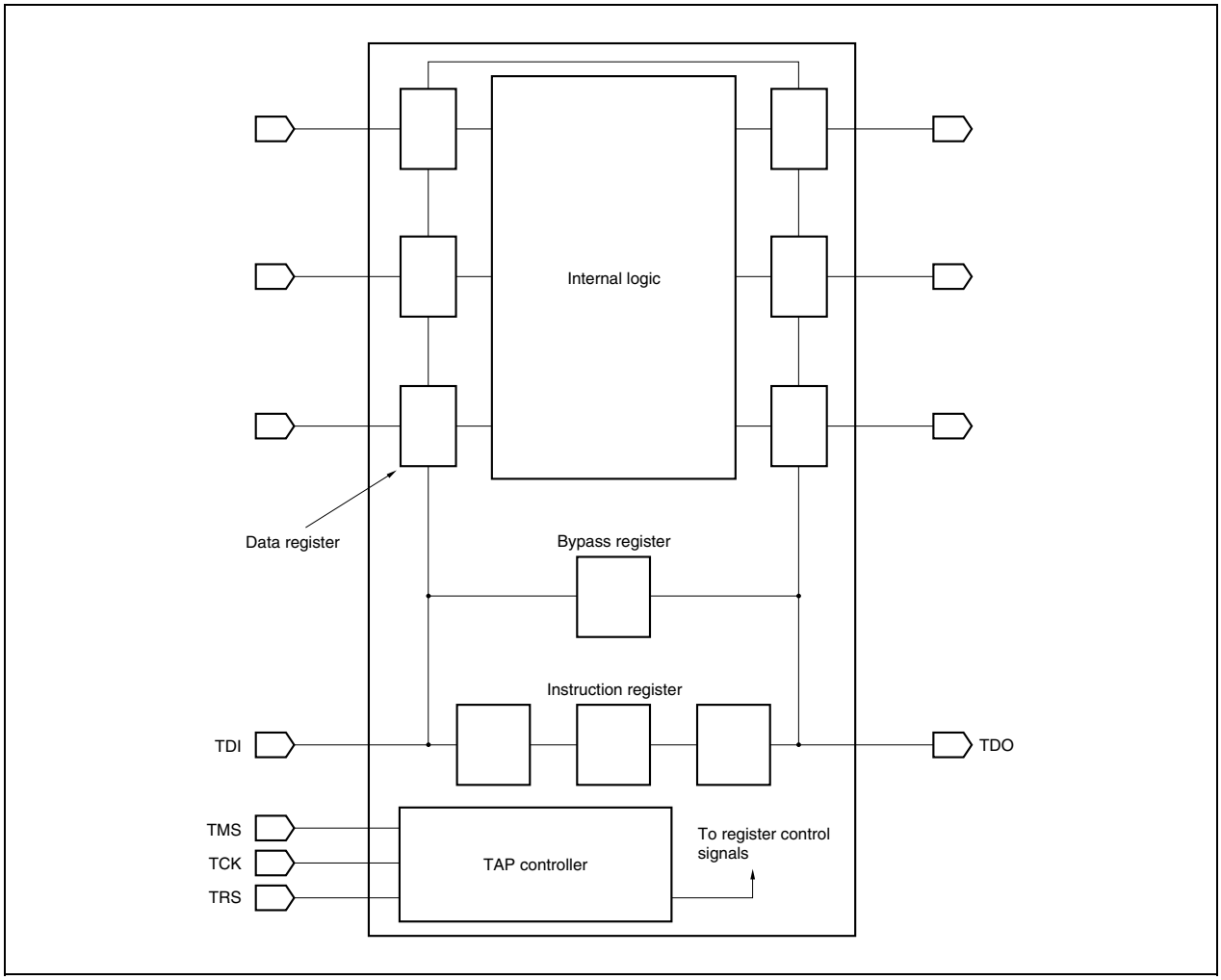
The boundary scan test method is an easy, highly reliable test method based on IEEE's 1149.1 standard.

This test makes it possible to check LSI connections, etc., by inputting and outputting test data with the dedicated register as if successively scanning the LSI input/output pins.

As can be seen in Figure 9-35, a boundary scan circuit includes dedicated buffers and data registers located between the LSI's internal logic and its external pins. These data registers can be used to measure values and control input and output at each pin. In other words, the data registers function in the same way as conventional test probes (the data registers are connected in serial).

For details, see **NEC SYSTEM LSI DESIGN Design For Test User's Manual**.

Figure 9-35. Boundary Scan Circuit Diagram



CHAPTER 10 CAUTIONS ON USE OF 5 V FULL-SWING BUFFER

This chapter provides cautions to be observed when placing 5 V full-swing buffers.

10.1 Placement Restrictions

An I/O cell is configured such that a different power source can be supplied for each side. At the EP-1 series gate array block, the side interfaced to the CPU side is used exclusively by a 3.3 V power supply, so a 3.3 V or 5 V power supply can be selected for the other three sides.

Note that the number of pins that can be used differs for each side depending on the signal interfaced to the CPU side.

10.2 Placement Conditions

<1> 3.3 V and 5 V signals cannot coexist within the three I/O groups that are divided for each side.

<2> When using a 5 V signal, an oscillation block cannot be used.

10.3 Special Handling

When using 5 V full-swing signals, contact NEC Electronics since a special request is needed.

<R>

CHAPTER 11 PACKAGES

The PFESiP EP-1 Series packages are outlined in this chapter.

Because the various packages are prepared every master, please choose the most suitable package in view of the specifications of the circuit.

11.1 Package Outline

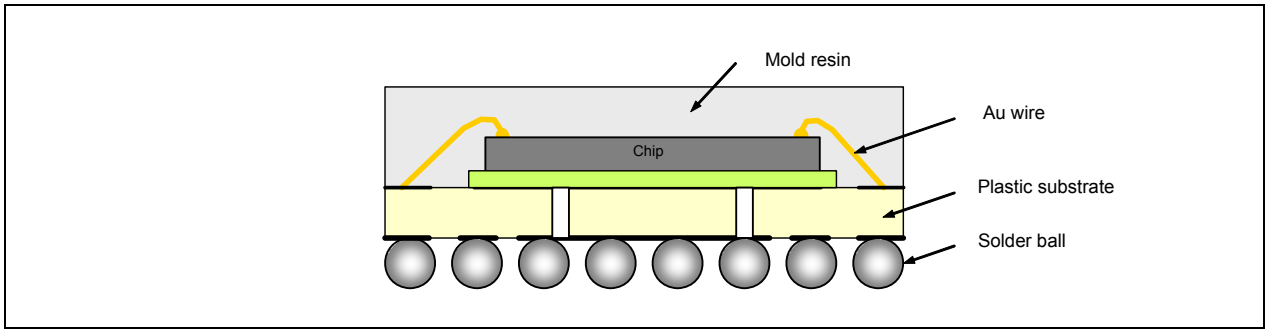
11.1.1 PBGA (Plastic BGA)

PBGA (Plastic BGA) is a BGA where solder balls are arranged using a pitch of 1.0 mm or more.

Compared with other packages, Plastic BGA has a smaller body size so that the mounting surface can be made smaller.

Plastic BGA is a basic wire bonded BGA that uses a plastic board as the interposer and offers excellent cost performance.

Figure 11-1. PBGA Cross-Section Diagram



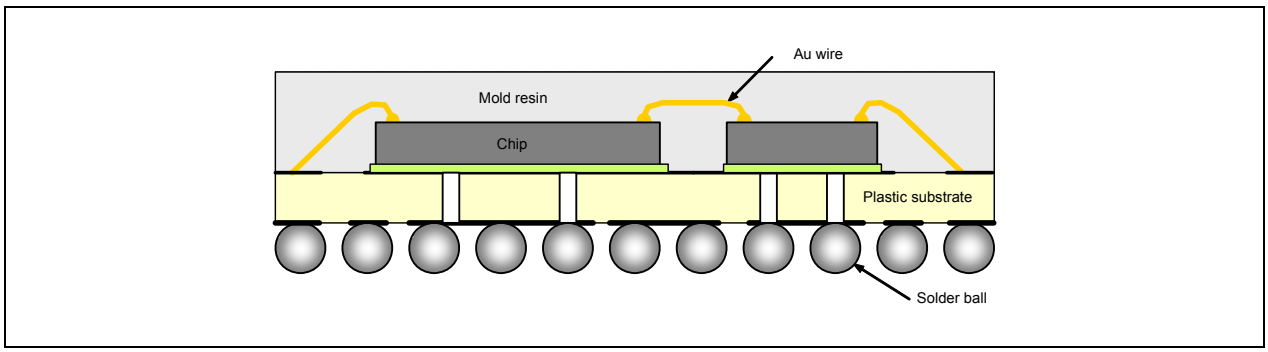
11.1.2 FPBGA (Fine-pitch BGA)

FPBGA (Fine-pitch BGA) is a plastic BGA where solder balls are arranged using a pitch of less than 1.0 mm.

11.2 PFESiP Structure

CPU function chip and EA-9HD Series chip are arranged in a horizontal direction, and they are connected by a direct bonding.

Figure 11-2. PFESiP Cross-Section Diagram



11.3 Lineup

The number of the usable user pins is different every package. Please choose it according to circuit specifications.

Table 11-1. Packages (16-bit External Bus)

Master	PBGA	FPBGA	
	464 pins (25 × 30 mm)	452 pins (22 × 22 mm)	433 pins (17 × 17 mm)
	1.00 mm ball pitch	0.80 mm ball pitch	0.65 mm ball pitch
MC-10501	○	No development plan	No development plan
MC-10502	○	○	To be planned
MC-10503	○	○	No development plan

Table 11-2. Packages (32-bit External Bus)

Master	PBGA
	550 pins (25 × 30 mm)
	1.00 mm ball pitch
MC-10505	○
MC-10506	○
MC-10507	○

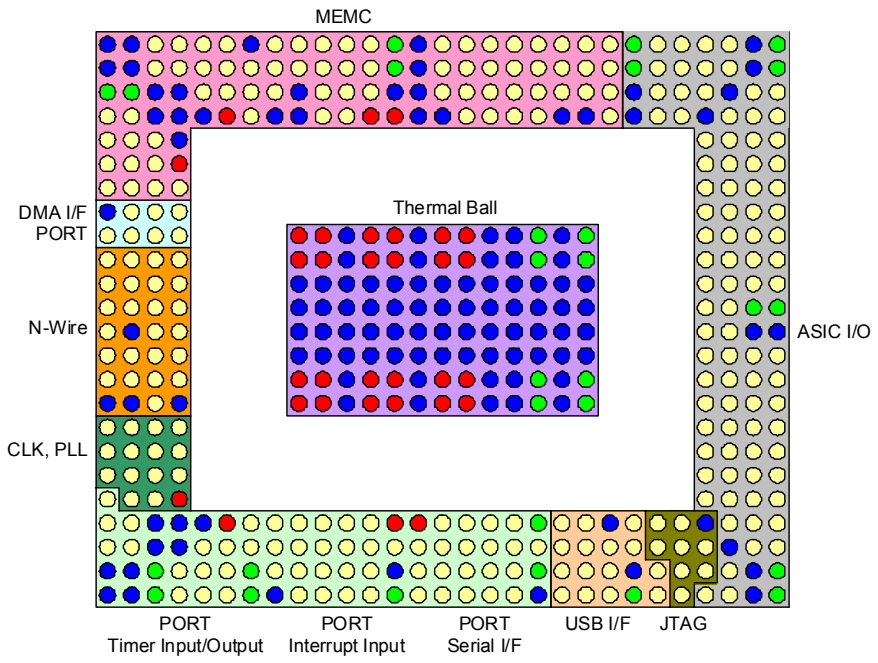
11.4 Pin Placement

The pin placement for each package is shown below.
For the CPU terminal function, see **2.3 I/O Interface**.

11.4.1 464-pin PBGA

(1) V_{DD33}, V_{DD15}, and GND pin placement

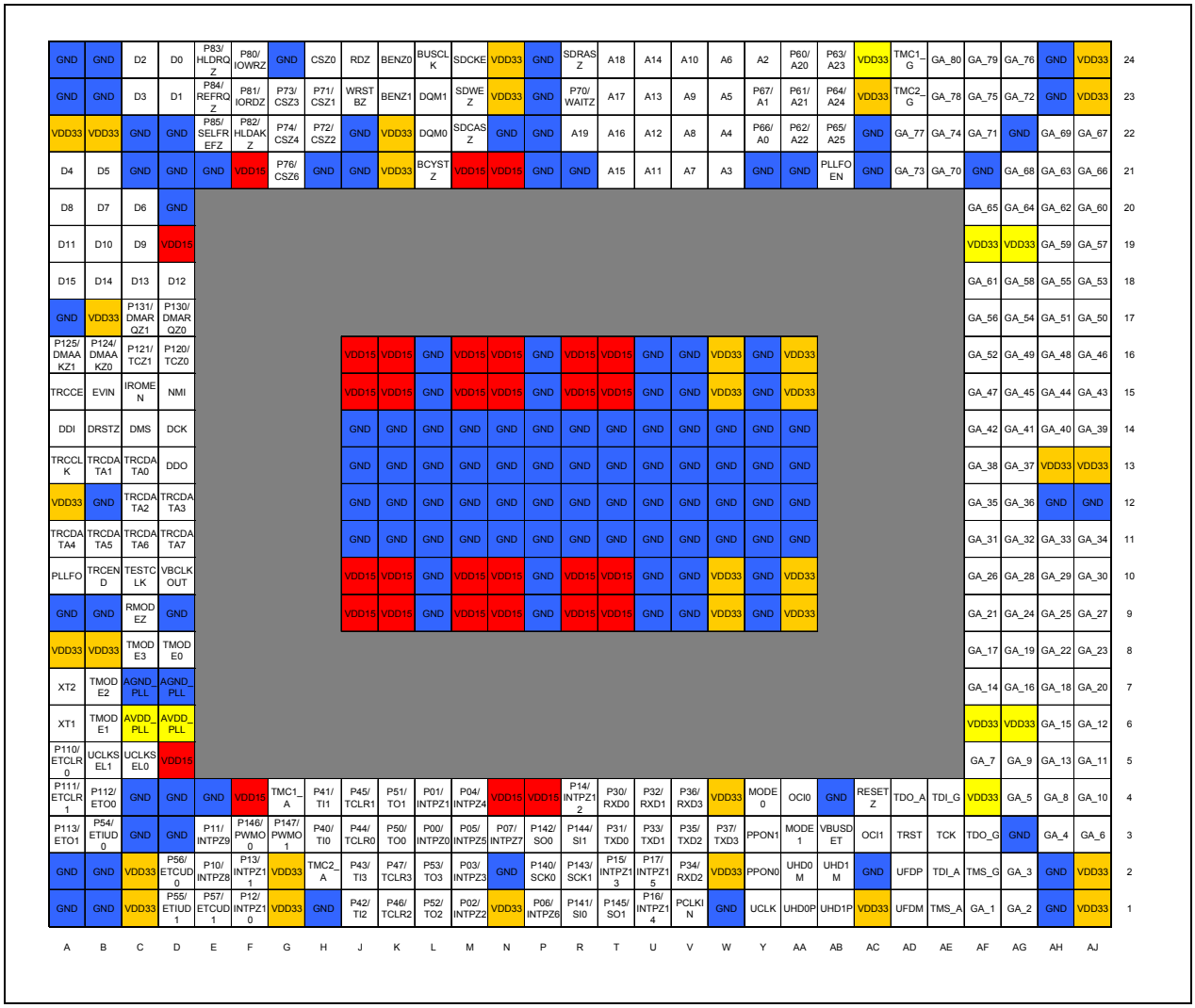
Figure 11-3. 464-pin PBGA (V_{DD33}, V_{DD15}, and GND Pin Placement)



●GND	●V_{DD15}	●V_{DD33}	●Signal
125	32	28	279

(2) Pin placement

Figure 11-4. 464-pin PBGA (Pin Placement: Top View)



Pin no.	Pin ID	Name
1	A1	GND
2	B1	GND
3	C1	V_{DD33}
4	D1	P55/ETIUD1
5	E1	P57/ETCUD1
6	F1	P12/INTPZ10
7	G1	V_{DD33}
8	H1	GND
9	J1	P42/TI2
10	K1	P46/TCLR2
11	L1	P52/TO2
12	M1	P02/INTPZ2
13	N1	V_{DD33}
14	P1	P06/INTPZ6
15	R1	P141/SI0
16	T1	P145/SO1
17	U1	P16/INTPZ14
18	V1	PCLKIN
19	W1	GND
20	Y1	UCLK
21	AA1	UHD0P
22	AB1	UHD1P
23	AC1	V_{DD33}
24	AD1	UFDM
25	AE1	TMS_A
26	AF1	GA_1
27	AG1	GA_2
28	AH1	GND
29	AJ1	V_{DD33}
30	AJ2	V_{DD33}
31	AJ3	GA_6
32	AJ4	GA_10
33	AJ5	GA_11
34	AJ6	GA_12
35	AJ7	GA_20
36	AJ8	GA_23
37	AJ9	GA_27
38	AJ10	GA_30
39	AJ11	GA_34
40	AJ12	GND
41	AJ13	V_{DD33}
42	AJ14	GA_39
43	AJ15	GA_43
44	AJ16	GA_46
45	AJ17	GA_50
46	AJ18	GA_53
47	AJ19	GA_57
48	AJ20	GA_60
49	AJ21	GA_66
50	AJ22	GA_67
51	AJ23	V_{DD33}
52	AJ24	V_{DD33}
53	AH24	GND
54	AG24	GA_76
55	AF24	GA_79
56	AE24	GA_80
57	AD24	TMC1_G
58	AC24	V_{DD33}
59	AB24	P63/A23
60	AA24	P60/A20
61	Y24	A2
62	W24	A6
63	V24	A10
64	U24	A14

Pin no.	Pin ID	Name
65	T24	A18
66	R24	SDRASZ
67	P24	GND
68	N24	V_{DD33}
69	M24	SDCKE
70	L24	BUSCLK
71	K24	BENZ0
72	J24	RDZ
73	H24	CSZ0
74	G24	GND
75	F24	P80/IOWRZ
76	E24	P83/HLDRQZ
77	D24	D0
78	C24	D2
79	B24	GND
80	A24	GND
81	A23	GND
82	A22	V_{DD33}
83	A21	D4
84	A20	D8
85	A19	D11
86	A18	D15
87	A17	GND
88	A16	P125/DMAAKZ1
89	A15	TRCCE
90	A14	DDI
91	A13	TRCCLK
92	A12	V_{DD33}
93	A11	TRCDATA4
94	A10	PLLFO
95	A9	GND
96	A8	V_{DD33}
97	A7	XT2
98	A6	XT1
99	A5	P110/ETCLR0
100	A4	P111/ETCLR1
101	A3	P113/ETO1
102	A2	GND
103	B2	GND
104	C2	V_{DD33}
105	D2	P56/ETCUD0
106	E2	P10/INTPZ8
107	F2	P13/INTPZ11
108	G2	V_{DD33}
109	H2	TMC2_A
110	J2	P43/TI3
111	K2	P47/TCLR3
112	L2	P53/TO3
113	M2	P03/INTPZ3
114	N2	GND
115	P2	P140/SCK0
116	R2	P143/SCK1
117	T2	P15/INTPZ13
118	U2	P17/INTPZ15
119	V2	P34/RXD2
120	W2	V_{DD33}
121	Y2	PPON0
122	AA2	UHD0M
123	AB2	UHD1M
124	AC2	GND
125	AD2	UFDP
126	AE2	TDI_A
127	AF2	TMS_G
128	AG2	GA_3

Pin no.	Pin ID	Name
129	AH2	GND
130	AH3	GA_4
131	AH4	GA_8
132	AH5	GA_13
133	AH6	GA_15
134	AH7	GA_18
135	AH8	GA_22
136	AH9	GA_25
137	AH10	GA_29
138	AH11	GA_33
139	AH12	GND
140	AH13	V_{DD33}
141	AH14	GA_40
142	AH15	GA_44
143	AH16	GA_48
144	AH17	GA_51
145	AH18	GA_55
146	AH19	GA_59
147	AH20	GA_62
148	AH21	GA_63
149	AH22	GA_69
150	AH23	GND
151	AG23	GA_72
152	AF23	GA_75
153	AE23	GA_78
154	AD23	TMC2_G
155	AC23	V_{DD33}
156	AB23	P64/A24
157	AA23	P61/A21
158	Y23	P67/A1
159	W23	A5
160	V23	A9
161	U23	A13
162	T23	A17
163	R23	P70/WAITZ
164	P23	GND
165	N23	V_{DD33}
166	M23	SDWEZ
167	L23	DQM1
168	K23	BENZ1
169	J23	WRSTBZ
170	H23	P71/CSZ1
171	G23	P73/CSZ3
172	F23	P81/IORDZ
173	E23	P84/REFRQZ
174	D23	D1
175	C23	D3
176	B23	GND
177	B22	V_{DD33}
178	B21	D5
179	B20	D7
180	B19	D10
181	B18	D14
182	B17	V_{DD33}
183	B16	P124/DMAAKZ0
184	B15	EVIN
185	B14	DRSTZ
186	B13	TRCDATA1
187	B12	GND
188	B11	TRCDATA5
189	B10	TRCEND
190	B9	GND
191	B8	V_{DD33}
192	B7	TMODE2

Pin no.	Pin ID	Name
193	B6	TMODE1
194	B5	UCLKSEL1
195	B4	P112/ETO0
196	B3	P54/ETIUD0
197	C3	GND
198	D3	GND
199	E3	P11/INTPZ9
200	F3	P146/PWMO0
201	G3	P147/PWMO1
202	H3	P40/TI0
203	J3	P44/TCLR0
204	K3	P50/TO0
205	L3	P00/INTPZ0
206	M3	P05/INTPZ5
207	N3	P07/INTPZ7
208	P3	P142/SO0
209	R3	P144/SI1
210	T3	P31/TXD0
211	U3	P33/TXD1
212	V3	P35/TXD2
213	W3	P37/TXD3
214	Y3	PPON1
215	AA3	MODE1
216	AB3	VBUSDET
217	AC3	OCI1
218	AD3	TRST
219	AE3	TCK
220	AF3	TDO_G
221	AG3	GND
222	AG4	GA_5
223	AG5	GA_9
224	AG6	V_{DD33}
225	AG7	GA_16
226	AG8	GA_19
227	AG9	GA_24
228	AG10	GA_28
229	AG11	GA_32
230	AG12	GA_36
231	AG13	GA_37
232	AG14	GA_41
233	AG15	GA_45
234	AG16	GA_49
235	AG17	GA_54
236	AG18	GA_58
237	AG19	V_{DD33}
238	AG20	GA_64
239	AG21	GA_68
240	AG22	GND
241	AF22	GA_71
242	AE22	GA_74
243	AD22	GA_77
244	AC22	GND
245	AB22	P65/A25
246	AA22	P62/A22
247	Y22	P66/A0
248	W22	A4
249	V22	A8
250	U22	A12
251	T22	A16
252	R22	A19
253	P22	GND
254	N22	GND
255	M22	SDCASZ
256	L22	DQM0

Pin no.	Pin ID	Name
257	K22	V_{DD33}
258	J22	GND
259	H22	P72/CSZ2
260	G22	P74/CSZ4
261	F22	P82/HLDAKZ
262	E22	P85/SELFREFZ
263	D22	GND
264	C22	GND
265	C21	GND
266	C20	D6
267	C19	D9
268	C18	D13
269	C17	P131/DMARQZ1
270	C16	P121/TCZ1
271	C15	IROMEN
272	C14	DMS
273	C13	TRCDATA0
274	C12	TRCDATA2
275	C11	TRCDATA6
276	C10	TESTCLK
277	C9	RMODEZ
278	C8	TMODE3
279	C7	AGND_PLL
280	C6	AV_{DD}_PLL
281	C5	UCLKSEL0
282	C4	GND
283	D4	GND
284	E4	GND
285	F4	V_{DD15}
286	G4	TMC1_A
287	H4	P41/TI1
288	J4	P45/TCLR1
289	K4	P51/TO1
290	L4	P01/INTPZ1
291	M4	P04/INTPZ4
292	N4	V_{DD15}
293	P4	V_{DD15}
294	R4	P14/INTPZ12
295	T4	P30/RXD0
296	U4	P32/RXD1
297	V4	P36/RXD3
298	W4	V_{DD33}
299	Y4	MODE0
300	AA4	OCI0
301	AB4	GND
302	AC4	RESETZ
303	AD4	TDO_A
304	AE4	TDI_G
305	AF4	V_{DD33}
306	AF5	GA_7
307	AF6	V_{DD33}
308	AF7	GA_14
309	AF8	GA_17
310	AF9	GA_21
311	AF10	GA_26
312	AF11	GA_31
313	AF12	GA_35
314	AF13	GA_38
315	AF14	GA_42
316	AF15	GA_47
317	AF16	GA_52
318	AF17	GA_56
319	AF18	GA_61
320	AF19	V_{DD33}

Pin no.	Pin ID	Name
321	AF20	GA_65
322	AF21	GND
323	AE21	GA_70
324	AD21	GA_73
325	AC21	GND
326	AB21	PLLFOEN
327	AA21	GND
328	Y21	GND
329	W21	A3
330	V21	A7
331	U21	A11
332	T21	A15
333	R21	GND
334	P21	GND
335	N21	V_{DD15}
336	M21	V_{DD15}
337	L21	BCYSTZ
338	K21	V_{DD33}
339	J21	GND
340	H21	GND
341	G21	P76/CSZ6
342	F21	V_{DD15}
343	E21	GND
344	D21	GND
345	D20	GND
346	D19	V_{DD15}
347	D18	D12
348	D17	P130/DMARQZ0
349	D16	P120/TCZ0
350	D15	NMI
351	D14	DCK
352	D13	DDO
353	D12	TRCDATA3
354	D11	TRCDATA7
355	D10	VBCLKOUT
356	D9	GND
357	D8	TMODE0
358	D7	AGND_PLL
359	D6	AV_{DD}_PLL
360	D5	V_{DD15}
361	J9	V_{DD15}
362	K9	V_{DD15}
363	L9	GND
364	M9	V_{DD15}
365	N9	V_{DD15}
366	P9	GND
367	R9	V_{DD15}
368	T9	V_{DD15}
369	U9	GND
370	V9	GND
371	W9	V_{DD33}
372	Y9	GND
373	AA9	V_{DD33}
374	AA10	V_{DD33}
375	AA11	GND
376	AA12	GND
377	AA13	GND
378	AA14	GND
379	AA15	V_{DD33}
380	AA16	V_{DD33}
381	Y16	GND
382	W16	V_{DD33}
383	V16	GND
384	U16	GND

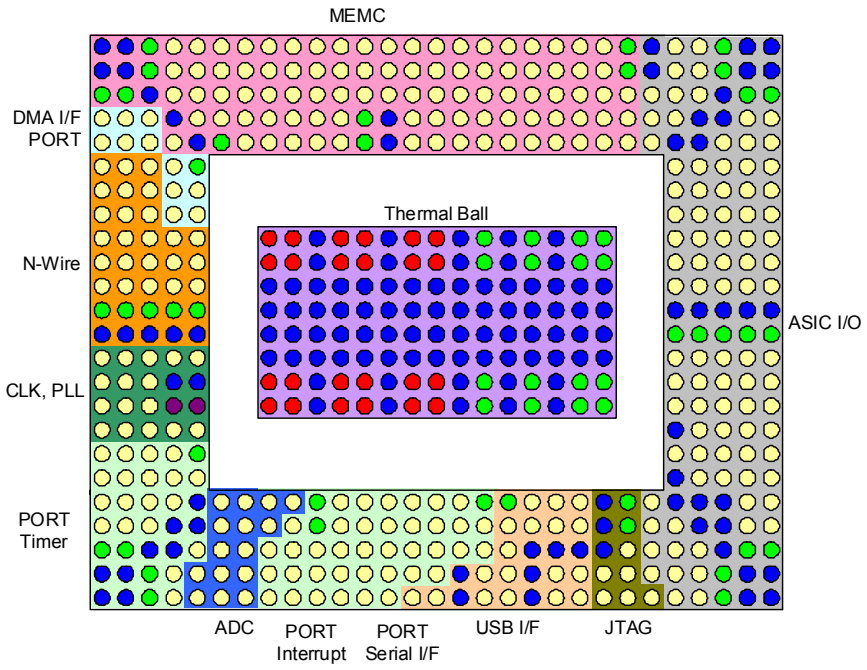
Pin no.	Pin ID	Name
385	T16	V_{DD15}
386	R16	V_{DD15}
387	P16	GND
388	N16	V_{DD15}
389	M16	V_{DD15}
390	L16	GND
391	K16	V_{DD15}
392	J16	V_{DD15}
393	J15	V_{DD15}
394	J14	GND
395	J13	GND
396	J12	GND
397	J11	GND
398	J10	V_{DD15}
399	K10	V_{DD15}
400	L10	GND
401	M10	V_{DD15}
402	N10	V_{DD15}
403	P10	GND
404	R10	V_{DD15}
405	T10	V_{DD15}
406	U10	GND
407	V10	GND
408	W10	V_{DD33}
409	Y10	GND
410	Y11	GND
411	Y12	GND
412	Y13	GND
413	Y14	GND
414	Y15	GND
415	W15	V_{DD33}
416	V15	GND
417	U15	GND
418	T15	V_{DD15}
419	R15	V_{DD15}
420	P15	GND
421	N15	V_{DD15}
422	M15	V_{DD15}
423	L15	GND
424	K15	V_{DD15}
425	K14	GND
426	K13	GND
427	K12	GND
428	K11	GND
429	L11	GND
430	M11	GND
431	N11	GND
432	P11	GND
433	R11	GND
434	T11	GND
435	U11	GND
436	V11	GND
437	W11	GND
438	W12	GND
439	W13	GND
440	W14	GND
441	V14	GND
442	U14	GND
443	T14	GND
444	R14	GND
445	P14	GND
446	N14	GND
447	M14	GND
448	L14	GND

Pin no.	Pin ID	Name
449	L13	GND
450	L12	GND
451	M12	GND
452	N12	GND
453	P12	GND
454	R12	GND
455	T12	GND
456	U12	GND
457	V12	GND
458	V13	GND
459	U13	GND
460	T13	GND
461	R13	GND
462	P13	GND
463	N13	GND
464	M13	GND

11.4.2 550-pin PBGA

(1) V_{DD33}, V_{DD15}, and GND pin placement

Figure 11-5. 550-pin PBGA (V_{DD33}, V_{DD15}, and GND Pin Placement)



●GND	●V_{DD15}	●V_{DD33}	●AV_{DD}_PLL	●Signal
141	24	55	2	328

(2) Pin placement

Figure 11-6. 550-pin PBGA (Pin Placement: Top View)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	
GND	GND	VDD33	P130/DMARQZ0	D11	D8	D2	P85/SELFREFZ	D0	P83/HLDRQZ	RDZ	P72/CSZ2	BENZ1	P104/D28	BUSCLK	BENZ0	P90/D16	BENZ3	SDCASZ	A16	A11	A10	VDD33	GND	GA_80	GA_76	VDD33	GND	GND	24
GND	GND	VDD33	D13	D12	D7	D3	D1	P91/D17	P82/HLDAKZ	P77/CSZ7	P71/CSZ1	P101/D25	P97/D23	P95/D21	P92/D18	BENZ2	SDRASZ	A15	A8	A9	A5	VDD33	GND	GA_79	GA_75	VDD33	GND	GND	23
VDD33	VDD33	GND	D14	D9	D4	P81/IORDZ	P107/D31	P94/D20	P80/IOWRZ	P76/CSZ6	P106/D30	P100/D24	P96/D22	P93/D19	DQM0	A19	A14	A12	A6	A3	P67/A1	P61/A21	TMC1_G	GA_78	GA_74	GND	VDD33	VDD33	22
P121/TCZ1	P120/TCZ0	P131/DMARQZ1	GND	D10	D5	P84/REFRQZ	WRSTBZ	P102/D26	P75/CSZ5	CSZ0	VDD33	GND	BCYSTZ	DQM1	A18	DQM2	P70/WAITZ	A7	A2	P60/A20	P62/A22	P64/A24	TMC2_G	GA_77	GND	GND	GA_73	GA_67	21
P126/DMAAKZ2	P124/DMAAKZ0	P123/TCZ3	D15	GND	VDD33	D6	P74/CSZ4	P103/D27	P73/CSZ3	P105/D29	VDD33	GND	DQM3	A17	SDCKE	SDWEZ	A13	A4	P66/A0	P65/A25	P63/A23	PLLFOEN	VDD33	GND	GND	GA_72	GA_71	GA_66	20
P153/INTPZ27	P152/INTPZ26	P150/INTPZ24	P132/DMARQZ2	VDD33																				GA_70	GA_69	GA_68	GA_64	GA_65	19
EVIN	IROMEN	NMI	P122/TCZ2	P133/DMARQZ3																				VDD33	VDD33	GA_61	GA_62	GA_63	18
DDI	DMS	TRCCE	P127/DMAAKZ3	P125/DMAAKZ1																				GA_60	GA_56	GA_57	GA_58	GA_59	17
TRCDATA1	TRCCLK	DDO	DCK	P151/INTPZ25			VDD15	VDD15	GND	VDD15	VDD15	GND	VDD15	VDD15	GND	VDD33	GND	VDD33	GND	VDD33	VDD33			GA_55	GA_51	GA_52	GA_53	GA_54	16
TRCDATA6	TRCDATA4	TRCDATA3	DRSTZ	TRCDATA0			VDD15	VDD15	GND	VDD15	VDD15	GND	VDD15	VDD15	GND	VDD33	GND	VDD33	GND	VDD33	VDD33			GA_50	GA_46	GA_47	GA_48	GA_49	15
P114/EVTTRG	TRCEND	TRCDATA7	TRCDATA5	TRCDATA2			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GA_45	GA_41	GA_42	GA_43	GA_44	14
VDD33	VDD33	VDD33	VDD33	VDD33			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND	GND	GND	GND	GND	13
GND	GND	GND	GND	GND			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			VDD33	VDD33	VDD33	VDD33	VDD33	12
VBCLKOUT	PLLFO	TMODE3	TESTCLK	RMODEZ			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GA_36	GA_37	GA_38	GA_39	GA_40	11
XT1	P115/DBINT	TMODE2	AGND_PLL	AGND_PLL			VDD15	VDD15	GND	VDD15	VDD15	GND	VDD15	VDD15	GND	VDD33	GND	VDD33	GND	VDD33	VDD33			GA_31	GA_32	GA_33	GA_34	GA_35	10
XT2	TMODE1	TMODE0	AVDD_PLL	AVDD_PLL			VDD15	VDD15	GND	VDD15	VDD15	GND	VDD15	VDD15	GND	VDD33	GND	VDD33	GND	VDD33	VDD33			GA_26	GA_27	GA_28	GA_29	GA_30	9
UCLKSEL1	UCLKSEL0	P110/ETCLR0	P55/ETIUD1	P112/ETO0																				GND	GA_22	GA_23	GA_24	GA_25	8
P111/ETCLR1	P113/ETO1	P54/ETIUD0	P10/INTPZ8	VDD33																				VDD33	VDD33	GA_19	GA_20	GA_21	7
P56/ETCUD0	P57/ETCUD1	P12/INTPZ10	P11/INTPZ9	P146/PWMO0																				GND	GA_15	GA_16	GA_17	GA_18	6
P13/INTPZ11	VBRESTOZ	P147/PWMO1	P155/INTPZ29	GND	AVDD_AD	AGND_AD	AVREFM	AGND_AD	VDD33	P53/TO3	P141/SI0	P17/INTPZ15	P34/RXD2	P37/TXD3	P35/TXD2	VDD33	VDD33	VBUSDET	TMS_A	RESETZ	GND	VDD33	VDD33	GND	GND	GND	GA_14	GA_12	5
P154/INTPZ28	P156/INTPZ30	P157/INTPZ31	GND	GND	AVDD_AD	AVREFP	AGND_AD	P44/TCLR0	VDD33	P04/INTPZ4	P145/SO1	P142/SO0	P15/INTPZ13	P36/RXD3	P30/RXD0	P32/RXD1	MODE1	PPON1	PPON0	TDO_A	GND	VDD33	GA_3	GA_7	GND	GND	GA_13	GA_11	4
VDD33	VDD33	GND	GND	P116/ADTRG	AIN0	AIN2	P40/TI0	P42/TI2	P47/TCLR3	P01/INTPZ1	P05/INTPZ5	P140/SCK0	P144/SI1	P16/INTPZ14	P31/TXD0	P33/TXD1	MODE0	GND	GND	GND	GND	TDO_G	GA_2	GA_6	GA_10	GND	VDD33	VDD33	3
GND	GND	VDD33	TMC1_A	AIN1	AIN5	AIN4	P41/TI1	P45/TCLR1	P50/TO0	P00/INTPZ0	P03/INTPZ3	P07/INTPZ7	P143/SCK1	P14/INTPZ12	GND	UHD0M	UHD1M	GND	UFDP	OCI1	TRST	TMS_G	GA_1	GA_5	GA_9	VDD33	GND	GND	2
GND	GND	VDD33	TMC2_A	AIN3	AIN6	AIN7	P43/TI3	P46/TCLR2	P51/TO1	P52/TO2	P02/INTPZ2	P06/INTPZ6	UCLK	PCLKIN	GND	UHD0P	UHD1P	GND	UFDM	OCI0	TDI_A	TCK	TDI_G	GA_4	GA_8	VDD33	GND	GND	1

Pin no.	Pin ID	Name
1	A1	GND
2	B1	GND
3	C1	V_{DD33}
4	D1	TMC2_A
5	E1	AIN3
6	F1	AIN6
7	G1	AIN7
8	H1	P43/TI3
9	J1	P46/TCLR2
10	K1	P51/TO1
11	L1	P52/TO2
12	M1	P02/INTPZ2
13	N1	P06/INTPZ6
14	P1	UCLK
15	R1	PCLKIN
16	T1	GND
17	U1	UHD0P
18	V1	UHD1P
19	W1	GND
20	Y1	UFDM
21	AA1	OCI0
22	AB1	TDI_A
23	AC1	TCK
24	AD1	TDI_G
25	AE1	GA_4
26	AF1	GA_5
27	AG1	V_{DD33}
28	AH1	GND
29	AJ1	GND
30	AJ2	GND
31	AJ3	V_{DD33}
32	AJ4	GA_11
33	AJ5	GA_12
34	AJ6	GA_18
35	AJ7	GA_21
36	AJ8	GA_25
37	AJ9	GA_30
38	AJ10	GA_35
39	AJ11	GA_40
40	AJ12	V_{DD33}
41	AJ13	GND
42	AJ14	GA_44
43	AJ15	GA_49
44	AJ16	GA_54
45	AJ17	GA_59
46	AJ18	GA_63
47	AJ19	GA_65
48	AJ20	GA_66
49	AJ21	GA_67
50	AJ22	V_{DD33}
51	AJ23	GND
52	AJ24	GND
53	AH24	GND
54	AG24	V_{DD33}
55	AF24	GA_76
56	AE24	GA_80
57	AD24	GND
58	AC24	V_{DD33}
59	AB24	A10
60	AA24	A11
61	Y24	A16
62	W24	SDCASZ
63	V24	BENZ3
64	U24	P90/D16

Pin no.	Pin ID	Name
65	T24	BENZ0
66	R24	BUSCLK
67	P24	P104/D28
68	N24	BENZ1
69	M24	P72/CSZ2
70	L24	RDZ
71	K24	P83/HLDRQZ
72	J24	D0
73	H24	P85/SELFREFZ
74	G24	D2
75	F24	D8
76	E24	D11
77	D24	P130/DMARQZ0
78	C24	V_{DD33}
79	B24	GND
80	A24	GND
81	A23	GND
82	A22	V_{DD33}
83	A21	P121/TCZ1
84	A20	P126/DMAAKZ2
85	A19	P153/INTPZ27
86	A18	EVIN
87	A17	DDI
88	A16	TRCDATA1
89	A15	TRCDATA6
90	A14	P114/EVTTRG
91	A13	V_{DD33}
92	A12	GND
93	A11	VBCLKOUT
94	A10	XT1
95	A9	XT2
96	A8	UCLKSEL1
97	A7	P111/ETCLR1
98	A6	P56/ETCUD0
99	A5	P13/INTPZ11
100	A4	P154/INTPZ28
101	A3	V_{DD33}
102	A2	GND
103	B2	GND
104	C2	V_{DD33}
105	D2	TMC1_A
106	E2	AIN1
107	F2	AIN5
108	G2	AIN4
109	H2	P41/TI1
110	J2	P45/TCLR1
111	K2	P50/TO0
112	L2	P00/INTPZ0
113	M2	P03/INTPZ3
114	N2	P07/INTPZ7
115	P2	P143/SCK1
116	R2	P14/INTPZ12
117	T2	GND
118	U2	UHD0M
119	V2	UHD1M
120	W2	GND
121	Y2	UFDP
122	AA2	OCI1
123	AB2	TRST
124	AC2	TMS_G
125	AD2	GA_1
126	AE2	GA_5
127	AF2	GA_9
128	AG2	V_{DD33}

Pin no.	Pin ID	Name
129	AH2	GND
130	AH3	V_{DD33}
131	AH4	GA_13
132	AH5	GA_14
133	AH6	GA_17
134	AH7	GA_20
135	AH8	GA_24
136	AH9	GA_29
137	AH10	GA_34
138	AH11	GA_39
139	AH12	V_{DD33}
140	AH13	GND
141	AH14	GA_43
142	AH15	GA_48
143	AH16	GA_53
144	AH17	GA_58
145	AH18	GA_62
146	AH19	GA_64
147	AH20	GA_71
148	AH21	GA_73
149	AH22	V_{DD33}
150	AH23	GND
151	AG23	V_{DD33}
152	AF23	GA_75
153	AE23	GA_79
154	AD23	GND
155	AC23	V_{DD33}
156	AB23	A5
157	AA23	A9
158	Y23	A8
159	W23	A15
160	V23	SDRASZ
161	U23	BENZ2
162	T23	P92/D18
163	R23	P95/D21
164	P23	P97/D23
165	N23	P101/D25
166	M23	P71/CSZ1
167	L23	P77/CSZ7
168	K23	P82/HLDAKZ
169	J23	P91/D17
170	H23	D1
171	G23	D3
172	F23	D7
173	E23	D12
174	D23	D13
175	C23	V_{DD33}
176	B23	GND
177	B22	V_{DD33}
178	B21	P120/TCZ0
179	B20	P124/DMAAKZ0
180	B19	P152/INTPZ26
181	B18	IROMEN
182	B17	DMS
183	B16	TRCCLK
184	B15	TRCDATA4
185	B14	TRCEND
186	B13	V_{DD33}
187	B12	GND
188	B11	PLLFO
189	B10	P115/DBINT
190	B9	TMODE1
191	B8	UCLKSEL0
192	B7	P113/ETO1

Pin no.	Pin ID	Name
193	B6	P57/ETCUD1
194	B5	VBRESTOZ
195	B4	P156/INTPZ30
196	B3	V_{DD33}
197	C3	GND
198	D3	GND
199	E3	P116/ADTRG
200	F3	AIN0
201	G3	AIN2
202	H3	P40/TI0
203	J3	P42/TI2
204	K3	P47/TCLR3
205	L3	P01/INTPZ1
206	M3	P05/INTPZ5
207	N3	P140/SCK0
208	P3	P144/SI1
209	R3	P16/INTPZ14
210	T3	P31/TXD0
211	U3	P33/TXD1
212	V3	MODE0
213	W3	GND
214	Y3	GND
215	AA3	GND
216	AB3	GND
217	AC3	TDO_G
218	AD3	GA_2
219	AE3	GA_6
220	AF3	GA_10
221	AG3	GND
222	AG4	GND
223	AG5	GND
224	AG6	GA_16
225	AG7	GA_19
226	AG8	GA_23
227	AG9	GA_28
228	AG10	GA_33
229	AG11	GA_38
230	AG12	V_{DD33}
231	AG13	GND
232	AG14	GA_42
233	AG15	GA_47
234	AG16	GA_52
235	AG17	GA_57
236	AG18	GA_61
237	AG19	GA_68
238	AG20	GA_72
239	AG21	GND
240	AG22	GND
241	AF22	GA_74
242	AE22	GA_78
243	AD22	TMC1_G
244	AC22	P61/A21
245	AB22	P67/A1
246	AA22	A3
247	Y22	A6
248	W22	A12
249	V22	A14
250	U22	A19
251	T22	DQM0
252	R22	P93/D19
253	P22	P96/D22
254	N22	P100/D24
255	M22	P106/D30
256	L22	P76/CSZ6

Pin no.	Pin ID	Name
257	K22	P80/IOWRZ
258	J22	P94/D20
259	H22	P107/D31
260	G22	P81/IORDZ
261	F22	D4
262	E22	D9
263	D22	D14
264	C22	GND
265	C21	P131/DMARQZ1
266	C20	P123/TCZ3
267	C19	P150/INTPZ24
268	C18	NMI
269	C17	TRCCE
270	C16	DDO
271	C15	TRCDATA3
272	C14	TRCDATA7
273	C13	V_{DD33}
274	C12	GND
275	C11	TMODE3
276	C10	TMODE2
277	C9	TMODE0
278	C8	P110/ETCLR0
279	C7	P54/ETIUD0
280	C6	P12/INTPZ10
281	C5	P147/PWMO1
282	C4	P157/INTPZ31
283	D4	GND
284	E4	GND
285	F4	AV_{DD}_AD
286	G4	AVREFP
287	H4	AGND_AD
288	J4	P44/TCLR0
289	K4	V_{DD33}
290	L4	P04/INTPZ4
291	M4	P145/SO1
292	N4	P142/SO0
293	P4	P15/INTPZ13
294	R4	P36/RXD3
295	T4	P30/RXD0
296	U4	P32/RXD1
297	V4	MODE1
298	W4	PPON1
299	Y4	PPON0
300	AA4	TDO_A
301	AB4	GND
302	AC4	V_{DD33}
303	AD4	GA_3
304	AE4	GA_7
305	AF4	GND
306	AF5	GND
307	AF6	GA_15
308	AF7	V_{DD33}
309	AF8	GA_22
310	AF9	GA_27
311	AF10	GA_32
312	AF11	GA_37
313	AF12	V_{DD33}
314	AF13	GND
315	AF14	GA_41
316	AF15	GA_46
317	AF16	GA_51
318	AF17	GA_56
319	AF18	V_{DD33}
320	AF19	GA_69

Pin no.	Pin ID	Name
321	AF20	GND
322	AF21	GND
323	AE21	GA_77
324	AD21	TMC2_G
325	AC21	P64/A24
326	AB21	P62/A22
327	AA21	P60/A20
328	Y21	A2
329	W21	A7
330	V21	P70/WAITZ
331	U21	DQM2
332	T21	A18
333	R21	DQM1
334	P21	BCYSTZ
335	N21	GND
336	M21	V_{DD33}
337	L21	CSZ0
338	K21	P75/CSZ5
339	J21	P102/D26
340	H21	WRSTBZ
341	G21	P84/REFRQZ
342	F21	D5
343	E21	D10
344	D21	GND
345	D20	D15
346	D19	P132/DMARQZ2
347	D18	P122/TCZ2
348	D17	P127/DMAAKZ3
349	D16	DCK
350	D15	DRSTZ
351	D14	TRCDATA5
352	D13	V_{DD33}
353	D12	GND
354	D11	TESTCLK
355	D10	AGND_PLL
356	D9	AV_{DD}_PLL
357	D8	P55/ETIUD1
358	D7	P10/INTPZ8
359	D6	P11/INTPZ9
360	D5	P155/INTPZ29
361	E5	GND
362	F5	AV_{DD}_AD
363	G5	AGND_AD
364	H5	AVREFM
365	J5	AGND_AD
366	K5	V_{DD33}
367	L5	P53/TO3
368	M5	P141/SI0
369	N5	P17/INTPZ15
370	P5	P34/RXD2
371	R5	P37/TXD3
372	T5	P35/TXD2
373	U5	V_{DD33}
374	V5	V_{DD33}
375	W5	VBUSDET
376	Y5	TMS_A
377	AA5	RESETZ
378	AB5	GND
379	AC5	V_{DD33}
380	AD5	V_{DD33}
381	AE5	GND
382	AE6	GND
383	AE7	V_{DD33}
384	AE8	GND

Pin no.	Pin ID	Name
385	AE9	GA_26
386	AE10	GA_31
387	AE11	GA_36
388	AE12	V_{DD33}
389	AE13	GND
390	AE14	GA_45
391	AE15	GA_50
392	AE16	GA_55
393	AE17	GA_60
394	AE18	V_{DD33}
395	AE19	GA_70
396	AE20	GND
397	AD20	V_{DD33}
398	AC20	PLLFOEN
399	AB20	P63/A23
400	AA20	P65/A25
401	Y20	P66/A0
402	W20	A4
403	V20	A13
404	U20	SDWEZ
405	T20	SDCKE
406	R20	A17
407	P20	DQM3
408	N20	GND
409	M20	V_{DD33}
410	L20	P105/D29
411	K20	P73/CSZ3
412	J20	P103/D27
413	H20	P74/CSZ4
414	G20	D6
415	F20	V_{DD33}
416	E20	GND
417	E19	V_{DD33}
418	E18	P133/DMARQZ3
419	E17	P125/DMAAKZ1
420	E16	P151/INTPZ25
421	E15	TRCDATA0
422	E14	TRCDATA2
423	E13	V_{DD33}
424	E12	GND
425	E11	RMODEZ
426	E10	AGND_PLL
427	E9	AV_{DD}_PLL
428	E8	P112/ETO0
429	E7	V_{DD33}
430	E6	P146/PWMO0
431	AB9	V_{DD33}
432	AB10	V_{DD33}
433	AB11	GND
434	AB12	GND
435	AB13	GND
436	AB14	GND
437	AB15	V_{DD33}
438	AB16	V_{DD33}
439	H16	V_{DD15}
440	H15	V_{DD15}
441	H14	GND
442	H13	GND
443	H12	GND
444	H11	GND
445	H10	V_{DD15}
446	H9	V_{DD15}
447	J9	V_{DD15}
448	K9	GND

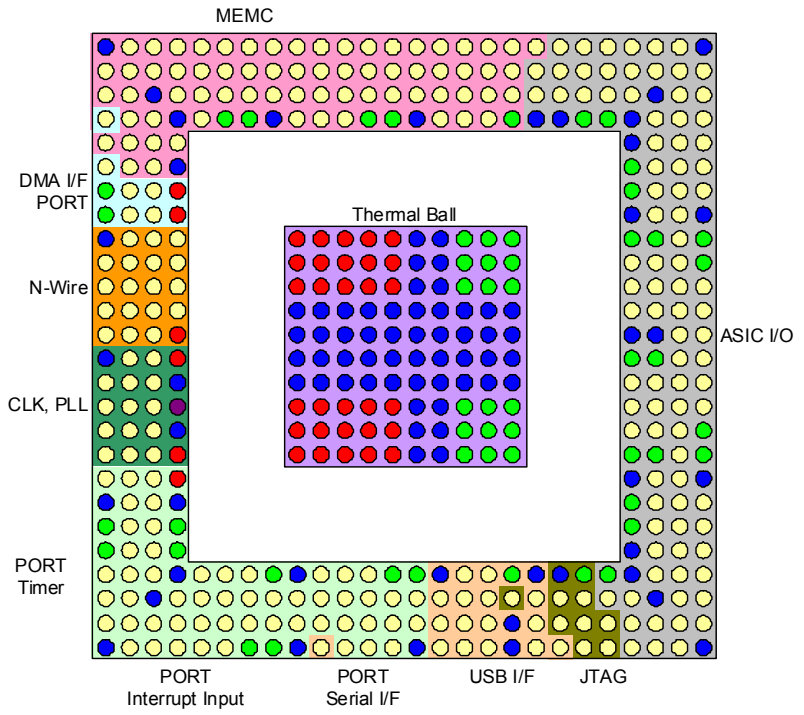
Pin no.	Pin ID	Name
449	L9	V_{DD15}
450	M9	V_{DD15}
451	N9	GND
452	P9	V_{DD15}
453	R9	V_{DD15}
454	T9	GND
455	U9	V_{DD33}
456	V9	GND
457	W9	V_{DD33}
458	Y9	GND
459	AA9	V_{DD33}
460	AA10	V_{DD33}
461	AA11	GND
462	AA12	GND
463	AA13	GND
464	AA14	GND
465	AA15	V_{DD33}
466	AA16	V_{DD33}
467	Y16	GND
468	W16	V_{DD33}
469	V16	GND
470	U16	V_{DD33}
471	T16	GND
472	R16	V_{DD15}
473	P16	V_{DD15}
474	N16	GND
475	M16	V_{DD15}
476	L16	V_{DD15}
477	K16	GND
478	J16	V_{DD15}
479	J15	V_{DD15}
480	J14	GND
481	J13	GND
482	J12	GND
483	J11	GND
484	J10	V_{DD15}
485	K10	GND
486	L10	V_{DD15}
487	M10	V_{DD15}
488	N10	GND
489	P10	V_{DD15}
490	R10	V_{DD15}
491	T10	GND
492	U10	V_{DD33}
493	V10	GND
494	W10	V_{DD33}
495	Y10	GND
496	Y11	GND
497	Y12	GND
498	Y13	GND
499	Y14	GND
500	Y15	GND
501	W15	V_{DD33}
502	V15	GND
503	U15	V_{DD33}
504	T15	GND
505	R15	V_{DD15}
506	P15	V_{DD15}
507	N15	GND
508	M15	V_{DD15}
509	L15	V_{DD15}
510	K15	GND
511	K14	GND
512	K13	GND

Pin no.	Pin ID	Name
513	K12	GND
514	K11	GND
515	L11	GND
516	M11	GND
517	N11	GND
518	P11	GND
519	R11	GND
520	T11	GND
521	U11	GND
522	V11	GND
523	W11	GND
524	W12	GND
525	W13	GND
526	W14	GND
527	V14	GND
528	U14	GND
529	T14	GND
530	R14	GND
531	P14	GND
532	N14	GND
533	M14	GND
534	L14	GND
535	L13	GND
536	L12	GND
537	M12	GND
538	N12	GND
539	P12	GND
540	R12	GND
541	T12	GND
542	U12	GND
543	V12	GND
544	V13	GND
545	U13	GND
546	T13	GND
547	R13	GND
548	P13	GND
549	N13	GND
550	M13	GND

11.4.3 452-pin FPBGA

(1) V_{DD33}, V_{DD15}, and GND pin placement

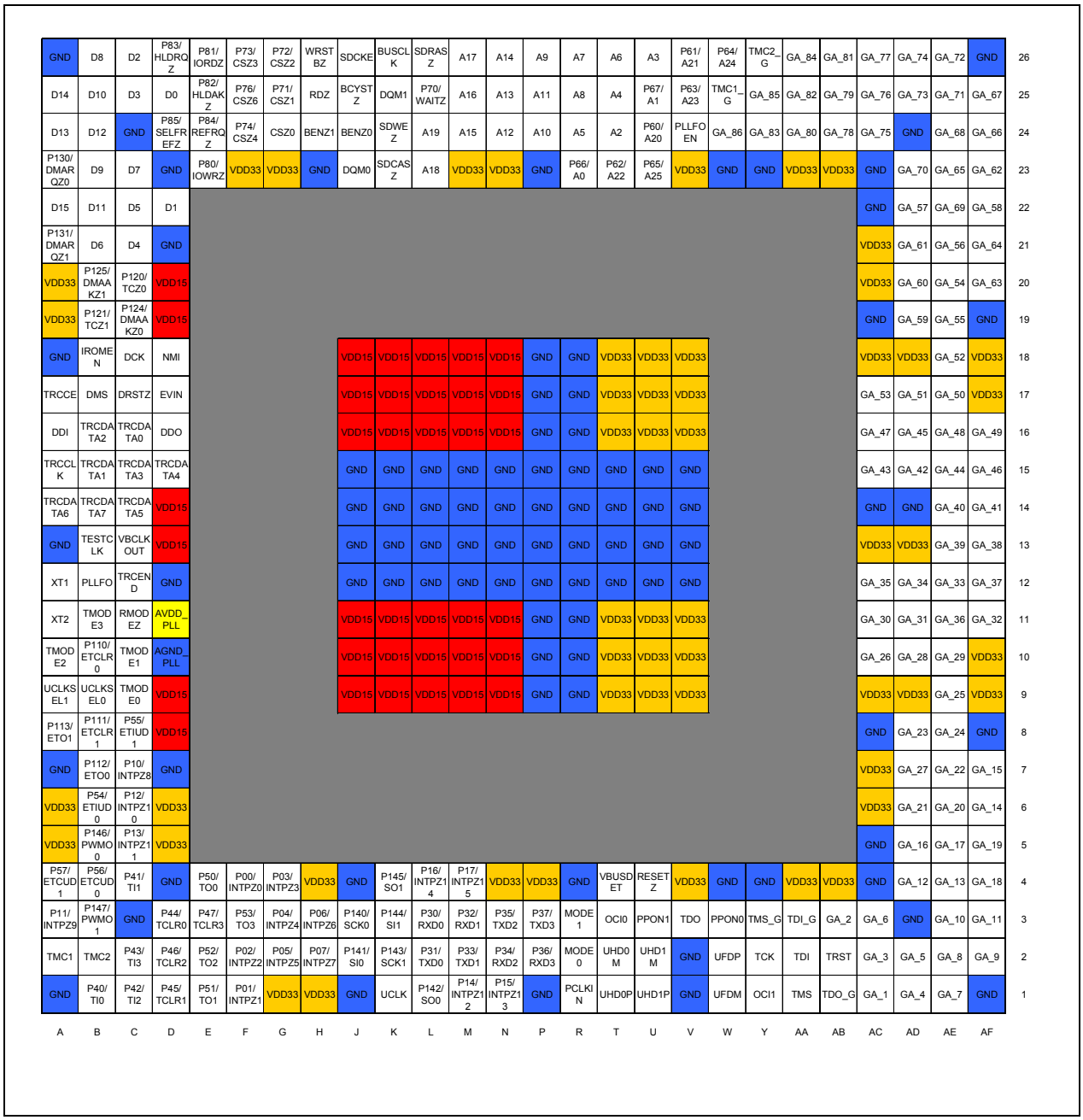
Figure 11-7. 452-pin FPBGA (V_{DD33}, V_{DD15}, and GND Pin Placement)



●GND	●V_{DD15}	●V_{DD33}	●AV_{DD}_PLL	●Signal
91	36	53	1	271

(2) Pin placement

Figure 11-8. 452-pin FPBGA (Pin Placement: Top View)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
26	GND	D8	D2	P83/ HLDRQ Z	P81/ IORDZ	P73/ CSZ3	P72/ CSZ2	WRST BZ	SDCKE	BUSCL K	SDRAS Z	A17	A14	A9	A7	A6	A3	P61/ A21	P64/ A24	TMC2_ G	GA_84	GA_81	GA_77	GA_74	GA_72	GND	26
25	D14	D10	D3	D0	P82/ HLDAK Z	P76/ CSZ6	P71/ CSZ1	RDZ	BCYST Z	DQM1	P70/ WAITZ	A16	A13	A11	A8	A4	P67/ A1	P63/ A23	TMC1_ G	GA_85	GA_82	GA_79	GA_76	GA_73	GA_71	GA_67	25
24	D13	D12	GND	P85/ SELFR EFZ	P84/ REFRQ Z	P74/ CSZ4	CSZ0	BENZ1	BENZ0	SDWE Z	A19	A15	A12	A10	A5	A2	P60/ A20	PLLFO EN	GA_86	GA_83	GA_80	GA_78	GA_75	GND	GA_68	GA_66	24
23	P130/ DMAR QZ0	D9	D7	GND	P80/ IOWRZ	VDD33	VDD33	GND	DQM0	SDCAS Z	A18	VDD33	VDD33	GND	P66/ A0	P62/ A22	P65/ A25	VDD33	GND	GND	VDD33	VDD33	GND	GA_70	GA_65	GA_62	23
22	D15	D11	D5	D1																			GND	GA_57	GA_69	GA_58	22
21	P131/ DMAR QZ1	D6	D4	GND																			VDD33	GA_61	GA_56	GA_64	21
20	VDD33	P125/ DMAA KZ1	P120/ TCZ0	VDD15																			VDD33	GA_60	GA_54	GA_63	20
19	VDD33	P121/ TCZ1	P124/ DMAA KZ0	VDD15																			GND	GA_59	GA_55	GND	19
18	GND	IROME N	DCK	NMI					VDD15	VDD15	VDD15	VDD15	VDD15	GND	GND	VDD33	VDD33	VDD33					VDD33	VDD33	GA_52	VDD33	18
17	TRCCE	DMS	DRSTZ	EVIN					VDD15	VDD15	VDD15	VDD15	VDD15	GND	GND	VDD33	VDD33	VDD33					GA_53	GA_51	GA_50	VDD33	17
16	DDI	TRCDA TA2	TRCDA TA0	DDO					VDD15	VDD15	VDD15	VDD15	VDD15	GND	GND	VDD33	VDD33	VDD33					GA_47	GA_45	GA_48	GA_49	16
15	TRCCL K	TRCDA TA1	TRCDA TA3	TRCDA TA4					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GA_43	GA_42	GA_44	GA_46	15
14	TRCDA TA6	TRCDA TA7	TRCDA TA5	VDD15					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	GND	GA_40	GA_41	14
13	GND	TESTC LK	VBCLK OUT	VDD15					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					VDD33	VDD33	GA_39	GA_38	13
12	XT1	PLLFO	TRCEN D	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GA_35	GA_34	GA_33	GA_37	12
11	XT2	TMOD E3	RMOD EZ	AVDD_ PLL					VDD15	VDD15	VDD15	VDD15	VDD15	GND	GND	VDD33	VDD33	VDD33					GA_30	GA_31	GA_36	GA_32	11
10	TMOD E2	P110/ ETCLR 0	TMOD E1	AGND_ PLL					VDD15	VDD15	VDD15	VDD15	VDD15	GND	GND	VDD33	VDD33	VDD33					GA_26	GA_28	GA_29	VDD33	10
9	UCLKS EL1	UCLKS EL0	TMOD E0	VDD15					VDD15	VDD15	VDD15	VDD15	VDD15	GND	GND	VDD33	VDD33	VDD33					VDD33	VDD33	GA_25	VDD33	9
8	P113/ ETO1	P111/ ETCLR 1	P55/ ETIUD 1	VDD15																			GND	GA_23	GA_24	GND	8
7	GND	P112/ ETO0	P10/ INTPZ8	GND																			VDD33	GA_27	GA_22	GA_15	7
6	VDD33	P54/ ETIUD 0	P12/ INTPZ1 0	VDD33																			VDD33	GA_21	GA_20	GA_14	6
5	VDD33	P146/ PWMO 0	P13/ INTPZ1 1	VDD33																			GND	GA_16	GA_17	GA_19	5
4	P57/ ETCUD 1	P56/ ETCUD 0	P41/ TI1	GND	P50/ TO0	P00/ INTPZ0	P03/ INTPZ3	VDD33	GND	P145/ SO1	P16/ INTPZ1 4	P17/ INTPZ1 5	VDD33	VDD33	GND	VBUSD ET	RESET Z	VDD33	GND	GND	VDD33	VDD33	GND	GA_12	GA_13	GA_18	4
3	P11/ INTPZ9	P147/ PWMO 1	GND	P44/ TCLR0	P47/ TCLR3	P53/ TO3	P04/ INTPZ4	P06/ INTPZ6	P140/ SCK0	P144/ SI1	P30/ RXD0	P32/ RXD1	P35/ TXD2	P37/ TXD3	MODE 1	OCI0	PPON1	TDO	PPON0	TMS_G	TDI_G	GA_2	GA_6	GND	GA_10	GA_11	3
2	TMC1	TMC2	P43/ TI3	P46/ TCLR2	P52/ TO2	P02/ INTPZ2	P05/ INTPZ5	P07/ INTPZ7	P141/ SI0	P143/ SCK1	P31/ TXD0	P33/ TXD1	P34/ RXD2	P36/ RXD3	MODE 0	UHD0 M	UHD1 M	GND	UFDP	TCK	TDI	TRST	GA_3	GA_5	GA_8	GA_9	2
1	GND	P40/ TI0	P42/ TI2	P45/ TCLR1	P51/ TO1	P01/ INTPZ1	VDD33	VDD33	GND	UCLK	P142/ SO0	P14/ INTPZ1 2	P15/ INTPZ1 3	GND	PCLKI N	UHD0P	UHD1P	GND	UFDM	OCI1	TMS	TDO_G	GA_1	GA_4	GA_7	GND	1

Pin no.	Pin ID	Name
1	A1	GND
2	B1	P40/TI0
3	C1	P42/TI2
4	D1	P45/TCLR1
5	E1	P51/TO1
6	F1	P01/INTPZ1
7	G1	V_{DD33}
8	H1	V_{DD33}
9	J1	GND
10	K1	UCLK
11	L1	P142/SO0
12	M1	P14/INTPZ12
13	N1	P15/INTPZ13
14	P1	GND
15	R1	PCLKIN
16	T1	UHD0P
17	U1	UHD1P
18	V1	GND
19	W1	UFDM
20	Y1	OCI1
21	AA1	TMS
22	AB1	TDO_G
23	AC1	GA_1
24	AD1	GA_4
25	AE1	GA_7
26	AF1	GND
27	AF2	GA_9
28	AF3	GA_11
29	AF4	GA_18
30	AF5	GA_19
31	AF6	GA_14
32	AF7	GA_15
33	AF8	GND
34	AF9	V_{DD33}
35	AF10	V_{DD33}
36	AF11	GA_32
37	AF12	GA_37
38	AF13	GA_38
39	AF14	GA_41
40	AF15	GA_46
41	AF16	GA_49
42	AF17	V_{DD33}
43	AF18	V_{DD33}
44	AF19	GND
45	AF20	GA_63
46	AF21	GA_64
47	AF22	GA_58
48	AF23	GA_62
49	AF24	GA_66
50	AF25	GA_67
51	AF26	GND
52	AE26	GA_72
53	AD26	GA_74
54	AC26	GA_77
55	AB26	GA_81
56	AA26	GA_84
57	Y26	TMC2_G
58	W26	P64/A24
59	V26	P61/A21
60	U26	A3
61	T26	A6
62	R26	A7
63	P26	A9
64	N26	A14

Pin no.	Pin ID	Name
65	M26	A17
66	L26	SDRASZ
67	K26	BUSCLK
68	J26	SDCKE
69	H26	WRSTBZ
70	G26	P72/CSZ2
71	F26	P73/CSZ3
72	E26	P81/IORDZ
73	D26	P83/HLDRQZ
74	C26	D2
75	B26	D8
76	A26	GND
77	A25	D14
78	A24	D13
79	A23	P130/DMARQZ0
80	A22	D15
81	A21	P131/DMARQZ1
82	A20	V_{DD33}
83	A19	V_{DD33}
84	A18	GND
85	A17	TRCCE
86	A16	DDI
87	A15	TRCCLK
88	A14	TRCDATA6
89	A13	GND
90	A12	XT1
91	A11	XT2
92	A10	TMODE2
93	A9	UCLKSEL1
94	A8	P113/ETO1
95	A7	GND
96	A6	V_{DD33}
97	A5	V_{DD33}
98	A4	P57/ETCUD1
99	A3	P11/INTPZ9
100	A2	TMC1
101	B2	TMC2
102	C2	P43/TI3
103	D2	P46/TCLR2
104	E2	P52/TO2
105	F2	P02/INTPZ2
106	G2	P05/INTPZ5
107	H2	P07/INTPZ7
108	J2	P141/SI0
109	K2	P143/SCK1
110	L2	P31/TXD0
111	M2	P33/TXD1
112	N2	P34/RXD2
113	P2	P36/RXD3
114	R2	MODE0
115	T2	UHD0M
116	U2	UHD1M
117	V2	GND
118	W2	UFDP
119	Y2	TCK
120	AA2	TDI
121	AB2	TRST
122	AC2	GA_3
123	AD2	GA_5
124	AE2	GA_8
125	AE3	GA_10
126	AE4	GA_13
127	AE5	GA_17
128	AE6	GA_20

Pin no.	Pin ID	Name
129	AE7	GA_22
130	AE8	GA_24
131	AE9	GA_25
132	AE10	GA_29
133	AE11	GA_36
134	AE12	GA_33
135	AE13	GA_39
136	AE14	GA_40
137	AE15	GA_44
138	AE16	GA_48
139	AE17	GA_50
140	AE18	GA_52
141	AE19	GA_55
142	AE20	GA_54
143	AE21	GA_56
144	AE22	GA_69
145	AE23	GA_65
146	AE24	GA_68
147	AE25	GA_71
148	AD25	GA_73
149	AC25	GA_76
150	AB25	GA_79
151	AA25	GA_82
152	Y25	GA_85
153	W25	TMC1_G
154	V25	P63/A23
155	U25	P67/A1
156	T25	A4
157	R25	A8
158	P25	A11
159	N25	A13
160	M25	A16
161	L25	P70/WAITZ
162	K25	DQM1
163	J25	BCYSTZ
164	H25	RDZ
165	G25	P71/CSZ1
166	F25	P76/CSZ6
167	E25	P82/HLDAKZ
168	D25	D0
169	C25	D3
170	B25	D10
171	B24	D12
172	B23	D9
173	B22	D11
174	B21	D6
175	B20	P125/DMAAKZ1
176	B19	P121/TCZ1
177	B18	IROMEN
178	B17	DMS
179	B16	TRCDATA2
180	B15	TRCDATA1
181	B14	TRCDATA7
182	B13	TESTCLK
183	B12	PLLFO
184	B11	TMODE3
185	B10	P110/ETCLR0
186	B9	UCLKSEL0
187	B8	P111/ETCLR1
188	B7	P112/ETO0
189	B6	P54/ETIUD0
190	B5	P146/PWMO0
191	B4	P56/ETCUD0
192	B3	P147/PWMO1

Pin no.	Pin ID	Name
257	C23	D7
258	C22	D5
259	C21	D4
260	C20	P120/TCZ0
261	C19	P124/DMAAKZ0
262	C18	DCK
263	C17	DRSTZ
264	C16	TRCDATA0
265	C15	TRCDATA3
266	C14	TRCDATA5
267	C13	VBCLKOUT
268	C12	TRCEND
269	C11	RMODEZ
270	C10	TMODE1
271	C9	TMODE0
272	C8	P55/ETIUD1
273	C7	P10/INTPZ8
274	C6	P12/INTPZ10
275	C5	P13/INTPZ11
276	C4	P41/TI1
277	D4	GND
278	E4	P50/TO0
279	F4	P00/INTPZ0
280	G4	P03/INTPZ3
281	H4	V_{DD33}
282	J4	GND
283	K4	P145/SO1
284	L4	P16/INTPZ14
285	M4	P17/INTPZ15
286	N4	V_{DD33}
287	P4	V_{DD33}
288	R4	GND
289	T4	VBUSDET
290	U4	RESETZ
291	V4	V_{DD33}
292	W4	GND
293	Y4	GND
294	AA4	V_{DD33}
295	AB4	V_{DD33}
296	AC4	GND
297	AC5	GND
298	AC6	V_{DD33}
299	AC7	V_{DD33}
300	AC8	GND
301	AC9	V_{DD33}
302	AC10	GA_26
303	AC11	GA_30
304	AC12	GA_35
305	AC13	V_{DD33}
306	AC14	GND
307	AC15	GA_43
308	AC16	GA_47
309	AC17	GA_53
310	AC18	V_{DD33}
311	AC19	GND
312	AC20	V_{DD33}
313	AC21	V_{DD33}
314	AC22	GND
315	AC23	GND
316	AB23	V_{DD33}
317	AA23	V_{DD33}
318	Y23	GND
319	W23	GND
320	V23	V_{DD33}

Pin no.	Pin ID	Name
257	K22	V_{DD33}
258	J22	GND
259	H22	P72/CSZ2
260	G22	P74/CSZ4
261	F22	P82/HLDAKZ
262	E22	P85/SELFREFZ
263	D22	GND
264	C22	GND
265	C21	GND
266	C20	D6
267	C19	D9
268	C18	D13
269	C17	P131/DMARQZ1
270	C16	P121/TCZ1
271	C15	IROMEN
272	C14	DMS
273	C13	TRCDATA0
274	C12	TRCDATA2
275	C11	TRCDATA6
276	C10	TESTCLK
277	C9	RMODEZ
278	C8	TMODE3
279	C7	AGND_PLL
280	C6	AV_{DD}_PLL
281	C5	UCLKSEL0
282	C4	GND
283	D4	GND
284	E4	GND
285	F4	V_{DD15}
286	G4	TMC1_A
287	H4	P41/TI1
288	J4	P45/TCLR1
289	K4	P51/TO1
290	L4	P01/INTPZ1
291	M4	P04/INTPZ4
292	N4	V_{DD15}
293	P4	V_{DD15}
294	R4	P14/INTPZ12
295	T4	P30/RXD0
296	U4	P32/RXD1
297	V4	P36/RXD3
298	W4	V_{DD33}
299	Y4	MODE0
300	AA4	OCI0
301	AB4	GND
302	AC4	RESETZ
303	AD4	TDO_A
304	AE4	TDI_G
305	AF4	V_{DD33}
306	AF5	GA_7
307	AF6	V_{DD33}
308	AF7	GA_14
309	AF8	GA_17
310	AF9	GA_21
311	AF10	GA_26
312	AF11	GA_31
313	AF12	GA_35
314	AF13	GA_38
315	AF14	GA_42
316	AF15	GA_47
317	AF16	GA_52
318	AF17	GA_56
319	AF18	GA_61
320	AF19	V_{DD33}

Pin no.	Pin ID	Name
321	U23	P65/A25
322	T23	P62/A22
323	R23	P66/A0
324	P23	GND
325	N23	V_{DD33}
326	M23	V_{DD33}
327	L23	A18
328	K23	SDCASZ
329	J23	DQM0
330	H23	GND
331	G23	V_{DD33}
332	F23	V_{DD33}
333	E23	P80/IOWRZ
334	D23	GND
335	D22	D1
336	D21	GND
337	D20	V_{DD15}
338	D19	V_{DD15}
339	D18	NMI
340	D17	EVIN
341	D16	DDO
342	D15	TRCDATA4
343	D14	V_{DD15}
344	D13	V_{DD15}
345	D12	GND
346	D11	AV_{DD}_PLL
347	D10	AGND_PLL
348	D9	V_{DD15}
349	D8	V_{DD15}
350	D7	GND
351	D6	V_{DD33}
352	D5	V_{DD33}
353	J9	V_{DD15}
354	K9	V_{DD15}
355	L9	V_{DD15}
356	M9	V_{DD15}
357	N9	V_{DD15}
358	P9	GND
359	R9	GND
360	T9	V_{DD33}
361	U9	V_{DD33}
362	V9	V_{DD33}
363	V10	V_{DD33}
364	V11	V_{DD33}
365	V12	GND
366	V13	GND
367	V14	GND
368	V15	GND
369	V16	V_{DD33}
370	V17	V_{DD33}
371	V18	V_{DD33}
372	U18	V_{DD33}
373	T18	V_{DD33}
374	R18	GND
375	P18	GND
376	N18	V_{DD15}
377	M18	V_{DD15}
378	L18	V_{DD15}
379	K18	V_{DD15}
380	J18	V_{DD15}
381	J17	V_{DD15}
382	J16	V_{DD15}
383	J15	GND
384	J14	GND

Pin no.	Pin ID	Name
385	J13	GND
386	J12	GND
387	J11	V_{DD15}
388	J10	V_{DD15}
389	K10	V_{DD15}
390	L10	V_{DD15}
391	M10	V_{DD15}
392	N10	V_{DD15}
393	P10	GND
394	R10	GND
395	T10	V_{DD33}
396	U10	V_{DD33}
397	U11	V_{DD33}
398	U12	GND
399	U13	GND
400	U14	GND
401	U15	GND
402	U16	V_{DD33}
403	U17	V_{DD33}
404	T17	V_{DD33}
405	R17	GND
406	P17	GND
407	N17	V_{DD15}
408	M17	V_{DD15}
409	L17	V_{DD15}
410	K17	V_{DD15}
411	K16	V_{DD15}
412	K15	GND
413	K14	GND
414	K13	GND
415	K12	GND
416	K11	V_{DD15}
417	L11	V_{DD15}
418	M11	V_{DD15}
419	N11	V_{DD15}
420	P11	GND
421	R11	GND
422	T11	V_{DD33}
423	T12	GND
424	T13	GND
425	T14	GND
426	T15	GND
427	T16	V_{DD33}
428	R16	GND
429	P16	GND
430	N16	V_{DD15}
431	M16	V_{DD15}
432	L16	V_{DD15}
433	L15	GND
434	L14	GND
435	L13	GND
436	L12	GND
437	M12	GND
438	N12	GND
439	P12	GND
440	R12	GND
441	R13	GND
442	R14	GND
443	R15	GND
444	P15	GND
445	N15	GND
446	M15	GND
447	M14	GND
448	M13	GND

Pin no.	Pin ID	Name
449	N13	GND
450	P13	GND
451	P14	GND
452	N14	GND

11.5 Oscillator-Block Pins That Can Be Arranged for Gate Array

When the gate array is equipped with oscillator block, please use the following oscillator-block pins that can be arranged. These pins are designed so that interval between the pin pairs becomes equal to that of the noise-conscious pattern design. However, the number of the oscillator blocks that can be equipped is two or less.

When the oscillator block is not used, the oscillator-block pins that can be arranged will be usable as normal user pins.

Example: When two oscillator blocks are equipped in MC-10501 (464 pins), the XT1/XT2 pins of one oscillator block are assigned to GA_11/GA_12, and the XT1/XT2 pins of another oscillator block are assigned to GA_66/GA_67.

Table 11-3. Position Where Oscillator Block Can Be Arranged (16-bit External Bus)

Master	PBGA	FPBGA	
	464 pins (25 × 30 mm)	452 pins (22 × 22 mm)	433 pins (17 × 17 mm)
	1.00 mm ball pitch	0.80 mm ball pitch	0.65 mm ball pitch
MC-10501	GA_11/GA_12 and GA_66/GA_67	No development plan	No development plan
MC-10502	GA_11/GA_12 and GA_60/GA_61	GA_14/GA_15 and GA_63/GA_64	To be planned
MC-10503	GA_11/GA_12 and GA_60/GA_61	T.B.D.	No development plan

Table 11-4. Position Where Oscillator Block Can Be Arranged (32-bit External Bus)

Master	PBGA
	550 pins (25 × 30 mm)
	1.00 mm ball pitch
MC-10505	GA_11/GA_12 and GA_66/GA_67
MC-10506	T.B.D.
MC-10507	T.B.D.

11.6 Thermal Resistance

The maximum allowable power consumption under usage environment conditions must be calculated by means of the maximum junction temperature (T_J (MAX.)), the maximum ambient temperature (T_A (MAX.)) and the thermal resistance (θ_{ja}) specified for each package and master.

$P_{WL} = (125 - T_A) / \theta_{ja}$ (W)
Condition $T_A \geq 40$ °C

Table 11-5. Thermal Resistance (16-bit External Bus)

Master	PBGA	FPBGA	
	464 pins (25 × 30 mm)	452 pins (22 × 22 mm)	433 pins (17 × 17 mm)
	1.00 mm ball pitch	0.80 mm ball pitch	0.65 mm ball pitch
MC-10501	16.87 °C/W	No development plan	No development plan
MC-10502	16.52 °C/W	16.12 °C/W	To be planned
MC-10503	16.18 °C/W	T.B.D.	No development plan

Table 11-6. Thermal Resistance (32-bit External Bus)

Master	PBGA
	550 pins (25 × 30 mm)
	1.00 mm ball pitch
MC-10505	14.71 °C/W
MC-10506	T.B.D.
MC-10507	T.B.D.

11.7 Allowable Power Consumption

The allowable power consumption specified for each package and master is shown below for reference.

Conditions Maximum Junction Temperature (T_J (MAX.): 125 °C
Maximum Ambient Temperature (T_A (MAX.): 85 °C
PFESiP/V850EP1 Power Consumption: 1.5 W

Please calculate the maximum allowable power for for each package under the customer usage environment conditions.

Table 11-7. Allowable Power Consumption (16-bit External Bus)

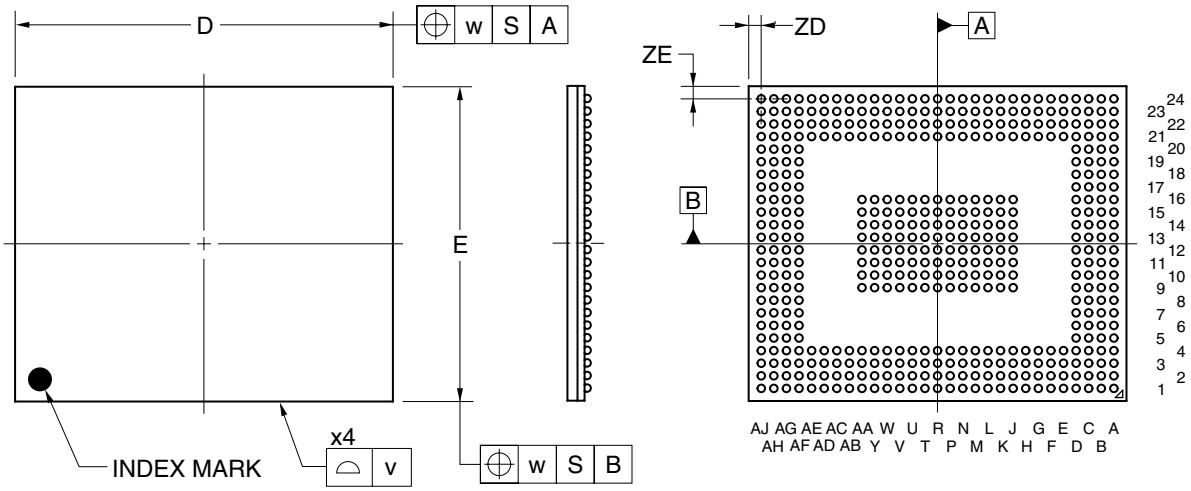
Master	PBGA	FPBGA	
	464 pins (25 × 30 mm)	452 pins (22 × 22 mm)	433 pins (17 × 17 mm)
	1.00 mm ball pitch	0.80 mm ball pitch	0.65 mm ball pitch
MC-10501	0.87 W	No development plan	No development plan
MC-10502	0.92 W	0.98 W	To be planned
MC-10503	0.97 W	T.B.D.	No development plan

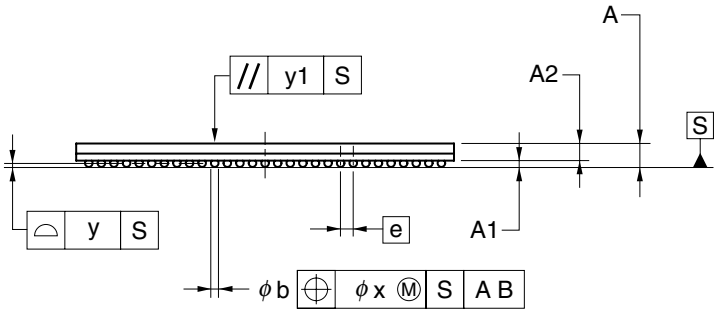
Table 11-8. Allowable Power Consumption (32-bit External Bus)

Master	PBGA
	550 pins (25 × 30 mm)
	1.00 mm ball pitch
MC-10505	1.22 W
MC-10506	T.B.D.
MC-10507	T.B.D.

11.8 Package Drawings

11.8.1 464-pin PBGA



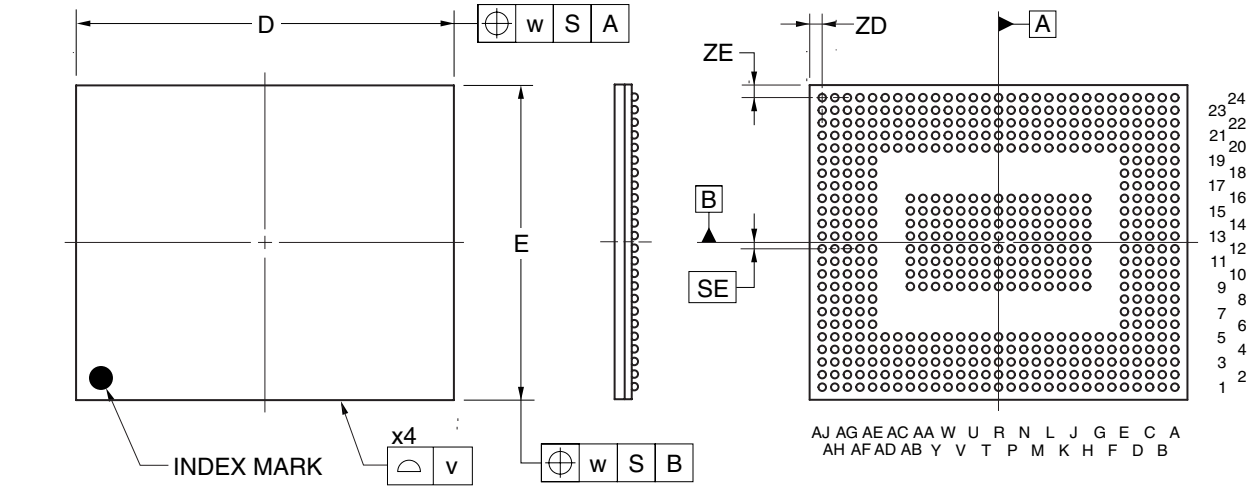


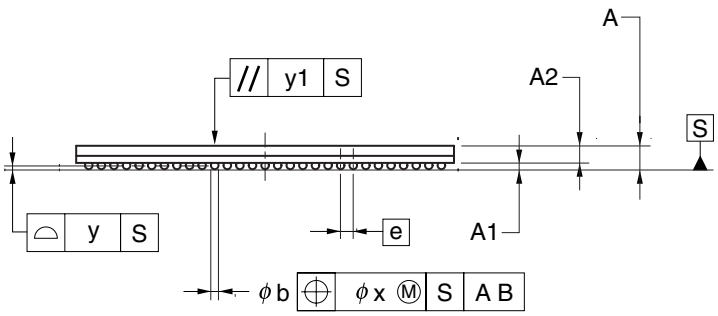
(UNIT:mm)

ITEM	DIMENSIONS
D	30.00±0.10
E	25.00±0.10
v	0.20
w	0.30
A	1.83±0.20
A1	0.50±0.10
A2	1.33
e	1.00
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P464F1-100-LT3

11.8.2 550-pin PBGA





(UNIT:mm)

ITEM	DIMENSIONS
D	30.00±0.10
E	25.00±0.10
v	0.20
w	0.30
A	1.86±0.20
A1	0.50±0.10
A2	1.36
e	1.00
SE	0.50
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P550F1-100-LT2

11.8.3 452-pin FPBGA

T.B.D.

11.9 Package Markings

The following shows examples of the markings for various packages. In some cases, the type font, size, and relative positions of the markings may differ from the examples shown here.

Caution Be sure to confirm with NEC Electronics that the desired package has been released.
Also contact NEC Electronics when the desired package does not appear in the package list.

Figure 11-9. 464-pin PBGA and 550-pin PBGA (25 × 30 mm) (Example of Standard Marking)

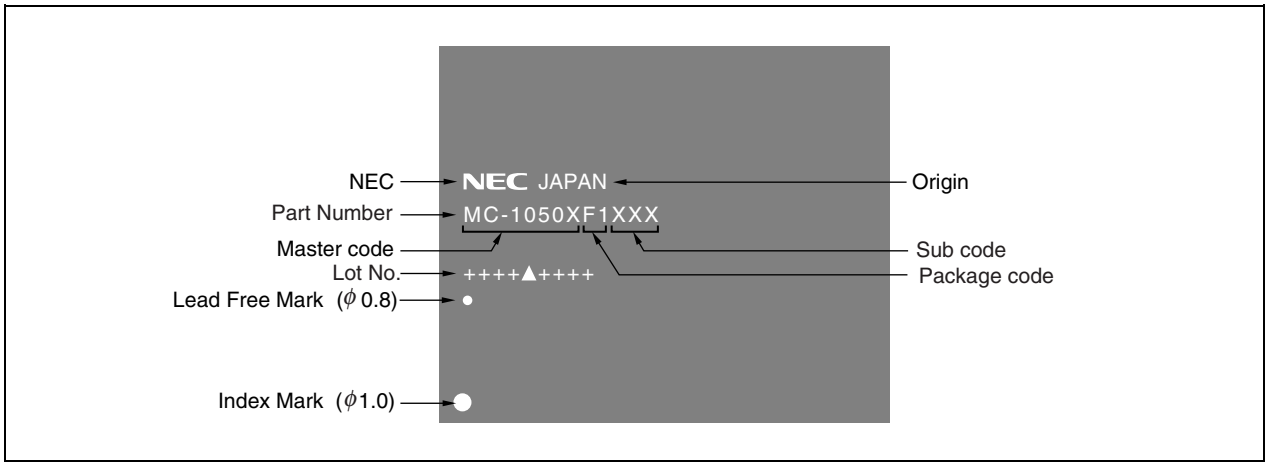


Figure 11-10. 452-pin PBGA (22 × 22 mm) (Example of Standard Marking)

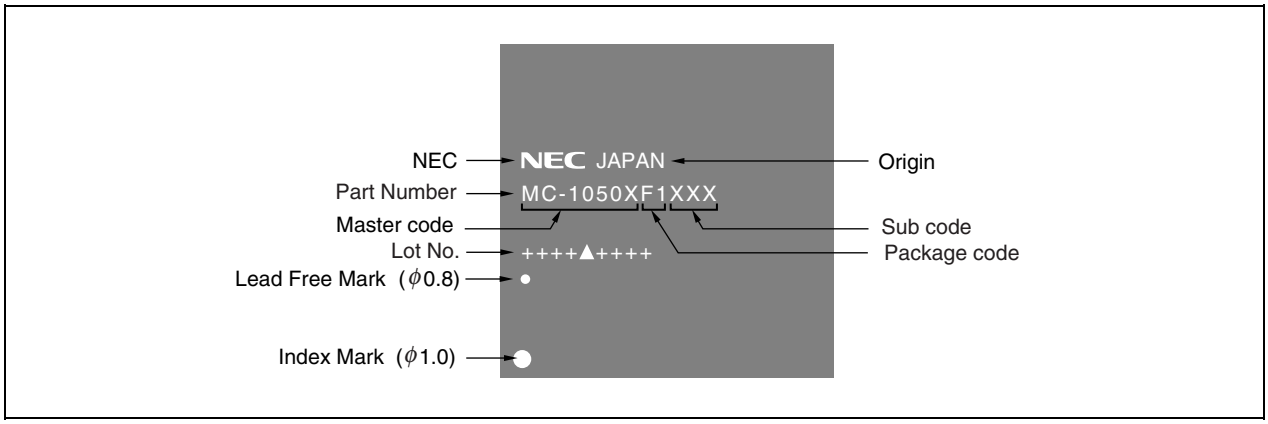
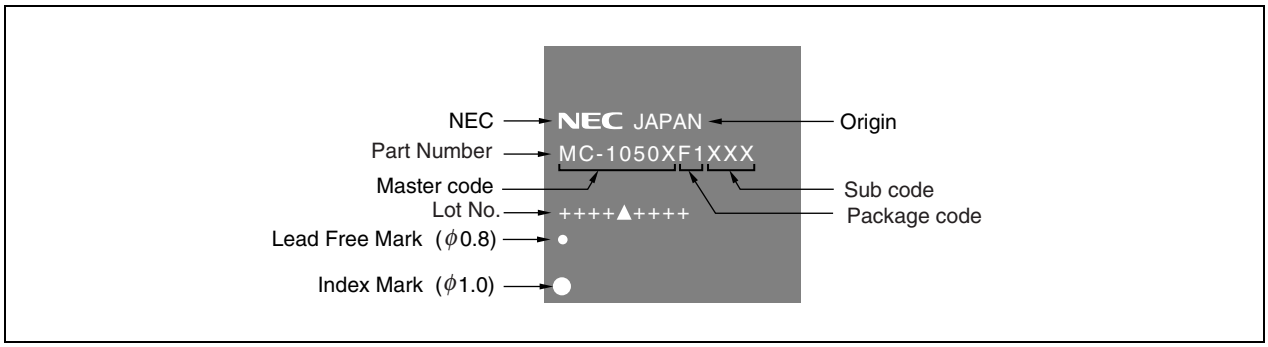


Figure 11-11. 433-pin FPBGA (17 × 17 mm) (Example of Standard Marking)



11.10 Recommended Soldering Conditions

The PFESiP EP-1 Series is Lead (Pb)-free product.
This product should be soldered and mounted under the following recommended conditions.
For the details of the recommended soldering conditions, refer to the below.

Semiconductor Device Mounting Technology Manual (http://www.necel.com/pkg/en/mount/index.html)

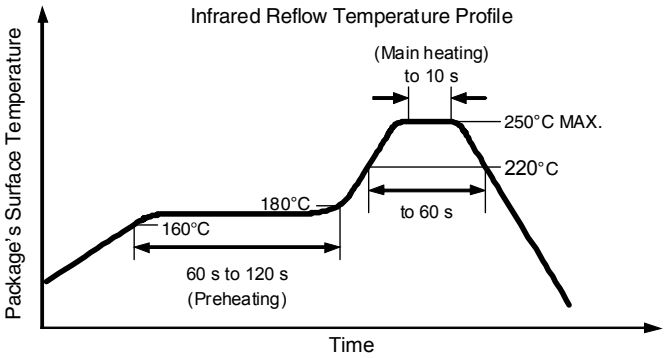
Table 11-9. Recommended Soldering Conditions (16-bit External Bus)

Master	PBGA	FPBGA	
	464 pins (25 × 30 mm)	452 pins (22 × 22 mm)	433 pins (17 × 17 mm)
	1.00 mm ball pitch	0.80 mm ball pitch	0.65 mm ball pitch
MC-10501	IR50-207-3	No development plan	No development plan
MC-10502	IR50-207-3	IR50-207-3	To be planned
MC-10503	IR50-207-3	T.B.D.	No development plan

Table 11-10. Recommended Soldering Conditions (32-bit External Bus)

Master	PBGA
	550 pins (25 × 30 mm)
	1.00 mm ball pitch
MC-10505	IR50-207-3
MC-10506	T.B.D.
MC-10507	T.B.D.

Table 11-11. Soldering Conditions

Recommended Condition Symbol	Soldering Method	Soldering Condition
IR50-207-3	Infrared Reflow	Maximum temperature (package's surface temperature): 250°C or below Time at maximum temperature: 10 s or less Time of temperature higher than 220°C: 60 s or less Preheating time at 160 to 180°C : 60 s to 120 s  The maximum number of reflow times: 3 Maximum chlorine content of rosin flux (percentage mass): 0.2 % The time limit after the dry pack has been opened: 7 days[Note1] (The 125°C pre-baking of 10 to 72 hour is required, when soldering after the 7 days.)[Note2]

Notes 1. It is the maximum storage-days after the dry pack has been opened, and the storage condition is 25°C , 65%RH.

2. Packages including magazine and taping except heat-resistant tray, can not be baked as matters now stand.

APPENDIX A POWER CONSUMPTION

An accurate calculation of the power consumption of internal circuits requires a very large amount of information, such as capacitance, number of synchronously operating blocks, and operating frequency of each block. Consequently, the calculation becomes too complicated to be performed. On the basis of assumptions concerning such items as circuit operation and configuration, NEC Electronics provides reference values for power consumption.

It must be noted that these values may be larger or smaller than the actual values, depending on factors such as the user's actual circuit and its configuration.

This chapter provides a power consumption calculation method that divides the power consumption of the internal circuit into combination circuits, latches, and flip-flops. This calculation should be used to review circuit power consumption. However, if the results are to be used to calculate the life-span of a battery, an extra margin should be provided.

Internal Cell Power Consumption

$$\Sigma P_{DCELL} = \Sigma P_{DGate} + \Sigma P_{DLatch} + \Sigma P_{DF/F} + \Sigma P_{DT}$$

(1) Combination circuits

$$P_{DGate} = 0.524 \times f \times Cell \ (\mu W)$$

f : Operating frequency of data (MHz)

Cell : Number of cells that operate at f **Note**

(2) Latches

$$P_{DLatch} = (P_{D(Gate = ON)} \times N + P_{D(Gate = OFF)} \times (1 - N)) \times f \times Cell \ (\mu W)$$

f : Operating frequency of data (MHz)

Cell : Number of cells that operate at f **Note**

N : Percentage of "Gate = ON" = $\dfrac{T_{(Gate = ON)}}{T_{(Gate = ON)} + T_{(Gate = OFF)}}$

$P_{D(Gate = ON)}$:0.516 (μW/Cell/MHz)

$P_{D(Gate = OFF)}$:0.0385 (μW/Cell/MHz)

Note "Cell" is not number of blocks.

(3) D-F/F, JK-F/F, shift registers, and counters

$$P_{DF/F} = \frac{2 \times P_{D(OUTPUT)} + P_{D(CLK)} \times (N - 2)}{N} \times f \times Cell \ (\mu W)$$

f : Operating frequency of data (MHz)

Cell : Number of cells that operate at f **Note**

N : $\dfrac{T_{(DATA)}}{T_{(CLK)}}$

$P_{D(OUTPUT)}$:0.412 (μW/Cell/MHz)

$P_{D(CLK)}$:0.121 (μW/Cell/MHz)

Remark T (DATA): Data cycle

T (CLK): Clock cycle

Example When the clock is twice as fast as one data cycle: N = 1/0.5 = 2

(4) T-F/F

$$P_{DT} = 0.367 \times f \times Cell \ (\mu W)$$

f : Clock operating frequency (MHz)

Cell : Number of cells that operate at f **Note**

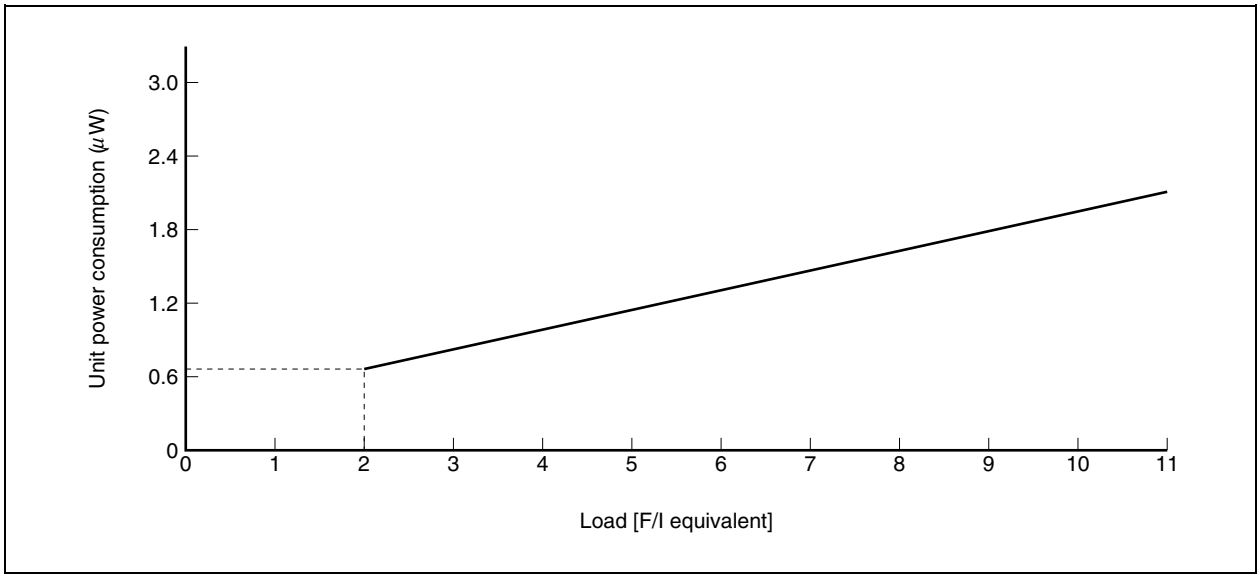
Note "Cell" is not number of blocks.

(5) Load dependency of power consumption (preliminary)

Power consumption depends to a great extent on the load capacitance, as expressed by $P_D = CV^2f$.

Note "Cell" is not number of blocks.

Figure A-1. Load Dependency of Power Consumption



As shown in Figure A-1, the unit power consumption when F/O = 2 is an extremely small 0.66 μW/MHz. Because power consumption has a significant effect on reliability, a realistic value must be used.

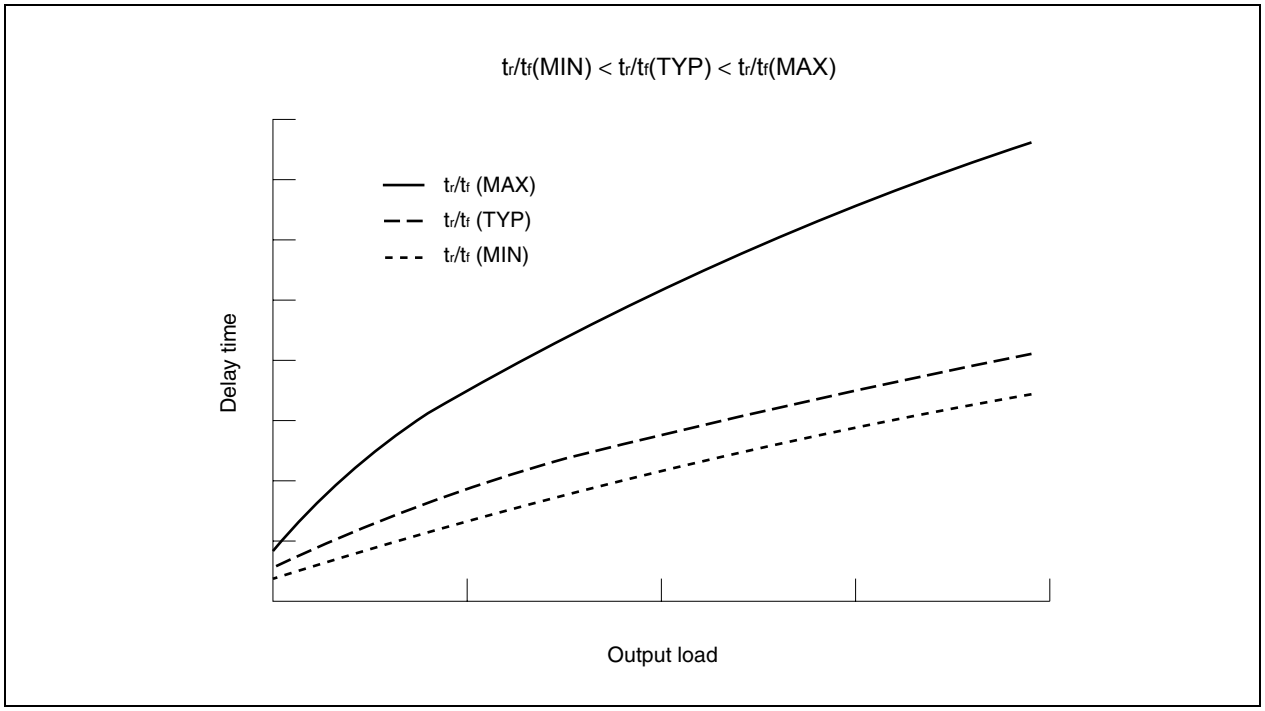
The value of load = 4.98 (F/I equivalent) covers a distribution of about 70% of load values, based on statistical data accumulated at NEC Electronics, such as wiring length and pin pairs.

Load = 4.98 (F/I equivalent) Example F/O:2+λ:2.98

APPENDIX B PROPAGATION DELAY TIME

The propagation delay time of each block varies significantly with the input signal waveform as shown in Figure B-1. With the EA-9HD Series, whose delay time is as short as several 100 ps at each block, the influence of the input waveform is not negligible.

Figure B-1. Delay Time Increase Due to Input Waveform



Consequently, the simulator considers the input waveform of each block so that highly accurate delay simulation is executed. However, discrepancies in results due to the input waveform cannot be listed in the block library[Note]. For this reason, the accuracy of the propagation delay time calculations listed in the block library[Note] are valid only under certain limited conditions. The propagation delay times of critical paths, in which the load is likely to be light, are calculated accurately in the EA-9HD Series.

Note that Figure B-1 is indicating a tendency only. Verify the actual value by performing simulation.

Note CMOS-9HD Series, EA-9HD Series Block Library (A13052E)

APPENDIX C ALBATROSS AND DIF FILE FORMATS

C.1 ALBATROSS File Format (Circuit Name.alb)

(1) File format

The ALBATROSS file format has the following characteristics:

- Free format
- Parameters must be delimited by blank space or a colon (:).
- Each statement must be terminated with a semicolon (;).
- Items within brackets ([ ]) can be repeated.
- Maximum of 80 columns per line (when the last character is not a semicolon, the line must continue on the next line)
- Identifiers, pin names, and units (NS; fixed) must be specified in uppercase letters
- Pin names consist of a maximum of 64 characters
- The description of the timing data (MODULATION + CLOCK) is based on the limitations shown for the High-speed function test in the “Design Manual” for each Series.

(2) File configuration

The ALBATROSS file consists of the following seven parameters.

*ALBATROSS .....File header
*TIMING .....Header
PERIOD.....Pattern period
MODULATION .....Input skew
CLOCK.....Clock pin
*END_OF_TIMING.....End record
*END .....File end

(3) Details of file

The details of each parameter are as follows:

(a) File header

Syntax: *ALBATROSS circuit;
Function: Pattern header
1: circuit (character string) circuit name

(b) Header

Syntax: *TIMING
Function: Header

(c) Pattern period

Syntax: PERIOD period_t time_unit;
Function: Period value of pattern

1: period_t Pattern cycle
2: time_unit Cycle time

(d) Input skew

Syntax: MODULATION modulation_t time_unit: [pin];
Function: Value of skew added to input pin

1: modulation_t Value of input skew
2: time_unit Unit of value of skew
3: pin Pin name

(e) Clock

Syntax: CLOCKTYPE = type: [ch_time time_unit]: pin;
Function: Definition of clock pin and clock waveform

• TYPE = type
P: Positive clock
N: Negative clock
• ch_time Waveform time
• time_unit Unit of change time
• pin Pin name

(f) End

Syntax: *END_OF_TIMING;
Function: End

(g) File end

Syntax: *END
Function: File end

(4) Example

```
*ALBATROSSΔCF191
*TIMING;
PERIOD 200 NS;
MODULATION 20 NS: IN1 IN2 IN3;
CLOCK TYPE = P: 50NS 150NS:CLK;
*END_OF_TIMING;
*END
```

C.2 DIF File Format (Circuit Name.dif)

For details, see **NEC SYSTEM LSI DESIGN OPENCAD OPC_VSHELL User's Manual (A15050E)**.

(1) File format

The DIF file format has the following characteristics:

- Free format
- The delimiter is a blank space.
- Maximum of 512 characters per line
- The first column of a comment line begins with [-].

(2) File configuration

The DIF file consists of the following three parameters:

DIF ..... Header
/DESIGN..... Design block
/END..... End

(3) Details of file

The details of each parameter are as follows:

(a) Header

Syntax: DIF
Function: Header

(b) Design block

Syntax: /PIA
Function: Whole external pin (V_{DD}, VBLK52 <R> [Note], GND, etc.)

Note External 5 V power supply for in 5 V areas

(c) Condition block

Syntax: /PIN
Function: Whole design (value of pin capacitance added to output pin, etc.)

(d) End card

Syntax: /END
Function: End of the DIF file

(4) Example

```
*DIF opc_pinbe (1.11) 2002.12.12 (12:39:32)
/DESIGN 65445999
 TECHNOLOGY = EA9HD;
 CONDITION = cmos_3.3V;
 MASTER = 65445;
 PACKAGE = LQFP;
 PINS = 144;
 LAYER = 3L;
  /CONDITION 1
   /PIN
      ADO
          DIR = INPUT
      ;
      DATA1
          DIR = IO
      ;
      PC1
          DIR = OUTPUT
      ;
     /END PIN
  /END CONDITION
 /PIA
  /EPIN PAD
    ADO
          PAD =        77 # dut_ID 22 pin_type IN
          BLOCK = XINB;
    DATA1
          PAD =         24 # dut_ID 179 pin_type IO
          BLOCK = XWN2;
    PCR1
          PAD =       125 # dut_ID 68 pin_type OUT
          BLOCK = XB0D;
  /END EPIN
    /POWER PAD
           GND PAD = 13 191;
           VDD PAD = 14;
           VBLK52 PAD = 15;
    /END POWER
/END PIA
/END DESIGN
*END
```

APPENDIX D DRAWING CIRCUIT DIAGRAMS AND TIMING CHARTS

D.1 Drawing Circuit Diagrams

Today, circuits are designed using an engineering workstation (EWS). The circuit diagram drawn by the user is converted to NEC format on the EWS or through the interface service offered by NEC Electronics.

When the user draws a circuit diagram, the following points should be kept in mind to ensure smooth interfacing with NEC Electronics.

D.1.1 Logic symbols

As a general rule, use the logic symbols that are in the block library[Note]. However, when there are differences between the EWS library and the block library[Note], follow the format of the EWS library.

Note CMOS-9HD Series, EA-9HD Series Block Library (A13052E)

D.1.2 Block names (function names)

Input buffers and other blocks have different designations, but may have logic symbols that are virtually the same. In particular, the various input/output buffer interface levels cannot be determined from simulation results. Because of this, the block name should be entered so that it is easily understood.

In addition, since block names are expressed in advance in EWS libraries, entries cannot be made by the EWS.

D.1.3 Pin names (I/O pin name of block)

Block I/O pins are named in the order “H01, H02,.../N01, N02,....” If a block has more than one I/O pin, the pin names must be used whenever possible. Pin names are usually displayed in EWS libraries. If a pin name is displayed, it need not be entered. For more information on displaying pin names, follow the instructions in the interface manual for the EWS.

D.1.4 Gate names (specific name of each block)

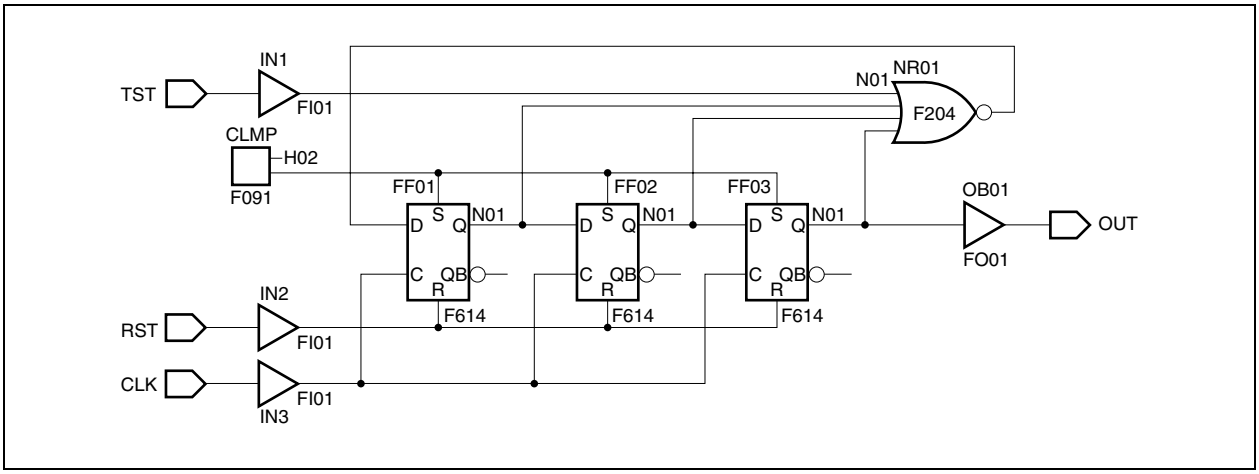
Enter the respective characteristic gate names for block names entered in a circuit diagram. A gate name must have 255 or fewer letters. To avoid duplication of gate names and pin names, make the names unique. When EWS is used, there are special cases where the naming rules are a function of the system being employed. See the EWS Interface Manual for details.

D.1.5 I/O pin names

A pin name of up to 64 alphanumeric characters must be assigned to each I/O pin of the LSI device. Each pin name must be unique and must not duplicate a gate name.

When EWS is used, there are special cases where the naming rules are a function of the system being employed. See the EWS Interface Manual for details.

Figure D-1. Circuit Diagram Example



(1) Input pin names

The pin name of an input pin must consist of up to 64 alphanumeric characters.

In addition, undefined and high impedance states cannot be input to an input pin because this causes the measurement conditions to change during testing with the LSI tester, making measurement impossible.

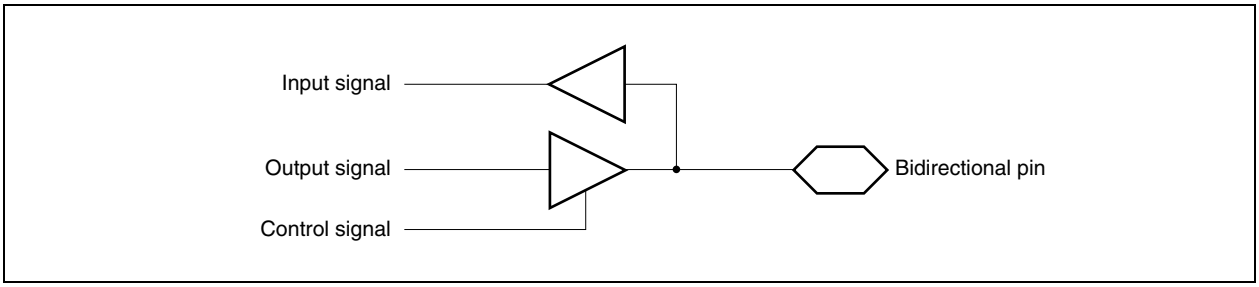
Undefined and high impedance states also cannot be input to the input pins of input buffers and bidirectional buffers with on-chip pull-up/pull-down resistors.

If undefined or high impedance states are input as a test pattern, an error will result when simulation is executed.

(2) Bidirectional pin names

If the input and output of a bidirectional buffer are implemented from one pin, this must be named by using a bidirectional pin. The pin name must consist of up to 64 alphanumeric characters.

Figure D-2. Bidirectional Pin Names



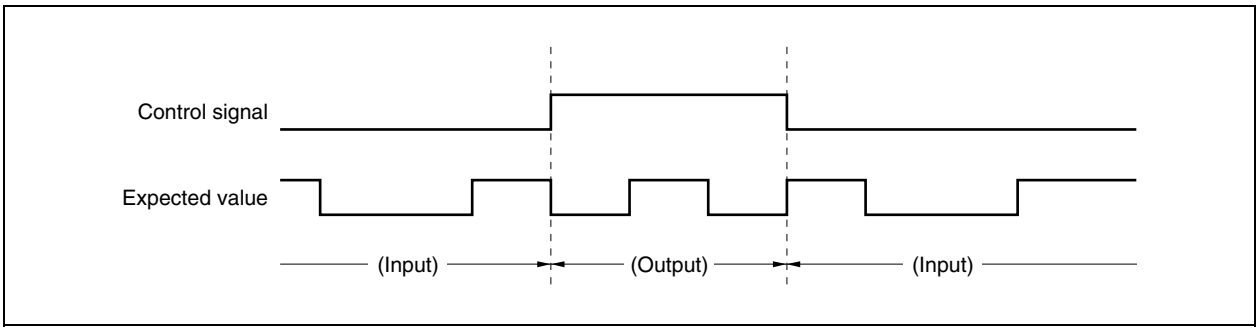
When a bidirectional pin test pattern is generated, care must be taken with regard to the following points:

<1> For switching from the output mode to the input mode, set the input and output signals to the same level.

<2> Do not set the control signal to the undefined state (if the state of the control signal becomes undefined, an undefined state is propagated to the input signal, generating an error in simulation).

During switching from the input mode to the output mode, an undefined state is propagated to the input signal due to the delay time of the control signal, generating an error in simulation. For such switching, it is important to configure the circuit so that an undefined state is not propagated to the input signal.

Figure D-3. Bidirectional Pin Test Pattern Generation



(3) 3-state output pin notation

3-state output pin must be named as shown in the examples in Figures D-4 and D-5. The pin name must consist of up to 64 alphanumeric characters.

Figure D-4. 3-state Output Pin Names

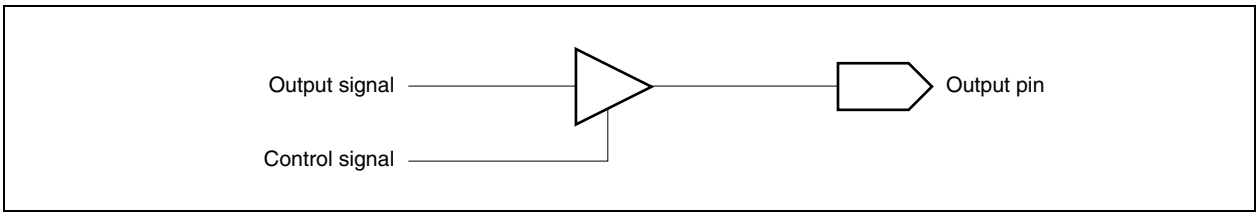
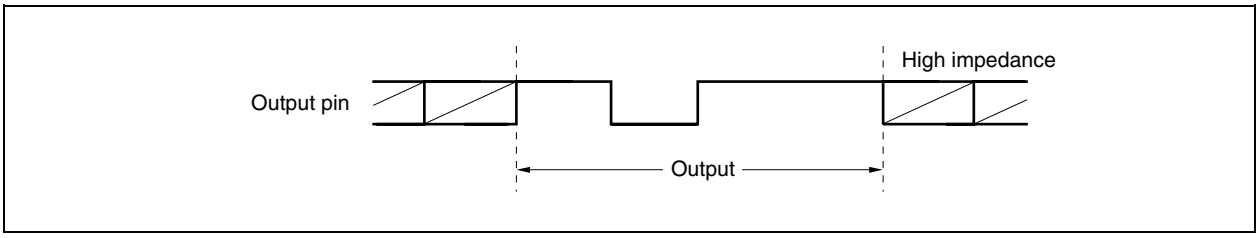


Figure D-5. 3-state Output Pin Test Pattern Generation



D.2 Handling Macros

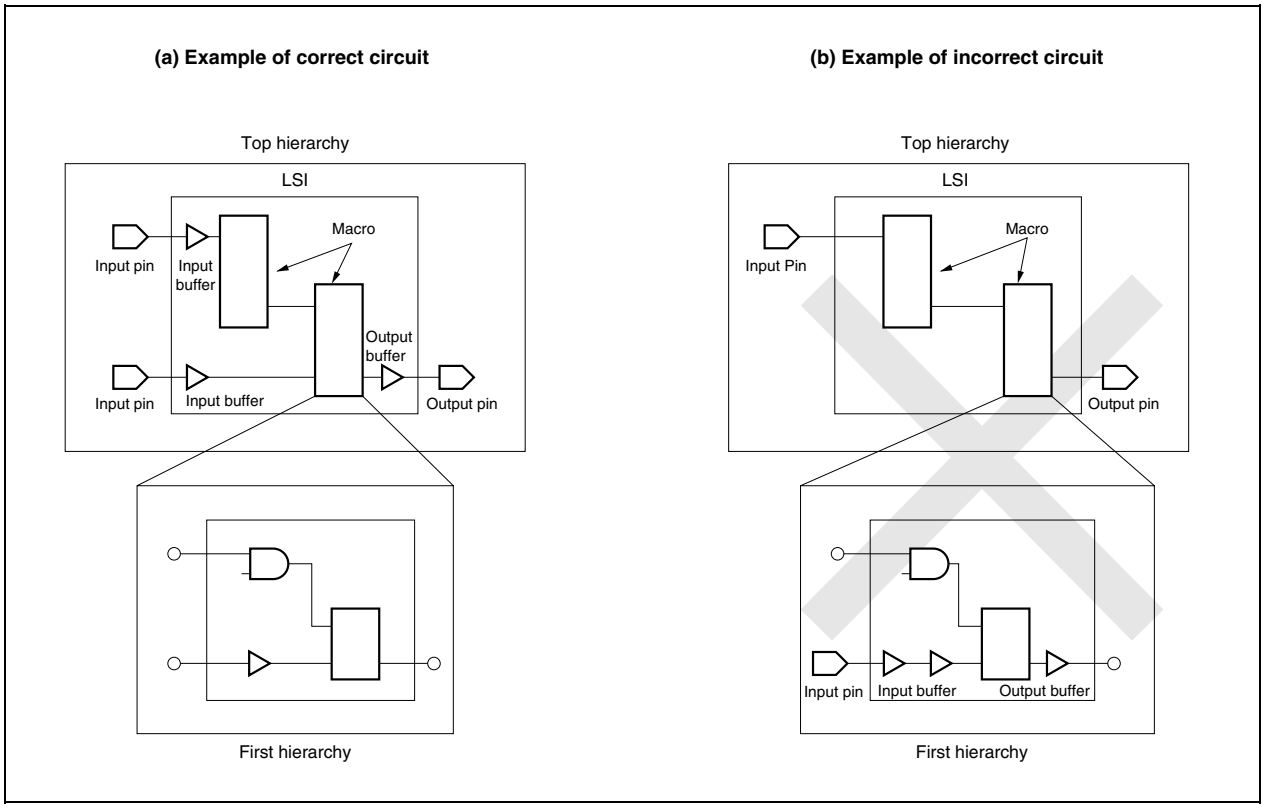
In logic design of a large scale circuit, in order to divide system internal block design and design man-hours, there are many cases where design is carried out using a hierarchical design method.

In the hierarchical design technique, functional units used in common are defined as macros (user macros). Each LSI chip is designed by connecting several macros to enable a specified function. In particular, a large-scale circuit is usually divided into several blocks, each of which is a hierarchical block and combined to configure the entire circuit.

In EWS, etc., if a hierarchical design is done using a user macro, please use caution concerning the following points (see Figure D-6).

<1> Each Hierarchical block should perform a single logical operation.
<2> Design so that the total structure and the signal flow can be understood at the highest stage (the highest stage should be drawn on a single page).
<3> Whenever possible, design circuits that include a feedback loop so that the loop fits within the macro.
<4> Input pins and clamps (if needed) must be on the same page.
<5> Exercise care in the clock line flow. Ensure that delay differentials between pages do not exceed the allowable system clock skew.
<6> Each macro (bottom layer) must have a single function.
<7> A page should not contain signal lines only (pass-through only).
<8> External I/O buffers can be specified only at the top level. Avoid connecting I/O pins directly to an external device from a macro lower than that at the top level.
<9> A macro should not contain input, output, and bidirectional buffers.

Figure D-6. Handling Macros



D.3 Preparing Timing Charts

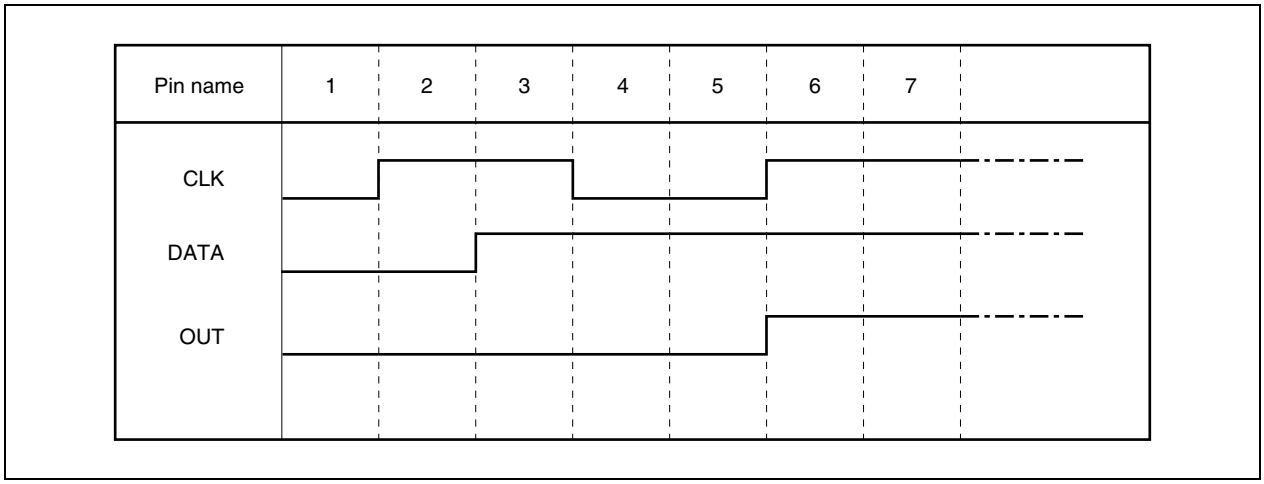
If the user provides NEC Electronics with a timing chart for generating the test patterns, or even if the user generates the test patterns, the timing charts must be drawn taking into account the following two points.

(1) Entry method

The pin names of all input/output pins must be written in the vertical column. For each pattern, describe a "1" or "0" pattern for inputs and the expected values for outputs. Continuous sequential numbers, starting with 1, must be assigned to the test patterns.

Figure D-7 shows an example of filling out the timing chart.

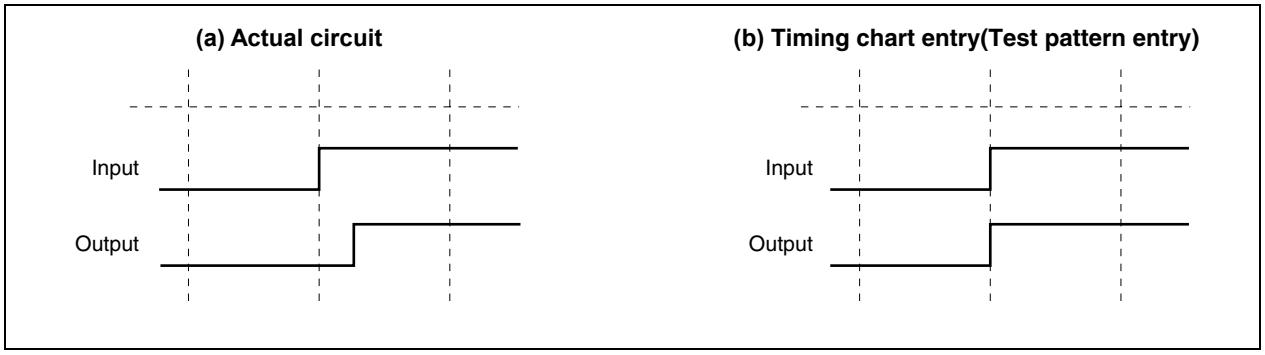
Figure D-7. Timing Chart Entry



(2) Timing discrepancies

Because the output in actual circuits changes after the input pattern is applied, there is a timing delay between the input and output, as shown in Figure D-8 (a). However, the delay time between the input and output can be ignored when test patterns are generated, as shown in Figure D-8 (b). The patterns must be generated so that the entire circuit operates by the same timing.

Figure D-8. Timing Chart



Entry example

	Mode No.	Specified pin	Output load (pF)	Pattern No.	Delay time (ns)		Judgment
					MIN	MAX	
1	1	IN1→OUT2	15	131	13	50	OK
2							
3							
4							
5							
6							

APPENDIX E LIST OF BLOCKS

E.1 Interface Block

E.1.1 3.3 V interface

Function	Block	Description	Cells (I/O)
Input Buffer	FI01	–	7 (1)
	FID1	50 kΩ Pull-down	7 (1)
	FIU1	50 kΩ Pull-up	7 (1)
	FIW1	5 kΩ Pull-up	7 (1)
	FIS1	Schmitt	11 (1)
	FDS1	Schmitt 50 kΩ Pull-down	11 (1)
	FUS1	Schmitt 50 kΩ Pull-up	11 (1)
	FWS1	Schmitt 5 kΩ Pull-up	11 (1)
	FIB1	Clock Driver	56 (1)
	FDB1	Clock Driver 50 kΩ Pull-down	56 (1)
	FUB1	Clock Driver 50 kΩ Pull-up	56 (1)
	FWB1	Clock Driver 5 kΩ Pull-up	56 (1)
Input Buffer with Failsafe	FIA1	–	7 (1)
	FDA1	50 kΩ Pull-down	7 (1)
	FIE1	Schmitt	11 (1)
	FDE1	Schmitt 50 kΩ Pull-down	11 (1)
	FIH1	Clock Driver	56 (1)
	FDH1	Clock Driver 50 kΩ Pull-down	56 (1)
Input Buffer with EN (AND)	FN11	–	8 (1)
	FN21	50 kΩ Pull-down	8 (1)
Input Buffer with EN (OR)	FN13	–	8 (1)
	FN23	50 kΩ Pull-down	8 (1)
Output Buffer	FO09	3 mA	8 (1)
	FO04	6 mA	8 (1)
	FO01	9 mA	8 (1)
	FO02	12 mA	8 (1)
	FO03	18 mA	18 (1)
	FO06	24 mA	18 (1)
Low-noise Output Buffer	FE04	6 mA	10 (1)
	FE01	9 mA	10 (1)
	FE02	12 mA	10 (1)
	FE03	18 mA	10 (1)
	FE06	24 mA	10 (1)

Function	Block	Description	Cells (I/O)
3-State Buffer	B00T	3 mA	18 (1)
	B0DT	3 mA 50 kΩ Pull-down	18 (1)
	B0UT	3 mA 50 kΩ Pull-up	18 (1)
	B0WT	3 mA 5 kΩ Pull-up	18 (1)
	B00E	6 mA	18 (1)
	B0DE	6 mA 50 kΩ Pull-down	18 (1)
	B0UE	6 mA 50 kΩ Pull-up	18 (1)
	B0WE	6 mA 5 kΩ Pull-up	18 (1)
	B008	9 mA	18 (1)
	B0D8	9 mA 50 kΩ Pull-down	18 (1)
	B0U8	9 mA 50 kΩ Pull-up	18 (1)
	B0W8	9 mA 5 kΩ Pull-up	18 (1)
	B007	12 mA	18 (1)
	B0D7	12 mA 50 kΩ Pull-down	18 (1)
	B0U7	12 mA 50 kΩ Pull-up	18 (1)
	B0W7	12 mA 5 kΩ Pull-up	18 (1)
	B009	18 mA	20 (1)
	B0D9	18 mA 50 kΩ Pull-down	20 (1)
	B0U9	18 mA 50 kΩ Pull-up	20 (1)
	B0W9	18 mA 5 kΩ Pull-up	20 (1)
	B00H	24 mA	20 (1)
	B0DH	24 mA 50 kΩ Pull-down	20 (1)
	B0UH	24 mA 50 kΩ Pull-up	20 (1)
	B0WH	24 mA 5 kΩ Pull-up	20 (1)
Low-noise 3-State Buffer	BE0E	6 mA	11 (1)
	BEDE	6 mA 50 kΩ Pull-down	11 (1)
	BEUE	6 mA 50 kΩ Pull-up	11 (1)
	BEWE	6 mA 5 kΩ Pull-up	11 (1)
	BE08	9 mA	11 (1)
	BED8	9 mA 50 kΩ Pull-down	11 (1)
	BEU8	9 mA 50 kΩ Pull-up	11 (1)
	BEW8	9 mA 5 kΩ Pull-up	11 (1)
	BE07	12 mA	11 (1)
	BED7	12 mA 50 kΩ Pull-down	11 (1)
	BEU7	12 mA 50 kΩ Pull-up	11 (1)
	BEW7	12 mA 5 kΩ Pull-up	11 (1)
	BE09	18 mA	11 (1)
	BED9	18 mA 50 kΩ Pull-down	11 (1)
	BEU9	18 mA 50 kΩ Pull-up	11 (1)
	BEW9	18 mA 5 kΩ Pull-up	11 (1)
	BE0H	24 mA	11 (1)
	BEDH	24 mA 50 kΩ Pull-down	11 (1)
	BEUH	24 mA 50 kΩ Pull-up	11 (1)
	BEWH	24 mA 5 kΩ Pull-up	11 (1)

Function	Block	Description	Cells (I/O)
N-ch Open drain Buffer	EXTH	3 mA	8 (1)
	EXUH	3 mA 50 kΩ Pull-up	8 (1)
	EXWH	3 mA 5 kΩ Pull-up	8 (1)
	EXTJ	6 mA	8 (1)
	EXUJ	6 mA 50 kΩ Pull-up	8 (1)
	EXWJ	6 mA 5 kΩ Pull-up	8 (1)
	EXT1	9 mA	8 (1)
	EXT3	9 mA 50 kΩ Pull-up	8 (1)
	EXW3	9 mA 5 kΩ Pull-up	8 (1)
	EXT9	12 mA	8 (1)
	EXTB	12 mA 50 kΩ Pull-up	8 (1)
	EXWB	12 mA 5 kΩ Pull-up	8 (1)
	EXT5	18 mA	18 (1)
	EXT7	18 mA 50 kΩ Pull-up	18 (1)
	EXW7	18 mA 5 kΩ Pull-up	18 (1)
	EXTD	24 mA	18 (1)
	EXTF	24 mA 50 kΩ Pull-up	18 (1)
	EXWF	24 mA 5 kΩ Pull-up	18 (1)
Low-noise N-ch Open drain Buffer	EETJ	6 mA	5 (1)
	EEUJ	6 mA 50 kΩ Pull-up	5 (1)
	EEWJ	6 mA 5 kΩ Pull-up	5 (1)
	EET1	9 mA	5 (1)
	EET3	9 mA 50 kΩ Pull-up	5 (1)
	EEW3	9 mA 5KΩ Pull-up	5 (1)
	EET9	12 mA	5 (1)
	EETB	12 mA 50 kΩ Pull-up	5 (1)
	EEWB	12 mA 5 kΩ Pull-up	5 (1)
	EET5	18 mA	5 (1)
	EET7	18 mA 50 kΩ Pull-up	5 (1)
	EEW7	18 mA 5 kΩ Pull-up	5 (1)
	EETD	24 mA	5 (1)
	EETF	24 mA 50 kΩ Pull-up	5 (1)
	EEWF	24 mA 5 kΩ Pull-up	5 (1)

Function	Block	Description	Cells (I/O)
I/O Buffer	B00U	3 mA	25 (1)
	B0DU	3 mA 50 kΩ Pull-down	25 (1)
	B0UU	3 mA 50 kΩ Pull-up	25 (1)
	B0WU	3 mA 5 kΩ Pull-up	25 (1)
	B00C	6 mA	25 (1)
	B0DC	6 mA 50 kΩ Pull-down	25 (1)
	B0UC	6 mA 50 kΩ Pull-up	25 (1)
	B0WC	6 mA 5 kΩ Pull-up	25 (1)
	B003	9 mA	25 (1)
	B0D3	9 mA 50 kΩ Pull-down	25 (1)
	B0U3	9 mA 50 kΩ Pull-up	25 (1)
	B0W3	9 mA 5 kΩ Pull-up	25 (1)
	B001	12 mA	25 (1)
	B0D1	12 mA 50 kΩ Pull-down	25 (1)
	B0U1	12 mA 50 kΩ Pull-up	25 (1)
	B0W1	12 mA 5 kΩ Pull-up	25 (1)
	B005	18 mA	27 (1)
	B0D5	18 mA 50 kΩ Pull-down	27 (1)
	B0U5	18 mA 50 kΩ Pull-up	27 (1)
	B0W5	18 mA 5 kΩ Pull-up	27 (1)
	B00F	24 mA	27 (1)
	B0DF	24 mA 50 kΩ Pull-down	27 (1)
	B0UF	24 mA 50 kΩ Pull-up	27 (1)
	B0WF	24 mA 5 kΩ Pull-up	27 (1)
Low-noise I/O Buffer	BE0C	6 mA	18 (1)
	BEDC	6 mA 50 kΩ Pull-down	18 (1)
	BEUC	6 mA 50 kΩ Pull-up	18 (1)
	BEWC	6 mA 5 kΩ Pull-up	18 (1)
	BE03	9 mA	18 (1)
	BED3	9 mA 50 kΩ Pull-down	18 (1)
	BEU3	9 mA 50 kΩ Pull-up	18 (1)
	BEW3	9 mA 5 kΩ Pull-up	18 (1)
	BE01	12 mA	18 (1)
	BED1	12 mA 50 kΩ Pull-down	18 (1)
	BEU1	12 mA 50 kΩ Pull-up	18 (1)
	BEW1	12 mA 5 kΩ Pull-up	18 (1)
	BE05	18 mA	18 (1)
	BED5	18 mA 50 kΩ Pull-down	18 (1)
	BEU5	18 mA 50 kΩ Pull-up	18 (1)
	BEW5	18 mA 5 kΩ Pull-up	18 (1)
	BE0F	24 mA	18 (1)
	BEDF	24 mA 50 kΩ Pull-down	18 (1)
	BEUF	24 mA 50 kΩ Pull-up	18 (1)
	BEWF	24 mA 5 kΩ Pull-up	18 (1)

Function	Block	Description	Cells (I/O)
Schmitt I/O Buffer	BSIU	3 mA	29 (1)
	BSDU	3 mA 50 kΩ Pull-down	29 (1)
	BSUU	3 mA 50 kΩ Pull-up	29 (1)
	BSWU	3 mA 5 kΩ Pull-up	29 (1)
	BSIC	6 mA	29 (1)
	BSDC	6 mA 50 kΩ Pull-down	29 (1)
	BSUC	6 mA 50 kΩ Pull-up	29 (1)
	BSWC	6 mA 5 kΩ Pull-up	29 (1)
	BSI3	9 mA	29 (1)
	BSD3	9 mA 50 kΩ Pull-down	29 (1)
	BSU3	9 mA 50 kΩ Pull-up	29 (1)
	BSW3	9 mA 5 kΩ Pull-up	29 (1)
	BSI1	12 mA	29 (1)
	BSD1	12 mA 50 kΩ Pull-down	29 (1)
	BSU1	12 mA 50 kΩ Pull-up	29 (1)
	BSW1	12 mA 5 kΩ Pull-up	29 (1)
	BSI5	18 mA	31 (1)
	BSD5	18 mA 50 kΩ Pull-down	31 (1)
	BSU5	18 mA 50 kΩ Pull-up	31 (1)
	BSW5	18 mA 5 kΩ Pull-up	31 (1)
	BSIF	24 mA	31 (1)
	BSDF	24 mA 50 kΩ Pull-down	31 (1)
	BSUF	24 mA 50 kΩ Pull-up	31 (1)
	BSWF	24 mA 5 kΩ Pull-up	31 (1)
Low-noise Schmitt I/O Buffer	BFIC	6 mA	22 (1)
	BFDC	6 mA 50 kΩ Pull-down	22 (1)
	BFUC	6 mA 50 kΩ Pull-up	22 (1)
	BFWC	6 mA 5 kΩ Pull-up	22 (1)
	BFI3	9 mA	22 (1)
	BFD3	9 mA 50 kΩ Pull-down	22 (1)
	BFU3	9 mA 50 kΩ Pull-up	22 (1)
	BFW3	9 mA 5 kΩ Pull-up	22 (1)
	BFI1	12 mA	22 (1)
	BFD1	12 mA 50 kΩ Pull-down	22 (1)
	BFU1	12 mA 50 kΩ Pull-up	22 (1)
	BFW1	12 mA 5 kΩ Pull-up	22 (1)
	BFI5	18 mA	22 (1)
	BFD5	18 mA 50 kΩ Pull-down	22 (1)
	BFU5	18 mA 50 kΩ Pull-up	22 (1)
	BFW5	18 mA 5 kΩ Pull-up	22 (1)
	BFIF	24 mA	22 (1)
	BFDF	24 mA 50 kΩ Pull-down	22 (1)
	BFUF	24 mA 50 kΩ Pull-up	22 (1)
	BFWF	24 mA 5 kΩ Pull-up	22 (1)

Function	Block	Description	Cells (I/O)
I/O Buffer with EN (AND)	BN2U	3 mA	26 (1)
	BN4U	3 mA 50 kΩ Pull-down	26 (1)
	BN2C	6 mA	26 (1)
	BN4C	6 mA 50 kΩ Pull-down	26 (1)
	BN23	9 mA	26 (1)
	BN43	9 mA 50 kΩ Pull-down	26 (1)
	BN21	12 mA	26 (1)
	BN41	12 mA 50 kΩ Pull-down	26 (1)
	BN25	18 mA	28 (1)
	BN45	18 mA 50 kΩ Pull-down	28 (1)
	BN2F	24 mA	28 (1)
	BN4F	24 mA 50 kΩ Pull-down	28 (1)
I/O Buffer with EN (OR)	BN3U	3 mA	26 (1)
	BN5U	3 mA 50 kΩ Pull-down	26 (1)
	BN3C	6 mA	26 (1)
	BN5C	6 mA 50 kΩ Pull-down	26 (1)
	BN33	9 mA	26 (1)
	BN53	9 mA 50 kΩ Pull-down	26 (1)
	BN31	12 mA	26 (1)
	BN51	12 mA 50 kΩ Pull-down	26 (1)
	BN35	18 mA	28 (1)
	BN55	18 mA 50 kΩ Pull-down	28 (1)
	BN3F	24 mA	28 (1)
	BN5F	24 mA 50 kΩ Pull-down	28 (1)

E.1.2 5 V interface

Function	Block	Description	Cells (I/O)
Input Buffer	FIV1	–	7 (1)
	FDV1	50 kΩ Pull-down	7 (1)
	FIF1	Schmitt	11 (1)
	FDF1	Schmitt 50 kΩ Pull-down	11 (1)
	FIG1	Clock Driver	56 (1)
	FDG1	Clock Driver 50 kΩ Pull-down	56 (1)
Input Buffer with EN (AND)	FN1135	–	8 (1)
	FN2135	50 kΩ Pull-down	8 (1)
Input Buffer with EN (OR)	FN1335	–	8 (1)
	FN2335	50 kΩ Pull-down	8 (1)

Function		Block	Description	Cells (I/O)
CMOS Level	Output Buffer	FY09	3 mA	26 (1)
		FY04	6 mA	26 (1)
		FY01	9 mA	28 (1)
		FY02	12 mA	28 (1)
		FY03	18 mA	28 (1)
		FY06	24 mA	28 (1)
	Low-noise Output Buffer	FZ02	12 mA	28 (1)
		FZ03	18 mA	28 (1)
		FZ06	24 mA	28 (1)
	3-State Buffer	BD0T	3 mA	45 (1)
		BD0E	6 mA	45 (1)
		BD08	9 mA	47 (1)
		BD07	12 mA	47 (1)
		BD09	18 mA	47 (1)
		BD0H	24 mA	47 (1)
	Low-noise 3-State Buffer	BJ07	12 mA	40 (1)
		BJ09	18 mA	40 (1)
		BJ0H	24 mA	40 (1)
	I/O Buffer	BM0U	3 mA	52 (1)
		BM0C	6 mA	52 (1)
		BM03	9 mA	54 (1)
		BM01	12 mA	54 (1)
		BM05	18 mA	54 (1)
		BM0F	24 mA	54 (1)
	Low-noise I/O Buffer	BP01	12 mA	47 (1)
		BP05	18 mA	47 (1)
		BP0F	24 mA	47 (1)
	Schmitt I/O Buffer	BQIU	3 mA	56 (1)
		BQIC	6 mA	56 (1)
		BQI3	9 mA	58 (1)
		BQI1	12 mA	58 (1)
		BQI5	18 mA	58 (1)
		BQIF	24 mA	58 (1)
	Low-noise Schmitt I/O Buffer	BUI1	12 mA	51 (1)
		BUI5	18 mA	51 (1)
		BUIF	24 mA	51 (1)
	I/O Buffer with EN (AND)	BNXU35	3 mA	53 (1)
		BNXC35	6 mA	53 (1)
		BNX335	9 mA	55 (1)
		BNX135	12 mA	55 (1)
		BNX535	18 mA	55 (1)
		BNXF35	24 mA	55 (1)
	I/O Buffer with EN (OR)	BNMU35	3 mA	53 (1)
		BNMC35	6 mA	53 (1)
		BNM335	9 mA	55 (1)
		BNM135	12 mA	55 (1)
		BNM535	18 mA	55 (1)
		BNMF35	24 mA	55 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Output Buffer	FV0A	1 mA	8 (1)
		FV0B	2 mA	8 (1)
		FV09	3 mA	8 (1)
		FV04	6 mA	8 (1)
		FV01	9 mA	18 (1)
		FV02	12 mA	18 (1)
		FV03	18 mA	18 (1)
		FV06	24 mA	18 (1)
	Low-noise Output Buffer	FW02	12 mA	10 (1)
		FW03	18 mA	10 (1)
		FW06	24 mA	10 (1)
	3-State Buffer	BV0Q	1 mA	40 (1)
		BVDQ	1 mA 50 kΩ Pull-down	40 (1)
		BV0M	2 mA	40 (1)
		BVDM	2 mA 50 kΩ Pull-down	40 (1)
		BV0T	3 mA	40 (1)
		BVDT	3 mA 50 kΩ Pull-down	40 (1)
		BV0E	6 mA	40 (1)
		BVDE	6 mA 50 kΩ Pull-down	40 (1)
		BV08	9 mA	42 (1)
		BVD8	9 mA 50 kΩ Pull-down	42 (1)
		BV07	12 mA	42 (1)
		BVD7	12 mA 50 kΩ Pull-down	42 (1)
		BV09	18 mA	42 (1)
		BVD9	18 mA 50 kΩ Pull-down	42 (1)
		BV0H	24 mA	42 (1)
		BVDH	24 mA 50 kΩ Pull-down	42 (1)
	Low-noise 3-state Buffer	BY07	12 mA	28 (1)
		BYD7	12 mA 50 kΩ Pull-down	28 (1)
		BY09	18 mA	28 (1)
		BYD9	18 mA 50 kΩ Pull-down	28 (1)
		BY0H	24 mA	28 (1)
		BYDH	24 mA 50 kΩ Pull-down	28 (1)
	N-ch Open drain Buffer	EVTT	1 mA	8 (1)
		EVTK	2 mA	8 (1)
		EVTH	3 mA	8 (1)
		EVTJ	6 mA	8 (1)
		EVT1	9 mA	18 (1)
		EVT9	12 mA	18 (1)
		EVT5	18 mA	18 (1)
		EVTD	24 mA	18 (1)
	Low-noise N-ch Open drain Buffer	EYT9	12 mA	5 (1)
		EYT5	18 mA	5 (1)
		EYTD	24 mA	5 (1)

Function		Block	Description	Cells (I/O)
TTL Level	I/O Buffer	BW0X	1 mA	47 (1)
		BWDX	1 mA 50 kΩ Pull-down	47 (1)
		BW0K	2 mA	47 (1)
		BWDK	2 mA 50 kΩ Pull-down	47 (1)
		BW0U	3 mA	47 (1)
		BWDU	3 mA 50 kΩ Pull-down	47 (1)
		BW0C	6 mA	47 (1)
		BWDC	6 mA 50 kΩ Pull-down	47 (1)
		BW03	9 mA	49 (1)
		BWD3	9 mA 50 kΩ Pull-down	49 (1)
		BW01	12 mA	49 (1)
		BWD1	12 mA 50 kΩ Pull-down	49 (1)
		BW05	18 mA	49 (1)
		BWD5	18 mA 50 kΩ Pull-down	49 (1)
		BW0F	24 mA	49 (1)
		BWDF	24 mA 50 kΩ Pull-down	49 (1)
	Low-noise I/O Buffer	BX01	12 mA	35 (1)
		BXD1	12 mA 50 kΩ Pull-down	35 (1)
		BX05	18 mA	35 (1)
		BXD5	18 mA 50 kΩ Pull-down	35 (1)
		BX0F	24 mA	35 (1)
		BXDF	24 mA 50 kΩ Pull-down	35 (1)
	Schmitt I/O Buffer	BKIX	1 mA	51 (1)
		BKDX	1 mA 50 kΩ Pull-down	51 (1)
		BKIK	2 mA	51 (1)
		BKDK	2 mA 50 kΩ Pull-down	51 (1)
		BKIU	3 mA	51 (1)
		BKDU	3 mA 50 kΩ Pull-down	51 (1)
		BKIC	6 mA	51 (1)
		BKDC	6 mA 50 kΩ Pull-down	51 (1)
		BKI3	9 mA	53 (1)
		BKD3	9 mA 50 kΩ Pull-down	53 (1)
		BKI1	12 mA	53 (1)
		BKD1	12 mA 50 kΩ Pull-down	53 (1)
		BKI5	18 mA	53 (1)
		BKD5	18 mA 50 kΩ Pull-down	53 (1)
		BKIF	24 mA	53 (1)
		BKDF	24 mA 50 kΩ Pull-down	53 (1)
	Low-noise Schmitt I/O Buffer	BZI1	12 mA	39 (1)
		BZD1	12 mA 50 kΩ Pull-down	39 (1)
		BZI5	18 mA	39 (1)
		BZD5	18 mA 50 kΩ Pull-down	39 (1)
		BZIF	24 mA	39 (1)
		BZDF	24 mA 50 kΩ Pull-down	39 (1)

Function		Block	Description	Cells (I/O)
TTL Level	I/O Buffer with EN (AND)	BNXV35	3 mA	48 (1)
		BNYV35	3 mA 50 kΩ Pull-down	48 (1)
		BNXD35	6 mA	48 (1)
		BNYD35	6 mA 50 kΩ Pull-down	48 (1)
		BNX435	9 mA	50 (1)
		BNY435	9 mA 50 kΩ Pull-down	50 (1)
		BNX235	12 mA	50 (1)
		BNY235	12 mA 50 kΩ Pull-down	50 (1)
		BNX635	18 mA	50 (1)
		BNY635	18 mA 50 kΩ Pull-down	50 (1)
		BNXG35	24 mA	50 (1)
		BNYG35	24 mA 50 kΩ Pull-down	50 (1)
	I/O Buffer with EN (OR)	BNMV35	3 mA	48 (1)
		BNVV35	3 mA 50 kΩ Pull-down	48 (1)
		BNMD35	6 mA	48 (1)
		BNVD35	6 mA 50 kΩ Pull-down	48 (1)
		BNM435	9 mA	50 (1)
		BNV435	9 mA 50 kΩ Pull-down	50 (1)
		BNM235	12 mA	50 (1)
		BNV235	12 mA 50 kΩ Pull-down	50 (1)
		BNM635	18 mA	50 (1)
		BNV635	18 mA 50 kΩ Pull-down	50 (1)
		BNMG35	24 mA	50 (1)
		BNVG35	24 mA 50 kΩ Pull-down	50 (1)

E.1.3 5 V full-swing

Function		Block	Description	Cells (I/O)
CMOS Level	Input Buffer	FIV1AL	–	7 (1)
		FDV1AL	50 kΩ Pull-down	7 (1)
		FUV1AL	50 kΩ Pull-up	7 (1)
		FWV1AL	5 kΩ Pull-up	7 (1)
		FIF1AL	Schmitt	7 (1)
		FDF1AL	Schmitt, 50 kΩ Pull-down	7 (1)
		FUF1AL	Schmitt, 50 kΩ Pull-up	7 (1)
		FWF1AL	Schmitt, 5 kΩ Pull-up	7 (1)
	Input Buffer with Failsafe	FIC1AL	–	7 (1)
		FDC1AL	50 kΩ Pull-down	7 (1)
		FII1AL	Schmitt	7 (1)
		FDI1AL	Schmitt, 50 kΩ Pull-down	7 (1)
	Input Buffer with CTL (OR)	FIVAAL	–	7 (1)
	Input Buffer with Failsafe, CTL (OR)	FICAAL	–	7 (1)
		FDCAAL	(OR) FDCAAL 50 kΩ Pull-down	7 (1)

Function		Block	Description	Cells (I/O)
CMOS Level	Output Buffer	FV0AAL	1 mA	8 (1)
		FV0BAL	2 mA	8 (1)
		FV09AL	3 mA	8 (1)
		FV04AL	6 mA	8 (1)
		FV01AL	9 mA	8 (1)
		FV02AL	12 mA	8 (1)
		FV03AL	18 mA	8 (1)
	Output Buffer Low-noise	FW09AL	3 mA	8 (1)
		FW04AL	6 mA	8 (1)
		FW02AL	12 mA	8 (1)
		FW03AL	18 mA	8 (1)
	3-state Output Buffer	BV0QAL	1 mA	18 (1)
		BVDQAL	1 mA, 50 kΩ Pull-down	18 (1)
		BVUQAL	1 mA, 50 kΩ Pull-up	18 (1)
		BVWQAL	1 mA[Note], 5 kΩ Pull-up	18 (1)
		BV0MAL	2 mA	18 (1)
		BVDMAL	2 mA, 50 kΩ Pull-down	18 (1)
		BVUMAL	2 mA, 50 kΩ Pull-up	18 (1)
		BVWMAL	2 mA[Note], 5 kΩ Pull-up	18 (1)
		BV0TAL	3 mA	18 (1)
		BVDTAL	3 mA, 50 kΩ Pull-down	18 (1)
		BVUTAL	3 mA, 50 kΩ Pull-up	18 (1)
		BVWTAL	3 mA[Note], 5 kΩ Pull-up	18 (1)
		BV0EAL	6 mA	18 (1)
		BVDEAL	6 mA, 50 kΩ Pull-down	18 (1)
		BVUEAL	6 mA, 50 kΩ Pull-up	18 (1)
		BVWEAL	6 mA, 5 kΩ Pull-up	18 (1)
		BV08AL	9 mA	18 (1)
		BVD8AL	9 mA, 50 kΩ Pull-down	18 (1)
		BVU8AL	9 mA, 50 kΩ Pull-up	18 (1)
		BVW8AL	9 mA, 5 kΩ Pull-up	18 (1)
		BV07AL	12 mA	18 (1)
		BVD7AL	12 mA, 50 kΩ Pull-down	18 (1)
		BVU7AL	12 mA, 50 kΩ Pull-up	18 (1)
		BVW7AL	12 mA, 5 kΩ Pull-up	18 (1)
		BV09AL	18 mA	18 (1)
		BVD9AL	18 mA, 50 kΩ Pull-down	18 (1)
		BVU9AL	18 mA, 50 kΩ Pull-up	18 (1)
		BVW9AL	18 mA, 5 kΩ Pull-up	18 (1)

Note This block can not output the current value as is written in the list because of the pull-up resistor.

Function		Block	Description	Cells (I/O)
CMOS Level	3-state Output Buffer, Low-noise	BY0TAL	3 mA	18 (1)
		BYDTAL	3 mA, 50 kΩ Pull-down	18 (1)
		BYUTAL	3 mA, 50 kΩ Pull-up	18 (1)
		BYWTAL	3 mA[Note], 5 kΩ Pull-up	18 (1)
		BY0EAL	6 mA	18 (1)
		BYDEAL	6 mA, 50 kΩ Pull-down	18 (1)
		BYUEAL	6 mA, 50 kΩ Pull-up	18 (1)
		BYWEAL	6 mA, 5 kΩ Pull-up	18 (1)
		BY07AL	12 mA	18 (1)
		BYD7AL	12 mA, 50 kΩ Pull-down	18 (1)
		BYU7AL	12 mA, 50 kΩ Pull-up	18 (1)
		BYW7AL	12 mA, 5 kΩ Pull-up	18 (1)
		BY09AL	18 mA	18 (1)
		BYD9AL	18 mA, 50 kΩ Pull-down	18 (1)
		BYU9AL	18 mA, 50 kΩ Pull-up	18 (1)
		BYW9AL	18 mA, 5 kΩ Pull-up	18 (1)
	I/O Buffer	BW0XAL	1 mA	25 (1)
		BWDXAL	1 mA, 50 kΩ Pull-down	25 (1)
		BWUXAL	1 mA, 50 kΩ Pull-up	25 (1)
		BWWXAL	1 mA[Note], 5 kΩ Pull-up	25 (1)
		BW0KAL	2 mA	25 (1)
		BWDKAL	2 mA, 50 kΩ Pull-down	25 (1)
		BWUKAL	2 mA, 50 kΩ Pull-up	25 (1)
		BWWKAL	2 mA[Note] 5 kΩ Pull-up	25 (1)
		BW0UAL	3 mA	25 (1)
		BWDUAL	3 mA, 50 kΩ Pull-down	25 (1)
		BWUUAL	3 mA, 50 kΩ Pull-up	25 (1)
		BWWUAL	3 mA[Note], 5 kΩ Pull-up	25 (1)
		BW0CAL	6 mA	25 (1)
		BWDCAL	6 mA, 50 kΩ Pull-down	25 (1)
		BWUCAL	6 mA, 50 kΩ Pull-up	25 (1)
		BWWCAL	6 mA, 5 kΩ Pull-up	25 (1)
		BW03AL	9 mA	25 (1)
		BWD3AL	9 mA, 50 kΩ Pull-down	25 (1)
		BWU3AL	9 mA, 50 kΩ Pull-up	25 (1)
		BWW3AL	9 mA, 5 kΩ Pull-up	25 (1)
		BW01AL	12 mA	25 (1)
		BWD1AL	12 mA, 50 kΩ Pull-down	25 (1)
		BWU1AL	12 mA, 50 kΩ Pull-up	25 (1)
		BWW1AL	12 mA, 5 kΩ Pull-up	25 (1)
		BW05AL	18 mA	25 (1)
		BWD5AL	18 mA, 50 kΩ Pull-down	25 (1)
		BWU5AL	18 mA, 50 kΩ Pull-up	25 (1)
		BWW5AL	18 mA, 5 kΩ Pull-up	25 (1)

Note This block can not output the current value as is written in the list because of the pull-up resistor.

Function		Block	Description	Cells (I/O)
CMOS Level	I/O Buffer Low-noise	BX01AL	12 mA	25 (1)
		BXD1AL	12 mA, 50 kΩ Pull-down	25 (1)
		BXU1AL	12 mA, 50 kΩ Pull-up	25 (1)
		BXW1AL	12 mA, 5 kΩ Pull-up	25 (1)
		BX05AL	18 mA	25 (1)
		BXD5AL	18 mA, 50 kΩ Pull-down	25 (1)
		BXU5AL	18 mA, 50 kΩ Pull-up	25 (1)
		BXW5AL	18 mA, 5 kΩ Pull-up	25 (1)
	I/O Buffer Schmitt in	BKIXAL	1 mA	25 (1)
		BKDXAL	1 mA, 50 kΩ Pull-down	25 (1)
		BKUXAL	1 mA, 50 kΩ Pull-up	25 (1)
		BKWXAL	1 mA[Note], 5 kΩ Pull-up	25 (1)
		BKIKAL	2 mA	25 (1)
		BKDKAL	2 mA, 50 kΩ Pull-down	25 (1)
		BKUKAL	2 mA, 50 kΩ Pull-up	25 (1)
		BKWKAL	2 mA[Note], 5 kΩ Pull-up	25 (1)
		BKIUAL	3 mA	25 (1)
		BKDUAL	3 mA, 50 kΩ Pull-down	25 (1)
		BKUUAL	3 mA, 50 kΩ Pull-up	25 (1)
		BKWUAL	3 mA[Note] 5 kΩ Pull-up	25 (1)
		BKICAL	6 mA	25 (1)
		BKDCAL	6 mA, 50 kΩ Pull-down	25 (1)
		BKUCAL	6 mA, 50 kΩ Pull-up	25 (1)
		BKWCAL	6 mA, 5 kΩ Pull-up	25 (1)
		BKI3AL	9 mA	25 (1)
		BKD3AL	9 mA, 50 kΩ Pull-down	25 (1)
		BKU3AL	9 mA, 50 kΩ Pull-up	25 (1)
		BKW3AL	9 mA, 5 kΩ Pull-up	25 (1)
		BKI1AL	12 mA	25 (1)
		BKD1AL	12 mA, 50 kΩ Pull-down	25 (1)
		BKU1AL	12 mA, 50 kΩ Pull-up	25 (1)
		BKW1AL	12 mA, 5 kΩ Pull-up	25 (1)
		BKI5AL	18 mA	25 (1)
		BKD5AL	18 mA, 50 kΩ Pull-down	25 (1)
		BKU5AL	18 mA, 50 kΩ Pull-up	25 (1)
		BKW5AL	18 mA, 5 kΩ Pull-up	25 (1)
	I/O Buffer Schmitt in, Low-noise	BZI1AL	12 mA	25 (1)
		BZD1AL	12 mA, 50 kΩ Pull-down	25 (1)
		BZU1AL	12 mA, 50 kΩ Pull-up	25 (1)
		BZW1AL	12 mA, 5 kΩ Pull-up	25 (1)
		BZI5AL	18 mA	25 (1)
		BZD5AL	18 mA, 50 kΩ Pull-down	25 (1)
		BZU5AL	18 mA, 50 kΩ Pull-up	25 (1)
		BZW5AL	18 mA, 5 kΩ Pull-up	25 (1)

Note This block can not output the current value as is written in the list because of the pull-up resistor.

Function		Block	Description	Cells (I/O)
CMOS Level	I/O Buffer with CTL (OR)	B20XAL	1 mA	25 (1)
		B20KAL	2 mA	25 (1)
		B20UAL	3 mA	25 (1)
		B20CAL	6 mA	25 (1)
		B203AL	9 mA	25 (1)
		B201AL	12 mA	25 (1)
		B205AL	18 mA	25 (1)
	N-ch Open Drain Output Buffer	EVTHAL	3 mA	8 (1)
		EVUHAL	3 mA, 50 kΩ Pull-up	8 (1)
		EVWHAL	3 mA[Note], 5 kΩ Pull-up	8 (1)
		EVTJAL	6 mA	8 (1)
		EVUJAL	6 mA, 50 kΩ Pull-up	8 (1)
		EVWJAL	6 mA, 5 kΩ Pull-up	8 (1)
		EVT1AL	9 mA	8 (1)
		EVT3AL	9 mA, 50 kΩ Pull-up	8 (1)
		EVW3AL	9 mA, 5 kΩ Pull-up	8 (1)
		EVT9AL	12 mA	8 (1)
		EVTBAL	12 mA, 50 kΩ Pull-up	8 (1)
		EVWBAL	12 mA, 5 kΩ Pull-up	8 (1)
		EVT5AL	18 mA	8 (1)
		EVT7AL	18 mA, 50 kΩ Pull-up	8 (1)
		EVW7AL	18 mA, 5 kΩ Pull-up	8 (1)
	N-ch Open Drain Output Buffer Low-noise	EYTJAL	6 mA	8 (1)
		EYUJAL	6 mA, 50 kΩ Pull-up	8 (1)
		EYWJAL	6 mA, 5 kΩ Pull-up	8 (1)
		EYT1AL	9 mA	8 (1)
		EYT3AL	9 mA, 50 kΩ Pull-up	8 (1)
		EYW3AL	9 mA, 5 kΩ Pull-up	8 (1)
		EYT9AL	12 mA	8 (1)
		EYTBAL	12 mA, 50 kΩ Pull-up	8 (1)
		EYWBAL	12 mA, 5 kΩ Pull-up	8 (1)
		EYT5AL	18 mA	8 (1)
		EYT7AL	18 mA, 50 kΩ Pull-up	8 (1)
		EYW7AL	18 mA, 5 kΩ Pull-up	8 (1)
TTL Level	Input Buffer	FI41AL	–	7 (1)
		FD41AL	50 kΩ Pull-down	7 (1)
		FU41AL	50 kΩ Pull-up	7 (1)
		FW41AL	5 kΩ Pull-up	7 (1)
		FIL1AL	Schmitt	7 (1)
		FDL1AL	Schmitt, 50 kΩ Pull-down	7 (1)
		FUL1AL	Schmitt, 50 kΩ Pull-up	7 (1)
		FWL1AL	Schmitt, 5 kΩ Pull-up	7 (1)
	Input Buffer with Failsafe	FI61AL	–	7 (1)
		FD61AL	50 kΩ Pull-down	7 (1)
		FIM1AL	Schmitt	7 (1)
		FDM1AL	Schmitt, 50 kΩ Pull-down	7 (1)

Note This block can not output the current value as is written in the list because of the pull-up resistor.

Function		Block	Description	Cells (I/O)
TTL Level	I/O Buffer	BV0XAL	1 mA	25 (1)
		BVDXAL	1 mA, 50 kΩ Pull-down	25 (1)
		BVUXAL	1 mA, 50 kΩ Pull-up	25 (1)
		BVWXAL	1 mA[Note], 5 kΩ Pull-up	25 (1)
		BV0KAL	2 mA	25 (1)
		BVDKAL	2 mA, 50 kΩ Pull-down	25 (1)
		BVUKAL	2 mA, 50 kΩ Pull-up	25 (1)
		BVWKAL	2 mA[Note], 5 kΩ Pull-up	25 (1)
		BV0UAL	3 mA	25 (1)
		BVDUAL	3 mA, 50 kΩ Pull-down	25 (1)
		BVUUAL	3 mA, 50 kΩ Pull-up	25 (1)
		BVWUAL	3 mA[Note], 5 kΩ Pull-up	25 (1)
		BV0CAL	6 mA	25 (1)
		BVDCAL	6 mA, 50 kΩ Pull-down	25 (1)
		BVUCAL	6 mA, 50 kΩ Pull-up	25 (1)
		BVWCAL	6 mA, 5 kΩ Pull-up	25 (1)
		BV03AL	9 mA	25 (1)
		BVD3AL	9 mA, 50 kΩ Pull-down	25 (1)
		BVU3AL	9 mA, 50 kΩ Pull-up	25 (1)
		BVW3AL	9 mA, 5 kΩ Pull-up	25 (1)
		BV01AL	12 mA	25 (1)
		BVD1AL	12 mA, 50 kΩ Pull-down	25 (1)
		BVU1AL	12 mA, 50 kΩ Pull-up	25 (1)
		BVW1AL	12 mA, 5 kΩ Pull-up	25 (1)
		BV05AL	18 mA	25 (1)
		BVD5AL	18 mA, 50 kΩ Pull-down	25 (1)
		BVU5AL	18 mA, 50 kΩ Pull-up	25 (1)
		BVW5AL	18 mA, 5 kΩ Pull-up	25 (1)
	I/O Buffer Low-noise	BY01AL	12 mA	25 (1)
		BYD1AL	12 mA, 50 kΩ Pull-down	25 (1)
		BYU1AL	12 mA, 50 kΩ Pull-up	25 (1)
		BYW1AL	12 mA, 5 kΩ Pull-up	25 (1)
		BY05AL	18 mA	25 (1)
		BYD5AL	18 mA, 50 kΩ Pull-down	25 (1)
		BYU5AL	18 mA, 50 kΩ Pull-up	25 (1)
		BYW5AL	18 mA, 5 kΩ Pull-up	25 (1)
	I/O Buffer Schmitt in	BIJXAL	1 mA	25 (1)
		BIVXAL	1 mA, 50 kΩ Pull-up	25 (1)
		BIJKAL	2 mA	25 (1)
		BIVKAL	2 mA, 50 kΩ Pull-up	25 (1)
	I/O Buffer Schmitt in, Low-noise	BJIUAL	3 mA	25 (1)
		BJUUAL	3 mA, 50 kΩ Pull-up	25 (1)
		BJICAL	6 mA	25 (1)
		BJUCAL	6 mA, 50 kΩ Pull-up	25 (1)

Note This block can not output the current value as is written in the list because of the pull-up resistor.

Function	Block	Description	Cells (I/O)
Special power supply	VDD4	Internal 3.3 V power supply (for power supply division)	–
	VDD4C	Internal 3.3 V power supply (for power supply division, when near to a corner block)	–
	VBLK2	I/O block 3.3 V power supply (for power supply division)	–
	VBLK3	3.3 V power supply (5 V full-swing buffer area)	–
	VBLK4	Internal 3.3 V power supply (for power supply division, 5 V full-swing buffer area)	–
	GBLK3	GND (5 V full-swing buffer area)	–
	VBLK52	5V power supply (5 V full-swing buffer area)	–
CUT sharing buffer	VBLK3CUT	CUT sharing V_{DD} (left side: 3.3 V, right side: 5 V)	–
	VBLK3FCUT	CUT sharing V_{DD} (left side: 5 V, right side: 3.3 V)	–
	GBLK3CUT	CUT sharing GND (left side: 3.3 V, right side: 5 V)	–
	GBLK3FCUT	CUT sharing GND (left side: 5 V, right side: 3.3 V)	–
	VBLKO5CUT	CUT sharing 5 V V_{DD} (left side: 3.3 V, right side: 5 V)	–
	VBLKO5FCUT	CUT sharing 5 V V_{DD} (left side: 5 V, right side: 3.3 V)	–

E.1.4 Oscillator

Function	Block	Description	Cells (I/O)
Oscillator Input Buffer	OSI1	–	0 (1)
Oscillator Input Buffer for Enable	OSI2	–	0 (1)
Oscillator Output Buffer (Internal Feedback Resistor)	OSO1	–	0 (1)
Oscillator Output Buffer (for OSF Type)	OSO3	–	0 (1)
Oscillator Output Buffer (for Enable Type)	OSO7	–	0 (1)
Oscillator Output Buffer (External Feedback Resistor)	OSO9	–	0 (1)
Feedback Resistor for Oscillator	OSF1	–	0 (1)
Feedback Resistor for Oscillator For Enable	OSF3	–	0 (1)

E.1.5 PCI

Function	Block	Description	Cells (I/O)
3V PCI Input Buffer	BP3I	–	7 (1)
3V PCI Output Buffer	BP3O	–	18 (1)
3V PCI 3-State Buffer	BP3T	–	20 (1)
3V PCI I/O Buffer	BP3B	–	27 (1)
5V PCI Input Buffer	BP5I	–	7 (1)
5V PCI Output Buffer	BP5O	–	18 (1)
5V PCI 3-State Buffer	BP5T	–	42 (1)
5V PCI I/O Buffer	BP5B	–	49 (1)

<R> E.1.6 High Speed Signal Transmission

Function	Block	Description	Cells (I/O)
3V GTL/GTL+/P-ECL Input Buffer for Enable Terminal	FIXA	-	56 (1)
	FUXA	50 kΩ Pull-up	56 (1)
5V GTL/GTL+/P-ECL Input Buffer for Enable Terminal	FIZA	-	56 (1)
GTL+ Input Buffer with EN	FIR2	-	19 (1)
GTL+ Input Buffer for Reference VOLTAGE	FIP2	-	0 (1)
GTL+ Output Buffer with ENB	ELTL	-	6 (1)
GTL+ I/O Buffer	BL0W	-	25 (1)

E.1.7 Digital PLL

Function	Block	Description	Cells (I/O)
3V Input Buffer Reference Clock	FI0P	–	7 (1)
5V Input Buffer Reference Clock	FI0Q	–	7 (1)
DPLL (Phase locked loop)	F9E4	–	3770 (–)
DPLL (Phase locked loop-Clock multiply)	F9H3	–	15840 (–)
DPLL (Phase locked loop-Clock multiply)	F9H2	–	9000 (–)

E.1.8 SSCG

Function	Block	Description	Cells (I/O)
SSCG	F9H4SSCG	–	17550 (–)

<R> **E.1.9 Analog PLL**

Function	Block	Description	Cells (I/O)
APLL (Phase locked loop-Clock multiply)	ABPLMWFB	-	16320 (2)
APLL (Phase locked loop-Clock multiply)	ADPLSHFB	-	5400 (2)
APLL (Phase locked loop-Clock multiply)	ADPLSMFB	-	5400 (2)
APLL (Phase locked loop-Clock multiply)	ACPLSLFB	-	5400 (2)

<R> **E.1.10 Power on Reset**

Function	Block	Description	Cells (I/O)
Power on Reset	ABPORPFB	-	2940 (1)

E.2 Function Block

E.2.1 Level generator

Function	Block	Description	Cells (I/O)
H,L Level Generator	F091	–	1 (–)

E.2.2 Inverter, buffer, CTS driver, delay gate

Function	Block	Description	Cells (I/O)
Inverter	L101	Single Out (Low Power)	1 (–)
	F101	Single Out	1 (–)
	F102	Single Out (X2 Drive)	2 (–)
	F143K	Single Out (X3 Drive)	3 (–)
	F144K	Single Out (X4 Drive)	4 (–)
	F145K	Single Out (X5 Drive)	5 (–)
	F146K	Single Out (X6 Drive)	6 (–)
	F148K	Single Out (X8 Drive)	12 (–)
	F148P	Single Out (X8 Drive)	8 (–)
	F148BR	Single Out (X8 Drive)	12 (–)
	F14AK	Single Out (X12 Drive)	21 (–)
Buffer	L111	Single Out (Low Power)	1 (–)
	F111	Single Out	2 (–)
	F112	Single Out (X2 Drive)	3 (–)
	F153K	Single Out (X3 Drive)	4 (–)
	F154K	Single Out (X4 Drive)	5 (–)
	F158K	Single Out (X8 Drive)	11 (–)
	F158BR	Single Out (X8 Drive)	11 (–)
	F15AK	Single Out (X12 Drive)	20 (–)
CTS Driver (Inverter Type)	FC42	Single type	132 (–)
	FC82	Single type (X2 Drive)	396 (–)
	FC44	Double type	340 (–)
	FC84	Double type (X2 Drive)	1020 (–)
CTS Driver (Buffer Type)	FC52	Single type	100 (–)
	FC92	Single type (X2 Drive)	143 (–)
	FC53	Standard type	1905 (–)
	FC93	Standard type (X2 Drive)	1727 (–)
	FC54	Double type	36200 (–)
	FC94	Double type (X2 Drive)	20735 (–)
Delay Gate	F131	–	6 (–)
	F132	–	10 (–)
	F137	–	18 (–)
	F138	–	34 (–)

E.2.3 OR (NOR), AND (NAND)

Function	Block	Description	Cells (I/O)
2-Input NOR	L202	(Low Power)	1 (–)
	F202	–	2 (–)
	F222	(X2 Drive)	4 (–)
	F282	(X4 Drive)	6 (–)
	F2C2K	(X8 Drive)	12 (–)
	L202N1	1-Input Inverter (Low Power)	2 (–)
	F202N1	1-Input Inverter	3 (–)
	F222N1	1-Input Inverter (X2 Drive)	5 (–)
	F282N1	1-Input Inverter (X4 Drive)	7 (–)
3-Input NOR	F203	–	3 (–)
	F223	(X2 Drive)	6 (–)
	F2C3	(X4 Drive)	9 (–)
	F2C3NS	(X4 Drive)	12 (–)
	F203N1	1-Input Inverter	4 (–)
	F223N1	1-Input Inverter (X2 Drive)	7 (–)
	F2C3N1	1-Input Inverter (X4 Drive)	10 (–)
	F2C3N1S	1-Input Inverter (X4 Drive)	14 (–)
	F203N2	2-Input Inverter	4 (–)
	F223N2	2-Input Inverter (X2 Drive)	7 (–)
	F2C3N2	2-Input Inverter (X4 Drive)	9 (–)
	F2C3N2S	2-Input Inverter (X4 Drive)	12 (–)
4-Input NOR	L204	(Low Power)	4 (–)
	F204	–	4 (–)
	F224	(X2 Drive)	8 (–)
	L204N1	1-Input Inverter (Low Power)	4 (–)
	F204N1	1-Input Inverter	5 (–)
	F224N1	1-Input Inverter (X2 Drive)	9 (–)
	L204N2	2-Input Inverter (Low Power)	5 (–)
	F204N2	2-Input Inverter	5 (–)
	F224N2	2-Input Inverter (X2 Drive)	9 (–)
5-Input NOR	L205	(Low Power)	4 (–)
	F205	–	5 (–)
	F225	(X2 Drive)	6 (–)
	L205N1	1-Input Inverter (Low Power)	5 (–)
	F205N1	1-Input Inverter	6 (–)
	F225N1	1-Input Inverter (X2 Drive)	6 (–)
	L205N2	2-Input Inverter (Low Power)	5 (–)
	F205N2	2-Input Inverter	6 (–)
	F225N2	2-Input Inverter (X2 Drive)	7 (–)
	L205N3	3-Input Inverter (Low Power)	6 (–)
	F205N3	3-Input Inverter	7 (–)
	F225N3	3-Input Inverter (X2 Drive)	7 (–)

Function	Block	Description	Cells (I/O)
6-Input NOR	F206	–	5 (–)
	F226	(X2 Drive)	6 (–)
	L206N1	1-Input Inverter (Low Power)	5 (–)
	F206N1	1-Input Inverter	6 (–)
	F226N1	1-Input Inverter (X2 Drive)	7 (–)
	F206N2	2-Input Inverter	6 (–)
	F226N2	2-Input Inverter (X2 Drive)	7 (–)
	L206N3	3-Input Inverter (Low Power)	6 (–)
	F206N3	3-Input Inverter	7 (–)
	F226N3	3-Input Inverter (X2 Drive)	8 (–)
8-Input NOR	L208	(Low Power)	7 (–)
	F208	–	7 (–)
	F228	(X2 Drive)	8 (–)
	L208N1	1-Input Inverter (Low Power)	8 (–)
	F208N1	1-Input Inverter	8 (–)
	F228N1	1-Input Inverter (X2 Drive)	9 (–)
	L208N2	2-Input Inverter (Low Power)	8 (–)
	F208N2	2-Input Inverter	8 (–)
	F228N2	2-Input Inverter (X2 Drive)	9 (–)
	L208N3	3-Input Inverter (Low Power)	9 (–)
	F208N3	3-Input Inverter	9 (–)
	F228N3	3-Input Inverter (X2 Drive)	10 (–)
	L208N4	4-Input Inverter (Low Power)	9 (–)
	F208N4	4-Input Inverter	9 (–)
	F228N4	4-Input Inverter (X2 Drive)	10 (–)
2-Input OR	L212	(Low Power)	2 (–)
	F212	–	2 (–)
	F232	(X2 Drive)	3 (–)
	F252	(X4 Drive)	6 (–)
	F232NS	(X2 Drive)	4 (–)
	F2D2	(X4 Drive)	7 (–)
3-Input OR	L213	(Low Power)	2 (–)
	F213	–	3 (–)
	F233	(X2 Drive)	4 (–)
	F233NS	(X2 Drive)	5 (–)
	F2D3	(X4 Drive)	9 (–)
4-Input OR	L214	(Low Power)	3 (–)
	F214	–	3 (–)
	F234	(X2 Drive)	4 (–)
	L214N1	1-Input Inverter (Low Power)	3 (–)
	F214N1	1-Input Inverter	4 (–)
	F234N1	1-Input Inverter (X2 Drive)	5 (–)
5-Input OR	L215	(Low Power)	4 (–)
	F215	–	5 (–)
	F235	(X2 Drive)	7 (–)
	L215N1	1-Input Inverter (Low Power)	4 (–)
	F215N1	1-Input Inverter	5 (–)
	F235N1	1-Input Inverter (X2 Drive)	8 (–)

Function	Block	Description	Cells (I/O)
6-Input OR	L216	(Low Power)	4 (–)
	F216	–	5 (–)
	F236	(X2 Drive)	7 (–)
	L216N1	1-Input Inverter (Low Power)	5 (–)
	F216N1	1-Input Inverter	6 (–)
	F236N1	1-Input Inverter (X2 Drive)	8 (–)
	L216N2	2-Input Inverter (Low Power)	5 (–)
	F216N2	2-Input Inverter	6 (–)
	F236N2	2-Input Inverter (X2 Drive)	8 (–)
8-Input OR	L218	(Low Power)	6 (–)
	F218	–	8 (–)
	F238	(X2 Drive)	9 (–)
	L218N1	1-Input Inverter (Low Power)	7 (–)
	F218N1	1-Input Inverter	9 (–)
	F238N1	1-Input Inverter (X2 Drive)	10 (–)
	L218N2	2-Input Inverter (Low Power)	7 (–)
	F218N2	2-Input Inverter	9 (–)
	F238N2	2-Input Inverter (X2 Drive)	10 (–)
	L218N3	3-Input Inverter (Low Power)	8 (–)
	F218N3	3-Input Inverter	10 (–)
	F238N3	3-Input Inverter (X2 Drive)	11 (–)
2-Input NAND	L302	(Low Power)	1 (–)
	F302	–	2 (–)
	F322	(X2 Drive)	4 (–)
	F382	(X4 Drive)	6 (–)
	F3C2K	(X8 Drive)	12 (–)
	F382NS	(X4 Drive)	8 (–)
	L302N1	1-Input Inverter (Low Power)	2 (–)
	F302N1	1-Input Inverter	3 (–)
	F322N1	1-Input Inverter (X2 Drive)	5 (–)
	F382N1	1-Input Inverter (X4 Drive)	7 (–)
	F382N1S	1-Input Inverter (X4 Drive)	10 (–)
3-Input NAND	L303	(Low Power)	2 (–)
	F303	–	3 (–)
	F323	(X2 Drive)	6 (–)
	F3C3	(X4 Drive)	9 (–)
	F3C3NS	(X4 Drive)	12 (–)
	L303N1	1-Input Inverter (Low Power)	2 (–)
	F303N1	1-Input Inverter	4 (–)
	F323N1	1-Input Inverter (X2 Drive)	7 (–)
	F3C3N1	1-Input Inverter (X4 Drive)	10 (–)
	F3C3N1S	1-Input Inverter (X4 Drive)	14 (–)
	L303N2	2-Input Inverter (Low Power)	3 (–)
	F303N2	2-Input Inverter	4 (–)
	F323N2	2-Input Inverter (X2 Drive)	7 (–)
	F3C3N2	2-Input Inverter (X4 Drive)	10 (–)
	F3C3N2S	2-Input Inverter (X4 Drive)	16 (–)

Function	Block	Description	Cells (I/O)
4-Input NAND	L304	(Low Power)	2 (–)
	F304	–	4 (–)
	F324	(X2 Drive)	8 (–)
	F3C4	(X4 Drive)	10 (–)
	F3C4NS	(X4 Drive)	16 (–)
	L304N1	1-Input Inverter (Low Power)	3 (–)
	F304N1	1-Input Inverter	5 (–)
	F324N1	1-Input Inverter (X2 Drive)	9 (–)
	F3C4N1	1-Input Inverter (X4 Drive)	11 (–)
	F3C4N1S	1-Input Inverter (X4 Drive)	18 (–)
	L304N2	2-Input Inverter (Low Power)	3 (–)
	F304N2	2-Input Inverter	5 (–)
	F324N2	2-Input Inverter (X2 Drive)	9 (–)
	F3C4N2	2-Input Inverter (X4 Drive)	11 (–)
	F3C4N2S	2-Input Inverter (X4 Drive)	20 (–)
5-Input NAND	L305	(Low Power)	4 (–)
	F305	–	5 (–)
	F325	(X2 Drive)	6 (–)
	L305N1	1-Input Inverter (Low Power)	5 (–)
	F305N1	1-Input Inverter	6 (–)
	F325N1	1-Input Inverter (X2 Drive)	6 (–)
	L305N2	2-Input Inverter (Low Power)	5 (–)
	F305N2	2-Input Inverter	6 (–)
	F325N2	2-Input Inverter (X2 Drive)	7 (–)
	L305N3	3-Input Inverter (Low Power)	6 (–)
	F305N3	3-Input Inverter	7 (–)
	F325N3	3-Input Inverter (X2 Drive)	7 (–)
6-Input NAND	L306	(Low Power)	5 (–)
	F306	–	5 (–)
	F326	(X2 Drive)	6 (–)
	L306N1	1-Input Inverter (Low Power)	5 (–)
	F306N1	1-Input Inverter	6 (–)
	F326N1	1-Input Inverter (X2 Drive)	7 (–)
	L306N2	2-Input Inverter (Low Power)	6 (–)
	F306N2	2-Input Inverter	6 (–)
	F326N2	2-Input Inverter (X2 Drive)	7 (–)
	L306N3	3-Input Inverter (Low Power)	6 (–)
	F306N3	3-Input Inverter	7 (–)
	F326N3	3-Input Inverter (X2 Drive)	8 (–)
8-Input NAND	F308	–	6 (–)
	F328	(X2 Drive)	7 (–)
	L308N1	1-Input Inverter (Low Power)	6 (–)
	F308N1	1-Input Inverter	7 (–)
	F328N1	1-Input Inverter (X2 Drive)	8 (–)
	F308N2	2-Input Inverter	7 (–)
	F328N2	2-Input Inverter (X2 Drive)	8 (–)
	L308N3	3-Input Inverter (Low Power)	7 (–)
	F308N3	3-Input Inverter	8 (–)
	F328N3	3-Input Inverter (X2 Drive)	9 (–)
	F308N4	4-Input Inverter	8 (–)
	F328N4	4-Input Inverter (X2 Drive)	9 (–)

Function	Block	Description	Cells (I/O)
2-Input AND	L312	(Low Power)	2 (–)
	F312	–	2 (–)
	F332	(X2 Drive)	3 (–)
	F352	(X4 Drive)	6 (–)
	F3D2	(X8 Drive)	16 (–)
	F332NS	(X2 Drive)	4 (–)
	F352NS	(X4 Drive)	7 (–)
3-Input AND	L313	(Low Power)	2 (–)
	F313	–	3 (–)
	F333	(X2 Drive)	4 (–)
	F3D3	(X4 Drive)	9 (–)
	F333NS	(X2 Drive)	5 (–)
4-Input AND	L314	(Low Power)	3 (–)
	F314	–	3 (–)
	F334	(X2 Drive)	4 (–)
	F3D4	(X4 Drive)	10 (–)
	F334NS	(X2 Drive)	6 (–)
	L314N1	1-Input Inverter (Low Power)	3 (–)
	F314N1	1-Input Inverter	4 (–)
	F334N1	1-Input Inverter (X2 Drive)	5 (–)
5-Input AND	L315	(Low Power)	4 (–)
	F315	–	5 (–)
	F335	(X2 Drive)	7 (–)
	L315N1	1-Input Inverter (Low Power)	4 (–)
	F315N1	1-Input Inverter	5 (–)
	F335N1	1-Input Inverter (X2 Drive)	7 (–)
6-Input AND	L316	(Low Power)	4 (–)
	F316	–	5 (–)
	F336	(X2 Drive)	7 (–)
	L316N1	1-Input Inverter (Low Power)	5 (–)
	F316N1	1-Input Inverter	6 (–)
	F336N1	1-Input Inverter (X2 Drive)	8 (–)
	L316N2	2-Input Inverter (Low Power)	5 (–)
	F316N2	2-Input Inverter	6 (–)
	F336N2	2-Input Inverter (X2 Drive)	8 (–)
8-Input AND	L318	(Low Power)	5 (–)
	F318	–	6 (–)
	F338	(X2 Drive)	8 (–)
	L318N1	1-Input Inverter (Low Power)	6 (–)
	F318N1	1-Input Inverter	7 (–)
	F338N1	1-Input Inverter (X2 Drive)	9 (–)
	L318N2	2-Input Inverter (Low Power)	6 (–)
	F318N2	2-Input Inverter	7 (–)
	F338N2	2-Input Inverter (X2 Drive)	9 (–)
	L318N3	3-Input Inverter (Low Power)	7 (–)
	F318N3	3-Input Inverter	8 (–)
	F338N3	3-Input Inverter (X2 Drive)	10 (–)

E.2.4 AND-NOR

Function	Block	Description	Cells (I/O)
1-2-Input AND-NOR	L421	(Low Power)	2 (–)
	F421	–	3 (–)
	F421NP	(X2 Drive)	5 (–)
	F421T	(X4 Drive)	12 (–)
	L421NA	(Low Power)	2 (–)
	F421NA	–	4 (–)
	F421NAP	(X2 Drive)	5 (–)
	F421NAT	(X4 Drive)	14 (–)
	L421NB	(Low Power)	3 (–)
	F421NB	–	4 (–)
	F421NBP	(X2 Drive)	6 (–)
	F421NBT	(X4 Drive)	16 (–)
	L421NC	(Low Power)	3 (–)
	F421NC	–	5 (–)
	F421NCP	(X2 Drive)	6 (–)
	F421NCT	(X4 Drive)	9 (–)
	L421ND	(Low Power)	2 (–)
	F421ND	–	4 (–)
	F421NDP	(X2 Drive)	5 (–)
	F421NDT	(X4 Drive)	14 (–)
	L421NE	(Low Power)	3 (–)
	F421NE	–	4 (–)
	F421NEP	(X2 Drive)	6 (–)
	F421NET	(X4 Drive)	16 (–)
1-1-2-Input AND-NOR	F422	–	4 (–)
	F422NP	(X2 Drive)	5 (–)
	F422T	(X4 Drive)	16 (–)
	F422NA	–	5 (–)
	F422NAP	(X2 Drive)	6 (–)
	F422NAT	(X4 Drive)	18 (–)
	F422NB	–	5 (–)
	F422NBP	(X2 Drive)	6 (–)
	F422NBT	(X4 Drive)	16 (–)
	F422NC	–	6 (–)
	F422NCP	(X2 Drive)	7 (–)
	F422NCT	(X4 Drive)	18 (–)
	F422ND	–	6 (–)
	F422NDP	(X2 Drive)	7 (–)
	F422NDT	(X4 Drive)	10 (–)
	F422NE	–	5 (–)
	F422NEP	(X2 Drive)	6 (–)
	F422NET	(X4 Drive)	20 (–)
	F422NF	–	6 (–)
	F422NFP	(X2 Drive)	7 (–)
	F422NFT	(X4 Drive)	22 (–)
	F422NG	–	5 (–)
	F422NGP	(X2 Drive)	6 (–)
	F422NGT	(X4 Drive)	18 (–)
	F422NH	–	5 (–)
	F422NHP	(X2 Drive)	6 (–)
	F422NHT	(X4 Drive)	20 (–)

Function	Block	Description	Cells (I/O)
1-3-Input AND-NOR	L423	(Low Power)	2 (–)
	F423	–	4 (–)
	F423NP	(X2 Drive)	5 (–)
	F423T	(X4 Drive)	16 (–)
	L423NA	(Low Power)	3 (–)
	F423NA	–	5 (–)
	F423NAP	(X2 Drive)	6 (–)
	F423NAT	(X4 Drive)	18 (–)
	L423NB	(Low Power)	3 (–)
	F423NB	–	5 (–)
	F423NBP	(X2 Drive)	6 (–)
	F423NBT	(X4 Drive)	20 (–)
	L423NC	(Low Power)	4 (–)
	F423NC	–	6 (–)
	F423NCP	(X2 Drive)	7 (–)
	F423NCT	(X4 Drive)	22 (–)
	L423ND	(Low Power)	4 (–)
	F423ND	–	6 (–)
	F423NDP	(X2 Drive)	7 (–)
	F423NDT	(X4 Drive)	10 (–)
	L423NE	(Low Power)	3 (–)
	F423NE	–	5 (–)
	F423NEP	(X2 Drive)	6 (–)
	F423NET	(X4 Drive)	18 (–)
	L423NF	(Low Power)	3 (–)
	F423NF	–	5 (–)
	F423NFP	(X2 Drive)	6 (–)
	F423NFT	(X4 Drive)	20 (–)
	L423NG	(Low Power)	4 (–)
	F423NG	–	6 (–)
	F423NGP	(X2 Drive)	7 (–)
	F423NGT	(X4 Drive)	22 (–)
2-2-Input AND-NOR	L424	(Low Power)	2 (–)
	F424	–	4 (–)
	F424NP	(X2 Drive)	5 (–)
	F424T	(X4 Drive)	16 (–)
	L424NA	(Low Power)	3 (–)
	F424NA	–	5 (–)
	F424NAP	(X2 Drive)	6 (–)
	F424NAT	(X4 Drive)	18 (–)
	L424NB	(Low Power)	3 (–)
	F424NB	–	5 (–)
	F424NBP	(X2 Drive)	6 (–)
	F424NBT	(X4 Drive)	20 (–)
	L424NC	(Low Power)	4 (–)
	F424NC	–	6 (–)
	F424NCP	(X2 Drive)	7 (–)
	F424NCT	(X4 Drive)	10 (–)
	L424ND	(Low Power)	3 (–)
	F424ND	–	5 (–)
	F424NDP	(X2 Drive)	6 (–)

Function	Block	Description	Cells (I/O)
2-2-Input AND-NOR	F424NDT	(X4 Drive)	20 (–)
	L424NE	(Low Power)	4 (–)
	F424NE	–	6 (–)
	F424NEP	(X2 Drive)	7 (–)
	F424NET	(X4 Drive)	22 (–)
2-2-2-Input AND-NOR	L425	(Low Power)	5 (–)
	F425	–	6 (–)
	F425NP	(X2 Drive)	6 (–)
	F425T	(X4 Drive)	24 (–)
3-3-Input AND-NOR	L426	(Low Power)	5 (–)
	F426	–	6 (–)
	F426NP	(X2 Drive)	6 (–)
	F426T	(X4 Drive)	24 (–)
2-3-Input AND-NOR	L427	(Low Power)	4 (–)
	F427	–	5 (–)
	F427NP	(X2 Drive)	6 (–)
	F427T	(X4 Drive)	20 (–)
1-2-2-Input AND-NOR	F428	–	5 (–)
	F428NP	(X2 Drive)	6 (–)
	F428T	(X4 Drive)	20 (–)
2-2-2-2-Input AND-NOR	L429	(Low Power)	6 (–)
	F429	–	6 (–)
	F429NP	(X2 Drive)	7 (–)
1-4-Input AND-NOR	L440	(Low Power)	3 (–)
	F440	–	5 (–)
	F440NP	(X2 Drive)	6 (–)
1-5-Input AND-NOR	L441	(Low Power)	5 (–)
	F441	–	7 (–)
	F441NP	(X2 Drive)	8 (–)
4-4-Input AND-NOR	L442	(Low Power)	6 (–)
	F442	–	11 (–)
	F442NP	(X2 Drive)	12 (–)
4-4-4-Input AND-NOR	L444	(Low Power)	8 (–)
	F444	–	8 (–)
	F444NP	(X2 Drive)	9 (–)
2-4-Input AND-NOR	L445	(Low Power)	5 (–)
	F445	–	6 (–)
	F445NP	(X2 Drive)	6 (–)
1-1-1-2-Input AND-NOR	L446	(Low Power)	4 (–)
	F446	–	5 (–)
	F446NP	(X2 Drive)	6 (–)
1-1-1-3-Input AND-NOR	L447	(Low Power)	5 (–)
	F447	–	5 (–)
	F447NP	(X2 Drive)	6 (–)
1-1-2-2-Input AND-NOR	L448	(Low Power)	5 (–)
	F448	–	5 (–)
	F448NP	(X2 Drive)	6 (–)
3-3-3-3-Input AND-NOR	F449	–	8 (–)
	F449NP	(X2 Drive)	9 (–)

Function	Block	Description	Cells (I/O)
3-3-3-Input AND-NOR	L460	(Low Power)	6 (–)
	F460	–	7 (–)
	F460NP	(X2 Drive)	8 (–)
1-2-3-Input AND-NOR	L462	(Low Power)	5 (–)
	F462	–	6 (–)
	F462NP	(X2 Drive)	6 (–)
1-1-3-Input AND-NOR	L463	(Low Power)	4 (–)
	F463	–	5 (–)
	F463NP	(X2 Drive)	6 (–)
1-1-4-Input AND-NOR	L464	(Low Power)	5 (–)
	F464	–	5 (–)
	F464NP	(X2 Drive)	6 (–)
1-1-1-1-2-Input AND-NOR	F465	–	5 (–)
	F465NP	(X2 Drive)	6 (–)
4-4-4-4-Input AND-NOR	F466	–	10 (–)
	F466NP	(X2 Drive)	11 (–)

E.2.5 OR-NAND

Function	Block	Description	Cells (I/O)
1-4-Input OR-NAND	L430	(Low Power)	4 (–)
	F430	–	5 (–)
	F430NP	(X2 Drive)	7 (–)
1-2-Input OR-NAND	L431	(Low Power)	2 (–)
	F431	–	3 (–)
	F431NP	(X2 Drive)	5 (–)
	F431T	(X4 Drive)	12 (–)
	L431NA	(Low Power)	2 (–)
	F431NA	–	4 (–)
	F431NAP	(X2 Drive)	5 (–)
	F431NAT	(X4 Drive)	14 (–)
	L431NB	(Low Power)	3 (–)
	F431NB	–	4 (–)
	F431NBP	(X2 Drive)	6 (–)
	F431NBT	(X4 Drive)	16 (–)
	L431NC	(Low Power)	3 (–)
	F431NC	–	5 (–)
	F431NCP	(X2 Drive)	6 (–)
	F431NCT	(X4 Drive)	14 (–)
	L431ND	(Low Power)	2 (–)
	F431ND	–	4 (–)
	F431NDP	(X2 Drive)	5 (–)
	F431NDT	(X4 Drive)	14 (–)
	L431NE	(Low Power)	3 (–)
	F431NE	–	4 (–)
	F431NEP	(X2 Drive)	6 (–)
	F431NET	(X4 Drive)	12 (–)

Function	Block	Description	Cells (I/O)
1-1-2-Input OR-NAND	L432	(Low Power)	2 (–)
	F432	–	4 (–)
	F432NP	(X2 Drive)	5 (–)
	F432T	(X4 Drive)	16 (–)
	L432NA	(Low Power)	3 (–)
	F432NA	–	5 (–)
	F432NAP	(X2 Drive)	6 (–)
	F432NAT	(X4 Drive)	18 (–)
	L432NB	(Low Power)	3 (–)
	F432NB	–	5 (–)
	F432NBP	(X2 Drive)	6 (–)
	F432NBT	(X4 Drive)	20 (–)
	L432NC	(Low Power)	4 (–)
	F432NC	–	6 (–)
	F432NCP	(X2 Drive)	7 (–)
	F432NCT	(X4 Drive)	22 (–)
	L432ND	(Low Power)	4 (–)
	F432ND	–	6 (–)
	F432NDP	(X2 Drive)	7 (–)
	F432NDT	(X4 Drive)	20 (–)
	L432NE	(Low Power)	3 (–)
	F432NE	–	5 (–)
	F432NEP	(X2 Drive)	6 (–)
	F432NET	(X4 Drive)	20 (–)
	L432NF	(Low Power)	4 (–)
	F432NF	–	6 (–)
	F432NFP	(X2 Drive)	7 (–)
	F432NFT	(X4 Drive)	18 (–)
	L432NG	(Low Power)	3 (–)
	F432NG	–	5 (–)
	F432NGP	(X2 Drive)	6 (–)
	F432NGT	(X4 Drive)	18 (–)
	L432NH	(Low Power)	3 (–)
	F432NH	–	5 (–)
	F432NHP	(X2 Drive)	6 (–)
	F432NHT	(X4 Drive)	16 (–)
1-3-Input OR-NAND	F433	–	4 (–)
	F433NP	(X2 Drive)	5 (–)
	F433T	(X4 Drive)	16 (–)
	F433NA	–	5 (–)
	F433NAP	(X2 Drive)	6 (–)
	F433NAT	(X4 Drive)	18 (–)
	F433NB	–	5 (–)
	F433NBP	(X2 Drive)	6 (–)
	F433NBT	(X4 Drive)	20 (–)
	F433NC	–	6 (–)
	F433NCP	(X2 Drive)	7 (–)
	F433NCT	(X4 Drive)	18 (–)
	F433ND	–	6 (–)
	F433NDP	(X2 Drive)	7 (–)

Function	Block	Description	Cells (I/O)
1-3-Input OR-NAND	F433NDT	(X4 Drive)	16 (–)
	F433NE	–	5 (–)
	F433NEP	(X2 Drive)	6 (–)
	F433NET	(X4 Drive)	18 (–)
	F433NF	–	5 (–)
	F433NFP	(X2 Drive)	6 (–)
	F433NFT	(X4 Drive)	16 (–)
	F433NG	–	6 (–)
	F433NGP	(X2 Drive)	7 (–)
	F433NGT	(X4 Drive)	14 (–)
2-2-Input OR-NAND	L434	(Low Power)	2 (–)
	F434	–	4 (–)
	F434NP	(X2 Drive)	5 (–)
	F434T	(X4 Drive)	16 (–)
	L434NA	(Low Power)	3 (–)
	F434NA	–	5 (–)
	F434NAP	(X2 Drive)	6 (–)
	F434NAT	(X4 Drive)	18 (–)
	L434NB	(Low Power)	3 (–)
	F434NB	–	5 (–)
	F434NBP	(X2 Drive)	6 (–)
	F434NBT	(X4 Drive)	16 (–)
	L434NC	(Low Power)	4 (–)
	F434NC	–	6 (–)
	F434NCP	(X2 Drive)	7 (–)
	F434NCT	(X4 Drive)	16 (–)
	L434ND	(Low Power)	3 (–)
	F434ND	–	5 (–)
	F434NDP	(X2 Drive)	6 (–)
	F434NDT	(X4 Drive)	20 (–)
	L434NE	(Low Power)	4 (–)
	F434NE	–	6 (–)
	F434NEP	(X2 Drive)	7 (–)
	F434NET	(X4 Drive)	18 (–)
2-3-Input OR-NAND	L435	(Low Power)	4 (–)
	F435	–	8 (–)
	F435NP	(X2 Drive)	9 (–)
	F435T	(X4 Drive)	20 (–)
3-3-Input OR-NAND	L436	(Low Power)	5 (–)
	F436	–	9 (–)
	F436NP	(X2 Drive)	10 (–)
	F436T	(X4 Drive)	24 (–)
1-2-2-Input OR-NAND	F437	–	5 (–)
	F437NP	(X2 Drive)	6 (–)
	F437T	(X4 Drive)	20 (–)
2-2-2-Input OR-NAND	L438	(Low Power)	5 (–)
	F438	–	6 (–)
	F438NP	(X2 Drive)	6 (–)
1-5-Input OR-NAND	L439	(Low Power)	5 (–)
	F439	–	6 (–)
	F439NP	(X2 Drive)	8 (–)

Function	Block	Description	Cells (I/O)
2-4-Input OR-NAND	L450	(Low Power)	5 (–)
	F450	–	6 (–)
	F450NP	(X2 Drive)	8 (–)
4-4-Input OR-NAND	L451	(Low Power)	7 (–)
	F451	–	8 (–)
	F451NP	(X2 Drive)	10 (–)
1-1-3-Input OR-NAND	L452	(Low Power)	4 (–)
	F452	–	5 (–)
	F452NP	(X2 Drive)	6 (–)
1-1-4-Input OR-NAND	L453	(Low Power)	5 (–)
	F453	–	6 (–)
	F453NP	(X2 Drive)	9 (–)
2-2-2-2-Input OR-NAND	F454	–	13 (–)
	F454NP	(X2 Drive)	14 (–)
4-4-4-Input OR-NAND	F457	–	10 (–)
	F457NP	(X2 Drive)	11 (–)
1-1-1-2-Input OR-NAND	L458	(Low Power)	4 (–)
	F458	–	5 (–)
	F458NP	(X2 Drive)	5 (–)
1-1-1-3-Input OR-NAND	L459	(Low Power)	5 (–)
	F459	–	5 (–)
	F459NP	(X2 Drive)	6 (–)
1-1-1-1-2-Input OR-NAND	F490	–	5 (–)
	F490NP	(X2 Drive)	6 (–)
1-2-3-Input OR-NAND	L491	(Low Power)	5 (–)
	F491	–	5 (–)
	F491NP	(X2 Drive)	6 (–)
3-3-3-Input OR-NAND	L493	(Low Power)	6 (–)
	F493	–	7 (–)
	F493NP	(X2 Drive)	8 (–)
1-1-2-2-Input OR-NAND	L495	(Low Power)	5 (–)
	F495	–	6 (–)
	F495NP	(X2 Drive)	6 (–)
3-3-3-3-Input OR-NAND	F496	–	8 (–)
	F496NP	(X2 Drive)	9 (–)
4-4-4-4-Input OR-NAND	F498	–	14 (–)
	F498NP	(X2 Drive)	16 (–)

E.2.6 Exclusive OR, Exclusive NOR

Function	Block	Description	Cells (I/O)
2-Input Exclusive OR	L511	(Low Power)	3 (–)
	F511	–	4 (–)
	F511NP	(X2 Drive)	5 (–)
	F511NT	(X4 Drive)	11 (–)
3-Input Exclusive OR	L516	(Low Power)	6 (–)
	F516	–	9 (–)
	F516NP	(X2 Drive)	9 (–)
	F516NT	(X4 Drive)	14 (–)
2-Input Exclusive NOR	L512	(Low Power)	3 (–)
	F512	–	4 (–)
	F512NP	(X2 Drive)	5 (–)
	F512NT	(X4 Drive)	11 (–)
3-Input Exclusive NOR	L517	(Low Power)	6 (–)
	F517	–	8 (–)
	F517NT	(X4 Drive)	14 (–)

E.2.7 Adder, 3-state buffer, decoder, multiplexer, generator

Function	Block	Description	Cells (I/O)
1-Bit Full Adder	F521	–	9 (–)
	F521NP	(X2 Drive)	19 (–)
	F521NT	(X4 Drive)	26 (–)
4-Bit Full Adder	F523	–	34 (–)
1-Bit Carry Save Adder	F528	–	11 (–)
3-State Buffer	L531	with EN (Low Power)	4 (–)
	F531	with EN	5 (–)
	F533	with EN (X2 Drive)	7 (–)
	F53F	with EN (X4 Drive)	11 (–)
	F53H	with EN (X8 Drive)	24 (–)
	L532	with ENB (Low Power)	4 (–)
	F532	with ENB	5 (–)
	F534	with ENB (X2 Drive)	7 (–)
	F53G	with ENB (X4 Drive)	11 (–)
	F53K	with ENB (X8 Drive)	24 (–)
	F541	Inverter with EN	3 (–)
	F543	Inverter with EN (X2 Drive)	4 (–)
	F54F	Inverter with EN (X4 Drive)	6 (–)
	F54H	Inverter with EN (X8 Drive)	25 (–)
	F542	Inverter with ENB	3 (–)
	F544	Inverter with ENB (X2 Drive)	4 (–)
	F54G	Inverter with ENB (X4 Drive)	6 (–)
	F54K	Inverter with ENB (X8 Drive)	25 (–)
2 to 4 Decoder	L560	Positive Out (Low Power)	6 (–)
	F560	Positive Out	10 (–)
	F560NP	Positive Out (X2 Drive)	18 (–)
	L561	Negative Out (Low Power)	6 (–)
	F561	Negative Out	10 (–)
	F561NP	Negative Out (X2 Drive)	18 (–)
	L981	Negative Out with ENB (Low Power)	8 (–)
	F981	Negative Out with ENB	13 (–)

Function	Block	Description	Cells (I/O)
3 to 8 Decoder	L982	Negative Out with ENB (Low Power)	17 (–)
	F982	Negative Out with ENB	26 (–)
2 to 1 Multiplexer (Positive Out)	F565	–	4 (–)
	F56C	(X2 Drive)	7 (–)
	F565NT	(X4 Drive)	11 (–)
	L571	with ENB (Low Power)	4 (–)
	F571	with ENB	6 (–)
	F571NP	with ENB (X2 Drive)	8 (–)
2 to 1 Multiplexer (Negative Out)	F57B	–	5 (–)
	F57BNP	(X2 Drive)	6 (–)
4 to 1 Multiplexer (Positive Out)	F564	–	8 (–)
	F56B	(X2 Drive)	11 (–)
	F564NT	(X4 Drive)	16 (–)
	F570	with ENB	10 (–)
	F570NP	with ENB (X2 Drive)	12 (–)
	F56BNSP	High-speed (X2 Drive)	15 (–)
	F564NST	High-speed (X4 Drive)	21 (–)
4 to 1 Multiplexer (Negative Out)	F57A	–	10 (–)
	F57ANP	(X2 Drive)	10 (–)
8 to 1 Multiplexer (Positive Out)	F563	–	17 (–)
	F563NP	(X2 Drive)	20 (–)
	F563NT	(X4 Drive)	25 (–)
	F569	with ENB	19 (–)
	F569NP	with ENB (X2 Drive)	21 (–)
	F563NSP	High-speed (X2 Drive)	31 (–)
	F563NST	High-speed (X4 Drive)	41 (–)
8 to 1 Multiplexer (Negative Out)	F579	–	17 (–)
Quad 2 to 1 Multiplexer (Positive Out)	F552	–	13 (–)
Quad 2 to 1 Multiplexer (Negative Out)	F555	–	9 (–)
	L572	with ENB (Low Power)	10 (–)
	F572	with ENB	14 (–)
Quad 4 to 1 Multiplexer (Positive Out)	F551	–	27 (–)
Quad 4 to 1 Multiplexer (Negative Out)	F554	–	29 (–)
Quad 8 to 1 Multiplexer (Positive Out)	F550	–	64 (–)
Quad 8 to 1 Multiplexer (Negative Out)	F553	–	64 (–)
8-Bit Odd Parity Generator	F581	–	19 (–)
	F581NSP	(X2 Drive)	21 (–)
8-Bit Even Parity Generator	F582	–	19 (–)
	F582NSP	(X2 Drive)	21 (–)

E.2.8 RS-F/F, RS-latch

Function	Block	Description	Cells (I/O)
RS-Latch	F595	–	5 (–)
RS-F/F with R,S	F596	–	11 (–)

E.2.9 D-latch

Function	Block	Description	Cells (I/O)
D-Latch	F601NL	(Low Power)	5 (–)
	F601	–	6 (–)
	F601NP	(X2 Drive)	8 (–)
	L601	Q Out (Low Power)	4 (–)
	F601NQL	Q Out (Low Power)	4 (–)
	F601NQ	Q Out	5 (–)
	F601NQP	Q Out (X2 Drive)	6 (–)
	F601NBL	QB Out (Low Power)	4 (–)
	F601NB	QB Out	5 (–)
	F601NBP	QB Out (X2 Drive)	6 (–)
D-Latch (High Speed)	F6R1	–	6 (–)
D-Latch with R	F602NL	(Low Power)	6 (–)
	F602	–	6 (–)
	F602NP	(X2 Drive)	9 (–)
	L602	Q Out (Low Power)	5 (–)
	F602NQL	Q Out (Low Power)	5 (–)
	F602NQ	Q Out	6 (–)
	F602NQP	Q Out (X2 Drive)	7 (–)
	F602NB	QB Out	6 (–)
	F602NBP	QB Out (X2 Drive)	7 (–)
D-Latch with R (High Speed)	F6R2	–	7 (–)
D-Latch with RB	F603NL	(Low Power)	5 (–)
	F603	–	7 (–)
	F603NP	(X2 Drive)	8 (–)
	L603	Q Out (Low Power)	4 (–)
	F603NQ	Q Out	5 (–)
	F603NQP	Q Out (X2 Drive)	6 (–)
	F603NBL	QB Out (Low Power)	5 (–)
	F603NB	QB Out	6 (–)
	F603NBP	QB Out (X2 Drive)	7 (–)
D-Latch with RB (High Speed)	F6R5	–	6 (–)
D-Latch with SB	F60KNL	(Low Power)	6 (–)
	F60K	–	7 (–)
	F60KNP	(X2 Drive)	9 (–)
	F60KNQL	Q Out (Low Power)	5 (–)
	F60KNQ	Q Out	6 (–)
	F60KNQP	Q Out (X2 Drive)	7 (–)
	F60KNB	QB Out	5 (–)
	F60KNBP	QB Out (X2 Drive)	6 (–)
D-Latch with RB,SB	F60JNL	(Low Power)	6 (–)
	F60J	–	7 (–)
	F60JNP	(X2 Drive)	9 (–)
	F60JNQ	Q Out	6 (–)
	F60JNQP	Q Out (X2 Drive)	7 (–)
	F60JNBL	QB Out (Low Power)	5 (–)
	F60JNB	QB Out	6 (–)
	F60JNBP	QB Out (X2 Drive)	7 (–)

Function	Block	Description	Cells (I/O)
D-Latch (GB)	F604NL	(Low Power)	5 (–)
	F604	–	6 (–)
	F604NP	(X2 Drive)	8 (–)
	L604	Q Out (Low Power)	4 (–)
	F604NQL	Q Out (Low Power)	4 (–)
	F604NQ	Q Out	5 (–)
	F604NQP	Q Out (X2 Drive)	6 (–)
	F604NBL	QB Out (Low Power)	4 (–)
	F604NB	QB Out	5 (–)
	F604NBP	QB Out (X2 Drive)	6 (–)
D-Latch (GB) (High Speed)	F6R8	–	6 (–)
D-Latch (GB) with RB	F605NL	(Low Power)	5 (–)
	F605	–	7 (–)
	F605NP	(X2 Drive)	8 (–)
	L605	Q Out (Low Power)	4 (–)
	F605NQ	Q Out	5 (–)
	F605NQP	Q Out (X2 Drive)	6 (–)
	F605NBL	QB Out (Low Power)	5 (–)
	F605NB	QB Out	6 (–)
	F605NBP	QB Out (X2 Drive)	7 (–)
D-Latch (GB) with RB (High Speed)	F6R9	–	6 (–)

E.2.10 D-F/F

Function	Block	Description	Cells (I/O)
D-F/F	F611	–	8 (–)
	F611NT	(X4 Drive)	14 (–)
	L611	Q Out (Low Power)	6 (–)
	F611NQT	Q Out (X4 Drive)	10 (–)
	F611NBT	QB Out (X4 Drive)	10 (–)
	F641NL	(Low Power)	7 (–)
	F641	–	8 (–)
	F641NP	(X2 Drive)	10 (–)
	F641NQL	Q Out (Low Power)	7 (–)
	F641NQ	Q Out	7 (–)
	F641NQP	Q Out (X2 Drive)	8 (–)
	F641NBL	QB Out (Low Power)	7 (–)
	F641NB	QB Out	7 (–)
	F641NBP	QB Out (X2 Drive)	8 (–)
D-F/F with R	F612NQT	Q Out (X4 Drive)	11 (–)
	F612NBT	QB Out (X4 Drive)	12 (–)
	F642NL	(Low Power)	8 (–)
	F642	–	9 (–)
	F642NP	(X2 Drive)	11 (–)
	F642NQL	Q Out (Low Power)	8 (–)
	F642NQ	Q Out	8 (–)
	F642NQP	Q Out (X2 Drive)	9 (–)
	F642NBL	QB Out (Low Power)	8 (–)
	F642NB	QB Out	8 (–)
	F642NBP	QB Out (X2 Drive)	9 (–)

Function	Block	Description	Cells (I/O)
D-F/F with S	F613NQT	Q Out (X4 Drive)	12 (–)
	F613NBT	QB Out (X4 Drive)	11 (–)
	F643NL	(Low Power)	8 (–)
	F643	–	9 (–)
	F643NP	(X2 Drive)	11 (–)
	F643NQL	Q Out (Low Power)	7 (–)
	F643NQ	Q Out	8 (–)
	F643NQP	Q Out (X2 Drive)	9 (–)
	F643NBL	QB Out (Low Power)	7 (–)
	F643NB	QB Out	8 (–)
	F643NBP	QB Out (X2 Drive)	9 (–)
D-F/F with R,S	F614	–	10 (–)
	L614	Q Out (Low Power)	8 (–)
	F614NQT	Q Out (X4 Drive)	13 (–)
	F614NBT	QB Out (X4 Drive)	13 (–)
	F644NL	(Low Power)	9 (–)
	F644	–	10 (–)
	F644NP	(X2 Drive)	12 (–)
	F644NQL	Q Out (Low Power)	9 (–)
	F644NQ	Q Out	9 (–)
	F644NQP	Q Out (X2 Drive)	10 (–)
	F644NBL	QB Out (Low Power)	9 (–)
	F644NB	QB Out	9 (–)
	F644NBP	QB Out (X2 Drive)	10 (–)
D-F/F with RB	F615NL	(Low Power)	8 (–)
	F615	–	9 (–)
	F615NP	(X2 Drive)	11 (–)
	F615NT	(X4 Drive)	16 (–)
	F615NQL	Q Out (Low Power)	8 (–)
	F615NQ	Q Out	8 (–)
	F615NQP	Q Out (X2 Drive)	9 (–)
	F615NQT	Q Out (X4 Drive)	12 (–)
	F615NBL	QB Out (Low Power)	8 (–)
	F615NB	QB Out	8 (–)
	F615NBP	QB Out (X2 Drive)	9 (–)
	F615NBT	QB Out (X4 Drive)	11 (–)
D-F/F with SB	F616NL	(Low Power)	8 (–)
	F616	–	9 (–)
	F616NP	(X2 Drive)	11 (–)
	F616NQL	Q Out (Low Power)	8 (–)
	F616NQ	Q Out	8 (–)
	F616NQP	Q Out (X2 Drive)	9 (–)
	F616NQT	Q Out (X4 Drive)	11 (–)
	F616NBL	QB Out (Low Power)	8 (–)
	F616NB	QB Out	8 (–)
	F616NBP	QB Out (X2 Drive)	9 (–)
	F616NBT	QB Out (X4 Drive)	12 (–)

Function	Block	Description	Cells (I/O)
D-F/F with RB, SB	F617	–	10 (–)
	L617	Q Out (Low Power)	8 (–)
	F617NQT	Q Out (X4 Drive)	13 (–)
	F617NBT	QB Out (X4 Drive)	13 (–)
	F647NL	(Low Power)	9 (–)
	F647	–	10 (–)
	F647NP	(X2 Drive)	12 (–)
	F647NQL	Q Out (Low Power)	9 (–)
	F647NQ	Q Out	9 (–)
	F647NQP	Q Out (X2 Drive)	10 (–)
	F647NBL	QB Out (Low Power)	9 (–)
	F647NB	QB Out	9 (–)
	F647NBP	QB Out (X2 Drive)	10 (–)
D-F/F (CB)	F631	–	8 (–)
	F631NT	(X4 Drive)	14 (–)
	L631	Q Out (Low Power)	6 (–)
	F631NQT	Q Out (X4 Drive)	10 (–)
	F631NBT	QB Out (X4 Drive)	10 (–)
	F661NL	(Low Power)	7 (–)
	F661	–	8 (–)
	F661NP	(X2 Drive)	10 (–)
	F661NQL	Q Out (Low Power)	7 (–)
	F661NQ	Q Out	7 (–)
	F661NQP	Q Out (X2 Drive)	8 (–)
	F661NBL	QB Out (Low Power)	7 (–)
	F661NB	QB Out	7 (–)
	F661NBP	QB Out (X2 Drive)	8 (–)
D-F/F (CB) with RB	F635NQT	Q Out (X4 Drive)	12 (–)
	F635NBT	QB Out (X4 Drive)	11 (–)
	F665NL	(Low Power)	8 (–)
	F665	–	9 (–)
	F665NP	(X2 Drive)	11 (–)
	F665NQL	Q Out (Low Power)	7 (–)
	F665NQ	Q Out	8 (–)
	F665NQP	Q Out (X2 Drive)	9 (–)
	F665NBL	QB Out (Low Power)	7 (–)
	F665NB	QB Out	8 (–)
	F665NBP	QB Out (X2 Drive)	9 (–)
D-F/F (CB) with SB	F636NQT	Q Out (X4 Drive)	11 (–)
	F636NBT	QB Out (X4 Drive)	12 (–)
	F666NL	(Low Power)	8 (–)
	F666	–	9 (–)
	F666NP	(X2 Drive)	11 (–)
	F666NQL	Q Out (Low Power)	7 (–)
	F666NQ	Q Out	8 (–)
	F666NQP	Q Out (X2 Drive)	9 (–)
	F666NBL	QB Out (Low Power)	7 (–)
	F666NB	QB Out	8 (–)
	F666NBP	QB Out (X2 Drive)	9 (–)

Function	Block	Description	Cells (I/O)
D-F/F (CB) with RB, SB	F637	–	10 (–)
	L637	Q Out (Low Power)	8 (–)
	F637NQT	Q Out (X4 Drive)	13 (–)
	F637NBT	QB Out (X4 Drive)	13 (–)
	F667NL	(Low Power)	9 (–)
	F667	–	10 (–)
	F667NP	(X2 Drive)	12 (–)
	F667NQL	Q Out (Low Power)	9 (–)
	F667NQ	Q Out	9 (–)
	F667NQP	Q Out (X2 Drive)	10 (–)
	F667NBL	QB Out (Low Power)	9 (–)
	F667NB	QB Out	9 (–)
	F667NBP	QB Out (X2 Drive)	10 (–)
D-F/F with 2 to 1 Selector	F611ST	(X4 Drive)	17 (–)
	F611SQT	Q Out (X4 Drive)	13 (–)
	F611SBT	QB Out (X4 Drive)	13 (–)
	F641SL	(Low Power)	9 (–)
	F641S	–	10 (–)
	F641SP	(X2 Drive)	12 (–)
	F641SQ	Q Out	9 (–)
	F641SQP	Q Out (X2 Drive)	10 (–)
	F641SB	QB Out	9 (–)
	F641SBP	QB Out (X2 Drive)	10 (–)
D-F/F with R, 2 to 1 Selector	F612SQT	Q Out (X4 Drive)	14 (–)
	F612SBT	QB Out (X4 Drive)	14 (–)
	F642SL	(Low Power)	10 (–)
	F642S	–	11 (–)
	F642SP	(X2 Drive)	13 (–)
	F642SQ	Q Out	10 (–)
	F642SQP	Q Out (X2 Drive)	11 (–)
	F642SB	QB Out	10 (–)
	F642SBP	QB Out (X2 Drive)	11 (–)
D-F/F with S, 2 to 1 Selector	F613SQT	Q Out (X4 Drive)	14 (–)
	F613SBT	QB Out (X4 Drive)	14 (–)
	F643SL	(Low Power)	10 (–)
	F643S	–	11 (–)
	F643SP	(X2 Drive)	13 (–)
	F643SQ	Q Out	10 (–)
	F643SQP	Q Out (X2 Drive)	11 (–)
	F643SB	QB Out	10 (–)
	F643SBP	QB Out (X2 Drive)	11 (–)
D-F/F with R, S, 2 to 1 Selector	F614SQT	Q Out (X4 Drive)	15 (–)
	F614SBT	QB Out (X4 Drive)	15 (–)
	F644SL	(Low Power)	11 (–)
	F644S	–	12 (–)
	F644SP	(X2 Drive)	14 (–)
	F644SQ	Q Out	11 (–)
	F644SQP	Q Out (X2 Drive)	12 (–)
	F644SB	QB Out	11 (–)
	F644SBP	QB Out (X2 Drive)	12 (–)

Function	Block	Description	Cells (I/O)
D-F/F with RB, 2 to 1 Selector	F615SL	(Low Power)	10 (–)
	F615S	–	11 (–)
	F615SP	(X2 Drive)	13 (–)
	F615ST	(X4 Drive)	18 (–)
	F615SQ	Q Out	10 (–)
	F615SQP	Q Out (X2 Drive)	11 (–)
	F615SQT	Q Out (X4 Drive)	14 (–)
	F615SB	QB Out	10 (–)
	F615SBP	QB Out (X2 Drive)	11 (–)
	F615SBT	QB Out (X4 Drive)	14 (–)
D-F/F with SB,2 to 1 Selector	F616SL	(Low Power)	10 (–)
	F616S	–	11 (–)
	F616SP	(X2 Drive)	13 (–)
	F616SQ	Q Out	10 (–)
	F616SQP	Q Out (X2 Drive)	11 (–)
	F616SQT	Q Out (X4 Drive)	14 (–)
	F616SB	QB Out	10 (–)
	F616SBP	QB Out (X2 Drive)	11 (–)
	F616SBT	QB Out (X4 Drive)	14 (–)
D-F/F with RB, SB, 2 to 1 Selector	F617SQT	Q Out (X4 Drive)	15 (–)
	F617SBT	QB Out (X4 Drive)	15 (–)
	F647SL	(Low Power)	11 (–)
	F647S	–	12 (–)
	F647SP	(X2 Drive)	14 (–)
	F647SQ	Q Out	11 (–)
	F647SQP	Q Out (X2 Drive)	12 (–)
	F647SB	QB Out	11 (–)
	F647SBP	QB Out (X2 Drive)	12 (–)
D-F/F (CB) with 2 to 1 Selector	F631ST	(X4 Drive)	17 (–)
	F631SQT	Q Out (X4 Drive)	13 (–)
	F631SBT	QB Out (X4 Drive)	13 (–)
	F661SL	(Low Power)	9 (–)
	F661S	–	10 (–)
	F661SP	(X2 Drive)	12 (–)
	F661SQ	Q Out	9 (–)
	F661SQP	Q Out (X2 Drive)	10 (–)
	F661SB	QB Out	9 (–)
	F661SBP	QB Out (X2 Drive)	10 (–)
D-F/F (CB) with RB, 2 to 1 Selector	F635ST	(X4 Drive)	18 (–)
	F635SQT	Q Out (X4 Drive)	14 (–)
	F635SBT	QB Out (X4 Drive)	14 (–)
	F665SL	(Low Power)	10 (–)
	F665S	–	11 (–)
	F665SP	(X2 Drive)	13 (–)
	F665SQ	Q Out	10 (–)
	F665SQP	Q Out (X2 Drive)	11 (–)
	F665SB	QB Out	10 (–)
	F665SBP	QB Out (X2 Drive)	11 (–)

Function	Block	Description	Cells (I/O)
D-F/F (CB) with SB, 2 to 1 Selector	F636ST	(X4 Drive)	18 (–)
	F636SBT	QB Out (X4 Drive)	14 (–)
	F666SL	(Low Power)	10 (–)
	F666S	–	11 (–)
	F666SP	(X2 Drive)	13 (–)
	F666SQ	Q Out	10 (–)
	F666SQP	Q Out (X2 Drive)	11 (–)
	F666SB	QB Out	10 (–)
	F666SBP	QB Out (X2 Drive)	11 (–)
D-F/F (CB) with RB, SB, 2 to 1 Selector	F637SQT	Q Out (X4 Drive)	15 (–)
	F637SBT	QB Out (X4 Drive)	15 (–)
	F667SL	(Low Power)	11 (–)
	F667S	–	12 (–)
	F667SP	(X2 Drive)	14 (–)
	F667SQ	Q Out	11 (–)
	F667SQP	Q Out (X2 Drive)	12 (–)
	F667SB	QB Out	11 (–)
	F667SBP	QB Out (X2 Drive)	12 (–)
D-F/F with Hold	F641HL	(Low Power)	9 (–)
	F641H	–	10 (–)
	F641HP	(X2 Drive)	12 (–)
	F641HQ	Q Out	9 (–)
	F641HQP	Q Out (X2 Drive)	10 (–)
	F641HB	QB Out	9 (–)
	F641HBP	QB Out (X2 Drive)	10 (–)
D-F/F with RB, Hold	F615HL	(Low Power)	10 (–)
	F615H	–	11 (–)
	F615HP	(X2 Drive)	13 (–)
	F615HQ	Q Out	10 (–)
	F615HQP	Q Out (X2 Drive)	11 (–)
	F615HB	QB Out	10 (–)
	F615HBP	QB Out (X2 Drive)	11 (–)
D-F/F with SB, Hold	F616HL	(Low Power)	10 (–)
	F616H	–	11 (–)
	F616HP	(X2 Drive)	13 (–)
	F616HQ	Q Out	10 (–)
	F616HQP	Q Out (X2 Drive)	11 (–)
	F616HB	QB Out	10 (–)
	F616HBP	QB Out (X2 Drive)	11 (–)
D-F/F with RB, SB, Hold	F647HL	(Low Power)	11 (–)
	F647H	–	12 (–)
	F647HP	(X2 Drive)	14 (–)
	F647HQ	Q Out	11 (–)
	F647HQP	Q Out (X2 Drive)	12 (–)
	F647HB	QB Out	11 (–)
	F647HBP	QB Out (X2 Drive)	12 (–)
D-F/F (CB) with 2 to 1 Selector (2 CTRL), RB	F673	–	11 (–)
D-F/F (CB) with Hold, 2 to 1 Selector (2 CTRL), RB	F674	–	12 (–)

E.2.11 T-F/F, JK-F/F

Function	Block	Description	Cells (I/O)
T-F/F with R, S	F744NL	(Low Power)	8 (–)
	F744	–	9 (–)
	F714	–	9 (–)
	F744NP	(X2 Drive)	11 (–)
	L714	Q Out (Low Power)	8 (–)
	F744NQ	Q Out	8 (–)
	F744NQP	Q Out (X2 Drive)	9 (–)
T-F/F with RB	F745NL	(Low Power)	7 (–)
	F745	–	8 (–)
	F745NP	(X2 Drive)	10 (–)
	F745NQ	Q Out	7 (–)
	F745NQP	Q Out (X2 Drive)	8 (–)
T-F/F with RB, SB	F747NL	(Low Power)	8 (–)
	F747	–	9 (–)
	F717	–	9 (–)
	F747NP	(X2 Drive)	11 (–)
	L717	Q Out (Low Power)	8 (–)
	F747NQ	Q Out	8 (–)
	F747NQP	Q Out (X2 Drive)	9 (–)
T-F/F with Data-Hold R,S	F791	–	12 (–)
T-F/F (TB) with RB	F765NL	(Low Power)	7 (–)
	F765	–	8 (–)
	F765NP	(X2 Drive)	10 (–)
	F765NQ	Q Out	7 (–)
	F765NQP	Q Out (X2 Drive)	8 (–)
T-F/F (TB) with RB, SB	F767NL	(Low Power)	8 (–)
	F767	–	9 (–)
	F737	–	9 (–)
	F767NP	(X2 Drive)	11 (–)
	L737	Q Out (Low Power)	8 (–)
	F767NQ	Q Out	8 (–)
	F767NQP	Q Out (X2 Drive)	9 (–)
JK-F/F	F771NL	(Low Power)	9 (–)
	F771	–	10 (–)
	F771NP	(X2 Drive)	12 (–)
	F771NQL	Q Out (Low Power)	9 (–)
	F771NQ	Q Out	9 (–)
	F771NQP	Q Out (X2 Drive)	10 (–)
	F771NBL	QB Out (Low Power)	9 (–)
	F771NB	QB Out	9 (–)
	F771NBP	QB Out (X2 Drive)	10 (–)
JK-F/F (High Speed)	F7D1	–	10 (–)

Function	Block	Description	Cells (I/O)
JK-F/F with R, S	F774NL	(Low Power)	11 (–)
	F774	–	12 (–)
	F774NP	(X2 Drive)	14 (–)
	F774NQL	Q Out (Low Power)	11 (–)
	F774NQ	Q Out	11 (–)
	F774NQP	Q Out (X2 Drive)	12 (–)
	F774NBL	QB Out (Low Power)	11 (–)
	F774NB	QB Out	11 (–)
	F774NBP	QB Out (X2 Drive)	12 (–)
JK-F/F with RB	F775NL	(Low Power)	10 (–)
	F775	–	11 (–)
	F775NP	(X2 Drive)	13 (–)
	F775NQL	Q Out (Low Power)	10 (–)
	F775NQ	Q Out	10 (–)
	F775NQP	Q Out (X2 Drive)	11 (–)
	F775NBL	QB Out (Low Power)	10 (–)
	F775NB	QB Out	10 (–)
	F775NBP	QB Out (X2 Drive)	11 (–)
JK-F/F with SB	F776NL	(Low Power)	11 (–)
	F776	–	12 (–)
	F776NP	(X2 Drive)	14 (–)
	F776NQL	Q Out (Low Power)	11 (–)
	F776NQ	Q Out	11 (–)
	F776NQP	Q Out (X2 Drive)	12 (–)
	F776NBL	QB Out (Low Power)	11 (–)
	F776NB	QB Out	11 (–)
	F776NBP	QB Out (X2 Drive)	12 (–)
JK-F/F with RB, SB	F777NL	(Low Power)	11 (–)
	F777	–	12 (–)
	F777NP	(X2 Drive)	14 (–)
	F777NQL	Q Out (Low Power)	11 (–)
	F777NQ	Q Out	11 (–)
	F777NQP	Q Out (X2 Drive)	12 (–)
	F777NBL	QB Out (Low Power)	11 (–)
	F777NB	QB Out	11 (–)
	F777NBP	QB Out (X2 Drive)	12 (–)
JK-F/F (CB)	F781NL	(Low Power)	9 (–)
	F781	–	10 (–)
	F781NP	(X2 Drive)	12 (–)
	F781NQL	Q Out (Low Power)	9 (–)
	F781NQ	Q Out	9 (–)
	F781NQP	Q Out (X2 Drive)	10 (–)
	F781NBL	QB Out (Low Power)	9 (–)
	F781NB	QB Out	9 (–)
	F781NBP	QB Out (X2 Drive)	10 (–)
JK-F/F (CB) (High Speed)	F7E1	–	10 (–)

Function	Block	Description	Cells (I/O)
JK-F/F (CB) with RB, SB	F787NL	(Low Power)	11 (–)
	F787	–	12 (–)
	F787NP	(X2 Drive)	14 (–)
	F787NQL	Q Out (Low Power)	11 (–)
	F787NQ	Q Out	11 (–)
	F787NQP	Q Out (X2 Drive)	12 (–)
	F787NBL	QB Out (Low Power)	11 (–)
	F787NB	QB Out	11 (–)
	F787NBP	QB Out (X2 Drive)	12 (–)

E.2.12 Other block

Function	Block	Description	Cells (I/O)
4-Bit D-Latch	F901	–	20 (–)
	L901	Q Out (Low Power)	12 (–)
4-Bit D-Latch (High Speed)	F971	–	20 (–)
8-Bit D-Latch	F902	–	38 (–)
	L902	Q Out (Low Power)	22 (–)
8-Bit D-Latch (High Speed)	F972	–	38 (–)
4-Bit D-F/F	L924	Q Out (Low Power)	20 (–)
4-Bit Shift Register	L914	Q Out (Low Power)	20 (–)
4-Bit Magnitude Comparator	F985	–	32 (–)

E.3 Scan Path Block

E.3.1 Standard type

Function	Block	Description	Cells (I/O)
D-F/F with R,S,2 to 1 Selector	S000	–	12 (–)
D-F/F with 2 to 1 Selector	S001	(Low Power)	9 (–)
	S002	–	10 (–)
D-F/F with RB,2 to 1 Selector	S004	–	11 (–)
D-F/F with SB,2 to 1 Selector	S005	–	11 (–)
D-F/F with R,S,Hold,2 to 1 Selector	S050	–	14 (–)
D-F/F with Hold,2 to 1 Selector	S052	–	12 (–)
JK-F/F with R,S,D-F/F Function	S100	–	14 (–)
JK-F/F with D-F/F Function	S102	–	12 (–)
JK-F/F with R,S,Hold,D-F/F Function	S150	–	17 (–)
JK-F/F with Hold,D-F/F Function	S152	–	15 (–)
D-Latch with R,D-F/F Function	S201	–	12 (–)
D-Latch with D-F/F Function	S202	–	11 (–)
D-Latch with D-F/F Function (High Speed)	S204	–	11 (–)
D-Latch with R,Special Function,R	S301	–	8 (–)
D-Latch with Special Function	S302	–	7 (-)
D-Latch with Special Function (High Speed)	S303	–	7 (–)
2 to 1 Data Selector	S999	–	4 (–)

E.3.2 LSSD scan

Function	Block	Description	Cells (I/O)
Clocked LSSD D-Latch	SD601	–	10 (–)
	SD601NP	(X2 Drive)	13 (–)
Clocked LSSD D-Latch with R	SD602	–	11 (–)
	SD602NP	(X2 Drive)	14 (–)
Clocked LSSD D-Latch with RB	SD603	–	11 (–)
	SD603NP	(X2 Drive)	14 (–)
Clocked LSSD D-Latch (GB)	SD604	–	10 (–)
	SD604NP	(X2 Drive)	13 (–)
Clocked LSSD D-Latch (GB) with RB	SD605	–	11 (–)
	SD605NP	(X2 Drive)	14 (–)
Clocked LSSD D-F/F	SD611	–	12 (–)
	SD641	(X2 Drive)	15 (–)
	SD611T	(X4 Drive)	19 (–)
Clocked LSSD D-F/F with R, S	SD614	–	14 (–)
	SD644	(X2 Drive)	17 (–)
Clocked LSSD D-F/F with RB	SD615	–	13 (–)
	SD645	(X2 Drive)	16 (–)
Clocked LSSD D-F/F with SB	SD616	–	13 (–)
	SD646	(X2 Drive)	16 (–)
Clocked LSSD D-F/F with RB,SB	SD617	–	14 (–)
	SD647	(X2 Drive)	17 (–)
Clocked LSSD D-F/F (CB)	SD631	–	12 (–)
	SD661	(X2 Drive)	15 (–)
Clocked LSSD D-F/F (CB) with RB,SB	SD637	–	14 (–)
	SD667	(X2 Drive)	17 (–)

E.3.3 NEC scan

Function	Block	Description	Cells (I/O)
D-Latch	SE601	–	12 (–)
	SE601NP	(X2 Drive)	15 (–)
	SE601NQ	Q Out	11 (–)
	SE601NQP	Q Out (X2 Drive)	13 (–)
	SE601NB	QB Out	11 (–)
	SE601NBP	QB Out (X2 Drive)	13 (–)
D-Latch with R	SE602	–	13 (–)
	SE602NP	(X2 Drive)	16 (–)
	SE602NQ	Q Out	12 (–)
	SE602NQP	Q Out (X2 Drive)	14 (–)
	SE602NB	QB Out	12 (–)
	SE602NBP	QB Out (X2 Drive)	14 (–)
D-Latch with RB	SE603	–	13 (–)
	SE603NP	(X2 Drive)	16 (–)
	SE603NQ	Q Out	12 (–)
	SE603NQP	Q Out (X2 Drive)	14 (–)
	SE603NB	QB Out	12 (–)
	SE603NBP	QB Out (X2 Drive)	14 (–)
D-Latch(GB)	SE604	–	12 (–)
	SE604NP	(X2 Drive)	15 (–)
	SE604NQ	Q Out	11 (–)
	SE604NQP	Q Out (X2 Drive)	13 (–)
	SE604NB	QB Out	11 (–)
	SE604NBP	QB Out (X2 Drive)	13 (–)
D-Latch(GB) with RB	SE605	–	13 (–)
	SE605NP	(X2 Drive)	16 (–)
	SE605NQ	Q Out	12 (–)
	SE605NQP	Q Out (X2 Drive)	14 (–)
	SE605NB	QB Out	12 (–)
	SE605NBP	QB Out (X2 Drive)	14 (–)
D-F/F	SE611	–	11 (–)
	SE611NT	(X4 Drive)	18 (–)
	SE611NQT	Q Out (X4 Drive)	14 (–)
	SE611NBT	QB Out (X4 Drive)	14 (–)
	SE641	–	11 (–)
	SE641NP	(X2 Drive)	14 (–)
	SE641NQ	Q Out	10 (–)
	SE641NQP	Q Out (X2 Drive)	12 (–)
	SE641NB	QB Out	10 (–)
	SE641NBP	QB Out (X2 Drive)	12 (–)
D-F/F with R, S	SE614	–	13 (–)
	SE614NQT	Q Out (X4 Drive)	16 (–)
	SE614NBT	QB Out (X4 Drive)	16 (–)
	SE644	–	13 (–)
	SE644NP	(X2 Drive)	16 (–)
	SE644NQ	Q Out	12 (–)
	SE644NQP	Q Out (X2 Drive)	14 (–)
	SE644NB	QB Out	12 (–)
	SE644NBP	QB Out (X2 Drive)	14 (–)

Function	Block	Description	Cells (I/O)
D-F/F with RB	SE615	–	12 (–)
	SE615NQ	Q Out	11 (–)
	SE615NQT	Q Out (X4 Drive)	15 (–)
	SE615NB	QB Out	11 (–)
	SE615NBT	QB Out (X4 Drive)	15 (–)
	SE645NP	(X2 Drive)	15 (–)
	SE645NQP	Q Out (X2 Drive)	13 (–)
	SE645NBP	QB Out (X2 Drive)	13 (–)
D-F/F with SB	SE616	–	12 (–)
	SE616NQ	Q Out	11 (–)
	SE616NQT	Q Out (X4 Drive)	15 (–)
	SE616NB	QB Out	11 (–)
	SE616NBT	QB Out (X4 Drive)	15 (–)
	SE646NP	(X2 Drive)	15 (–)
	SE646NQP	Q Out (X2 Drive)	13 (–)
	SE646NBP	QB Out (X2 Drive)	13 (–)
D-F/F with RB, SB	SE617	–	13 (–)
	SE617NQT	Q Out (X4 Drive)	16 (–)
	SE617NBT	QB Out (X4 Drive)	16 (–)
	SE647	–	13 (–)
	SE647NP	(X2 Drive)	16 (–)
	SE647NQ	Q Out	12 (–)
	SE647NQP	Q Out (X2 Drive)	14 (–)
	SE647NB	QB Out	12 (–)
	SE647NBP	QB Out (X2 Drive)	14 (–)
D-F/F (CB)	SE631	–	11 (–)
	SE631NT	(X4 Drive)	18 (–)
	SE631NQT	Q Out (X4 Drive)	14 (–)
	SE631NBT	QB Out (X4 Drive)	14 (–)
	SE661	–	11 (–)
	SE661NP	(X2 Drive)	14 (–)
	SE661NQ	Q Out	10 (–)
	SE661NQP	Q Out (X2 Drive)	12 (–)
	SE661NB	QB Out	10 (–)
	SE661NBP	QB Out (X2 Drive)	12 (–)
D-F/F (CB) with RB, SB	SE637	–	13 (–)
	SE637NQT	Q Out (X4 Drive)	16 (–)
	SE637NBT	QB Out (X4 Drive)	16 (–)
	SE667	–	13 (–)
	SE667NP	(X2 Drive)	16 (–)
	SE667NQ	Q Out	12 (–)
	SE667NQP	Q Out (X2 Drive)	14 (–)
	SE667NB	QB Out	12 (–)
	SE667NBP	QB Out (X2 Drive)	14 (–)

E.3.4 Scan controller

Function	Block	Description	Cells (I/O)
Clock Distributor	SCD1	–	8 (–)
Clock Distributor with Test (Positive Clock)	SCDC	–	2 (–)
Clock Distributor with Test (Negative Clock)	SCDD	–	2 (–)
I/F Control (AMC) with EN	SFEH	–	3 (–)
I/F Control (AMC) with ENB	SFEL	–	2 (–)
I/F Control (SMC) with EN	SOEH	–	4 (–)
	SOEH2	(X2 Drive)	7 (–)
I/F Control (SMC) with ENB	SOEL	–	3 (–)
	SOEL2	(X2 Drive)	6 (–)
Mega Macro Skip	SMS1	–	4 (–)
Set/Reset Control	SRH1	–	2 (–)
Set-B/Reset-B Control	SRL1	–	2 (–)
Loop Cut	SRPD	–	12 (–)
Clock Generator	SCKG	–	16 (–)
Common Input	SCI1	–	2 (–)
Common Output	SCO1	–	5 (–)
GND	SGND	–	2 (–)

E.4 Boundary Scan Block (Interface)

E.4.1 3.3 V interface

Function	Block	Description	Cells (I/O)
Input Buffer	FI01BI	–	7 (1)
	FID1BI	50 kΩ Pull-down	7 (1)
	FIU1BI	50 kΩ Pull-up	7 (1)
	FIW1BI	5 kΩ Pull-up	7 (1)
	FIS1BI	Schmitt	11 (1)
	FDS1BI	Schmitt 50 kΩ Pull-down	11 (1)
	FUS1BI	Schmitt 50 kΩ Pull-up	11 (1)
	FWS1BI	Schmitt 5 kΩ Pull-up	11 (1)
	FIB1BI	Clock Driver	56 (1)
	FDB1BI	Clock Driver 50 kΩ Pull-down	56 (1)
	FUB1BI	Clock Driver 50 kΩ Pull-up	56 (1)
	FWB1BI	Clock Driver 5 kΩ Pull-up	56 (1)
Input Buffer with Failsafe	FIA1BI	–	7 (1)
	FDA1BI	50 kΩ Pull-down	7 (1)
	FIE1BI	Schmitt	11 (1)
	FDE1BI	Schmitt 50 kΩ Pull-down	11 (1)
	FIH1BI	Clock Driver	56 (1)
	FDH1BI	Clock Driver 50 kΩ Pull-down	56 (1)
Output Buffer	FO09B2	3 mA	13 (1)
	FO04B2	6 mA	13 (1)
	FO01B2	9 mA	13 (1)
	FO02B2	12 mA	13 (1)
	FO03B2	18 mA	25 (1)
	FO06B2	24 mA	25 (1)
Low-noise Output Buffer	FE04B2	6 mA	15 (1)
	FE01B2	9 mA	15 (1)
	FE02B2	12 mA	15 (1)
	FE03B2	18 mA	15 (1)
	FE06B2	24 mA	15 (1)
3-State Buffer	B00TB3	3 mA	29 (1)
	B0DTB3	3 mA 50 kΩ Pull-down	29 (1)
	B0UTB3	3 mA 50 kΩ Pull-up	29 (1)
	B0WTB3	3 mA 5 kΩ Pull-up	29 (1)
	B00EB3	6 mA	29 (1)
	B0DEB3	6 mA 50 kΩ Pull-down	29 (1)
	B0UEB3	6 mA 50 kΩ Pull-up	29 (1)
	B0WEB3	6 mA 5 kΩ Pull-up	29 (1)
	B008B3	9 mA	29 (1)
	B0D8B3	9 mA 50 kΩ Pull-down	29 (1)
	B0U8B3	9 mA 50 kΩ Pull-up	29 (1)
	B0W8B3	9 mA 5 kΩ Pull-up	29 (1)
	B007B3	12 mA	29 (1)
	B0D7B3	12 mA 50 kΩ Pull-down	29 (1)
	B0U7B3	12 mA 50 kΩ Pull-up	29 (1)
	B0W7B3	12 mA 5 kΩ Pull-up	29 (1)
	B009B3	18 mA	32 (1)
	B0D9B3	18 mA 50 kΩ Pull-down	32 (1)

Function	Block	Description	Cells (I/O)
3-State Buffer	B0U9B3	18 mA 50 kΩ Pull-up	32 (1)
	B0W9B3	18 mA 5 kΩ Pull-up	32 (1)
	B00HB3	24 mA	32 (1)
	B0DHB3	24 mA 50 kΩ Pull-down	32 (1)
	B0UHB3	24 mA 50 kΩ Pull-up	32 (1)
	B0WHB3	24 mA 5 kΩ Pull-up	32 (1)
Low-noise 3-State Buffer	BE0EB3	6 mA	22 (1)
	BEDEB3	6 mA 50 kΩ Pull-down	22 (1)
	BEUEB3	6 mA 50 kΩ Pull-up	22 (1)
	BEWEB3	6 mA 5 kΩ Pull-up	22 (1)
	BE08B3	9 mA	22 (1)
	BED8B3	9 mA 50 kΩ Pull-down	22 (1)
	BEU8B3	9 mA 50 kΩ Pull-up	22 (1)
	BEW8B3	9 mA 5 kΩ Pull-up	22 (1)
	BE07B3	12 mA	22 (1)
	BED7B3	12 mA 50 kΩ Pull-down	22 (1)
	BEU7B3	12 mA 50 kΩ Pull-up	22 (1)
	BEW7B3	12 mA 5 kΩ Pull-up	22 (1)
	BE09B3	18 mA	22 (1)
	BED9B3	18 mA 50 kΩ Pull-down	22 (1)
	BEU9B3	18 mA 50 kΩ Pull-up	22 (1)
	BEW9B3	18 mA 5 kΩ Pull-up	22 (1)
	BE0HB3	24 mA	22 (1)
	BEDHB3	24 mA 50 kΩ Pull-down	22 (1)
	BEUHB3	24 mA 50 kΩ Pull-up	22 (1)
	BEWHB3	24 mA 5 kΩ Pull-up	22 (1)
I/O Buffer	B00UBB	3 mA	38 (1)
	B0DUBB	3 mA 50 kΩ Pull-down	38 (1)
	B0UUBB	3 mA 50 kΩ Pull-up	38 (1)
	B0WUBB	3 mA 5 kΩ Pull-up	38 (1)
	B00CBB	6 mA	38 (1)
	B0DCBB	6 mA 50 kΩ Pull-down	38 (1)
	B0UCBB	6 mA 50 kΩ Pull-up	38 (1)
	B0WCBB	6 mA 5 kΩ Pull-up	38 (1)
	B003BB	9 mA	38 (1)
	B0D3BB	9 mA 50 kΩ Pull-down	38 (1)
	B0U3BB	9 mA 50 kΩ Pull-up	38 (1)
	B0W3BB	9 mA 5 kΩ Pull-up	38 (1)
	B001BB	12 mA	38 (1)
	B0D1BB	12 mA 50 kΩ Pull-down	38 (1)
	B0U1BB	12 mA 50 kΩ Pull-up	38 (1)
	B0W1BB	12 mA 5 kΩ Pull-up	38 (1)
	B005BB	18 mA	41 (1)
	B0D5BB	18 mA 50 kΩ Pull-down	41 (1)
	B0U5BB	18 mA 50 kΩ Pull-up	41 (1)
	B0W5BB	18 mA 5 kΩ Pull-up	41 (1)
	B00FBB	24 mA	41 (1)
	B0DFBB	24 mA 50 kΩ Pull-down	41 (1)
	B0UFBB	24 mA 50 kΩ Pull-up	41 (1)
	B0WFBB	24 mA 5 kΩ Pull-up	41 (1)

Function	Block	Description	Cells (I/O)
Low-noise I/O Buffer	BE0CBB	6 mA	31 (1)
	BEDCBB	6 mA 50 kΩ Pull-down	31 (1)
	BEUCBB	6 mA 50 kΩ Pull-up	31 (1)
	BEWCBB	6 mA 5 kΩ Pull-up	31 (1)
	BE03BB	9 mA	31 (1)
	BED3BB	9 mA 50 kΩ Pull-down	31 (1)
	BEU3BB	9 mA 50 kΩ Pull-up	31 (1)
	BEW3BB	9 mA 5 kΩ Pull-up	31 (1)
	BE01BB	12 mA	31 (1)
	BED1BB	12 mA 50 kΩ Pull-down	31 (1)
	BEU1BB	12 mA 50 kΩ Pull-up	31 (1)
	BEW1BB	12 mA 5 kΩ Pull-up	31 (1)
	BE05BB	18 mA	31 (1)
	BED5BB	18 mA 50 kΩ Pull-down	31 (1)
	BEU5BB	18 mA 50 kΩ Pull-up	31 (1)
	BEW5BB	18 mA 5 kΩ Pull-up	31 (1)
	BE0FBB	24 mA	31 (1)
	BEDFBB	24 mA 50 kΩ Pull-down	31 (1)
	BEUFBB	24 mA 50 kΩ Pull-up	31 (1)
	BEWFBB	24 mA 5 kΩ Pull-up	31 (1)
Schmitt I/O Buffer	BSIUBB	3 mA	42 (1)
	BSDUBB	3 mA 50 kΩ Pull-down	42 (1)
	BSUUBB	3 mA 50 kΩ Pull-up	42 (1)
	BSWUBB	3 mA 5 kΩ Pull-up	42 (1)
	BSICBB	6 mA	42 (1)
	BSDCBB	6 mA 50 kΩ Pull-down	42 (1)
	BSUCBB	6 mA 50 kΩ Pull-up	42 (1)
	BSWCBB	6 mA 5 kΩ Pull-up	42 (1)
	BSI3BB	9 mA	42 (1)
	BSD3BB	9 mA 50 kΩ Pull-down	42 (1)
	BSU3BB	9 mA 50 kΩ Pull-up	42 (1)
	BSW3BB	9 mA 5 kΩ Pull-up	42 (1)
	BSI1BB	12 mA	42 (1)
	BSD1BB	12 mA 50 kΩ Pull-down	42 (1)
	BSU1BB	12 mA 50 kΩ Pull-up	42 (1)
	BSW1BB	12 mA 5 kΩ Pull-up	42 (1)
	BSI5BB	18 mA	45 (1)
	BSD5BB	18 mA 50 kΩ Pull-down	45 (1)
	BSU5BB	18 mA 50 kΩ Pull-up	45 (1)
	BSW5BB	18 mA 5 kΩ Pull-up	45 (1)
	BSIFBB	24 mA	45 (1)
	BSDFBB	24 mA 50 kΩ Pull-down	45 (1)
	BSUFBB	24 mA 50 kΩ Pull-up	45 (1)
	BSWFBB	24 mA 5 kΩ Pull-up	45 (1)

Function	Block	Description	Cells (I/O)
Low-noise Schmitt I/O Buffer	BFICBB	6 mA	35 (1)
	BFDCBB	6 mA 50 kΩ Pull-down	35 (1)
	BFUCBB	6 mA 50 kΩ Pull-up	35 (1)
	BFWCBB	6 mA 5 kΩ Pull-up	35 (1)
	BFI3BB	9 mA	35 (1)
	BFD3BB	9 mA 50 kΩ Pull-down	35 (1)
	BFU3BB	9 mA 50 kΩ Pull-up	35 (1)
	BFW3BB	9 mA 5 kΩ Pull-up	35 (1)
	BFI1BB	12 mA	35 (1)
	BFD1BB	12 mA 50 kΩ Pull-down	35 (1)
	BFU1BB	12 mA 50 kΩ Pull-up	35 (1)
	BFW1BB	12 mA 5 kΩ Pull-up	35 (1)
	BFI5BB	18 mA	35 (1)
	BFD5BB	18 mA 50 kΩ Pull-down	35 (1)
	BFU5BB	18 mA 50 kΩ Pull-up	35 (1)
	BFW5BB	18 mA 5 kΩ Pull-up	35 (1)
	BFIFBB	24 mA	35 (1)
	BFDFBB	24 mA 50 kΩ Pull-down	35 (1)
	BFUFBB	24 mA 50 kΩ Pull-up	35 (1)
	BFWFBB	24 mA 5 kΩ Pull-up	35 (1)
N-ch Open drain Buffer	EXTHB2	3 mA	13 (1)
	EXUHB2	3 mA 50 kΩ Pull-up	13 (1)
	EXWHB2	3 mA 5 kΩ Pull-up	13 (1)
	EXTJB2	6 mA	13 (1)
	EXUJB2	6 mA 50 kΩ Pull-up	13 (1)
	EXWJB2	6 mA 5 kΩ Pull-up	13 (1)
	EXT1B2	9 mA	13 (1)
	EXT3B2	9 mA 50 kΩ Pull-up	13 (1)
	EXW3B2	9 mA 5 kΩ Pull-up	13 (1)
	EXT9B2	12 mA	13 (1)
	EXTBB2	12 mA 50 kΩ Pull-up	13 (1)
	EXWBB2	12 mA 5 kΩ Pull-up	13 (1)
	EXT5B2	18 mA	25 (1)
	EXT7B2	18 mA 50 kΩ Pull-up	25 (1)
	EXW7B2	18 mA 5 kΩ Pull-up	25 (1)
	EXTDB2	24 mA	25 (1)
	EXTFB2	24 mA 50 kΩ Pull-up	25 (1)
	EXWFB2	24 mA 5 kΩ Pull-up	25 (1)
Low-noise N-ch Open drain Buffer	EETJB2	6 mA	10 (1)
	EEUJB2	6 mA 50 kΩ Pull-up	10 (1)
	EEWJB2	6 mA 5 kΩ Pull-up	10 (1)
	EET1B2	9 mA	10 (1)
	EET3B2	9 mA 50 kΩ Pull-up	10 (1)
	EEW3B2	9 mA 5KΩ Pull-up	10 (1)
	EET9B2	12 mA	10 (1)
	EETBB2	12 mA 50 kΩ Pull-up	10 (1)
	EEWBB2	12 mA 5 kΩ Pull-up	10 (1)
	EET5B2	18 mA	10 (1)
	EET7B2	18 mA 50 kΩ Pull-up	10 (1)
	EEW7B2	18 mA 5 kΩ Pull-up	10 (1)
	EETDB2	24 mA	10 (1)
	EETFB2	24 mA 50 kΩ Pull-up	10 (1)
	EEWFB2	24 mA 5 kΩ Pull-up	10 (1)

E.4.2 5 V interface

Function		Block	Description	Cells (I/O)
Input Buffer		FIV1BI	–	7 (1)
		FDV1BI	50 kΩ Pull-down	7 (1)
		FIF1BI	–	11 (1)
		FDF1BI	50 kΩ Pull-down	11 (1)
		FIG1BI	–	56 (1)
		FDG1BI	50 kΩ Pull-down	56 (1)
CMOS Level	Output Buffer	FY09B2	3 mA	31 (1)
		FY04B2	6 mA	31 (1)
		FY01B2	9 mA	34 (1)
		FY02B2	12 mA	34 (1)
		FY03B2	18 mA	34 (1)
		FY06B2	24 mA	34 (1)
	Low-noise Output Buffer	FZ02B2	12 mA	33 (1)
		FZ03B2	18 mA	33 (1)
		FZ06B2	24 mA	33 (1)
	3-State Buffer	BD0TB3	3 mA	57 (1)
		BD0EB3	6 mA	57 (1)
		BD08B3	9 mA	60 (1)
		BD07B3	12 mA	60 (1)
		BD09B3	18 mA	60 (1)
		BD0HB3	24 mA	60 (1)
	Low-noise 3-State Buffer	BJ07B3	12 mA	51 (1)
		BJ09B3	18 mA	51 (1)
		BJ0HB3	24 mA	51 (1)
	I/O Buffer	BM0UBB	3 mA	66 (1)
		BM0CBB	6 mA	66 (1)
		BM03BB	9 mA	69 (1)
		BM01BB	12 mA	69 (1)
		BM05BB	18 mA	69 (1)
		BM0FBB	24 mA	69 (1)
	Low-noise I/O Buffer	BP01BB	12 mA	60 (1)
		BP05BB	18 mA	60 (1)
		BP0FBB	24 mA	60 (1)
	Schmitt I/O Buffer	BQIUBB	3 mA	70 (1)
		BQICBB	6 mA	70 (1)
		BQI3BB	9 mA	73 (1)
		BQI1BB	12 mA	73 (1)
		BQI5BB	18 mA	73 (1)
		BQIFBB	24 mA	73 (1)
	Low-noise Schmitt I/O Buffer	BUI1BB	12 mA	64 (1)
		BUI5BB	18 mA	64 (1)
		BUIFBB	24 mA	64 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Output Buffer	FV0AB2	1 mA	13 (1)
		FV0BB2	2 mA	13 (1)
		FV09B2	3 mA	13 (1)
		FV04B2	6 mA	13 (1)
		FV01B2	9 mA	25 (1)
		FV02B2	12 mA	25 (1)
		FV03B2	18 mA	25 (1)
		FV06B2	24 mA	25 (1)
	Low-noise Output Buffer	FW02B2	12 mA	15 (1)
		FW03B2	18 mA	15 (1)
		FW06B2	24 mA	15 (1)
	3-State Buffer	BV0QB3	1 mA	52 (1)
		BVDQB3	1 mA 50 kΩ Pull-down	52 (1)
		BV0MB3	2 mA	52 (1)
		BVDMB3	2 mA 50 kΩ Pull-down	52 (1)
		BV0TB3	3 mA	52 (1)
		BVDTB3	3 mA 50 kΩ Pull-down	52 (1)
		BV0EB3	6 mA	52 (1)
		BVDEB3	6 mA 50 kΩ Pull-down	52 (1)
		BV08B3	9 mA	54 (1)
		BVD8B3	9 mA 50 kΩ Pull-down	54 (1)
		BV07B3	12 mA	54 (1)
		BVD7B3	12 mA 50 kΩ Pull-down	54 (1)
		BV09B3	18 mA	54 (1)
		BVD9B3	18 mA 50 kΩ Pull-down	54 (1)
		BV0HB3	24 mA	54 (1)
		BVDHB3	24 mA 50 kΩ Pull-down	54 (1)
	Low-noise 3-State Buffer	BY07B3	12 mA	39 (1)
		BYD7B3	12 mA 50 kΩ Pull-down	39 (1)
		BY09B3	18 mA	39 (1)
		BYD9B3	18 mA 50 kΩ Pull-down	39 (1)
		BY0HB3	24 mA	39 (1)
		BYDHB3	24 mA 50 kΩ Pull-down	39 (1)
	I/O Buffer	BW0XBB	1 mA	61 (1)
		BWDXBB	1 mA 50 kΩ Pull-down	61 (1)
		BW0KBB	2 mA	61 (1)
		BWDKBB	2 mA 50 kΩ Pull-down	61 (1)
		BW0UBB	3 mA	61 (1)
		BWDUBB	3 mA 50 kΩ Pull-down	61 (1)
		BW0CBB	6 mA	61 (1)
		BWDCBB	6 mA 50 kΩ Pull-down	61 (1)
		BW03BB	9 mA	63 (1)
		BWD3BB	9 mA 50 kΩ Pull-down	63 (1)
		BW01BB	12 mA	63 (1)
		BWD1BB	12 mA 50 kΩ Pull-down	63 (1)
		BW05BB	18 mA	63 (1)
		BWD5BB	18 mA 50 kΩ Pull-down	63 (1)
		BW0FBB	24 mA	63 (1)
		BWDFBB	24 mA 50 kΩ Pull-down	63 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Low-noise I/O Buffer	BX01BB	12 mA	48 (1)
		BXD1BB	12 mA 50 kΩ Pull-down	48 (1)
		BX05BB	18 mA	48 (1)
		BXD5BB	18 mA 50 kΩ Pull-down	48 (1)
		BX0FBB	24 mA	48 (1)
		BXDFBB	24 mA 50 kΩ Pull-down	48 (1)
	Schmitt I/O Buffer	BKIXBB	1 mA	65 (1)
		BKDXBB	1 mA 50 kΩ Pull-down	65 (1)
		BKIKBB	2 mA	65 (1)
		BKDKBB	2 mA 50 kΩ Pull-down	65 (1)
		BKIUBB	3 mA	65 (1)
		BKDUBB	3 mA 50 kΩ Pull-down	65 (1)
		BKICBB	6 mA	65 (1)
		BKDCBB	6 mA 50 kΩ Pull-down	65 (1)
		BKI3BB	9 mA	67 (1)
		BKD3BB	9 mA 50 kΩ Pull-down	67 (1)
		BKI1BB	12 mA	67 (1)
		BKD1BB	12 mA 50 kΩ Pull-down	67 (1)
		BKI5BB	18 mA	67 (1)
		BKD5BB	18 mA 50 kΩ Pull-down	67 (1)
		BKIFBB	24 mA	67 (1)
		BKDFBB	24 mA 50 kΩ Pull-down	67 (1)
	Low-noise Schmitt I/O Buffer	BZI1BB	12 mA	52 (1)
		BZD1BB	12 mA 50 kΩ Pull-down	52 (1)
		BZI5BB	18 mA	52 (1)
		BZD5BB	18 mA 50 kΩ Pull-down	52 (1)
		BZIFBB	24 mA	52 (1)
		BZDFBB	24 mA 50 kΩ Pull-down	52 (1)
	N-ch Open drain Buffer	EVTTB2	1 mA	13 (1)
		EVTKB2	2 mA	13 (1)
		EVTHB2	3 mA	13 (1)
		EVTJB2	6 mA	13 (1)
		EVT1B2	9 mA	25 (1)
		EVT9B2	12 mA	25 (1)
		EVT5B2	18 mA	25 (1)
		EVTDB2	24 mA	25 (1)
	Low-noise N-ch Open drain Buffer	EYT9B2	12 mA	10 (1)
		EYT5B2	18 mA	10 (1)
		EYTDB2	24 mA	10 (1)

E.4.3 PCI

Function	Block	Description	Cells (I/O)
3V PCI Input Buffer	BP3IBI	–	7 (1)
3V PCI Output Buffer	BP3OB2	–	25 (1)
3V PCI 3-State Buffer	BP3TB3	–	32 (1)
3V PCI I/O Buffer	BP3BBB	–	41 (1)
5V PCI Input Buffer	BP5IBI	–	7 (1)
5V PCI Output Buffer	BP5OB2	–	25 (1)
5V PCI 3-State Buffer	BP5TB3	–	54 (1)
5V PCI I/O Buffer	BP5BBB	–	63 (1)

E.5 Boundary Scan Block (Function)

E.5.1 TAP macro

Function	Block	Description	Cells (I/O)
TAP MACRO	SBC4	–	– (–)
TAP Macro with NEC Scan	SBCL	–	– (–)

E.5.2 Level generator

Function	Block	Description	Cells (I/O)
Level Generator (CLANP)	SBZ1	–	0 (–)

E.5.3 D-latch

Function	Block	Description	Cells (I/O)
D-Latch with SB Q Out (Low Power) for Boundary Scan Block	L606	–	5 (–)

[MEMO]

For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
http://www.cn.necel.com/

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

G0706