お客様各位

カタログ等資料中の旧社名の扱いについて

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ルネサスエレクトロニクス ホームページ（http://www.renesas.com）

2010年4月1日
ルネサスエレクトロニクス株式会社

【発行】ルネサスエレクトロニクス株式会社（http://www.renesas.com）

【問い合わせ先】http://japan.renesas.com/inquiry

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   標準水準： コンピュータ、OA 機器、通信機器、計測機器、AV 機器、家電、工作機械、パーソナル機器、産業用ロボット

   高品質水準： 輸送機器（自動車、電車、船舶等）、交通用信号機器、防災・防犯装置、各種安全装置、生命維持を目的として設計されていない医療機器（厚生労働省定義の管理医療機器に相当）

   特定水準： 航空機器、航空宇宙機器、海底中継機器、原子力制御システム、生命維持のための医療機器（生命維持装置、人体に埋め込み使用するもの、治療行為（患部切り出し等）を行うもの、その他直接人命に影響を与えるもの）（厚生労働省定義の高度管理医療機器に相当）またはシステム等
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RENESAS

Block Library

CMOS-N5 Family

CMOS Gate Array

Memory Ver.2.0

Document No. A14683JJ2V0BL00 (2nd edition)
Date Published September 2000 N CP(K)

[MEMO]

Summary of Contents

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  標準水準：コンピュータ，OA機器，通信機器，計測機器，AV機器，家電，工作機械，パーソナル機器，産業用ロボット

  特別水準：輸送機器（自動車，列車，船舶等），交通用信号機器，防災／防犯装置，各種安全装置，生命維持を直接の目的としない医療機器

  特定水準：航空機器，航空宇宙機器，海底中継機器，原子力制御システム，生命維持のための医療機器，生命維持のための装置またはシステム等

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M7　98.8

本版で改訂された主な個所

箇　　所	内　　容
pp.12〜15, 52, 53, 60, 61	**次のブロックの** Basic RAM, **端子情報（**Input, Output**）**, Switching speed, Read Cycle Timing, Write Cycle Timing, Equivalent Cells **を追加。** RB4H, RB4M, RBCM, RBEH

本文欄外の★印は，本版で改訂された主な箇所を示しています。

巻末にアンケート・コーナを設けております。このドキュメントに対するご意見をお気軽にお寄せください。

[MEMO]

はじめに

1．構成

このマニュアルは, CMOS-N5ファミリ用メモリ･ブロック・ライブラリについて記載しています。
回路設計を行う際は必ず先にCMOS-N5ファミリ　設計マニュアル(A13826J)を読んでください。
また, マニュアルに記載された事項（一般事項、注意事項、制限事項）は必ずお守りください。お守りいただけない場合, LSI製品の品質や性能の低下，および動作の異常が生じることがあります。

このマニュアルは, 次のような構成になっています。

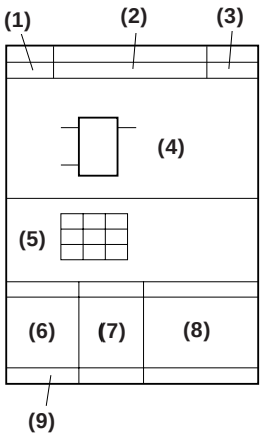
(1) はじめに
このマニュアルを活用されるにあたっての注意事項, 用語, 定義などを説明しています。

(2) CONTENTS
目次をインタフェース／ファンクション・ブロックのアルファベット順リストとして作成してあります。ブロック名から探すときなどに利用してください。CONTENTS中のハイフンは“検討中”を表します。

(3) CHAPTER1　HIGH DENSITY SINGLE-PORT RAM BLOCK (Soft Macro)
(4) CHAPTER2　HIGH DENSITY DUAL-PORT RAM BLOCK (Soft Macro)
(5) APPENDIX　BASIC RAM BLOCK
CHAPTER 1, CHAPTER 2, APPENDIXは, それぞれのブロックについて，アルファベット順に並べてあります。各ページには, 論理シンボル, 真理値表, 入出力データ, スイッチング・スピード（伝達遅延時間）などを記載してあります。

なお，CMOS-N5ファミリの高密度RAMブロックはソフト･マクロ構成となっています。６種類のハード・マクロを基にビット，ワードを構成し，テスト回路（BIST），セレクタを内蔵するソフト・マクロです。そのため，このマニュアルでは，ベーシックRAMブロック（ハード・マクロ）と高密度RAMブロック（ソフト・マクロ）を記載しています。またメモリ･ブロックを使用する場合，使用セル数と各マスタごとの使用可能セル数により搭載不可能な場合があります。回路設計を行う際は，必ず先にCMOS-N5ファミリ　設計マニュアル(A13826J)をお読みください。

2. ブロック・ライブラリ記載内容の説明



(1) Block Type : 機能ブロックの名称
(2) Function : そのブロックの機能名
(3) Basic RAM : そのブロックのBasic RAM構成
(4) Logic Diagram : そのブロックの論理シンボル（論理図）
(5) Truth Table : そのブロックの真理値表
(6) Input : 入力端子の端子名，ファンイン
(7) Output : 出力端子の端子名，ファンアウト
(8) Switching speed : そのブロックの伝達遅延時間など
(9) Equivalent Cells : 使用セル数

なお，スイッチング・スピードの記号は以下のとおりです。

A → Y (H L)
↑ ↑↑
(10) (11)(12)

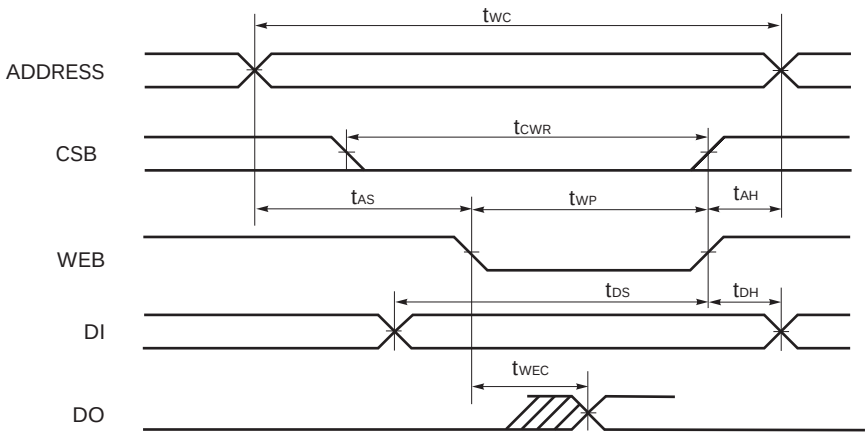
(10) 信号のパス名（入力→出力）
(11) 入力信号の状態（H :ハイ・レベル，L : ロウ・レベル，Z :ハイ・インピーダンス）
(12) 出力信号の状態（H :ハイ・レベル，L : ロウ・レベル，Z :ハイ・インピーダンス）

3. メモリ・タイミング

斜線の部分はアドレスまたはCSBが変化するとき，内部回路で一時的にハイ・インピーダンス状態になります。そのため出力がこの間不定になります。

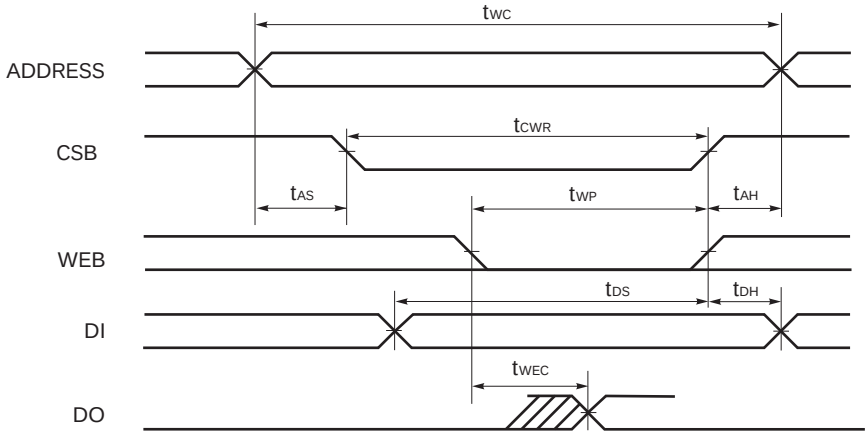
3.1 高密度RAM（シングルポート）

(1) ライト・サイクル・タイミング 1（WEBコントロール・モード）



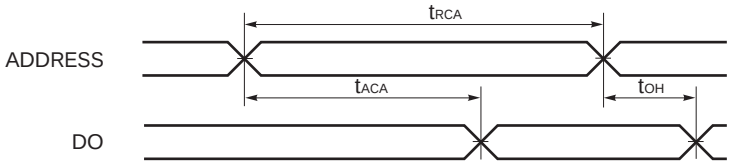
注意　WEBまたはCSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。また，DOにDIが出力される時間は，WEBの立ち下がりからtwec経過した時間と，DIの変化からDOが変化するまでの時間のどちらか遅い方で決まります。

(2) ライト・サイクル・タイミング 2（CSBコントロール・モード）



注意　WEBまたはCSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。また，DOにDIが出力される時間は，WEBの立ち下がりからtwec経過した時間と，DIの変化からDOが変化するまでの時間のどちらか遅い方で決まります。

(3) リード・サイクル・タイミング 1（アドレス・アクセス）

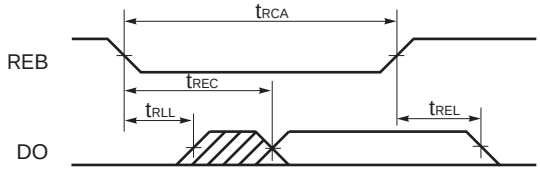


CSB = 0, WEB = 1, REB = 0

t_{ACA}：アドレスが決定後，出力が確定するまでの時間。

t_{OH}：任意のアドレスが変化したとき，変化する前のデータが保持されている時間

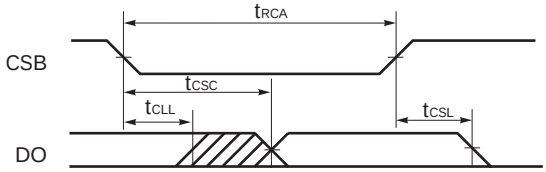
(4) リード・サイクル・タイミング 2（REBアクセス）



CSB = 0, WEB = 1

注意　ADDRESS信号は，REB信号のロウ・レベル伝達と同時に，あるいはそれ以前に確定しなければなりません。

(5) リード・サイクル・タイミング 3（CSBアクセス）

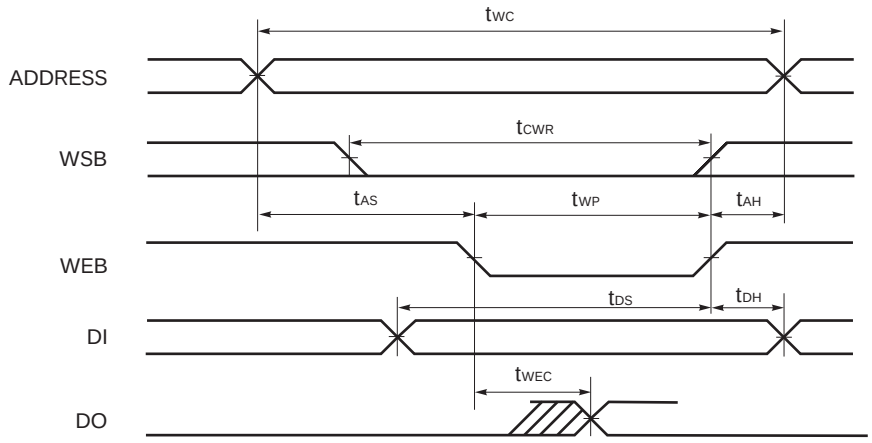


REB = 0, WEB = 1

注意　ADDRESS信号は，CSB信号のロウ・レベル伝達と同時に，あるいはそれ以前に確定しなければなりません。

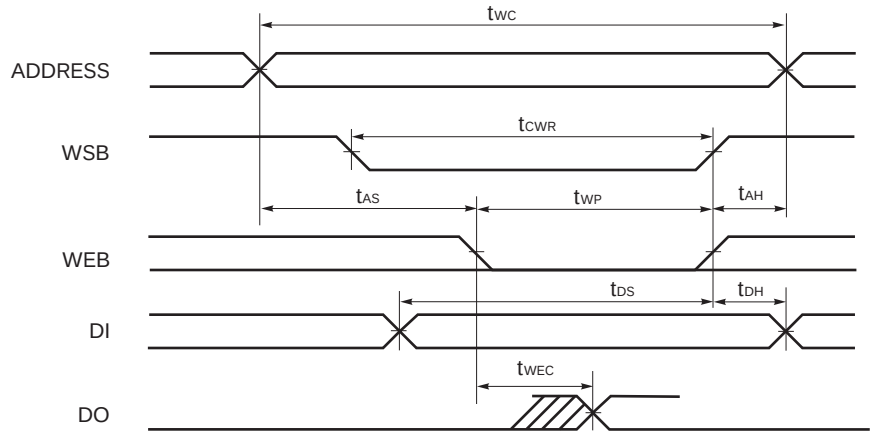
3.2　高密度RAM（デュアルポート）

(1) ライト・サイクル・タイミング 1（WEBコントロール・モード）



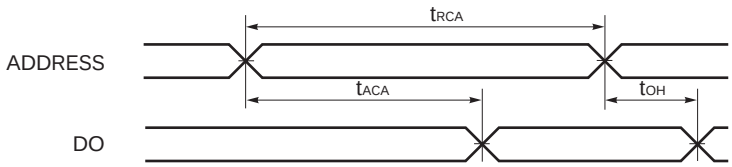
注意　WEBまたはWSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。また，READアドレス，WRITEアドレスが同一アドレスの場合，DOにDIが出力される時間は，WEBの立ち下がりからtWEC経過した時間と，DIの変化からDOが変化するまでの時間のどちらか遅い方で決まります。

(2) ライト・サイクル・タイミング 2（WSBコントロール・モード）

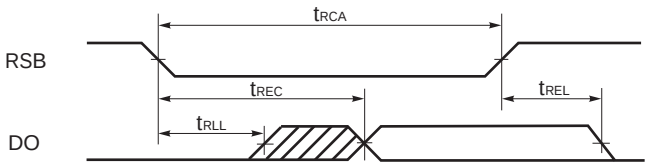


注意　WEBまたはWSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。また，READアドレス，WRITEアドレスが同一アドレスの場合，DOにDIが出力される時間は，WEBの立ち下がりからtWEC経過した時間と，DIの変化からDOが変化するまでの時間のどちらか遅い方で決まります。

(3) リード・サイクル・タイミング 1（RSB=0）



(4) リード・サイクル・タイミング 2



注意　ADDRESS信号は，RSB信号のロウ・レベル伝達と同時に，あるいはそれ以前に確定していなければなりません。

4. BIST(Built in Self Test)

BISTとはRAM用テスト回路のことです。テスト･アドレス発生器，テスト・データ発生器，テスト・イネーブル発生器，期待値発生器，比較器から構成されています。テスト用端子としてTEB,TIN,TOUTの３本を外部端子に接続するだけでRAMのテストが行えます。また複数のRAMを搭載した場合にも，簡単にテストすることができます。

関連資料

関連資料は暫定版の場合がありますが，この資料では「暫定」の表示をしておりません。あらかじめ，ご了承ください。

- CMOS-N5ファミリ　設計マニュアル　（A13826J）
- CMOS-N5 Family Block Library　（A13872J）
- CMOS-N5 Family Memory Block Library　（このマニュアル）
- CMOS-N5 ファミリ　設計マニュアル　メガマクロ編　（A14759J）
- テスト容易化設計　ユーザーズ・マニュアル　（A14357J）

設計する際は最新の資料を使用していただくため, NEC販売担当または特約店にご確認ください。

CONTENTS

Remark (*): Under development

SINGLE-PORT HIGH DENSITY RAM

Block Type	Function	Basic RAM	Test Block	Equivalent Cells	Page
RBEB	64 words x 20 bits Single-port RAM	K1AB × 2	RUEB	4463	54
RBED	128 words x 20 bits Single-port RAM	K1AB × 4	RUED	8574	56
RBEF	256 words x 20 bits Single-port RAM	K1AB × 8	RUEF	16751	58
RBEH(*)	512 words x 20 bits Single-port RAM	K1AB × 16	RUEH	33080	60
RBH7	16 words x 32 bits Single-port RAM	K147 × 8	RUH7	3262	62
RBH9	32 words x 32 bits Single-port RAM	K149 × 8	RUH9	5222	64
RBHB	64 words x 32 bits Single-port RAM	K18B × 4	RUHB	7318	66
RBHD	128 words x 32 bits Single-port RAM	K14D × 8	RUHD	14245	68
RBHF	256 words x 32 bits Single-port RAM	K18F × 4	RUHF	24442	70
RBHH	512 words x 32 bits Single-port RAM	K18F × 8	RUHH	48463	72
RBKB	64 words x 40 bits Single-port RAM	K1AB × 4	RUKB	8704	74
RBKD	128 words x 40 bits Single-port RAM	K1AB × 8	RUKD	16905	76
RBKF	256 words x 40 bits Single-port RAM	K18F × 5	RUKF	30497	78

Remark (*): Under development

CHAPTER 2 HIGH DENSITY DUAL-PORT RAM BLOCK (Soft Macro)

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APPENDIX **BASIC RAM BLOCK** Page **133**

CHAPTER 1

HIGH DENSITY

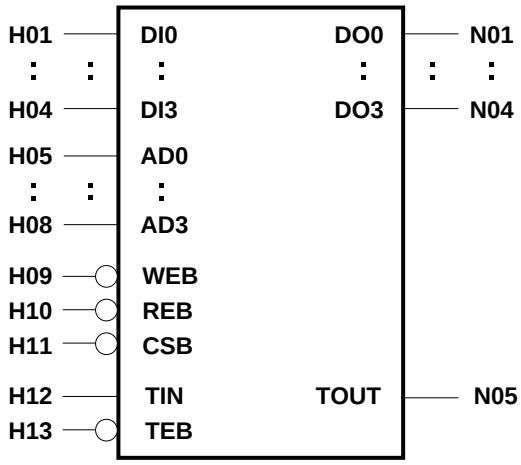
SINGLE-PORT RAM BLOCK

(Soft Macro)

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB47	**16 words × 4 bits Single-port RAM**	**K147 × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD3 (LH)		4.21	
:	:	:	:	:	:	→DO0 to DO3 (HH)		4.27	
H04	DI3	2.1	N04	DO3	32.0	(HL)		3.77	
H05	AD0	2.1	N05	TOUT	34.0	(LL)		3.71	
:	:	:							
H08	AD3	2.1				CSB (LH)		1.54	
H09	WEB	2.1				→DO0 to DO3 (HL)		1.54	
H10	REB	1.0							
H11	CSB	1.0				REB (LH)		1.54	
H12	TIN	2.1				→DO0 to DO3 (HL)		1.54	
H13	TEB	4.1							
						DI0 to DI3 (HH)		2.53	
						→DO0 to DO3 (LL)		2.38	

Equivalent Cells	572

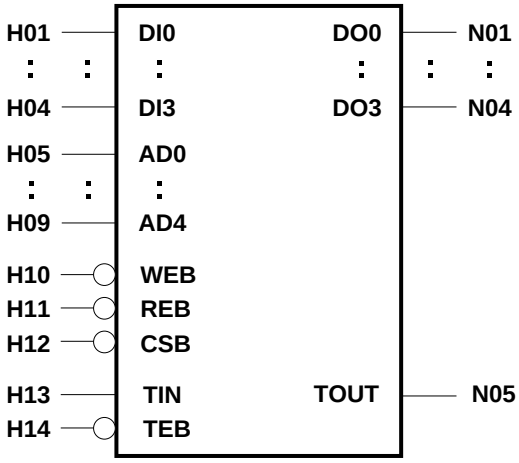
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.686**		
Address access time	**t_{ACA}**			**7.686**
Address output hold time	**t_{OH}**	**2.226**		
CSB access time	**t_{CSC}**			**2.772**
CSB output hold time	**t_{CSL}**	**0.924**		**2.772**
CSB output set time	**t_{CLL}**	**0.924**		
REB access time	**t_{REC}**			**2.772**
REB output hold time	**t_{REL}**	**0.924**		**2.772**
REB output set time	**t_{RLL}**	**0.924**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.630**		
CSB-WEB reset time	**t_{CWR}**	**4.819**		
Write pulse width	**t_{WP}**	**4.819**		
Address setup time	**t_{AS}**	**6.032**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.520**		
Input data hold time	**t_{DH}**	**3.144**		
WEB access time	**t_{WEC}**			**3.132**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB49	**32 words × 4 bits Single-port RAM**	**K149 × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD4 (LH)		4.29	
:	:	:	:	:	:	→DO0 to DO3 (HH)		4.35	
H04	DI3	2.1	N04	DO3	32.0	(HL)		3.92	
H05	AD0	2.1	N05	TOUT	34.0	(LL)		3.86	
:	:	:							
H09	AD4	2.1				CSB (LH)		1.57	
H10	WEB	2.1				→DO0 to DO3 (HL)		1.55	
H11	REB	1.0							
H12	CSB	1.0				REB (LH)		1.57	
H13	TIN	2.1				→DO0 to DO3 (HL)		1.55	
H14	TEB	4.1							
						DI0 to DI3 (HH)		2.54	
						→DO0 to DO3 (LL)		2.37	

Equivalent Cells	825

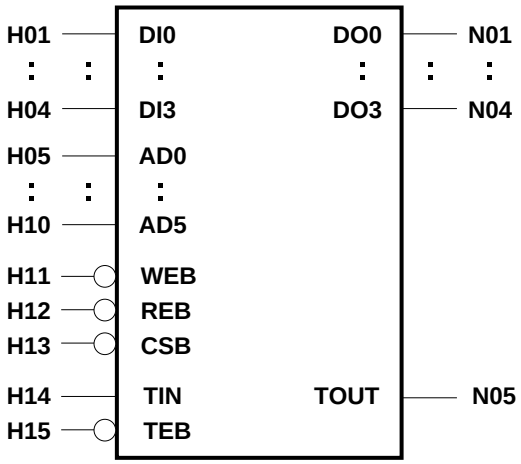
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.830**		
Address access time	**t_{ACA}**			**7.830**
Address output hold time	**t_{OH}**	**2.316**		
CSB access time	**t_{CSC}**			**2.826**
CSB output hold time	**t_{CSL}**	**0.930**		**2.790**
CSB output set time	**t_{CLL}**	**0.942**		
REB access time	**t_{REC}**			**2.826**
REB output hold time	**t_{REL}**	**0.930**		**2.790**
REB output set time	**t_{RLL}**	**0.942**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.464**		
CSB-WEB reset time	**t_{CWR}**	**4.590**		
Write pulse width	**t_{WP}**	**4.590**		
Address setup time	**t_{AS}**	**6.096**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.187**		
Input data hold time	**t_{DH}**	**3.114**		
WEB access time	**t_{WEC}**			**3.132**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB4B	**64 words × 4 bits Single-port RAM**	**K149 × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD5 (LH)		4.60	
:	:	:	:	:	:	→DO0 to DO3 (HH)		4.63	
H04	DI3	2.1	N04	DO3	32.0	(HL)		2.33	
H05	AD0	2.1	N05	TOUT	34.0	(LL)		4.27	
:	:	:							
H10	AD5	2.1				CSB (LH)		2.01	
H11	WEB	2.1				→DO0 to DO3 (HL)		2.05	
H12	REB	1.0							
H13	CSB	2.1				REB (LH)		1.87	
H14	TIN	2.1				→DO0 to DO3 (HL)		1.95	
H15	TEB	4.1							
						DI0 to DI3 (HH)		2.83	
						→DO0 to DO3 (LL)		2.78	

Equivalent Cells	1448

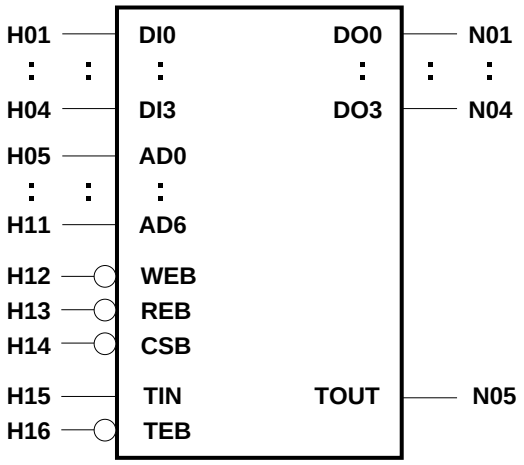
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.334**		
Address access time	**t_{ACA}**			**8.334**
Address output hold time	**t_{OH}**	**1.398**		
CSB access time	**t_{CSC}**			**3.618**
CSB output hold time	**t_{CSL}**	**1.230**		**3.690**
CSB output set time	**t_{CLL}**	**1.206**		
REB access time	**t_{REC}**			**3.366**
REB output hold time	**t_{REL}**	**1.170**		**3.510**
REB output set time	**t_{RLL}**	**1.122**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.464**		
CSB-WEB reset time	**t_{CWR}**	**4.590**		
Write pulse width	**t_{WP}**	**4.590**		
Address setup time	**t_{AS}**	**6.096**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.187**		
Input data hold time	**t_{DH}**	**3.114**		
WEB access time	**t_{WEC}**			**3.672**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB4D	**128 words × 4 bits Single-port RAM**	**K14D × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD6 (LH)		4.59	
:	:	:	:	:	:	→DO0 to DO3 (HH)		4.65	
H04	DI3	2.1	N04	DO3	32.0	(HL)		4.26	
H05	AD0	2.1	N05	TOUT	34.0	(LL)		4.20	
:	:	:							
H11	AD6	2.1				CSB (LH)		1.66	
H12	WEB	2.1				→DO0 to DO3 (HL)		1.61	
H13	REB	1.0							
H14	CSB	1.0				REB (LH)		1.66	
H15	TIN	2.1				→DO0 to DO3 (HL)		1.61	
H16	TEB	4.1							
						DI0 to DI3 (HH)		2.85	
						→DO0 to DO3 (LL)		2.61	

Equivalent Cells	1983

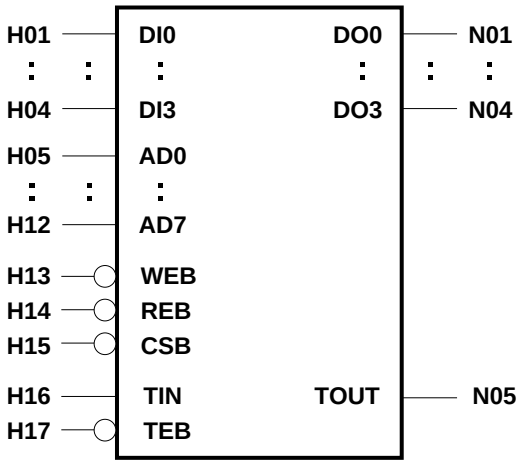
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.370**		
Address access time	**t_{ACA}**			**8.370**
Address output hold time	**t_{OH}**	**2.520**		
CSB access time	**t_{CSC}**			**2.988**
CSB output hold time	**t_{CSL}**	**0.966**		**2.898**
CSB output set time	**t_{CLL}**	**0.996**		
REB access time	**t_{REC}**			**2.988**
REB output hold time	**t_{REL}**	**0.966**		**2.898**
REB output set time	**t_{RLL}**	**0.996**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**3.294**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB4F	**256 words × 4 bits Single-port RAM**	**K14D × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H04	DI3	2.1	N04	DO3	32.0
H05	AD0	2.1	N05	TOUT	34.0
:	:	:			
H12	AD7	2.1			
H13	WEB	2.1			
H14	REB	1.0			
H15	CSB	2.1			
H16	TIN	2.1			
H17	TEB	4.1			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
AD0 to AD7 →DO0 to DO3	(LH)		4.91	
	(HH)		4.93	
	(HL)		2.39	
	(LL)		4.62	
CSB →DO0 to DO3	(LH)		2.11	
	(HL)		2.10	
REB →DO0 to DO3	(LH)		1.96	
	(HL)		2.00	
DI0 to DI3 →DO0 to DO3	(HH)		3.14	
	(LL)		3.03	

Equivalent Cells	3726

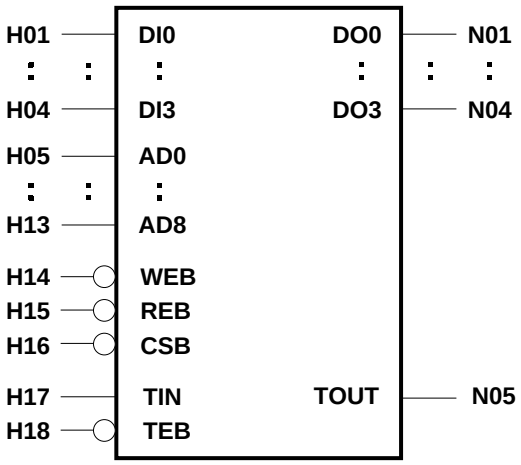
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.874**		
Address access time	**t_{ACA}**			**8.874**
Address output hold time	**t_{OH}**	**1.434**		
CSB access time	**t_{CSC}**			**3.798**
CSB output hold time	**t_{CSL}**	**1.260**		**3.780**
CSB output set time	**t_{CLL}**	**1.266**		
REB access time	**t_{REC}**			**3.600**
REB output hold time	**t_{REL}**	**1.200**		**3.600**
REB output set time	**t_{RLL}**	**1.176**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**3.834**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
★ **RB4H**	**512 words × 4 bits Single-port RAM**	**K14D × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

★

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD8 (LH)		5.07	
:	:	:	:	:	:	→DO0 to DO3 (HH)		5.04	
H04	DI3	2.1	N04	DO3	32.0	(HL)		3.20	
H05	AD0	2.1	N05	TOUT	34.0	(LL)		4.95	
:	:	:							
H13	AD8	2.1				CSB (LH)		2.78	
H14	WEB	2.1				→DO0 to DO3 (HL)		2.89	
H15	REB	1.0							
H16	CSB	1.0				REB (LH)		2.08	
H17	TIN	2.1				→DO0 to DO3 (HL)		2.50	
H18	TEB	4.1							
						DI0 to DI3 (HH)		3.25	
						→DO0 to DO3 (LL)		3.36	

Equivalent Cells	7165

★

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.126**		
Address access time	**t_{ACA}**			**9.126**
Address output hold time	**t_{OH}**	**1.920**		
CSB access time	**t_{CSC}**			**5.004**
CSB output hold time	**t_{CSL}**	**1.734**		**5.202**
CSB output set time	**t_{CLL}**	**1.668**		
REB access time	**t_{REC}**			**3.744**
REB output hold time	**t_{REL}**	**1.500**		**4.500**
REB output set time	**t_{RLL}**	**1.248**		

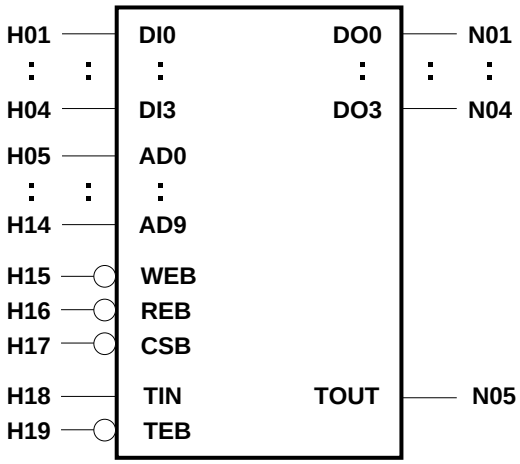
★

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**4.194**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB4M	**1K words × 4 bits Single-port RAM**	**K14D × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	24.0	AD0 to AD9 (LH)		5.63	
:	:	:	:	:	:	→DO0 to DO3 (HH)		5.56	
H04	DI3	2.1	N04	DO3	24.0	(HL)		3.55	
H05	AD0	2.1	N05	TOUT	34.0	(LL)		5.45	
:	:	:							
H14	AD9	2.1				CSB (LH)		3.22	
H15	WEB	2.1				→DO0 to DO3 (HL)		3.03	
H16	REB	1.0							
H17	CSB	1.0				REB (LH)		2.52	
H18	TIN	2.1				→DO0 to DO3 (HL)		2.75	
H19	TEB	4.1							
						DI0 to DI3 (HH)		3.76	
						→DO0 to DO3 (LL)		3.86	

Equivalent Cells	14102

★

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.134**		
Address access time	**t_{ACA}**			**10.134**
Address output hold time	**t_{OH}**	**2.130**		
CSB access time	**t_{CSC}**			**5.796**
CSB output hold time	**t_{CSL}**	**1.818**		**5.454**
CSB output set time	**t_{CLL}**	**1.932**		
REB access time	**t_{REC}**			**4.536**
REB output hold time	**t_{REL}**	**1.650**		**4.950**
REB output set time	**t_{RLL}**	**1.512**		

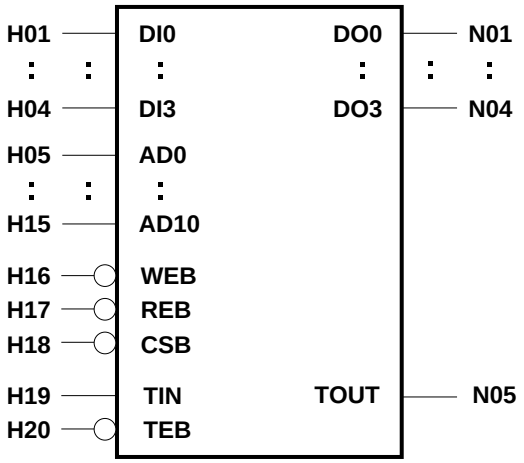
★

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**5.148**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB4S	**2K words × 4 bits Single-port RAM**	**K14D × 16**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	15.0	AD0 to AD10 (LH)		5.77	
:	:	:	:	:	:	→DO0 to DO3 (HH)		5.67	
H04	DI3	2.1	N04	DO3	15.0	(HL)		3.69	
H05	AD0	2.1	N05	TOUT	34.0	(LL)		5.73	
:	:	:							
H15	AD10	2.1				CSB (LH)		3.56	
H16	WEB	2.1				→DO0 to DO3 (HL)		3.41	
H17	REB	1.0							
H18	CSB	2.1				REB (LH)		2.66	
H19	TIN	2.1				→DO0 to DO3 (HL)		3.07	
H20	TEB	4.1							
						DI0 to DI3 (HH)		3.87	
						→DO0 to DO3 (LL)		4.14	

Equivalent Cells	27942

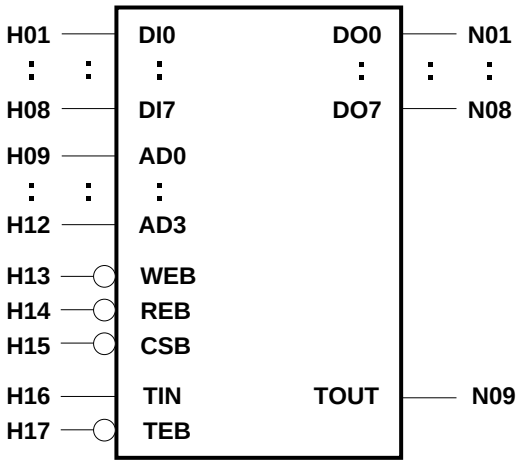
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.386**		
Address access time	**t_{ACA}**			**10.386**
Address output hold time	**t_{OH}**	**2.214**		
CSB access time	**t_{CSC}**			**6.408**
CSB output hold time	**t_{CSL}**	**2.046**		**6.138**
CSB output set time	**t_{CLL}**	**2.136**		
REB access time	**t_{REC}**			**4.824**
REB output hold time	**t_{REL}**	**1.842**		**5.526**
REB output set time	**t_{RLL}**	**1.608**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**5.580**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB87	**16 words × 8 bits Single-port RAM**	**K147 × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD3 (LH)		4.27	
:	:	:	:	:	:	→DO0 to DO7 (HH)		4.31	
H08	DI7	2.1	N08	DO7	32.0	(HL)		3.80	
H09	AD0	2.1	N09	TOUT	34.0	(LL)		3.76	
:	:	:							
H12	AD3	2.1				CSB (LH)		1.59	
H13	WEB	2.1				→DO0 to DO7 (HL)		1.58	
H14	REB	1.0							
H15	CSB	1.0				REB (LH)		1.59	
H16	TIN	2.1				→DO0 to DO7 (HL)		1.58	
H17	TEB	4.1							
						DI0 to DI7 (HH)		2.53	
						→DO0 to DO7 (LL)		2.38	

Equivalent Cells	952

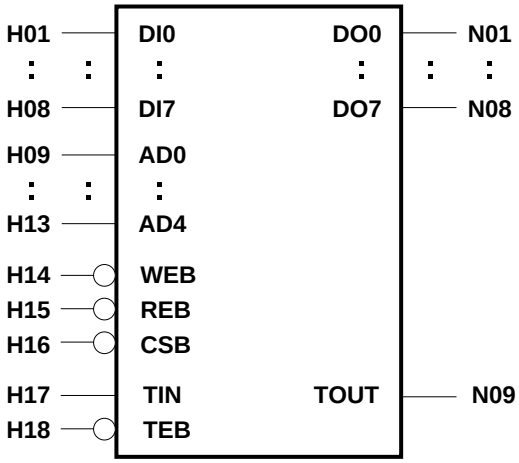
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.758**		
Address access time	**t_{ACA}**			**7.758**
Address output hold time	**t_{OH}**	**2.256**		
CSB access time	**t_{CSC}**			**2.862**
CSB output hold time	**t_{CSL}**	**0.948**		**2.844**
CSB output set time	**t_{CLL}**	**0.954**		
REB access time	**t_{REC}**			**2.862**
REB output hold time	**t_{REL}**	**0.948**		**2.844**
REB output set time	**t_{RLL}**	**0.954**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.630**		
CSB-WEB reset time	**t_{CWR}**	**4.819**		
Write pulse width	**t_{WP}**	**4.819**		
Address setup time	**t_{AS}**	**6.032**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.520**		
Input data hold time	**t_{DH}**	**3.144**		
WEB access time	**t_{WEC}**			**3.222**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB89	**32 words × 8 bits Single-port RAM**	**K149 × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD4 (LH)		4.34	
:	:	:	:	:	:	→DO0 to DO7 (HH)		4.39	
H08	DI7	2.1	N08	DO7	32.0	(HL)		3.97	
H09	AD0	2.1	N09	TOUT	34.0	(LL)		3.92	
:	:	:							
H13	AD4	2.1				CSB (LH)		1.61	
H14	WEB	2.1				→DO0 to DO7 (HL)		1.59	
H15	REB	1.0							
H16	CSB	1.0				REB (LH)		1.61	
H17	TIN	2.1				→DO0 to DO7 (HL)		1.59	
H18	TEB	4.1							
						DI0 to DI7 (HH)		2.55	
						→DO0 to DO7 (LL)		2.38	

Equivalent Cells	1454

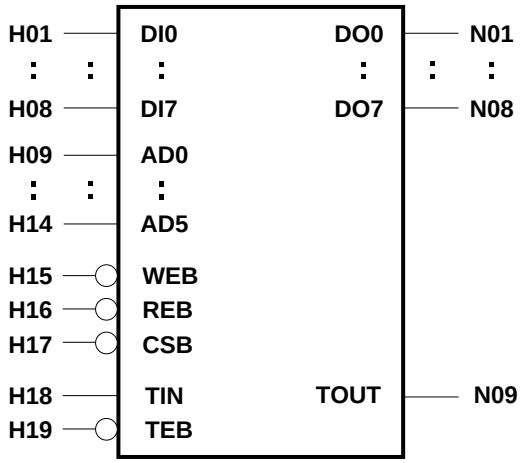
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.902**		
Address access time	**t_{ACA}**			**7.902**
Address output hold time	**t_{OH}**	**2.352**		
CSB access time	**t_{CSC}**			**2.898**
CSB output hold time	**t_{CSL}**	**0.954**		**2.862**
CSB output set time	**t_{CLL}**	**0.966**		
REB access time	**t_{REC}**			**2.898**
REB output hold time	**t_{REL}**	**0.954**		**2.862**
REB output set time	**t_{RLL}**	**0.966**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.464**		
CSB-WEB reset time	**t_{CWR}**	**4.590**		
Write pulse width	**t_{WP}**	**4.590**		
Address setup time	**t_{AS}**	**6.096**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.187**		
Input data hold time	**t_{DH}**	**3.114**		
WEB access time	**t_{WEC}**			**3.240**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB8B	**64 words × 8 bits Single-port RAM**	**K18B × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD5 (LH)		4.65	
:	:	:	:	:	:	→DO0 to DO7 (HH)		4.71	
H08	DI7	2.1	N08	DO7	32.0	(HL)		4.36	
H09	AD0	2.1	N09	TOUT	34.0	(LL)		4.30	
:	:	:							
H14	AD5	2.1				CSB (LH)		1.63	
H15	WEB	2.1				→DO0 to DO7 (HL)		1.58	
H16	REB	1.0							
H17	CSB	1.0				REB (LH)		1.63	
H18	TIN	2.1				→DO0 to DO7 (HL)		1.58	
H19	TEB	4.1							
						DI0 to DI7 (HH)		2.70	
						→DO0 to DO7 (LL)		2.47	

Equivalent Cells	1993

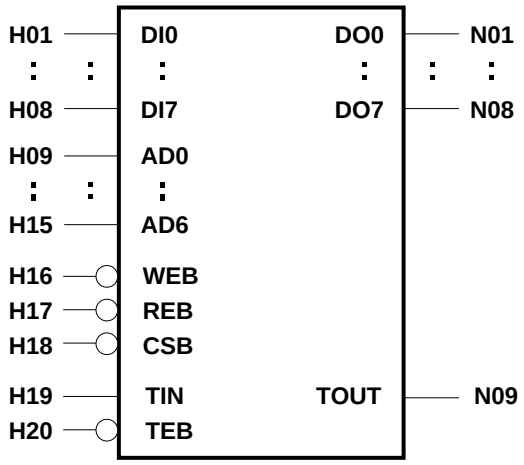
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.478**		
Address access time	**t_{ACA}**			**8.478**
Address output hold time	**t_{OH}**	**2.580**		
CSB access time	**t_{CSC}**			**2.934**
CSB output hold time	**t_{CSL}**	**0.948**		**2.844**
CSB output set time	**t_{CLL}**	**0.978**		
REB access time	**t_{REC}**			**2.934**
REB output hold time	**t_{REL}**	**0.948**		**2.844**
REB output set time	**t_{RLL}**	**0.978**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.482**		
CSB-WEB reset time	**t_{CWR}**	**4.981**		
Write pulse width	**t_{WP}**	**4.981**		
Address setup time	**t_{AS}**	**6.722**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.375**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**3.222**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB8D	**128 words × 8 bits Single-port RAM**	**K14D × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD6 (LH)		4.66	
:	:	:	:	:	:	→DO0 to DO7 (HH)		4.70	
H08	DI7	2.1	N08	DO7	32.0	(HL)		4.30	
H09	AD0	2.1	N09	TOUT	34.0	(LL)		4.26	
:	:	:							
H15	AD6	2.1				CSB (LH)		1.70	
H16	WEB	2.1				→DO0 to DO7 (HL)		1.65	
H17	REB	1.0							
H18	CSB	1.0				REB (LH)		1.70	
H19	TIN	2.1				→DO0 to DO7 (HL)		1.65	
H20	TEB	4.1							
						DI0 to DI7 (HH)		2.86	
						→DO0 to DO7 (LL)		2.61	

Equivalent Cells	3735

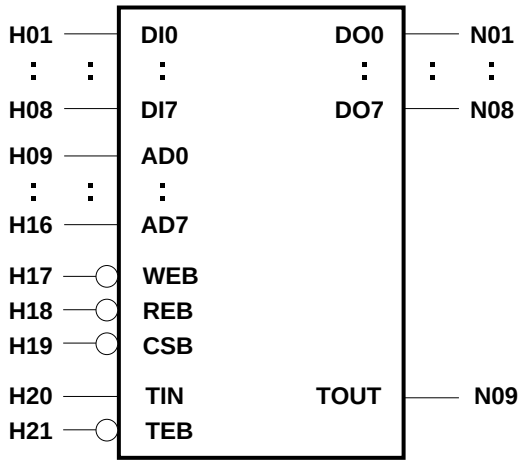
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.460**		
Address access time	**t_{ACA}**			**8.460**
Address output hold time	**t_{OH}**	**2.556**		
CSB access time	**t_{CSC}**			**3.060**
CSB output hold time	**t_{CSL}**	**0.990**		**3.060**
CSB output set time	**t_{CLL}**	**1.020**		
REB access time	**t_{REC}**			**3.060**
REB output hold time	**t_{REL}**	**0.990**		**2.970**
REB output set time	**t_{RLL}**	**1.020**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**3.402**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB8F	**256 words × 8 bits Single-port RAM**	**K18F × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD6 (LH)		4.76	
:	:	:	:	:	:	→DO0 to DO7 (HH)		5.02	
H08	DI7	2.1	N08	DO7	32.0	(HL)		4.54	
H09	AD0	2.1	N09	TOUT	34.0	(LL)		4.48	
:	:	:				CSB (LH)		2.00	
H16	AD7	2.1				→DO0 to DO7 (HL)		1.83	
H17	WEB	2.1				REB (LH)		2.00	
H18	REB	1.0				→DO0 to DO7 (HL)		1.83	
H19	CSB	1.0				DI0 to DI7 (HH)		2.95	
H20	TIN	2.1				→DO0 to DO7 (LL)		2.71	
H21	TEB	4.1							

Equivalent Cells	6307

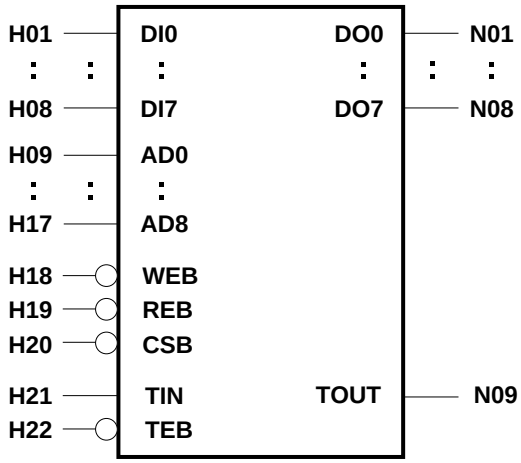
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.036**		
Address access time	**t_{ACA}**			**9.036**
Address output hold time	**t_{OH}**	**2.688**		
CSB access time	**t_{CSC}**			**3.600**
CSB output hold time	**t_{CSL}**	**1.098**		**3.294**
CSB output set time	**t_{CLL}**	**1.200**		
REB access time	**t_{REC}**			**3.600**
REB output hold time	**t_{REL}**	**1.098**		**3.294**
REB output set time	**t_{RLL}**	**1.200**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**3.888**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB8H	**512 words × 8 bits Single-port RAM**	**K18F × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD6 (LH)		5.29	
:	:	:	:	:	:	→DO0 to DO7 (HH)		5.31	
H08	DI7	2.1	N08	DO7	32.0	(HL)		2.61	
H09	AD0	2.1	N09	TOUT	34.0	(LL)		4.90	
:	:	:				CSB (LH)		2.46	
H17	AD6	2.1				→DO0 to DO7 (HL)		2.33	
H16	WEB	2.1				REB (LH)		2.32	
H17	REB	1.0				→DO0 to DO7 (HL)		2.23	
H18	CSB	2.1				DI0 to DI7 (HH)		3.24	
H19	TIN	2.1				→DO0 to DO7 (LL)		3.14	
H20	TEB	4.1							

Equivalent Cells	12330

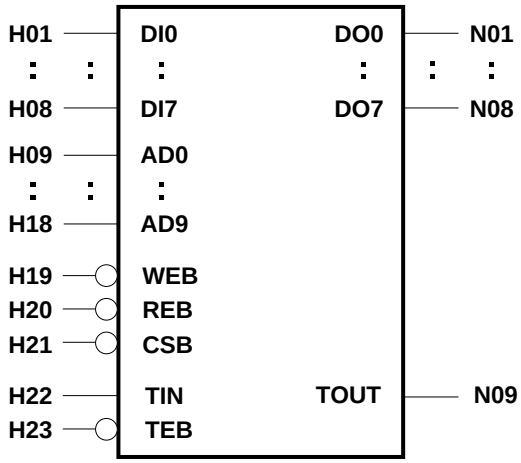
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.558**		
Address access time	**t_{ACA}**			**9.558**
Address output hold time	**t_{OH}**	**1.566**		
CSB access time	**t_{CSC}**			**4.428**
CSB output hold time	**t_{CSL}**	**1.398**		**4.194**
CSB output set time	**t_{CLL}**	**1.476**		
REB access time	**t_{REC}**			**4.176**
REB output hold time	**t_{REL}**	**1.338**		**4.014**
REB output set time	**t_{RLL}**	**1.392**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**4.446**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RB8M	**1K words × 8 bits Single-port RAM**	**K18F × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	24.0
:	:	:	:	:	:
H08	DI7	2.1	N08	DO7	24.0
H09	AD0	2.1	N09	TOUT	34.0
:	:	:			
H18	AD9	2.1			
H19	WEB	2.1			
H20	REB	1.0			
H21	CSB	1.0			
H22	TIN	2.1			
H23	TEB	4.1			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
AD0 to AD9	(LH)		5.55	
→DO0 to DO7	(HH)		5.54	
	(HL)		3.22	
	(LL)		5.35	
CSB	(LH)		3.43	
→DO0 to DO7	(HL)		3.11	
REB	(LH)		2.52	
→DO0 to DO7	(HL)		2.63	
DI0 to DI7	(HH)		3.47	
→DO0 to DO7	(LL)		3.58	

Equivalent Cells	24310

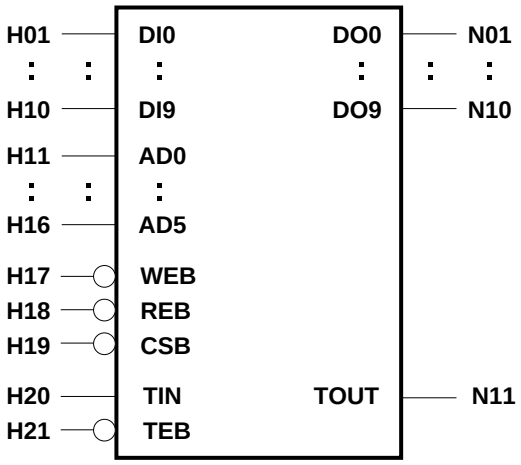
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.990**		
Address access time	**t_{ACA}**			**9.990**
Address output hold time	**t_{OH}**	**1.932**		
CSB access time	**t_{CSC}**			**6.174**
CSB output hold time	**t_{CSL}**	**1.866**		**5.598**
CSB output set time	**t_{CLL}**	**2.058**		
REB access time	**t_{REC}**			**4.536**
REB output hold time	**t_{REL}**	**1.578**		**4.734**
REB output set time	**t_{RLL}**	**1.512**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**4.968**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBAB	**64 words × 10 bits Single-port RAM**	**K1AB × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD5 (LH)		4.76	
:	:	:	:	:	:	→DO0 to DO9 (HH)		4.82	
H10	DI9	2.1	N10	DO9	32.0	(HL)		4.40	
H11	AD0	2.1	N11	TOUT	34.0	(LL)		4.34	
:	:	:							
H16	AD5	2.1				CSB (LH)		1.67	
H17	WEB	2.1				→DO0 to DO9 (HL)		1.60	
H18	REB	1.0							
H19	CSB	1.0				REB (LH)		1.67	
H20	TIN	2.1				→DO0 to DO9 (HL)		1.60	
H21	TEB	4.1							
						DI0 to DI9 (HH)		2.69	
						→DO0 to DO9 (LL)		2.47	

Equivalent Cells	2338

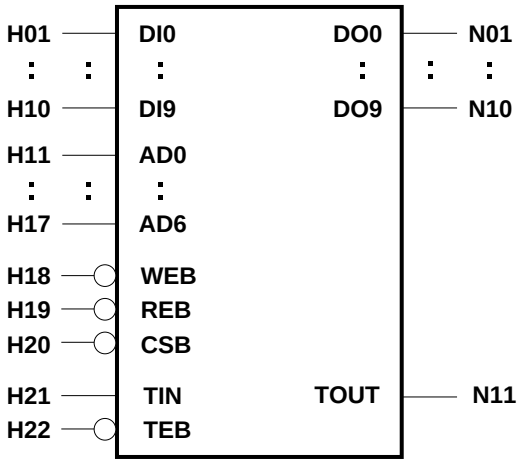
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.676**		
Address access time	**t_{ACA}**			**8.676**
Address output hold time	**t_{OH}**	**2.604**		
CSB access time	**t_{CSC}**			**3.006**
CSB output hold time	**t_{CSL}**	**0.960**		**2.880**
CSB output set time	**t_{CLL}**	**1.002**		
REB access time	**t_{REC}**			**3.006**
REB output hold time	**t_{REL}**	**0.960**		**2.880**
REB output set time	**t_{RLL}**	**1.002**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**3.294**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBAD	**128 words × 10 bits Single-port RAM**	**K1AB × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H10	DI9	2.1	N10	DO9	32.0
H11	AD0	2.1	N11	TOUT	34.0
:	:	:			
H17	AD6	2.1			
H18	WEB	2.1			
H19	REB	1.0			
H20	CSB	2.1			
H21	TIN	2.1			
H22	TEB	4.1			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
AD0 to AD6	(LH)		5.08	
→DO0 to DO9	(HH)		5.10	
	(HL)		2.38	
	(LL)		4.76	
CSB	(LH)		2.12	
→DO0 to DO9	(HL)		2.09	
REB	(LH)		1.97	
→DO0 to DO9	(HL)		1.99	
DI0 to DI9	(HH)		2.97	
→DO0 to DO9	(LL)		2.89	

Equivalent Cells	4404

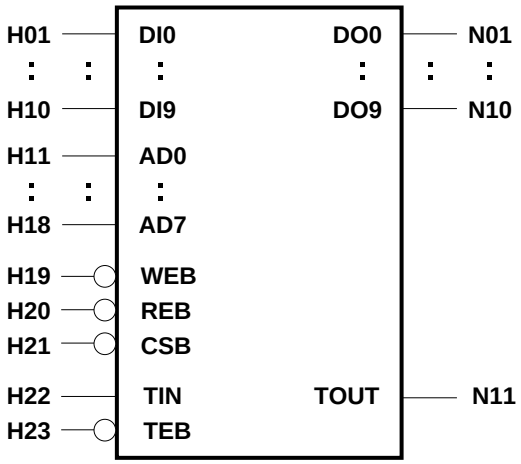
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.180**		
Address access time	**t_{ACA}**			**9.180**
Address output hold time	**t_{OH}**	**1.428**		
CSB access time	**t_{CSC}**			**3.816**
CSB output hold time	**t_{CSL}**	**1.254**		**3.762**
CSB output set time	**t_{CLL}**	**1.272**		
REB access time	**t_{REC}**			**3.546**
REB output hold time	**t_{REL}**	**1.194**		**3.582**
REB output set time	**t_{RLL}**	**1.182**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**3.834**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBAF	**256 words × 10 bits Single-port RAM**	**K1AB × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	24.0	AD0 to AD7 (LH)		5.31	
:	:	:	:	:	:	→DO0 to DO9 (HH)		5.31	
H10	DI9	2.1	N10	DO9	24.0	(HL)		2.93	
H11	AD0	2.1	N11	TOUT	34.0	(LL)		5.16	
:	:	:							
H18	AD7	2.1				CSB (LH)		3.02	
H19	WEB	2.1				→DO0 to DO9 (HL)		2.83	
H20	REB	1.0							
H21	CSB	1.0				REB (LH)		2.16	
H22	TIN	2.1				→DO0 to DO9 (HL)		2.37	
H23	TEB	4.1							
						DI0 to DI9 (HH)		3.18	
						→DO0 to DO9 (LL)		3.30	

Equivalent Cells	8495

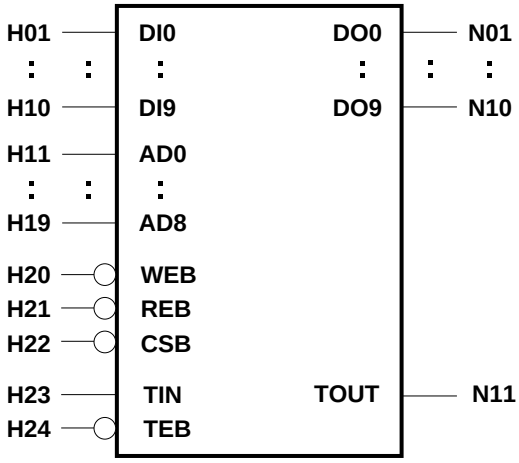
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.558**		
Address access time	**t_{ACA}**			**9.558**
Address output hold time	**t_{OH}**	**1.758**		
CSB access time	**t_{CSC}**			**5.436**
CSB output hold time	**t_{CSL}**	**1.698**		**5.094**
CSB output set time	**t_{CLL}**	**1.812**		
REB access time	**t_{REC}**			**3.888**
REB output hold time	**t_{REL}**	**1.422**		**4.266**
REB output set time	**t_{RLL}**	**1.296**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**4.338**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBAH	**512 words × 10 bits Single-port RAM**	**K1AB × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD8 (LH)		5.88	
:	:	:	:	:	:	→DO0 to DO9 (HH)		5.79	
H10	DI9	2.1	N10	DO9	32.0	(HL)		3.64	
H11	AD0	2.1	N11	TOUT	34.0	(LL)		5.77	
:	:	:							
H19	AD8	2.1				CSB (LH)		3.56	
H20	WEB	2.1				→DO0 to DO9 (HL)		3.37	
H21	REB	1.0							
H22	CSB	2.1				REB (LH)		2.62	
H23	TIN	2.1				→DO0 to DO9 (HL)		2.91	
H24	TEB	4.1							
						DI0 to DI9 (HH)		3.66	
						→DO0 to DO9 (LL)		3.91	

Equivalent Cells	16689

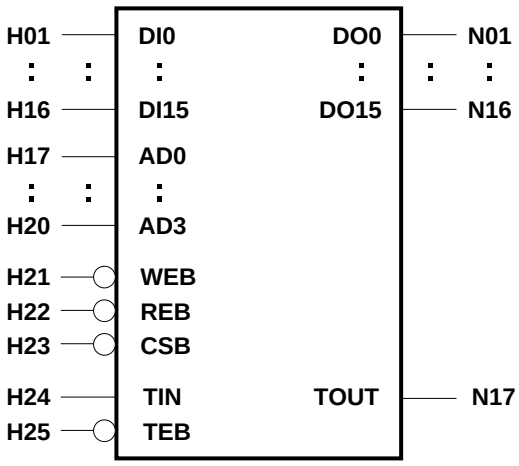
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.584**		
Address access time	**t_{ACA}**			**10.584**
Address output hold time	**t_{OH}**	**2.184**		
CSB access time	**t_{CSC}**			**6.408**
CSB output hold time	**t_{CSL}**	**2.022**		**6.066**
CSB output set time	**t_{CLL}**	**2.136**		
REB access time	**t_{REC}**			**4.716**
REB output hold time	**t_{REL}**	**1.746**		**5.238**
REB output set time	**t_{RLL}**	**1.572**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**5.436**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBC7	**16 words × 16 bits Single-port RAM**	**K147 × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD3 (LH)		4.37	
:	:	:	:	:	:	→DO0 to DO15 (HH)		4.38	
H16	DI15	2.1	N16	DO15	32.0	(HL)		3.87	
H17	AD0	2.1	N17	TOUT	34.0	(LL)		3.86	
:	:	:							
H20	AD3	2.1				CSB (LH)		1.65	
H21	WEB	2.1				→DO0 to DO15 (HL)		1.65	
H22	REB	1.0							
H23	CSB	1.0				REB (LH)		1.65	
H24	TIN	2.1				→DO0 to DO15 (HL)		1.65	
H25	TEB	2.0							
						DI0 to DI15 (HH)		2.53	
						→DO0 to DO15 (LL)		2.38	

Equivalent Cells	1722

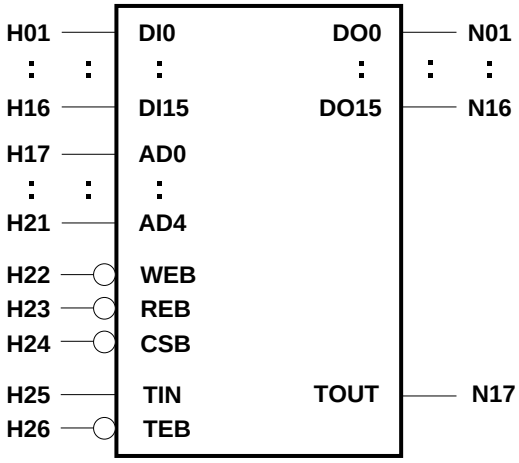
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.884**		
Address access time	**t_{ACA}**			**7.884**
Address output hold time	**t_{OH}**	**2.316**		
CSB access time	**t_{CSC}**			**2.970**
CSB output hold time	**t_{CSL}**	**0.990**		**2.970**
CSB output set time	**t_{CLL}**	**0.990**		
REB access time	**t_{REC}**			**2.970**
REB output hold time	**t_{REL}**	**0.990**		**2.970**
REB output set time	**t_{RLL}**	**0.990**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.630**		
CSB-WEB reset time	**t_{CWR}**	**4.819**		
Write pulse width	**t_{WP}**	**4.819**		
Address setup time	**t_{AS}**	**6.032**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.520**		
Input data hold time	**t_{DH}**	**3.144**		
WEB access time	**t_{WEC}**			**3.402**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBC9	**32 words × 16 bits Single-port RAM**	**K149 × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD4 (LH)		4.45	
:	:	:	:	:	:	→DO0 to DO15 (HH)		4.46	
H16	DI15	2.1	N16	DO15	32.0	(HL)		4.04	
H17	AD0	2.1	N17	TOUT	34.0	(LL)		4.03	
:	:	:							
H21	AD4	2.1				CSB (LH)		1.69	
H22	WEB	2.1				→DO0 to DO15 (HL)		1.68	
H23	REB	1.0							
H24	CSB	1.0				REB (LH)		1.69	
H25	TIN	2.1				→DO0 to DO15 (HL)		1.68	
H26	TEB	2.0							
						DI0 to DI15 (HH)		2.55	
						→DO0 to DO15 (LL)		2.38	

Equivalent Cells	2710

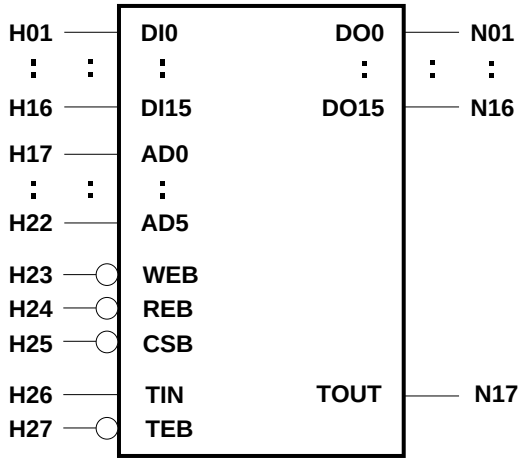
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.028**		
Address access time	**t_{ACA}**			**8.028**
Address output hold time	**t_{OH}**	**2.418**		
CSB access time	**t_{CSC}**			**3.042**
CSB output hold time	**t_{CSL}**	**1.008**		**3.024**
CSB output set time	**t_{CLL}**	**1.014**		
REB access time	**t_{REC}**			**3.042**
REB output hold time	**t_{REL}**	**1.008**		**3.024**
REB output set time	**t_{RLL}**	**1.014**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.464**		
CSB-WEB reset time	**t_{CWR}**	**4.59**		
Write pulse width	**t_{WP}**	**4.59**		
Address setup time	**t_{AS}**	**6.096**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.187**		
Input data hold time	**t_{DH}**	**3.114**		
WEB access time	**t_{WEC}**			**3.438**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBCB	**64 words × 16 bits Single-port RAM**	**K18B × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H16	DI15	2.1	N16	DO15	32.0
H17	AD0	2.1	N17	TOUT	34.0
:	:	:			
H22	AD5	2.1			
H23	WEB	2.1			
H24	REB	1.0			
H25	CSB	1.0			
H26	TIN	2.1			
H27	TEB	2.0			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
AD0 to AD5	(LH)		4.71	
→DO0 to DO15	(HH)		4.75	
	(HL)		4.40	
	(LL)		4.36	
CSB	(LH)		1.68	
→DO0 to DO15	(HL)		1.62	
REB	(LH)		1.68	
→DO0 to DO15	(HL)		1.62	
DI0 to DI15	(HH)		2.71	
→DO0 to DO15	(LL)		2.48	

Equivalent Cells	3765

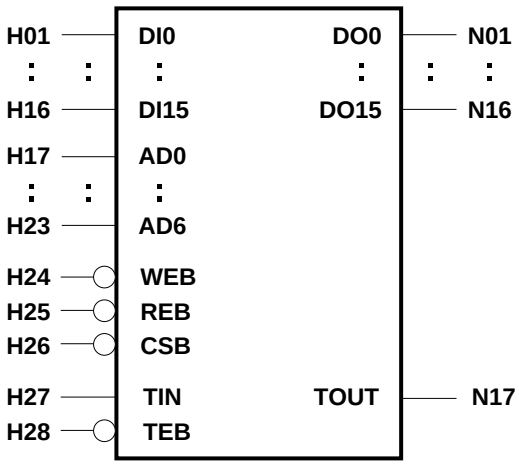
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.550**		
Address access time	**t_{ACA}**			**8.550**
Address output hold time	**t_{OH}**	**2.616**		
CSB access time	**t_{CSC}**			**3.024**
CSB output hold time	**t_{CSL}**	**0.972**		**2.916**
CSB output set time	**t_{CLL}**	**1.008**		
REB access time	**t_{REC}**			**3.024**
REB output hold time	**t_{REL}**	**0.972**		**2.916**
REB output set time	**t_{RLL}**	**1.008**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.482**		
CSB-WEB reset time	**t_{CWR}**	**4.981**		
Write pulse width	**t_{WP}**	**4.981**		
Address setup time	**t_{AS}**	**6.722**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.375**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**3.330**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBCD	**128 words × 16 bits Single-port RAM**	**K14D × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H16	DI15	2.1	N16	DO15	32.0
H17	AD0	2.1	N17	TOUT	34.0
:	:	:			
H23	AD6	2.1			
H24	WEB	2.1			
H25	REB	1.0			
H26	CSB	1.0			
H27	TIN	2.1			
H28	TEB	4.1			

Switching speed

Path	t_{LD0} (ns)		
IN → OUT	MIN.	TYP.	MAX.
AD0 to AD6 (LH)		4.78	
→DO0 to DO15 (HH)		4.79	
(HL)		4.40	
(LL)		4.39	
CSB (LH)		1.79	
→DO0 to DO15 (HL)		1.76	
REB (LH)		1.79	
→DO0 to DO15 (HL)		1.76	
DI0 to DI15 (HH)		2.86	
→DO0 to DO15 (LL)		2.62	

Equivalent Cells	7236

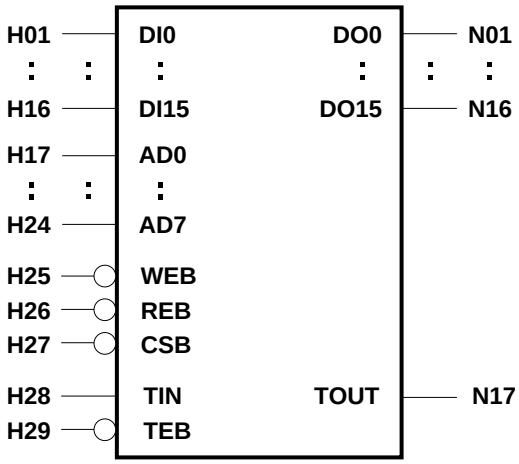
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.622**		
Address access time	**t_{ACA}**			**8.622**
Address output hold time	**t_{OH}**	**2.634**		
CSB access time	**t_{CSC}**			**3.222**
CSB output hold time	**t_{CSL}**	**1.056**		**3.168**
CSB output set time	**t_{CLL}**	**1.074**		
REB access time	**t_{REC}**			**3.222**
REB output hold time	**t_{REL}**	**1.056**		**3.168**
REB output set time	**t_{RLL}**	**1.074**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**3.636**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBCF	**256 words × 16 bits Single-port RAM**	**K18F × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD7 (LH)		5.03	
:	:	:	:	:	:	→DO0 to DO15 (HH)		5.07	
H16	DI15	2.1	N16	DO15	32.0	(HL)		4.60	
H17	AD0	2.1	N17	TOUT	34.0	(LL)		4.56	
:	:	:							
H24	AD7	2.1				CSB (LH)		2.06	
H25	WEB	2.1				→DO0 to DO15 (HL)		1.88	
H26	REB	1.0							
H27	CSB	1.0				REB (LH)		2.06	
H28	TIN	2.1				→DO0 to DO15 (HL)		1.88	
H29	TEB	4.1							
						DI0 to DI15 (HH)		2.95	
						→DO0 to DO15 (LL)		2.72	

Equivalent Cells	12367

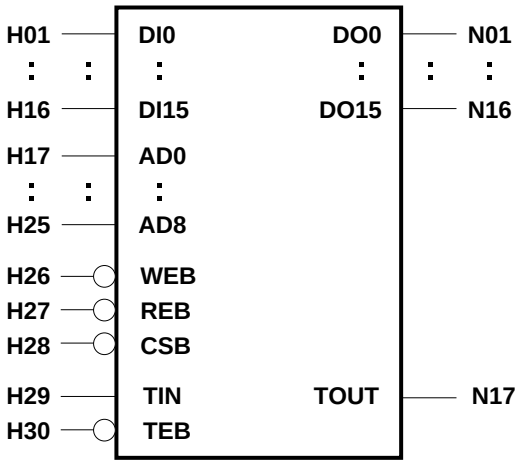
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.126**		
Address access time	**t_{ACA}**			**9.126**
Address output hold time	**t_{OH}**	**2.736**		
CSB access time	**t_{CSC}**			**3.708**
CSB output hold time	**t_{CSL}**	**1.128**		**3.384**
CSB output set time	**t_{CLL}**	**1.236**		
REB access time	**t_{REC}**			**3.708**
REB output hold time	**t_{REL}**	**1.128**		**3.384**
REB output set time	**t_{RLL}**	**1.236**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**4.032**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBCH	**512 words × 16 bits Single-port RAM**	**K18F × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H16	DI15	2.1	N16	DO15	32.0
H17	AD0	2.1	N17	TOUT	34.0
:	:	:			
H25	AD8	2.1			
H26	WEB	2.1			
H27	REB	1.0			
H28	CSB	2.1			
H29	TIN	2.1			
H30	TEB	4.1			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
AD0 to AD8	(LH)		5.46	
→DO0 to DO15	(HH)		5.43	
	(HL)		2.69	
	(LL)		5.07	
CSB	(LH)		2.56	
→DO0 to DO15	(HL)		2.41	
REB	(LH)		2.43	
→DO0 to DO15	(HL)		2.36	
DI0 to DI15	(HH)		3.26	
→DO0 to DO15	(LL)		3.16	

Equivalent Cells	24366

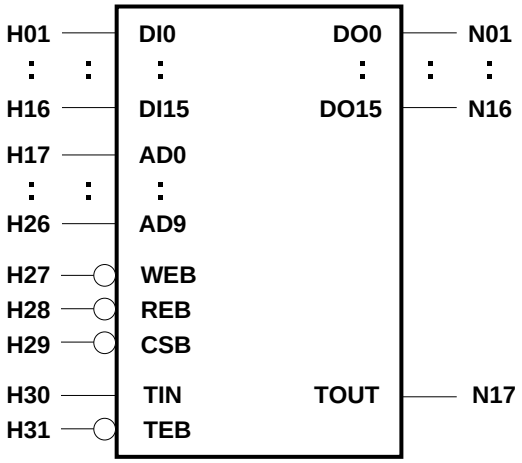
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.828**		
Address access time	**t_{ACA}**			**9.828**
Address output hold time	**t_{OH}**	**1.614**		
CSB access time	**t_{CSC}**			**4.608**
CSB output hold time	**t_{CSL}**	**1.446**		**4.338**
CSB output set time	**t_{CLL}**	**1.536**		
REB access time	**t_{REC}**			**4.374**
REB output hold time	**t_{REL}**	**1.416**		**4.248**
REB output set time	**t_{RLL}**	**1.458**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**4.752**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBCM	**1K words × 16 bits Single-port RAM**	**K18F × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD9 (LH)		5.91	
:	:	:	:	:	:	→DO0 to DO15 (HH)		5.81	
H16	DI15	2.1	N16	DO15	32.0	(HL)		3.51	
H17	AD0	2.1	N17	TOUT	34.0	(LL)		5.71	
:	:	:							
H26	AD9	2.1				CSB (LH)		3.57	
H27	WEB	2.1				→DO0 to DO15 (HL)		3.26	
H28	REB	1.0							
H29	CSB	1.0				REB (LH)		2.75	
H30	TIN	2.1				→DO0 to DO15 (HL)		2.91	
H31	TEB	4.1							
						DI0 to DI15 (HH)		3.50	
						→DO0 to DO15 (LL)		3.61	

Equivalent Cells	48372

★

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.638**		
Address access time	**t_{ACA}**			**10.638**
Address output hold time	**t_{OH}**	**2.106**		
CSB access time	**t_{CSC}**			**6.426**
CSB output hold time	**t_{CSL}**	**1.956**		**5.868**
CSB output set time	**t_{CLL}**	**2.142**		
REB access time	**t_{REC}**			**4.950**
REB output hold time	**t_{REL}**	**1.746**		**5.238**
REB output set time	**t_{RLL}**	**1.650**		

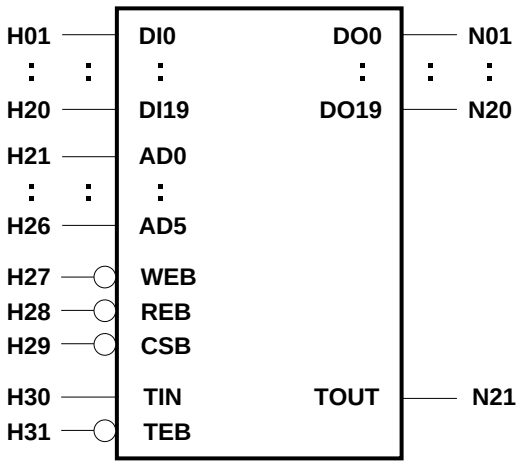
★

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**5.616**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBEB	**64 words × 20 bits Single-port RAM**	**K1AB × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD5 (LH)		4.82	
:	:	:	:	:	:	→DO0 to DO19 (HH)		4.86	
H20	DI19	2.1	N20	DO19	32.0	(HL)		4.44	
H21	AD0	2.1	N21	TOUT	34.0	(LL)		4.40	
:	:	:							
H26	AD5	2.1				CSB (LH)		1.71	
H27	WEB	2.1				→DO0 to DO19 (HL)		1.64	
H28	REB	1.0							
H29	CSB	1.0				REB (LH)		1.71	
H30	TIN	2.1				→DO0 to DO19 (HL)		1.64	
H31	TEB	2.0							
						DI0 to DI19 (HH)		2.70	
						→DO0 to DO19 (LL)		2.48	

Equivalent Cells	4463

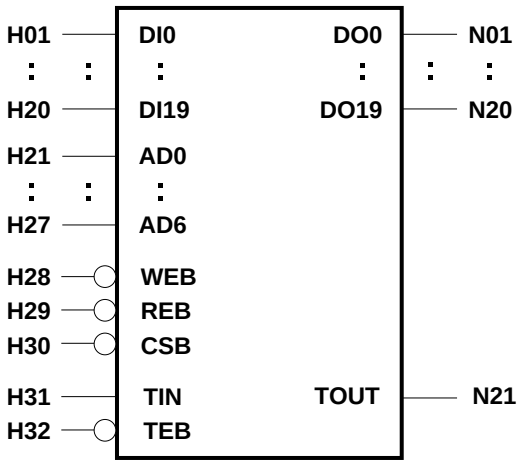
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.748**		
Address access time	**t_{ACA}**			**8.748**
Address output hold time	**t_{OH}**	**2.640**		
CSB access time	**t_{CSC}**			**3.078**
CSB output hold time	**t_{CSL}**	**0.948**		**2.952**
CSB output set time	**t_{CLL}**	**1.026**		
REB access time	**t_{REC}**			**3.078**
REB output hold time	**t_{REL}**	**0.984**		**2.952**
REB output set time	**t_{RLL}**	**1.026**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**3.420**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBED	**128 words × 20 bits Single-port RAM**	**K1AB × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD6 (LH)		5.22	
:	:	:	:	:	:	→DO0 to DO19 (HH)		5.20	
H20	DI19	2.1	N20	DO19	32.0	(HL)		2.44	
H21	AD0	2.1	N21	TOUT	34.0	(LL)		4.89	
:	:	:							
H27	AD6	2.1				CSB (LL)		2.20	
H28	WEB	2.1				→DO0 to DO19 (LH)		2.16	
H29	REB	1.0				(HL)			
H30	CSB	2.1							
H31	TIN	2.1				REB (LH)		2.07	
H32	TEB	2.0				→DO0 to DO19 (HL)		2.10	
						DI0 to DI19 (HH)		2.99	
						→DO0 to DO19 (LL)		2.90	

Equivalent Cells	8574

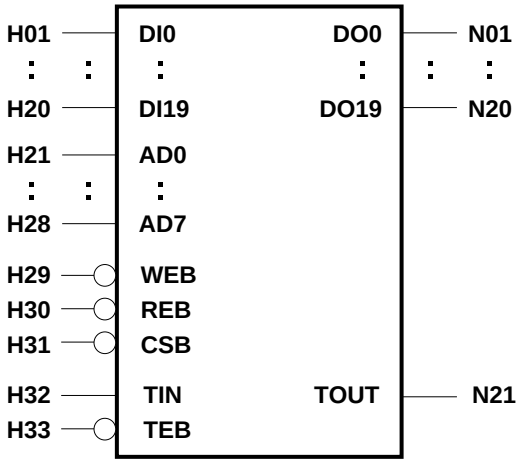
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.396**		
Address access time	**t_{ACA}**			**9.396**
Address output hold time	**t_{OH}**	**1.464**		
CSB access time	**t_{CSC}**			**3.960**
CSB output hold time	**t_{CSL}**	**1.296**		**3.888**
CSB output set time	**t_{CLL}**	**1.320**		
REB access time	**t_{REC}**			**3.726**
REB output hold time	**t_{REL}**	**1.260**		**3.780**
REB output set time	**t_{RLL}**	**1.242**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**4.086**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBEF	**256 words × 20 bits Single-port RAM**	**K1AB × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD7 (LH)		5.61	
:	:	:	:	:	:	→DO0 to DO19 (HH)		5.54	
H20	DI19	2.1	N20	DO19	32.0	(HL)		3.17	
H21	AD0	2.1	N21	TOUT	34.0	(LL)		5.45	
:	:	:							
H28	AD7	2.1				CSB (LH)		3.13	
H29	WEB	2.1				→DO0 to DO19 (HL)		2.94	
H30	REB	1.0							
H31	CSB	1.0				REB (LH)		2.35	
H32	TIN	2.1				→DO0 to DO19 (HL)		2.59	
H33	TEB	4.1							
						DI0 to DI19 (HH)		3.21	
						→DO0 to DO19 (LL)		3.32	

Equivalent Cells	16751

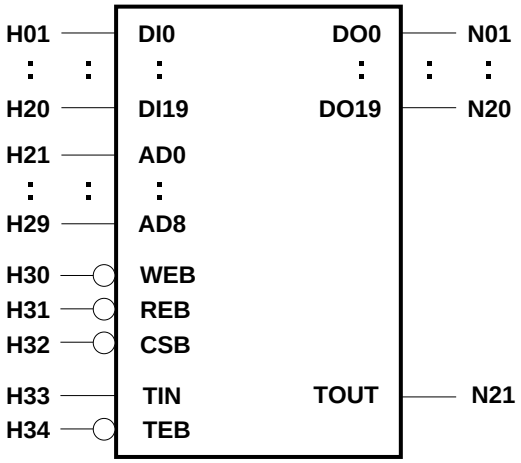
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.098**		
Address access time	**t_{ACA}**			**10.098**
Address output hold time	**t_{OH}**	**1.902**		
CSB access time	**t_{CSC}**			**5.634**
CSB output hold time	**t_{CSL}**	**1.764**		**5.292**
CSB output set time	**t_{CLL}**	**1.878**		
REB access time	**t_{REC}**			**4.230**
REB output hold time	**t_{REL}**	**1.554**		**4.662**
REB output set time	**t_{RLL}**	**1.410**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**4.860**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
★ **RBEH**	**512 words × 20 bits Single-port RAM**	**K1AB × 16**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

★

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD8 (LH)		6.55	
:	:	:	:	:	:	→DO0 to DO19 (HH)		6.27	
H20	DI19	2.1	N20	DO19	32.0	(HL)		3.80	
H21	AD0	2.1	N21	TOUT	34.0	(LL)		6.45	
:	:	:							
H29	AD8	2.1				CSB (LH)		3.72	
H30	WEB	2.1				→DO0 to DO19 (HL)		3.52	
H31	REB	1.0							
H32	CSB	2.1				REB (LH)		3.02	
H33	TIN	2.1				→DO0 to DO19 (HL)		3.43	
H34	TEB	4.1							
						DI0 to DI19 (HH)		3.70	
						→DO0 to DO19 (LL)		3.98	

Equivalent Cells	33080

★

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**11.790**		
Address access time	**t_{ACA}**			**11.790**
Address output hold time	**t_{OH}**	**2.280**		
CSB access time	**t_{CSC}**			**6.696**
CSB output hold time	**t_{CSL}**	**2.112**		**6.336**
CSB output set time	**t_{CLL}**	**2.232**		
REB access time	**t_{REC}**			**5.436**
REB output hold time	**t_{REL}**	**2.058**		**6.174**
REB output set time	**t_{RLL}**	**1.812**		

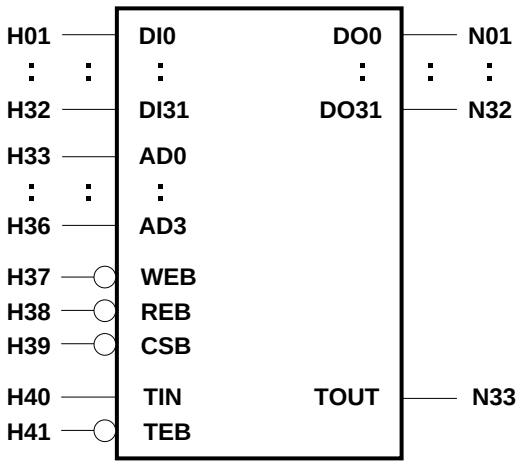
★

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**6.660**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBH7	**16 words × 32 bits Single-port RAM**	**K147 × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H32	DI31	2.1	N32	DO31	32.0
H33	AD0	2.1	N33	TOUT	34.0
:	:	:			
H36	AD3	2.1			
H37	WEB	2.1			
H38	REB	1.0			
H39	CSB	1.0			
H40	TIN	2.1			
H41	TEB	2.0			

Switching speed

Path	t_{LD0} (ns)		
IN → OUT	MIN.	TYP.	MAX.
AD0 to AD3 (LH)		4.59	
→DO0 to DO31 (HH)		4.54	
(HL)		4.04	
(LL)		4.09	
CSB (LH)		1.79	
→DO0 to DO31 (HL)		1.83	
REB (LH)		1.79	
→DO0 to DO31 (HL)		1.83	
DI0 to DI31 (HH)		2.54	
→DO0 to DO31 (LL)		2.39	

Equivalent Cells	3262

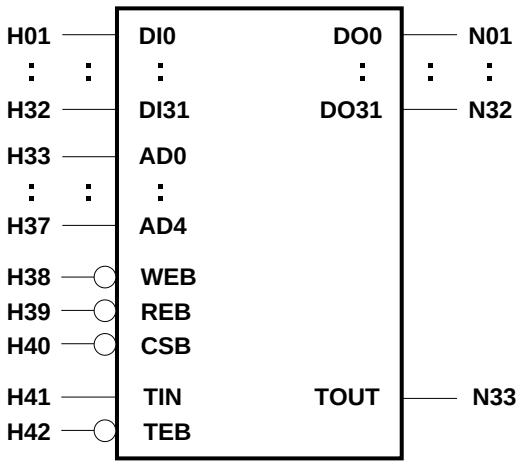
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.262**		
Address access time	**t_{ACA}**			**8.262**
Address output hold time	**t_{OH}**	**2.424**		
CSB access time	**t_{CSC}**			**3.222**
CSB output hold time	**t_{CSL}**	**1.098**		**3.294**
CSB output set time	**t_{CLL}**	**1.074**		
REB access time	**t_{REC}**			**3.222**
REB output hold time	**t_{REL}**	**1.098**		**3.294**
REB output set time	**t_{RLL}**	**1.074**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.630**		
CSB-WEB reset time	**t_{CWR}**	**4.819**		
Write pulse width	**t_{WP}**	**4.819**		
Address setup time	**t_{AS}**	**6.032**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.520**		
Input data hold time	**t_{DH}**	**3.144**		
WEB access time	**t_{WEC}**			**3.816**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBH9	**32 words × 32 bits Single-port RAM**	**K149 × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD4 (LH)		4.70	
:	:	:	:	:	:	→DO0 to DO31 (HH)		4.65	
H32	DI31	2.1	N32	DO31	32.0	(HL)		4.22	
H33	AD0	2.1	N33	TOUT	34.0	(LL)		4.27	
:	:	:							
H37	AD4	2.1				CSB (LH)		1.84	
H38	WEB	2.1				→DO0 to DO31 (HL)		1.86	
H39	REB	1.0							
H40	CSB	1.0				REB (LH)		1.84	
H41	TIN	2.1				→DO0 to DO31 (HL)		1.86	
H42	TEB	2.0							
						DI0 to DI31 (HH)		2.56	
						→DO0 to DO31 (LL)		2.39	

Equivalent Cells	5222

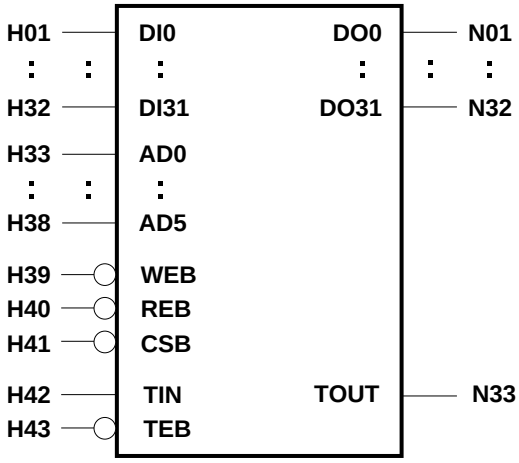
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.460**		
Address access time	**t_{ACA}**			**8.460**
Address output hold time	**t_{OH}**	**2.532**		
CSB access time	**t_{CSC}**			**3.312**
CSB output hold time	**t_{CSL}**	**1.116**		**3.348**
CSB output set time	**t_{CLL}**	**1.104**		
REB access time	**t_{REC}**			**3.312**
REB output hold time	**t_{REL}**	**1.116**		**3.348**
REB output set time	**t_{RLL}**	**1.104**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.464**		
CSB-WEB reset time	**t_{CWR}**	**4.590**		
Write pulse width	**t_{WP}**	**4.590**		
Address setup time	**t_{AS}**	**6.096**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.187**		
Input data hold time	**t_{DH}**	**3.114**		
WEB access time	**t_{WEC}**			**3.888**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBHB	**64 words × 32 bits Single-port RAM**	**K18B × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H32	DI31	2.1	N32	DO31	32.0
H33	AD0	2.1	N33	TOUT	34.0
:	:	:			
H38	AD5	2.1			
H39	WEB	2.1			
H40	REB	1.0			
H41	CSB	1.0			
H42	TIN	2.1			
H43	TEB	2.0			

Switching speed

Path	t_{LD0} (ns)		
IN → OUT	MIN.	TYP.	MAX.
AD0 to AD5 (LH)		4.84	
→DO0 to DO31 (HH)		4.85	
(HL)		4.50	
(LL)		4.49	
CSB (LH)		1.76	
→DO0 to DO31 (HL)		1.73	
REB (LH)		1.76	
→DO0 to DO31 (HL)		1.73	
DI0 to DI31 (HH)		2.71	
→DO0 to DO31 (LL)		2.48	

Equivalent Cells	7318

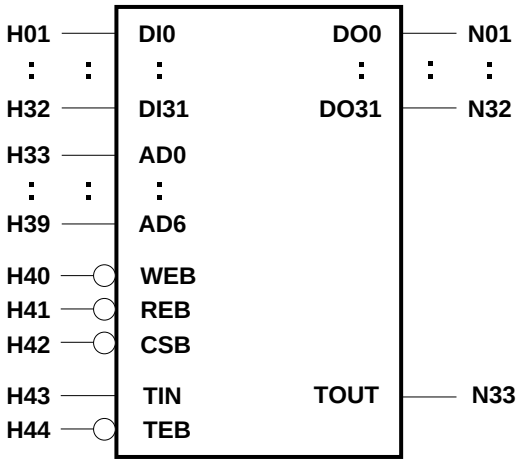
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.730**		
Address access time	**t_{ACA}**			**8.730**
Address output hold time	**t_{OH}**	**2.694**		
CSB access time	**t_{CSC}**			**3.168**
CSB output hold time	**t_{CSL}**	**1.038**		**3.114**
CSB output set time	**t_{CLL}**	**1.056**		
REB access time	**t_{REC}**			**3.168**
REB output hold time	**t_{REL}**	**1.038**		**3.114**
REB output set time	**t_{RLL}**	**1.056**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.482**		
CSB-WEB reset time	**t_{CWR}**	**4.981**		
Write pulse width	**t_{WP}**	**4.981**		
Address setup time	**t_{AS}**	**6.722**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.375**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**3.564**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBHD	**128 words × 32 bits Single-port RAM**	**K14D × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.1	N01	DO0	32.0
:	:	:	:	:	:
H32	DI31	2.1	N32	DO31	32.0
H33	AD0	2.1	N33	TOUT	34.0
:	:	:			
H39	AD6	2.1			
H40	WEB	2.1			
H41	REB	1.0			
H42	CSB	1.0			
H43	TIN	2.1			
H44	TEB	4.1			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
AD0 to AD6	(LH)		5.08	
→DO0 to DO31	(HH)		5.01	
	(HL)		4.61	
	(LL)		4.68	
CSB	(LH)		1.97	
→DO0 to DO31	(HL)		1.99	
REB	(LH)		1.97	
→DO0 to DO31	(HL)		1.99	
DI0 to DI31	(HH)		2.87	
→DO0 to DO31	(LL)		2.62	

Equivalent Cells	14245

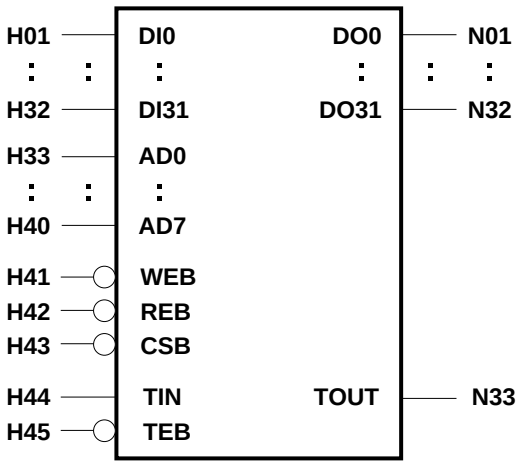
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.144**		
Address access time	**t_{ACA}**			**9.144**
Address output hold time	**t_{OH}**	**2.766**		
CSB access time	**t_{CSC}**			**3.546**
CSB output hold time	**t_{CSL}**	**1.194**		**3.582**
CSB output set time	**t_{CLL}**	**1.182**		
REB access time	**t_{REC}**			**3.546**
REB output hold time	**t_{REL}**	**1.194**		**3.582**
REB output set time	**t_{RLL}**	**1.182**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.114**		
CSB-WEB reset time	**t_{CWR}**	**5.056**		
Write pulse width	**t_{WP}**	**5.056**		
Address setup time	**t_{AS}**	**6.281**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.540**		
Input data hold time	**t_{DH}**	**2.956**		
WEB access time	**t_{WEC}**			**4.158**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBHF	**256 words × 32 bits Single-port RAM**	**K18F × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD7 (LH)		5.20	
:	:	:	:	:	:	→DO0 to DO31 (HH)		5.19	
H32	DI31	2.1	N32	DO31	32.0	(HL)		4.71	
H33	AD0	2.1	N33	TOUT	34.0	(LL)		4.72	
:	:	:							
H40	AD7	2.1				CSB (LH)		2.17	
H41	WEB	2.1				→DO0 to DO31 (HL)		2.01	
H42	REB	1.0							
H43	CSB	1.0				REB (LH)		2.17	
H44	TIN	2.1				→DO0 to DO31 (HL)		2.01	
H45	TEB	4.1							
						DI0 to DI31 (HH)		2.96	
						→DO0 to DO31 (LL)		2.72	

Equivalent Cells	24442

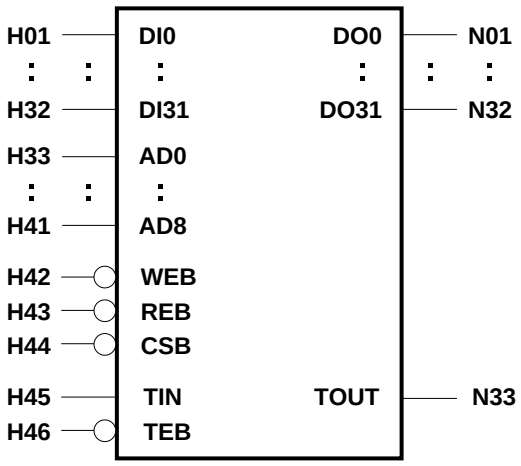
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.360**		
Address access time	**t_{ACA}**			**9.360**
Address output hold time	**t_{OH}**	**2.826**		
CSB access time	**t_{CSC}**			**3.906**
CSB output hold time	**t_{CSL}**	**1.206**		**3.618**
CSB output set time	**t_{CLL}**	**1.302**		
REB access time	**t_{REC}**			**3.906**
REB output hold time	**t_{REL}**	**1.206**		**3.618**
REB output set time	**t_{RLL}**	**1.302**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**4.338**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBHH	**512 words × 32 bits Single-port RAM**	**K18F × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD8 (LH)		5.81	
:	:	:	:	:	:	→DO0 to DO31 (HH)		5.69	
H32	DI31	2.1	N32	DO31	32.0	(HL)		2.83	
H33	AD0	2.1	N33	TOUT	34.0	(LL)		5.43	
:	:	:							
H41	AD8	2.1				CSB (LH)		2.75	
H42	WEB	2.1				→DO0 to DO31 (HL)		2.55	
H43	REB	1.0							
H44	CSB	2.1				REB (LH)		2.65	
H45	TIN	2.1				→DO0 to DO31 (HL)		2.63	
H46	TEB	4.1							
						DI0 to DI31 (HH)		3.26	
						→DO0 to DO31 (LL)		3.18	

Equivalent Cells	48463

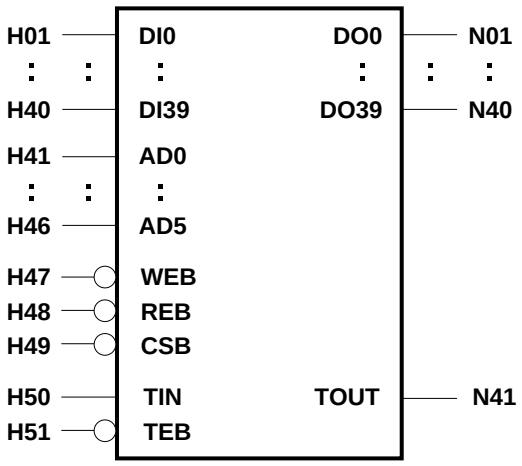
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.458**		
Address access time	**t_{ACA}**			**10.458**
Address output hold time	**t_{OH}**	**1.698**		
CSB access time	**t_{CSC}**			**4.950**
CSB output hold time	**t_{CSL}**	**1.530**		**4.590**
CSB output set time	**t_{CLL}**	**1.650**		
REB access time	**t_{REC}**			**4.770**
REB output hold time	**t_{REL}**	**1.578**		**4.734**
REB output set time	**t_{RLL}**	**1.590**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**5.382**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBKB	**64 words × 40 bits Single-port RAM**	**K1AB × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD5 (LH)		4.96	
:	:	:	:	:	:	→DO0 to DO39 (HH)		4.96	
H40	DI39	2.1	N40	DO39	32.0	(HL)		4.54	
H41	AD0	2.1	N41	TOUT	34.0	(LL)		4.54	
:	:	:							
H46	AD5	2.1				CSB (LH)		1.81	
H47	WEB	2.1				→DO0 to DO39 (HL)		1.75	
H48	REB	1.0							
H49	CSB	1.0				REB (LH)		1.81	
H50	TIN	2.1				→DO0 to DO39 (HL)		1.75	
H51	TEB	2.0							
						DI0 to DI39 (HH)		2.70	
						→DO0 to DO39 (LL)		2.48	

Equivalent Cells	8704

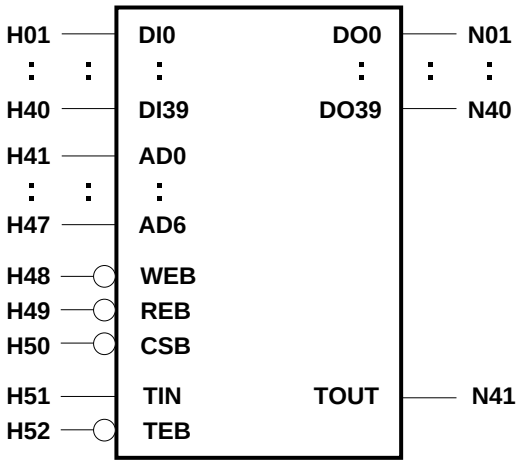
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.928**		
Address access time	**t_{ACA}**			**8.928**
Address output hold time	**t_{OH}**	**2.724**		
CSB access time	**t_{CSC}**			**3.258**
CSB output hold time	**t_{CSL}**	**1.050**		**3.150**
CSB output set time	**t_{CLL}**	**1.086**		
REB access time	**t_{REC}**			**3.258**
REB output hold time	**t_{REL}**	**1.050**		**3.150**
REB output set time	**t_{RLL}**	**1.086**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**3.654**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBKD	**128 words × 40 bits Single-port RAM**	**K1AB × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD6 (LH)		5.51	
:	:	:	:	:	:	→DO0 to DO39 (HH)		5.42	
H40	DI39	2.1	N40	DO39	32.0	(HL)		2.55	
H41	AD0	2.1	N41	TOUT	34.0	(LL)		5.19	
:	:	:							
H47	AD6	2.1				CSB (LH)		2.35	
H48	WEB	2.1				→DO0 to DO39 (HL)		2.27	
H49	REB	1.0							
H50	CSB	2.1				REB (LH)		2.25	
H51	TIN	2.1				→DO0 to DO39 (HL)		2.33	
H52	TEB	2.0							
						DI0 to DI39 (HH)		2.99	
						→DO0 to DO39 (LL)		2.91	

Equivalent Cells	16905

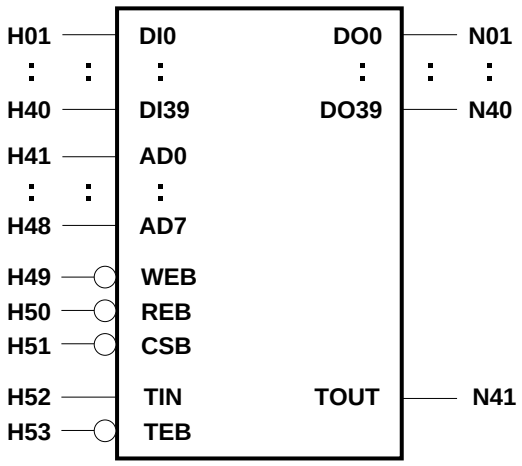
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.918**		
Address access time	**t_{ACA}**			**9.918**
Address output hold time	**t_{OH}**	**1.530**		
CSB access time	**t_{CSC}**			**4.230**
CSB output hold time	**t_{CSL}**	**1.362**		**4.086**
CSB output set time	**t_{CLL}**	**1.410**		
REB access time	**t_{REC}**			**4.050**
REB output hold time	**t_{REL}**	**1.398**		**4.194**
REB output set time	**t_{RLL}**	**1.350**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.953**		
CSB-WEB reset time	**t_{CWR}**	**5.414**		
Write pulse width	**t_{WP}**	**5.414**		
Address setup time	**t_{AS}**	**6.761**		
Address hold time	**t_{AH}**	**2.778**		
Input data setup time	**t_{DS}**	**4.279**		
Input data hold time	**t_{DH}**	**3.288**		
WEB access time	**t_{WEC}**			**4.608**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBKF	**256 words × 40 bits Single-port RAM**	**K18F × 5**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD7 (LH)		5.29	
:	:	:	:	:	:	→DO0 to DO39 (HH)		5.26	
H40	DI39	2.1	N40	DO39	32.0	(HL)		4.78	
H41	AD0	2.1	N41	TOUT	34.0	(LL)		4.81	
:	:	:							
H48	AD7	2.1				CSB (LH)		2.22	
H49	WEB	2.1				→DO0 to DO39 (HL)		2.08	
H50	REB	1.0							
H51	CSB	1.0				REB (LH)		2.22	
H52	TIN	2.1				→DO0 to DO39 (HL)		2.08	
H53	TEB	4.1							
						DI0 to DI39 (HH)		2.96	
						→DO0 to DO39 (LL)		2.73	

Equivalent Cells	30497

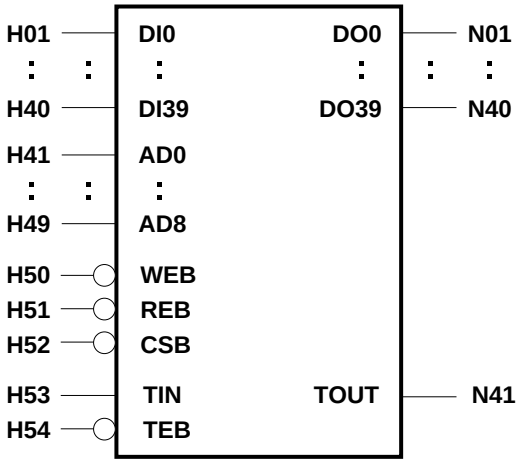
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.522**		
Address access time	**t_{ACA}**			**9.522**
Address output hold time	**t_{OH}**	**2.868**		
CSB access time	**t_{CSC}**			**3.996**
CSB output hold time	**t_{CSL}**	**1.248**		**3.744**
CSB output set time	**t_{CLL}**	**1.332**		
REB access time	**t_{REC}**			**3.996**
REB output hold time	**t_{REL}**	**1.248**		**3.744**
REB output set time	**t_{RLL}**	**1.332**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**4.482**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	Basic RAM
RBKH	**512 words × 40 bits Single-port RAM**	**K18F × 10**

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	AD0 to AD8 (LH)		5.65	
:	:	:	:	:	:	→DO0 to DO39 (HH)		5.59	
H40	DI39	2.1	N40	DO39	32.0	(HL)		2.90	
H41	AD0	2.1	N41	TOUT	34.0	(LL)		5.26	
:	:	:							
H49	AD8	2.1				CSB (LH)		2.86	
H50	WEB	2.1				→DO0 to DO39 (HL)		2.64	
H51	REB	1.0							
H52	CSB	2.1				REB (LH)		2.78	
H53	TIN	2.1				→DO0 to DO39 (HL)		2.79	
H54	TEB	4.1							
						DI0 to DI39 (HH)		3.27	
						→DO0 to DO39 (LL)		3.18	

Equivalent Cells	60499

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.170**		
Address access time	**t_{ACA}**			**10.170**
Address output hold time	**t_{OH}**	**1.740**		
CSB access time	**t_{CSC}**			**5.148**
CSB output hold time	**t_{CSL}**	**1.584**		**4.752**
CSB output set time	**t_{CLL}**	**1.716**		
REB access time	**t_{REC}**			**5.004**
REB output hold time	**t_{REL}**	**1.674**		**5.002**
REB output set time	**t_{RLL}**	**1.668**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.555**		
CSB-WEB reset time	**t_{CWR}**	**6.128**		
Write pulse width	**t_{WP}**	**6.128**		
Address setup time	**t_{AS}**	**5.297**		
Address hold time	**t_{AH}**	**3.130**		
Input data setup time	**t_{DS}**	**3.800**		
Input data hold time	**t_{DH}**	**4.188**		
WEB access time	**t_{WEC}**			**5.094**

[MEMO]

CHAPTER 2

HIGH DENSITY

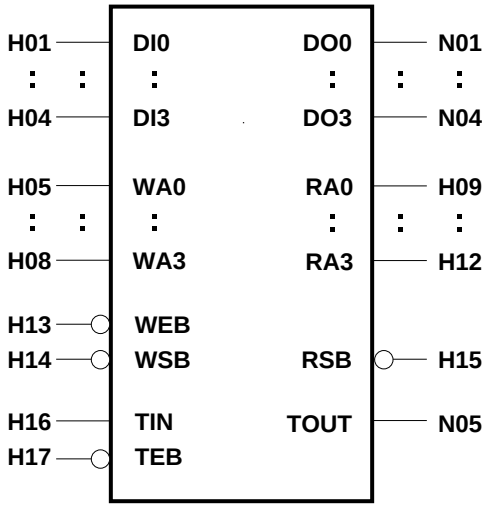
DUAL-PORT RAM BLOCK

(Soft Macro)

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R947	**16 words × 4 bits Dual-port RAM**	**K247 × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H04	DI3	2.1	N04	DO3	32.0	RA0 to RA3 (LH)		3.31	
H05	WA0	2.1	N05	TOUT	34.0	→DO0 to DO3 (HH)		3.26	
:	:	:				(HL)		3.22	
H08	WA3	2.1				(LL)		3.27	
H09	RA0	2.1							
:	:	:				RSB (LH)		1.52	
H12	RA3	2.1				→DO0 to DO3 (HL)		1.66	
H13	WEB	2.1							
H14	WSB	1.0				DI0 to DI3 (HH)		3.00	
H15	RSB	1.0				→DO0 to DO3 (LL)		3.09	
H16	TIN	2.1							
H17	TEB	2.0							

Equivalent Cells	727

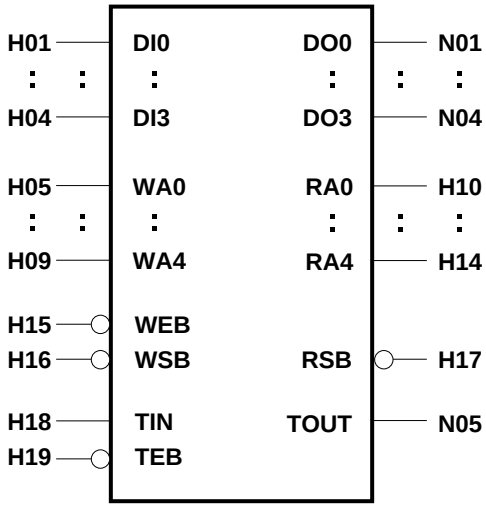
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**5.958**		
Address access time	**t_{ACA}**			**5.958**
Address output hold time	**t_{OH}**	**1.932**		
RSB access time	**t_{REC}**			**2.736**
RSB output hold time	**t_{REL}**	**0.996**		**2.988**
RSB output set time	**t_{RLL}**	**0.912**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.161**		
WSB-WEB reset time	**t_{CWR}**	**3.514**		
Write pulse width	**t_{WP}**	**3.514**		
Address setup time	**t_{AS}**	**5.920**		
Address hold time	**t_{AH}**	**2.728**		
Input data setup time	**t_{DS}**	**3.781**		
Input data hold time	**t_{DH}**	**2.963**		
WEB access time	**t_{WEC}**			**6.066**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R949	**32 words × 4 bits Dual-port RAM**	**K249 × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA5 (LH)		3.44	
:	:	:	:	:	:	→DO0 to DO3 (HH)		3.49	
H04	DI3	2.1	N04	DO3	32.0	(HL)		3.51	
H05	WA0	2.1	N05	TOUT	34.0	(LL)		3.46	
:	:	:							
H09	WA5	2.1				RSB (LH)		1.52	
H10	RA0	2.1				→DO0 to DO3 (HL)		1.66	
:	:	:							
H14	RA5	2.1				DI0 to DI3 (HH)		3.21	
H15	WEB	2.1				→DO0 to DO3 (LL)		3.29	
H16	WSB	1.0							
H17	RSB	1.0							
H18	TIN	2.1							
H19	TEB	2.0							

Equivalent Cells	1190

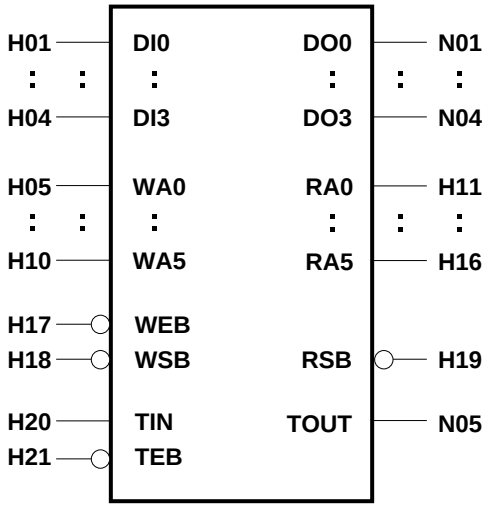
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.318**		
Address access time	**t_{ACA}**			**6.318**
Address output hold time	**t_{OH}**	**2.064**		
RSB access time	**t_{REC}**			**2.736**
RSB output hold time	**t_{REL}**	**0.996**		**2.988**
RSB output set time	**t_{RLL}**	**0.912**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.196**		
WSB-WEB reset time	**t_{CWR}**	**3.463**		
Write pulse width	**t_{WP}**	**3.463**		
Address setup time	**t_{AS}**	**6.018**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.856**		
Input data hold time	**t_{DH}**	**2.857**		
WEB access time	**t_{WEC}**			**6.372**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R94B	**64 words × 4 bits Dual-port RAM**	**K249 × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA5 (LH)		3.76	
:	:	:	:	:	:	→DO0 to DO3 (HH)		3.77	
H04	DI3	2.1	N04	DO3	32.0	(HL)		2.50	
H05	WA0	2.1	N05	TOUT	34.0	(LL)		3.87	
:	:	:							
H10	WA5	2.1				RSB (LH)		2.17	
H11	RA0	2.1				→DO0 to DO3 (HL)		2.35	
:	:	:							
H16	RA5	2.1				DI0 to DI3 (HH)		3.49	
H17	WEB	2.1				→DO0 to DO3 (LL)		3.70	
H18	WSB	1.0							
H19	RSB	1.0							
H20	TIN	2.1							
H21	TEB	2.0							

Equivalent Cells	2164

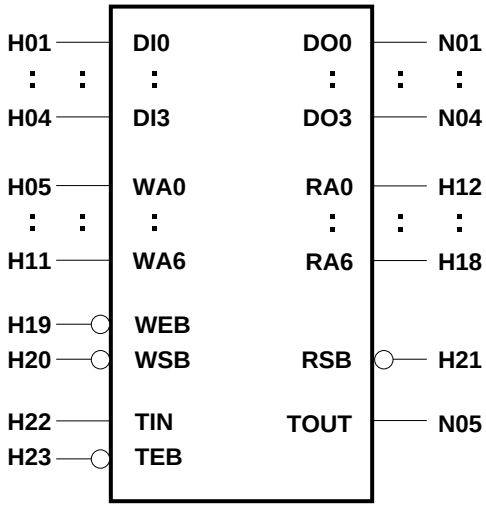
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.966**		
Address access time	**t_{ACA}**			**6.966**
Address output hold time	**t_{OH}**	**1.500**		
RSB access time	**t_{REC}**			**3.906**
RSB output hold time	**t_{REL}**	**1.410**		**4.230**
RSB output set time	**t_{RLL}**	**1.302**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.196**		
WSB-WEB reset time	**t_{CWR}**	**3.463**		
Write pulse width	**t_{WP}**	**3.463**		
Address setup time	**t_{AS}**	**6.018**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.856**		
Input data hold time	**t_{DH}**	**2.857**		
WEB access time	**t_{WEC}**			**7.128**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R94D	**128 words × 4 bits Dual-port RAM**	**K24D × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA6 (LH)		4.00	
:	:	:	:	:	:	→DO0 to DO3 (HH)		4.05	
H04	DI3	2.1	N04	DO3	32.0	(HL)		4.02	
H05	WA0	2.1	N05	TOUT	34.0	(LL)		3.97	
:	:	:							
H11	WA6	2.1				RSB (LH)		1.58	
H12	RA0	2.1				→DO0 to DO3 (HL)		1.72	
:	:	:							
H18	RA6	2.1				DI0 to DI3 (HH)		3.89	
H19	WEB	2.1				→DO0 to DO3 (LL)		3.95	
H20	WSB	1.0							
H21	RSB	1.0							
H22	TIN	2.1							
H23	TEB	2.0							

Equivalent Cells	2979

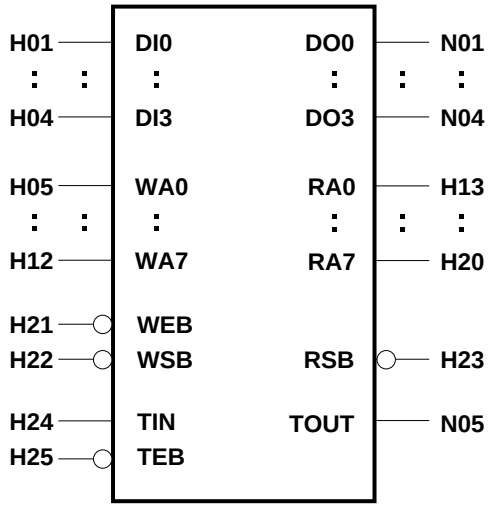
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.290**		
Address access time	**t_{ACA}**			**7.290**
Address output hold time	**t_{OH}**	**2.382**		
RSB access time	**t_{REC}**			**2.844**
RSB output hold time	**t_{REL}**	**1.032**		**3.096**
RSB output set time	**t_{RLL}**	**0.948**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.836**		
WSB-WEB reset time	**t_{CWR}**	**3.964**		
Write pulse width	**t_{WP}**	**3.964**		
Address setup time	**t_{AS}**	**6.157**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**4.276**		
Input data hold time	**t_{DH}**	**2.778**		
WEB access time	**t_{WEC}**			**7.578**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R94F	**256 words × 4 bits Dual-port RAM**	**K24D × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA7 (LH)		4.33	
:	:	:	:	:	:	→DO0 to DO3 (HH)		4.34	
H04	DI3	2.1	N04	DO3	32.0	(HL)		2.56	
H05	WA0	2.1	N05	TOUT	34.0	(LL)		4.39	
:	:	:							
H12	WA7	2.1				RSB (LH)		2.24	
H13	RA0	2.1				→DO0 to DO3 (HL)		2.41	
:	:	:							
H20	RA7	2.1				DI0 to DI3 (HH)		4.18	
H21	WEB	2.1				→DO0 to DO3 (LL)		4.37	
H22	WSB	1.0							
H23	RSB	1.0							
H24	TIN	2.1							
H25	TEB	2.0							

Equivalent Cells	5692

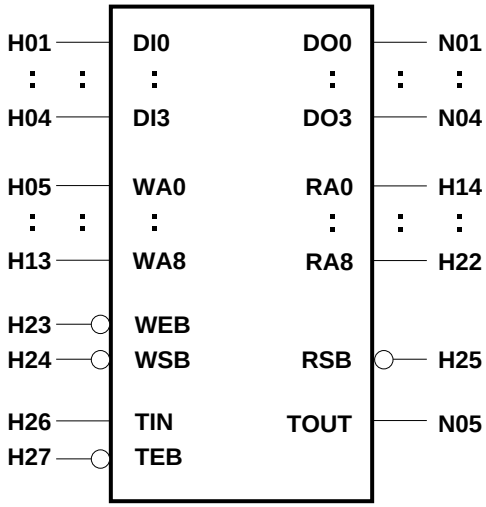
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.902**		
Address access time	**t_{ACA}**			**7.902**
Address output hold time	**t_{OH}**	**1.536**		
RSB access time	**t_{REC}**			**4.032**
RSB output hold time	**t_{REL}**	**1.446**		**4.338**
RSB output set time	**t_{RLL}**	**1.344**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.836**		
WSB-WEB reset time	**t_{CWR}**	**3.964**		
Write pulse width	**t_{WP}**	**3.964**		
Address setup time	**t_{AS}**	**6.157**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**4.276**		
Input data hold time	**t_{DH}**	**2.778**		
WEB access time	**t_{WEC}**			**8.334**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R94H	**512 words × 4 bits Dual-port RAM**	**K24D × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA8 (LH)		4.51	
:	:	:	:	:	:	→DO0 to DO3 (HH)		4.47	
H04	DI3	2.1	N04	DO3	32.0	(HL)		3.40	
H05	WA0	2.1	N05	TOUT	34.0	(LL)		4.76	
:	:	:							
H13	WA8	2.1				RSB (LH)		2.68	
H14	RA0	2.1				→DO0 to DO3 (HL)		3.03	
:	:	:							
H22	RA8	2.1				DI0 to DI3 (HH)		4.30	
H23	WEB	2.1				→DO0 to DO3 (LL)		4.73	
H24	WSB	1.0							
H25	RSB	1.0							
H26	TIN	2.1							
H27	TEB	2.0							

Equivalent Cells	11056

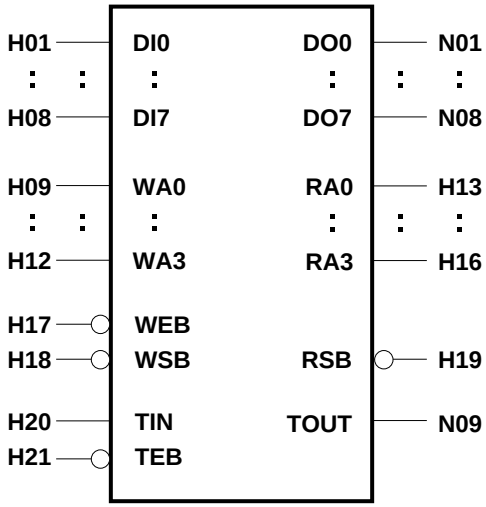
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.568**		
Address access time	**t_{ACA}**			**8.568**
Address output hold time	**t_{OH}**	**2.040**		
RSB access time	**t_{REC}**			**4.824**
RSB output hold time	**t_{REL}**	**1.818**		**5.454**
RSB output set time	**t_{RLL}**	**1.608**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.847**		
WSB-WEB reset time	**t_{CWR}**	**3.964**		
Write pulse width	**t_{WP}**	**3.964**		
Address setup time	**t_{AS}**	**6.181**		
Address hold time	**t_{AH}**	**2.702**		
Input data setup time	**t_{DS}**	**4.276**		
Input data hold time	**t_{DH}**	**2.778**		
WEB access time	**t_{WEC}**			**8.982**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R987	**16 words × 8 bits Dual-port RAM**	**K247 × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H08	DI7	2.1	N08	DO7	32.0	RA0 to RA3 (LH)		3.32	
H09	WA0	2.1	N09	TOUT	34.0	→DO0 to DO7 (HH)		3.36	
:	:	:				(HL)		3.32	
H12	WA3	2.1				(LL)		3.28	
H13	RA0	2.1							
:	:	:				RSB (LH)		1.55	
H16	RA3	2.1				→DO0 to DO7 (HL)		1.70	
H17	WEB	2.1							
H18	WSB	1.0				DI0 to DI7 (HH)		3.01	
H19	RSB	1.0				→DO0 to DO7 (LL)		3.09	
H20	TIN	2.1							
H21	TEB	2.0							

Equivalent Cells	1243

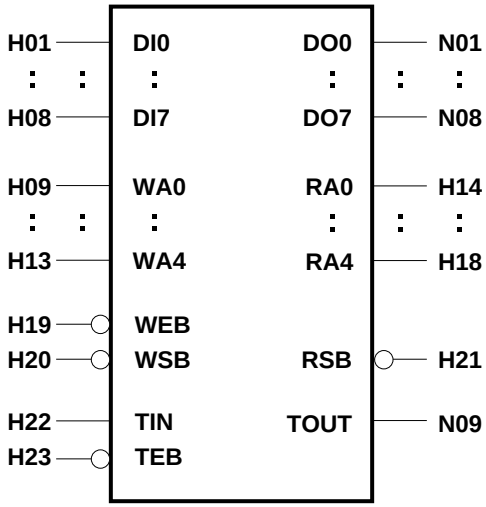
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.048**		
Address access time	**t_{ACA}**			**6.048**
Address output hold time	**t_{OH}**	**1.968**		
RSB access time	**t_{REC}**			**2.790**
RSB output hold time	**t_{REL}**	**1.020**		**3.060**
RSB output set time	**t_{RLL}**	**0.930**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.172**		
WSB-WEB reset time	**t_{CWR}**	**3.514**		
Write pulse width	**t_{WP}**	**3.514**		
Address setup time	**t_{AS}**	**5.944**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.781**		
Input data hold time	**t_{DH}**	**2.963**		
WEB access time	**t_{WEC}**			**6.156**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R989	**32 words × 8 bits Dual-port RAM**	**K249 × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA4 (LH)		3.50	
:	:	:	:	:	:	→DO0 to DO7 (HH)		3.53	
H08	DI7	2.1	N08	DO7	32.0	(HL)		3.55	
H09	WA0	2.1	N09	TOUT	34.0	(LL)		3.52	
:	:	:							
H13	WA4	2.1				RSB (LH)		1.56	
H14	RA0	2.1				→DO0 to DO7 (HL)		1.72	
:	:	:							
H18	RA4	2.1				DI0 to DI7 (HH)		3.21	
H19	WEB	2.1				→DO0 to DO7 (LL)		3.29	
H20	WSB	1.0							
H21	RSB	1.0							
H22	TIN	2.1							
H23	TEB	2.0							

Equivalent Cells	2160

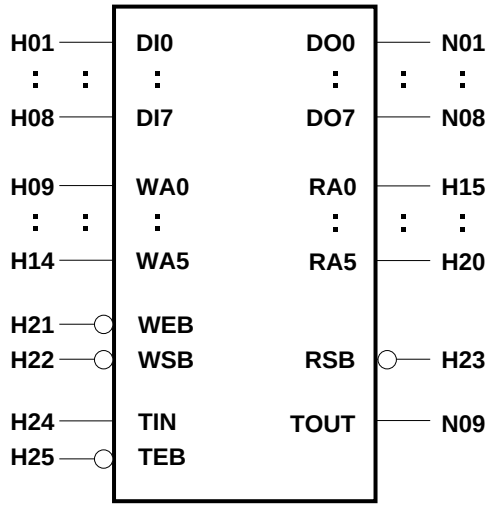
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.390**		
Address access time	**t_{ACA}**			**6.390**
Address output hold time	**t_{OH}**	**2.100**		
RSB access time	**t_{REC}**			**2.808**
RSB output hold time	**t_{REL}**	**1.032**		**3.096**
RSB output set time	**t_{RLL}**	**0.936**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.196**		
WSB-WEB reset time	**t_{CWR}**	**3.463**		
Write pulse width	**t_{WP}**	**3.463**		
Address setup time	**t_{AS}**	**6.018**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.856**		
Input data hold time	**t_{DH}**	**2.857**		
WEB access time	**t_{WEC}**			**6.498**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R98B	**64 words × 8 bits Dual-port RAM**	**K28B × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H08	DI7	2.1	N08	DO7	32.0	RA0 to RA5 (LH)		3.97	
H09	WA0	2.1	N09	TOUT	34.0	→DO0 to DO7 (HH)		4.02	
:	:	:				(HL)		3.96	
H14	WA5	2.1				(LL)		3.91	
H15	RA0	2.1							
:	:	:				RSB (LH)		1.56	
H20	RA5	2.1				→DO0 to DO7 (HL)		1.68	
H21	WEB	2.1							
H22	WSB	1.0				DI0 to DI7 (HH)		3.81	
H23	RSB	1.0				→DO0 to DO7 (LL)		3.77	
H24	TIN	2.1							
H25	TEB	2.0							

Equivalent Cells	3023

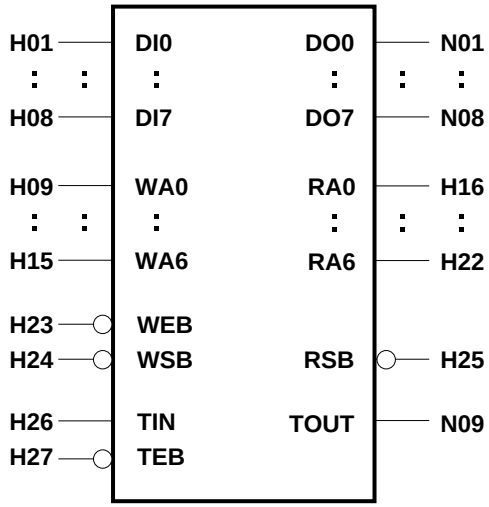
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.236**		
Address access time	**t_{ACA}**			**7.236**
Address output hold time	**t_{OH}**	**2.346**		
RSB access time	**t_{REC}**			**2.808**
RSB output hold time	**t_{REL}**	**1.008**		**3.024**
RSB output set time	**t_{RLL}**	**0.936**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.812**		
WSB-WEB reset time	**t_{CWR}**	**3.847**		
Write pulse width	**t_{WP}**	**3.847**		
Address setup time	**t_{AS}**	**6.250**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**4.130**		
Input data hold time	**t_{DH}**	**2.852**		
WEB access time	**t_{WEC}**			**7.290**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R98D	**128 words × 8 bits Dual-port RAM**	**K24D × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H08	DI7	2.1	N08	DO7	32.0	RA0 to RA6 (LH)		4.07	
H09	WA0	2.1	N09	TOUT	34.0	→DO0 to DO7 (HH)		4.10	
:	:	:				(HL)		4.07	
H15	WA6	2.1				(LL)		4.04	
H16	RA0	2.1							
:	:	:				RSB (LH)		1.62	
H22	RA6	2.1				→DO0 to DO7 (HL)		1.77	
H23	WEB	2.1							
H24	WSB	1.0				DI0 to DI7 (HH)		3.89	
H25	RSB	1.0				→DO0 to DO7 (LL)		3.95	
H26	TIN	2.1							
H27	TEB	2.0							

Equivalent Cells	5699

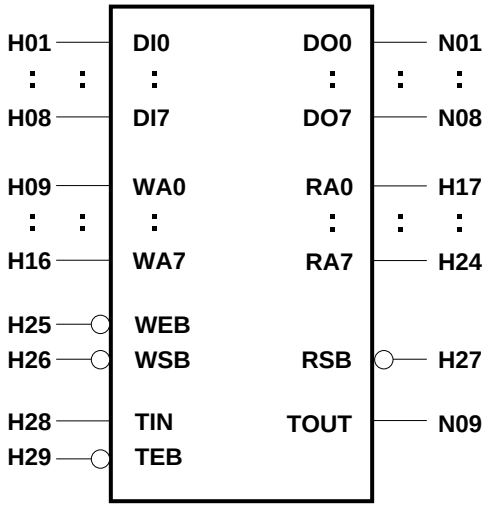
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.380**		
Address access time	**t_{ACA}**			**7.380**
Address output hold time	**t_{OH}**	**2.424**		
RSB access time	**t_{REC}**			**2.916**
RSB output hold time	**t_{REL}**	**1.062**		**3.186**
RSB output set time	**t_{RLL}**	**0.972**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.836**		
WSB-WEB reset time	**t_{CWR}**	**3.964**		
Write pulse width	**t_{WP}**	**3.964**		
Address setup time	**t_{AS}**	**6.157**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**4.276**		
Input data hold time	**t_{DH}**	**2.778**		
WEB access time	**t_{WEC}**			**7.704**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R98F	**256 words × 8 bits Dual-port RAM**	**K28F × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA7 (LH)		4.38	
:	:	:	:	:	:	→DO0 to DO7 (HH)		4.42	
H08	DI7	2.1	N08	DO7	32.0	(HL)		4.35	
H09	WA0	2.1	N09	TOUT	34.0	(LL)		4.31	
:	:	:							
H16	WA7	2.1				RSB (LH)		1.87	
H17	RA0	2.1				→DO0 to DO7 (HL)		2.08	
:	:	:							
H24	RA7	2.1				DI0 to DI7 (HH)		3.97	
H25	WEB	2.1				→DO0 to DO7 (LL)		4.04	
H26	WSB	1.0							
H27	RSB	1.0							
H28	TIN	2.1							
H29	TEB	2.0							

Equivalent Cells	9504

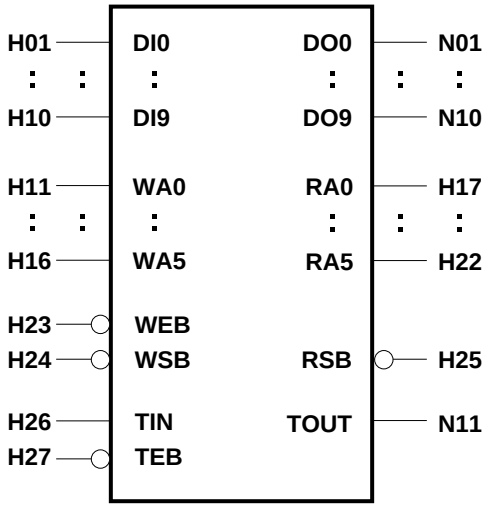
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.956**		
Address access time	**t_{ACA}**			**7.956**
Address output hold time	**t_{OH}**	**2.586**		
RSB access time	**t_{REC}**			**3.366**
RSB output hold time	**t_{REL}**	**1.248**		**3.744**
RSB output set time	**t_{RLL}**	**1.122**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.004**		
WSB-WEB reset time	**t_{CWR}**	**5.096**		
Write pulse width	**t_{WP}**	**5.096**		
Address setup time	**t_{AS}**	**6.205**		
Address hold time	**t_{AH}**	**2.702**		
Input data setup time	**t_{DS}**	**3.913**		
Input data hold time	**t_{DH}**	**3.494**		
WEB access time	**t_{WEC}**			**8.298**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9AB	**64 words × 10 bits Dual-port RAM**	**K2AB × 1**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H10	DI9	2.1	N10	DO9	32.0	RA0 to RA5 (LH)		4.48	
H11	WA0	2.1	N11	TOUT	34.0	→DO0 to DO9 (HH)		4.53	
:	:	:				(HL)		4.36	
H16	WA5	2.1				(LL)		4.31	
H17	RA0	2.1							
:	:	:				RSB (LH)		1.75	
H22	RA5	2.1				→DO0 to DO9 (HL)		1.90	
H23	WEB	2.1							
H24	WSB	1.0				DI0 to DI9 (HH)		3.81	
H25	RSB	1.0				→DO0 to DO9 (LL)		3.79	
H26	TIN	2.1							
H27	TEB	2.0							

Equivalent Cells	3494

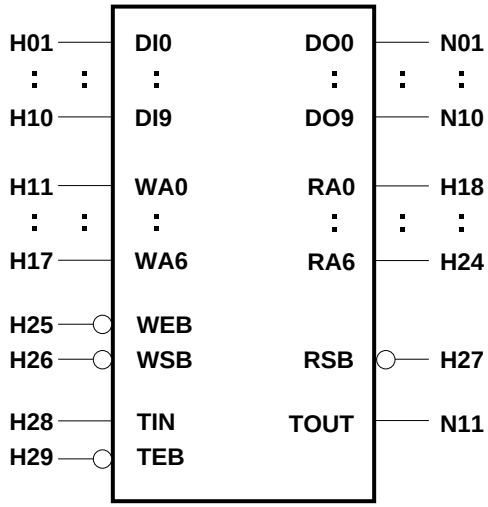
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.154**		
Address access time	**t_{ACA}**			**8.154**
Address output hold time	**t_{OH}**	**2.586**		
RSB access time	**t_{REC}**			**3.150**
RSB output hold time	**t_{REL}**	**1.140**		**3.420**
RSB output set time	**t_{RLL}**	**1.050**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.509**		
WSB-WEB reset time	**t_{CWR}**	**4.302**		
Write pulse width	**t_{WP}**	**4.302**		
Address setup time	**t_{AS}**	**6.492**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.872**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**7.884**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9AD	**128 words × 10 bits Dual-port RAM**	**K2AB × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H10	DI9	2.1	N10	DO9	32.0	RA0 to RA6 (LH)		4.81	
H11	WA0	2.1	N11	TOUT	34.0	→DO0 to DO9 (HH)		4.83	
:	:	:				(HL)		2.74	
H17	WA6	2.1				(LL)		4.73	
H18	RA0	2.1							
:	:	:				RSB (LH)		2.40	
H24	RA6	2.1				→DO0 to DO9 (HL)		2.59	
H25	WEB	2.1							
H26	WSB	1.0				DI0 to DI9 (HH)		4.11	
H27	RSB	1.0				→DO0 to DO9 (LL)		4.22	
H28	TIN	2.1							
H29	TEB	2.0							

Equivalent Cells	6703

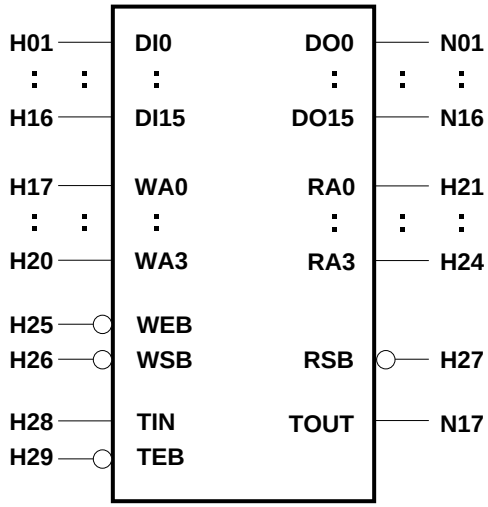
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.694**		
Address access time	**t_{ACA}**			**8.694**
Address output hold time	**t_{OH}**	**1.644**		
RSB access time	**t_{REC}**			**4.320**
RSB output hold time	**t_{REL}**	**1.554**		**4.662**
RSB output set time	**t_{RLL}**	**1.440**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.509**		
WSB-WEB reset time	**t_{CWR}**	**4.302**		
Write pulse width	**t_{WP}**	**4.302**		
Address setup time	**t_{AS}**	**6.492**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.872**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**8.658**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9C7	**16 words × 16 bits Dual-port RAM**	**K247 × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA3 (LH)		3.43	
:	:	:	:	:	:	→DO0 to DO15 (HH)		3.44	
H16	DI15	2.1	N16	DO15	32.0	(HL)		3.39	
H17	WA0	2.1	N17	TOUT	34.0	(LL)		3.38	
:	:	:							
H20	WA3	2.1				RSB (LH)		1.63	
H21	RA0	2.1				→DO0 to DO15 (HL)		1.79	
:	:	:							
H24	RA3	2.1				DI0 to DI15 (HH)		3.010	
H25	WEB	2.1				→DO0 to DO15 (LL)		3.150	
H26	WSB	1.0							
H27	RSB	1.0							
H28	TIN	2.1							
H29	TEB	2.0							

Equivalent Cells	2291

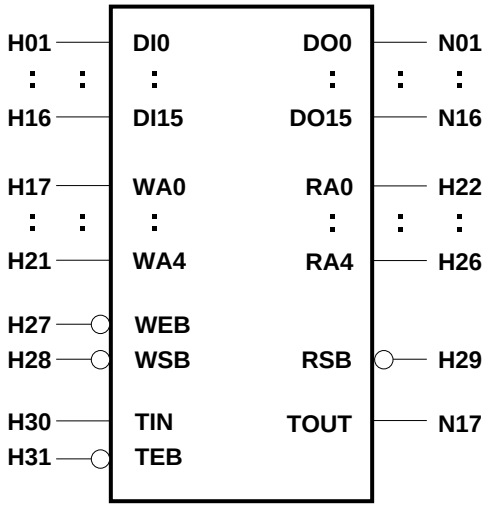
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.192**		
Address access time	**t_{ACA}**			**6.192**
Address output hold time	**t_{OH}**	**2.028**		
RSB access time	**t_{REC}**			**2.934**
RSB output hold time	**t_{REL}**	**1.074**		**3.222**
RSB output set time	**t_{RLL}**	**0.978**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.172**		
WSB-WEB reset time	**t_{CWR}**	**3.514**		
Write pulse width	**t_{WP}**	**3.514**		
Address setup time	**t_{AS}**	**5.944**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.781**		
Input data hold time	**t_{DH}**	**2.963**		
WEB access time	**t_{WEC}**			**6.372**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9C9	**32 words × 16 bits Dual-port RAM**	**K249 × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA4 (LH)		3.62	
:	:	:	:	:	:	→DO0 to DO15 (HH)		3.62	
H16	DI15	2.1	N16	DO15	32.0	(HL)		3.63	
H17	WA0	2.1	N17	TOUT	34.0	(LL)		3.63	
:	:	:							
H21	WA4	2.1				RSB (LH)		1.64	
H22	RA0	2.1				→DO0 to DO15 (HL)		1.80	
:	:	:							
H26	RA4	2.1				DI0 to DI15 (HH)		3.22	
H27	WEB	2.1				→DO0 to DO15 (LL)		3.30	
H28	WSB	1.0							
H29	RSB	1.0							
H30	TIN	2.1							
H31	TEB	2.0							

Equivalent Cells	4104

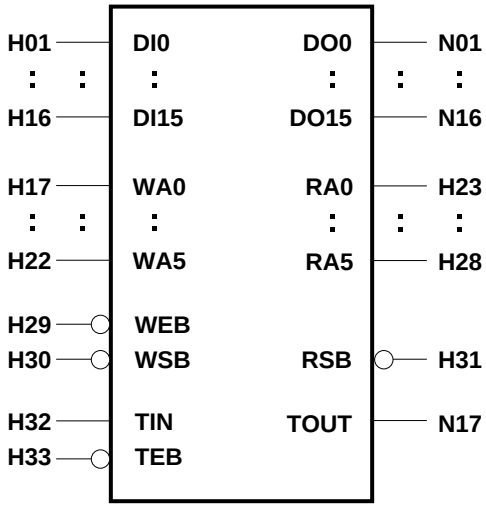
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.532**		
Address access time	**t_{ACA}**			**6.532**
Address output hold time	**t_{OH}**	**2.172**		
RSB access time	**t_{REC}**			**2.952**
RSB output hold time	**t_{REL}**	**1.080**		**3.240**
RSB output set time	**t_{RLL}**	**0.984**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.196**		
WSB-WEB reset time	**t_{CWR}**	**3.463**		
Write pulse width	**t_{WP}**	**3.463**		
Address setup time	**t_{AS}**	**6.018**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.856**		
Input data hold time	**t_{DH}**	**2.857**		
WEB access time	**t_{WEC}**			**6.696**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9CB	**64 words × 16 bits Dual-port RAM**	**K28B × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H16	DI15	2.1	N16	DO15	32.0				
H17	WA0	2.1	N17	TOUT	34.0				
:	:	:							
H22	WA5	2.1							
H23	RA0	2.1							
:	:	:							
H28	RA5	2.1							
H29	WEB	2.1							
H30	WSB	1.0							
H31	RSB	1.0							
H32	TIN	2.1							
H33	TEB	2.0							
						RA0 to RA5 (LH)		4.03	
						→DO0 to DO15 (HH)		4.06	
						(HL)		4.00	
						(LL)		3.97	
						RSB (LH)		1.61	
						→DO0 to DO15 (HL)		1.74	
						DI0 to DI15 (HH)		3.81	
						→DO0 to DO15 (LL)		3.78	

Equivalent Cells	5802

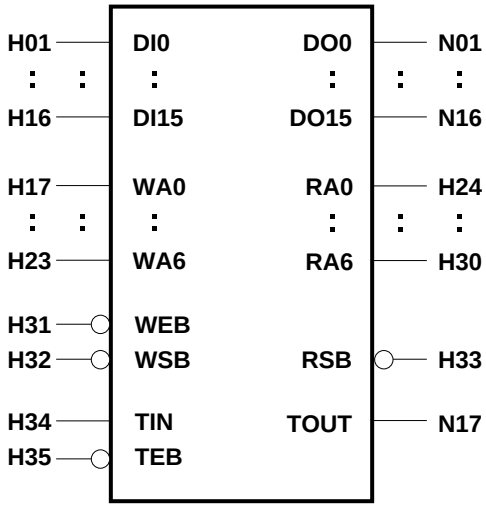
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.308**		
Address access time	**t_{ACA}**			**7.308**
Address output hold time	**t_{OH}**	**2.382**		
RSB access time	**t_{REC}**			**2.898**
RSB output hold time	**t_{REL}**	**1.044**		**3.132**
RSB output set time	**t_{RLL}**	**0.966**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.812**		
WSB-WEB reset time	**t_{CWR}**	**3.847**		
Write pulse width	**t_{WP}**	**3.847**		
Address setup time	**t_{AS}**	**6.250**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**4.130**		
Input data hold time	**t_{DH}**	**2.852**		
WEB access time	**t_{WEC}**			**7.416**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9CD	**128 words × 16 bits Dual-port RAM**	**K24D × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H16	DI15	2.1	N16	DO15	32.0				
H17	WA0	2.1	N17	TOUT	34.0				
:	:	:							
H23	WA6	2.1							
H24	RA0	2.1							
:	:	:							
H30	RA6	2.1							
H31	WEB	2.1							
H32	WSB	1.0							
H33	RSB	1.0							
H34	TIN	2.1							
H35	TEB	2.0							
						RA0 to RA6 (LH)		4.22	
						→DO0 to DO15 (HH)		4.22	
						(HL)		4.18	
						(LL)		4.18	
						RSB (LH)		1.72	
						→DO0 to DO15 (HL)		1.89	
						DI0 to DI15 (HH)		3.90	
						→DO0 to DO15 (LL)		3.96	

Equivalent Cells	11119

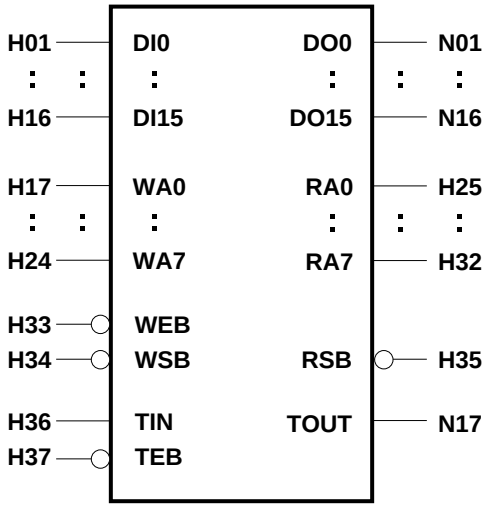
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.596**		
Address access time	**t_{ACA}**			**7.596**
Address output hold time	**t_{OH}**	**2.508**		
RSB access time	**t_{REC}**			**3.096**
RSB output hold time	**t_{REL}**	**1.134**		**3.402**
RSB output set time	**t_{RLL}**	**1.032**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.847**		
WSB-WEB reset time	**t_{CWR}**	**3.964**		
Write pulse width	**t_{WP}**	**3.964**		
Address setup time	**t_{AS}**	**6.181**		
Address hold time	**t_{AH}**	**2.702**		
Input data setup time	**t_{DS}**	**4.276**		
Input data hold time	**t_{DH}**	**2.778**		
WEB access time	**t_{WEC}**			**7.956**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9CF	**256 words × 16 bits Dual-port RAM**	**K28F × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA7 (LH)		4.46	
:	:	:	:	:	:	→DO0 to DO15 (HH)		4.48	
H16	DI15	2.1	N16	DO15	32.0	(HL)		4.42	
H17	WA0	2.1	N17	TOUT	34.0	(LL)		4.40	
:	:	:							
H24	WA7	2.1				RSB (LH)		1.93	
H25	RA0	2.1				→DO0 to DO15 (HL)		2.14	
:	:	:							
H32	RA7	2.1				DI0 to DI15 (HH)		3.98	
H33	WEB	2.1				→DO0 to DO15 (LL)		4.05	
H34	WSB	1.0							
H35	RSB	1.0							
H36	TIN	2.1							
H37	TEB	2.0							

Equivalent Cells	18708

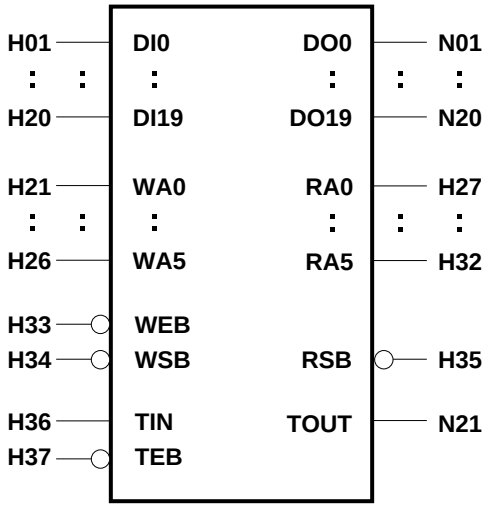
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.064**		
Address access time	**t_{ACA}**			**8.064**
Address output hold time	**t_{OH}**	**2.640**		
RSB access time	**t_{REC}**			**3.474**
RSB output hold time	**t_{REL}**	**1.284**		**3.852**
RSB output set time	**t_{RLL}**	**1.158**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**14.027**		
WSB-WEB reset time	**t_{CWR}**	**5.096**		
Write pulse width	**t_{WP}**	**5.096**		
Address setup time	**t_{AS}**	**6.229**		
Address hold time	**t_{AH}**	**2.702**		
Input data setup time	**t_{DS}**	**3.913**		
Input data hold time	**t_{DH}**	**3.494**		
WEB access time	**t_{WEC}**			**8.460**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9EB	**64 words × 20 bits Dual-port RAM**	**K2AB × 2**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA5 (LH)		4.55	
:	:	:	:	:	:	→DO0 to DO19 (HH)		4.59	
H20	DI19	2.1	N20	DO19	32.0	(HL)		4.42	
H21	WA0	2.1	N21	TOUT	34.0	(LL)		4.38	
:	:	:							
H26	WA5	2.1				RSB (LH)		1.79	
H27	RA0	2.1				→DO0 to DO19 (HL)		1.96	
:	:	:							
H32	RA5	2.1				DI0 to DI19 (HH)		3.81	
H33	WEB	2.1				→DO0 to DO19 (LL)		3.80	
H34	WSB	1.0							
H35	RSB	1.0							
H36	TIN	2.1							
H37	TEB	2.0							

Equivalent Cells	6748

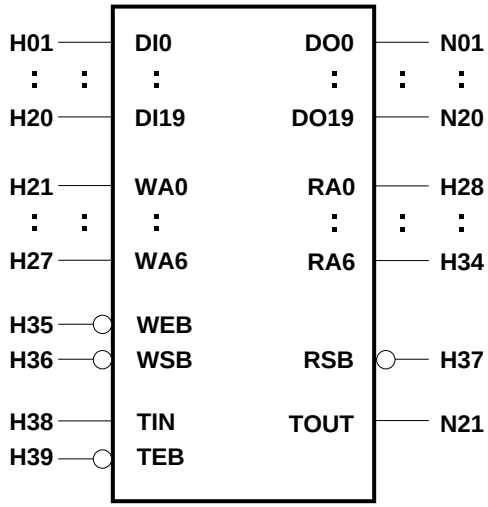
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.262**		
Address access time	**t_{ACA}**			**8.262**
Address output hold time	**t_{OH}**	**2.628**		
RSB access time	**t_{REC}**			**3.222**
RSB output hold time	**t_{REL}**	**1.176**		**3.528**
RSB output set time	**t_{RLL}**	**1.074**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.509**		
WSB-WEB reset time	**t_{CWR}**	**4.302**		
Write pulse width	**t_{WP}**	**4.302**		
Address setup time	**t_{AS}**	**6.492**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.872**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**8.028**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9ED	**128 words × 20 bits Dual-port RAM**	**K2AB × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H20	DI19	2.1	N20	DO19	32.0				
H21	WA0	2.1	N21	TOUT	34.0				
:	:	:							
H27	WA6	2.1							
H28	RA0	2.1							
:	:	:							
H34	RA6	2.1							
H35	WEB	2.1							
H36	WSB	1.0							
H37	RSB	1.0							
H38	TIN	2.1							
H39	TEB	2.0							
						RA0 to RA6 (LH)		4.96	
						→DO0 to DO19 (HH)		4.93	
						(HL)		2.82	
						(LL)		4.89	
						RSB (LH)		2.47	
						→DO0 to DO19 (HL)		2.65	
						DI0 to DI19 (HH)		4.11	
						→DO0 to DO19 (LL)		4.23	

Equivalent Cells	13118

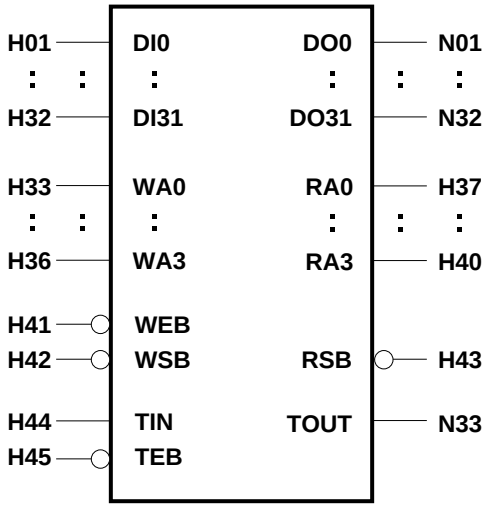
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.928**		
Address access time	**t_{ACA}**			**8.928**
Address output hold time	**t_{OH}**	**1.692**		
RSB access time	**t_{REC}**			**4.446**
RSB output hold time	**t_{REL}**	**1.590**		**4.770**
RSB output set time	**t_{RLL}**	**1.482**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.520**		
WSB-WEB reset time	**t_{CWR}**	**4.302**		
Write pulse width	**t_{WP}**	**4.302**		
Address setup time	**t_{AS}**	**6.515**		
Address hold time	**t_{AH}**	**2.702**		
Input data setup time	**t_{DS}**	**3.872**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**8.910**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9H7	**16 words × 32 bits Dual-port RAM**	**K247 × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA3 (LH)		3.66	
:	:	:	:	:	:	→DO0 to DO31 (HH)		3.61	
H32	DI31	2.1	N32	DO31	32.0	(HL)		3.57	
H33	WA0	2.1	N33	TOUT	34.0	(LL)		3.62	
:	:	:							
H36	WA3	2.1				RSB (LH)		1.77	
H37	RA0	2.1				→DO0 to DO31 (HL)		1.97	
:	:	:							
H40	RA3	2.1				DI0 to DI31 (HH)		3.01	
H41	WEB	2.1				→DO0 to DO31 (LL)		3.10	
H42	WSB	1.0							
H43	RSB	1.0							
H44	TIN	2.1							
H45	TEB	2.0							

Equivalent Cells	4363

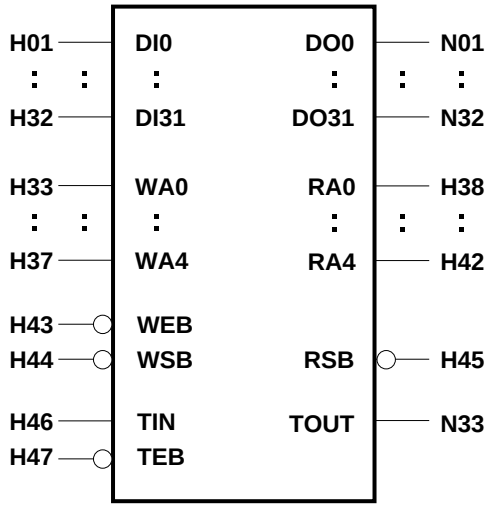
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.588**		
Address access time	**t_{ACA}**			**6.588**
Address output hold time	**t_{OH}**	**2.142**		
RSB access time	**t_{REC}**			**3.186**
RSB output hold time	**t_{REL}**	**1.182**		**3.546**
RSB output set time	**t_{RLL}**	**1.062**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.172**		
WSB-WEB reset time	**t_{CWR}**	**3.514**		
Write pulse width	**t_{WP}**	**3.514**		
Address setup time	**t_{AS}**	**5.944**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.781**		
Input data hold time	**t_{DH}**	**2.963**		
WEB access time	**t_{WEC}**			**6.462**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9H9	**32 words × 32 bits Dual-port RAM**	**K249 × 8**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA4 (LH)		3.87	
:	:	:	:	:	:	→DO0 to DO31 (HH)		3.81	
H32	DI31	2.1	N32	DO31	32.0	(HL)		3.83	
H33	WA0	2.1	N33	TOUT	34.0	(LL)		3.89	
:	:	:							
H37	WA4	2.1				RSB (LH)		1.81	
H38	RA0	2.1				→DO0 to DO31 (HL)		2.01	
:	:	:							
H42	RA4	2.1				DI0 to DI31 (HH)		3.22	
H43	WEB	2.1				→DO0 to DO31 (LL)		3.30	
H44	WSB	1.0							
H45	RSB	1.0							
H46	TIN	2.1							
H47	TEB	2.0							

Equivalent Cells	7968

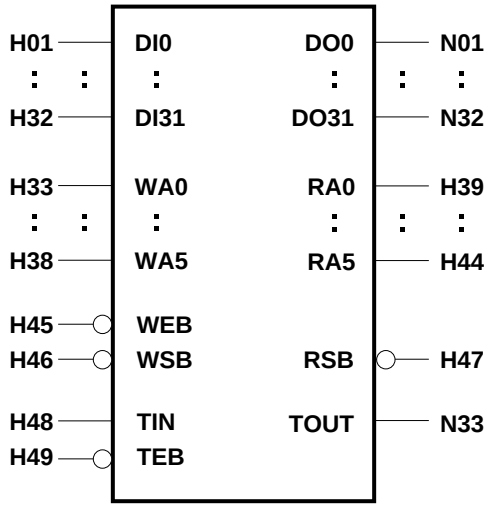
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.002**		
Address access time	**t_{ACA}**			**7.002**
Address output hold time	**t_{OH}**	**2.286**		
RSB access time	**t_{REC}**			**3.258**
RSB output hold time	**t_{REL}**	**1.206**		**3.618**
RSB output set time	**t_{RLL}**	**1.086**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.196**		
WSB-WEB reset time	**t_{CWR}**	**3.463**		
Write pulse width	**t_{WP}**	**3.463**		
Address setup time	**t_{AS}**	**6.018**		
Address hold time	**t_{AH}**	**2.715**		
Input data setup time	**t_{DS}**	**3.856**		
Input data hold time	**t_{DH}**	**2.857**		
WEB access time	**t_{WEC}**			**6.822**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9HB	**64 words × 32 bits Dual-port RAM**	**K28B × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0	RA0 to RA5 (LH)		4.18	
:	:	:	:	:	:	→DO0 to DO31 (HH)		4.18	
H32	DI31	2.1	N32	DO31	32.0	(HL)		4.12	
H33	WA0	2.1	N33	TOUT	34.0	(LL)		4.12	
:	:	:							
H38	WA5	2.1				RSB (LH)		1.70	
H39	RA0	2.1				→DO0 to DO31 (HL)		1.86	
:	:	:							
H44	RA5	2.1				DI0 to DI31 (HH)		3.82	
H45	WEB	2.1				→DO0 to DO31 (LL)		3.78	
H46	WSB	1.0							
H47	RSB	1.0							
H48	TIN	2.1							
H49	TEB	2.0							

Equivalent Cells	11341

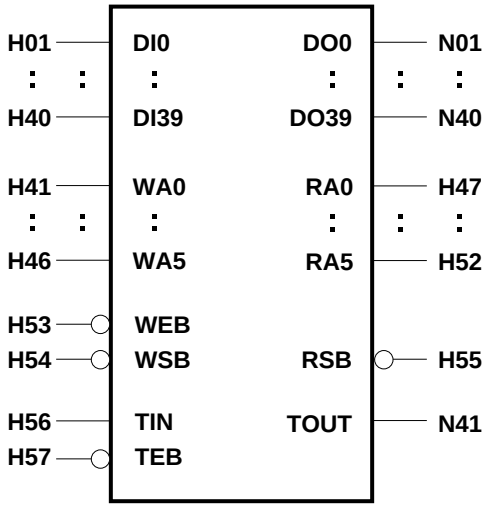
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.524**		
Address access time	**t_{ACA}**			**7.524**
Address output hold time	**t_{OH}**	**2.472**		
RSB access time	**t_{REC}**			**3.060**
RSB output hold time	**t_{REL}**	**1.116**		**3.348**
RSB output set time	**t_{RLL}**	**1.020**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.823**		
WSB-WEB reset time	**t_{CWR}**	**3.847**		
Write pulse width	**t_{WP}**	**3.847**		
Address setup time	**t_{AS}**	**6.273**		
Address hold time	**t_{AH}**	**2.702**		
Input data setup time	**t_{DS}**	**4.130**		
Input data hold time	**t_{DH}**	**2.852**		
WEB access time	**t_{WEC}**			**7.668**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	Basic RAM
R9KB	**64 words × 40 bits Dual-port RAM**	**K2AB × 4**

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	0	DIn(WAn)	X	1	0	X	Write
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn(RAn)	X	Read
1	X	X	X	1	X	Hold	X	X	X	X	Hold
1	X	X	X	X	1	Hold	X	X	X	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data
TEB : Test enable
TIN : Test input
TOUT : Test output

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.1	N01	DO0	32.0				
:	:	:	:	:	:				
H40	DI39	2.1	N40	DO39	32.0				
H41	WA0	2.1	N41	TOUT	34.0				
:	:	:							
H46	WA5	2.1							
H47	RA0	2.1							
:	:	:							
H52	RA5	2.1							
H53	WEB	2.1							
H54	WSB	1.0							
H55	RSB	1.0							
H56	TIN	2.1							
H57	TEB	2.0							
						RA0 to RA5 (LH)		4.70	
						→DO0 to DO39 (HH)		4.69	
						(HL)		4.52	
						(LL)		4.53	
						RSB (LH)		1.89	
						→DO0 to DO39 (HL)		2.07	
						DI0 to DI39 (HH)		3.82	
						→DO0 to DO39 (LL)		3.80	

Equivalent Cells	13237

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.460**		
Address access time	**t_{ACA}**			**8.460**
Address output hold time	**t_{OH}**	**2.712**		
RSB access time	**t_{REC}**			**3.402**
RSB output hold time	**t_{REL}**	**1.242**		**3.726**
RSB output set time	**t_{RLL}**	**1.134**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.520**		
WSB-WEB reset time	**t_{CWR}**	**4.302**		
Write pulse width	**t_{WP}**	**4.302**		
Address setup time	**t_{AS}**	**6.515**		
Address hold time	**t_{AH}**	**2.702**		
Input data setup time	**t_{DS}**	**3.872**		
Input data hold time	**t_{DH}**	**3.119**		
WEB access time	**t_{WEC}**			**8.280**

[MEMO]

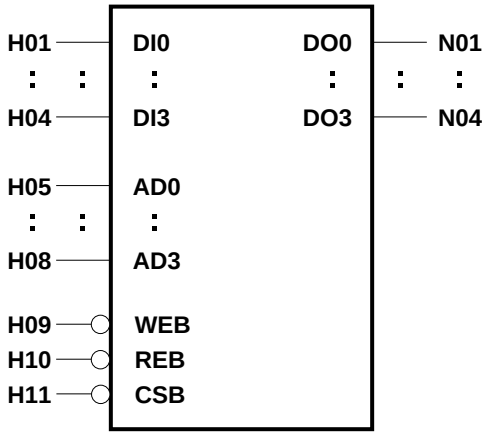
APPENDIX

BASIC RAM BLOCK

BASIC RAM BLOCK

Block Type	Function
K147	**16 words × 4 bits Single-port RAM**

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	34.0	AD0 to AD3 (LH)	1.751	3.534	7.598
:	:	:	:	:	:	→DO0 to DO3 (HH)	1.751	3.534	7.598
H04	DI3	1.0	N04	DO3	34.0	(HL)	1.456	3.048	6.675
H05	AD0	1.0				(LL)	1.456	3.048	6.675
:	:	:							
H08	AD3	1.0				CSB (LH)	0.368	0.973	2.350
H09	WEB	1.0				→DO0 to DO3 (HL)	0.345	0.877	2.087
H10	REB	1.0							
H11	CSB	1.0				REB (LH)	0.368	0.973	2.350
						→DO0 to DO3 (HL)	0.345	0.877	2.087
						DI0 to DI3 (HH)	0.805	1.788	4.028
						→DO0 to DO3 (LL)	0.803	1.719	3.808

Equivalent Cells	29 x 12 = 348	Power (mW/MHz)	Read cycle	0.188
			Write cycle	0.261

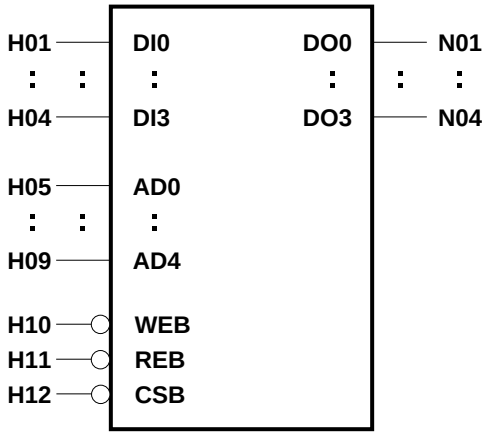
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.598**		
Address access time	**t_{ACA}**			**7.598**
Address output hold time	**t_{OH}**	**1.456**		
CSB access time	**t_{CSC}**			**2.350**
CSB output hold time	**t_{CSL}**	**0.345**		**2.087**
CSB output set time	**t_{CLL}**	**0.368**		
REB access time	**t_{REC}**			**2.350**
REB output hold time	**t_{REL}**	**0.345**		**2.087**
REB output set time	**t_{RLL}**	**0.368**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.593**		
CSB-WEB reset time	**t_{CWR}**	**3.881**		
Write pulse width	**t_{WP}**	**3.881**		
Address setup time	**t_{AS}**	**4.712**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**3.452**		
Input data hold time	**t_{DH}**	**2.305**		
WEB access time	**t_{WEC}**			**2.486**

BASIC RAM BLOCK

Block Type	Function
K149	**32 words × 4 bits Single-port RAM**

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	**DI0**	**1.0**	**N01**	**DO0**	**34.0**
:	**:**	**:**	**:**	**:**	**:**
H04	**DI3**	**1.0**	**N04**	**DO3**	**34.0**
H05	**AD0**	**1.0**			
:	**:**	**:**			
H09	**AD4**	**1.0**			
H10	**WEB**	**1.0**			
H11	**REB**	**1.0**			
H12	**CSB**	**1.0**			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD4	**(LH)**	**1.819**	**3.605**	**7.676**
→DO0 to DO3	**(HH)**	**1.819**	**3.605**	**7.676**
	(HL)	**1.590**	**3.202**	**6.875**
	(LL)	**1.590**	**3.202**	**6.875**
CSB	**(LH)**	**0.380**	**0.996**	**2.399**
→DO0 to DO3	**(HL)**	**0.354**	**0.888**	**2.105**
REB	**(LH)**	**0.380**	**0.996**	**2.399**
→DO0 to DO3	**(HL)**	**0.354**	**0.888**	**2.105**
DI0 to DI3	**(HH)**	**0.845**	**1.803**	**3.986**
→DO0 to DO3	**(LL)**	**0.834**	**1.714**	**3.719**

Equivalent Cells	**47 x 13 = 611**	Power (mW/MHz)	Read cycle	0.198
			Write cycle	0.285

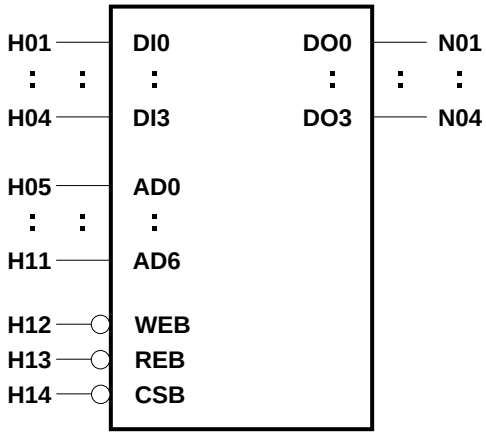
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.676**		
Address access time	**t_{ACA}**			**7.676**
Address output hold time	**t_{OH}**	**1.590**		
CSB access time	**t_{CSC}**			**2.399**
CSB output hold time	**t_{CSL}**	**0.354**		**2.105**
CSB output set time	**t_{CLL}**	**0.380**		
REB access time	**t_{REC}**			**2.399**
REB output hold time	**t_{REL}**	**0.354**		**2.105**
REB output set time	**t_{RLL}**	**0.380**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.455**		
CSB-WEB reset time	**t_{CWR}**	**3.690**		
Write pulse width	**t_{WP}**	**3.690**		
Address setup time	**t_{AS}**	**4.765**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**3.174**		
Input data hold time	**t_{DH}**	**2.280**		
WEB access time	**t_{WEC}**			**2.523**

BASIC RAM BLOCK

Block Type	Function
K14D	**128 words × 4 bits Single-port RAM**

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	34.0	AD0 to AD6 (LH)	2.021	3.906	8.201
:	:	:	:	:	:	→DO0 to DO3 (HH)	2.021	3.906	8.201
H04	DI3	1.0	N04	DO3	34.0	(HL)	1.834	3.534	7.408
H05	AD0	1.0				(LL)	1.834	3.534	7.408
:	:	:							
H11	AD6	1.0				CSB (LH)	0.438	1.079	2.540
H12	WEB	1.0				→DO0 to DO3 (HL)	0.394	0.945	2.199
H13	REB	1.0							
H14	CSB	1.0				REB (LH)	0.438	1.079	2.540
						→DO0 to DO3 (HL)	0.394	0.945	2.199
						DI0 to DI3 (HH)	1.058	2.107	4.498
						→DO0 to DO3 (LL)	1.002	1.942	4.082

Equivalent Cells	79 x 22 = 1738	Power (mW/MHz)	Read cycle	0.191
			Write cycle	0.336

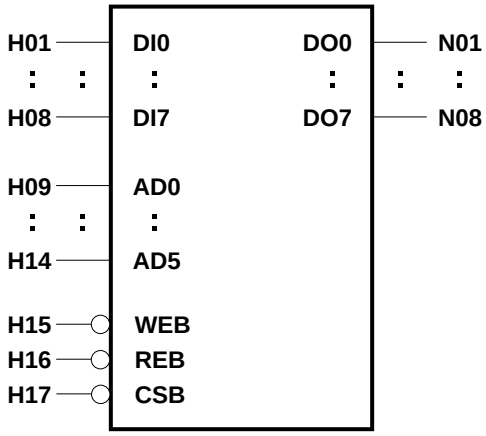
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.201**		
Address access time	**t_{ACA}**			**8.201**
Address output hold time	**t_{OH}**	**1.834**		
CSB access time	**t_{CSC}**			**2.540**
CSB output hold time	**t_{CSL}**	**0.394**		**2.199**
CSB output set time	**t_{CLL}**	**0.438**		
REB access time	**t_{REC}**			**2.540**
REB output hold time	**t_{REL}**	**0.394**		**2.199**
REB output set time	**t_{RLL}**	**0.438**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.997**		
CSB-WEB reset time	**t_{CWR}**	**4.078**		
Write pulse width	**t_{WP}**	**4.078**		
Address setup time	**t_{AS}**	**4.919**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**3.468**		
Input data hold time	**t_{DH}**	**2.148**		
WEB access time	**t_{WEC}**			**2.655**

BASIC RAM BLOCK

Block Type	Function
K18B	**64 words × 8 bits Single-port RAM**

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**34.0**	**AD0 to AD5 (LH)**	**2.056**	**3.961**	**8.302**
:	**:**	**:**	**:**	**:**	**:**	**→DO0 to DO7 (HH)**	**2.056**	**3.961**	**8.302**
H08	**DI7**	**1.0**	**N08**	**DO7**	**34.0**	**(HL)**	**1.898**	**3.631**	**7.579**
H09	**AD0**	**1.0**				**(LL)**	**1.898**	**3.631**	**7.579**
:	**:**	**:**							
H14	**AD5**	**1.0**				**CSB (LH)**	**0.428**	**1.055**	**2.483**
H15	**WEB**	**1.0**				**→DO0 to DO7 (HL)**	**0.365**	**0.914**	**2.165**
H16	**REB**	**1.0**							
H17	**CSB**	**1.0**				**REB (LH)**	**0.428**	**1.055**	**2.483**
						→DO0 to DO7 (HL)	**0.365**	**0.914**	**2.165**
						DI0 to DI7 (HH)	**0.969**	**1.954**	**4.197**
						→DO0 to DO7 (LL)	**0.928**	**1.808**	**3.812**

Equivalent Cells	**81 x 21 = 1701**	Power (mW/MHz)	Read cycle	0.359
			Write cycle	0.579

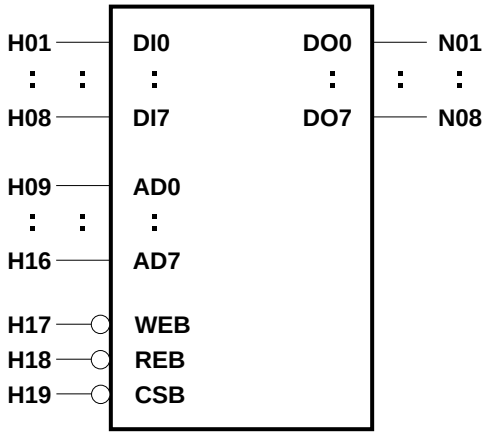
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.302**		
Address access time	**t_{ACA}**			**8.302**
Address output hold time	**t_{OH}**	**1.898**		
CSB access time	**t_{CSC}**			**2.483**
CSB output hold time	**t_{CSL}**	**0.365**		**2.165**
CSB output set time	**t_{CLL}**	**0.428**		
REB access time	**t_{REC}**			**2.483**
REB output hold time	**t_{REL}**	**0.365**		**2.165**
REB output set time	**t_{RLL}**	**0.428**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**11.303**		
CSB-WEB reset time	**t_{CWR}**	**4.016**		
Write pulse width	**t_{WP}**	**4.016**		
Address setup time	**t_{AS}**	**5.287**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**3.331**		
Input data hold time	**t_{DH}**	**2.284**		
WEB access time	**t_{WEC}**			**2.563**

BASIC RAM BLOCK

Block Type	Function
K18F	**256 words × 8 bits Single-port RAM**

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	34.0	AD0 to AD7 (LH)	2.215	4.261	8.925
:	:	:	:	:	:	→DO0 to DO7 (HH)	2.215	4.261	8.925
H08	DI7	1.0	N08	DO7	34.0	(HL)	1.983	3.807	7.963
H09	AD0	1.0				(LL)	1.983	3.807	7.963
:	:	:				CSB (LH)	0.650	1.418	3.168
H16	AD7	1.0				→DO0 to DO7 (HL)	0.508	1.152	2.617
H17	WEB	1.0				REB (LH)	0.650	1.418	3.168
H18	REB	1.0				→DO0 to DO7 (HL)	0.508	1.152	2.617
H19	CSB	1.0				DI0 to DI7 (HH)	1.110	2.189	4.648
						→DO0 to DO7 (LL)	1.074	2.038	4.235

Equivalent Cells	158 x 38 = 6004	Power (mW/MHz)	Read cycle	0.380
			Write cycle	0.735

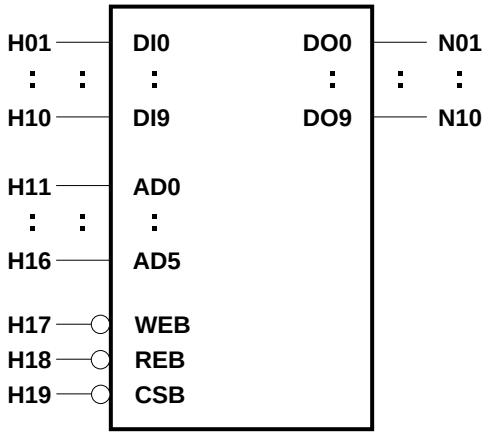
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.925**		
Address access time	**t_{ACA}**			**8.925**
Address output hold time	**t_{OH}**	**1.983**		
CSB access time	**t_{CSC}**			**3.168**
CSB output hold time	**t_{CSL}**	**0.508**		**2.617**
CSB output set time	**t_{CLL}**	**0.650**		
REB access time	**t_{REC}**			**3.168**
REB output hold time	**t_{REL}**	**0.508**		**2.617**
REB output set time	**t_{RLL}**	**0.650**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**11.364**		
CSB-WEB reset time	**t_{CWR}**	**4.972**		
Write pulse width	**t_{WP}**	**4.972**		
Address setup time	**t_{AS}**	**4.099**		
Address hold time	**t_{AH}**	**2.293**		
Input data setup time	**t_{DS}**	**2.852**		
Input data hold time	**t_{DH}**	**3.175**		
WEB access time	**t_{WEC}**			**3.244**

BASIC RAM BLOCK

Block Type	Function
K1AB	**64 words × 10 bits Single-port RAM**

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	34.0	AD0 to AD5 (LH)	2.152	4.070	8.441
:	:	:	:	:	:	→DO0 to DO9 (HH)	2.152	4.070	8.441
H10	DI9	1.0	N10	DO9	34.0	(HL)	1.924	3.670	7.648
H11	AD0	1.0				(LL)	1.924	3.670	7.648
:	:	:							
H16	AD5	1.0				CSB (LH)	0.444	1.087	2.553
H17	WEB	1.0				→DO0 to DO9 (HL)	0.381	0.931	2.186
H18	REB	1.0							
H19	CSB	1.0				REB (LH)	0.444	1.087	2.553
						→DO0 to DO9 (HL)	0.381	0.931	2.186
						DI0 to DI9 (HH)	0.969	1.945	4.168
						→DO0 to DO9 (LL)	0.928	1.807	3.810

Equivalent Cells	81 x 25 = 2025	Power (mW/MHz)	Read cycle	0.420
			Write cycle	0.689

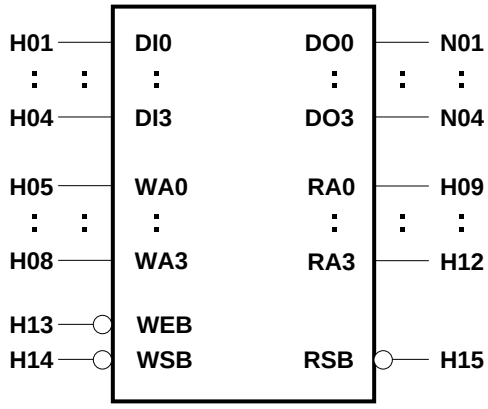
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.441**		
Address access time	**t_{ACA}**			**8.441**
Address output hold time	**t_{OH}**	**1.924**		
CSB access time	**t_{CSC}**			**2.553**
CSB output hold time	**t_{CSL}**	**0.381**		**2.186**
CSB output set time	**t_{CLL}**	**0.444**		
REB access time	**t_{REC}**			**2.553**
REB output hold time	**t_{REL}**	**0.381**		**2.186**
REB output set time	**t_{RLL}**	**0.444**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**11.695**		
CSB-WEB reset time	**t_{CWR}**	**4.377**		
Write pulse width	**t_{WP}**	**4.377**		
Address setup time	**t_{AS}**	**5.319**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**3.251**		
Input data hold time	**t_{DH}**	**2.425**		
WEB access time	**t_{WEC}**			**2.640**

BASIC RAM BLOCK

Block Type	Function
K247	**16words × 4 bits Dual-port RAM**

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	Operation
DIn	WAn	0	0	DIn(WAn)	X	1	0	Write
DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	Write, Read
X	X	1	X	Hold	RAn	0	DMn(RAn)	Read
X	X	X	1	Hold	RAn	0	DMn(RAn)	Read
X	X	1	X	Hold	X	X	X	Hold
X	X	X	1	Hold	X	X	X	Hold

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**34.0**				
:	:	:	:	:	:				
H04	**DI3**	**1.0**	**N04**	**DO3**	**34.0**				
H05	**WA0**	**1.0**							
:	:	:							
H08	**WA3**	**1.0**							
H09	**RA0**	**1.0**							
:	:	:							
H12	**RA3**	**1.0**							
H13	**WEB**	**1.0**							
H14	**WSB**	**1.0**							
H15	**RSB**	**1.0**							
						RA0 to RA3 (LH)	**1.105**	**2.530**	**5.780**
						→DO0 to DO3 (HH)	**1.105**	**2.530**	**5.780**
						(HL)	**1.253**	**2.506**	**5.361**
						(LL)	**1.253**	**2.506**	**5.361**
						RSB (LH)	**0.356**	**0.920**	**2.205**
						→DO0 to DO3 (HL)	**0.412**	**1.011**	**2.376**
						DI0 to DI3 (HH)	**1.031**	**2.261**	**5.066**
						→DO0 to DO3 (LL)	**1.226**	**2.432**	**5.180**

Equivalent Cells	**37 x 13 = 481**	Power (mW/MHz)	Read cycle	0.079
			Write cycle	0.256

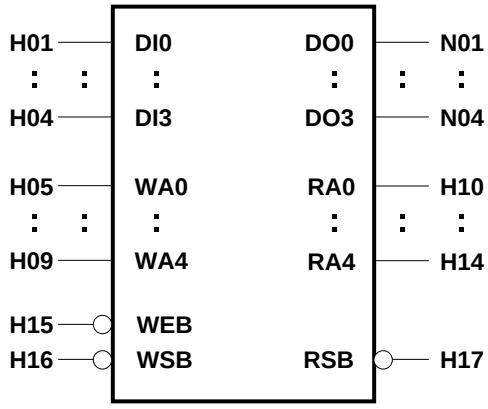
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**5.780**		
Address access time	**t_{ACA}**			**5.780**
Address output hold time	**t_{OH}**	**1.105**		
REB access time	**t_{REC}**			**2.205**
REB output hold time	**t_{REL}**	**0.412**		**2.376**
REB output set time	**t_{RLL}**	**0.356**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.533**		
CSB-WEB reset time	**t_{CWR}**	**2.793**		
Write pulse width	**t_{WP}**	**2.793**		
Address setup time	**t_{AS}**	**4.560**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**2.836**		
Input data hold time	**t_{DH}**	**2.154**		
WEB access time	**t_{WEC}**			**5.799**

BASIC RAM BLOCK

Block Type	Function
K249	**32 words × 4 bits Dual-port RAM**

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	Operation
DIn	WAn	0	0	DIn(WAn)	X	1	0	Write
DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	Write, Read
X	X	1	X	Hold	RAn	0	DMn(RAn)	Read
X	X	X	1	Hold	RAn	0	DMn(RAn)	Read
X	X	1	X	Hold	X	X	X	Hold
X	X	X	1	Hold	X	X	X	Hold

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**34.0**	**RA0 to RA4 →DO0 to DO3**	**(LH)**	**1.284**	**2.694**	**5.906**
:	:	:	:	:	:		**(HH)**	**1.284**	**2.694**	**5.906**
H04	**DI3**	**1.0**	**N04**	**DO3**	**34.0**		**(HL)**	**1.481**	**2.733**	**5.586**
H05	**WA0**	**1.0**					**(LL)**	**1.481**	**2.733**	**5.586**
:	:	:								
H09	**WA4**	**1.0**				**RSB →DO0 to DO3**	**(LH)**	**0.356**	**0.919**	**2.202**
H10	**RA0**	**1.0**					**(HL)**	**0.412**	**1.011**	**2.376**
:	:	:								
H14	**RA4**	**1.0**				**DI0 to DI3 →DO0 to DO3**	**(HH)**	**1.170**	**2.464**	**5.413**
H15	**WEB**	**1.0**					**(LL)**	**1.389**	**2.627**	**5.448**
H16	**WSB**	**1.0**								
H17	**RSB**	**1.0**								

Equivalent Cells	**63 x 15 = 945**	Power (mW/MHz)	Read cycle	0.085
			Write cycle	0.280

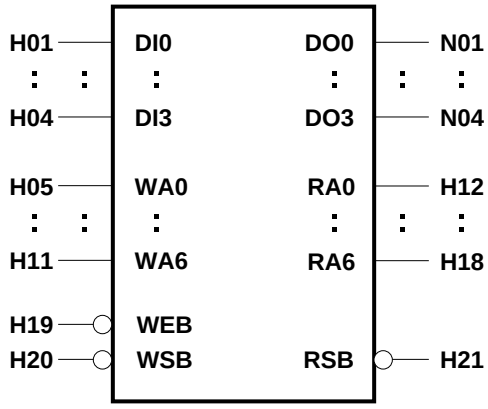
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**5.906**		
Address access time	**t_{ACA}**			**5.906**
Address output hold time	**t_{OH}**	**1.284**		
REB access time	**t_{REC}**			**2.202**
REB output hold time	**t_{REL}**	**0.412**		**2.376**
REB output set time	**t_{RLL}**	**0.356**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.373**		
CSB-WEB reset time	**t_{CWR}**	**2.751**		
Write pulse width	**t_{WP}**	**2.751**		
Address setup time	**t_{AS}**	**4.622**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**2.898**		
Input data hold time	**t_{DH}**	**2.066**		
WEB access time	**t_{WEC}**			**6.003**

BASIC RAM BLOCK

Block Type	Function
K24D	**128 words × 4 bits Dual-port RAM**

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	Operation
DIn	WAn	0	0	DIn(WAn)	X	1	0	Write
DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	Write, Read
X	X	1	X	Hold	RAn	0	DMn(RAn)	Read
X	X	X	1	Hold	RAn	0	DMn(RAn)	Read
X	X	1	X	Hold	X	X	X	Hold
X	X	X	1	Hold	X	X	X	Hold

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**34.0**				
:	:	:	:	:	:				
H04	**DI3**	**1.0**	**N04**	**DO3**	**34.0**				
H05	**WA0**	**1.0**							
:	:	:							
H11	**WA6**	**1.0**							
H12	**RA0**	**1.0**							
:	:	:							
H18	**RA6**	**1.0**							
H19	**WEB**	**1.0**							
H20	**WSB**	**1.0**							
H21	**RSB**	**1.0**							
						RA0 to RA6 (LH)	**1.673**	**3.253**	**6.855**
						→DO0 to DO3 (HH)	**1.673**	**3.253**	**6.855**
						(HL)	**1.868**	**3.245**	**6.381**
						(LL)	**1.868**	**3.245**	**6.381**
						RSB (LH)	**0.389**	**0.968**	**2.287**
						→DO0 to DO3 (HL)	**0.451**	**1.060**	**2.450**
						DI0 to DI3 (HH)	**1.655**	**3.137**	**6.514**
						→DO0 to DO3 (LL)	**1.895**	**3.281**	**6.439**

Equivalent Cells	**112 x 24 = 2688**	Power (mW/MHz)	Read cycle	0.075
			Write cycle	0.314

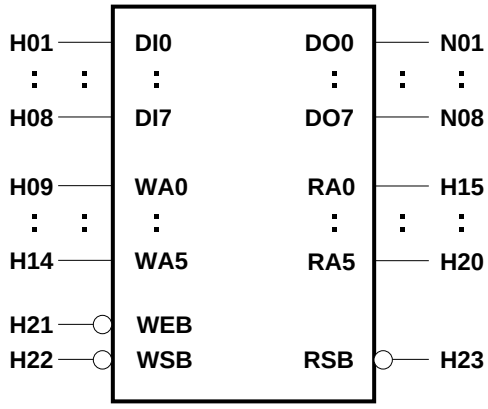
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.855**		
Address access time	**t_{ACA}**			**6.855**
Address output hold time	**t_{OH}**	**1.673**		
REB access time	**t_{REC}**			**2.287**
REB output hold time	**t_{REL}**	**0.451**		**2.450**
REB output set time	**t_{RLL}**	**0.389**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.906**		
CSB-WEB reset time	**t_{CWR}**	**3.168**		
Write pulse width	**t_{WP}**	**3.168**		
Address setup time	**t_{AS}**	**4.738**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**3.248**		
Input data hold time	**t_{DH}**	**2.000**		
WEB access time	**t_{WEC}**			**7.244**

BASIC RAM BLOCK

Block Type	Function
K28B	**64 words × 8bits Dual-port RAM**

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	Operation
DIn	WAn	0	0	DIn(WAn)	X	1	0	Write
DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	Write, Read
X	X	1	X	Hold	RAn	0	DMn(RAn)	Read
X	X	X	1	Hold	RAn	0	DMn(RAn)	Read
X	X	1	X	Hold	X	X	X	Hold
X	X	X	1	Hold	X	X	X	Hold

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	34.0	RA0 to RA5 →DO0 to DO7	(LH)	1.650	3.217	6.788
:	:	:	:	:	:		(HH)	1.650	3.217	6.788
H08	DI7	1.0	N08	DO7	34.0		(HL)	1.835	3.182	6.251
H09	WA0	1.0					(LL)	1.835	3.182	6.251
:	:	:				RSB →DO0 to DO7	(LH)	0.379	0.951	2.254
H14	WA5	1.0					(HL)	0.436	1.027	2.374
H15	RA0	1.0				DI0 to DI7 →DO0 to DO7	(HH)	1.567	3.055	6.446
:	:	:					(LL)	1.769	3.104	6.144
H20	RA5	1.0								
H21	WEB	1.0								
H22	WSB	1.0								
H23	RSB	1.0								

Equivalent Cells	113 x 24 = 2712	Power (mW/MHz)	Read cycle	0.176
			Write cycle	0.561

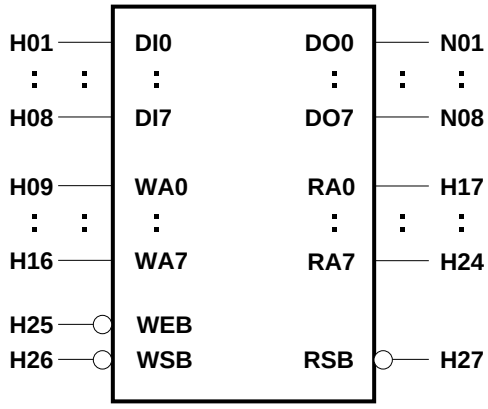
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.788**		
Address access time	**t_{ACA}**			**6.788**
Address output hold time	**t_{OH}**	**1.650**		
REB access time	**t_{REC}**			**2.254**
REB output hold time	**t_{REL}**	**0.436**		**2.374**
REB output set time	**t_{RLL}**	**0.379**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.885**		
CSB-WEB reset time	**t_{CWR}**	**3.071**		
Write pulse width	**t_{WP}**	**3.071**		
Address setup time	**t_{AS}**	**4.815**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**3.127**		
Input data hold time	**t_{DH}**	**2.062**		
WEB access time	**t_{WEC}**			**7.025**

BASIC RAM BLOCK

Block Type	Function
K28F	**256 words × 8bits Dual-port RAM**

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	Operation
DIn	WAn	0	0	DIn(WAn)	X	1	0	Write
DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	Write, Read
X	X	1	X	Hold	RAn	0	DMn(RAn)	Read
X	X	X	1	Hold	RAn	0	DMn(RAn)	Read
X	X	1	X	Hold	X	X	X	Hold
X	X	X	1	Hold	X	X	X	Hold

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**34.0**	**RA0 to RA7 (LH)**	**1.864**	**3.606**	**7.577**
:	:	:	:	:	:	**→DO0 to DO7 (HH)**	**1.864**	**3.606**	**7.577**
H08	**DI7**	**1.0**	**N08**	**DO7**	**34.0**	**(HL)**	**2.054**	**3.565**	**7.008**
H09	**WA0**	**1.0**				**(LL)**	**2.054**	**3.565**	**7.008**
:	:	:							
H16	**WA7**	**1.0**							
H17	**RA0**	**1.0**				**RSB (LH)**	**0.545**	**1.283**	**2.965**
:	:	:				**→DO0 to DO7 (HL)**	**0.633**	**1.399**	**3.144**
H24	**RA7**	**1.0**							
H25	**WEB**	**1.0**				**DI0 to DI7 (HH)**	**1.701**	**3.214**	**6.663**
H26	**WSB**	**1.0**				**→DO0 to DO7 (LL)**	**1.987**	**3.364**	**6.500**
H27	**RSB**	**1.0**							

Equivalent Cells	**224 x41 = 9184**	Power (mW/MHz)	Read cycle	0.182
			Write cycle	0.630

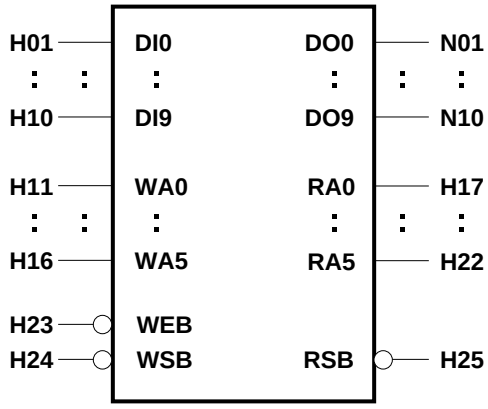
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.577**		
Address access time	**t_{ACA}**			**7.577**
Address output hold time	**t_{OH}**	**1.864**		
REB access time	**t_{REC}**			**2.965**
REB output hold time	**t_{REL}**	**0.633**		**3.144**
REB output set time	**t_{RLL}**	**0.545**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.891**		
CSB-WEB reset time	**t_{CWR}**	**4.112**		
Write pulse width	**t_{WP}**	**4.112**		
Address setup time	**t_{AS}**	**4.778**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**2.946**		
Input data hold time	**t_{DH}**	**2.597**		
WEB access time	**t_{WEC}**			**8.162**

BASIC RAM BLOCK

Block Type	Function
K2AB	**64 words × 10bits Dual-port RAM**

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	Operation
DIn	WAn	0	0	DIn(WAn)	X	1	0	Write
DIn	WAn	0	0	DIn(WAn)	RAn	0	DIn(RAn)	Write, Read
X	X	1	X	Hold	RAn	0	DMn(RAn)	Read
X	X	X	1	Hold	RAn	0	DMn(RAn)	Read
X	X	1	X	Hold	X	X	X	Hold
X	X	X	1	Hold	X	X	X	Hold

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**34.0**					
:	:	:	:	:	:					
H10	**DI9**	**1.0**	**N10**	**DO9**	**34.0**					
H11	**WA0**	**1.0**								
:	:	:								
H16	**WA5**	**1.0**								
H17	**RA0**	**1.0**								
:	:	:								
H22	**RA5**	**1.0**								
H23	**WEB**	**1.0**								
H24	**WSB**	**1.0**								
H25	**RSB**	**1.0**								
						RA0 to RA5	**(LH)**	**1.954**	**3.728**	**7.769**
						→DO0 to DO9	**(HH)**	**1.954**	**3.728**	**7.769**
							(HL)	**2.107**	**3.585**	**6.952**
							(LL)	**2.107**	**3.585**	**6.952**
						RSB	**(LH)**	**0.480**	**1.135**	**2.626**
						→DO0 to DO9	**(HL)**	**0.565**	**1.245**	**2.793**
						DI0 to DI9	**(HH)**	**1.556**	**3.057**	**6.478**
						→DO0 to DO9	**(LL)**	**1.799**	**3.123**	**6.142**

Equivalent Cells	**113 x 28 = 3164**	Power (mW/MHz)	Read cycle	0.211
			Write cycle	0.654

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.769**		
Address access time	**t_{ACA}**			**7.769**
Address output hold time	**t_{OH}**	**1.954**		
REB access time	**t_{REC}**			**2.626**
REB output hold time	**t_{REL}**	**0.565**		**2.793**
REB output set time	**t_{RLL}**	**0.480**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.466**		
CSB-WEB reset time	**t_{CWR}**	**3.450**		
Write pulse width	**t_{WP}**	**3.450**		
Address setup time	**t_{AS}**	**5.017**		
Address hold time	**t_{AH}**	**2.000**		
Input data setup time	**t_{DS}**	**2.912**		
Input data hold time	**t_{DH}**	**2.284**		
WEB access time	**t_{WEC}**			**7.265**

お問い合わせ先

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お手数ですが，このドキュメントに対するご意見をお寄せください。今後のドキュメント作成の参考にさせていただきます。

［ドキュメント名］CMOS-N5 Family Memory Ver.2.0 Block Library
（A14683JJ2V0BL00（2nd edition））

［お名前など］（さしつかえのない範囲で）

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説明内容					
用語解説					
調べやすさ					
デザイン，字の大きさなど					
その他（　　）					
（　　）					

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