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RENESAS

Design Manual

# CMOS-9HD Series, EA-9HD Series

## CMOS Gate Array, CMOS Embedded Array

## Mega Macro Ver. 8.1

Document No. A13941EJ8V1DM00 (8th edition)
Date Published November 2008 NS

**[MEMO]**

## NOTES FOR CMOS DEVICES

### ① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

### ② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

### ③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

### ④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

### ⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

### ⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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**[MEMO]**

## Major Revisions in This Edition

A13941EJ7V0DM00 → A13941EJ8V1DM00

| Page | Description |
|---|---|
| p.16 | Modification of **Table 1-2. Number of Pins Necessary for Testing Mega Macro** |
| pp.83, 84 | Addition of **5.1 Overview** |
| p.87 | Modification of **5.2.1 Pin function list** |
| pp.90 to 93 | Addition of **5.2.2 Pin Descriptions** |
| p.94 | Addition of **Note.3** in **Figure 5-1. Initialization Pattern**<br>Correction of the waveform of CSB in Figure 5-1 |
| p.96 | Addition of **5.3.3 Notes on Creating Test Pattern** |
| p.108 | Addition of **5.6 (16) Timing in transmission READY FIFO mode (DMA mode = 0)** |
| p.108 | Modification of **5.6 (17) Timing in transmission READY FIFO mode (DMA mode = 1)** |
| pp.112 to 122 | Addition of **5.8.2 Register Description** |
| p.123 | Addition of **5.9 Typical Applications** |

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

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# INTRODUCTION

This manual explains how to design gate arrays using the mega macros (large-scale function blocks) of NEC's CMOS-9HD Series gate arrays.

Thoroughly read this manual for smooth LSI design.

Be sure to observe the points (general information, cautions, and limitations) described in this manual; otherwise, the quality and performance of the LSI may be degraded and the LSI may malfunction.

## Lineup of Mega Macros

| Mega Macro Name | Function | General-Purpose Models with Equivalent Functions |
|---|---|---|
| NA51A | Serial control unit | μPD71051 |
| NA54A | Programmable timer/counter | μPD71054 |
| NA59A | Interrupt control unit | μPD71059 |
| NZ16550A | UART with FIFO | PC16550D |

Because the gate placement and routing of each macro are predetermined, the internal timing specification of a macro is the same before and after placement and routing. However, the shape of the macro and the shape of the master, as well as the number of cells of the macro, must be taken into consideration when selecting the master on which the macro is to be mounted because the shape of the occupied cell area is fixed. In particular, when using two or more mega macros and when other hard macros (such as memory macros) are mounted, the combination of the shapes of the macros is complicated and mounting separate macros must be studied. In this case, consult NEC.

**Related Documents**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- CMOS-9HD Series Design Manual (A12985E)
- CMOS-9HD Series, EA-9HD Series Block Library (A13052E)
- CMOS-9HD Series, EA-9HD Series Memory Block Library (A13071E)
- CMOS-9HD Series, EA-9HD Series Mega Macro Design Manual (This manual)
- Design For Test User's Manual (A14357E)
- μPD71059 User's Manual (U13042J)[Note]
- μPD71059 Data Sheet (U11932J)[Note]

**Note** Only Japanese version is available.

## CONTENTS

## LIST OF FIGURES

## LIST OF TABLES

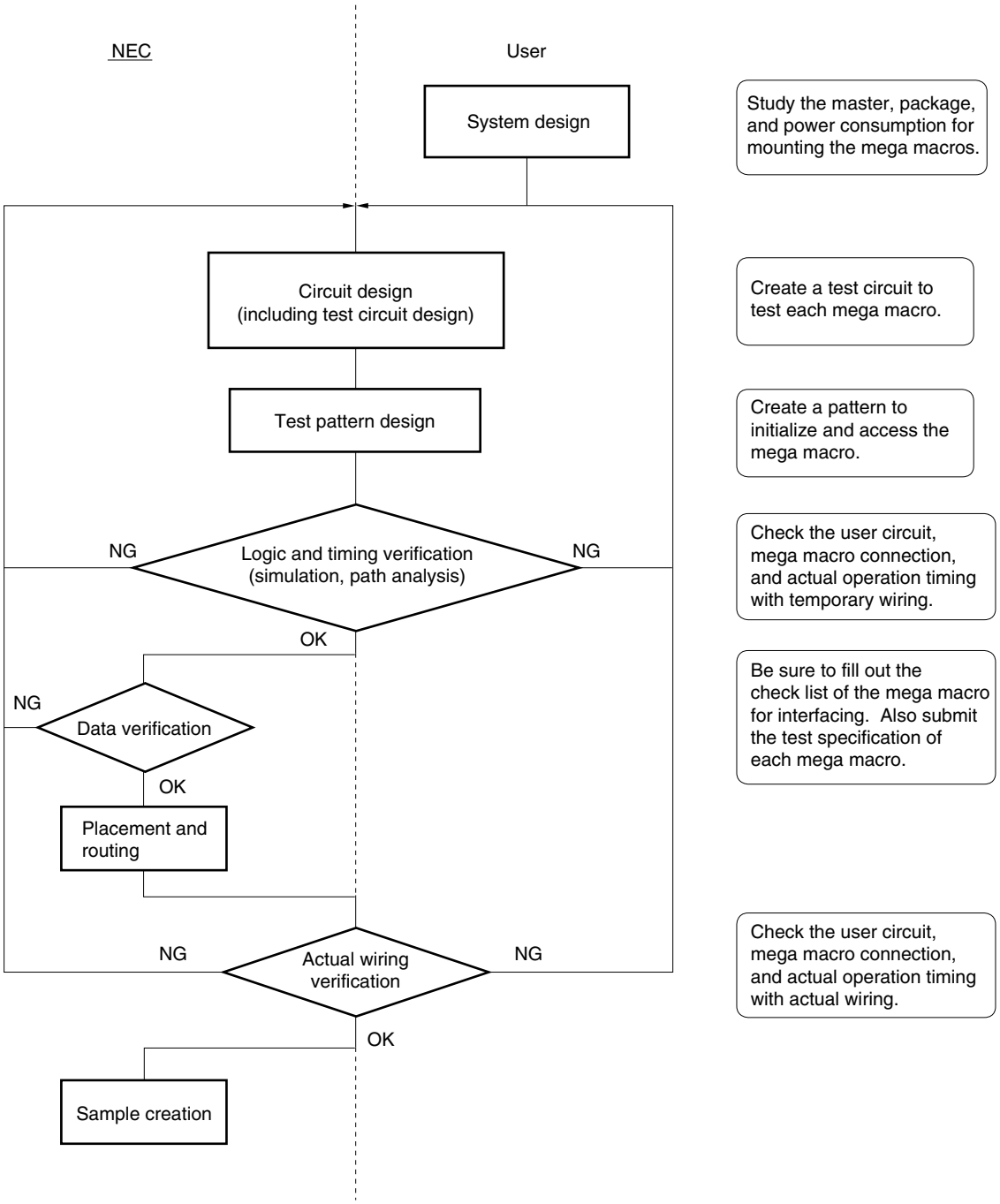
# CHAPTER 1 COMMON INFORMATION

This chapter explains the points that always apply when designing a gate array using mega macros. Also refer to the related documents of each series.

## 1.1 Development Flow

**Figure 1-1 Gate Array Development Flow When Mounting Mega Macros** shows a development flowchart illustrating how mega macros are mounted on a gate array. The points to be noted when mounting mega macros are explained below.

**Figure 1-1. Gate Array Development Flow When Mounting Mega Macros**



## 1.2 System Design

The points to be considered when studying the specifications of the gate array on which mega macros are mounted are described in this section.

### 1.2.1 Selecting master

Because the shape of a mega macro is determined in advance, some mega macros cannot be used, depending on the master, and the number of cells and shape of the macro. Table 1-1 lists the masters that can be selected when each mega macro is mounted.

When mounting two or more mega macros or memory macros, a separate study is necessary. Consult NEC.

**Table 1-1. Mega Macro Mountable Masters**

| Master Name | NA51A | NA54A | NA59A | NZ16550A |
|---|---|---|---|---|
| μPD65943 | √ | √ | √ | √ |
| μPD65944 | √ | √ | √ | √ |
| μPD65945 | √ | √ | √ | √ |
| μPD65946 | √ | √ | √ | √ |
| μPD65948 | √ | √ | √ | √ |
| μPD65949 | √ | √ | √ | √ |
| μPD65951 | √ | √ | √ | √ |
| μPD65954 | √ | √ | √ | √ |
| μPD65956 | √ | √ | √ | √ |
| μPD65958 | √ | √ | √ | √ |

**Remark** √: Supported

### 1.2.2 Number of pins

To enable NEC to confirm the operation of a mega macro, the user is requested to create a test circuit. Connect the pins of the test circuit so that the operation of the macro can be monitored from outside the gate array without inverting the logic of several pins of the macro and without going through a sequential circuit.

Therefore, assign test pins to the gate array. Table 1-2 shows the number of pins necessary for testing each mega macro. Take these values into consideration when studying the number of pins.

**Table 1-2. Number of Pins Necessary for Testing Mega Macro**

<R>

| Mega Macro Name | | | NA51A | NA54A | NA59A | NZ16550A |
|---|---|---|---|---|---|---|
| Necessary number of test pins | Input | Dedicated[Note 1] | 1 | 1 | 1 | 1 |
| | | Multiplexed[Notes 2, 4] | 23 | 22 | 38 | 32 |
| | Output | Multiplexed[Notes 3, 4] | 15 | 11 | 29 | 20 |

**Notes 1.** Be sure to provide a signal for selecting the test mode.

**2.** When clamping CSE, CSD, and TTHR, the number of pins can be reduced.

**3.** Be sure to output any pins you do not use.

**4.** Do not share the test pin of one macro.

### 1.2.3 Number of test patterns

The test circuit tests each mega macro. The number of patterns necessary for testing each macro is determined as shown in Table 1-3.

The maximum number of test patterns of a gate array is limited by the series. Because the number of test patterns of a mega macro is included in this maximum number, create a test pattern that satisfies the conditions indicated below. Note that the test pattern of each mega macro is prepared by NEC and used only when delivering the LSI, and is not submitted to the user.

"Maximum number of test patterns for each series"
≥ Σ "Number of mega macro test patterns"[Note 1] + Σ "Number of user test patterns"[Note 2]

**Notes 1.** Including when two or more instances of the same mega macro are mounted
**2.** Including the initialization pattern of the mega macro

**Table 1-3. Number of Test Patterns of Each Mega Macro (Per Macro)**

| Mega Macro Name | Number of Test Patterns |
|---|---|
| NA51A | 12874 |
| NA54A | 3483 |
| NA59A | 7335 |
| NZ16550A | 14889 |

### 1.2.4 Delay time

When roughly estimating the delay time, use the methods described below. To estimate the delay time more accurately, use a simulator or delay analysis tool.

**(1) Input timing**

Use the fanin of the input pins, the AC characteristics, and the block name of each mega macro to investigate the input timing.

**(2) Output timing**

Use the fanout of the output pins, the AC characteristics, and the block name of each mega macro to investigate the output timing.

For reference, expressions to estimate delay time are shown below.

**<1> Delay time of input buffer and internal function block**

$t_{PD} = t_{LD0} + (\Sigma\ F/O + I) \times t_1$ (ns)

**<2> Delay time of internal bus**

$t_{PD} = t_{LD0} + (\Sigma\ F/O + I + (N - 1) \times 0.96) \times t_1$ (ns)

$t_{PD}$: Propagation delay time (ns)
$t_{LD0}$: Basic delay time without load (ns)
F/O: Fanout value
I: Wiring capacitance connected to each output pin
(Refer to the **CMOS-9HD Series Design Manual (A12985E)**).
$t_1$: Delay coefficient of block output pin
N: Number of 3-state buffers connected to bus

### 1.2.5 Power consumption

The power consumption of each mega macro is calculated by using the operating frequency or read/write access cycle. The expressions to calculate the power consumption are shown below. These expressions are at $V_{DD}$ = 3.3 V, $T_A$ = 85°C.

#### (1) Power consumption of NA51A macro (P51)

| Series | Expression |
|---|---|
| CMOS-9HD | P51 = 133 × f (μW) |

f: Clock frequency (input pin CLK, in MHz)

#### (2) Power consumption of NA54A macro (P54)

| Series | Expression |
|---|---|
| CMOS-9HD | P54 = 240 × (f0 + f1 + f2) (μW) |

f0: Counter 0 clock frequency (input pin CLK0, in MHz)

f1: Counter 1 clock frequency (input pin CLK1, in MHz)

f2: Counter 2 clock frequency (input pin CLK2, in MHz)

#### (3) Power consumption of NA59A macro (P59)

| Series | Expression |
|---|---|
| CMOS-9HD | P59 = 120 × 1/T (μW) |

T: Read/write access cycle (μs)

#### (4) Power consumption of NZ16550A macro (P16550)

| Series | Expression |
|---|---|
| CMOS-9HD | P16550 = 361 × f (μW) |

f: Clock frequency (input pin XIN, in MHz)

## 1.3 Circuit Design

Keep in mind the following two points when embedding a mega macro in a circuit. Details of circuit design are explained from **1.3.1** onwards.

**(1) Processing of output pins of mega macro**

A mega macro is provided with 3-state output control signals so that a bus can be configured. Because there is a possibility that the input signal of a cell may float inside the ASIC, therefore, provide a circuit that prevents floating when using 3-state output signals.

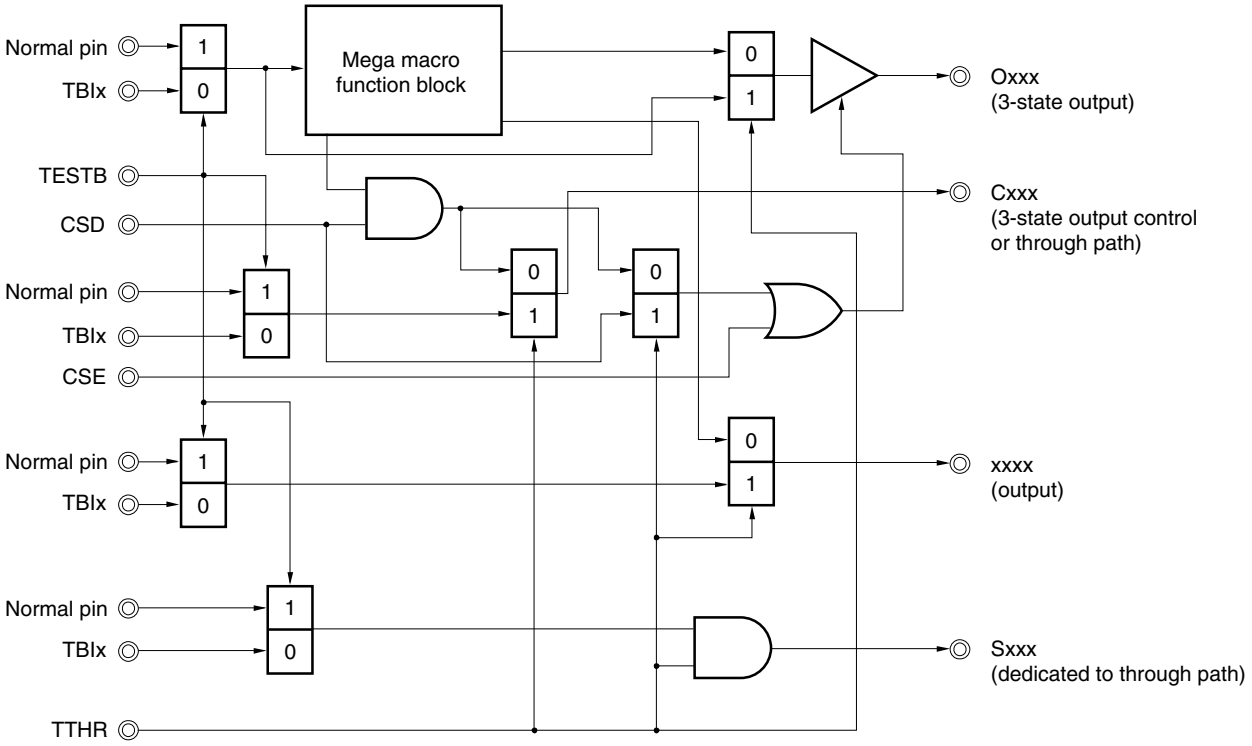
**(2) Test circuit for each mega macro**

Because the operation of each mega macro is tested using NEC's test pattern, be sure to design the test circuit so that the operation of each macro can be monitored from the external pins of the gate array without inverting the logic of the test pins of the macro and without going through a sequential circuit. Conduct a through path test as your application requires.

### 1.3.1 Internal configuration of mega macro

Figure 1-2 shows the internal configuration of the mega macro. The mega macro is provided with an output control circuit and a test circuit in the block that realizes the functions of the mega macro.

**Figure 1-2. Internal Circuit Configuration of Mega Macro**



### 1.3.2 Mode

The mega macro has several modes to facilitate application design and creating circuits. To control these modes, the following pins are provided:

- TESTB: Selects a test mode for each mega macro.
- TTHR: Selects a through path test mode.
- CSE: Forcibly enables the 3-state output pin of the mega macro. Fix the level of this pin by using F091.
- CSD: Controls the 3-state control pin of the mega macro.

#### (1) Operation mode of mega macro

The operation mode of the mega macro is selected by a combination of the TESTB and TTHR pins. Table 1-4 shows the truth table. Control the 3-state output pin separately.

**Table 1-4. Operation Modes of Mega Macro**

| TTHR | TESTB | Normal Input Pin | Test Input Pin | Mode |
|---|---|---|---|---|
| 0 | 0 | Invalid | Valid | Mega macro test mode |
| 0 | 1 | Valid | Invalid | Normal operation |
| 1 | 0 | Invalid | Valid | Post-macro stage test mode (through path test) |
| 1 | 1 | Valid | Invalid | Pre-macro stage test mode (through path test) |

- **Mega macro test mode**

  In this mode, the test input pins of the mega macro become valid and operate normally. The result of the normal operation is output from a function block of the mega macro to the output pins.

- **Normal operation**

  In this mode, the normal input pins of the mega macro become valid and operate normally. The result of the normal operation is output from a function block of the mega macro to the output pins.

- **Post-macro stage test mode (through path test)**

  In this mode, the test input pins of the mega macro become valid. The signals of the corresponding test input pins are output to the output pins as is.

- **Pre-macro stage test mode (through path test)**

  In this mode, the normal pins of the mega macro become valid. The signals of the corresponding normal input pins are output to the output pins as is.

### (2) Output control mode of mega macro

**Table 1-5. Output Control Truth Table of Mega Macro**

| TTHR | CSE | CSD | 3-State Output Pin[Note 1] | 3-State Control Pin | Other Output Pins | Output Pin Dedicated Through Path[Note 2] |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Hi-Z | 0 | Normal operation | 0 |
| 0 | 0 | 1 | Normal operation | Normal operation | | |
| 0 | 1 | 0 | Hi-Z is not output. | 0 | | |
| 0 | 1 | 1 | | Normal operation | | |
| 1 | 0 | 0 | Hi-Z | Through path | Through path | Through path |
| 1 | 0 | 1 | Through path | | | |
| 1 | 1 | × | | | | |

**Notes 1.** Control the output buffer by using the CSD pin when CSE = 0 for the through path test.

**2.** Some macros do not have a dedicated through path output pin.

Exercise care in controlling the 3-state output pin of the mega macro so that a high impedance is not input to the circuit in the stage succeeding the mega macro. If CSE is fixed to “L” when conducting a through path test, control the control signals so that the bus does not float or fight.

### 1.3.3 Connecting mega macro and user circuit

#### (1) Basic rule

**<1> Connection to test each mega macro**

Basically, externally connect all the output pins, except the test input and 3-state control pins of the mega macro, as the pins of the gate array.

**<2> Adjusting fanout**

Make sure that the fanout limit is not exceeded when connecting the input and output pins of the mega macro to the user circuit. For the fanin and fanout limits of the mega macro, refer to the description of each macro.

**<3> Handling of unused pins**

Fix the input pins not used with the mega macro to “H” or “L” level by using F091. The output pins not used with the mega macro are used to test each mega macro; therefore, connect all the pins, except the 3-state control pins, for testing.

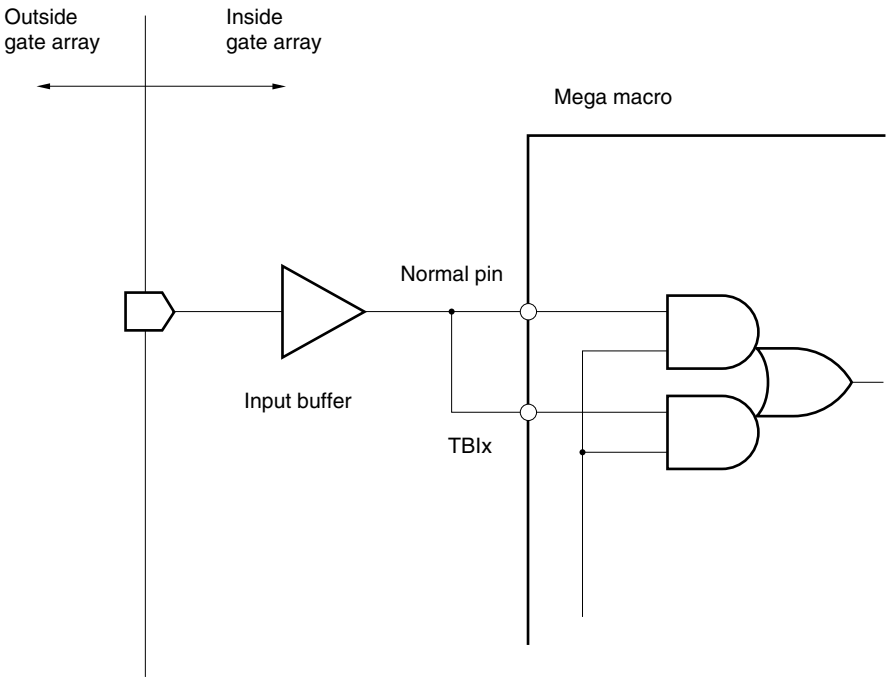
**(2) Connection of mega macro and interface block**

How to connect the pins of the mega macro to the pins of the gate array via interface block is explained below.

**<1> Input pins**

Connect input pins to a normal pin and a test pin via an input buffer (this pin is shared between normal operation and testing each macro).

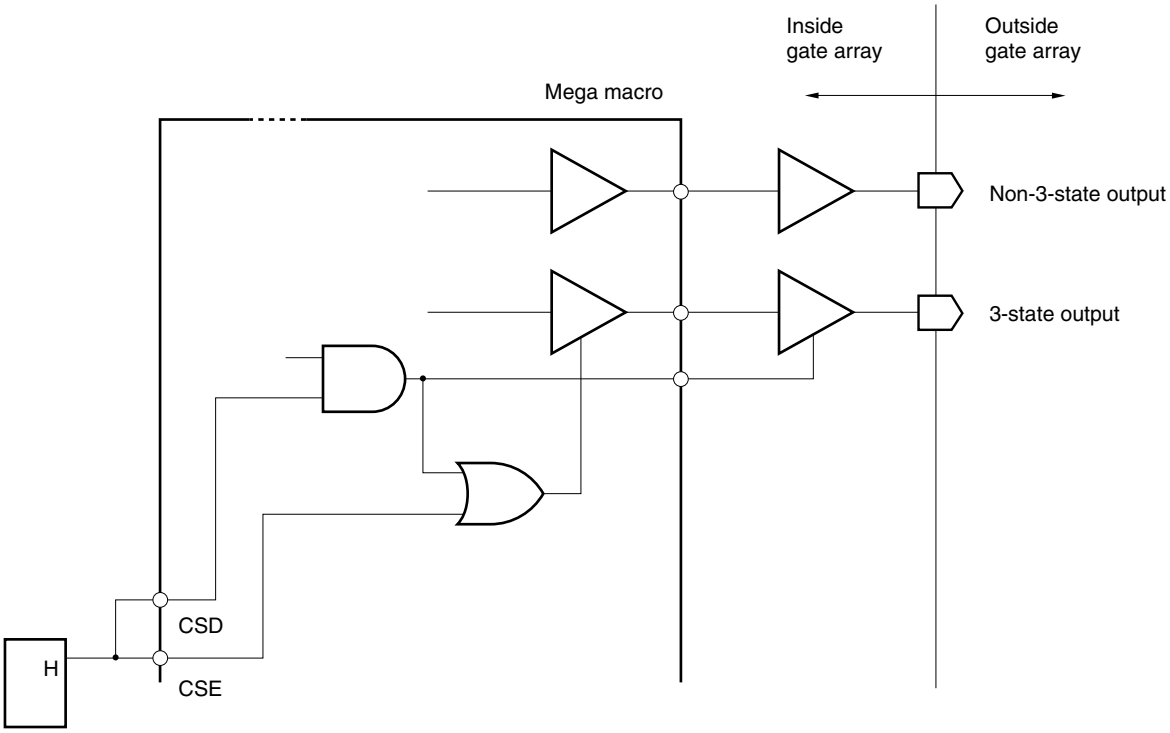
**Figure 1-3. Connection with Input Pins**



**<2> Output pins**

Connect the non-3-state output pins of the macro to output pins via an output buffer as is. Connect the 3-state output pins of the macro to the signal input of the 3-state buffer, and connect the 3-state control pins to the control signal input of the 3-state buffer. At this time, control CSE and CSD of the macro to make sure that the signal input of the 3-state buffer does not float.

**Figure 1-4. Connection with Output Pins**




**<3> Bidirectional pins**

Connecting the input pins or output pins of the mega macro as the gate array pins via a bidirectional buffer is possible. However, note the following.

- When connecting input pin to bidirectional pin
  Be sure to set the input mode when testing the macro.
- When connecting output pin to bidirectional pin
  Be sure to set the output mode when testing the macro.

### (3) Connection of mega macro and function cell

#### <1> Output and input pins other than 3-state pins

Connect these pins to function cells so that the fanout limitations are satisfied. In doing so, make sure that all the input pins and all the output pins except the 3-state control pins can be monitored from outside the gate array.

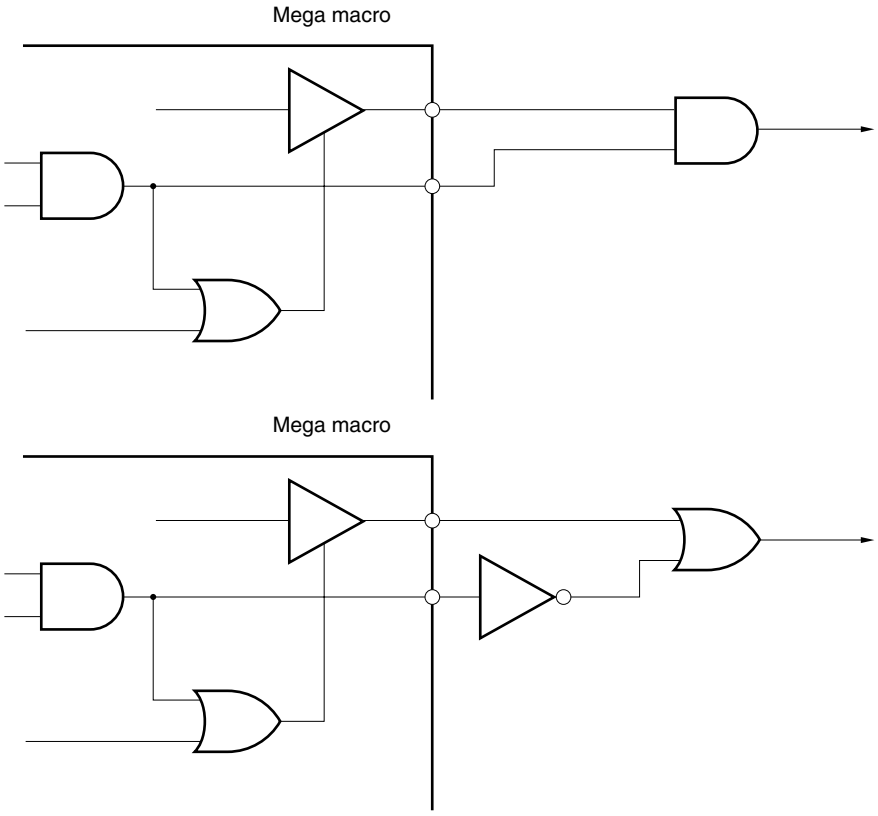
#### <2> 3-state output pins

Because a high impedance may be output to the output pin of the macro, take countermeasures against the high impedance in any of the following three ways:

- **By using AND, NAND, OR, or NOR gate in the next stage**

  Connect an AND, NAND, OR, or NOR gate with three inputs or less, and input signals including the control signals. When making this connection, determine the logic so that the output value of the AND, NAND, OR, or NOR gate is determined regardless of the 3-state output of the macro when the control signal is inactive. Do not use any gate other than above.

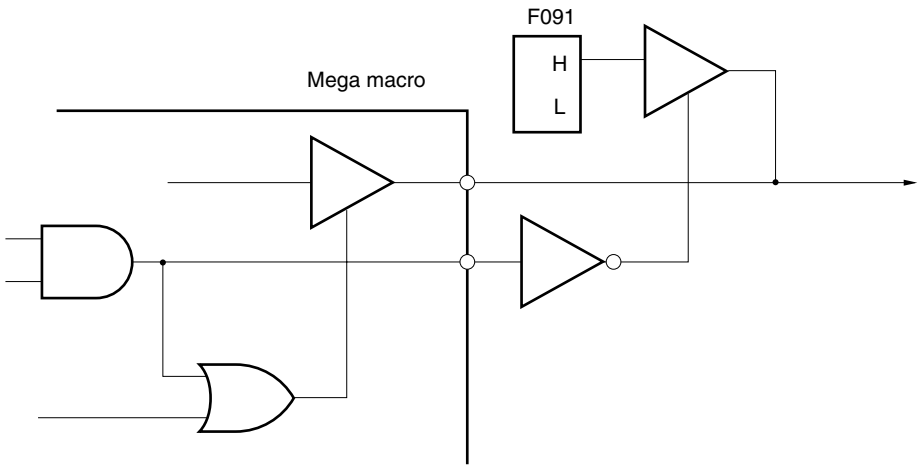
**Figure 1-5. Examples of Using AND and OR Gates**



- **Configure bus with F091**

  Assert the control signal of the 3-state block connected to F091 active when the 3-state output of the macro is inactive (high-impedance), by using F091 and a 3-state buffer as shown in Figure 1-6.

**Figure 1-6. Example of Connecting Bus by Using F091**




- **Fix CSE to "H"**

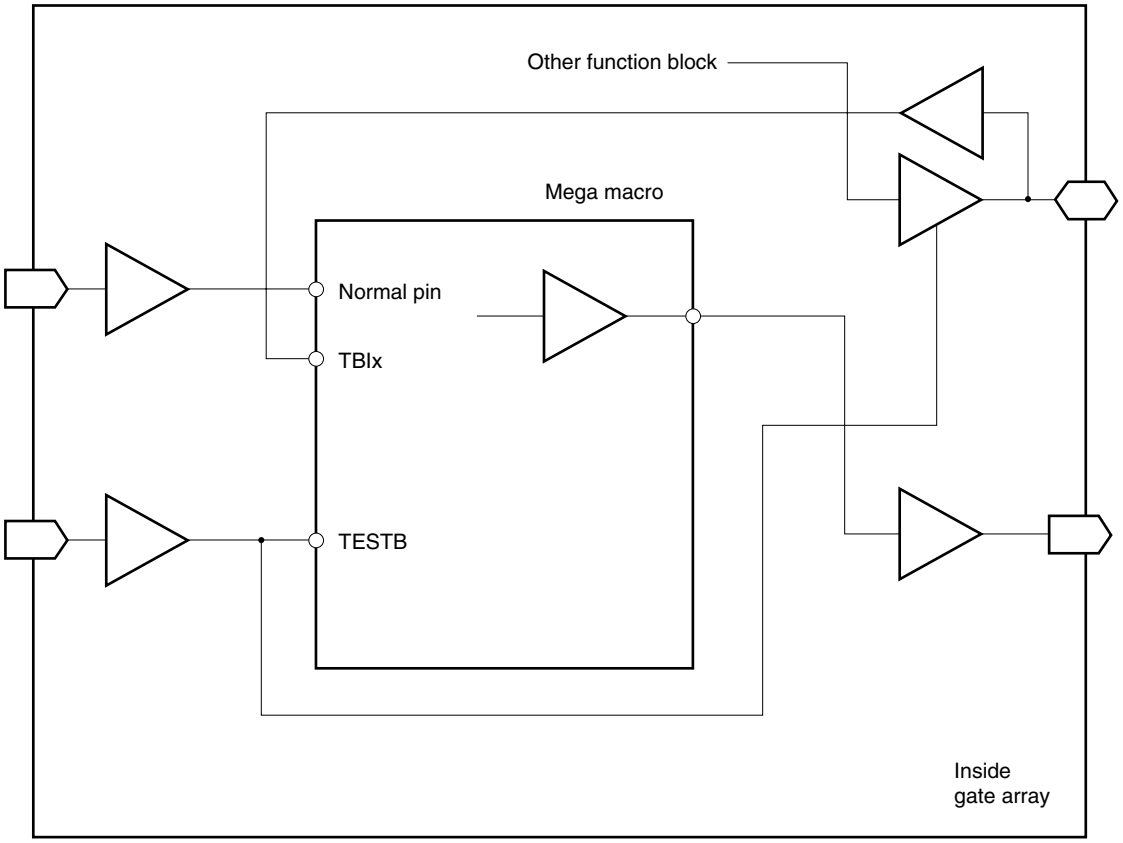
  If CSE is fixed to "H", a high impedance is not output to the output pin of the macro. Therefore, no special countermeasures against high impedance are necessary.

### 1.3.4 Assigning test signal

Although test pins are assigned to test each mega macro, a test signal and a normal signal are shared in most cases. To share a normal signal and a test signal, bear in mind the following three points:

- When pins are shared in the normal mode and test mode, use the control pins of the interface block so that a test signal can be accurately input or output in the test mode.
- Supply the clock signal of the mega macro from an input pin without sharing the pin with any other output signal, regardless of whether the pin is for normal input or test input.
- Note that normal pins using a GTL interface buffer, N-ch open-drain buffer, or CMOS 5 V withstand voltage output buffer cannot be used as test pins.

**Figure 1-7. Example of Sharing Input Pin and Normal Output Pin of Mega Macro**



### 1.3.5 Through path test

A through path test is used to test the user circuit connected to the mega macro. The signals input to the normal pins or test pins are output to the output pin of the macro, bypassing the macro function realization block.

By selecting a normal pin or test pin by using TESTB, the pre-macro-stage circuit and post-macro-stage circuit can be tested. To test the pre-macro-stage circuit, the output signals of the user circuit connected to the input pins of the mega macro are output to an output pin of the macro as is. To test the post-macro-stage, the signals input from the test pins of the mega macro are supplied to the user circuit via the output pins of the macro and tested.

**Figure 1-8. Illustration of Normal Operation**

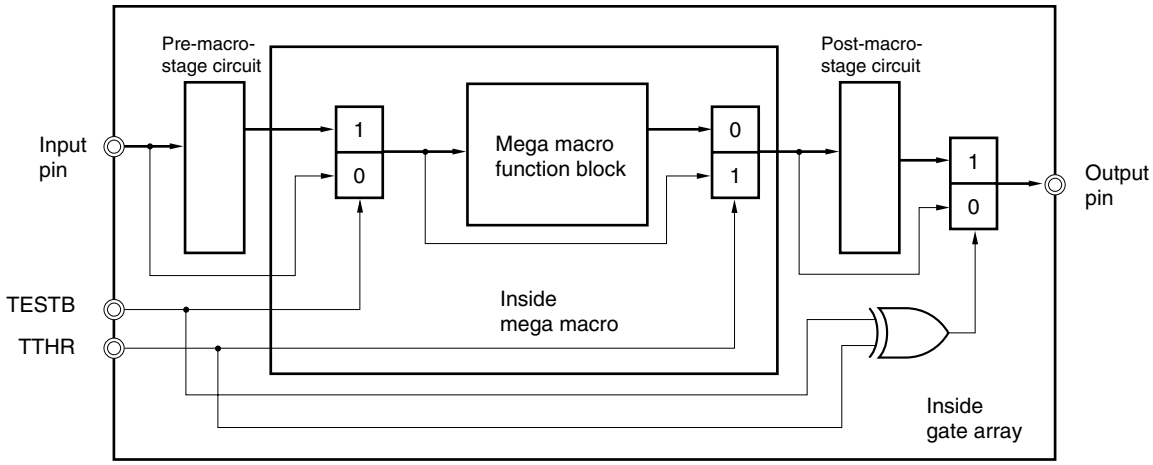



**Figure 1-9. Illustration of Testing Each Mega Macro**

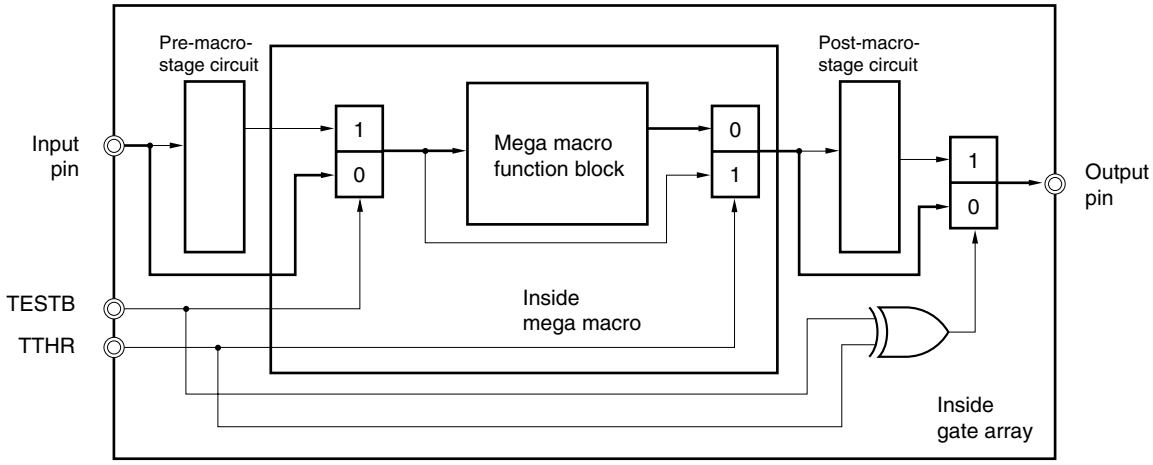


**Figure 1-10. Illustration of Testing Pre-Macro-Stage Circuit (Through Path Test)**

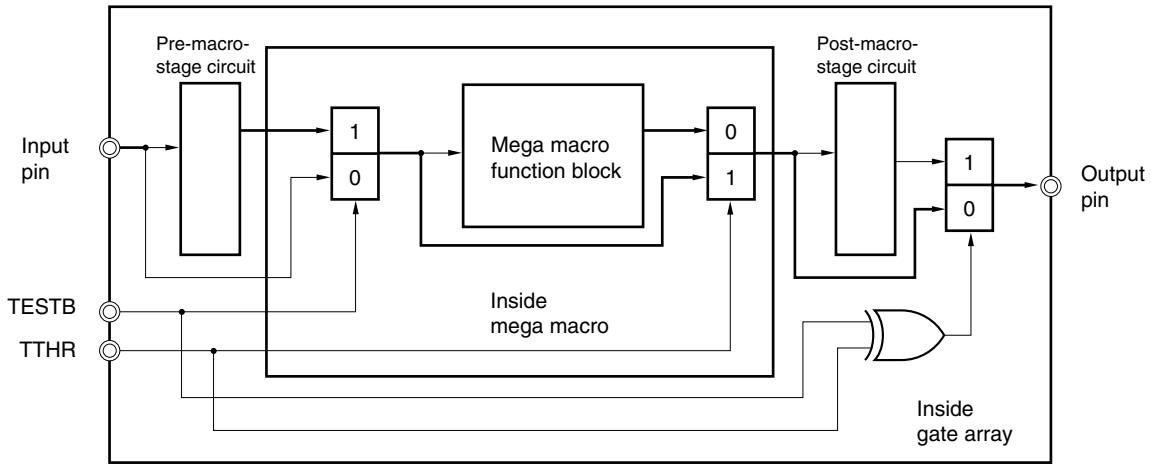
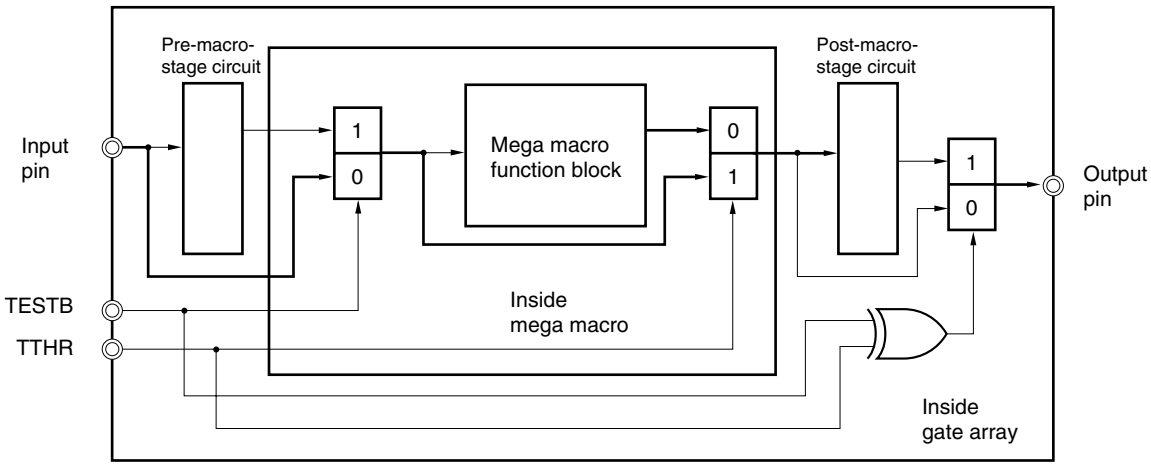



**Figure 1-11. Illustration of Testing Post-Macro-Stage Circuit (Through Path Test)**



### 1.3.6 Circuit example

An example of a circuit when mounting multiple mega macros is shown below.

**Figure 1-12. Example of Circuit When Mounting Multiple Mega Macros**

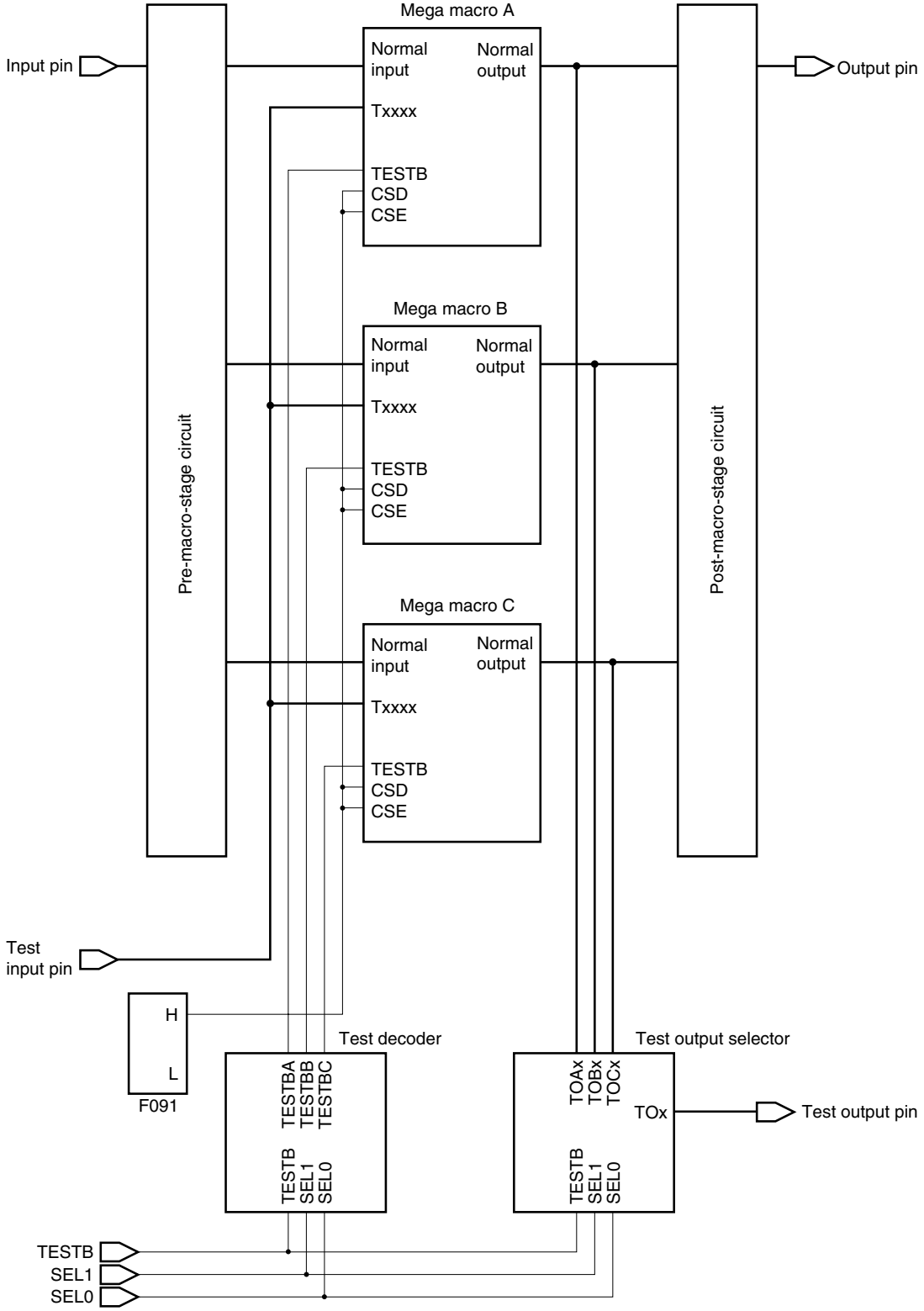


**Table 1-6. Test Decoder Truth Table**

| Input | | | Output | | |
|---|---|---|---|---|---|
| TESTB | SEL1 | SEL0 | TESTBA | TESTBB | TESTBC |
| 1 | × | × | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |

×: “0” or “1”

**Table 1-7. Test Output Selector Truth Table**

| Input | | | | | | Output |
|---|---|---|---|---|---|---|
| TESTB | SEL1 | SEL0 | TOA× | TOB× | TOC× | TO× |
| 1 | × | × | × | × | × | × |
| 0 | 0 | 0 | TOA× | × | × | TOA× |
| 0 | 0 | 1 | × | TOB× | × | TOB× |
| 0 | 1 | 0 | × | × | TOC× | TOC× |

×: “0” or “1”

During the mega macro test, create the circuit and initialization pattern so that only TESTB of the target mega macro is “0” and TESTB of other mega macros is “1”.

Take care to avoid floating because the mega macro outputs include 3-state outputs.

## 1.4 Notes on Creating Test Pattern

This section describes notes on creating a test pattern.

### 1.4.1 Notes on creating a mega macro initialization pattern

Because the internal circuit of the mega macro is not initialized unless an initialization pattern is used, be sure to add an initialization pattern for the mega macro at the beginning of the test pattern. Moreover, because the initialization pattern differs depending on the mega macro, initialize each macro by referring to the corresponding field of each macro.

Initialization may not be performed correctly because of the circuit configuration if a loop circuit exits between the mega macro and other user circuits. Therefore, also initialize any sequential circuit that constitutes a loop.

If the test pattern is divided, provide an initialization pattern for each test pattern.

### 1.4.2 Notes on creating a mega macro test setting pattern

The following six cautions must be observed to ensure normal operation of mega macro test patterns.

**(1) Timing specification is prohibited**

Do not specify RZ or the NRZ modulation.

**(2) Initialization of a user logic other than a mega macro**

Initialize so that a defined value is input to the mega macro normal pin from the user logic.

**(3) Input of an undefined value (X) and Hi-Z to the gate array input pin is prohibited**

Input a defined value to the gate array input pin.

**(4) Expected values from pins other than the mega macro test output pin**

Handle expected values from pins other than the mega macro test output pin as “don’t care”.

Input an expected value to the oscillation block output.

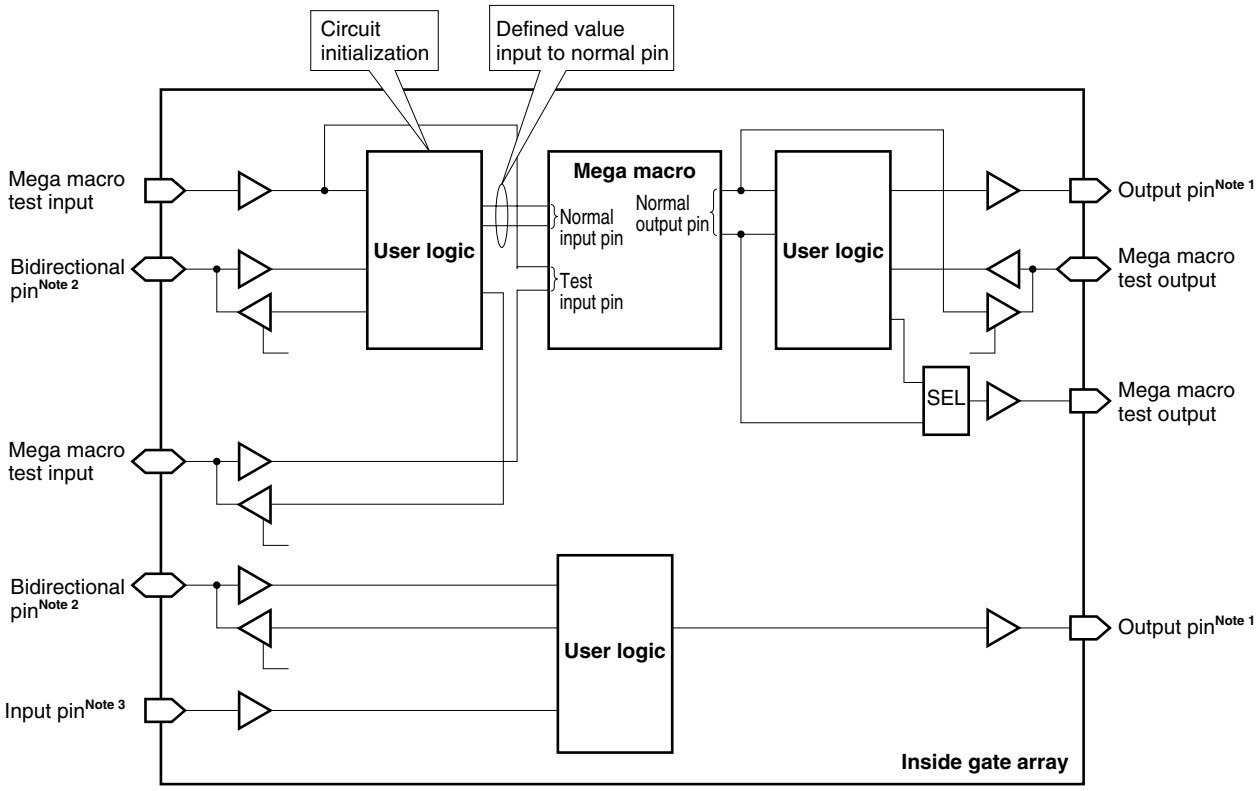
**(5) Defining input mode for the input/output buffer**

Define the direction of input/output, regardless of the output state of the mega macro test pin.

**(6) Dealing with a mega macro that cannot be accessed directly**

Settings to ensure that the mega macro is visible from outside the gate array should also be incorporated as a mega macro test setting pattern if the TESTB pin cannot be directly accessed externally or the unit does not have a decoder configuration.

**Figure 1-13. Creating a Mega Macro Test Setting Pattern**




**Notes 1.** don't care

**2.** Define input/output direction
During input: defined value input
During output: don't care

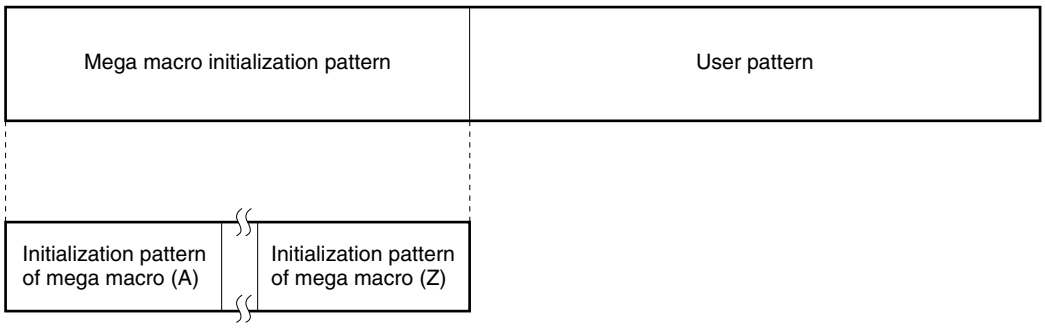
**3.** Defined value input

### 1.4.3 Limit of maximum number of test patterns

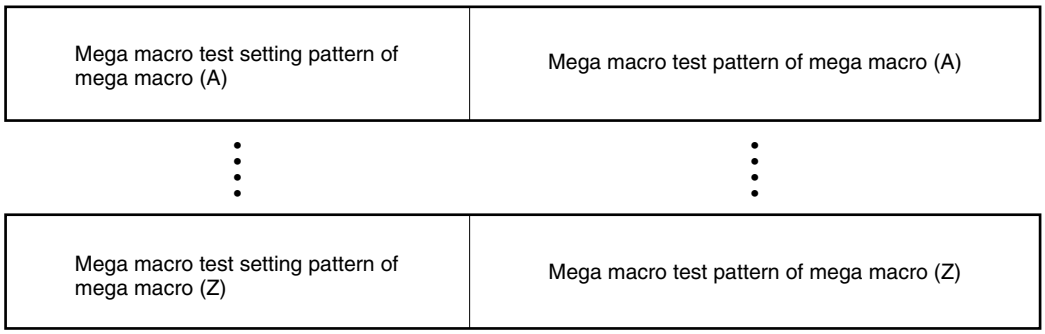
A test pattern is configured as shown in Figure 1-14. Make sure that the total number of these patterns does not exceed the maximum number of test patterns determined for each series.

**Figure 1-14. Breakdown of Test Pattern**

**(a) Mega macro initialization pattern and user pattern**




**(b) Mega macro test setting pattern and mega macro test pattern**




**Remark** Indicates configuration when multiple (A) to (Z) mega macros are used.

**(1) Mega macro initialization pattern**

Create a pattern for each mega macro mounted.

**(2) User pattern**

This is a test pattern for the circuit created by the user. Change the levels of all the I/O pins related to the functions used by the mega macro from “0” to “1” or from “1” to “0”.

**(3) Mega macro test setting pattern**

Create a pattern for each mega macro mounted.

**(4) Mega macro test pattern**

This pattern is used by NEC for delivery inspection and does not have to be created by the user. The test pattern length basically differs depending on the types of and the total number of macros used. For details, refer to **Table 1-3 Number of Test Patterns of Each Mega Macro (Per Macro)**.

### 1.4.4 Notes on clock input

Supply a clock signal[Note] from an input pin, not a bidirectional pin, regardless of whether the pin is a normal pin or test pin.

**Note** The “clock signal” means the signal described as “clock” in the Function column in **2.1**, **3.1**, **4.1**, and **5.2**.

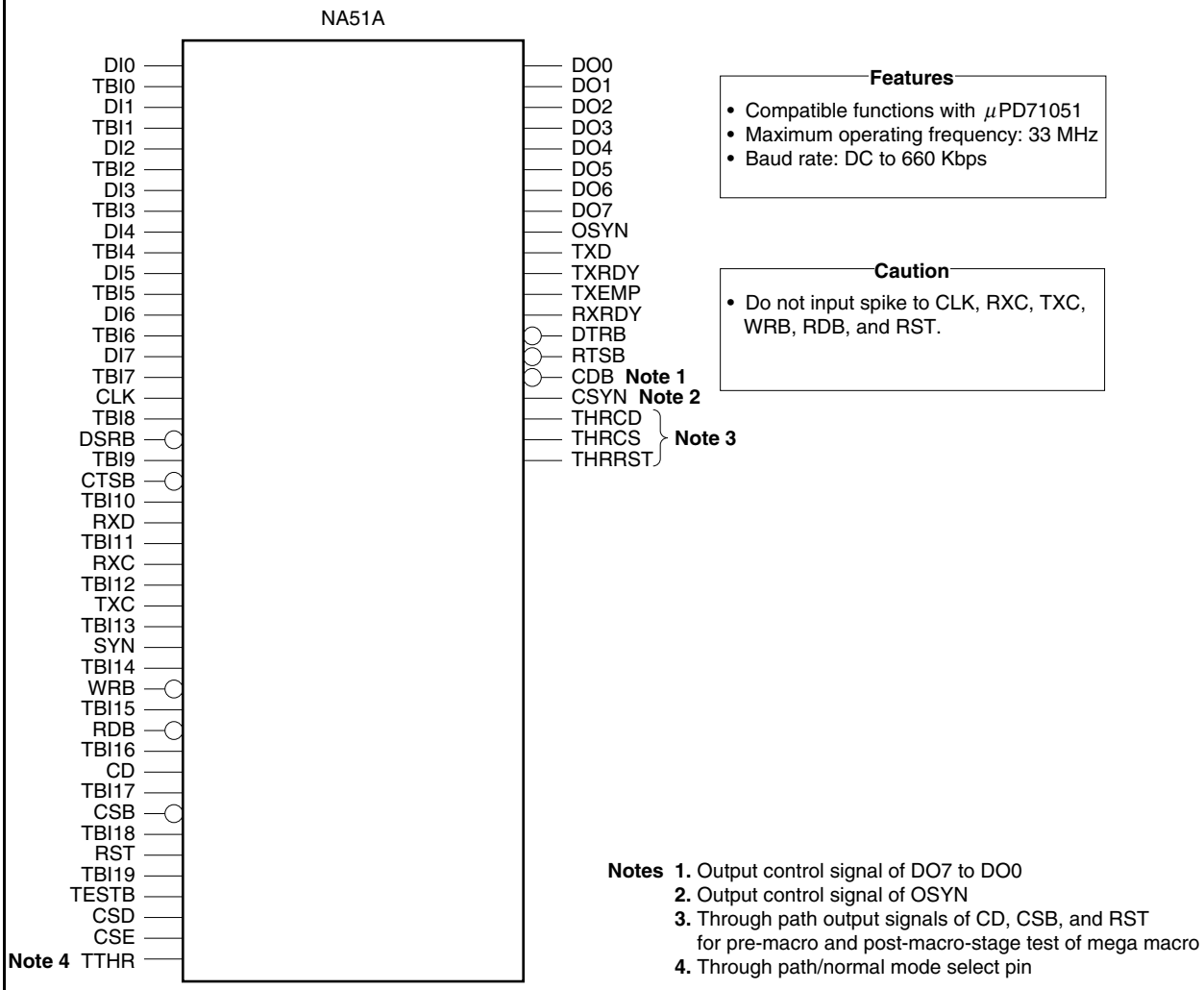
## 1.5 Other Points to Be Noted

(1) Each mega macro and its equivalent general-purpose product may partly differ from each other in terms of functions. Refer to the description of each mega macro.
(2) Note that an unexpected timing error may occur inside the mega macro when simulation is executed in the through path mode.
(3) For interfacing, create a mega macro test specification and submit it to NEC by referring to **A.1 Mega Macro Test Specification**.

# CHAPTER 2 NA51A MACRO

This chapter explains the functions of the NA51A.

| Block Type | Function |
|---|---|
| NA51A | Universal synchronous/asynchronous receiver/transmitter |




**Features**

- Compatible functions with μPD71051
- Maximum operating frequency: 33 MHz
- Baud rate: DC to 660 Kbps

**Caution**

- Do not input spike to CLK, RXC, TXC, WRB, RDB, and RST.

**Notes 1.** Output control signal of DO7 to DO0
**2.** Output control signal of OSYN
**3.** Through path output signals of CD, CSB, and RST for pre-macro and post-macro-stage test of mega macro
**4.** Through path/normal mode select pin

**Remark** The input signal pins with “TBI” prefixed are test pins.

| | |
|---|---|
| Number of cells used (configuration) | 2904 (121 × 24) |
| Mega macro test pattern length | 12874 |

## 2.1 NA51A Pins

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| DI0 | Input | Data bus input signal (LSB) | | TBI0 | 2.4 | F424 |
| DI1 | Input | Data bus input signal | | TBI1 | 2.4 | F424 |
| DI2 | Input | Data bus input signal | | TBI2 | 2.4 | F424 |
| DI3 | Input | Data bus input signal | | TBI3 | 2.4 | F424 |
| DI4 | Input | Data bus input signal | | TBI4 | 2.4 | F424 |
| DI5 | Input | Data bus input signal | | TBI5 | 2.4 | F424 |
| DI6 | Input | Data bus input signal | | TBI6 | 2.4 | F424 |
| DI7 | Input | Data bus input signal (MSB) | | TBI7 | 2.4 | F424 |
| CLK | Input | System clock signal | | TBI8 | 2.5 | F101 |
| DSRB | Input | General-purpose input pin (Data Set Ready) | Low | TBI9 | 2.4 | F424 |
| CTSB | Input | Transmit control input pin (Clear To Send) | Low | TBI10 | 1.1 | L101 |
| RXD | Input | Serial data receive pin | | TBI11 | 2.4 | F424 |
| RXC | Input | Receive clock signal | | TBI12 | 1.1 | L101 |
| TXC | Input | Transmit clock signal | | TBI13 | 1.1 | L101 |
| SYN | Input | Used to detect external synchronization in synchronization mode | | TBI14 | 1.1 | L101 |
| WRB | Input | Write signal | Low | TBI15 | 1.1 | L101 |
| RDB | Input | Read signal | Low | TBI16 | 1.1 | L101 |
| CD | Input | “H”: Control word<br>“L”: Character data | | TBI17 | 1.1 | L101 |
| CSB | Input | Chip select signal | Low | TBI18 | 1.1 | L101 |
| RST | Input | System reset signal | High | TBI19 | 1.1 | L101 |
| TESTB | Input | Test/normal mode selection<br>“H”: Normal mode<br>“L”: Test mode | | – | 2.4 | F154 |
| CSD | Input | 3-state output control | | – | 2.4 | F111 |
| CSE | Input | 3-state output control | | – | 1.1 | L111 |
| TTHR | Input | Through path/normal mode select signal<br>“H”: Through path mode<br>“L”: Normal mode | | – | 2.5 | F101 |
| DO0 | Output | Data bus output signal (LSB) | | – | 99.0 | F53F |
| DO1 | Output | Data bus output signal | | – | 99.0 | F53F |
| DO2 | Output | Data bus output signal | | – | 99.0 | F53F |
| DO3 | Output | Data bus output signal | | – | 99.0 | F53F |
| DO4 | Output | Data bus output signal | | – | 99.0 | F53F |
| DO5 | Output | Data bus output signal | | – | 99.0 | F53F |
| DO6 | Output | Data bus output signal | | – | 99.0 | F53F |
| DO7 | Output | Data bus output signal (MSB) | | – | 99.0 | F53F |

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| OSYN | Output | In synchronous mode:<br>Internal synchronization detection signal<br>In asynchronous mode:<br>break signal | | – | 98.0 | F53G |
| TXD | Output | Serial data transmit pin | | – | 107.0 | F154 |
| TXRDY | Output | Signal indicating transmit data write enable | | – | 107.0 | F154 |
| TXEMP | Output | Signal indicating that the two transmit data buffers are empty | | – | 107.0 | F154 |
| RXRDY | Output | Signal indicating receive data read enable | | – | 107.0 | F154 |
| DTRB | Output | General-purpose output pin (data terminal ready) | | – | 107.0 | F154 |
| RTSB | Output | General-purpose output pin (request to send) | | – | 107.0 | F154 |
| CDB | Output | Enable signal of data bus | | – | 107.0 | F154 |
| CSYN | Output | Enable signal of OSYN | | – | 107.0 | F154 |
| THRCD | Output | Through path output pin | | – | 26.0 | F312 |
| THRCS | Output | Through path output pin | | – | 26.0 | F312 |
| THRRST | Output | Through path output pin | | – | 26.0 | F312 |
| TBI0 | Input | Test input | | – | 2.5 | F424 |
| TBI1 | Input | Test input | | – | 2.5 | F424 |
| TBI2 | Input | Test input | | – | 2.5 | F424 |
| TBI3 | Input | Test input | | – | 2.5 | F424 |
| TBI4 | Input | Test input | | – | 2.5 | F424 |
| TBI5 | Input | Test input | | – | 2.5 | F424 |
| TBI6 | Input | Test input | | – | 2.5 | F424 |
| TBI7 | Input | Test input | | – | 2.5 | F424 |
| TBI8 | Input | Test input | | – | 2.5 | F101 |
| TBI9 | Input | Test input | | – | 2.5 | F424 |
| TBI10 | Input | Test input | | – | 1.1 | L101 |
| TBI11 | Input | Test input | | – | 2.5 | F424 |
| TBI12 | Input | Test input | | – | 1.1 | L101 |
| TBI13 | Input | Test input | | – | 1.1 | L101 |
| TBI14 | Input | Test input | | – | 1.1 | L101 |
| TBI15 | Input | Test input | | – | 1.1 | L101 |
| TBI16 | Input | Test input | | – | 1.1 | L101 |
| TBI17 | Input | Test input | | – | 1.1 | L101 |
| TBI18 | Input | Test input | | – | 1.1 | L101 |
| TBI19 | Input | Test input | | – | 1.1 | L101 |

**Remark** Input: Input pin
Output: Output pin

**Remarks 1.** TBIx is a test input pin. A signal can be input from TBIx by making the TESTB input low. Make a connection so that signals can be directly input to the mega macro from outside the gate array in the test mode. "Directly" here means a circuit configuration where the input signal is not inverted and no sequential circuit such as a flip-flop is inserted in between.

| TESTB | Input Pin |
|---|---|
| 1 | Normal pin[Note] |
| 0 | TBIx |

**Note** Input a defined value of 0 or 1 to the test input pins in the normal mode (it does not matter if 0 and 1 are mixed).

**2.** Functions of CSD input and CSE input

CSE input : Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input : Turns off (high-impedance: Hi-Z) of all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

| CSE | CSD | Status of Output Pin | Status of 3-State Output Pin[Note] |
|---|---|---|---|
| 0 | 0 | Normal operation | Hi-Z |
| 0 | 1 | Normal operation | Normal operation |
| 1 | – | Normal operation | Hi-Z is not output. |

**Note** 3-state pins are DO7 to DO0 and OSYN.

**3.** When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

| "Hi-Z" Pin | Corresponding Output Control Signal and Output | |
|---|---|---|
| DO7 to DO0 | CDB | 0 |
| OSYN | CSYN | 0 |

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

**4.** CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

**Remarks 5.** Operating status of output pin depending on combination of TTHR, CSE, and CSD

| TTHR Pin | CSE Pin | CSD Pin | 3-State Output Pin (DOx) | 3-State Control Pin (CDB(SD)) | Other Pins | Through Path Pin (Output THRxxx) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Hi-Z | 0 | Normal operation | 0 |
| | | 1 | Normal operation | Normal operation | | |
| | 1 | 0 | Hi-Z is not output. | 0 | | |
| | | 1 | | Normal operation | | |
| 1 | 0 | 0 | Hi-Z | Through path | Through path | Through path |
| | | 1 | Through path | | | |
| | 1 | × | | | | |

**6.** I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

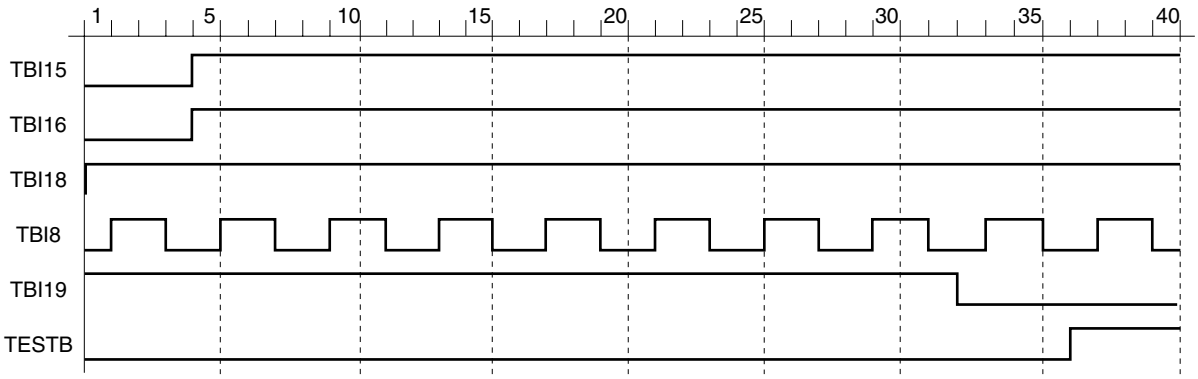
| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| DO0 | DI0 | TBI0 |
| DO1 | DI1 | TBI1 |
| DO2 | DI2 | TBI2 |
| DO3 | DI3 | TBI3 |
| DO4 | DI4 | TBI4 |
| DO5 | DI5 | TBI5 |
| DO6 | DI6 | TBI6 |
| DO7 | DI7 | TBI7 |
| OSYN | CLK | TBI8 |
| TXD | DSRB | TBI9 |

| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| TXRDY | CTSB | TBI10 |
| TXEMP | RXD | TBI11 |
| RXRDY | RXC | TBI12 |
| DTRB | TXC | TBI13 |
| RTSB | SYN | TBI14 |
| CDB | WRB | TBI15 |
| CSYN | RDB | TBI16 |
| THRCD | CD | TBI17 |
| THRCS | CSB | TBI18 |
| THRRST | RST | TBI19 |

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high impedance).

## 2.2 NA51A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.




Input “0” or “1” to the other input pins (normal input and test input).
Exercise care that “X” is not input.

- **Value of mega macro output pin after initialization pattern**

| Pin Name | Status |
|---|---|
| DO7 to DO0 | Hi-Z |
| OSYN | 0 |
| TXD | 1 |
| TXRDY | 0 |
| TXEMP | 1 |
| RXRDY | 0 |
| DTRB | 1 |
| RTSB | 1 |
| CDB | 0 |
| CSYN | 1 |
| THRCD | 0 |
| THRCS | 0 |
| THRRST | 0 |

**Cautions 1. NA51A is in the standby mode after the initialization pattern.**
**2. The clock is necessary during reset (the reset pulse width must be at least 6 clocks).**
**3. Configure the circuit of the following input pins so that spike is not input:**
**CLK, RXC, TXC, WRB, RDB, RST**

## 2.3 Delay Time

Refer to **1.2.4 Delay time**.

## 2.4 AC Characteristics ($T_A$ = –40 to 85°C, $V_{DD}$ = 3.3 ±0.3 V)

### (1) Read cycle

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Address (CSB, CD) setup time (to RDB ↓) | $t_{SAR}$ | 2 | | ns |
| Address (CSB, CD) hold time (from RDB ↑) | $t_{HRA}$ | 0 | | ns |
| RDB pulse width | $t_{RRL}$ | 30 | | ns |
| Data delay time (to RDB ↓) | $t_{DRD}$ | 3 | 9 | ns |
| Data float delay time (to RDB ↑) | $t_{FRD}$ | 1 | 3 | ns |
| Port (DSRB, CTSB) setup time (to RDB ↓) | $t_{SPR}$ | 20 | | $t_{CYK}$ |
| CDB high delay time (to RDB ↓) | $t_{CDHR}$ | 1 | 3 | ns |
| CDB low delay time (to RDB ↑) | $t_{CDLR}$ | 1 | 3 | ns |

### (2) Write cycle

| Parameter | | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Address (CSB, CD) setup time (to WRB ↓) | | $t_{SAW}$ | 1 | | ns |
| Address (CSB, CD) hold time (from WRB ↑) | | $t_{HWA}$ | 0 | | ns |
| WRB pulse width | | $t_{WWL}$ | 30 | | ns |
| Data setup time (to WRB ↑) | | $t_{SDW}$ | 1 | | ns |
| Data hold time (from WRB ↑) | | $t_{HWD}$ | 1 | | ns |
| Port (DTRB, RTSB), TXEN delay time (to WRB ↑) | | $t_{DWP}$ | | 8 | $t_{CYK}$ |
| Write recovery time | When mode is specified | $t_{RV}$ | 6 | | $t_{CYK}$ |
| | Asynchronous mode | | 12 | | $t_{CYK}$ |
| | Synchronous mode | | 16 | | $t_{CYK}$ |

### (3) Other timing

| Parameter | | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Clock cycle | | $t_{CYK}$ | 30 | | ns |
| Clock pulse high-level width | | $t_{KKH}$ | 13.5 | | ns |
| Clock pulse low-level width | | $t_{KKL}$ | 13.5 | | ns |
| TXD delay time (to TXCB ↓) | | $t_{DTKTD}$ | 1 | 5 | ns |
| Setup time of all input pins[Note 1] (to CLK ↑) | | $t_{SU}$ | 10 | | ns |
| Transmitter input clock pulse low-level width | 1 × BR | $t_{TKTKL}$ | 12 | | $t_{CYK}$ |
| | 16 × BR, 64 × BR | | 1 | | $t_{CYK}$ |
| Transmitter input clock pulse high-level width | 1 × BR | $t_{TKTKH}$ | 15 | | $t_{CYK}$ |
| | 16 × BR, 64 × BR | | 3 | | $t_{CYK}$ |
| Transmitter input clock frequency | 1 × BR | $f_{TK}$[Note 2] | DC | 660 | kHz |
| | 16 × BR | | DC | 4400 | kHz |
| | 64 × BR | | DC | 4400 | kHz |
| Receiver input clock pulse low-level width | 1 × BR | $t_{RKRKL}$ | 12 | | $t_{CYK}$ |
| | 16 × BR, 64 × BR | | 1 | | $t_{CYK}$ |
| Receiver input clock pulse high-level width | 1 × BR | $t_{RKRKH}$ | 15 | | $t_{CYK}$ |
| | 16 × BR, 64 × BR | | 3 | | $t_{CYK}$ |
| Receiver input clock frequency | 1 × BR | $f_{RK}$[Note 2] | | 600 | kHz |
| | 16 × BR | | | 4400 | kHz |
| | 64 × BR | | | 4400 | kHz |
| RXD setup time (to sampling pulse ↑) | | $t_{SRDSP}$[Note 3] | 1 | | μs |
| RXD hold time (from sampling pulse ↓) | | $t_{HSPRD}$[Note 3] | 1 | | μs |
| TXEM delay time | | $t_{DTXEP}$ | | 20 | $t_{CYK}$ |
| TXRD delay time (to TXRD ↑) | | $t_{DTXR}$ | | 8 | $t_{CYK}$ |
| TXRD delay time (to TXRD ↓) | | $t_{DWTXR}$ | 2 | 6 | ns |
| RXRD delay time (to RXRD ↑) | | $t_{DRXR}$ | | 26 | $t_{CYK}$ |
| RXRD delay time (to RXRD ↓) | | $t_{DRRXR}$ | 1 | 4 | ns |
| OSYN output delay time (internal synchronization) | | $t_{DRKSY}$ | | 26 | $t_{CYK}$ |
| SYN input setup time (external synchronization) | | $t_{SSYRK}$ | 18 | | $t_{CYK}$ |
| Reset pulse high-level width | | $t_{RST}$ | 6 | | $t_{CYK}$ |

**Notes 1.** Excluding test input pins.

**2.** The frequency of TXC and RXC is limited in respect to CLK as follows:

$1 \times BR$: $f_{TK}$ or $f_{RK} \leq 1/30\ t_{CYK}$

$16 \times BR$, $64 \times BR$: $f_{TK}$ or $f_{RK} \leq 1/4.5\ t_{CYK}$

**3.** In asynchronous mode ($16 \times BR$, $64 \times BR$), there is no problem if the bit widths of RXD serial inputs are equal to the set number of bits or set transfer rate length.

In asynchronous mode ($1 \times BR$) and synchronous mode, $3 \times t_{CYK}$ or more are required for both $t_{SRDSP}$ and $t_{HSPRD}$.

**Remarks 1.** The system clock must be input during reset.

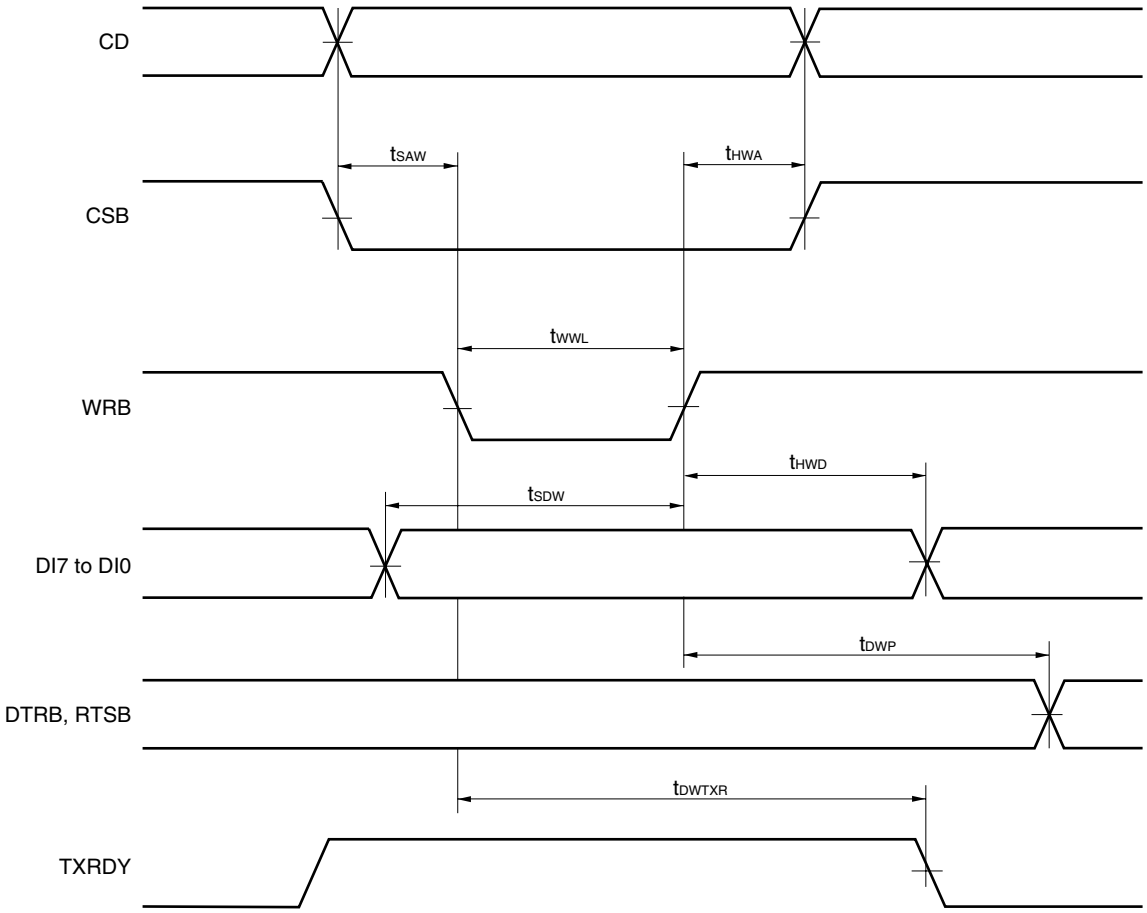
**2.** Updating the status is delayed by up to $28t_{CYK}$ after an event has influenced the status.

**3.** The output load conditions of the propagation delay time are fanout: 1, wiring length: 0 mm.

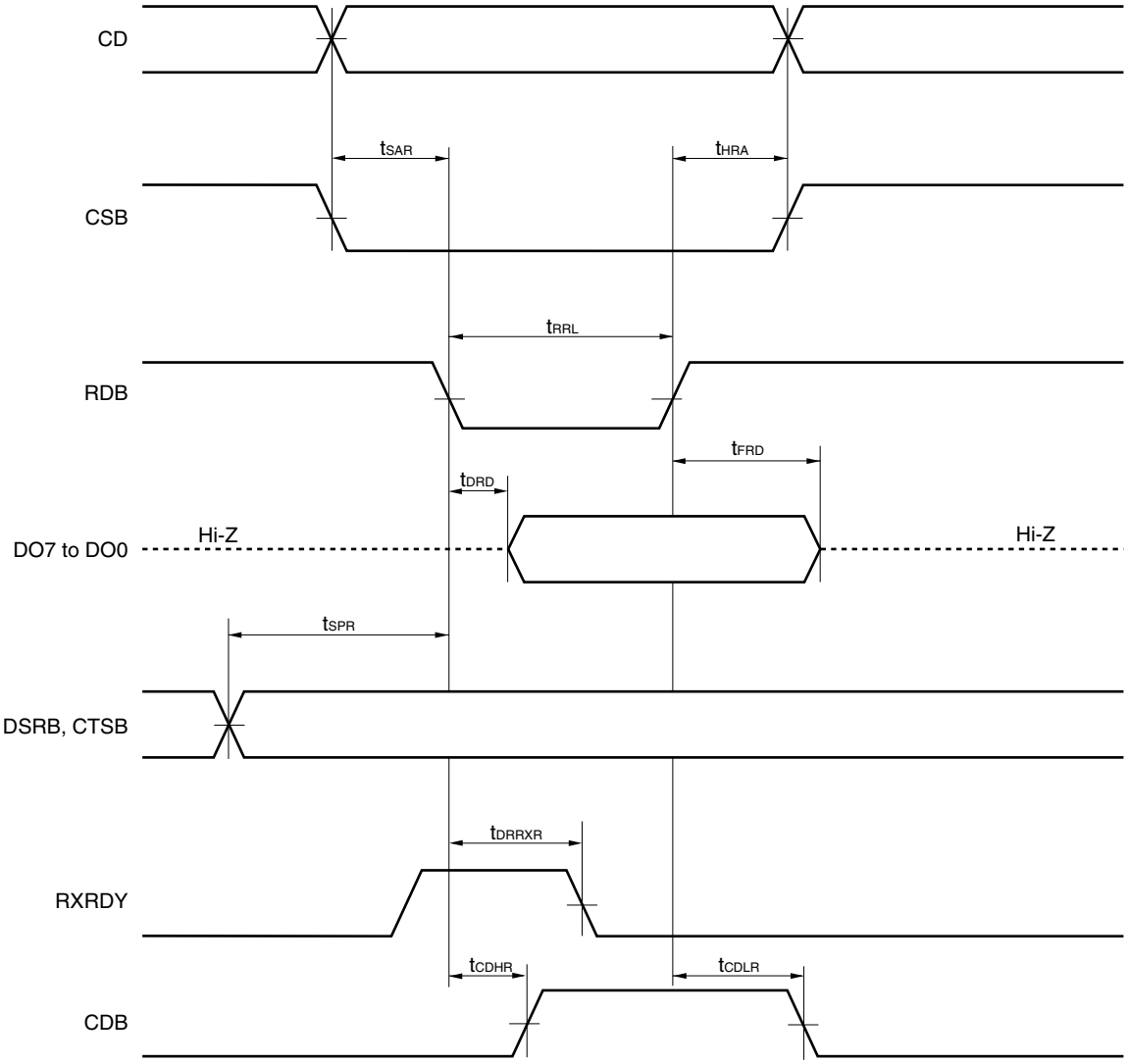
**4.** BR: Baud rate

## 2.5 Timing Charts

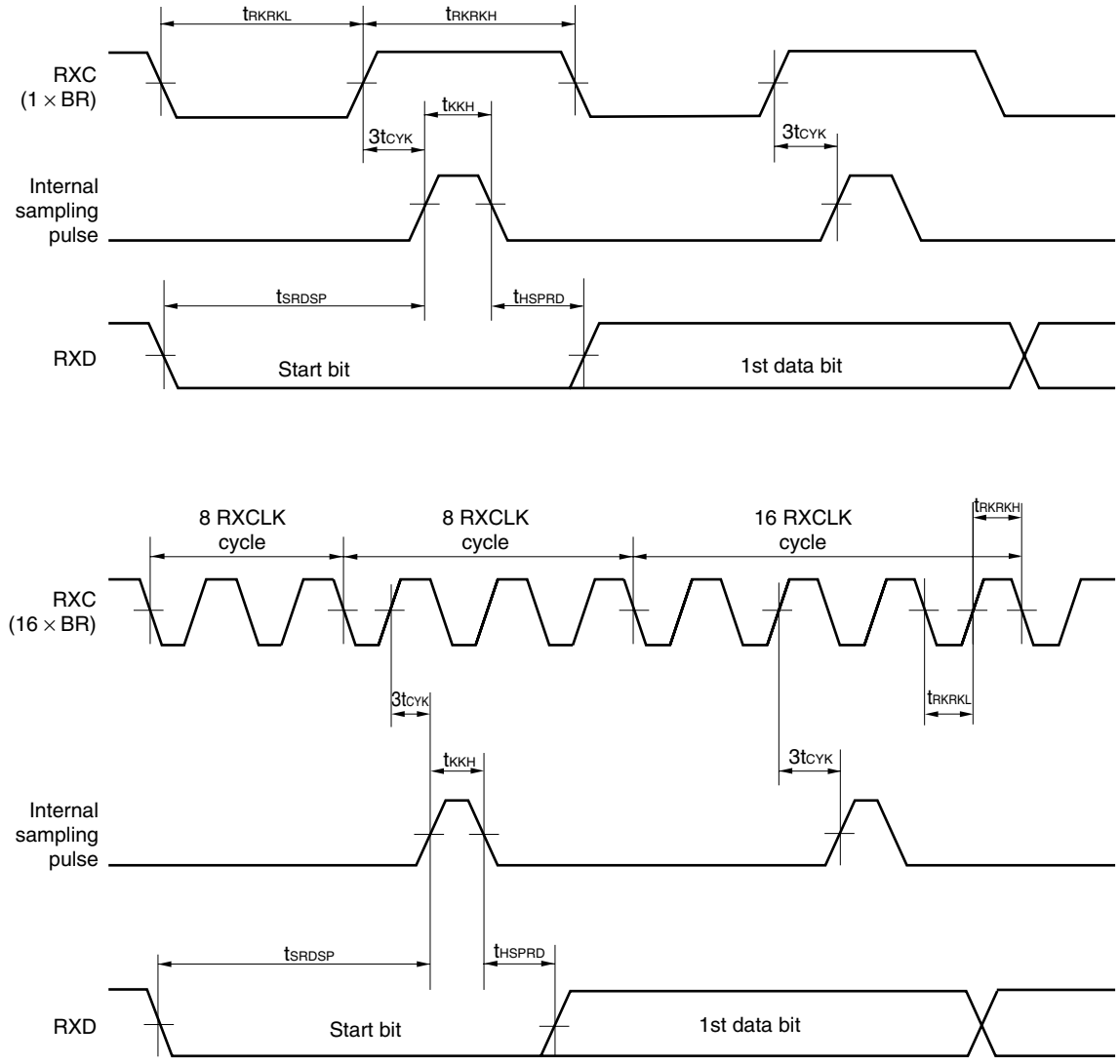
### (1) Write data timing



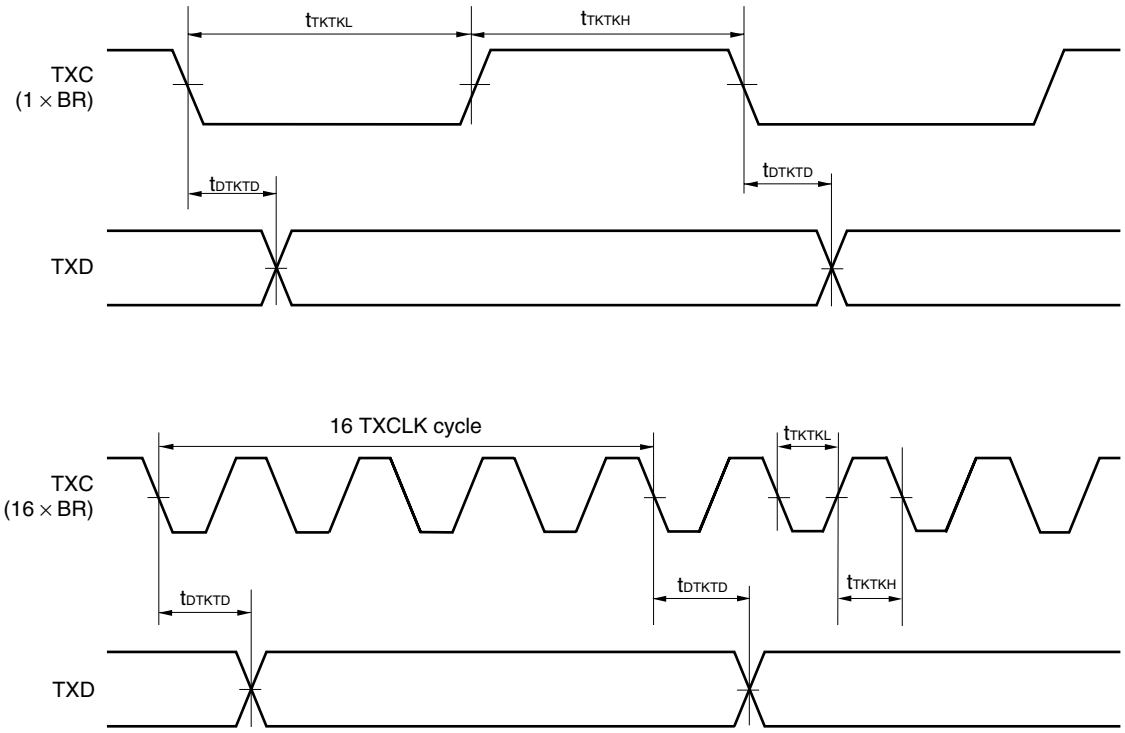
### (2) Read data timing



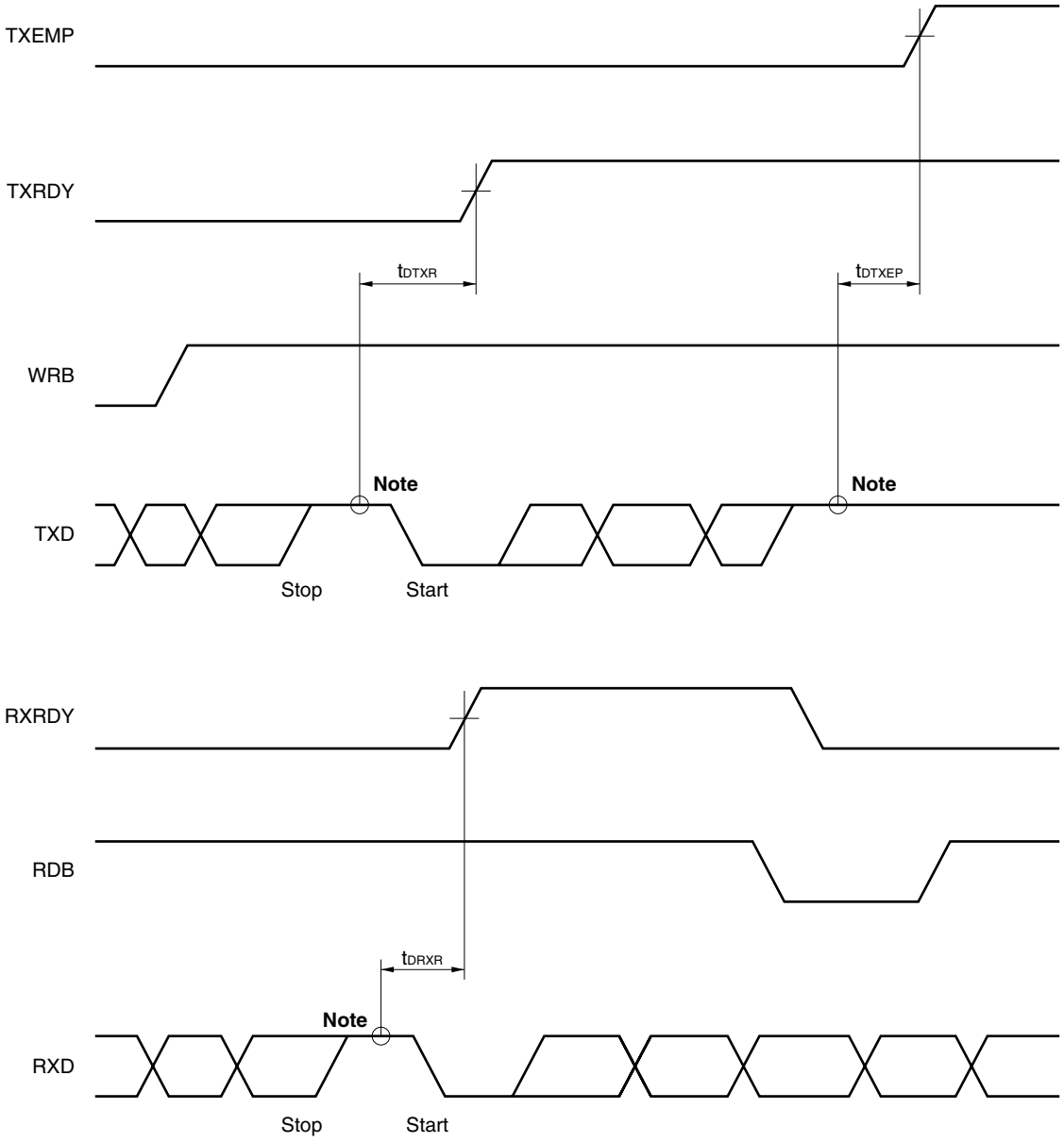
### (3) Receiver clock and RXD



### (4) Transmitter clock and TXD

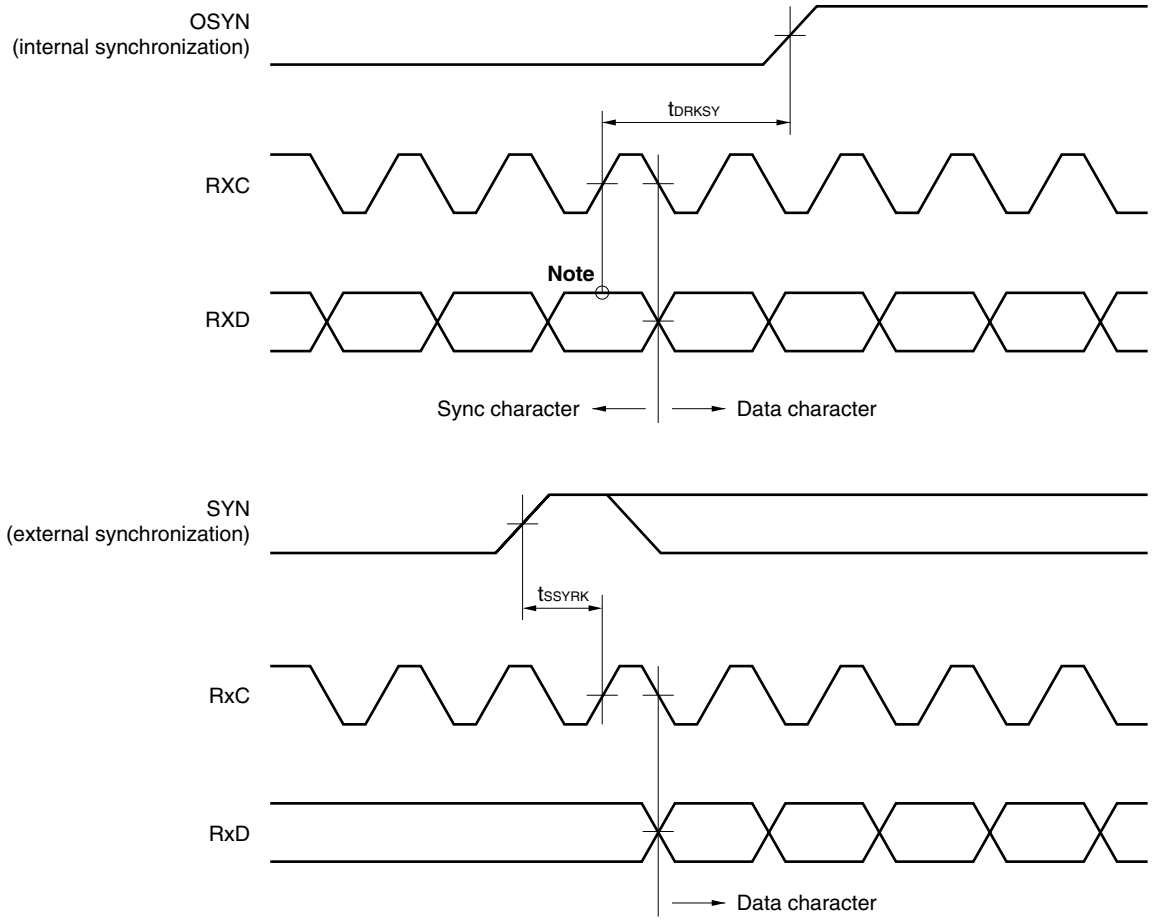


### (5) Timing of flag



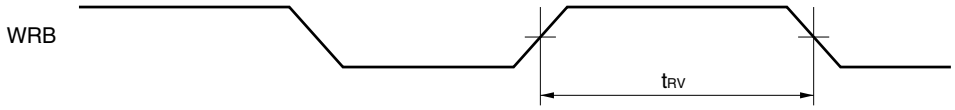

**Note** 1/2 bit.
Rising of the 8th clock if ×16 clock is used for sampling.
Rising of the 32nd clock if ×64 clock is used for sampling.

### (6) Timing of RXD, SYN, and OSYN

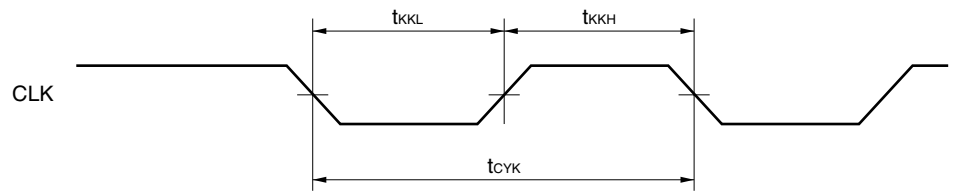



**Note** 1/2 bit.
Rising of the 8th clock if ×16 clock is used for sampling.
Rising of the 32nd clock if ×64 clock is used for sampling.

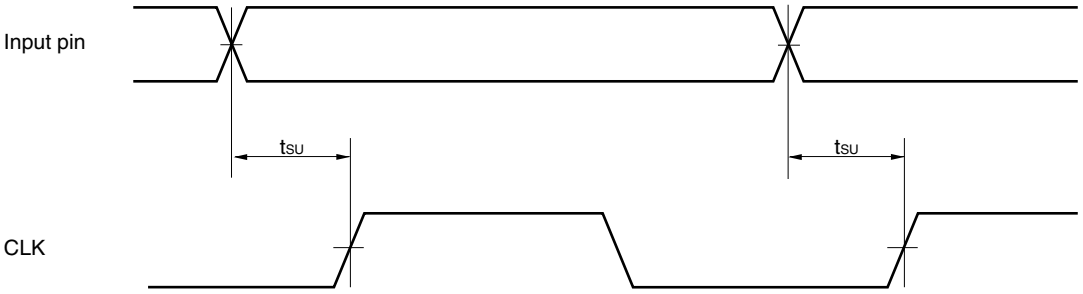
### (7) Write recovery time




### (8) Main clock



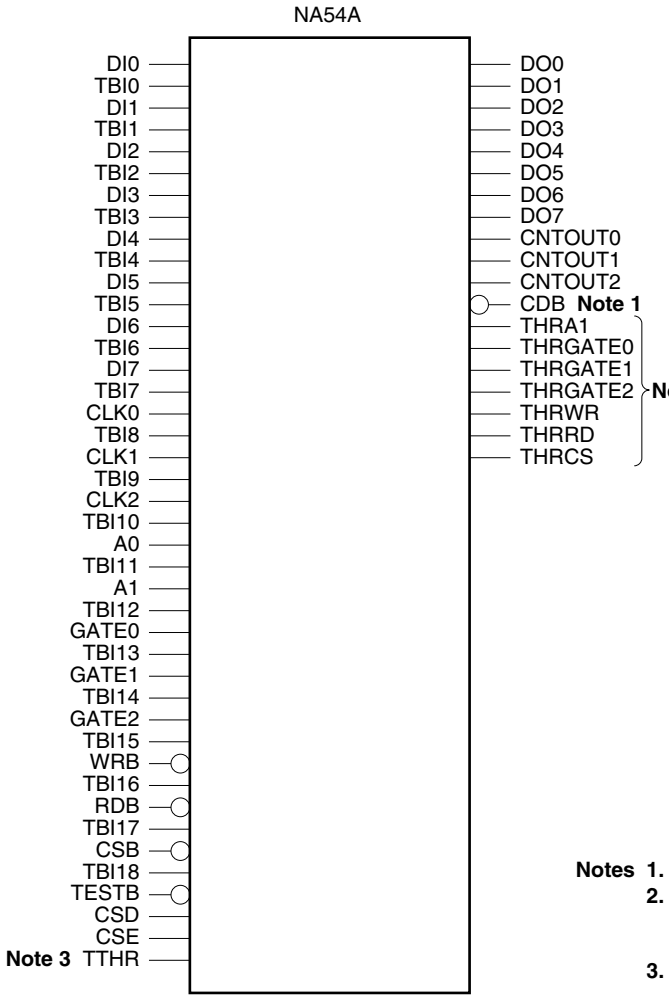
### (9) All input pins (excluding test input pins) and main clock



# CHAPTER 3 NA54A MACRO

This chapter explains the functions of the NA54A.

| Block Type | Function |
|---|---|
| NA54A | Programmable timer/counter |




**Features**

- Compatible functions with μPD71054
- Maximum operating frequency: 33 MHz

**Caution**

- Do not input spike to CLK0, CLK1, CLK2, GATE0, GATE1, GATE2, WRB, and RDB.

**Notes 1.** Output control signal of DO7 to DO0
**2.** Through path output pins of A1, GATE0, GATE1, GATE2, WRB, RDB, and CSB when pre-/post-mega-macro stage is tested
**3.** Through path/normal mode select pin

**Remark** The input signal pins with "TBI" prefixed are test pins.

| | |
|---|---|
| Number of cells used (configuration) | 5076 (141 × 36) |
| Mega macro test pattern length | 3483 |

## 3.1 NA54A Pins

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| DI0 | Input | Data bus input signal (LSB) | | TBI0 | 2.6 | F424 |
| DI1 | Input | Data bus input signal | | TBI1 | 2.7 | F424 |
| DI2 | Input | Data bus input signal | | TBI2 | 2.9 | F424 |
| DI3 | Input | Data bus input signal | | TBI3 | 2.9 | F424 |
| DI4 | Input | Data bus input signal | | TBI4 | 2.9 | F424 |
| DI5 | Input | Data bus input signal | | TBI5 | 2.9 | F424 |
| DI6 | Input | Data bus input signal | | TBI6 | 2.7 | F424 |
| DI7 | Input | Data bus input signal (MSB) | | TBI7 | 2.7 | F424 |
| CLK0 | Input | Clock of counter #0 | | TBI8 | 1.1 | L111 |
| CLK1 | Input | Clock of counter #1 | | TBI9 | 1.6 | L111 |
| CLK2 | Input | Clock of counter #2 | | TBI10 | 1.4 | L111 |
| A0 | Input | Address (LSB) | | TBI11 | 1.4 | L424 |
| A1 | Input | Address (MSB) | | TBI12 | 1.7 | L424 |
| GATE0 | Input | Gate input of counter #0 | | TBI13 | 1.2 | L111 |
| GATE1 | Input | Gate input of counter #1 | | TBI14 | 1.4 | L111 |
| GATE2 | Input | Gate input of counter #2 | | TBI15 | 1.4 | L111 |
| WRB | Input | Write signal | Low | TBI16 | 1.2 | L111 |
| RDB | Input | Read signal | Low | TBI17 | 1.3 | L111 |
| CSB | Input | Chip select signal | Low | TBI18 | 1.3 | L111 |
| CSD | Input | 3-state output control | | – | 1.4 | L101 |
| CSE | Input | 3-state output control | | – | 1.6 | L111 |
| TTHR | Input | Through path/normal mode select signal<br>“H”: Through path mode<br>“L”: Normal mode | | – | 3.0 | F112 |
| TESTB | Input | Test/normal mode select signal<br>“H”: Normal mode<br>“L”: Test mode | | – | 2.7 | F154 |
| DO0 | Output | Data bus output signal (LSB) | | – | 25.0 | F532 |
| DO1 | Output | Data bus output signal | | – | 25.0 | F532 |
| DO2 | Output | Data bus output signal | | – | 25.0 | F532 |
| DO3 | Output | Data bus output signal | | – | 25.0 | F532 |
| DO4 | Output | Data bus output signal | | – | 20.0 | F532 |
| DO5 | Output | Data bus output signal | | – | 25.0 | F532 |
| DO6 | Output | Data bus output signal | | – | 25.0 | F532 |
| DO7 | Output | Data bus output signal (MSB) | | – | 25.0 | F532 |
| CNTOUT0 | Output | Output of counter #0 | | – | 24.0 | F101 |
| CNTOUT1 | Output | Output of counter #1 | | – | 24.0 | F101 |
| CNTOUT2 | Output | Output of counter #2 | | – | 23.0 | F101 |

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| CDB | Output | Enable signal of data bus | | – | 436.0 | F15A |
| THRA1 | Output | Through path output pin | | – | 22.0 | F312 |
| THRGATE0 | Output | Through path output pin | | – | 26.0 | F312 |
| THRGATE1 | Output | Through path output pin | | – | 23.0 | F312 |
| THRGATE2 | Output | Through path output pin | | – | 26.0 | F312 |
| THRWR | Output | Through path output pin | | – | 22.0 | F312 |
| THRRD | Output | Through path output pin | | – | 22.0 | F312 |
| THRCS | Output | Through path output pin | | – | 22.0 | F312 |
| TBI0 | Input | Test input | | – | 2.6 | F424 |
| TBI1 | Input | Test input | | – | 2.8 | F424 |
| TBI2 | Input | Test input | | – | 2.9 | F424 |
| TBI3 | Input | Test input | | – | 2.9 | F424 |
| TBI4 | Input | Test input | | – | 2.8 | F424 |
| TBI5 | Input | Test input | | – | 2.9 | F424 |
| TBI6 | Input | Test input | | – | 2.8 | F424 |
| TBI7 | Input | Test input | | – | 2.6 | F424 |
| TBI8 | Input | Test input | | – | 1.3 | L111 |
| TBI9 | Input | Test input | | – | 1.5 | L111 |
| TBI10 | Input | Test input | | – | 1.3 | L111 |
| TBI11 | Input | Test input | | – | 1.4 | L424 |
| TBI12 | Input | Test input | | – | 1.6 | L424 |
| TBI13 | Input | Test input | | – | 1.3 | L111 |
| TBI14 | Input | Test input | | – | 1.3 | L111 |
| TBI15 | Input | Test input | | – | 1.4 | L111 |
| TBI16 | Input | Test input | | – | 1.1 | L111 |
| TBI17 | Input | Test input | | – | 1.2 | L111 |
| TBI18 | Input | Test input | | – | 1.2 | L111 |

**Remark** Input: Input pin
Output: Output pin

**Remarks 1.** TBIx is a test input pin. A signal can be input from TBIx by making the TESTB input low. Make a connection so that signals can be directly input to the mega macro from outside the gate array in the test mode. "Directly" here means a circuit configuration where the input signal is not inverted and no sequential circuit such as a flip-flop is inserted in between.

| TESTB | Input Pin |
|---|---|
| 1 | Normal pin[Note] |
| 0 | TBIx |

**Note** Input a defined value of 0 or 1 to the test input pins in the normal mode (it does not matter if 0 and 1 are mixed).

**2.** Functions of CSD input and CSE input

CSE input: Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input: Turns off (high-impedance: Hi-Z) of all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

| CSE | CSD | Status of Output Pin | Status of 3-State Output Pin[Note] |
|---|---|---|---|
| 0 | 0 | Normal operation | Hi-Z |
| 0 | 1 | Normal operation | Normal operation |
| 1 | – | Normal operation | Hi-Z is not output. |

**Note** 3-state pins are DO7 to DO0.

**3.** When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

| "Hi-Z" Pin | Corresponding Output Control Signal and Output | |
|---|---|---|
| DO7 to DO0 | CDB | 0 |

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

**4.** CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

**Remarks 5.** Operating status of output pin depending on combination of TTHR, CSE, and CSD

| TTHR Pin | CSE Pin | CSD Pin | 3-State Output Pin (DOx) | 3-State Control Pin (CDB(SD)) | Other Pins | Through Path Pin (Output THRxxx) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Hi-Z | 0 | Normal operation | 0 |
| | | 1 | Normal operation | Normal operation | | |
| | 1 | 0 | Hi-Z is not output. | 0 | | |
| | | 1 | | Normal operation | | |
| 1 | 0 | 0 | Hi-Z | Through path | Through path | Through path |
| | | 1 | Through path | | | |
| | 1 | × | | | | |

**6.** I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

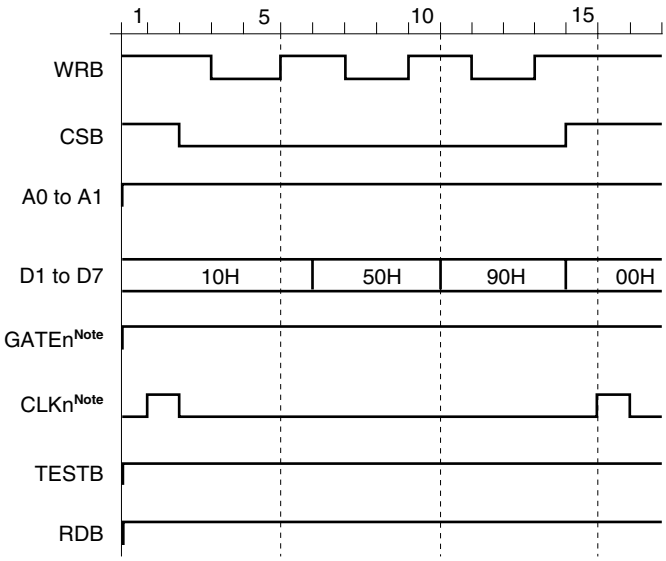
| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| DO0 | DI0 | TBI0 |
| DO1 | DI1 | TBI1 |
| DO2 | DI2 | TBI2 |
| DO3 | DI3 | TBI3 |
| DO4 | DI4 | TBI4 |
| DO5 | DI5 | TBI5 |
| DO6 | DI6 | TBI6 |
| DO7 | DI7 | TBI7 |
| CNTOUT0 | CLK0 | TBI8 |
| CNTOUT1 | CLK1 | TBI9 |

| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| CNTOUT2 | CLK2 | TBI10 |
| CDB | A0 | TBI11 |
| THRA1 | A1 | TBI12 |
| THRGATE0 | GATE0 | TBI13 |
| THRGATE1 | GATE1 | TBI14 |
| THRGATE2 | GATE2 | TBI15 |
| THRWR | WRB | TBI16 |
| THRRD | RDB | TBI17 |
| THRCS | CSB | TBI18 |

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high impedance).

## 3.2 NA54A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.




Example of initialization pattern

Mode setting is initialized.

[Example of setting counters #0 through #2 in mode 0]

**Note** n: 0, 1, or 2

Input “0” or “1” to the other input pins (normal input and test input).
Exercise care that “X” is not input.

- **Value of mega macro output pin after initialization pattern**

| Mode | DO7 to DO0 | CNTOUT2 to CNTOUT0 | CDB | THRA1, THRGATE2 to THRGATE0, THRWR |
|---|---|---|---|---|
| 0 | Hi-Z | 0 | 0 | 0 |
| 1 | Hi-Z | 1 | 0 | 0 |
| 2 | Hi-Z | 1 | 0 | 0 |
| 3 | Hi-Z | 1 | 0 | 0 |
| 4 | Hi-Z | 1 | 0 | 0 |
| 5 | Hi-Z | 1 | 0 | 0 |

**Caution Configure the circuit of the following input pins so that spike is not input:**
**CLK0, CLK1, CLK2, GATE0, GATE1, GATE2, WRB, RDB**
**The values of CNTOUT2 to CNTOUT0 are output when the register of the corresponding counter is set. If the register is not set, the value is × (undefined).**

## 3.3 Delay Time

Refer to **1.2.4 Delay time**.

## 3.4 AC Characteristics ($T_A$ = –40 to 85°C, $V_{DD}$ = 3.3 ±0.3 V)

### (1) Read cycle

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Address setup time (to RDB ↓) | $t_{SAR}$ | 3 | | ns |
| Address hold time (from RDB ↑) | $t_{HRA}$ | 0 | | ns |
| CSB setup time (to RDB ↓) | $t_{SCR}$ | 1 | | ns |
| Low-level RDB pulse width | $t_{RRL}$ | 30 | | ns |
| Data delay time (to RDB ↓) | $t_{DRD}$ | 4 | 24 | ns |
| Data float delay time (to RDB ↑) | $t_{FRD}$ | 9 | 20 | ns |
| Data delay time (to address) | $t_{DAD}$ | 5 | 25 | ns |
| Read recovery time | $t_{RV}$ | 30 | | ns |
| CDB high delay time (to RDB ↓) | $t_{CDHR}$ | 9 | 19 | ns |
| CDB low delay time (to RDB ↑) | $t_{CDLR}$ | 9 | 20 | ns |

### (2) Write cycle

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Address setup time (to WRB ↓) | $t_{SAW}$ | 0 | | ns |
| Address hold time (from WRB ↑) | $t_{HWA}$ | 10 | | ns |
| CSB setup time (to WRB ↓) | $t_{SCW}$ | 0 | | ns |
| Low-level WRB pulse width | $t_{WWL}$ | 30 | | ns |
| Data setup time (to WRB ↑) | $t_{SDW}$ | 4 | | ns |
| Data hold time (from WRB ↑) | $t_{HWD}$ | 0 | | ns |
| Write recovery time | $t_{RV}$ | 30 | | ns |

### (3) Clock, gate timing

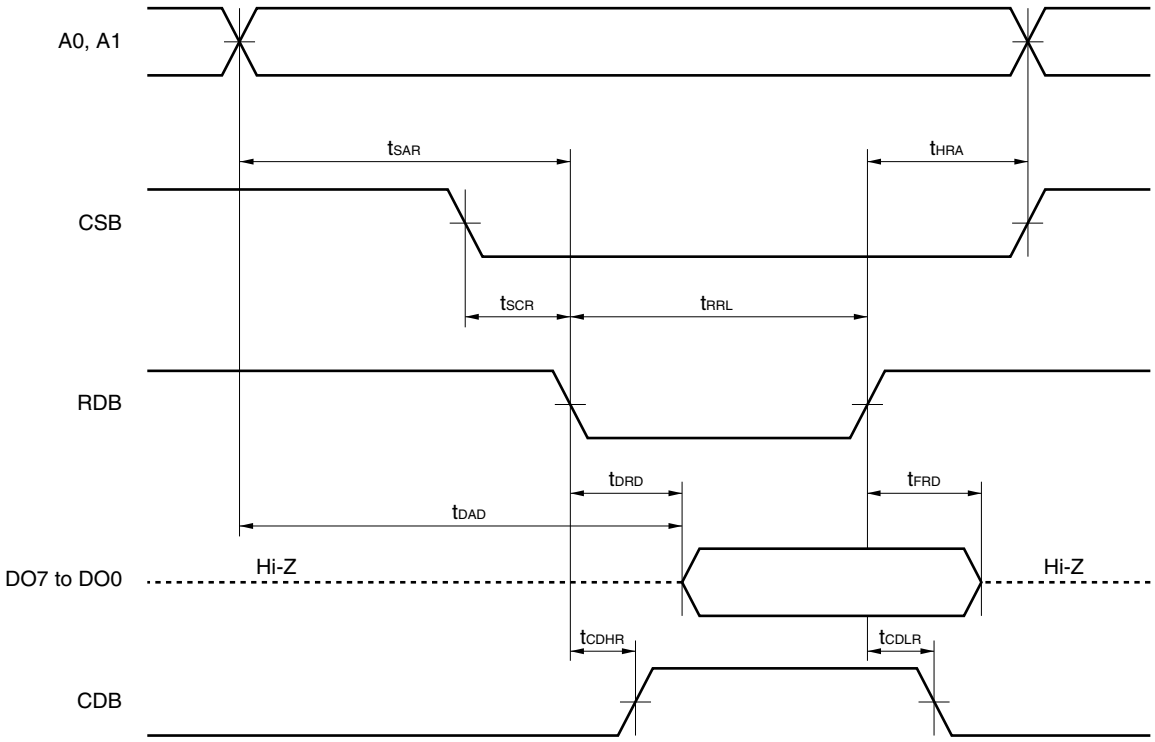
| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Clock cycle | $t_{CYK}$ | 30 | | ns |
| High-level clock pulse width | $t_{KKH}$ | 13.5 | | ns |
| Low-level clock pulse width | $t_{KKL}$ | 13.5 | | ns |
| High-level gate pulse width | $t_{GGH}$ | 15 | | ns |
| Low-level gate pulse width | $t_{GGL}$ | 15 | | ns |
| Gate setup time (to CLKn ↑)Note | $t_{SGK}$ | 7 | | ns |
| Gate hold time (from CLKn ↑)Note | $t_{HKG}$ | 1 | | ns |
| Clock delay time (to WRB ↑) (number of counts) | $t_{DWK}$ | 0 | | ns |
| Clock delay time (to WRB ↑) (latch command) | $t_{SKW}$ | 0 | | ns |
| Gate delay time (to WRB ↑) | $t_{DWG}$ | 0 | | ns |
| Output delay time (to GATEn ↓)Note | $t_{DGO}$ | | 4 | ns |
| Output delay time (to CLKn ↓)Note | $t_{DKO}$ | | 13 | ns |
| Output (initial OUT) delay time (to WRB ↑) | $t_{DWO}$ | | 6 | ns |

**Note** n = 0, 1, or 2

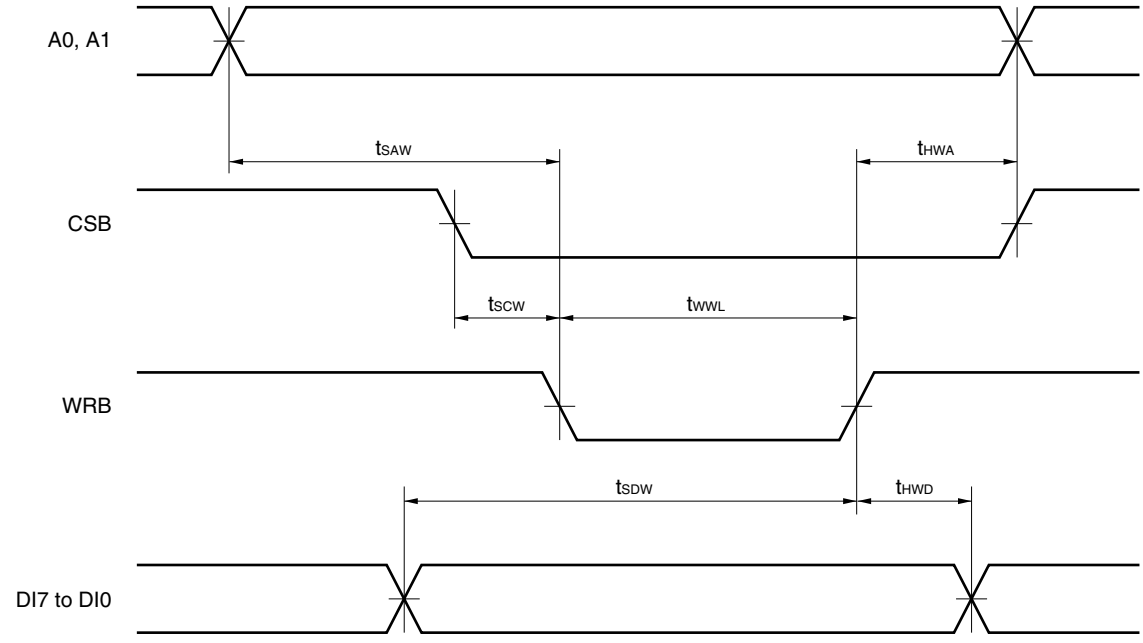
**Remark** The output load conditions of the propagation delay time are fanout: 1, wiring length: 0 mm.

## 3.5 Timing Charts

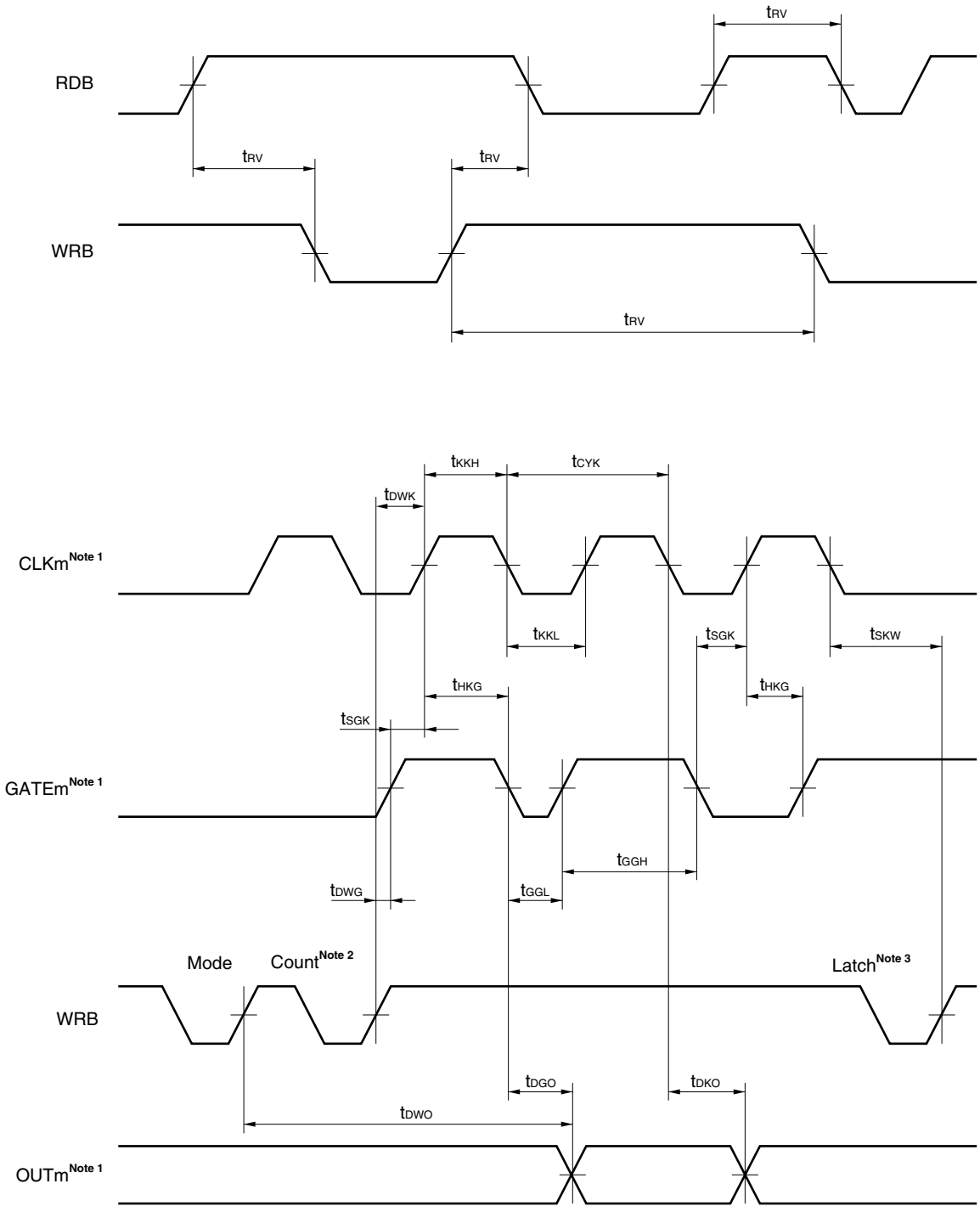
### (1) Read cycle timing




### (2) Write cycle timing



### (3) Read/write recovery time




**Notes 1.** m = 0, 1, or 2

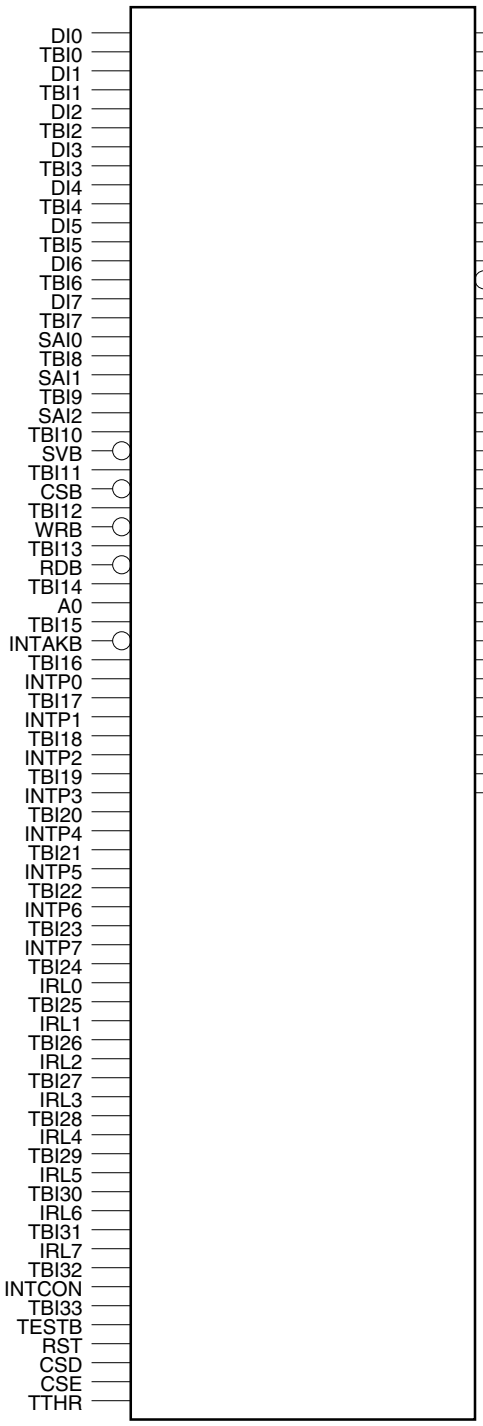
**2.** Writing of last byte of number of counts

**3.** Writing of count latch command or multiple latch command

# CHAPTER 4 NA59A MACRO

This chapter explains the functions of the NA59A.

| Block Type | Function |
|---|---|
| NA59A | Interrupt control unit |




**Features**

- Compatible functions with μPD71059 (some functions differ from the functions of μPD71059. For details, refer to **4.6 Differences Between NA59A and μPD71059**.)
- Maximum operating frequency: 33 MHz or equivalent

**Caution**

- Do not input spike to WRB, RDB, INTAKB, INTP7 to INTP0, and RST.

**Notes 1.** Output control signal of DO7 to DO0
**2.** Output control signal of SAO2 to SAO0
**3.** Output control signal of SVO
**4.** Through path output pins of CSB, WRB, RDB, A0, and INTP7 to INTP3 when pre-/post-mega-macro stage is tested

**Remark** The input signal pins with "TBI" prefixed are test pins.

| | |
|---|---|
| Number of cells used (configuration) | 2548 (91 × 28) |
| Mega macro test pattern length | 7335 |

## 4.1 NA59A Pins

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| DI0 | Input | Data bus input signal (LSB) | | TBI0 | 2.5 | F424 |
| DI1 | Input | Data bus input signal | | TBI1 | 2.4 | F424 |
| DI2 | Input | Data bus input signal | | TBI2 | 2.5 | F424 |
| DI3 | Input | Data bus input signal | | TBI3 | 2.5 | F424 |
| DI4 | Input | Data bus input signal | | TBI4 | 2.5 | F424 |
| DI5 | Input | Data bus input signal | | TBI5 | 2.8 | F424 |
| DI6 | Input | Data bus input signal | | TBI6 | 2.8 | F424 |
| DI7 | Input | Data bus input signal (MSB) | | TBI7 | 2.8 | F424 |
| SAI0 | Input | Slave address (LSB) | | TBI8 | 2.0 | L424 |
| SAI1 | Input | Slave address | | TBI9 | 1.5 | L424 |
| SAI2 | Input | Slave address (MSB) | | TBI10 | 1.5 | L424 |
| SVB | Input | Slave input signal | Low | TBI11 | 1.4 | L424 |
| CSB | Input | Chip select signal | Low | TBI12 | 2.2 | L101 |
| WRB | Input | Write signal | Low | TBI13 | 4.0 | F101 |
| RDB | Input | Read signal | Low | TBI14 | 3.3 | F101 |
| A0 | Input | Specifies command/data when RD or WR | | TBI15 | 2.6 | L424 |
| INTAKB | Input | Interrupt acknowledge signal | Low | TBI16 | 3.9 | F101 |
| INTP0 | Input | Interrupt request input signal (bit 0) | | TBI17 | 1.5 | L111 |
| INTP1 | Input | Interrupt request input signal (bit 1) | | TBI18 | 1.2 | L111 |
| INTP2 | Input | Interrupt request input signal (bit 2) | | TBI19 | 1.2 | L111 |
| INTP3 | Input | Interrupt request input signal (bit 3) | | TBI20 | 1.2 | L111 |
| INTP4 | Input | Interrupt request input signal (bit 4) | | TBI21 | 1.3 | L111 |
| INTP5 | Input | Interrupt request input signal (bit 5) | | TBI22 | 1.5 | L111 |
| INTP6 | Input | Interrupt request input signal (bit 6) | | TBI23 | 1.2 | L111 |
| INTP7 | Input | Interrupt request input signal (bit 7) | | TBI24 | 1.2 | L111 |
| IRL0 | Input | Level edge select signal (bit 0) H = trig | | TBI25 | 1.3 | L424 |
| IRL1 | Input | Level edge select signal (bit 1) H = trig | | TBI26 | 1.3 | L424 |
| IRL2 | Input | Level edge select signal (bit 2) H = trig | | TBI27 | 1.4 | L424 |
| IRL3 | Input | Level edge select signal (bit 3) H = trig | | TBI28 | 1.3 | L424 |
| IRL4 | Input | Level edge select signal (bit 4) H = trig | | TBI29 | 1.1 | L424 |
| IRL5 | Input | Level edge select signal (bit 5) H = trig | | TBI30 | 1.1 | L424 |
| IRL6 | Input | Level edge select signal (bit 6) H = trig | | TBI31 | 1.4 | L424 |
| IRL7 | Input | Level edge select signal (bit 7) H = trig | | TBI32 | 1.2 | L424 |
| INTCON | Input | INT output select | | TBI33 | 1.4 | L424 |
| TESTB | Input | Test/normal mode select signal<br>“H”: Normal mode<br>“L”: Test mode | | – | 1.3 | L101 |
| CSD | Input | 3-state output control | | – | 3.2 | F112 |
| RST | Input | Fix the value of OSV, CSA, CSV | High | – | 1.9 | L111 |

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| CSE | Input | 3-state output control | | – | 5.0 | L111 |
| TTHR | Input | Through path/normal mode select signal<br>“H”: Through path mode<br>“L”: Normal mode | | – | 3.4 | F111 |
| DO0 | Output | Data bus output signal (LSB) | | – | 26.0 | F531 |
| DO1 | Output | Data bus output signal | | – | 26.0 | F531 |
| DO2 | Output | Data bus output signal | | – | 25.0 | F531 |
| DO3 | Output | Data bus output signal | | – | 25.0 | F531 |
| DO4 | Output | Data bus output signal | | – | 25.0 | F531 |
| DO5 | Output | Data bus output signal | | – | 25.0 | F531 |
| DO6 | Output | Data bus output signal | | – | 25.0 | F531 |
| DO7 | Output | Data bus output signal (MSB) | | – | 25.0 | F531 |
| SAO0 | Output | Slave address output signal (LSB) | | – | 25.0 | F531 |
| SAO1 | Output | Slave address output signal | | – | 25.0 | F531 |
| SAO2 | Output | Slave address output signal (MSB) | | – | 26.0 | F531 |
| SVO | Output | Slave output enable | | – | 26.0 | F531 |
| INTR | Output | Interrupt request signal | | – | 24.0 | F101 |
| CDB | Output | Output control signal of DO0 to DO7 | | – | 435.0 | F15A |
| CSA | Output | Output control signal of SAO0 to SAO2 | | – | 26.0 | F111 |
| CSV | Output | Output control signal of SVO | | – | 26.0 | F111 |
| ESLC0 | Output | Interrupt reset output 0 (H = RESET) | | – | 23.0 | F101 |
| ESLC1 | Output | Interrupt reset output 1 (H = RESET) | | – | 24.0 | F101 |
| ESLC2 | Output | Interrupt reset output 2 (H = RESET) | | – | 23.0 | F101 |
| ESLC3 | Output | Interrupt reset output 3 (H = RESET) | | – | 25.0 | F101 |
| ESLC4 | Output | Interrupt reset output 4 (H = RESET) | | – | 24.0 | F101 |
| ESLC5 | Output | Interrupt reset output 5 (H = RESET) | | – | 25.0 | F101 |
| ESLC6 | Output | Interrupt reset output 6 (H = RESET) | | – | 24.0 | F101 |
| ESLC7 | Output | Interrupt reset output 7 (H = RESET) | | – | 23.0 | F101 |
| INTO0 | Output | Interrupt output 0 (H = interrupt) | | – | 24.0 | F101 |
| INTO1 | Output | Interrupt output 1 (H = interrupt) | | – | 24.0 | F101 |
| INTO2 | Output | Interrupt output 2 (H = interrupt) | | – | 26.0 | F101 |
| INTO3 | Output | Interrupt output 3 (H = interrupt) | | – | 26.0 | F101 |
| INTO4 | Output | Interrupt output 4 (H = interrupt) | | – | 25.0 | F101 |
| INTO5 | Output | Interrupt output 5 (H = interrupt) | | – | 25.0 | F101 |
| INTO6 | Output | Interrupt output 6 (H = interrupt) | | – | 25.0 | F101 |
| INTO7 | Output | Interrupt output 7 (H = interrupt) | | – | 25.0 | F101 |
| THRCSB | Output | Through path output pin | | – | 26.0 | F312 |
| THRWRB | Output | Through path output pin | | – | 26.0 | F312 |
| THRRDB | Output | Through path output pin | | – | 26.0 | F312 |
| THRA0 | Output | Through path output pin | | – | 26.0 | F312 |
| THRINTP3 | Output | Through path output pin | | – | 26.0 | F312 |

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| THRINTP4 | Output | Through path output pin | | – | 26.0 | F312 |
| THRINTP5 | Output | Through path output pin | | – | 26.0 | F312 |
| THRINTP6 | Output | Through path output pin | | – | 26.0 | F312 |
| THRINTP7 | Output | Through path output pin | | – | 26.0 | F312 |
| TBI0 | Input | Test input | | | 2.6 | F424 |
| TBI1 | Input | Test input | | | 2.6 | F424 |
| TBI2 | Input | Test input | | | 2.6 | F424 |
| TBI3 | Input | Test input | | | 2.7 | F424 |
| TBI4 | Input | Test input | | | 2.7 | F424 |
| TBI5 | Input | Test input | | | 2.8 | F424 |
| TBI6 | Input | Test input | | | 2.9 | F424 |
| TBI7 | Input | Test input | | | 2.9 | F424 |
| TBI8 | Input | Test input | | | 2.5 | L424 |
| TBI9 | Input | Test input | | | 1.4 | L424 |
| TBI10 | Input | Test input | | | 1.4 | L424 |
| TBI11 | Input | Test input | | | 1.2 | L424 |
| TBI12 | Input | Test input | | | 1.5 | L101 |
| TBI13 | Input | Test input | | | 4.1 | F101 |
| TBI14 | Input | Test input | | | 3.4 | F101 |
| TBI15 | Input | Test input | | | 2.6 | L424 |
| TBI16 | Input | Test input | | | 3.9 | F101 |
| TBI17 | Input | Test input | | | 1.6 | L111 |
| TBI18 | Input | Test input | | | 1.2 | L111 |
| TBI19 | Input | Test input | | | 1.3 | L111 |
| TBI20 | Input | Test input | | | 1.2 | L111 |
| TBI21 | Input | Test input | | | 1.2 | L111 |
| TBI22 | Input | Test input | | | 1.6 | L111 |
| TBI23 | Input | Test input | | | 1.2 | L111 |
| TBI24 | Input | Test input | | | 1.2 | L111 |
| TBI25 | Input | Test input | | | 1.6 | L424 |
| TBI26 | Input | Test input | | | 1.7 | L424 |
| TBI27 | Input | Test input | | | 1.5 | L424 |
| TBI28 | Input | Test input | | | 1.4 | L424 |
| TBI29 | Input | Test input | | | 1.2 | L424 |
| TBI30 | Input | Test input | | | 1.2 | L424 |
| TBI31 | Input | Test input | | | 1.3 | L424 |
| TBI32 | Input | Test input | | | 1.1 | L424 |
| TBI33 | Input | Test input | | | 1.4 | L424 |

**Remark** Input: Input pin
Output: Output pin

**Remarks 1.** TBIx is a test input pin. A signal can be input from TBIx by making the TESTB input low. Make a connection so that signals can be directly input to the mega macro from outside the gate array in the test mode. "Directly" here means a circuit configuration where the input signal is not inverted and no sequential circuit such as a flip-flop is inserted in between.

| TESTB | Input Pin |
|---|---|
| 1 | Normal pin[Note] |
| 0 | TBIx |

**Note** Input a defined value of 0 or 1 to the test input pins in the normal mode (it does not matter if 0 and 1 are mixed).

**2.** Functions of CSD input and CSE input

CSE input : Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input : Turns off (high-impedance: Hi-Z) all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

| CSE | CSD | Status of Output Pin | Status of 3-State Output Pin[Note] |
|---|---|---|---|
| 0 | 0 | Normal operation | Hi-Z |
| 0 | 1 | Normal operation | Normal operation |
| 1 | – | Normal operation | Hi-Z is not output. |

**Note** 3-state pins are DO7 to DO0, SAO2 to SAO0, and SVO.

**3.** When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

| "Hi-Z" Pin | Corresponding Output Control Signal and Output | |
|---|---|---|
| DO7 to DO0 | CDB | 0 |
| SAO2 to SAO0 | CSA | 0 |
| SVO | CSV | 0 |

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

**4.** CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

**Remarks 5.** Operating status of output pin depending on combination of TTHR, CSE, and CSD

| TTHR Pin | CSE Pin | CSD Pin | 3-State Output Pin (DOx) | 3-State Control Pin (CDB(SD)) | Other Pins | Through Path Pin (Output THRxxx) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Hi-Z | 0 | Normal operation | 0 |
| | | 1 | Normal operation | Normal operation | | |
| | 1 | 0 | Hi-Z is not output. | 0 | | |
| | | 1 | | Normal operation | | |
| 1 | 0 | 0 | Hi-Z | Through path | Through path | Through path |
| | | 1 | Through path | | | |
| | 1 | × | | | | |

**6.** I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

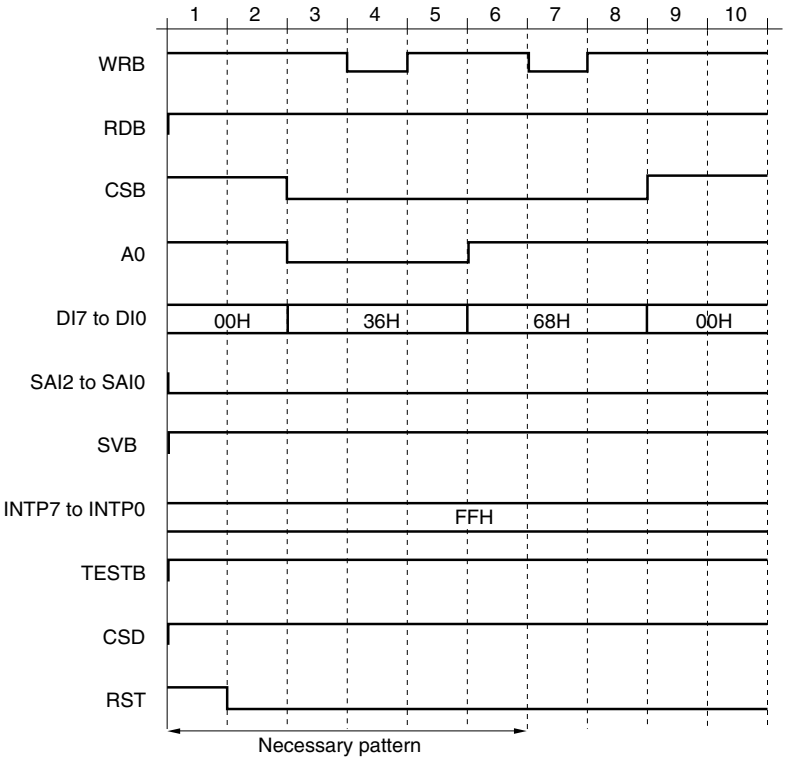
| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| DO0 | DI0 | TBI0 |
| DO1 | DI1 | TBI1 |
| DO2 | DI2 | TBI2 |
| DO3 | DI3 | TBI3 |
| DO4 | DI4 | TBI4 |
| DO5 | DI5 | TBI5 |
| DO6 | DI6 | TBI6 |
| DO7 | DI7 | TBI7 |
| SAO0 | SAI0 | TBI8 |
| SAO1 | SAI1 | TBI9 |
| SAO2 | SAI2 | TBI10 |
| SVO | SVB | TBI11 |
| INTR | INTAKB | TBI16 |

| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| CDB | INTP0 | TBI17 |
| CSA | INTP1 | TBI18 |
| CSV | INTP2 | TBI19 |
| THRCSB | CSB | TBI12 |
| THRWRB | WRB | TBI13 |
| THRRDB | RDB | TBI14 |
| THRA0 | A0 | TBI15 |
| THRINTP3 | INTP3 | TBI20 |
| THRINTP4 | INTP4 | TBI21 |
| THRINTP5 | INTP5 | TBI22 |
| THRINTP6 | INTP6 | TBI23 |
| THRINTP7 | INTP7 | TBI24 |

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high impedance).

## 4.2 NA59A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.




Example of initialization pattern

Be sure to input this pattern up to the second pattern for initialization. This initialization pattern sets the NA59A in the CALL mode, edge trigger mode, and single mode with address gap of 4 bytes.
To use the vector mode or extended mode, set the third pattern and those that follow in the mode to be used.
For details of how to set the mode, refer to **Figures 4-2 Initialization Sequence** and **4-3 Initialization Word Format** in **4.1 Initialization Word** in the **$\mu$PD71059 Data Sheet (U11932J)** (Japanese version only).

Input “0” or “1” to the other input pins (normal input and test input).

Status of output pin after mode setting

| Pin Name | Status |
|---|---|
| DO7 to DO0 | Hi-Z |
| CDB | 0 |
| SAO2 to SAO0 | 0 (single mode and master mode)<br>Hi-Z (slave mode) |
| CSA | 1 (single mode and master mode)<br>0 (slave mode) |
| SVO | 1 (buffer mode master)<br>Hi-Z (buffer mode slave and non-buffer mode) |
| CSV | 1 (buffer mode master)<br>0 (buffer mode slave and non-buffer mode) |
| INTR | 0 |

**Cautions 1. RST pin**

**The RST pin is peculiar to the NA59A. This pin makes the status of the NA59A same as that of the standard model immediately after power application (when SVB = 1).**

**Be sure to input a signal of “1” to this pin for 10 ns or more immediately after power application, and input “0” to it after initialization.**

**By inputting “1” to this pin, the output signals are determined as follows:**

**SVO ... Hi-Z**

**CSA ... 1**

**CSV ... 0**

**The other internal registers are not initialized.**

**2. Configure the circuit of the following input pins so that spike is not input:**

**WRB, RDB, INTAKB, INTP7 to INTP0, RST**

## 4.3 Delay Time

Refer to **1.2.4 Delay time**.

## 4.4 AC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 3.3 ±0.3V)

### (1) Read timing

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Address setup time (to RDB ↓) | $t_{SAR}$ | 1 | | ns |
| Address hold time (from RDB ↑) | $t_{HRA}$ | 1 | | ns |
| Low-level RDB pulse width | $t_{RRL}$ | 30 | | ns |
| High-level RDB pulse width | $t_{RRH}$ | 30 | | ns |
| Data delay time (from CSB) | $t_{DAD}$ | | 7 | ns |
| Data delay time (from A0) | $t_{DAD}$ | | 11 | ns |
| Data delay time (from RDB ↓) | $t_{DRD}$ | | 4 | ns |
| CDB high delay time (from RDB ↓) | $t_{CDHR}$ | | 15 | ns |
| Data float time (from RDB ↑) | $t_{FRD}$ | 7 | 16 | ns |
| CDB low delay time (from RDB ↑) | $t_{CDLR}$ | | 15 | ns |
| BUFR/W delay time (from RDB ↓) | $t_{DRBL}$ | | 3 | ns |
| BUFR/W delay time (from RDB ↑) | $t_{DRBH}$ | | 4 | ns |

### (2) Write timing

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Address setup time (to WRB ↓)[Note] | $t_{SAW}$ | 4 | | ns |
| Address hold time (from WRB ↑)[Note] | $t_{HWA}$ | 1 | | ns |
| Low-level WRB pulse width | $t_{WWL}$ | 30 | | ns |
| High-level WRB pulse width | $t_{WWH}$ | 30 | | ns |
| Data setup time (to WRB ↑) | $t_{SDW}$ | 4 | | ns |
| Data hold time (from WRB ↑) | $t_{HWD}$ | 0 | | ns |

**Note** “Address” means A0 and CSB.

### (3) Interrupt timing

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| INTP pulse width[Note 1] | $t_{IPIPL}$ | 20 | | ns |
| SA setup time (2nd, 3rd INTAKB ↓) (slave) | $t_{SSIA}$ | 20 | | ns |
| Low-level INTAKB pulse width | $t_{IAIAL}$ | 30 | | ns |
| High-level INTAKB pulse width | $t_{IAIAH}$ | 30 | | ns |
| INT delay time (from INTP ↑) | $t_{DIPI}$ | | 5 | ns |
| SA delay time (from 1st INTAKB ↓) (master) | $t_{DIAS}$ | | 4 | ns |
| Data delay time (from INTAKB ↓) | $t_{DIAD}$ | | 4 | ns |
| CDB high delay time (from INTAKB ↓) | $t_{CDHIA}$ | | 15 | ns |
| Data float time (from INTAKB ↑) | $t_{FIAD}$ | 8 | 17 | ns |
| CDB low delay time (from INTAKB ↑) | $t_{CDLIA}$ | | 15 | ns |
| Data delay time (from SA) (slave) | $t_{DSD}$ | | 11 | ns |
| BUFR/W delay time (from INTAKB ↓) | $t_{DIABL}$ | | 3 | ns |
| BUFR/W delay time (from INTAKB ↑) | $t_{DIABH}$ | | 3 | ns |

### (4) Other timing

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Read/write recovery time[Note 2] | $t_{RV1}$ | 30 | | ns |
| INTAKB recovery time[Note 3] | $t_{RV2}$ | 30 | | ns |
| INTAKB/command recovery time[Note 4] | $t_{RV3}$ | 30 | | ns |

**Notes 1.** Time necessary for clearing the input latch in the edge trigger mode

**2.** Time necessary for operation to change from read to write or from write to read

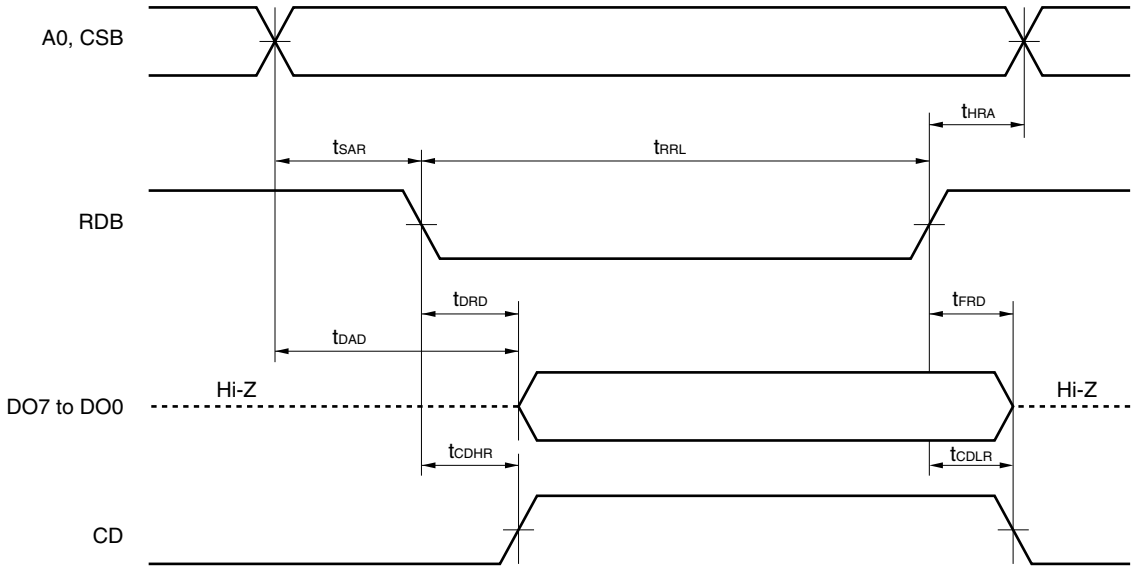
**3.** Time necessary to start the next INTAKB sequence from the last low pulse of an INTAKB sequence

**4.** Time necessary for operation to change from INTAKB to command (read/write) or from command to INTAKB

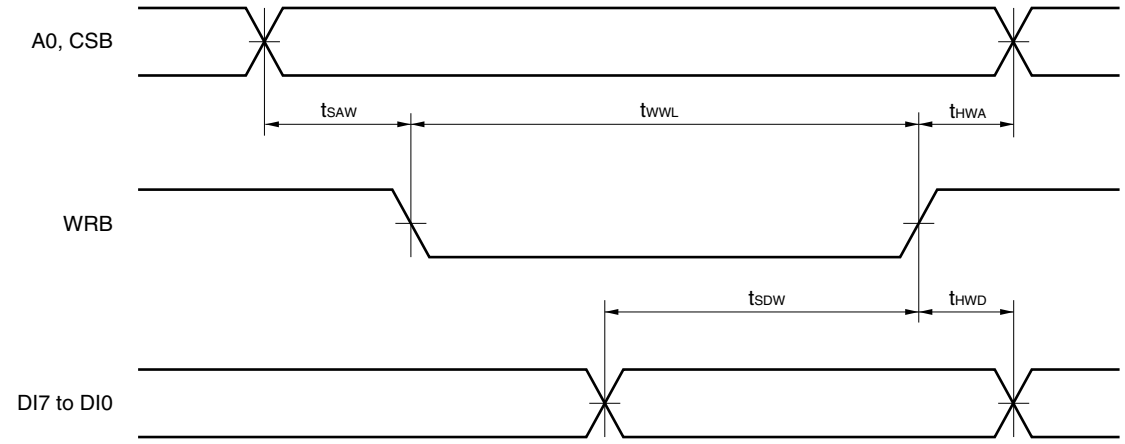
**Remark** The output load conditions of the propagation delay time are fanout: 1, wiring length: 0 mm.

## 4.5 Timing Charts

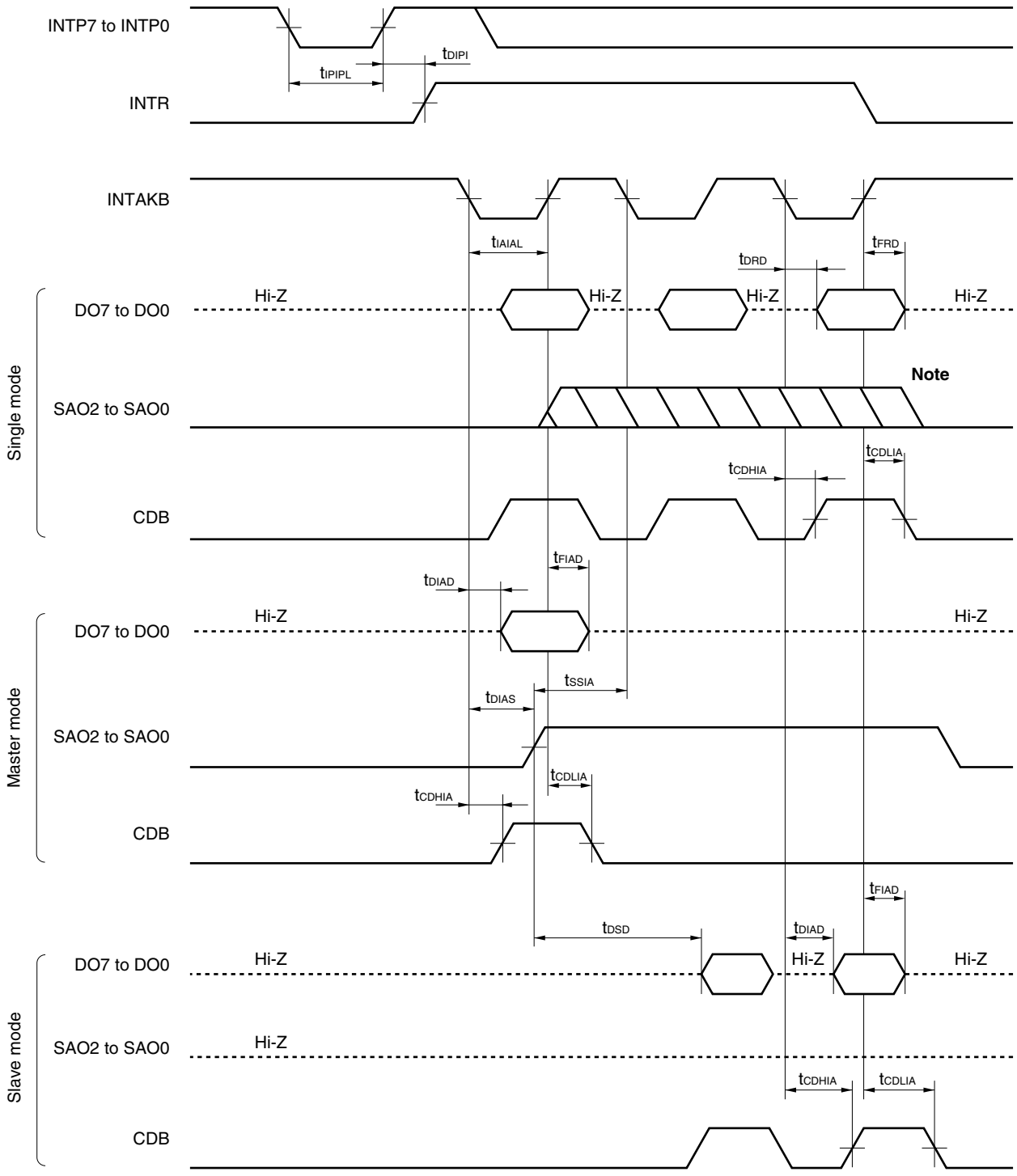
### (1) Read cycle




### (2) Write cycle

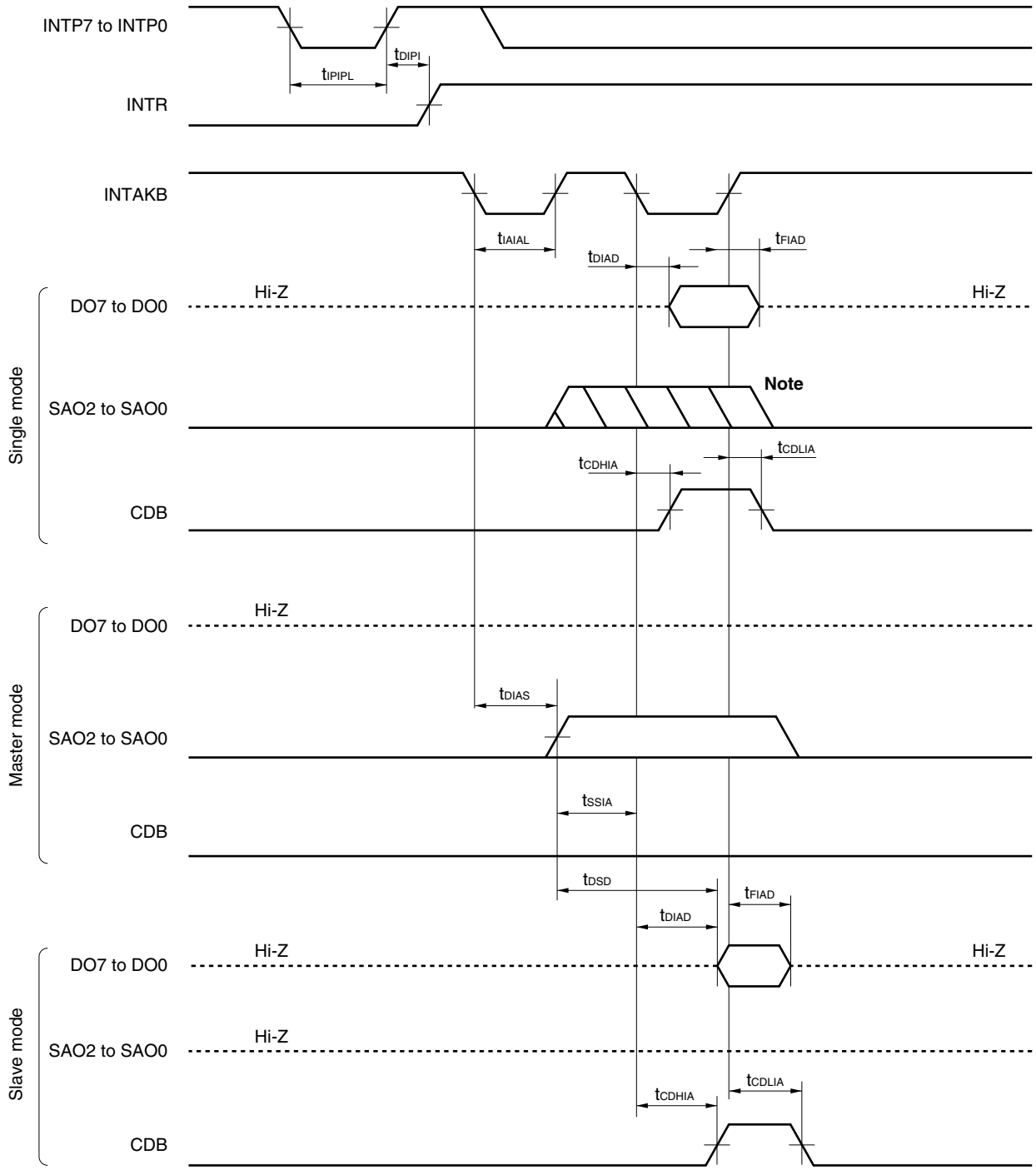


### (3) INTAKB sequence (CALL mode) timing




**Note** SAO2 to SAO0 are output even in the single mode but are meaningless.

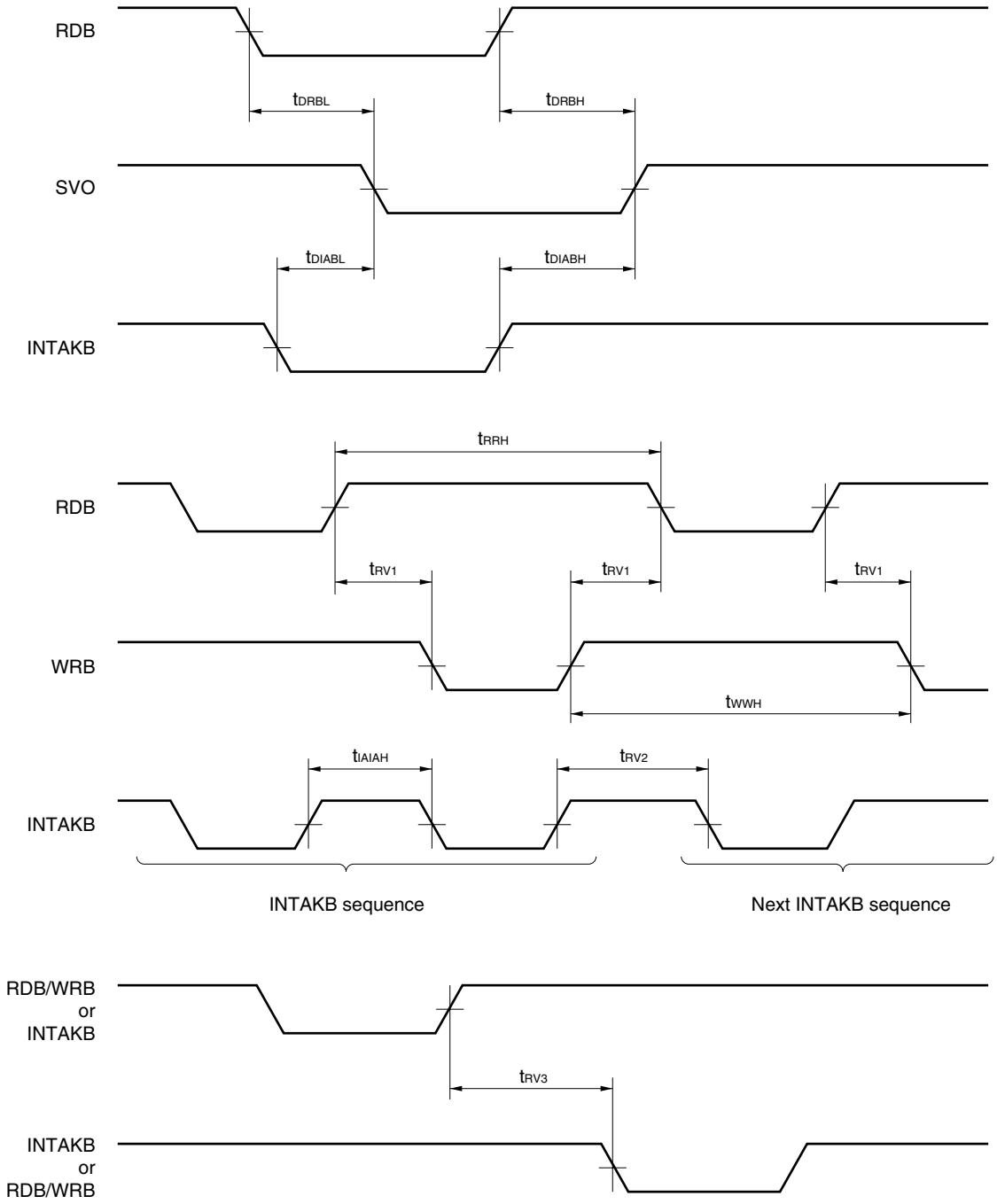
### (4) INTAKB sequence (vector mode) timing




**Note** SAO2 to SAO0 are output even in the single mode but are meaningless.

**Remark** Keep INTP input high at least until the INTAKB pulse falls the first time.

### (5) Other timing



## 4.6 Differences Between NA59A and μPD71059

- Level trigger or edge trigger of the interrupt request signal can be selected independently.
- Changes in the INTR signal can be prevented while it is high even if WRB goes low.
- Each interrupt request signal can be output independently.
- A reset signal can be issued independently in response to an interrupt request signal.
- Control pins for 3-state and output signals are added.
- Test pins are added (TBI33 to TBI0, TESTB, and through path test pin).
- DC and AC characteristics, and pin capacitance

Note that because the macro operations of the NA59A other than above are almost the same as those of the μPD71059, refer to the **μPD71059 User's Manual (U13042J)** (Japanese version only) and **μPD71059 Data Sheet (U11932J)** (Japanese version only) for operation details.

## 4.7 Notes on Designing Circuit

### 4.7.1 When using NA59A in same manner as μPD71059

**(1) INTP7 to INTP0**

The μPD71059 has internal pull-up resistors for INTP7 to INTP0, while the NA59A does not. To use the NA59A in the completely same manner as the μPD71059, connect a buffer with a pull-up resistor to INTP7 to INTP0 of the NA59A.

**(2) IRL7 to IRL0, INTCON**

Clamp all these pins to low level.

**(3) INTO7 to INTO0, ESLC7 to ESLC0**

Leave all these pins open. However, output these pins as test pins because they are used for the mega macro test in the same manner as the other pins.

**(4) SAI2 to SAI0, SAO2 to SAO0, CSA**

Use a bidirectional buffer and control the output by using CSA.

**(5) SVB, SVO, CSV**

Use a bidirectional buffer and control the output by using CSV.

### 4.7.2 Using IRL7 to IRL0

The μPD71059 can select an input trigger for INTP7 to INTP0 by using IW1, however, the same trigger must be selected for all these eight pins. The NA59A can set INTPx in the level trigger mode independently by making the corresponding IRLx high. When IRLx goes low, the corresponding INTPx is set in the edge trigger mode.

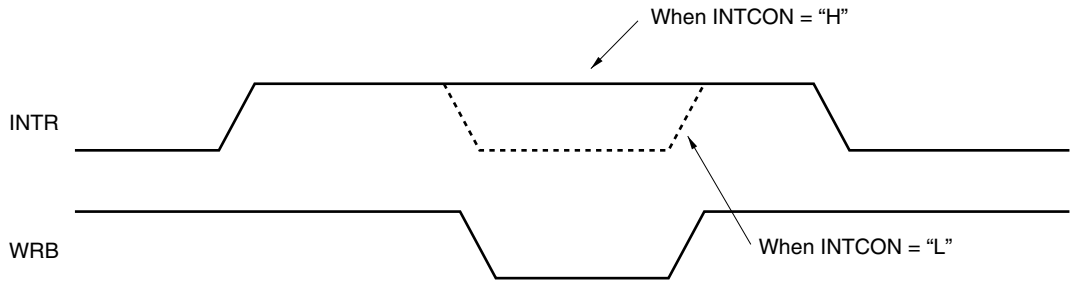
If D3 of IW1 is made high, all INTP7 to INTP0 are set in the level trigger mode, regardless of the level of IRL7 to IRL0.

**Remark** x: 0, 1, ...., 7

### 4.7.3 Using INTCON

If data is written to the μPD71059 while the INTR output is high, the INTR output goes low while WRB is low. With the NA59A, the INTR output can be kept high even while WRB is low, by making INTCON high in advance, even if data is written to the NA59A when the INTR output is high.

**Figure 4-1. Relationship Between INTCON, INTR, and WRB**




**Caution If INTR is connected to INTP of the NA59A (or μPD71059) when it is set in the edge trigger mode, or to a CPU that is detecting an edge, missing the detection of an interrupt can be prevented. This is because INTR goes low while WRB is low when the FI command is issued or when a no-operation command is used to write data.**
**If INTCON is high, however, the above feature cannot be used; therefore, use the level trigger mode.**

### 4.7.4 Using INTO7 to INTO0

INTO7 to INTO0 are output in response to the input signals INTP7 to INTP0 that serve as the source of the INTR output. INTP0 to INTP7 correspond to INTO0 to INTO7, respectively.

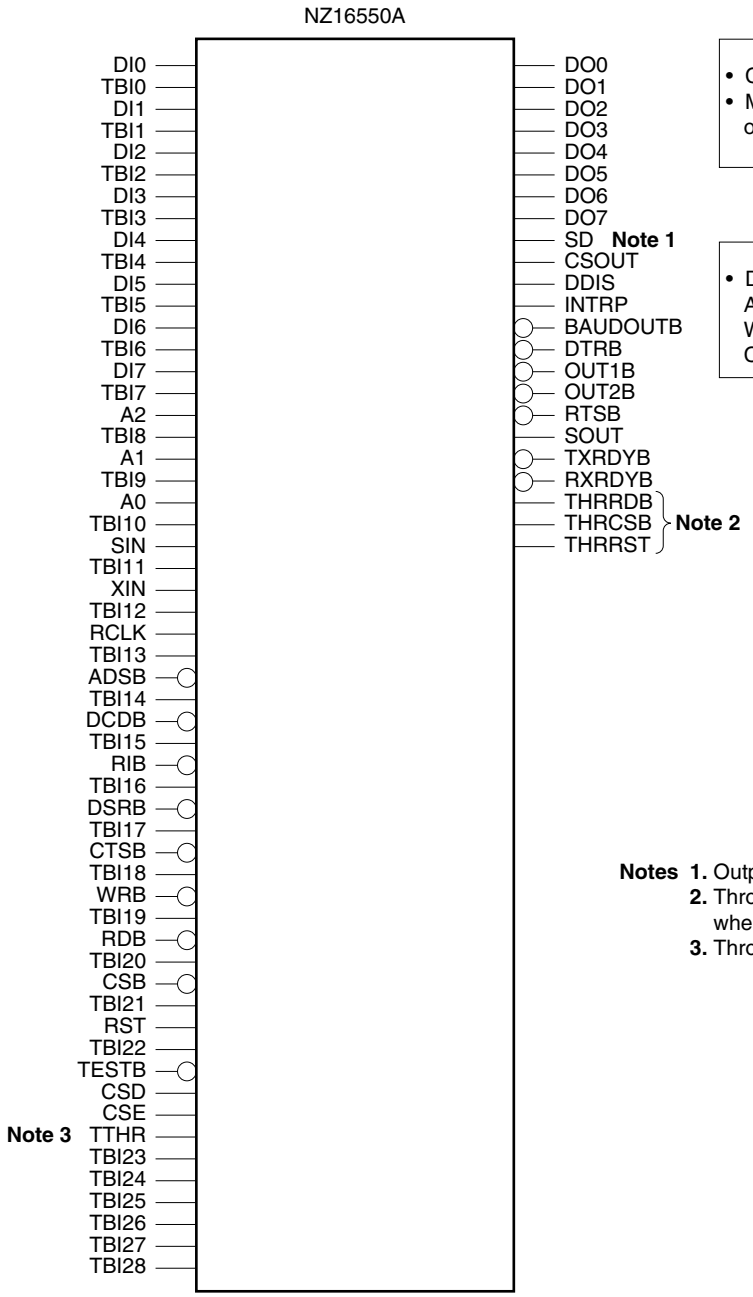
### 4.7.5 Using ESLC7 to ESLC0

These signals are asserted active (high) when ISR (in-service register) is cleared. They are output each time an interrupt signal that clears these signals is input.

# CHAPTER 5 NZ16550A MACRO

This chapter explains the functions of the NZ16550A.

| Block Type | Function |
|---|---|
| NZ16550A | UART + FIFO |




**Features**

- Compatible functions with PC16550D
- Maximum operating frequency: 33 MHz or equivalent

**Caution**

- Do not input spike to SIN, XIN, RCLK, ADSB, RIB, DCDB, DSRB, CTSB, WRB, RDB, CSB, RST, TESTB, CSD, CSE, TTHR, and TBI28 to TBI11.

**Notes 1.** Output control signal of DO7 to DO0
**2.** Through path output pins of RDB, CSB, and RST when pre-/post-mega-macro stages is tested
**3.** Through path/normal mode select pin

**Remark** The input signal pins with “TBI” prefixed are test pins.

| | |
|---|---|
| Number of cells used (configuration) | 9774 (181 × 54) |
| Mega macro test pattern length | 14889 |

<R>

## 5.1 Overview

### 5.1.1 General Description

The NZ16550A is an improved version of the original 16450 Universal Asynchronous Receiver/Transmitter (UART). Functionally identical to the 16450 on powerup (CHARACTER mode)[Note] the NZ16550A can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive software overhead.

In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is in logic to minimize system overhead and maximize system efficiency. Two pin functions have been changed to allow signalling of DMA transfers.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

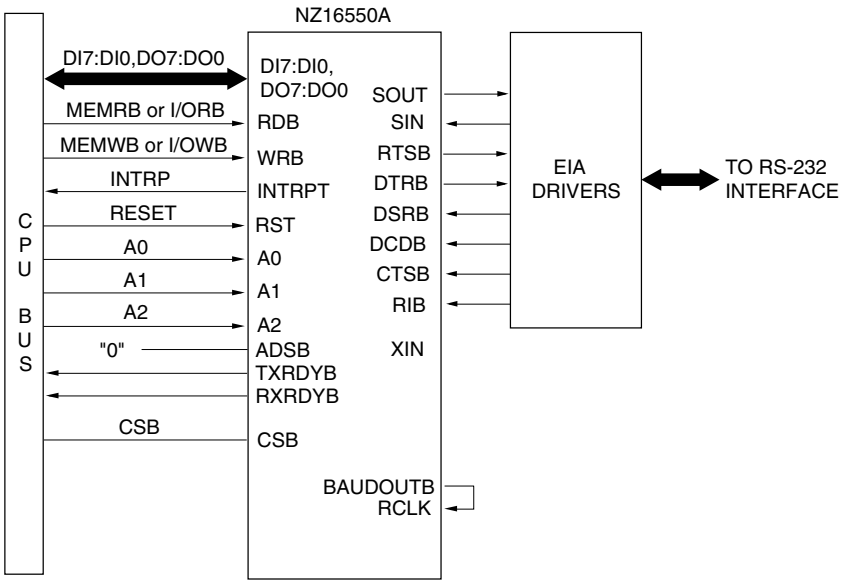
The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to ($2^{16}$-1), and producing a 16 $\times$ clock for driving the internal transmitter logic. Provisions are also included to use this 16 $\times$ clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

**Note** Can also be reset to 16450 Mode under software control.

### 5.1.2 Features

- Capable of running all existing 16450 software.
- After reset, all registers are identical to the 16450 register set.
- In the FIFO mode transmitter and receiver are each buffered with 16 byte FIFO's to reduce the number of interrupts presented to the CPU.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data.
- Holding and shift registers in the 16450 Mode eliminate the need for precise synchronization between the CPU and serial data.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator divides any input clock by 1 to ($2^{16}$-1) and generates the 16 × clock.
- Independent receiver clock input.
- MODEM control functions (CTSB, RTSB, DSRB, DTRB, RIB, and DCDB).
- Fully programmable serial-interface characteristics:
  5-, 6-, 7-, or 8-bit characters
  Even, odd, or no-parity bit generation and detection
  1-, 1 1/2-, or 2-stop bit generation
  Baud generation (DC to 1.5M baud).
- False start bit detection.
- Complete status reporting capabilities.
- TRI-STATE® TTL drive for the data and control buses.
- Line break generation and detection.
- Internal diagnostic capabilities:
  Loopback controls for communications link fault isolation
  Break, parity, overrun, framing error simulation.
- Full prioritized interrupt system controls.

**Basic Configuration**




**Caution Test pins are omitted.**

## 5.2 NZ16550A Pin Function

### 5.2.1 Pin function list

| Pin Name [Note 1] | I/O | Function | Active Level | Test Pin [Note 1] | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| DI0 | Input | Data bus input signal (LSB) | | TBI0 | 1.1 | L424 |
| DI1 | Input | Data bus input signal | | TBI1 | 1.1 | L424 |
| DI2 | Input | Data bus input signal | | TBI2 | 1.1 | L424 |
| DI3 | Input | Data bus input signal | | TBI3 | 1.1 | L424 |
| DI4 | Input | Data bus input signal | | TBI4 | 1.1 | L424 |
| DI5 | Input | Data bus input signal | | TBI5 | 1.1 | L424 |
| DI6 | Input | Data bus input signal | | TBI6 | 1.1 | L424 |
| DI7 | Input | Data bus input signal (MSB) | | TBI7 | 1.1 | L424 |
| A2 | Input | Address signal (used to access internal registers) | | TBI8 | 1.1 | L424 |
| A1 | Input | Address signal (used to access internal registers) | | TBI9 | 1.1 | L424 |
| A0 | Input | Address signal (used to access internal registers) | | TBI10 | 1.1 | L424 |
| SIN | Input | Serial data input | | TBI11 | 1.1 | L111 |
| <R> XIN | Input | System clock input [Note 2] | | TBI12 | 1.1 | L111 |
| <R> RCLK | Input | Reference clock input for determining reception rate [Note 2] | | TBI13 | 1.1 | L111 |
| ADSB | Input | Inputs strobe signal to latch address and chip select signals | Low | TBI14 | 1.1 | L111 |
| DCDB | Input | General-purpose input pin (Data Carrier Detect) | Low | TBI15 | 1.1 | L111 |
| RIB [Note 3] | Input | General-purpose input pin (Ring Indicator) | Low | TBI16 | 1.1 | L111 |
| DSRB | Input | General-purpose input pin (Data Set Ready) | Low | TBI17 | 1.1 | L111 |
| CTSB | Input | General-purpose input pin (Clear To Send) | Low | TBI18 | 1.1 | L111 |
| WRB | Input | Write signal | Low | TBI19 | 1.1 | L111 |
| RDB | Input | Read signal | Low | TBI20 | 1.1 | L111 |
| CSB | Input | Chip select signal | Low | TBI21 | 1.1 | L111 |
| RST | Input | Reset signal | High | TBI22 | 1.1 | L111 |
| TESTB | Input | Test/normal mode selection<br>“H”: Normal mode<br>“L”: Test mode | | – | 1.1 | L101 |
| CSD | Input | 3-state output control | | – | 1.1 | L101 |
| CSE | Input | 3-state output control | | – | 1.1 | L101 |
| TTHR | Input | Through path/normal mode select signal<br>“H”: Through path mode<br>“L”: Normal mode | | – | 1.1 | L101 |

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| DO0 | Output | Data bus output signal (LSB) | | – | 26.0 | F531 |
| DO1 | Output | Data bus output signal | | – | 26.0 | F531 |
| DO2 | Output | Data bus output signal | | – | 26.0 | F531 |
| DO3 | Output | Data bus output signal | | – | 26.0 | F531 |
| DO4 | Output | Data bus output signal | | – | 26.0 | F531 |
| DO5 | Output | Data bus output signal | | – | 26.0 | F531 |
| DO6 | Output | Data bus output signal | | – | 26.0 | F531 |
| DO7 | Output | Data bus output signal (MSB) | | – | 26.0 | F531 |
| SD | Output | Enable signal of data bus<br>0: High-impedance forced output<br>1: Normal 3-state operation | | – | 26.0 | F101 |
| CSOUT | Output | Signal indicating chip select status | High | – | 26.0 | F101 |
| DDIS | Output | Driver Disable | Low | – | 26.0 | F101 |
| INTRP | Output | Signal indicating interrupt status | High | – | 26.0 | F101 |
| BAUDOUTB | Output | Output clock from baud rate generator | | – | 26.0 | F101 |
| DTRB | Output | General-purpose input pin (Data Terminal Ready) | Low | – | 26.0 | F101 |
| OUT1B | Output | General-purpose input pin (Output1) | Low | – | 26.0 | F101 |
| OUT2B | Output | General-purpose input pin (Output2) | Low | – | 26.0 | F101 |
| RTSB | Output | General-purpose input pin (Request To Send) | Low | – | 26.0 | F101 |
| SOUT | Output | Serial data output | | – | 26.0 | F101 |
| TXRDYB | Output | Transmission ready signal | Low | – | 26.0 | F101 |
| RXRDYB | Output | Reception ready signal | Low | – | 26.0 | F101 |
| THRRDB | Output | Through path output test pin (RDB signal) | | – | 26.0 | F101 |
| THRCSB | Output | Through path output test pin (CSB signal) | | – | 26.0 | F101 |
| THRRST | Output | Through path output test pin (RST signal) | | – | 26.0 | F101 |
| TBI0 | Input | Test input | | – | 1.0 | L424 |
| TBI1 | Input | Test input | | – | 1.0 | L424 |
| TBI2 | Input | Test input | | – | 1.0 | L424 |
| TBI3 | Input | Test input | | – | 1.0 | L424 |
| TBI4 | Input | Test input | | – | 1.0 | L424 |
| TBI5 | Input | Test input | | – | 1.0 | L424 |
| TBI6 | Input | Test input | | – | 1.0 | L424 |
| TBI7 | Input | Test input | | – | 1.0 | L424 |
| TBI8 | Input | Test input | | – | 1.0 | L424 |
| TBI9 | Input | Test input | | – | 1.0 | L424 |
| TBI10 | Input | Test input | | – | 1.0 | L424 |
| TBI11 | Input | Test input | | – | 1.1 | L111 |
| <R> TBI12 | Input | Test input Note 2 | | – | 1.1 | L111 |
| <R> TBI13 | Input | Test input Note 2 | | – | 1.1 | L111 |
| TBI14 | Input | Test input | | – | 1.1 | L111 |

| Pin Name | I/O | Function | Active Level | Test Pin | Fanin/ Fanout | Block Name |
|---|---|---|---|---|---|---|
| TBI15 | Input | Test input | | – | 1.1 | L111 |
| TBI16 | Input | Test input | | – | 1.1 | L111 |
| TBI17 | Input | Test input | | – | 1.1 | L111 |
| TBI18 | Input | Test input | | – | 1.1 | L111 |
| TBI19 | Input | Test input | | – | 1.1 | L111 |
| TBI20 | Input | Test input | | – | 1.1 | L111 |
| TBI21 | Input | Test input | | – | 1.1 | L111 |
| TBI22 | Input | Test input | | – | 1.1 | L111 |
| TBI23 | Input | Test mode pin | | – | 1.1 | L302 |
| TBI24 | Input | Test mode pin | | – | 1.1 | L101 |
| TBI25 | Input | Test mode pin | | – | 1.1 | L101 |
| TBI26 | Input | Test mode pin | | – | 1.1 | L302 |
| TBI27 | Input | Test mode pin | | – | 1.1 | L302 |
| TBI28 | Input | Test mode pin | | – | 1.1 | L302 |

**Notes 1.** The (normal) pin and the test pin described in the same line have the same function.

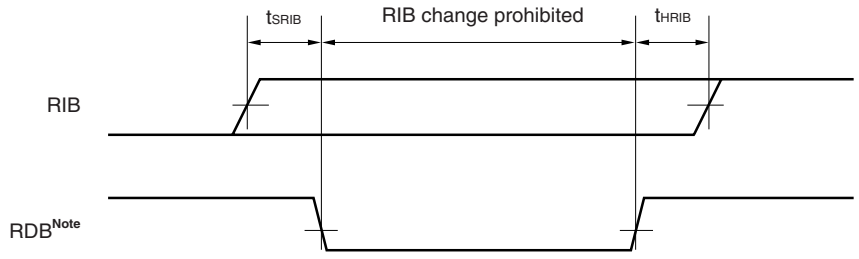
**2.** Provide a clock pin (a pin described as “clock” in the Function column) using an input pin, not a bidirectional pin. A pin of pertinence is as follows:

<R> Pin Name : XIN, RCLK, TBI12, TBI13

**3.** When not using the RIB pin, clamp it to “H” or “L”.

When using the RIB pin, satisfy the following timings:

| Parameter | Symbol | MIN. | Unit |
|---|---|---|---|
| RIB rise setup time (to RDB↓) | $t_{SRIB}$ | 5.0 | ns |
| RIB rise hold time (from RDB↑) | $t_{HRIB}$ | 5.0 | ns |




**Note** RDB is the timing at which the modem status register is read (MSR A = 6).

**Remark** Input: Input pin
Output: Output pin

**Remarks 1.** TBIx is a test input pin. A signal can be input from TBIx by making TESTB input low. Make a connection so that signals can be directly input to the mega macro from outside the gate array in the test mode. "Directly" here means a circuit configuration where the input signal is not inverted and no sequential circuit such as a flip-flop is inserted in between.

| TESTB | Input Pin |
|---|---|
| 1 | Normal pin[Note] |
| 0 | TBIx |

**Note** Input a defined value of 0 or 1 to the test input pins in the normal mode (it does not matter if 0 and 1 are mixed).

**2.** Functions of CSD input and CSE input

CSE input : Turned on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input : Turned off (high-impedance: Hi-Z) all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

| CSE | CSD | Status of Output Pin | Status of 3-State Output Pin[Note] |
|---|---|---|---|
| 0 | 0 | Normal operation | Hi-Z |
| 0 | 1 | Normal operation | Normal operation |
| 1 | – | Normal operation | Hi-Z is not output. |

**Note** The 3-state pins are DO7 to DO0.

**3.** When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

| "Hi-Z" Pin | Corresponding Output Control Signal and Output | |
|---|---|---|
| DO7 to DO0 | SD | 0 |

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output buffer does not go into a the "Hi-Z" state).

**4.** CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

**Remarks 5.** Operating status of output pin depending on combination of TTHR, CSE, and CSD

| TTHR Pin | CSE Pin | CSD Pin | 3-State Output Pin (DOx) | 3-State Control Pin (CDB(SD)) | Other Pins | Through Path Pin (Output THRxxx) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Hi-Z | 0 | Normal operation | 0 |
| | | 1 | Normal operation | Normal operation | | |
| | 1 | 0 | Hi-Z is not output. | 0 | | |
| | | 1 | | Normal operation | | |
| 1 | 0 | 0 | Hi-Z | Through path | Through path | Through path |
| | | 1 | Through path | | | |
| | 1 | × | | | | |

**6.** I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| DO0 | DI0 | TBI0 |
| DO1 | DI1 | TBI1 |
| DO2 | DI2 | TBI2 |
| DO3 | DI3 | TBI3 |
| DO4 | DI4 | TBI4 |
| DO5 | DI5 | TBI5 |
| DO6 | DI6 | TBI6 |
| DO7 | DI7 | TBI7 |
| SD | A2 | TBI8 |
| CSOUT | A1 | TBI9 |
| DDIS | A0 | TBI10 |
| INTRP | SIN | TBI11 |

| Output Pin | Through Path Corresponding Pin | |
|---|---|---|
| | TESTB = 1 | TESTB = 0 |
| BAUDOUTB | XIN | TBI12 |
| DTRB | RCLK | TBI13 |
| OUT1B | ADSB | TBI14 |
| OUT2B | DCDB | TBI15 |
| RTSB | RIB | TBI16 |
| SOUT | DSRB | TBI17 |
| TXRDYB | CTSB | TBI18 |
| RXRDYB | WRB | TBI19 |
| THRRDB | RDB | TBI20 |
| THRCSB | CSB | TBI21 |
| THRRST | RST | TBI22 |

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high-impedance status).

### <R> 5.2.2 Pin Descriptions

The following describes the function of all UART pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+3.3V nominal).

A0, A1, A2, Register Select : Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

**Register Addresses**

| DLAB | A2 | A1 | A0 | Register |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Receiver Buffer (read), Transmitter Holding Register (write) |
| 0 | 0 | 0 | 1 | Interrupt Enable |
| X | 0 | 1 | 0 | Interrupt Identification (read) |
| X | 0 | 1 | 0 | FIFO Control (write) |
| X | 0 | 1 | 1 | Line Control |
| X | 1 | 0 | 0 | MODEM Control |
| X | 1 | 0 | 1 | Line Status |
| X | 1 | 1 | 0 | MODEM Status |
| X | 1 | 1 | 1 | Scratch |
| 1 | 0 | 0 | 0 | Divisor Latch (least significant byte) |
| 1 | 0 | 0 | 1 | Divisor Latch (most significant byte) |

ADSB, Address Strobe : The positive edge of an active Address Strobe (ADSB) signal latches the Register Select (A0, A1, A2) and Chip Select (CSB) signals.

**Caution An active ADSB input is required when the Register Select (A0, A1, A2) and Chip Select (CSB) signals are not stable for the duration of a read or write operation. If not required, tie the ADS input permanently low.**

BAUDOUTB, Baud Out : This is the 16 × clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUTB may also be used for the receiver section by tying this output to the RCLK input of the chip.

CSB, Chip Select : When CSB is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If ADSB is always low, valid chip selects should stabilize according to the $t_{CSW}$ parameter.

CTSB, Clear to Send : When low, this indicates that the MODEM or data set is ready to exchange data. The CTSB signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the CTSB signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTSB input has changed state since the previous reading of the MODEM Status Register. CTSB has no effect on the Transmitter.

**Caution Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled**

DI0-DI7,DO0-DO7, Data Bus : This bus comprises eight TRISTATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the DI0-DI7,DO0-DO7 Data Bus.

DCDB, Data Carrier Detect : When low, indicates that the data carrier has been detected by the MODEM or data set. The DCDB signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the DCDB signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the DCDB input has changed state since the previous reading of the MODEM Status Register. DCDB has no effect on the receiver.

**Caution Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.**

DDIS, Driver Disable : This goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART.

DSRB, Data Set Ready : When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The DSRB signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the DSRB signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSRB input has changed state since the previous reading of the MODEM Status Register.

**Caution Whenever the DDSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.**

DTRB, Data Terminal Ready : When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The DTRB output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

INTRP, Interrupt : This pin goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available: timeout (FIFO Mode only); Transmitter Holding Register Empty; and MODEM Status. The INTRP signal is reset low upon the appropriate interrupt service or a Master Reset operation.

RST, Master Reset : When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTRP, OUT 1B, OUT 2B, RTSB, DTRB) are affected by an active RST input (Refer to Table 5-1. and Table 5-2.)

OUT 1B, Output 1 : This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.

OUT 2B, Output 2 : This user-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the XMOS parts this will achieve TTL levels.

RCLK, Receiver Clock : This input is the 16 × baud rate clock for the receiver section of the chip.

RDB, Read : When RDB is low while the chip is selected, the CPU can read status information or data from the selected UART register.

**Caution Only an active RDB input is required to transfer data from the UART during a read operation. Therefore, tie the RDB input permanently high, when it is not used.**

RIB, Ring Indicator : When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The RIB signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the RIB signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the RIB input signal has changed from a low to a high state since the previous reading of the MODEM Status Register.

**Caution Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.**

RTSB, Request to Send : When low, this informs the MODEM or data set that the UART is ready to exchange data. The RTSB output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

SIN, Serial Input : Serial data input from the communications link (peripheral device, MODEM, or data set).

SOUT, Serial Output : Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

TXRDYB, RXRDYB : Transmitter and Receiver DMA signalling is available through two pins. When operating in the FIFO mode, one of two types of DMA signalling per pin can be selected via FCR3. When operating as in the 16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied or the XMIT FIFO has been filled.

RXRDY, Mode 0: When in the 16450 Mode (FCR0=0) or in the FIFO Mode (FCR0=1, FCR3=0) and there is at least 1 character in the RCVR FIFO or RCVR holding register, the RXRDY pin will be low active. Once it is activated the RXRDY pin will go inactive when there are no more characters in the FIFO or holding register.

RXRDY, Mode 1: In the FIFO Mode (FCR0=1) when the FCR3=1 and the trigger level or the timeout has been reached, the RXRDY pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or holding register.

TXRDY, Mode 0: In the 16450 Mode (FCR0=0) or in the FIFO Mode (FCR0=1, FCR3=0) and there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY pin will be low active. Once it is activated the TXRDY pin will go inactive after the first character is loaded into the XMIT FIFO or holding register.

TXRDY, Mode 1: In the FIFO Mode (FCR0=1) when FCR3=1 and there are no characters in the XMIT FIFO, the TXRDYB pin will go low active. This pin will become inactive when the XMIT FIFO is completely full.

$V_{SS}$ : Ground (0V) reference.

WRB, Write : When WRB is low while the chip is selected, the CPU can write control words or data into the selected UART register.

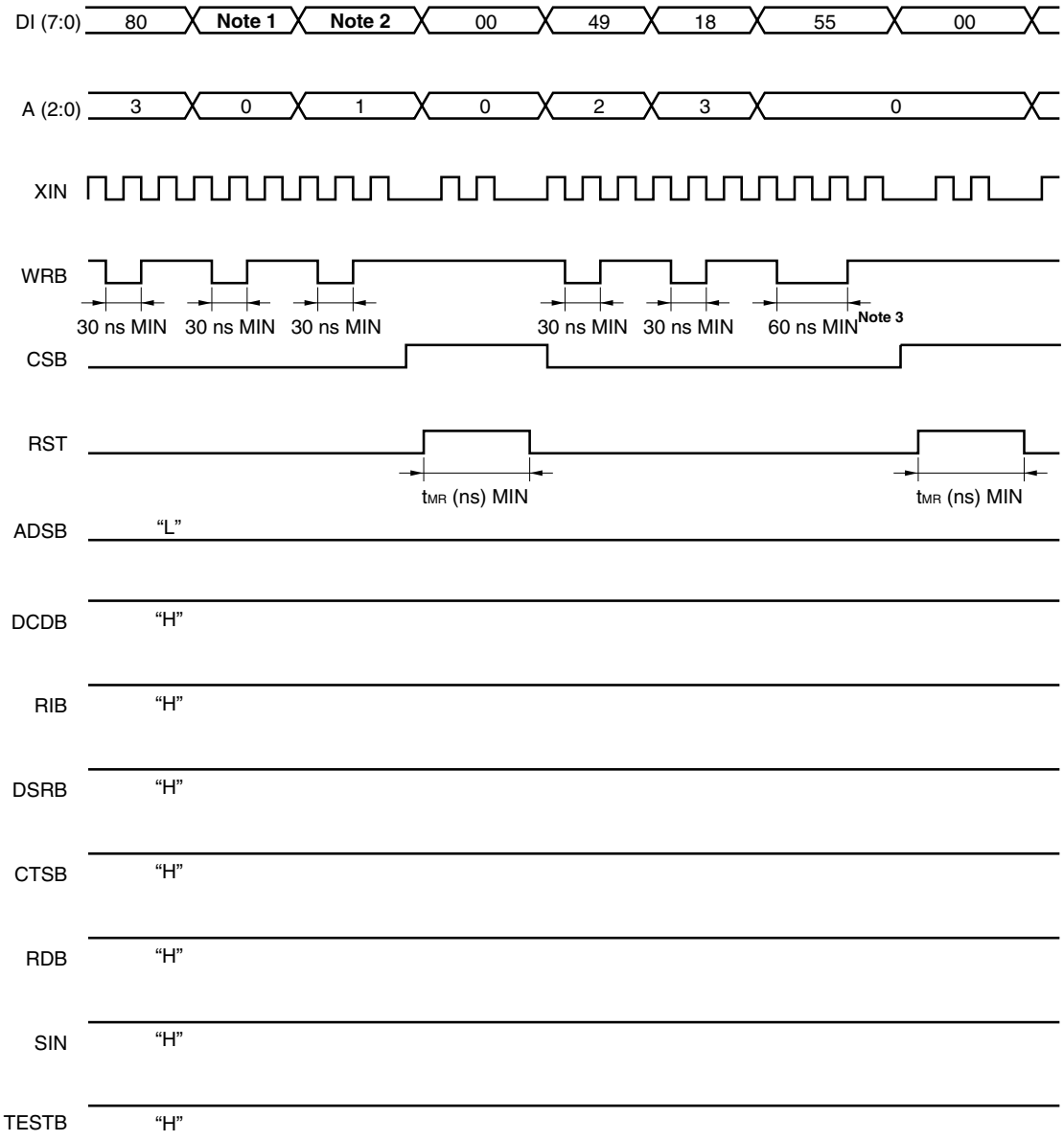
**Caution Only an active WRB input is required to transfer data to the UART during a write operation. Therefore, tie the WRB input permanently high, when it is not used.**

XIN (System Clock Input)

## <R> 5.3 NZ16550A Initialization Pattern and Notes on Creating Test Pattern

The NZ16550A is initialized as follows:

**Figure 5-1. Initialization Pattern**




**Notes 1.** Lower byte of division ratio to be used.

**2.** Higher byte of division ratio to be used.

<R> **3.** 60 ns or longer is required to fix the loop circuit value in simulation.

**Cautions 1. Input "0" or "1" to the other input pins (normal input and test input pins). Make sure that "X" is not input to these pins.**

**2. Input the division ratio to Notes 1, 2, and be sure to reset after the division ratio is set.**

**Remark** $t_{MR}$: Reset pulse high-level width

### 5.3.1 Status of output pin after initialization

The status of the output pin is as follows after initialization:

**Table 5-1. Status of Output Pin After Initialization**

| Output Pin Name | Pin Status |
|---|---|
| DO(7:0) | When CSE = 0: Hi-Z<br>When CSE = 1: Low level |
| SD | Low level |
| CSOUT | Low level |
| DDIS | High level |
| INTRP | Low level |
| BAUDOUTB | Clock resulting from dividing frequency of reference clock (XIN) by the value specified at the baud rate generator divisor latch. |
| DTRB | High level |
| OUT1B | High level |
| OUT2B | High level |
| RTSB | High level |
| SOUT | High level |
| TXRDYB | Low level |
| RXRDYB | High level |

### 5.3.2 Default value after reset

The default values of the registers and output signals (general-purpose output signals and serial data output signals) are as follows when the NZ16550A has been reset.

**Table 5-2. Default Values of Registers**

| Register | Default Value MSB LSB |
|---|---|
| IER | 00000000 |
| IIR | 00000001 |
| FCR | 00000000 |
| LCR | 00000000 |
| MCR | 00000000 |
| LSR | 01100000 |
| MSR | 00000000 |

**Table 5-3. Default Values of Output Signals (General-Purpose Output Signals and Serial Data Output Signals)**

| Output Signal Name | Default Value |
|---|---|
| SOUT | 1 |
| DTRB | 1 |
| OUT1B | 1 |
| OUT2B | 1 |
| RTSB | 1 |

<R> **5.3.3 Notes on Creating Test Pattern**

The description (1) is a restriction that affects actual chips. However, (2) to (5) are restrictions on simulation, so these are not applicable to actual chips.

(1) Configure the circuit of the following input pins so that spike is not input.
SIN, XIN, RCLK, ADSB, DCDB, RIB, DSRB, CTSB, WRB, RDB, CSB, RST, TESTB, CSD, CSE, TTHR, TBI28 to TBI11

(2) Do not change the divisor latch value after initialization.

(3) Configure the circuit so that the changes of XIN and RST do not conflict.

(4) Configure the circuit so that the rising edges of XIN and WRB do not conflict. (A pattern in which the falling edge of XIN and the rising edge of WRB are synchronized is recommended.)

(5) Configure the circuit so that the change of SIN and the rising edge of RCLK do not conflict. (A pattern in which the change of SIN and the falling edge of RCLK are synchronized is recommended.)

## 5.4 Delay Time

Refer to **1.2.4 Delay time**.

## 5.5 AC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 3.3 ±0.3 V)

### (1) Read cycle and write cycle

| Parameter | | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Address strobe (ADSB) pulse width | | $t_{ADS}$ | 10 | | ns |
| Address (A2, A1, A0) hold time (from ADSB ↑) | | $t_{AH}$ | 2 | | ns |
| Address (A2, A1, A0) setup time (to RDB ↓) | | $t_{AR}$ | 3 | | ns |
| Address (A2, A1, A0) setup time (to ADSB ↑) | | $t_{AS}$ | 3 | | ns |
| Address (A2, A1, A0) setup time (to WRB ↓) | | $t_{AW}$ | 3 | | ns |
| Chip select (CSB) hold time (from ADSB ↑) | | $t_{CH}$ | 0 | | ns |
| Chip select (CSB) setup time (to ADSB ↑) | | $t_{CS}$ | 4 | | ns |
| Chip select (CSB) setup time (to RDB ↓) | | $t_{CSR}$ | 4 | | ns |
| Chip select (CSB) setup time (to WRB ↓) | | $t_{CSW}$ | 4 | | ns |
| Data hold time (from WRB ↑) | | $t_{DH}$ | 8 | | ns |
| Data setup time (to WRB ↓) | | $t_{DS}$ | 0 | | ns |
| Data float delay time (from RDB ↑) | | $t_{HZ}$ | 1 | 3 | ns |
| Reset pulse high-level width | | $t_{MR}$ | 100 | | ns |
| Address (A2, A1, A0) hold time (from RDB ↑) | | $t_{RA}$ | 0 | | ns |
| Read cycle delay time | | $t_{RC1}$ | | 3 | ns |
| Read cycle ADSB hold time | | $t_{RC2}$ | | 10 | ns |
| Chip select (CSB) hold time (from RDB ↑) | | $t_{RCS}$ | 0 | | ns |
| RDB active pulse width | | $t_{RD}$ | 30 | | ns |
| DDIS delay time (from RDB) | | $t_{RDD}$ | 2 | 3 | ns |
| Data delay time (from RDB ↓) | | $t_{RVD}$ | | 10 | ns |
| Address (A2, A1, A0) hold time (from WRB ↑) | | $t_{WA}$ | 0 | | ns |
| Write cycle delay time | | $t_{WC1}$ | 30 | | ns |
| Write cycle ADSB hold time | | $t_{WC2}$ | 1 | | ns |
| Chip select (CSB) hold time (from WRB ↑) | | $t_{WCS}$ | 0 | | ns |
| WRB active pulse width | | $t_{WR}$ | 30 | | ns |
| Clock pulse high-level width | | $t_{XH}$ | 13.5 | | ns |
| Clock pulse low-level width | | $t_{XL}$ | 13.5 | | ns |
| Read cycle time | In 16450 mode | RC | 38 | | ns |
| | When RXRDYB is not used | | 47 | | ns |
| | When RXRDYB is used | | 55 | | ns |
| Write cycle time | In 16450 mode | WC | 38 | | ns |
| | When TXRDYB is not used | | 47 | | ns |
| | When TXRDYB is used | | 55 | | ns |
| Read/write recovery time | In 16450 mode | $t_{RV}$ | 8 | | ns |
| | When RXRDYB and TXRDYB are not used | | 17 | | ns |
| | When RXRDYB and TXRDYB are used | | 25 | | ns |

### (2) Baud rate generator

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| Transmission clock division ratio | N | 1 | $2^{16} - 1$ | |
| Transmission clock rise delay time (from XIN) | $t_{BHD}$ | | 4 | ns |
| Transmission clock fall delay time (from XIN) | $t_{BLD}$ | | 7 | ns |
| Transmission clock pulse high-level width[Note] | $t_{HW}$ | 120 | | ns |
| Transmission clock pulse low-level width[Note] | $t_{LW}$ | 120 | | ns |

**Note** $f_X$ = 8.0 MHz, BAUDOUTB = XIN/2

### (3) Receiver and transmitter

| Parameter | | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Interrupt clear time (from RDB ↑ when LSR is read)) | | $t_{RINT}$ | | 14 | ns |
| Interrupt clear time (from RDB ↓ when RBR is read)) | | $t_{RINT}$ | | 26 | ns |
| RXRDYB clear time (from RDB ↓ (RBR)) | 16450 mode | $t_{RXI0}$ | | 20 | ns |
| | FIFO mode | $t_{RXI1}$ | | 25 | ns |
| Sample clock delay time (from RCLK) | | $t_{SCD}$ | | 6 | ns |
| Interrupt generation time (from valid data reception or reception error) | | $t_{SINT}$ | | 1 | RCLK cycles[Note] |
| Interrupt clear time (from WRB ↓ (during THR write)) | | $t_{HR}$ | | 8 | ns |
| Interrupt clear time (from RDB ↑ (during IIR read)) | | $t_{IR}$ | | 7 | ns |
| Transmission start time | | $t_{IRS}$ | 8 | 24 | BAUDOUTB cycles |
| Interrupt generation time (from WRB ↑ (during THR write)) | | $t_{SI}$ | 16 | 24 | BAUDOUTB cycles |
| Interrupt (THRE) generation time (from stop bit) | | $t_{STI}$ | | 8 | BAUDOUTB cycles |
| TXRDYB generation time (vs. start bit) | | $t_{SXA}$ | | 8 | BAUDOUTB cycles |
| TXRDYB clear time | 16450 mode, FIFO mode (DMA = 0) (from WRB ↓ (during THR write)) | $t_{WXI0}$ | | 20 | ns |
| | FIFO mode (DMA = 1) (from WRB ↑ (during THR write)) | $t_{WXI1}$ | | 25 | ns |

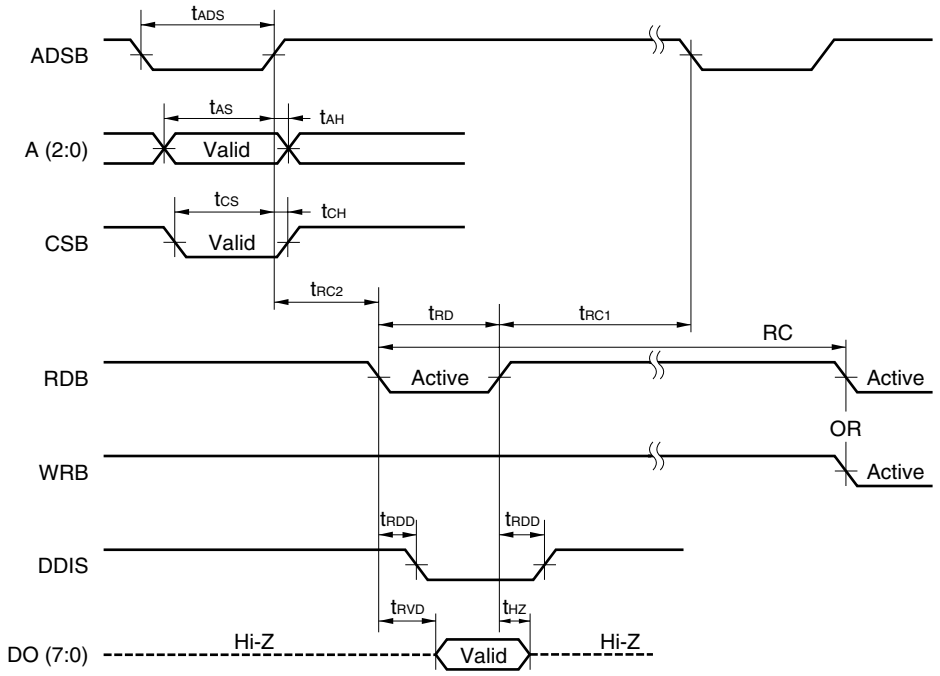
**Note** The high-level width of PRCLK is the same as $t_{XH}$, and the low-level width is the same as $t_{XL}$.
When FCR0 = 1, $t_{SINT}$ = 3RCLK. When a timeout interrupt occurs, $t_{SINT}$ = 8RCLK.

### (4) Modem control

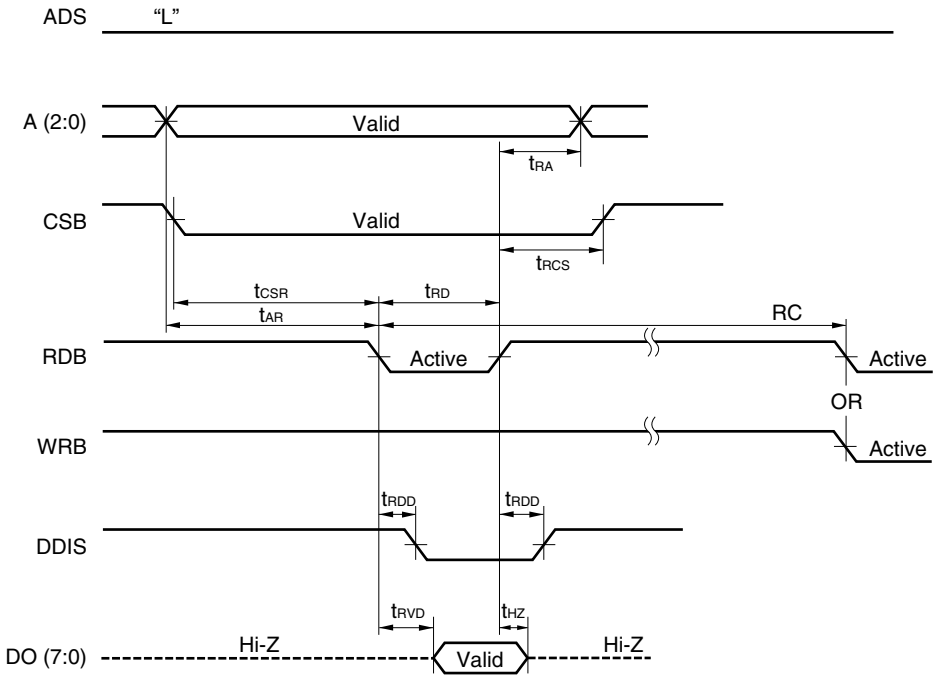
| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| RTSB, DTRB, OUT1B, OUT2B delay time (from WRB ↑ (during MCR write)) | $t_{MDO}$ | | 6 | ns |
| Interrupt clear time (from RDB ↓ (during MSR read)) | $t_{RIM}$ | | 9 | ns |
| Interrupt generation time (from RIB ↑, CTSB, DSRB, DCDB) | $t_{SIM}$ | | 8 | ns |

## 5.6 Timing Charts

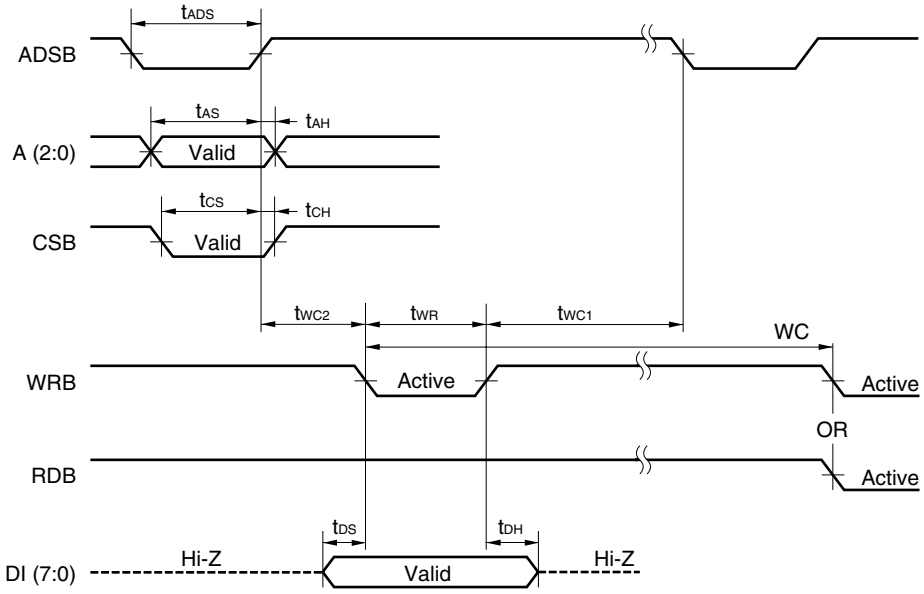
### (1) Read cycle timing (when ADSB is used)



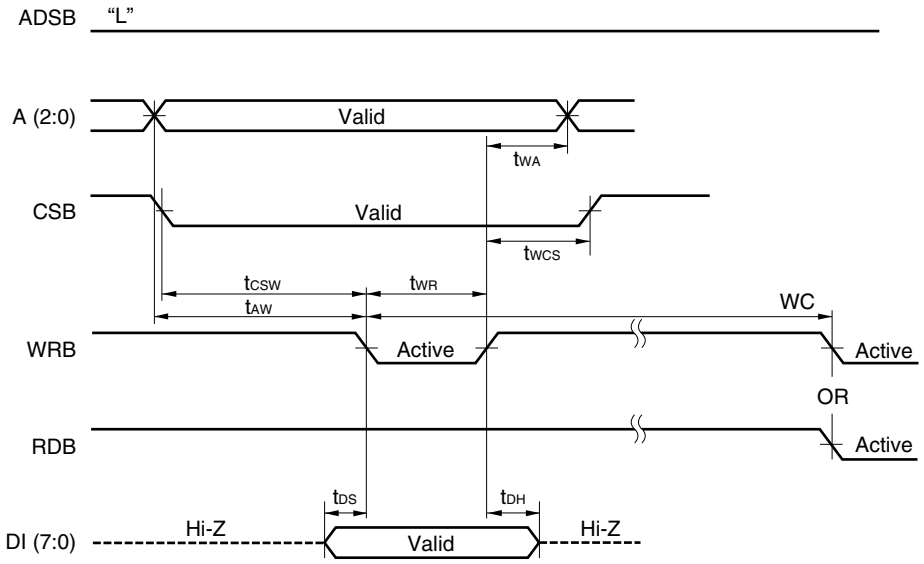

### (2) Read cycle timing (when ADSB is clamped low)



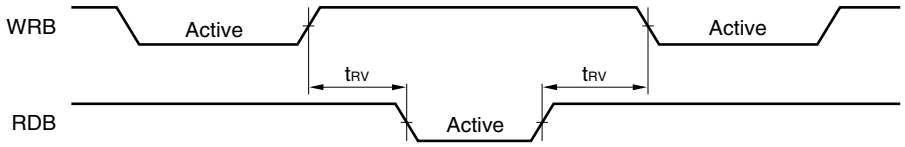
### (3) Write cycle timing (when ADSB is used)




### (4) Write cycle timing (when ADSB is clamped low)

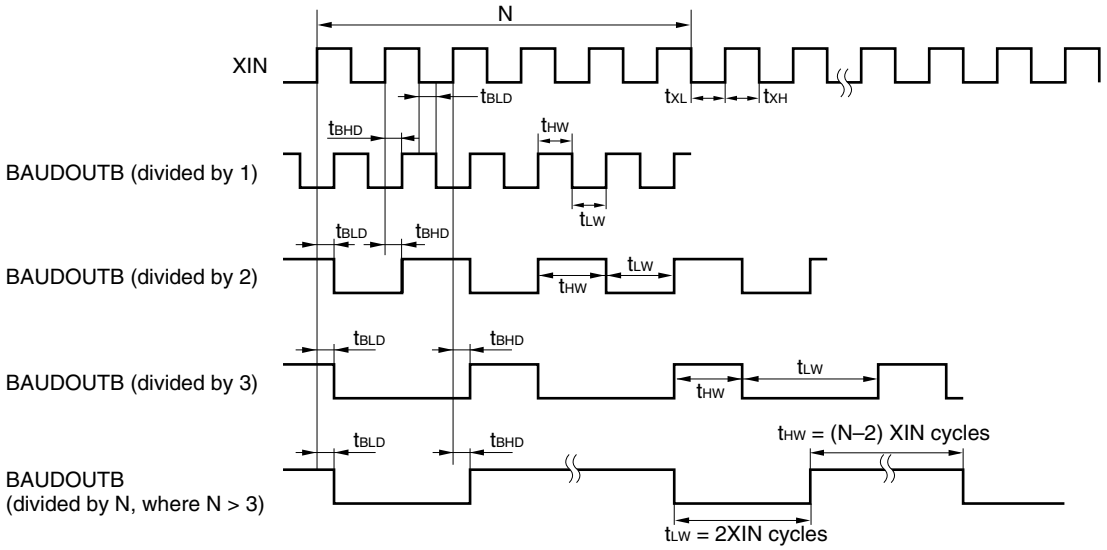


### (5) Write and read recovery time

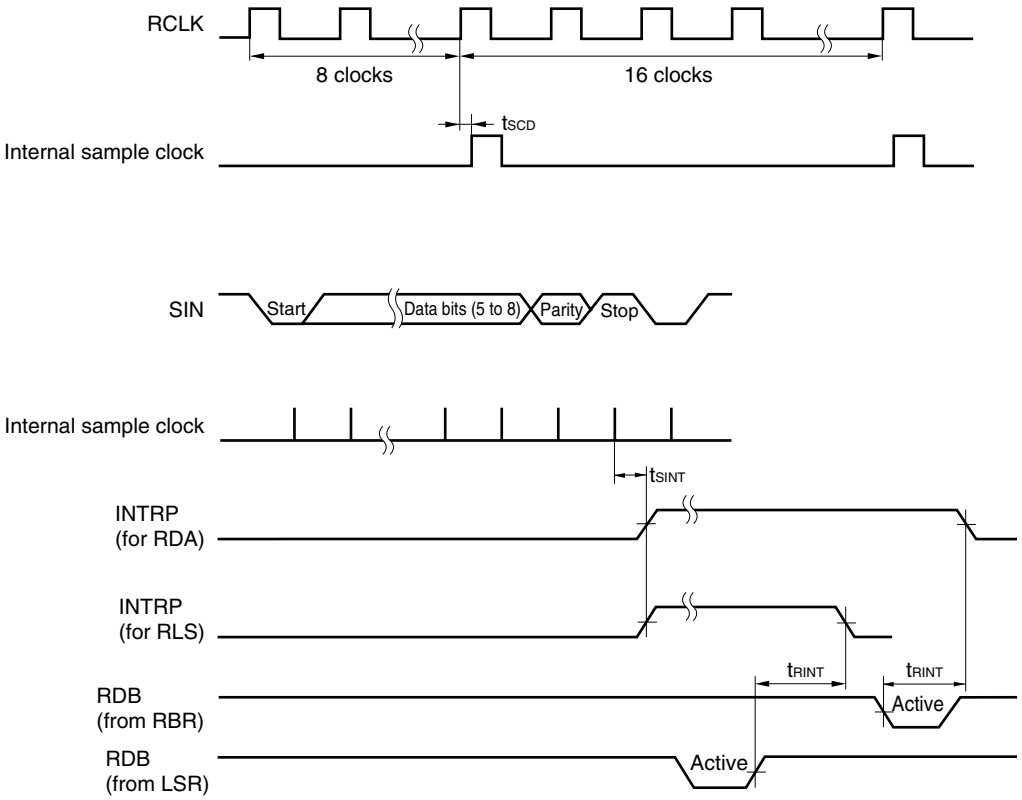



**Remark** When the RDB and WRB signals are simultaneously asserted active, an internal spike may be generated causing the device to malfunction. Therefore, do not assert the RDB and WRB signals active at the same time.

### (6) Baud out timing



### (7) Reception timing




**Remarks 1.** INTRP (for RDA) indicates the existence of receive data.
At this time, bit 0 of IER (ERBFI) is 1, and bits 1 to 3 of IIR are 010b.

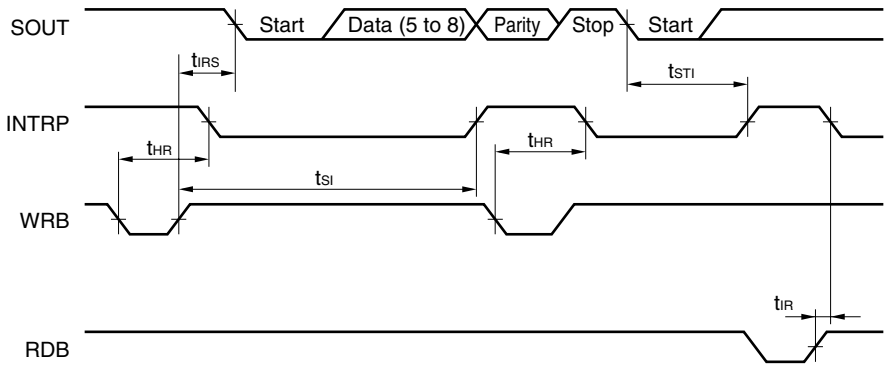
**2.** RDB (from RBR) reads RBR of A (2:0) = 000b.

**3.** INTRP (for RLS) indicates a receive line status.
At this time, bit 2 (ERLSI) of IER is 1, and bits 1 to 3 of IIR are 011b.

**4.** RDB (from LSR) reads LSR of A (2:0) = 101b.

For details of the read timing, refer to **(1) Read cycle timing (when ADSB is used)** and **(2) Read cycle timing (when ADSB is clamped low)**.

### (8) Transmission timing




**Remarks 1.** INTRP indicates that the transmit buffer is empty.
At this time, bit 1 (ETBEI) of IER is 1, and bits 1 to 3 of IIR are 001b.

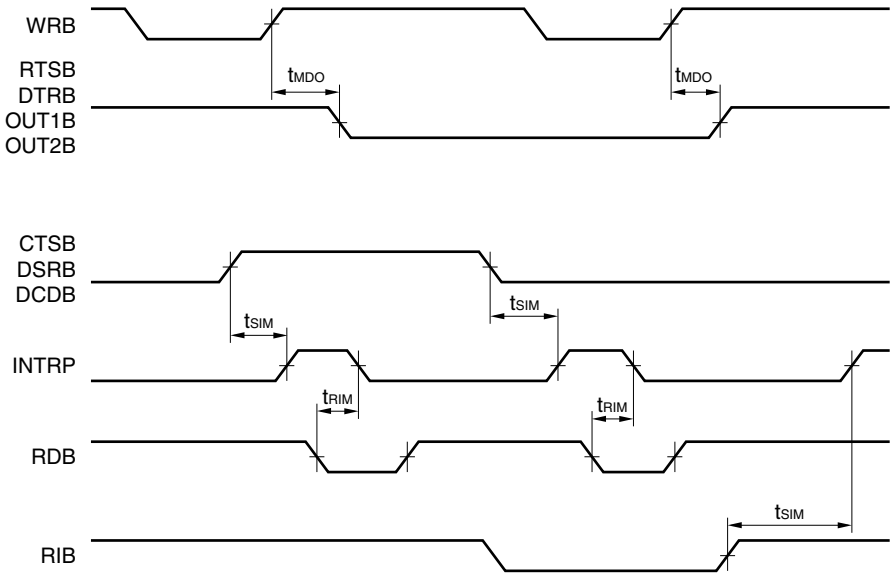
**2.** WRB writes THR of A (2:0) = 000b.

**3.** RDB reads IIR of A (2:0) = 010b.

For details of the read timing, refer to **(1) Read cycle timing (when ADSB is used)** and **(2) Read cycle timing (when ADSB is clamped low)**.

For details of the write timing, refer to **(3) Write cycle timing (when ADSB is used)** and **(4) Write cycle timing (when ADSB is clamped low)**.

### (9) Modem control timing




**Remarks 1.** INTRP indicates the modem status.
At this time, bit 3 (EDSSI) of IER is 1, and bits 1 to 3 of IIR are 000b.

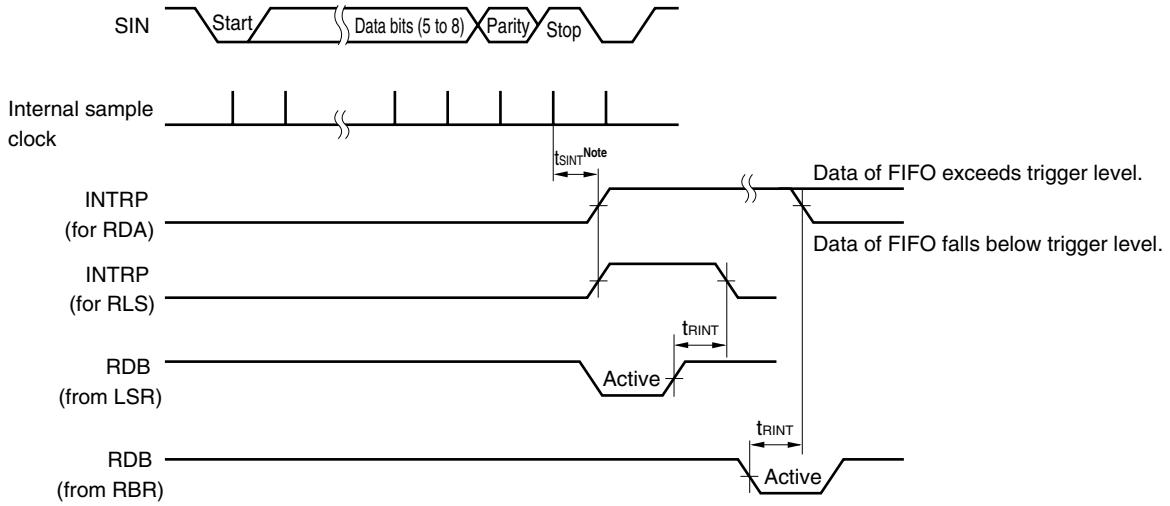
**2.** WRB writes MCR of A (2:0) = 100b.

**3.** RDB reads MSR of A (2:0) = 110b.

For details of the read timing, refer to **(1) Read cycle timing (when ADSB is used)** and **(2) Read cycle timing (when ADSB is clamped low)**.

For details of the write timing, refer to **(3) Write cycle timing (when ADSB is used)** and **(4) Write cycle timing (when ADSB is clamped low)**.

**(10) Timing of first byte of receive FIFO (when Data Ready is set)**

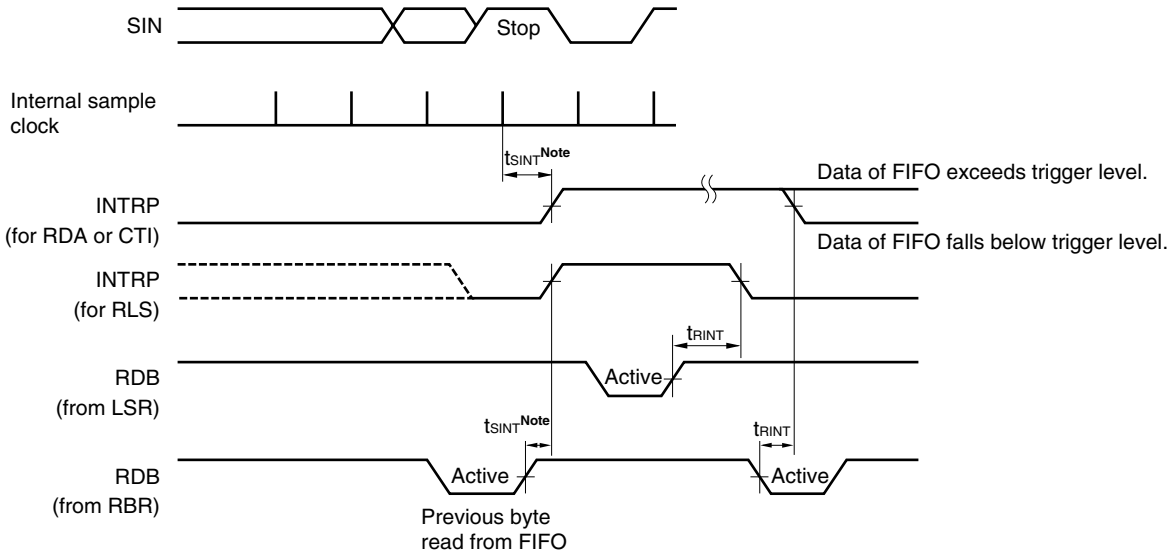



**Note** When FCR0 = 1, $t_{SINT}$ = 3RCLK. If a timeout interrupt occurs, $t_{SINT}$ = 8RCLK.

**Remarks 1.** INTRP (for RDA) indicates that the receive data has reached the trigger level of the FIFO.
At this time, bit 0 (ERBFI) of IER is 0, and bits 1 to 3 of IIR are 010b.
In the above figure, bits 6 and 7 of register FCR are cleared to 0.
INTRP is cleared depending on whether the receive data falls below the trigger level of the FIFO as a result of reading data.

**2.** INTRP (for RLS) indicates a receive line status.
At this time, bit 2 (ERLSI) of IER is 1, and bits 1 to 3 of IIR are 011b.

### (11) Timing of byte other than first byte of receive FIFO (when Data Ready is already set)

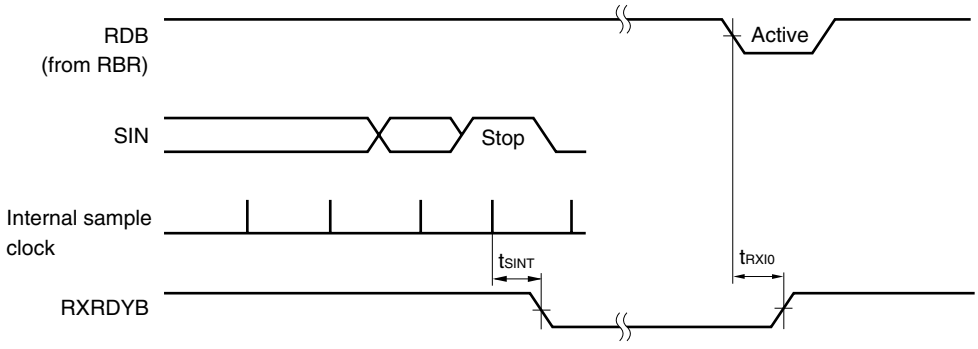



**Note** When FCR0 = 1, $t_{SINT}$ = 3RCLK. If a timeout interrupt occurs, $t_{SINT}$ = 8RCLK.

**Remarks 1.** INTRP (for RDA) occurs if the receive data exceeds the trigger level of the FIFO or if character time-out occurs.
At this time, bit 0 (ERBFI) of IER is 1, and bits 1 to 3 of IIR are 010b.
In the above figure, both bits 6 and 7 of register FCR are cleared to 0.
INTRP is cleared when the receive data falls below the trigger level of the FIFO as a result of reading data.

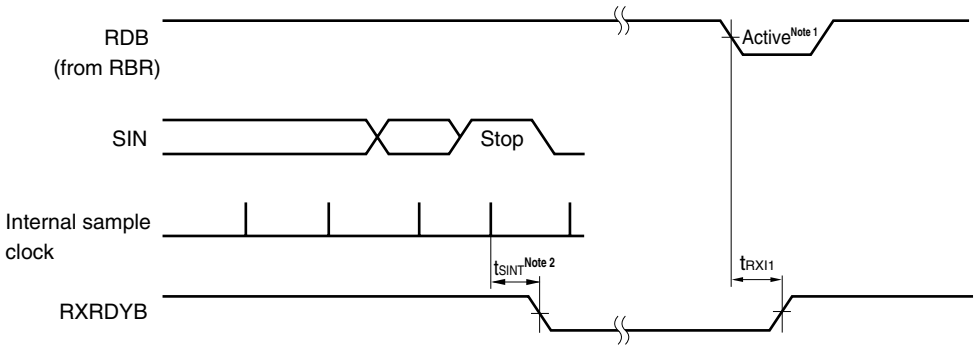
**2.** INTRP (for RLS) indicates a receive line status.
At this time, bit 2 (ERLSI) of IER is 1 and bits 1 to 3 of IIR are 011b.

### (12) Timing of reception READY in 16450 mode




**Remark** The input signal of SIN is the first byte.

### (13) Timing in reception READY FIFO mode (DMA mode = 0)

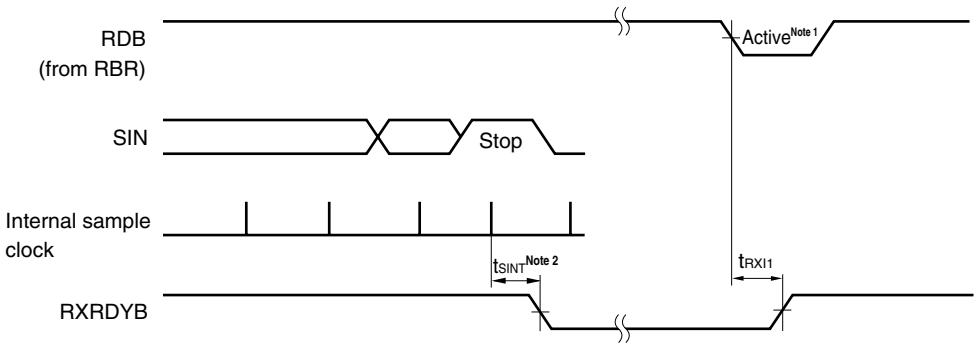



**Notes 1.** The last byte of the FIFO is read here.

**2.** When FCR0 = 1, $t_{SINT}$ = 3RCLK.

**Remark** The input signal of SIN is the first byte that reaches the trigger level of the receive FIFO.

### (14) Timing in reception READY FIFO mode (DMA mode = 1)

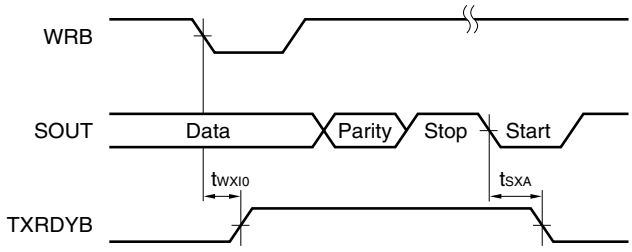



**Notes 1.** The last byte of the FIFO is read here.

**2.** When FCR0 = 1, $t_{SINT}$ = 3RCLK. When a timeout interrupt occurs, $t_{SINT}$ = 8RCLK.

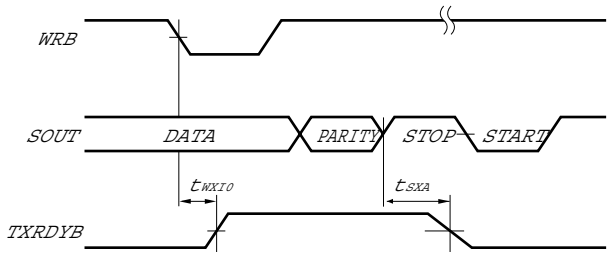
**Remark** The input signal of SIN is the first byte that reaches the trigger level of the receive FIFO.

### (15) Timing in transmission READY 16450 mode and FIFO mode (DMA mode = 0)



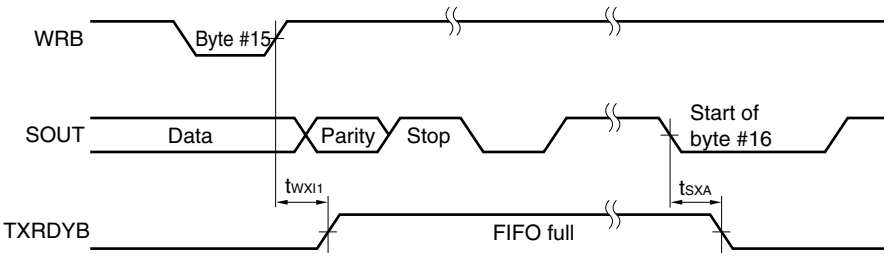

**Remark** WRB writes THR of A (2:0) = 000b.

<R> **(16) Timing in transmission READY FIFO mode (DMA mode = 0)**




**Remark** WRB writes THR of A (2:0) = 000b.

<R> **(17) Timing in transmission READY FIFO mode (DMA mode = 1)**

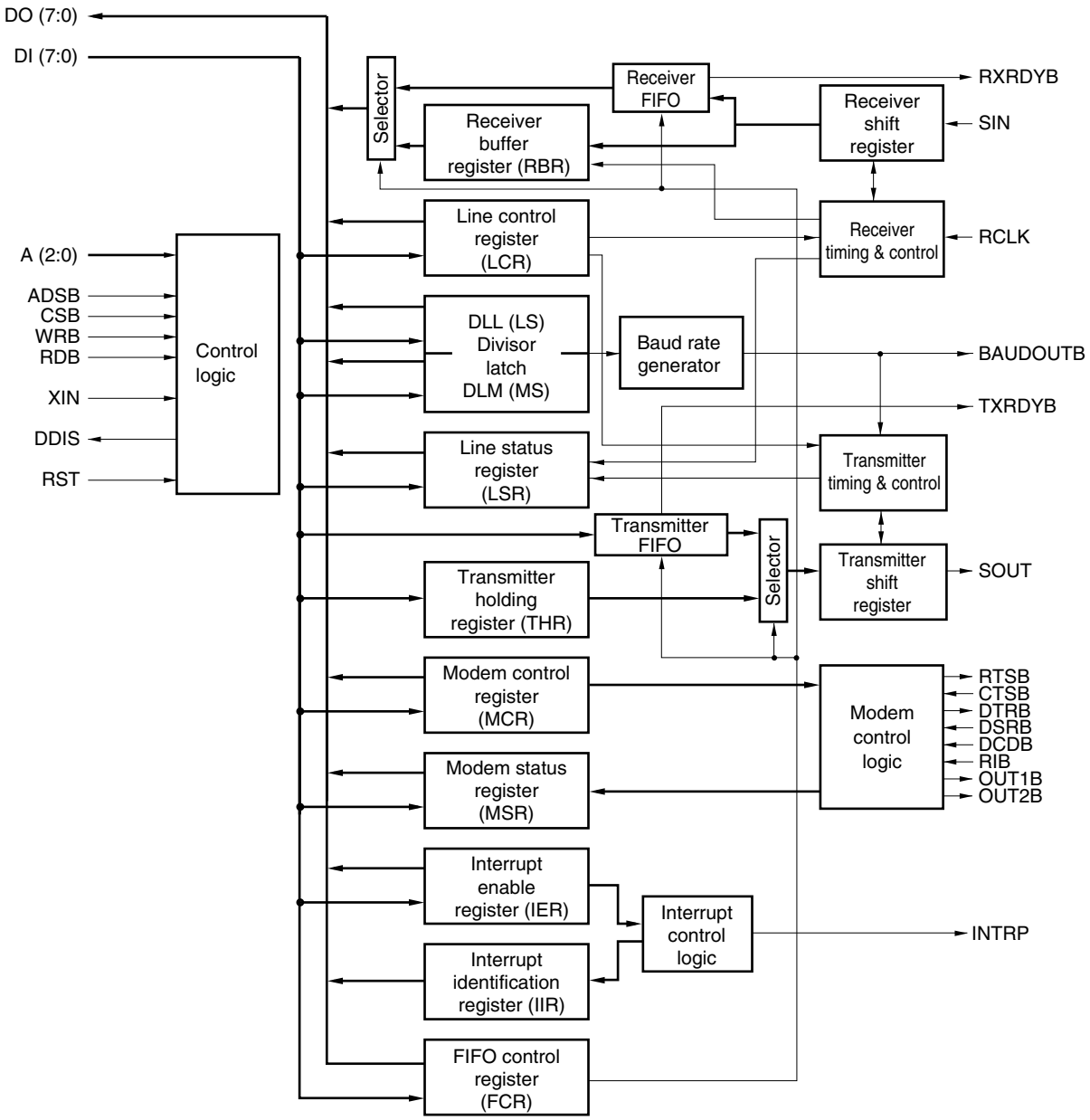



**Remark** WRB writes THR of A (2:0) = 000b.

## 5.7 Block Diagram

The block diagram of this macro is shown below. In this block diagram, the circuits related to testing are omitted.

**Figure 5-2. Block Diagram**



## 5.8 Register

### 5.8.1 Register List

**Table 5-4. Register List (1/2)**

| | | Register Address | | | | | |
|---|---|---|---|---|---|---|---|
| DLAB | | DLAB = 0 | DLAB = 0 | DLAB = 0 | DLAB = X | DLAB = X | DLAB = X |
| Address | | A = 0 | A = 0 | A = 1 | A = 2 | A = 2 | A = 3 |
| Register name | | Receiver buffer register (read only) | Transmitter holding register (write only) | Interrupt enable register | Interrupt ident. register (read only) | FIFO control register (write only) | Line control register |
| Register | | RBR | THR | IER | IIR | FCR | LCR |
| Bit No. | 0 | Data bit 0[Note 1] | Data bit 0[Note 1] | Enable received data available interrupt (ERBFI) | "0" if interrupt pending | FIFO enable | Word length select bit 0 (WLS0) |
| | 1 | Data bit 1 | Data bit 1 | Enable transmitter holding register empty interrupt (ETBEI) | Interrupt ID bit (0) | RCVR FIFO reset | Word length select bit 1 (WLS1) |
| | 2 | Data bit 2 | Data bit 2 | Enable receiver line status interrupt (ERLSI) | Interrupt ID bit (1) | XMIT FIFO reset | Number of stop bits (STB) |
| | 3 | Data bit 3 | Data bit 3 | Enable MODEM status interrupt (EDSSI) | Interrupt ID bit (2)[Note 2] | DMA mode select | Parity enable (PEN) |
| | 4 | Data bit 4 | Data bit 4 | 0 | 0 | Reserved | Even parity select (EPS) |
| | 5 | Data bit 5 | Data bit 5 | 0 | 0 | Reserved | Stick parity |
| | 6 | Data bit 6 | Data bit 6 | 0 | FIFOs enabled[Note 2] | RCVR trigger (LSB) | Set break |
| | 7 | Data bit 7 | Data bit 7 | 0 | FIFOs enabled[Note 2] | RCVR trigger (MSB) | Divisor latch access bit (DLAB) |

**Notes 1.** Data bit 0 is LSB; the first bit when serial data is transmitted/received.

**2.** Always set to 0 in 16450 mode.

**Remark** X: don't care.

**Table 5-4. Register List (2/2)**

| | | Register Address | | | | | |
|---|---|---|---|---|---|---|---|
| DLAB | | DLAB = X | DLAB = X | DLAB = X | DLAB = X | DLAB = 1 | DLAB = 1 |
| Address | | A = 4 | A = 5 | A = 6 | A = 7 | A = 0 | A = 1 |
| Register name | | MODEM control register | Line status register | MODEM status register | Scratch register | Divisor latch (LS) | Divisor latch (MS) |
| Register | | MCR | LSR | MSR | SCR | DLL | DLM |
| Bit No. | 0 | Data terminal ready (DTR) | Data ready (DR) | Delta clear to send (DCTS) | Bit 0 | Bit 0 | Bit 8 |
| | 1 | Request to send (RTS) | Overrun error (OE) | Delta data set ready (DDSR) | Bit 1 | Bit 1 | Bit 9 |
| | 2 | Out 1 | Parity error (PE) | Trailing edge ring indicator (TERI) | Bit 2 | Bit 2 | Bit 10 |
| | 3 | Out 2 | Framing error (FE) | Delta data carrier detect (DDCD) | Bit 3 | Bit 3 | Bit 11 |
| | 4 | Loop | Break interrupt (BI) | Clear to send (CTS) | Bit 4 | Bit 4 | Bit 12 |
| | 5 | 0 | Transmitter holding register (THRE) | Delta set ready (DSR) | Bit 5 | Bit 5 | Bit 13 |
| | 6 | 0 | Transmitter empty (TEMT) | Ring indicator (RI) | Bit 6 | Bit 6 | Bit 14 |
| | 7 | 0 | Error in PCVR FIFO[Note] | Data carrier detect (DCD) | Bit 7 | Bit 7 | Bit 15 |

**Note** Always set to 0 in 16450 mode.

**Remark** X: don't care.

### <R> 5.8.2 Register Description

The system programmer may access any of the UART registers summarized in Table 5-4 via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table 5-4 has its name and reset state shown.

**(1) Line Control Register**

The system programmer specifies the format of the asynchronous data communications exchange and set the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table 5-4 shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

| Bit 1 | Bit 0 | Character Length |
|---|---|---|
| 0 | 0 | 5 Bits |
| 0 | 1 | 6 Bits |
| 1 | 0 | 7 Bits |
| 1 | 1 | 8 Bits |

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

**Caution This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.**

**1. Load an all 0s, pad character, in response to THRE.**

**2. Set break after the next THRE.**

**3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.**

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

**(2) Programmable Baud Generator**

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 24 MHz and dividing it by any divisor from 2 to $2^{16}$-1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input) / (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table 5-5 provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 18.432 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

**Table 5-5. Baud Rates, Divisors and Crystals**

| Baud Rate | 1.8432 MHz Crystal | | 3.072 MHz Crystal | | 18.432 MHz Crystal | |
|---|---|---|---|---|---|---|
| | Decimal Divisor for 16 x Clock | Percent Error | Decimal Divisor for 16 x Clock | Percent Error | Decimal Divisor for 16 x Clock | Percent Error |
| 50 | 2304 | - | 3840 | - | 23040 | - |
| 75 | 1536 | - | 2560 | - | 15360 | - |
| 110 | 1047 | 0.026 | 1745 | 0.026 | 10473 | - |
| 134.5 | 857 | 0.058 | 1428 | 0.034 | 8565 | - |
| 150 | 768 | - | 1280 | - | 7680 | - |
| 300 | 384 | - | 640 | - | 3840 | - |
| 600 | 192 | - | 320 | - | 1920 | - |
| 1200 | 96 | - | 160 | - | 920 | - |
| 1800 | 64 | - | 107 | 0.312 | 640 | - |
| 2000 | 58 | 0.69 | 96 | - | 576 | - |
| 2400 | 48 | - | 80 | - | 480 | - |
| 3600 | 32 | - | 53 | 0.628 | 320 | - |
| 4800 | 24 | - | 40 | - | 240 | - |
| 7200 | 16 | - | 27 | 1.23 | 160 | - |
| 9600 | 12 | - | 20 | - | 120 | - |
| 19200 | 6 | - | 10 | - | 60 | - |
| 38400 | 3 | - | 5 | - | 30 | - |
| 56000 | 2 | 2.86 | - | - | 21 | 2.04 |
| 128000 | - | - | - | - | 9 | - |

**Caution For baud rates of 250k, 300k, 375k, 500k, 750k and 1.5M using a 24 MHz crystal causes minimal error.**

**(3) Line Status Register**

This register provides status information to the CPU concerning the data transfer. Table 5-4 shows the contents of the Line Status Register. Details on each bit follow.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a logic 0 bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this ''start'' bit twice and then takes in the ''data''.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

**Caution Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.**

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the 16450 Mode this is a 0. In the FIFO mode LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

**Caution The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing. In the FIFO mode the software must load a data byte in the Rx FIFO via Loopback Mode in order to write to LSR2-LSR4. LSR0 and LSR7 can't be written to in FIFO mode.**

**(4) FIFO Control Register**

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from the FIFO Mode to the 16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0=1 (see description of RXRDY and TXRDY pins).

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

| 7 | 6 | RCVR FIFO Trigger Level (Bytes) |
|---|---|---|
| 0 | 0 | 01 |
| 0 | 1 | 04 |
| 1 | 0 | 08 |
| 1 | 1 | 14 |

**(5) Interrupt Identification Register**

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table 5-4 shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 5-6.

Bit 3: In the 16450 Mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5: These two bits of the IIR are always logic 0.

Bits 6 and 7: These two bits are set when FCR0=1.

**Table 5-6. Interrupt Control Functions**

| FIFO Mode Only | Interrupt Identification Register | | | Interrupt Set and Reset Functions | | | |
|---|---|---|---|---|---|---|---|
| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Priority Level | Interrupt Type | Interrupt Source | Interrupt Reset Control |
| 0 | 0 | 0 | 1 | - | None | None | - |
| 0 | 1 | 1 | 0 | Highest | Receiver Line Status | Overrun Error or Parity Error or Framing Error or Break Interrupt | Reading the Line Status Register |
| 0 | 1 | 0 | 0 | Second | Received Data Available | Receiver Data Available or Trigger Level Reached | Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level |
| 1 | 1 | 0 | 0 | Second | Character Timeout Indication | No Characters Have Been Removed From or Input to the RCVR FIFO During the Last 4 Char. Times and There Is at Least 1 Char. in It During This Time | Reading the Receiver Buffer Register |
| 0 | 0 | 1 | 0 | Third | Transmitter Holding Register Empty | Transmitter Holding Register Empty | Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register |
| 0 | 0 | 0 | 0 | Fourth | MODEM Status | Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect | Reading the MODEM Status Register |

**(6) Interrupt Enable Register**

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTRP) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTRP output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table 5-4 shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

**(7) Modem Control Register**

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 5-4 and are described below.

Bit 0: This bit controls the Data Terminal Ready (DTRB) output. When bit 0 is set to a logic 1, the DTRB output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTRB output is forced to a logic 1.

**Caution The DTRB output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.**

Bit 1: This bit controls the Request to Send (RTSB) output. Bit 1 affects the RTSB output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 (OUT 1B) signal, which is an auxiliary user-designated output. Bit 2 affects the OUT 1B output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 (OUT 2B) signal, which is an auxiliary user-designated output. Bit 3 affects the OUT 2B output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is ''looped back'' into the Receiver Shift Register input; the four MODEM Control inputs (DSRB, CTSB, RIB, and DCDB) are disconnected; and the four MODEM Control outputs (DTRB, RTSB, OUT 1B, and OUT 2B) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the loopback mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and received-data paths of the UART.

In the loopback mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

**(8) Modem Status Register**

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register. The contents of the MODEM Status Register are indicated in Table 5-4 and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTSB input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the DSRB input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RIB input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCDB input to the chip has changed state.

**Caution Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.**

Bit 4: This bit is the complement of the Clear to Send (CTSB) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready (DSRB) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator (RIB) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect (DCDB) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

**(9) Scratchpad Register**

This 8-bit Read/Write Register does not control the UART in anyway. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

**(10) FIFO Interrupt Mode Operation**

When the RCVR FIFO and receiver interrupts are enabled (FCR0=1, IER0=1) RCVR interrupts will occur as follows:

(a) The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

(b) The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

(c) The receiver line status interrupt (IIR=06), as before, has higher priority than the received data available (IIR=04) interrupt.

(d) The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

(a) A FIFO timeout interrupt will occur, if the following conditions exist:

- at least one character is in the FIFO
- the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

The maximum time between a received character and a timeout interrupt will be 160 ms at 300 baud with a 12-bit receive character (i.e., 1 Start, 8 Data, 1 Parity and 2 Stop Bits).

(b) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

(c) When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

(d) When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0=1, IER1=1), XMIT interrupts will occur as follows:

(a) The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

(b) The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE=1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

**(11) FIFO Polled Mode Operation**

With FCR0=1 resetting IER0, IER1, IER2, IER3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR0 will be set as long as there is one byte in the RCVR FIFO.

LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2=0.

LSR5 will indicate when the XMIT FIFO is empty.

LSR6 will indicate that both the XMIT FIFO and shift register are empty.

LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

## <R> 5.9 Typical Applications

**Figure 5-3. Typical Interface for High-Capacity Data Bus**

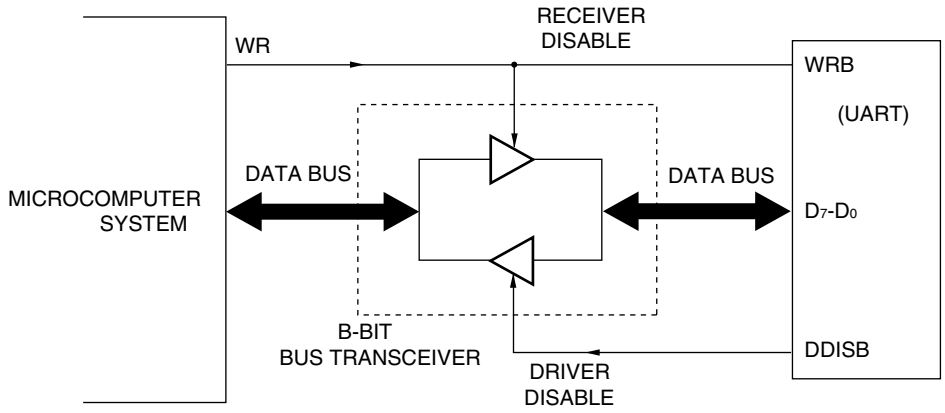
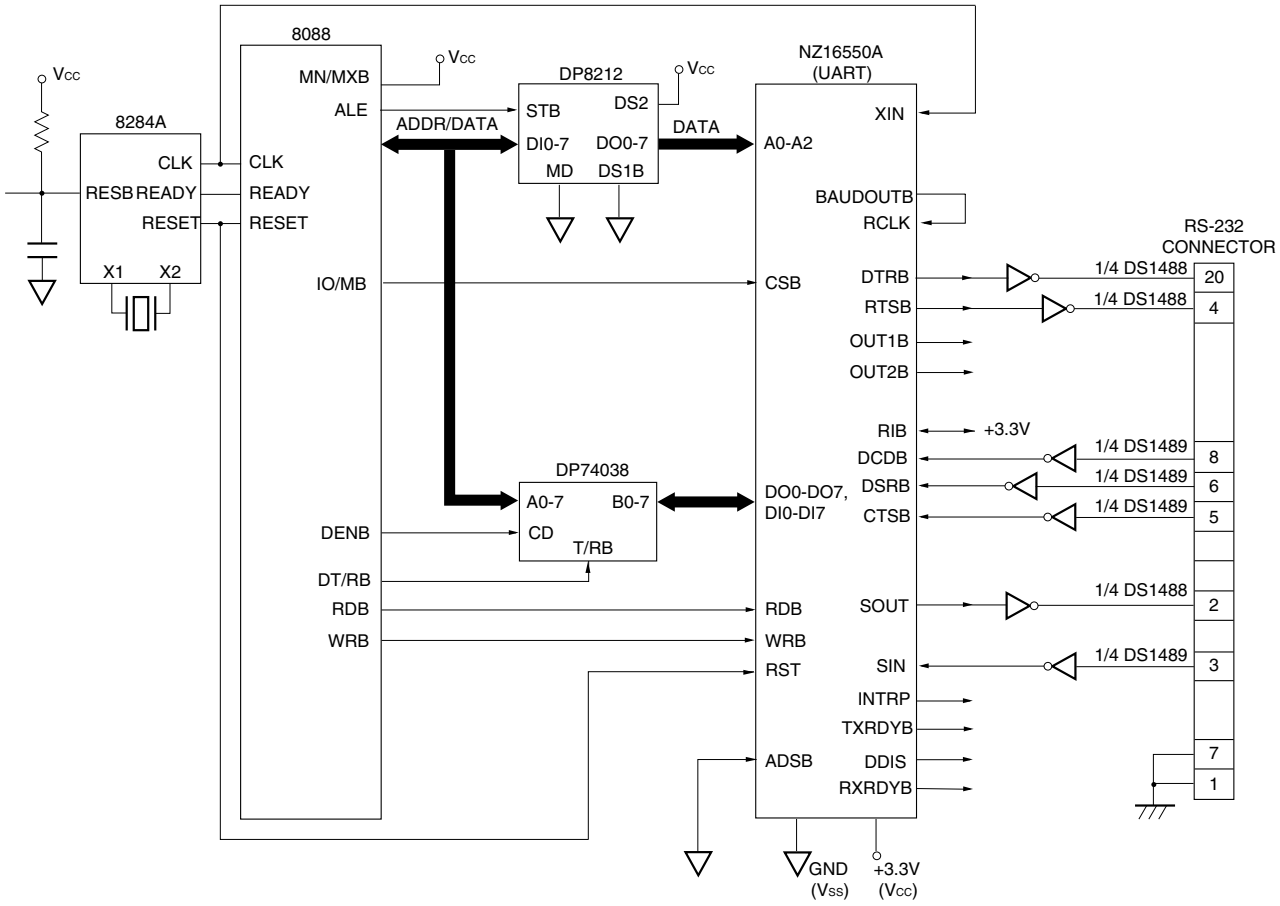



**Figure 5-4. Basic Connections of NZ16550A to 8088 CPU**




**Caution Test pins are omitted.**

# APPENDIX A TEST SPECIFICATIONS

## A.1 Mega Macro Test Specification

1. Part number μPD65 _ _ _ - _ _ _

2. Date of preparation 20 _ _ / _ _ / _ _
   Name of company of person in charge of preparation_____
   Telephone number of above person _____

3. Mega macro used
   NA51A × ___ pcs
   NA54A × ___ pcs
   NA59A × ___ pcs
   NZ16550A × ___ pcs Total ___ pcs

4. Number of pins

   | | |
   |---|---|
   | Number of input pins | ___ |
   | Number of output pins | ___ |
   | Number of bidirectional pins | ___ |
   | Total number of pins | ___ |

5. Number of patterns

   | | | |
   |---|---|---|
   | Number of user patterns | | = ___ patterns |
   | NA51A (12874 patterns) | × ___ pcs | = ___ patterns |
   | NA54A (3483 patterns) | × ___ pcs | = ___ patterns |
   | NA59A (7335 patterns) | × ___ pcs | = ___ patterns |
   | NZ16550A (14889 patterns) | × ___ pcs | = ___ patterns |
   | Total | | ___ patterns |

Fill out the “Pin reference table” on the following pages of each mega macro used and attach it to this specification.

## A.2 NA51A Pin Reference Table

Instance name _____ (1/ )

| Mega Macro Test Input | | Mega Macro Test Output | |
|---|---|---|---|
| Mega Macro Pin Name | External Pin Name | Mega Macro Pin Name | External Pin Name |
| TBI0 | | DO0 | |
| TBI1 | | DO1 | |
| TBI2 | | DO2 | |
| TBI3 | | DO3 | |
| TBI4 | | DO4 | |
| TBI5 | | DO5 | |
| TBI6 | | DO6 | |
| TBI7 | | DO7 | |
| TBI8 | | OSYN | |
| TBI9 | | TXD | |
| TBI10 | | TXRDY | |
| TBI11 | | TXEMP | |
| TBI12 | | RXRDY | |
| TBI13 | | DTRB | |
| TBI14 | | RTSB | |
| TBI15 | | CDB | |
| TBI16 | | CSYN | |
| TBI17 | | Test Mode Setting Input | |
| TBI18 | | External Pin Name | Input Value |
| TBI19 | | | |
| TESTB[Note 1] | | | |
| CSD[Note 2] | | | |
| CSE[Note 2] | | | |
| TTHR | | | |

**Notes 1.** "TESTB" can be replaced by the test mode setting input.

**2.** "CSD" and "CSE" can be fixed by clamping. However, write the input value.

**Remark** When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

## A.3 NA54A Pin Reference Table

Instance name _____ (1/ )

| Mega Macro Test Input | | Mega Macro Test Output | |
|---|---|---|---|
| Mega Macro Pin Name | External Pin Name | Mega Macro Pin Name | External Pin Name |
| TBI0 | | DO0 | |
| TBI1 | | DO1 | |
| TBI2 | | DO2 | |
| TBI3 | | DO3 | |
| TBI4 | | DO4 | |
| TBI5 | | DO5 | |
| TBI6 | | DO6 | |
| TBI7 | | DO7 | |
| TBI8 | | CNTOUT0 | |
| TBI9 | | CNTOUT1 | |
| TBI10 | | CNTOUT2 | |
| TBI11 | | CDB | |
| TBI12 | | Test Mode Setting Input | |
| TBI13 | | External Pin Name | Input Value |
| TBI14 | | | |
| TBI15 | | | |
| TBI16 | | | |
| TBI17 | | | |
| TBI18 | | | |
| TESTB[Note 1] | | | |
| CSD[Note 2] | | | |
| CSE[Note 2] | | | |
| TTHR | | | |

**Notes 1.** "TESTB" can be replaced by the test mode setting input.

**2.** "CSD" and "CSE" can be fixed by clamp. However, write the input value.

**Remark** When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

## A.4 NA59A Pin Reference Table

Instance name _____ (1/ )

| Mega Macro Test Input | | Mega Macro Test Output | |
|---|---|---|---|
| Mega Macro Pin Name | External Pin Name | Mega Macro Pin Name | External Pin Name |
| TBI0 | | DO0 | |
| TBI1 | | DO1 | |
| TBI2 | | DO2 | |
| TBI3 | | DO3 | |
| TBI4 | | DO4 | |
| TBI5 | | DO5 | |
| TBI6 | | DO6 | |
| TBI7 | | DO7 | |
| TBI8 | | SAO0 | |
| TBI9 | | SAO1 | |
| TBI10 | | SAO2 | |
| TBI11 | | SVO | |
| TBI12 | | INTR | |
| TBI13 | | CDB | |
| TBI14 | | CSA | |
| TBI15 | | CSV | |
| TBI16 | | ESLC0 | |
| TBI17 | | ESLC1 | |
| TBI18 | | ESLC2 | |
| TBI19 | | ESLC3 | |
| TBI20 | | ESLC4 | |
| TBI21 | | ESLC5 | |
| TBI22 | | ESLC6 | |
| TBI23 | | ESLC7 | |
| TBI24 | | INTO0 | |
| TBI25 | | INTO1 | |
| TBI26 | | INTO2 | |
| TBI27 | | INTO3 | |
| TBI28 | | INTO4 | |
| TBI29 | | INTO5 | |
| TBI30 | | INTO6 | |
| TBI31 | | INTO7 | |
| TBI32 | | Test Mode Setting Input | |
| TBI33 | | External Pin Name | Input Value |
| TESTB[Note 1] | | | |
| RST | | | |
| CSD[Note 2] | | | |
| CSE[Note 2] | | | |
| TTHR | | | |

**Notes 1.** “TESTB” can be replaced by the test mode setting input.
**2.** “CSD” and “CSE” can be fixed by clamp. However, write the input value.

**Remark** When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

## A.5 NZ16550A Pin Reference Table

Instance name _____ (1/ )

| Mega Macro Test Input | | Mega Macro Test Output | |
|---|---|---|---|
| Mega Macro Pin Name | External Pin Name | Mega Macro Pin Name | External Pin Name |
| TBI0 | | DO0 | |
| TBI1 | | DO1 | |
| TBI2 | | DO2 | |
| TBI3 | | DO3 | |
| TBI4 | | DO4 | |
| TBI5 | | DO5 | |
| TBI6 | | DO6 | |
| TBI7 | | DO7 | |
| TBI8 | | SD | |
| TBI9 | | CSOUT | |
| TBI10 | | DDIS | |
| TBI11 | | INTRP | |
| TBI12 | | BAUDOUTB | |
| TBI13 | | DTRB | |
| TBI14 | | OUT1B | |
| TBI15 | | OUT2B | |
| TBI16 | | RTSB | |
| TBI17 | | SOUT | |
| TBI18 | | TXRDYB | |
| TBI19 | | RXRDYB | |
| TBI20 | | Test Mode Setting Input | |
| TBI21 | | External Pin Name | Input Value |
| TBI22 | | | |
| TBI23 | | | |
| TBI24 | | | |
| TBI25 | | | |
| TBI26 | | | |
| TBI27 | | | |
| TBI28 | | | |
| TESTB[Note 1] | | | |
| CSD[Note 2] | | | |
| CSE[Note 2] | | | |
| TTHR | | | |

**Notes 1.** “TESTB” can be replaced by the test mode setting input.
**2.** “CSD” and “CSE” can be fixed by clamp. However, write the input value.

**Remark** When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

**[MEMO]**

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