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カタログ等資料中の旧社名の扱いについて

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ルネサスエレクトロニクス ホームページ（http://www.renesas.com）

2010年4月1日
ルネサスエレクトロニクス株式会社

【発行】ルネサスエレクトロニクス株式会社（http://www.renesas.com）

【問い合わせ先】http://japan.renesas.com/inquiry

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   高品質水準： 輸送機器（自動車、電車、船舶等）、交通用信号機器、防災・防犯装置、各種安全装置、生命維持を目的として設計されていない医療機器（厚生労働省定義の管理医療機器に相当）

   特定水準： 航空機器、航空宇宙機器、海底中継機器、原子力制御システム、生命維持のための医療機器（生命維持装置、人体に埋め込み使用するもの、治療行為（患部切り出し等）を行うもの、その他直接人命に影響を与えるもの）（厚生労働省定義の高度管理医療機器に相当）またはシステム等
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RENESAS

Block Library

CMOS-9HD Family, EA-9HD Family

CMOS Gate Array, CMOS Embedded Array

Memory Ver.4.0

Document No. A13071JJ4V0BL00 (4th edition)
Date Published October 2000 N CP(K)

[MEMO]

Summary of Contents

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  標準水準：コンピュータ，OA機器，通信機器，計測機器，AV機器，家電，工作機械，パーソナル機器，産業用ロボット

  特別水準：輸送機器（自動車，列車，船舶等），交通用信号機器，防災／防犯装置，各種安全装置，生命維持を直接の目的としない医療機器

  特定水準：航空機器，航空宇宙機器，海底中継機器，原子力制御システム，生命維持のための医療機器，生命維持のための装置またはシステム等

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M7　98.8

本版で改訂された主な箇所

箇 所	内　　容
全般	EA-9HD ファミリを追加
p.185	CHAPTER 3　ROM BLOCK を追加
旧版 p.223	旧版 APPENDIX B　BLOCK LIST（by Function）を削除

本文欄外の★印は，本版で改訂された主な箇所を示しています。

巻末にアンケート・コーナを設けております。このドキュメントに対するご意見をお気軽にお寄せください。

[MEMO]

はじめに

1．構成

このマニュアルは，CMOS-9HDファミリ，EA-9HDファミリ用メモリ・ブロック・ライブラリについて記載しています。

回路設計を行う際は必ず先に**CMOS-9HDファミリ　設計マニュアル（A12985J）, EA-9HDファミリ　設計マニュアル（A13282J）**を読んでください。

また，マニュアルに記載された事項（一般事項，注意事項，制限事項）は必ずお守りください。お守りいただけない場合，LSI製品の品質や性能の低下，および動作の異常が生じることがあります。

このマニュアルは, 次のような構成になっています。

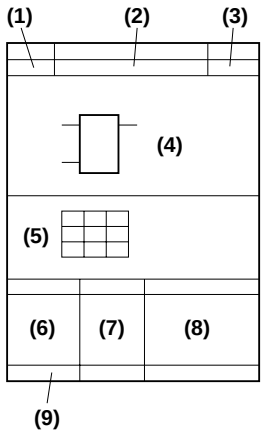
(1) はじめに
　このマニュアルを活用されるにあたっての注意事項，用語，定義などを説明しています。

(2) CONTENTS
　目次をインタフェース／ファンクション・ブロックのアルファベット順リストとして作成してあります。ブロック名から探すときなどに利用してください。

(3)　CHAPTER1　　HIGH DENSITY SINGLE-PORT RAM BLOCK (Soft Macro)
(4)　CHAPTER2　　HIGH DENSITY DUAL-PORT RAM BLOCK (Soft Macro)
(5)　CHAPTER3　　ROM BLOCK
(6)　APPENDIX A　BASIC RAM BLOCK
　CHAPTER 1～3とAPPENDIXは, それぞれのブロックについて，アルファベット順に並べてあります。各ページには, 論理シンボル，真理値表，入出力データ，スイッチング・スピード（伝達遅延時間）などを記載してあります。

なお，CMOS-9HDファミリ，EA-9HDファミリの高密度RAMブロックはソフト・マクロ構成となっています。６種類のハード・マクロを基にビット，ワードを構成し，テスト回路（BIST），セレクタを内蔵するソフト・マクロです。そのため，このマニュアルでは，ベーシックRAMブロック（ハード・マクロ）と高密度RAMブロック（ソフト・マクロ）を記載しています。またメモリ・ブロックを使用する場合，使用セル数と各マスタごとの使用可能セル数により搭載不可能な場合があります。回路設計を行う際は，必ず先に**CMOS-9HDファミリ　設計マニュアル（A12985J）, EA-9HDファミリ　設計マニュアル（A13282J）**をお読みください。

2. ブロック・ライブラリ記載内容の説明



(1) Block Type : 機能ブロックの名称
(2) Function : そのブロックの機能名
(3) SSI Family : 同じ機能を持つ74(LS)シリーズ名
(4) Logic Diagram : そのブロックの論理シンボル（論理図）
(5) Truth Table : そのブロックの真理値表
(6) Input : 入力端子の端子名，ファンイン
(7) Output : 出力端子の端子名，ファンアウト
(8) Switching speed: そのブロックの伝達遅延時間など
(9) Equivalent Cells: 使用セル数

なお，スイッチング・スピードの記号は以下のとおりです。

A → Y (H L)
↑ ↑↑
(10) (11)(12)

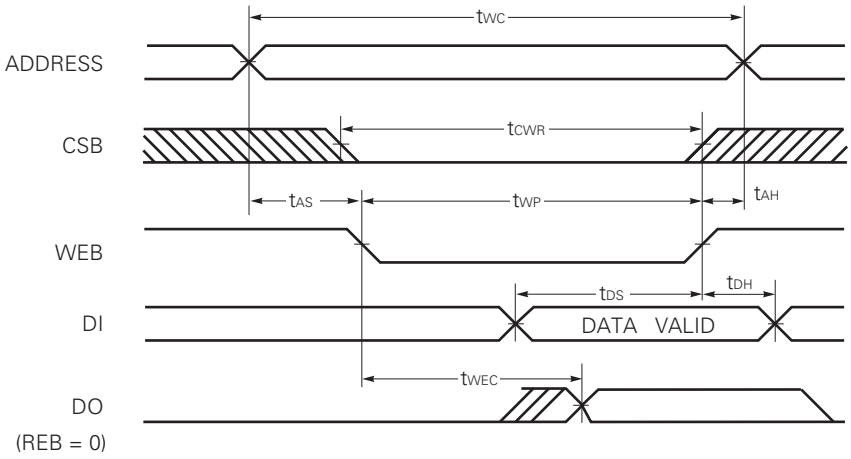
(10) 信号のパス名（入力→出力）
(11) 入力信号の状態（H：ハイ・レベル，L：ロウ・レベル，Z：ハイ・インピーダンス）
(12) 出力信号の状態（H：ハイ・レベル，L：ロウ・レベル，Z：ハイ・インピーダンス）

3. メモリ・タイミング

斜線の部分はアドレスまたはCSBが変化するとき，内部回路で一時的にハイ・インピーダンス状態になります。そのため出力がこの間不定になります。

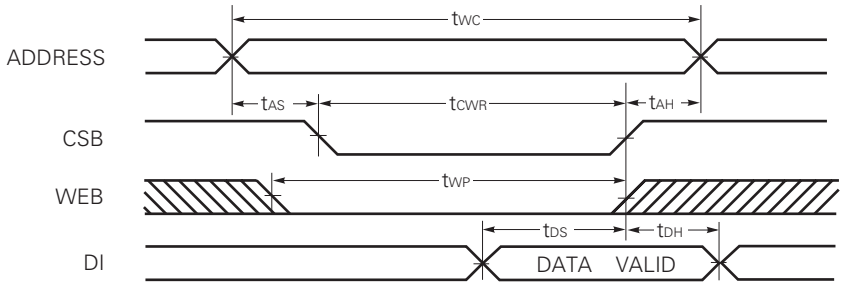
3.1 高密度RAM（シングルポート）

(1) ライト・サイクル・タイミング 1（WEB コントロール・モード）



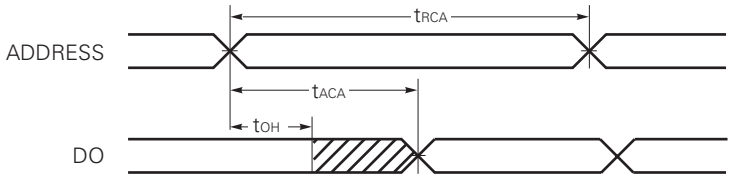
注意　WEBまたはCSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。
また，DOにDATA VALIDが出力される時間は，WEBの立ち下がりからtWEC経過した時間と，DIの変化からDOが変化するまでの時間のどちらか遅い方で決まります。

(2) ライト・サイクル・タイミング 2（CSB コントロール・モード）



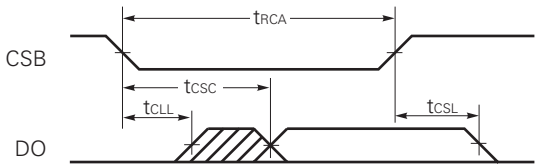
注意　WEBまたはCSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。

(3) リード・サイクル・タイミング 1（CSB=0，REB=0，WEB=1）



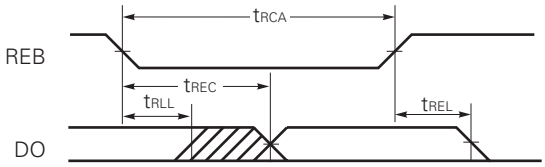
tACA ：アドレスが決定後，出力が確定するまでの時間。
tOH ：任意のアドレスが変化したとき，変化する前のデータが保持されている時間

(4) リード・サイクル・タイミング 2（REB=0，WEB=1）



注意　ADDRESS信号は，CSB信号のロウ・レベル伝達と同時に，あるいはそれ以前に確定しなければなりません。

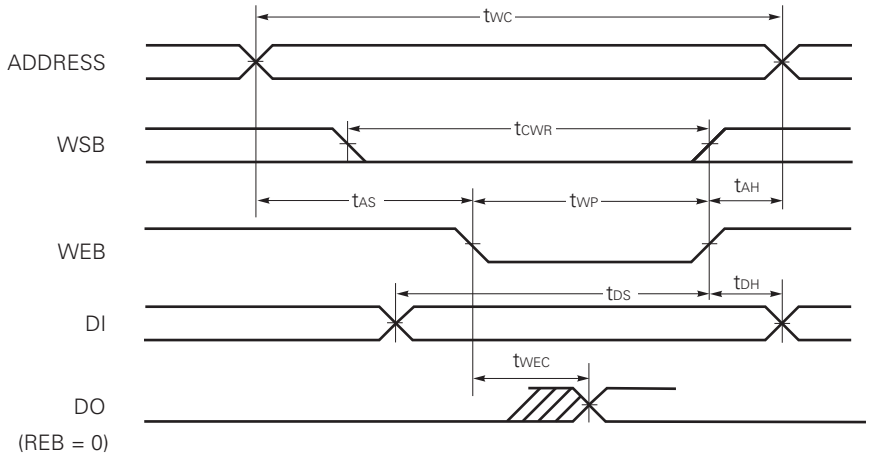
(5) リード・サイクル・タイミング 3（CSB=0，WEB=1）



注意　ADDRESS信号は，REB信号のロウ・レベル伝達と同時に，あるいはそれ以前に確定しなければなりません。

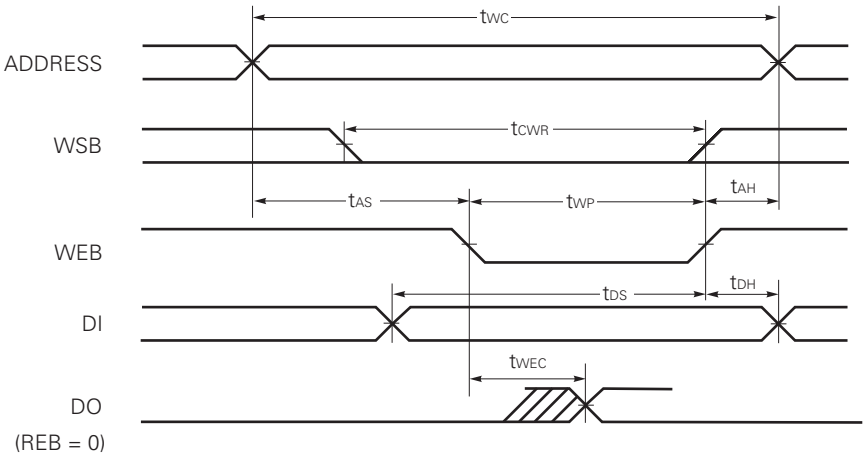
3.2　高密度RAM（デュアルポート）

(1) ライト・サイクル・タイミング 1（WEBコントロール・モード）



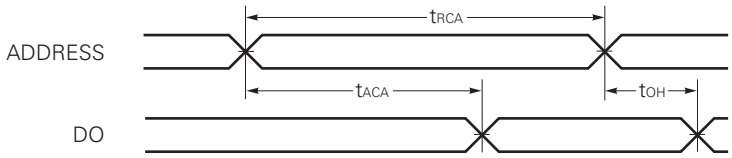
注意　WEBまたはWSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。また，READアドレス，WRITEアドレスが同一アドレスの場合，DOにDIが出力される時間は，WEBの立ち下がりからtWEC経過した時間と，DIの変化からDOが変化するまでの時間のどちらか遅い方で決まります。

(2) ライト・サイクル・タイミング 2（WSBコントロール・モード）

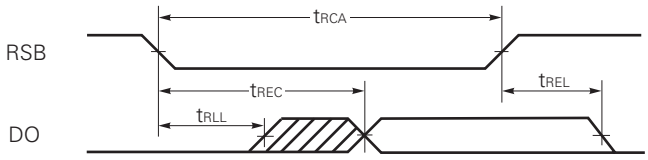


注意　WEBまたはWSBはADDRESS信号が変化する間はハイ・レベルでなければなりません。また，READアドレス，WRITEアドレスが同一アドレスの場合，DOにDIが出力される時間は，WEBの立ち下がりからtWEC経過した時間と，DIの変化からDOが変化するまでの時間のどちらか遅い方で決まります。

(3) リード・サイクル・タイミング 1（RSB=0）



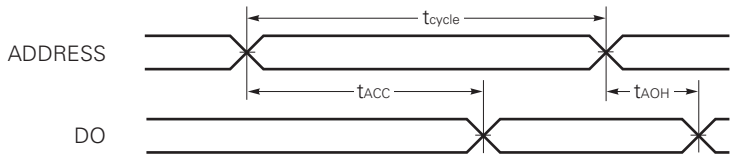
(4) リード・サイクル・タイミング 2



注意　ADDRESS信号は，RSB信号のロウ・レベル伝達と同時に，あるいはそれ以前に確定していなければなりません。

3.3　ROM

リード・サイクル・タイミング



4. BIST(Built in Self Test)

BISTとはRAM用テスト回路のことです。テスト･アドレス発生器，テスト・データ発生器，テスト・イネーブル発生器，期待値発生器，比較器から構成されています。テスト用端子としてTEB,TIN,TOUTの３本を外部端子に接続するだけでRAMのテストが行えます。また複数のRAMを搭載した場合にも，簡単にテストすることができます。それぞれのBISTの回路構成など詳細については，NECまでお問い合わせください。

関連資料

関連資料は暫定版の場合がありますが，この資料では「暫定」の表示をしておりません。あらかじめ，ご了承ください。

●CMOS-9HDファミリ，EA-9HDファミリ共通

- CMOS-9HD Family, EA-9HD Family Block Library　：A13052J
- CMOS-9HD Family, EA-9HD Family Memory Block Library　：このマニュアル
- テスト容易化設計　ユーザーズ・マニュアル　：A14357J

●CMOS-9HDファミリ

- CMOS-9HDファミリ　設計マニュアル　：A12985J
- CMOS-9HDファミリ　設計マニュアル　メガマクロ編　：A13941J

●EA-9HDファミリ

- EA-9HDファミリ　設計マニュアル　：A13282J
- EA-9HDファミリ　設計マニュアル　メモリ・マクロ編　：A13367J

設計する際は最新の資料を使用していただくため，NEC販売担当または特約店にご確認ください。

CONTENTS

SINGLE-PORT HIGH DENSITY RAM

Block Type	Function	Basic RAM	Test Block	Equivalent Cells	Page
RBEB	64 words × 20 bits Single-port RAM	K1AB	RUEB	5286	62
RBED	128 words × 20 bits Single-port RAM	K1AB	RUED	10220	64
RBEF	256 words × 20 bits Single-port RAM	K1AF	RUEF	15104	66
RBEH	512 words × 20 bits Single-port RAM	K1AF	RUEH	29778	68
RBEM	1 K words × 20 bits Single-port RAM	K1AM	RUEM	54541	70
RBH7	16 words × 32 bits Single-port RAM	K147	RUH7	3933	72
RBH9	32 words × 32 bits Single-port RAM	K149	RUH9	5694	74
RBHB	64 words × 32 bits Single-port RAM	K18B	RUHB	8411	76
RBHD	128 words × 32 bits Single-port RAM	K14D	RUHD	14311	78
RBHF	256 words × 32 bits Single-port RAM	K18F	RUHF	24189	80
RBHH	512 words × 32 bits Single-port RAM	K18F	RUHH	47955	82
RBKB	64 words × 40 bits Single-port RAM	K1AB	RUKB	10349	84
RBKD	128 words × 40 bits Single-port RAM	K1AB	RUKD	20195	86
RBKF	256 words × 40 bits Single-port RAM	K1AF	RUKF	29884	88
RBKH	512 words × 40 bits Single-port RAM	K1AF	RUKH	49856	90

DUAL-PORT HIGH DENSITY RAM

Block Type	Function	Basic RAM	Test Block	Equivalent Cells	Page
R947	16 words × 4 bits Dual-port RAM	K247	RU47	883	94
R949	32 words × 4 bits Dual-port RAM	K249	RU49	1427	96
R94B	64 words × 4 bits Dual-port RAM	K249	RU4B	2636	98
R94D	128 words × 4 bits Dual-port RAM	K24D	RU4D	4052	100
R94F	256 words × 4 bits Dual-port RAM	K24D	RU4F	7837	102
R94H	512 words × 4 bits Dual-port RAM	K24D	RU4H	15343	104
R94M	1 K words × 4 bits Dual-port RAM	K24D	RU4M	30396	106
R94S	2 K words × 4 bits Dual-port RAM	K24D	RU4S	60537	108
R94U	4 K words × 4 bits Dual-port RAM	K24D	RU4U	120704	110
R987	16 words × 8 bits Dual-port RAM	K247	RU87	1554	112
R989	32 words × 8 bits Dual-port RAM	K249	RU89	2632	114
R98B	64 words × 8 bits Dual-port RAM	K28B	RU8B	3446	116
R98D	128 words × 8 bits Dual-port RAM	K24D	RU8D	6613	118
R98F	256 words × 8 bits Dual-port RAM	K28F	RU8F	10369	120
R98H	512 words × 8 bits Dual-port RAM	K28F	RU8H	20418	122
R98M	1 K words × 8 bits Dual-port RAM	K28M	RU8M	37239	124
R98S	2 K words × 8 bits Dual-port RAM	K28M	RU8S	74136	126
R9AB	64 words × 10 bits Dual-port RAM	K2AB	RUAB	4187	128
R9AD	128 words × 10 bits Dual-port RAM	K2AB	RUAD	8079	130
R9AF	256 words × 10 bits Dual-port RAM	K2AF	RUAF	12791	132
R9AH	512 words × 10 bits Dual-port RAM	K2AF	RUAH	25244	134
R9AM	1 K words × 10 bits Dual-port RAM	K2AM	RUAM	46281	136
R9AS	2 K words × 10 bits Dual-port RAM	K2AM	RUAS	92206	138
R9C7	16 words × 16 bits Dual-port RAM	K247	RUC7	2902	140
R9C9	32 words × 16 bits Dual-port RAM	K249	RUC9	5036	142
R9CB	64 words × 16 bits Dual-port RAM	K28B	RUCB	6635	144
R9CD	128 words × 16 bits Dual-port RAM	K24D	RUCD	12939	146
R9CF	256 words × 16 bits Dual-port RAM	K28F	RUCF	20439	148
R9CH	512 words × 16 bits Dual-port RAM	K28F	RUCH	40489	150
R9CM	1 K words × 16 bits Dual-port RAM	K28M	RUCM	74160	152
R9EB	64 words × 20 bits Dual-port RAM	K2AB	RUEB	8125	154
R9ED	128 words × 20 bits Dual-port RAM	K2AB	RUED	15878	156
R9EF	256 words × 20 bits Dual-port RAM	K2AF	RUEF	25290	158
R9EH	512 words × 20 bits Dual-port RAM	K2AF	RUEH	50129	160
R9EM	1 K words × 20 bits Dual-port RAM	K2AM	RUEM	92244	162
R9H7	16 words × 32 bits Dual-port RAM	K247	RUH7	5606	164
R9H9	32 words × 32 bits Dual-port RAM	K249	RUH9	9852	166
R9HB	64 words × 32 bits Dual-port RAM	K28B	RUHB	13026	168
R9HD	128 words × 32 bits Dual-port RAM	K24D	RUHD	25605	170
R9HF	256 words × 32 bits Dual-port RAM	K28F	RUHF	40559	172
R9HH	512 words × 32 bits Dual-port RAM	K28F	RUHH	80657	174
R9KB	64 words × 40 bits Dual-port RAM	K2AB	RUHB	15994	176
R9KD	128 words × 40 bits Dual-port RAM	K2AB	RUKD	31469	178
R9KF	256 words × 40 bits Dual-port RAM	K2AF	RUKF	50227	180
R9KH	512 words × 40 bits Dual-port RAM	K2AF	RUKH	99937	182

ROM BLOCK

SINGLE-PORT BASIC RAM

DUAL-PORT BASIC RAM

[MEMO]

CHAPTER 1

HIGH DENSITY

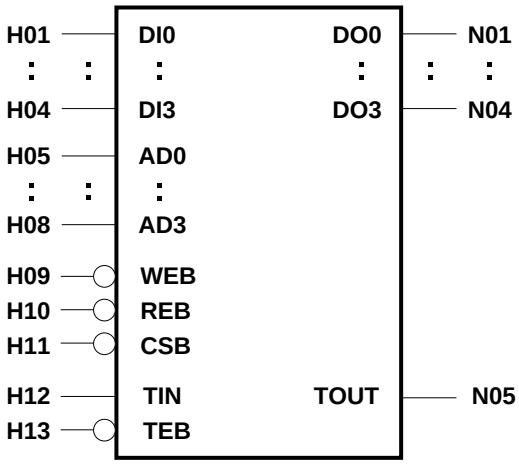
SINGLE-PORT RAM BLOCK

(Soft Macro)

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB47	**16 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	23.7
H05	AD0	2.4	N05	TOUT	26.0
:	:	:			
H08	AD3	2.4			
H09	WEB	2.4			
H10	REB	1.0			
H11	CSB	1.0			
H12	TIN	2.4			
H13	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD3	(LH)	2.25	3.73	6.13
→DO0 to DO3	(HH)	2.25	3.72	6.11
	(HL)	1.98	3.62	6.28
	(LL)	1.98	3.62	6.30
CSB	(LL)	1.99	3.44	5.80
→DO0 to DO3	(LH)	1.99	3.44	5.80
	(HL)	0.69	1.09	1.75
REB	(LH)	0.73	1.25	2.09
→DO0 to DO3	(HL)	0.78	1.22	1.94
DI0 to DI3	(HH)	1.85	3.20	5.40
→DO0 to DO3	(LL)	1.71	2.70	4.30

Equivalent Cells	655	Power (mW/MHz)		Rev.	1

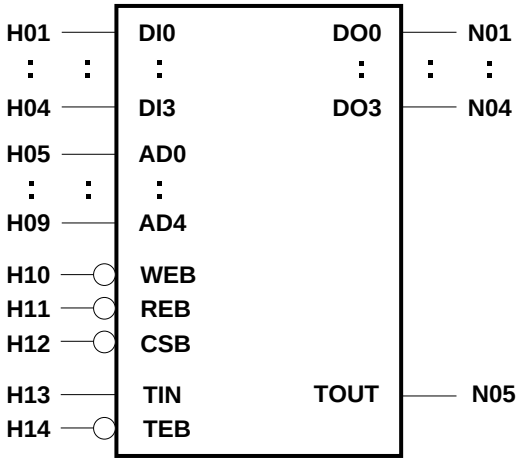
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.30**		
Address access time	**t_{ACA}**			**6.30**
Address output hold time	**t_{OH}**	**1.98**		
CSB access time	**t_{CSC}**			**5.80**
CSB output hold time	**t_{CSL}**	**0.93**		**2.60**
CSB output set time	**t_{CLL}**	**1.99**		
REB access time	**t_{REC}**			**2.10**
REB output hold time	**t_{REL}**	**0.78**		**1.94**
REB output set time	**t_{RLL}**	**0.74**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.37**		
CSB-WEB reset time	**t_{CWR}**	**4.03**		
Write pulse width	**t_{WP}**	**4.03**		
Address setup time	**t_{AS}**	**1.01**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**3.34**		
Input data hold time	**t_{DH}**	**0.42**		
WEB access time	**t_{WEC}**			**5.45**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB49	**32 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	23.7
H05	AD0	2.4	N05	TOUT	26.0
:	:	:			
H09	AD4	2.4			
H10	WEB	2.4			
H11	REB	1.0			
H12	CSB	1.0			
H13	TIN	2.4			
H14	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD4	(LH)	2.59	4.26	6.99
→DO0 to DO3	(HH)	2.59	4.25	6.97
	(HL)	2.32	4.15	7.14
	(LL)	2.32	4.16	7.16
CSB	(LL)	2.24	3.92	6.66
→DO0 to DO3	(LH)	2.24	3.92	6.66
	(HL)	0.94	1.58	2.61
REB	(LH)	0.74	1.26	2.10
→DO0 to DO3	(HL)	0.79	1.23	1.95
DI0 to DI3	(HH)	1.86	3.24	5.51
→DO0 to DO3	(LL)	1.72	2.74	4.41

Equivalent Cells	884	Power (mW/MHz)		Rev.	1

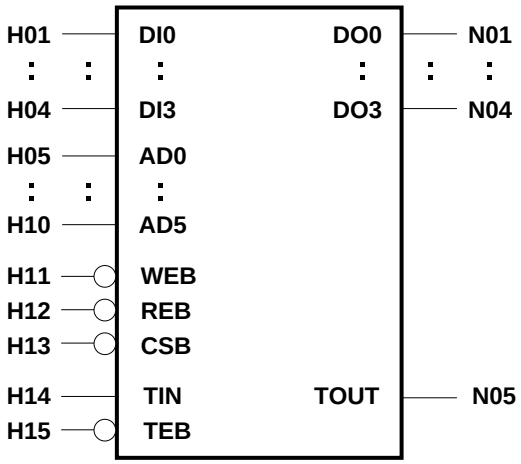
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.16**		
Address access time	**t_{ACA}**			**7.16**
Address output hold time	**t_{OH}**	**2.32**		
CSB access time	**t_{CSC}**			**6.66**
CSB output hold time	**t_{CSL}**	**0.94**		**2.61**
CSB output set time	**t_{CLL}**	**2.24**		
REB access time	**t_{REC}**			**2.11**
REB output hold time	**t_{REL}**	**0.79**		**1.95**
REB output set time	**t_{RLL}**	**0.75**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.89**		
CSB-WEB reset time	**t_{CWR}**	**4.53**		
Write pulse width	**t_{WP}**	**4.53**		
Address setup time	**t_{AS}**	**1.02**		
Address hold time	**t_{AH}**	**0.34**		
Input data setup time	**t_{DS}**	**3.35**		
Input data hold time	**t_{DH}**	**0.43**		
WEB access time	**t_{WEC}**			**5.55**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4B	**64 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	24.7
H05	AD0	2.4	N05	TOUT	26.0
:	:	:			
H10	AD5	2.4			
H11	WEB	2.4			
H12	REB	1.0			
H13	CSB	2.4			
H14	TIN	2.4			
H15	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD5	(LH)	2.81	4.80	8.04
→DO0 to DO3	(HH)	2.72	4.66	7.82
	(HL)	1.52	3.98	7.99
	(LL)	1.41	3.93	8.05
CSB	(LL)	2.55	4.41	7.43
→DO0 to DO3	(LH)	2.55	4.41	7.43
	(HL)	1.30	2.17	3.57
REB	(LH)	0.97	1.61	2.65
→DO0 to DO3	(HL)	1.12	1.76	2.81
DI0 to DI3	(HH)	2.08	3.58	6.03
→DO0 to DO3	(LL)	2.07	3.28	5.26

Equivalent Cells	1567	Power (mW/MHz)		Rev.	1

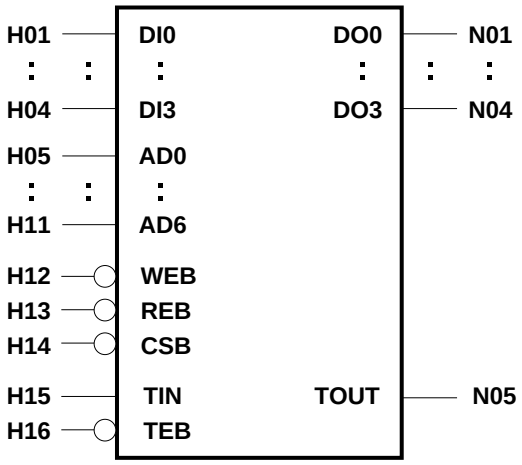
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.06**		
Address access time	**t_{ACA}**			**8.06**
Address output hold time	**t_{OH}**	**1.41**		
CSB access time	**t_{CSC}**			**7.43**
CSB output hold time	**t_{CSL}**	**1.30**		**3.57**
CSB output set time	**t_{CLL}**	**2.56**		
REB access time	**t_{REC}**			**2.65**
REB output hold time	**t_{REL}**	**1.12**		**2.81**
REB output set time	**t_{RLL}**	**0.97**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.34**		
CSB-WEB reset time	**t_{CWR}**	**4.72**		
Write pulse width	**t_{WP}**	**4.72**		
Address setup time	**t_{AS}**	**1.18**		
Address hold time	**t_{AH}**	**0.44**		
Input data setup time	**t_{DS}**	**3.39**		
Input data hold time	**t_{DH}**	**0.53**		
WEB access time	**t_{WEC}**			**6.09**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4D	**128 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)	2.00	4.48	8.53
:	:	:	:	:	:	→DO0 to DO3 (HH)	2.00	4.47	8.51
H04	DI3	2.4	N04	DO3	23.7	(HL)	1.81	4.30	8.35
H05	AD0	2.4	N05	TOUT	26.0	(LL)	1.81	4.31	8.38
:	:	:							
H11	AD6	2.4				CSB (LL)	1.02	3.51	7.55
H12	WEB	2.4				→DO0 to DO3 (LH)	1.02	3.51	7.55
H13	REB	1.0				(HL)	0.92	1.59	2.68
H14	CSB	1.0							
H15	TIN	2.4				REB (LH)	0.81	1.43	2.45
H16	TEB	5.0				→DO0 to DO3 (HL)	0.69	1.20	2.04
						DI0 to DI3 (HH)	1.85	3.46	6.09
						→DO0 to DO3 (LL)	1.64	2.99	5.20

Equivalent Cells	3753	Power (mW/MHz)		Rev.	1

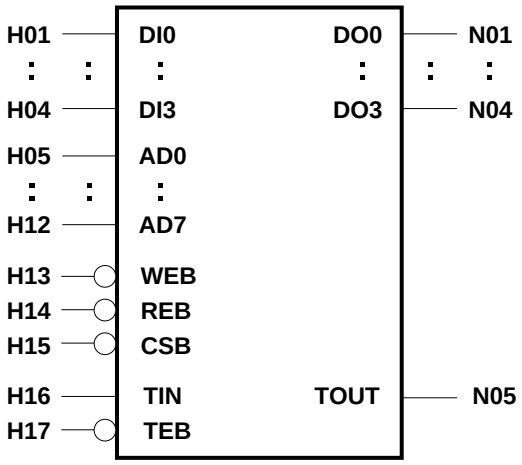
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.95**		
Address access time	**t_{ACA}**			**9.95**
Address output hold time	**t_{OH}**	**2.09**		
CSB access time	**t_{CSC}**			**7.56**
CSB output hold time	**t_{CSL}**	**1.08**		**2.69**
CSB output set time	**t_{CLL}**	**3.08**		
REB access time	**t_{REC}**			**2.45**
REB output hold time	**t_{REL}**	**0.80**		**2.04**
REB output set time	**t_{RLL}**	**0.93**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.76**		
CSB-WEB reset time	**t_{CWR}**	**3.70**		
Write pulse width	**t_{WP}**	**3.70**		
Address setup time	**t_{AS}**	**1.77**		
Address hold time	**t_{AH}**	**1.29**		
Input data setup time	**t_{DS}**	**3.46**		
Input data hold time	**t_{DH}**	**0.77**		
WEB access time	**t_{WEC}**			**5.83**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4F	**256 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	24.7
H05	AD0	2.4	N05	TOUT	26.0
:	:	:			
H12	AD7	2.4			
H13	WEB	2.4			
H14	REB	1.0			
H15	CSB	2.4			
H16	TIN	2.4			
H17	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD7	(LH)	1.60	4.51	9.24
→DO0 to DO3	(HH)	1.50	4.35	9.00
	(HL)	1.49	4.43	9.22
	(LL)	1.43	4.41	9.28
CSB	(LL)	1.34	4.05	8.45
→DO0 to DO3	(LH)	1.34	4.05	8.45
	(HL)	1.29	2.25	3.83
REB	(LH)	1.02	1.75	2.94
→DO0 to DO3	(HL)	0.97	1.71	2.92
DI0 to DI3	(HH)	2.04	3.76	6.56
→DO0 to DO3	(LL)	1.92	3.49	6.05

Equivalent Cells	3745	Power (mW/MHz)		Rev.	1

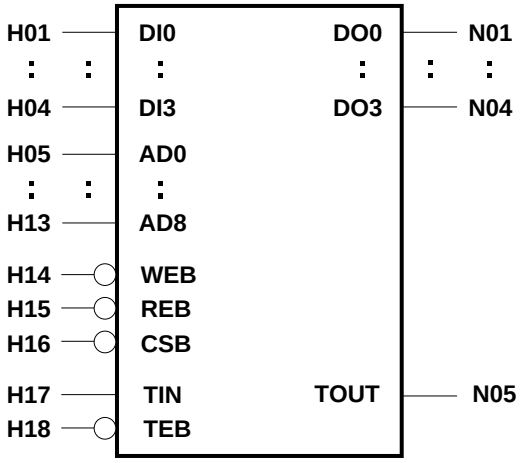
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.28**		
Address access time	**t_{ACA}**			**9.28**
Address output hold time	**t_{OH}**	**1.65**		
CSB access time	**t_{CSC}**			**8.46**
CSB output hold time	**t_{CSL}**	**1.49**		**3.84**
CSB output set time	**t_{CLL}**	**4.03**		
REB access time	**t_{REC}**			**2.95**
REB output hold time	**t_{REL}**	**1.13**		**2.92**
REB output set time	**t_{RLL}**	**1.18**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.79**		
CSB-WEB reset time	**t_{CWR}**	**3.73**		
Write pulse width	**t_{WP}**	**3.73**		
Address setup time	**t_{AS}**	**1.68**		
Address hold time	**t_{AH}**	**1.38**		
Input data setup time	**t_{DS}**	**3.37**		
Input data hold time	**t_{DH}**	**0.86**		
WEB access time	**t_{WEC}**			**6.49**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4H	**512 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	23.7
H05	AD0	2.4	N05	TOUT	26.0
:	:	:			
H13	AD8	2.4			
H14	WEB	2.4			
H15	REB	1.0			
H16	CSB	1.0			
H17	TIN	2.4			
H18	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD8	(LH)	1.81	4.90	9.94
→DO0 to DO3	(HH)	1.68	4.86	10.05
	(HL)	1.78	5.02	10.30
	(LL)	1.77	5.04	10.37
CSB	(LL)	1.75	4.73	9.60
→DO0 to DO3	(LH)	1.75	4.73	9.60
	(HL)	1.81	3.28	5.68
REB	(LH)	1.03	1.80	3.06
→DO0 to DO3	(HL)	1.29	2.31	3.99
DI0 to DI3	(HH)	2.07	3.83	6.69
→DO0 to DO3	(LL)	2.15	3.91	6.77

Equivalent Cells	7194	Power (mW/MHz)		Rev.	1

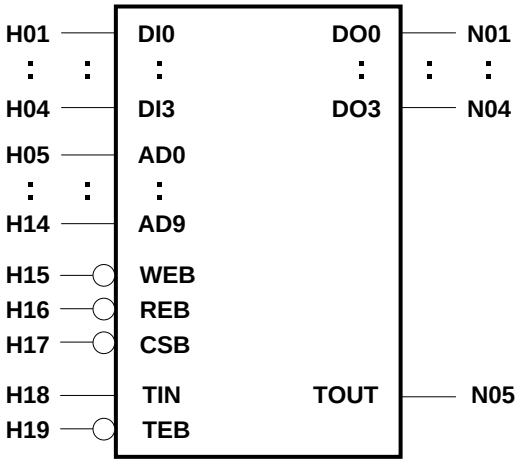
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.38**		
Address access time	**t_{ACA}**			**10.38**
Address output hold time	**t_{OH}**	**1.94**		
CSB access time	**t_{CSC}**			**9.61**
CSB output hold time	**t_{CSL}**	**2.65**		**5.68**
CSB output set time	**t_{CLL}**	**5.24**		
REB access time	**t_{REC}**			**3.07**
REB output hold time	**t_{REL}**	**1.49**		**3.99**
REB output set time	**t_{RLL}**	**1.20**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.73**		
CSB-WEB reset time	**t_{CWR}**	**4.15**		
Write pulse width	**t_{WP}**	**4.15**		
Address setup time	**t_{AS}**	**1.69**		
Address hold time	**t_{AH}**	**0.89**		
Input data setup time	**t_{DS}**	**3.42**		
Input data hold time	**t_{DH}**	**1.53**		
WEB access time	**t_{WEC}**			**7.48**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4M	**1K words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	21.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	21.7
H05	AD0	2.4	N05	TOUT	26.0
:	:	:			
H14	AD9	2.4			
H15	WEB	2.4			
H16	REB	1.0			
H17	CSB	1.0			
H18	TIN	2.4			
H19	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD9	(LH)	2.23	5.65	11.22
→DO0 to DO3	(HH)	2.07	5.58	11.32
	(HL)	2.01	5.14	10.24
	(LL)	1.93	5.14	10.38
CSB	(LL)	2.15	5.45	10.83
→DO0 to DO3	(LH)	2.15	5.45	10.83
	(HL)	1.96	3.39	5.74
REB	(LH)	1.28	2.20	3.71
→DO0 to DO3	(HL)	1.30	2.30	3.92
DI0 to DI3	(HH)	2.32	4.24	7.37
→DO0 to DO3	(LL)	2.29	4.16	7.20

Equivalent Cells	14155	Power (mW/MHz)		Rev.	1

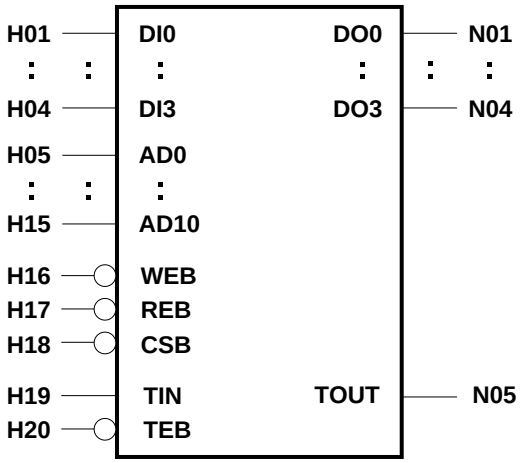
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**11.33**		
Address access time	**t_{ACA}**			**11.33**
Address output hold time	**t_{OH}**	**2.23**		
CSB access time	**t_{CSC}**			**10.84**
CSB output hold time	**t_{CSL}**	**2.26**		**5.74**
CSB output set time	**t_{CLL}**	**6.46**		
REB access time	**t_{REC}**			**3.72**
REB output hold time	**t_{REL}**	**1.50**		**3.93**
REB output set time	**t_{RLL}**	**0.89**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.24**		
CSB-WEB reset time	**t_{CWR}**	**4.58**		
Write pulse width	**t_{WP}**	**4.58**		
Address setup time	**t_{AS}**	**1.71**		
Address hold time	**t_{AH}**	**0.95**		
Input data setup time	**t_{DS}**	**3.52**		
Input data hold time	**t_{DH}**	**1.67**		
WEB access time	**t_{WEC}**			**8.47**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4S	**2K words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	17.7	AD0 to AD10 (LH)	2.26	5.99	12.07
:	:	:	:	:	:	→DO0 to DO3 (HH)	2.05	5.74	11.75
H04	DI3	2.4	N04	DO3	17.7	(HL)	2.12	5.37	10.68
H05	AD0	2.4	N05	TOUT	26.0	(LL)	2.04	5.35	10.74
:	:	:							
H15	AD10	2.4				CSB (LL)	2.27	5.68	11.25
H16	WEB	2.4				→DO0 to DO3 (LH)	2.27	5.68	11.25
H17	REB	1.0				(HL)	2.14	3.80	6.51
H18	CSB	2.4							
H19	TIN	2.4				REB (LH)	1.29	2.22	3.75
H20	TEB	5.0				→DO0 to DO3 (HL)	1.41	2.55	4.42
						DI0 to DI3 (HH)	2.32	4.24	7.37
						→DO0 to DO3 (LL)	2.38	4.36	7.60

Equivalent Cells	28077	Power (mW/MHz)		Rev.	1

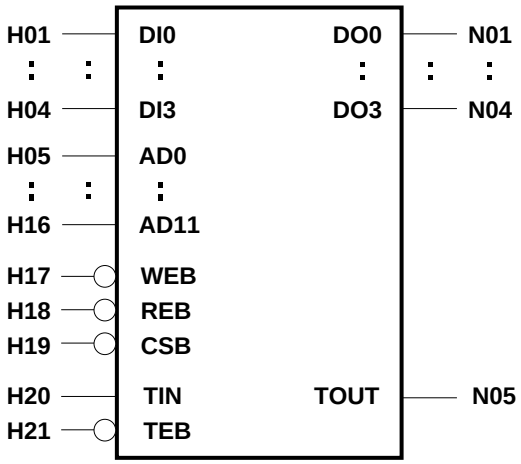
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.07**		
Address access time	**t_{ACA}**			**12.07**
Address output hold time	**t_{OH}**	**2.36**		
CSB access time	**t_{CSC}**			**11.26**
CSB output hold time	**t_{CSL}**	**2.47**		**6.52**
CSB output set time	**t_{CLL}**	**5.77**		
REB access time	**t_{REC}**			**3.77**
REB output hold time	**t_{REL}**	**1.63**		**4.43**
REB output set time	**t_{RLL}**	**1.49**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.54**		
CSB-WEB reset time	**t_{CWR}**	**4.76**		
Write pulse width	**t_{WP}**	**4.76**		
Address setup time	**t_{AS}**	**1.70**		
Address hold time	**t_{AH}**	**1.08**		
Input data setup time	**t_{DS}**	**3.44**		
Input data hold time	**t_{DH}**	**1.95**		
WEB access time	**t_{WEC}**			**8.86**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4U	**4K words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	17.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	17.7
H05	AD0	2.4	N05	TOUT	26.0
:	:	:			
H16	AD11	2.4			
H17	WEB	2.4			
H18	REB	2.4			
H19	CSB	1.0			
H20	TIN	2.4			
H21	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD11 →DO0 to DO3	(LH)	2.28	6.30	12.85
	(HH)	2.11	6.21	12.91
	(HL)	2.25	5.87	11.78
	(LL)	2.23	5.84	11.73
CSB →DO0 to DO3	(LL)	2.72	6.44	12.50
	(LH)	2.72	6.44	12.50
	(HL)	2.63	4.65	7.95
REB →DO0 to DO3	(LH)	1.39	2.38	3.99
	(HL)	1.66	3.03	5.26
DI0 to DI3 →DO0 to DO3	(HH)	2.57	4.65	8.04
	(LL)	2.72	4.95	8.59

Equivalent Cells	55775	Power (mW/MHz)		Rev.	1

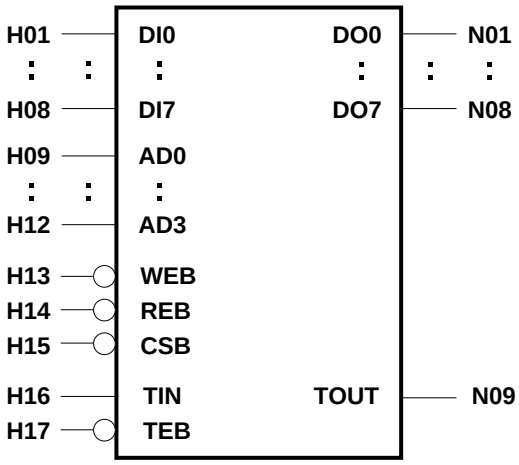
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.91**		
Address access time	**t_{ACA}**			**12.91**
Address output hold time	**t_{OH}**	**2.44**		
CSB access time	**t_{CSC}**			**12.51**
CSB output hold time	**t_{CSL}**	**3.04**		**7.95**
CSB output set time	**t_{CLL}**	**6.90**		
REB access time	**t_{REC}**			**3.99**
REB output hold time	**t_{REL}**	**1.92**		**5.28**
REB output set time	**t_{RLL}**	**1.60**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.28**		
CSB-WEB reset time	**t_{CWR}**	**5.20**		
Write pulse width	**t_{WP}**	**5.20**		
Address setup time	**t_{AS}**	**1.78**		
Address hold time	**t_{AH}**	**1.30**		
Input data setup time	**t_{DS}**	**3.55**		
Input data hold time	**t_{DH}**	**2.46**		
WEB access time	**t_{WEC}**			**9.80**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB87	**16 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	23.7
H09	AD0	2.4	N09	TOUT	26.0
:	:	:			
H12	AD3	2.4			
H13	WEB	2.4			
H14	REB	1.0			
H15	CSB	1.0			
H16	TIN	2.4			
H17	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD3	(LH)	2.31	3.81	6.26
→DO0 to DO7	(HH)	2.29	3.78	6.21
	(HL)	2.02	3.68	6.38
	(LL)	2.03	3.70	6.43
CSB	(LL)	2.02	3.49	5.89
→DO0 to DO7	(LH)	2.02	3.49	5.89
	(HL)	0.74	1.17	1.86
REB	(LH)	0.76	1.30	2.17
→DO0 to DO7	(HL)	0.83	1.29	2.04
DI0 to DI7	(HH)	1.85	3.20	5.41
→DO0 to DO7	(LL)	1.71	2.70	4.31

Equivalent Cells	1119	Power (mW/MHz)		Rev.	1

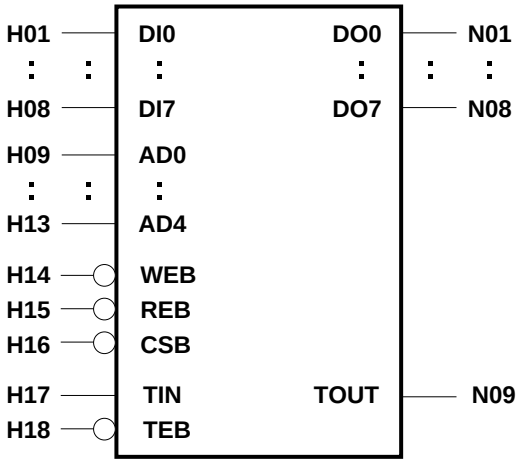
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.44**		
Address access time	**t_{ACA}**			**6.44**
Address output hold time	**t_{OH}**	**2.02**		
CSB access time	**t_{CSC}**			**5.89**
CSB output hold time	**t_{CSL}**	**0.99**		**2.71**
CSB output set time	**t_{CLL}**	**2.02**		
REB access time	**t_{REC}**			**2.14**
REB output hold time	**t_{REL}**	**0.84**		**2.04**
REB output set time	**t_{RLL}**	**0.77**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.68**		
CSB-WEB reset time	**t_{CWR}**	**4.05**		
Write pulse width	**t_{WP}**	**4.05**		
Address setup time	**t_{AS}**	**1.27**		
Address hold time	**t_{AH}**	**0.36**		
Input data setup time	**t_{DS}**	**3.30**		
Input data hold time	**t_{DH}**	**0.51**		
WEB access time	**t_{WEC}**			**5.57**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB89	**32 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	23.7
H09	AD0	2.4	N09	TOUT	26.0
:	:	:			
H13	AD4	2.4			
H14	WEB	2.4			
H15	REB	1.0			
H16	CSB	1.0			
H17	TIN	2.4			
H18	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD4	(LH)	2.65	4.34	7.12
→DO0 to DO7	(HH)	2.63	4.31	7.06
	(HL)	2.36	4.21	7.23
	(LL)	2.37	4.24	7.29
CSB	(LL)	2.27	3.97	6.74
→DO0 to DO7	(LH)	2.27	3.97	6.74
	(HL)	0.99	1.65	2.72
REB	(LH)	0.77	1.31	2.18
→DO0 to DO7	(HL)	0.84	1.30	2.05
DI0 to DI7	(HH)	1.86	3.25	5.52
→DO0 to DO7	(LL)	1.72	2.75	4.42

Equivalent Cells	1572	Power (mW/MHz)		Rev.	1

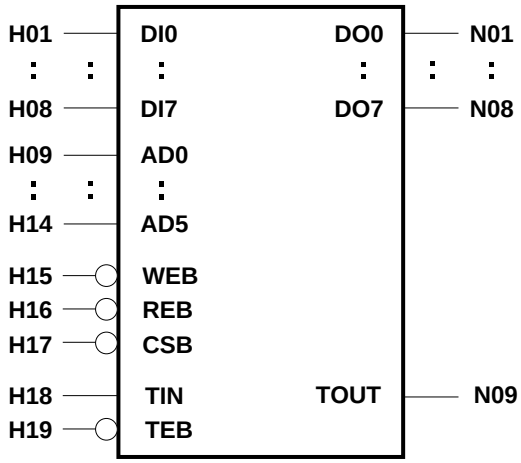
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.30**		
Address access time	**t_{ACA}**			**7.30**
Address output hold time	**t_{OH}**	**2.36**		
CSB access time	**t_{CSC}**			**6.74**
CSB output hold time	**t_{CSL}**	**1.00**		**2.72**
CSB output set time	**t_{CLL}**	**2.28**		
REB access time	**t_{REC}**			**2.15**
REB output hold time	**t_{REL}**	**0.85**		**2.05**
REB output set time	**t_{RLL}**	**0.78**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.20**		
CSB-WEB reset time	**t_{CWR}**	**4.55**		
Write pulse width	**t_{WP}**	**4.55**		
Address setup time	**t_{AS}**	**1.28**		
Address hold time	**t_{AH}**	**0.37**		
Input data setup time	**t_{DS}**	**3.31**		
Input data hold time	**t_{DH}**	**0.52**		
WEB access time	**t_{WEC}**			**5.68**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8B	**64 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD5 (LH)	2.86	4.45	7.04
:	:	:	:	:	:	→DO0 to DO7 (HH)	2.86	4.44	7.02
H08	DI7	2.4	N08	DO7	23.7	(HL)	2.46	4.44	7.67
H09	AD0	2.4	N09	TOUT	26.0	(LL)	2.46	4.45	7.69
:	:	:							
H14	AD5	2.4				CSB (LL)	2.34	4.25	7.38
H15	WEB	2.4				→DO0 to DO7 (LH)	2.34	4.25	7.38
H16	REB	1.0				(HL)	1.03	1.71	2.80
H17	CSB	1.0							
H18	TIN	2.4				REB (LH)	0.76	1.27	2.11
H19	TEB	5.0				→DO0 to DO7 (HL)	0.79	1.25	1.99
						DI0 to DI7 (HH)	1.74	3.17	5.51
						→DO0 to DO7 (LL)	1.60	2.92	5.06

Equivalent Cells	2267	Power (mW/MHz)		Rev.	1

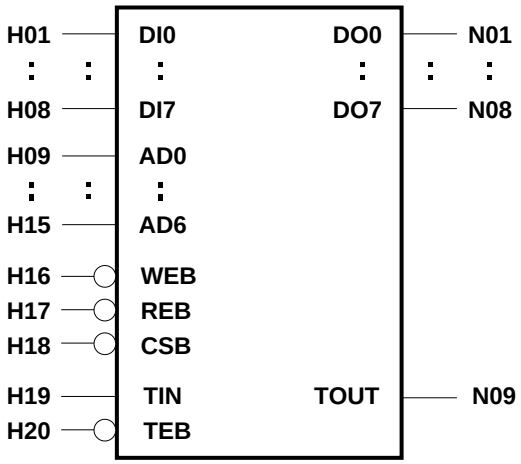
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.85**		
Address access time	**t_{ACA}**			**6.85**
Address output hold time	**t_{OH}**	**2.46**		
CSB access time	**t_{CSC}**			**7.39**
CSB output hold time	**t_{CSL}**	**1.04**		**2.80**
CSB output set time	**t_{CLL}**	**2.34**		
REB access time	**t_{REC}**			**2.12**
REB output hold time	**t_{REL}**	**0.79**		**2.00**
REB output set time	**t_{RLL}**	**0.76**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.48**		
CSB-WEB reset time	**t_{CWR}**	**3.63**		
Write pulse width	**t_{WP}**	**3.63**		
Address setup time	**t_{AS}**	**2.62**		
Address hold time	**t_{AH}**	**0.23**		
Input data setup time	**t_{DS}**	**2.62**		
Input data hold time	**t_{DH}**	**1.50**		
WEB access time	**t_{WEC}**			**4.78**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8D	**128 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)	2.02	4.52	8.58
:	:	:	:	:	:	→DO0 to DO7 (HH)	2.01	4.49	8.53
H08	DI7	2.4	N08	DO7	23.7	(HL)	1.82	4.31	8.38
H09	AD0	2.4	N09	TOUT	26.0	(LL)	1.83	4.34	8.43
:	:	:							
H15	AD6	2.4				CSB (LL)	1.03	3.52	7.59
H16	WEB	2.4				→DO0 to DO7 (LH)	1.03	3.52	7.59
H17	REB	1.0				(HL)	0.94	1.61	2.71
H18	CSB	1.0							
H19	TIN	2.4				REB (LH)	0.82	1.45	2.47
H20	TEB	5.0				→DO0 to DO7 (HL)	0.70	1.22	2.08
						DI0 to DI7 (HH)	1.85	3.46	6.09
						→DO0 to DO7 (LL)	1.64	2.99	5.20

Equivalent Cells	3753	Power (mW/MHz)		Rev.	1

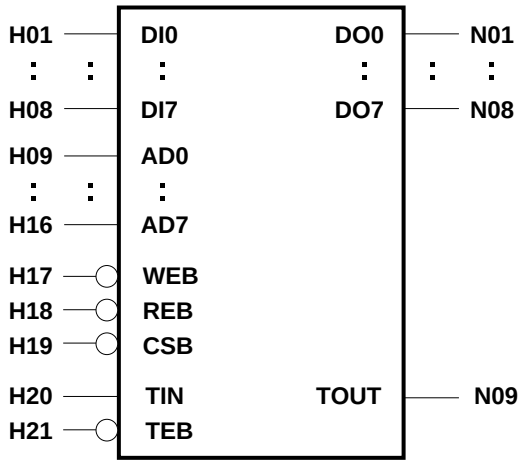
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.02**		
Address access time	**t_{ACA}**			**10.02**
Address output hold time	**t_{OH}**	**2.11**		
CSB access time	**t_{CSC}**			**7.60**
CSB output hold time	**t_{CSL}**	**1.08**		**2.71**
CSB output set time	**t_{CLL}**	**3.12**		
REB access time	**t_{REC}**			**2.48**
REB output hold time	**t_{REL}**	**0.71**		**2.08**
REB output set time	**t_{RLL}**	**0.82**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.45**		
CSB-WEB reset time	**t_{CWR}**	**3.73**		
Write pulse width	**t_{WP}**	**3.73**		
Address setup time	**t_{AS}**	**1.78**		
Address hold time	**t_{AH}**	**1.29**		
Input data setup time	**t_{DS}**	**3.82**		
Input data hold time	**t_{DH}**	**0.79**		
WEB access time	**t_{WEC}**			**5.87**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8F	**256 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	23.7
H09	AD0	2.4	N09	TOUT	26.0
:	:	:			
H16	AD7	2.4			
H17	WEB	2.4			
H18	REB	1.0			
H19	CSB	1.0			
H20	TIN	2.4			
H21	TEB	5.0			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
AD0 to AD7 →DO0 to DO7	(LH)	2.33	5.21	9.92
	(HH)	2.33	5.20	9.89
	(HL)	1.99	4.66	9.01
	(LL)	1.99	4.67	9.04
CSB →DO0 to DO7	(LL)	1.10	3.98	8.67
	(LH)	1.10	3.98	8.67
	(HL)	0.98	1.68	2.81
REB →DO0 to DO7	(LH)	0.95	1.59	2.64
	(HL)	0.72	1.26	2.13
DI0 to DI7 →DO0 to DO7	(HH)	1.99	3.70	6.49
	(LL)	1.75	3.23	5.65

Equivalent Cells	6246	Power (mW/MHz)		Rev.	1

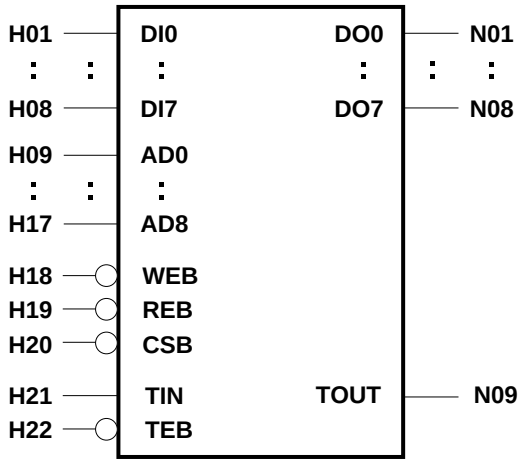
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.92**		
Address access time	**t_{ACA}**			**9.92**
Address output hold time	**t_{OH}**	**2.29**		
CSB access time	**t_{CSC}**			**8.67**
CSB output hold time	**t_{CSL}**	**1.13**		**2.81**
CSB output set time	**t_{CLL}**	**3.31**		
REB access time	**t_{REC}**			**2.64**
REB output hold time	**t_{REL}**	**0.83**		**2.13**
REB output set time	**t_{RLL}**	**1.10**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.43**		
CSB-WEB reset time	**t_{CWR}**	**4.15**		
Write pulse width	**t_{WP}**	**4.15**		
Address setup time	**t_{AS}**	**1.91**		
Address hold time	**t_{AH}**	**1.37**		
Input data setup time	**t_{DS}**	**3.64**		
Input data hold time	**t_{DH}**	**0.95**		
WEB access time	**t_{WEC}**			**6.53**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8H	**512 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	24.7
H09	AD0	2.4	N09	TOUT	26.0
:	:	:			
H17	AD8	2.4			
H18	WEB	2.4			
H19	REB	1.0			
H20	CSB	2.4			
H21	TIN	2.4			
H22	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD8	(LH)	1.68	5.01	10.44
→DO0 to DO7	(HH)	1.59	4.93	10.39
	(HL)	1.54	4.71	9.89
	(LL)	1.49	4.70	9.94
CSB	(LL)	1.42	4.52	9.57
→DO0 to DO7	(LH)	1.42	4.52	9.57
	(HL)	1.34	2.34	3.97
REB	(LH)	1.16	1.91	3.14
→DO0 to DO7	(HL)	1.01	1.77	3.01
DI0 to DI7	(HH)	2.18	4.00	6.97
→DO0 to DO7	(LL)	2.03	3.73	6.51

Equivalent Cells	12206	Power (mW/MHz)		Rev.	1

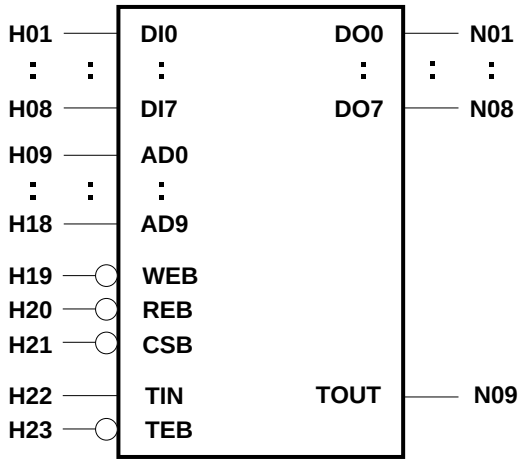
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.44**		
Address access time	**t_{ACA}**			**10.44**
Address output hold time	**t_{OH}**	**1.71**		
CSB access time	**t_{CSC}**			**9.57**
CSB output hold time	**t_{CSL}**	**1.55**		**3.97**
CSB output set time	**t_{CLL}**	**4.26**		
REB access time	**t_{REC}**			**3.15**
REB output hold time	**t_{REL}**	**1.16**		**3.01**
REB output set time	**t_{RLL}**	**1.34**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.59**		
CSB-WEB reset time	**t_{CWR}**	**4.18**		
Write pulse width	**t_{WP}**	**4.18**		
Address setup time	**t_{AS}**	**1.82**		
Address hold time	**t_{AH}**	**0.59**		
Input data setup time	**t_{DS}**	**3.54**		
Input data hold time	**t_{DH}**	**0.94**		
WEB access time	**t_{WEC}**			**6.99**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8M	**1K words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD9 (LH)	2.91	7.02	13.72
:	:	:	:	:	:	→DO0 to DO7 (HH)	2.91	7.01	13.69
H08	DI7	2.4	N08	DO7	23.7	(HL)	2.38	6.40	12.96
H09	AD0	2.4	N09	TOUT	26.0	(LL)	2.38	6.41	12.99
:	:	:							
H18	AD9	2.4				CSB (LL)	1.19	4.81	10.70
H19	WEB	2.4				→DO0 to DO7 (LH)	1.19	4.81	10.70
H20	REB	1.0				(HL)	1.06	1.87	3.19
H21	CSB	1.0							
H22	TIN	2.4				REB (LH)	1.01	1.72	2.88
H23	TEB	5.0				→DO0 to DO7 (HL)	0.74	1.35	2.35
						DI0 to DI7 (HH)	2.94	5.58	9.88
						→DO0 to DO7 (LL)	2.61	4.86	8.52

Equivalent Cells	22140	Power (mW/MHz)		Rev.	1

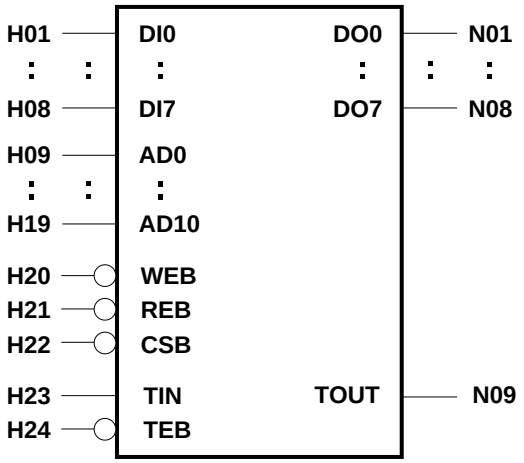
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**13.72**		
Address access time	**t_{ACA}**			**13.72**
Address output hold time	**t_{OH}**	**2.75**		
CSB access time	**t_{CSC}**			**10.70**
CSB output hold time	**t_{CSL}**	**1.23**		**3.19**
CSB output set time	**t_{CLL}**	**3.58**		
REB access time	**t_{REC}**			**2.89**
REB output hold time	**t_{REL}**	**0.86**		**2.35**
REB output set time	**t_{RLL}**	**1.16**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.71**		
CSB-WEB reset time	**t_{CWR}**	**5.22**		
Write pulse width	**t_{WP}**	**5.22**		
Address setup time	**t_{AS}**	**2.61**		
Address hold time	**t_{AH}**	**0.88**		
Input data setup time	**t_{DS}**	**5.22**		
Input data hold time	**t_{DH}**	**0.80**		
WEB access time	**t_{WEC}**			**9.82**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8S	**2K words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	24.7
H09	AD0	2.4	N09	TOUT	26.0
:	:	:			
H19	AD10	2.4			
H20	WEB	2.4			
H21	REB	1.0			
H22	CSB	2.4			
H23	TIN	2.4			
H24	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD10	(LH)	1.77	6.51	14.23
→DO0 to DO7	(HH)	1.67	6.43	14.19
	(HL)	1.61	6.26	13.84
	(LL)	1.56	6.25	13.89
CSB	(LL)	1.50	5.34	11.60
→DO0 to DO7	(LH)	1.50	5.34	11.60
	(HL)	1.42	2.53	4.34
REB	(LH)	1.21	2.03	3.38
→DO0 to DO7	(HL)	1.02	1.86	3.23
DI0 to DI7	(HH)	3.13	5.88	10.36
→DO0 to DO7	(LL)	2.89	5.35	9.36

Equivalent Cells	43983	Power (mW/MHz)		Rev.	1

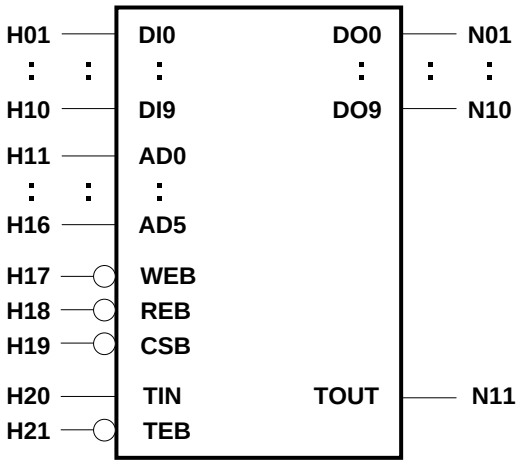
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**14.24**		
Address access time	**t_{ACA}**			**14.24**
Address output hold time	**t_{OH}**	**1.81**		
CSB access time	**t_{CSC}**			**11.60**
CSB output hold time	**t_{CSL}**	**1.64**		**4.34**
CSB output set time	**t_{CLL}**	**4.53**		
REB access time	**t_{REC}**			**3.38**
REB output hold time	**t_{REL}**	**1.18**		**3.23**
REB output set time	**t_{RLL}**	**1.40**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.29**		
CSB-WEB reset time	**t_{CWR}**	**4.86**		
Write pulse width	**t_{WP}**	**4.86**		
Address setup time	**t_{AS}**	**2.52**		
Address hold time	**t_{AH}**	**0.91**		
Input data setup time	**t_{DS}**	**5.12**		
Input data hold time	**t_{DH}**	**0.88**		
WEB access time	**t_{WEC}**			**10.34**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAB	**64 words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	23.7
H11	AD0	2.4	N11	TOUT	26.0
:	:	:			
H16	AD5	2.4			
H17	WEB	2.4			
H18	REB	1.0			
H19	CSB	1.0			
H20	TIN	2.4			
H21	TEB	5.0			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
AD0 to AD5 →DO0 to DO9	(LH)	2.86	4.73	7.78
	(HH)	2.86	4.72	7.76
	(HL)	2.40	4.27	7.33
	(LL)	2.40	4.28	7.35
CSB →DO0 to DO9	(LL)	2.29	4.30	7.56
	(LH)	2.29	4.30	7.56
	(HL)	1.05	1.73	2.85
REB →DO0 to DO9	(LH)	0.76	1.27	2.11
	(HL)	0.79	1.25	2.00
DI0 to DI9 →DO0 to DO9	(HH)	1.74	3.20	5.60
	(LL)	1.60	2.92	5.07

Equivalent Cells	2750	Power (mW/MHz)		Rev.	1

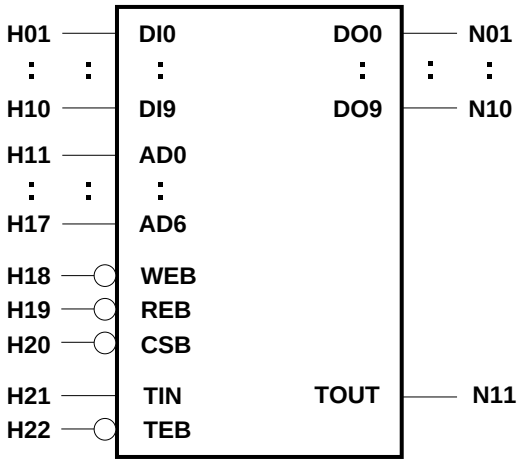
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.79**		
Address access time	**t_{ACA}**			**7.79**
Address output hold time	**t_{OH}**	**2.40**		
CSB access time	**t_{CSC}**			**7.58**
CSB output hold time	**t_{CSL}**	**1.05**		**2.85**
CSB output set time	**t_{CLL}**	**2.29**		
REB access time	**t_{REC}**			**2.12**
REB output hold time	**t_{REL}**	**0.79**		**2.01**
REB output set time	**t_{RLL}**	**0.76**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.03**		
CSB-WEB reset time	**t_{CWR}**	**3.90**		
Write pulse width	**t_{WP}**	**3.90**		
Address setup time	**t_{AS}**	**1.90**		
Address hold time	**t_{AH}**	**0.23**		
Input data setup time	**t_{DS}**	**2.47**		
Input data hold time	**t_{DH}**	**0.73**		
WEB access time	**t_{WEC}**			**4.70**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAD	**128 words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	23.7
H11	AD0	2.4	N11	TOUT	26.0
:	:	:			
H17	AD6	2.4			
H18	WEB	2.4			
H19	REB	1.0			
H20	CSB	1.0			
H21	TIN	2.4			
H22	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD6	(LH)	2.88	5.19	8.97
→DO0 to DO9	(HH)	2.78	5.05	8.74
	(HL)	1.61	4.11	8.19
	(LL)	1.50	4.06	8.24
CSB	(LL)	2.62	4.80	8.35
→DO0 to DO9	(LH)	2.62	4.80	8.35
	(HL)	1.39	2.31	3.81
REB	(LH)	1.02	1.64	2.66
→DO0 to DO9	(HL)	1.10	1.77	2.87
DI0 to DI9	(HH)	1.97	3.55	6.13
→DO0 to DO9	(LL)	1.94	3.46	5.93

Equivalent Cells	6383	Power (mW/MHz)		Rev.	1

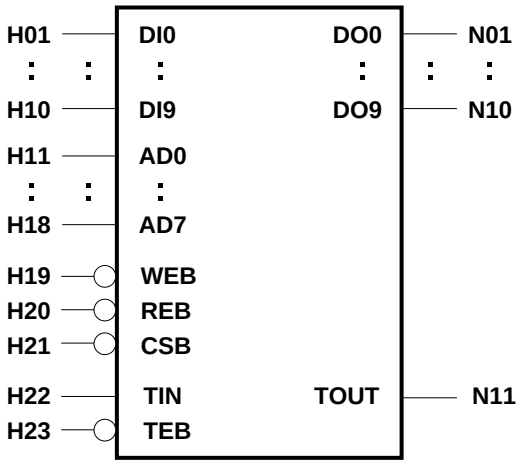
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.97**		
Address access time	**t_{ACA}**			**8.97**
Address output hold time	**t_{OH}**	**1.51**		
CSB access time	**t_{CSC}**			**8.36**
CSB output hold time	**t_{CSL}**	**1.40**		**3.81**
CSB output set time	**t_{CLL}**	**2.62**		
REB access time	**t_{REC}**			**2.68**
REB output hold time	**t_{REL}**	**1.11**		**2.88**
REB output set time	**t_{RLL}**	**1.02**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.05**		
CSB-WEB reset time	**t_{CWR}**	**3.96**		
Write pulse width	**t_{WP}**	**3.96**		
Address setup time	**t_{AS}**	**1.76**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**2.50**		
Input data hold time	**t_{DH}**	**0.83**		
WEB access time	**t_{WEC}**			**5.23**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAF	**256 words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	23.7
H11	AD0	2.4	N11	TOUT	26.0
:	:	:			
H18	AD7	2.4			
H19	WEB	2.4			
H20	REB	1.0			
H21	CSB	1.0			
H22	TIN	2.4			
H23	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD7	(LH)	2.27	5.25	10.11
→DO0 to DO9	(HH)	2.27	5.24	10.08
	(HL)	2.11	4.91	9.47
	(LL)	2.11	4.91	9.49
CSB	(LL)	1.13	3.95	8.56
→DO0 to DO9	(LH)	1.13	3.95	8.56
	(HL)	0.99	1.73	2.94
REB	(LH)	0.97	1.62	2.68
→DO0 to DO9	(HL)	0.74	1.31	2.25
DI0 to DI9	(HH)	1.99	3.70	6.49
→DO0 to DO9	(LL)	1.75	3.23	5.65

Equivalent Cells	7673	Power (mW/MHz)		Rev.	1

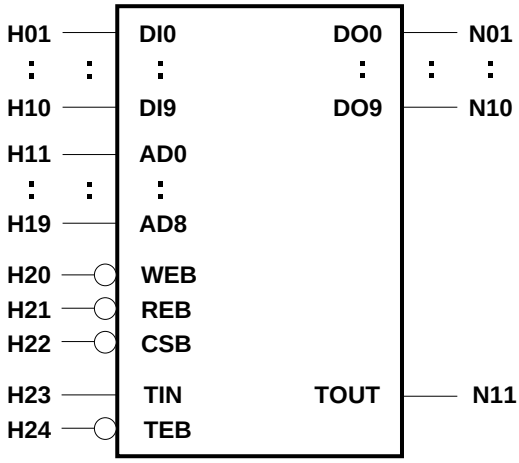
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.21**		
Address access time	**t_{ACA}**			**10.21**
Address output hold time	**t_{OH}**	**2.44**		
CSB access time	**t_{CSC}**			**8.57**
CSB output hold time	**t_{CSL}**	**1.15**		**2.94**
CSB output set time	**t_{CLL}**	**3.38**		
REB access time	**t_{REC}**			**2.69**
REB output hold time	**t_{REL}**	**0.86**		**2.25**
REB output set time	**t_{RLL}**	**1.13**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.67**		
CSB-WEB reset time	**t_{CWR}**	**4.41**		
Write pulse width	**t_{WP}**	**4.41**		
Address setup time	**t_{AS}**	**1.89**		
Address hold time	**t_{AH}**	**1.37**		
Input data setup time	**t_{DS}**	**3.59**		
Input data hold time	**t_{DH}**	**1.01**		
WEB access time	**t_{WEC}**			**6.48**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAH	**512 words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	24.7
H11	AD0	2.4	N11	TOUT	26.0
:	:	:			
H19	AD8	2.4			
H20	WEB	2.4			
H21	REB	1.0			
H22	CSB	2.4			
H23	TIN	2.4			
H24	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD8	(LH)	1.71	5.10	10.64
→DO0 to DO9	(HH)	1.60	5.02	10.58
	(HL)	1.55	4.90	10.35
	(LL)	1.50	4.88	10.39
CSB	(LL)	1.44	4.49	9.46
→DO0 to DO9	(LH)	1.44	4.49	9.46
	(HL)	1.35	2.40	4.10
REB	(LH)	1.18	1.94	3.18
→DO0 to DO9	(HL)	1.02	1.82	3.12
DI0 to DI9	(HH)	2.18	4.00	6.97
→DO0 to DO9	(LL)	2.03	3.73	6.51

Equivalent Cells	15042	Power (mW/MHz)		Rev.	1

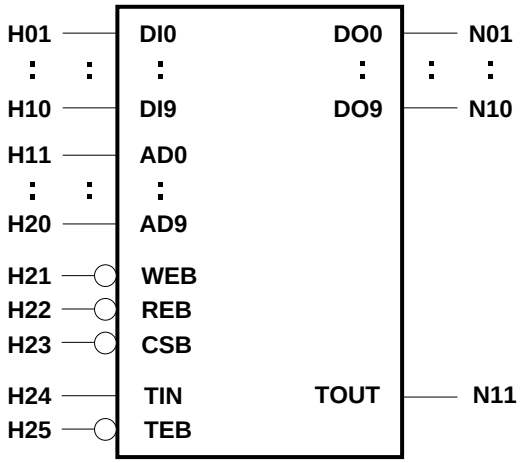
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.64**		
Address access time	**t_{ACA}**			**10.64**
Address output hold time	**t_{OH}**	**1.73**		
CSB access time	**t_{CSC}**			**9.46**
CSB output hold time	**t_{CSL}**	**1.56**		**4.10**
CSB output set time	**t_{CLL}**	**4.33**		
REB access time	**t_{REC}**			**3.18**
REB output hold time	**t_{REL}**	**1.18**		**3.12**
REB output set time	**t_{RLL}**	**1.36**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.81**		
CSB-WEB reset time	**t_{CWR}**	**4.44**		
Write pulse width	**t_{WP}**	**4.44**		
Address setup time	**t_{AS}**	**1.78**		
Address hold time	**t_{AH}**	**0.59**		
Input data setup time	**t_{DS}**	**3.49**		
Input data hold time	**t_{DH}**	**0.99**		
WEB access time	**t_{WEC}**			**6.94**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAM	**1K words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD9 (LH)	3.03	7.41	14.54
:	:	:	:	:	:	→DO0 to DO9 (HH)	3.03	7.39	14.51
H10	DI9	2.4	N10	DO9	23.7	(HL)	2.38	6.71	13.79
H11	AD0	2.4	N11	TOUT	26.0	(LL)	2.38	6.72	13.81
:	:	:							
H20	AD9	2.4				CSB (LL)	1.21	5.03	11.26
H21	WEB	2.4				→DO0 to DO9 (LH)	1.21	5.03	11.26
H22	REB	1.0				(HL)	1.07	1.91	3.27
H23	CSB	1.0							
H24	TIN	2.4				REB (LH)	1.02	1.75	2.94
H25	TEB	5.0				→DO0 to DO9 (HL)	0.77	1.40	2.42
						DI0 to DI9 (HH)	2.94	5.58	9.88
						→DO0 to DO9 (LL)	2.61	4.81	8.39

Equivalent Cells	27400	Power (mW/MHz)		Rev.	1

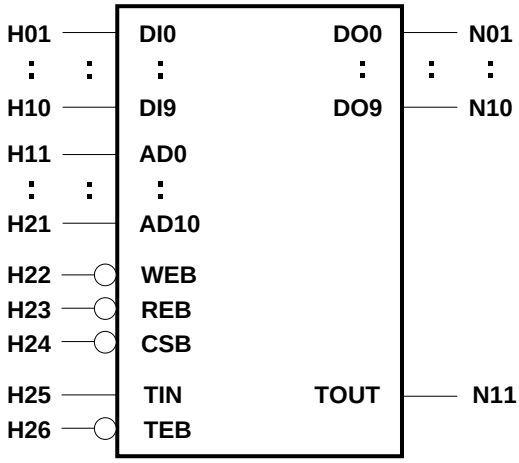
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**14.54**		
Address access time	**t_{ACA}**			**14.54**
Address output hold time	**t_{OH}**	**2.75**		
CSB access time	**t_{CSC}**			**11.27**
CSB output hold time	**t_{CSL}**	**1.23**		**3.27**
CSB output set time	**t_{CLL}**	**3.64**		
REB access time	**t_{REC}**			**2.94**
REB output hold time	**t_{REL}**	**0.90**		**2.42**
REB output set time	**t_{RLL}**	**1.18**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.90**		
CSB-WEB reset time	**t_{CWR}**	**5.04**		
Write pulse width	**t_{WP}**	**5.04**		
Address setup time	**t_{AS}**	**2.94**		
Address hold time	**t_{AH}**	**0.92**		
Input data setup time	**t_{DS}**	**5.17**		
Input data hold time	**t_{DH}**	**0.90**		
WEB access time	**t_{WEC}**			**9.53**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAS	**2K words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	24.7
H11	AD0	2.4	N11	TOUT	26.0
:	:	:			
H21	AD10	2.4			
H22	WEB	2.4			
H23	REB	1.0			
H24	CSB	2.4			
H25	TIN	2.4			
H26	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD10	(LH)	1.79	6.83	15.07
→DO0 to DO9	(HH)	1.70	6.76	15.01
	(HL)	1.63	5.49	11.78
	(LL)	1.57	6.56	14.71
CSB	(LL)	1.53	5.57	12.16
→DO0 to DO9	(LH)	1.53	5.57	12.16
	(HL)	1.43	2.57	4.43
REB	(LH)	1.23	2.07	3.43
→DO0 to DO9	(HL)	1.06	1.91	3.30
DI0 to DI9	(HH)	3.13	5.88	10.36
→DO0 to DO9	(LL)	2.89	5.30	9.23

Equivalent Cells	54491	Power (mW/MHz)		Rev.	1

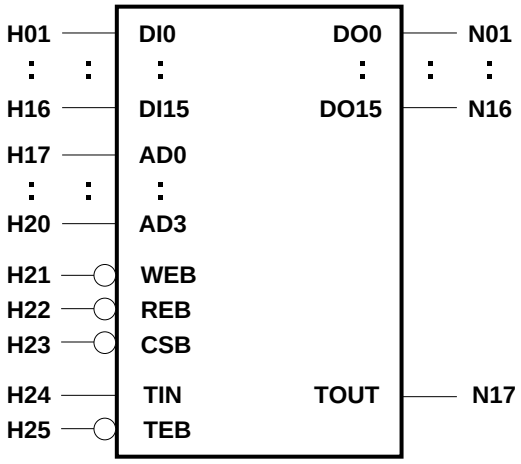
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**15.07**		
Address access time	**t_{ACA}**			**15.07**
Address output hold time	**t_{OH}**	**1.81**		
CSB access time	**t_{CSC}**			**12.16**
CSB output hold time	**t_{CSL}**	**1.65**		**4.43**
CSB output set time	**t_{CLL}**	**4.59**		
REB access time	**t_{REC}**			**3.45**
REB output hold time	**t_{REL}**	**1.23**		**3.30**
REB output set time	**t_{RLL}**	**1.43**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.85**		
CSB-WEB reset time	**t_{CWR}**	**5.06**		
Write pulse width	**t_{WP}**	**5.06**		
Address setup time	**t_{AS}**	**2.85**		
Address hold time	**t_{AH}**	**0.96**		
Input data setup time	**t_{DS}**	**5.07**		
Input data hold time	**t_{DH}**	**0.99**		
WEB access time	**t_{WEC}**			**10.05**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBC7	**16 words × 16 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD3 (LH)	2.43	3.98	6.52
:	:	:	:	:	:	→DO0 to DO15 (HH)	2.39	3.90	6.38
H16	DI15	2.4	N16	DO15	23.7	(HL)	2.11	3.80	6.55
H17	AD0	2.4	N17	TOUT	26.0	(LL)	2.15	3.88	6.70
:	:	:							
H20	AD3	2.4				CSB (LL)	2.11	3.60	6.03
H21	WEB	2.4				→DO0 to DO15 (LH)	2.11	3.60	6.03
H22	REB	1.0				(HL)	0.83	1.30	2.05
H23	CSB	1.0							
H24	TIN	2.4				REB (LH)	0.86	1.42	2.33
H25	TEB	2.5				→DO0 to DO15 (HL)	0.92	1.42	2.24
						DI0 to DI15 (HH)	2.21	3.29	5.06
						→DO0 to DO15 (LL)	1.73	2.71	4.31

Equivalent Cells	2057	Power (mW/MHz)		Rev.	1

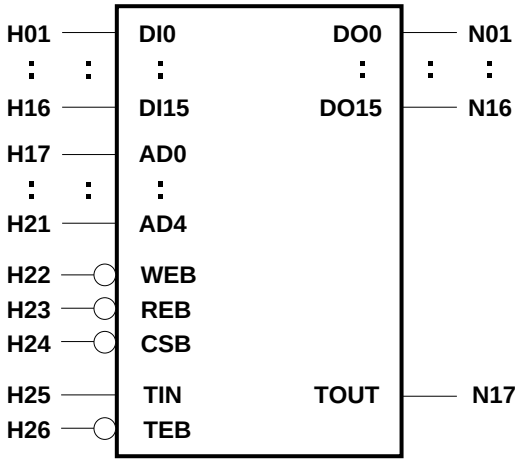
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.70**		
Address access time	**t_{ACA}**			**6.70**
Address output hold time	**t_{OH}**	**2.20**		
CSB access time	**t_{CSC}**			**6.05**
CSB output hold time	**t_{CSL}**	**1.08**		**2.90**
CSB output set time	**t_{CLL}**	**2.35**		
REB access time	**t_{REC}**			**2.33**
REB output hold time	**t_{REL}**	**0.92**		**2.24**
REB output set time	**t_{RLL}**	**0.86**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.05**		
CSB-WEB reset time	**t_{CWR}**	**4.34**		
Write pulse width	**t_{WP}**	**4.34**		
Address setup time	**t_{AS}**	**1.29**		
Address hold time	**t_{AH}**	**0.42**		
Input data setup time	**t_{DS}**	**3.20**		
Input data hold time	**t_{DH}**	**0.69**		
WEB access time	**t_{WEC}**			**5.80**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBC9	**32 words × 16 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	AD0	2.4	N17	TOUT	26.0
:	:	:			
H21	AD4	2.4			
H22	WEB	2.4			
H23	REB	1.0			
H24	CSB	1.0			
H25	TIN	2.4			
H26	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD4	(LH)	2.76	4.51	7.37
→DO0 to DO15	(HH)	2.72	4.44	7.23
	(HL)	2.44	4.33	7.40
	(LL)	2.49	4.41	7.55
CSB	(LL)	2.36	4.08	6.89
→DO0 to DO15	(LH)	2.36	4.08	6.89
	(HL)	1.08	1.78	2.91
REB	(LH)	0.87	1.43	2.34
→DO0 to DO15	(HL)	0.92	1.43	2.25
DI0 to DI15	(HH)	1.86	3.25	5.52
→DO0 to DO15	(LL)	1.74	2.76	4.42

Equivalent Cells	2946	Power (mW/MHz)		Rev.	1

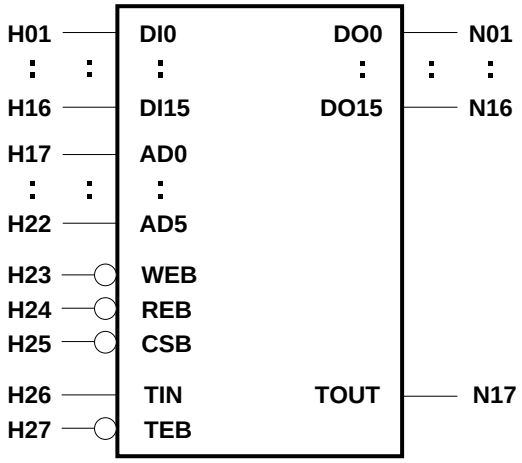
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.55**		
Address access time	**t_{ACA}**			**7.55**
Address output hold time	**t_{OH}**	**2.45**		
CSB access time	**t_{CSC}**			**6.90**
CSB output hold time	**t_{CSL}**	**1.08**		**2.91**
CSB output set time	**t_{CLL}**	**2.36**		
REB access time	**t_{REC}**			**2.34**
REB output hold time	**t_{REL}**	**0.93**		**2.25**
REB output set time	**t_{RLL}**	**0.87**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.57**		
CSB-WEB reset time	**t_{CWR}**	**4.84**		
Write pulse width	**t_{WP}**	**4.84**		
Address setup time	**t_{AS}**	**1.30**		
Address hold time	**t_{AH}**	**0.43**		
Input data setup time	**t_{DS}**	**3.21**		
Input data hold time	**t_{DH}**	**0.70**		
WEB access time	**t_{WEC}**			**5.91**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCB	**64 words × 16 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	AD0	2.4	N17	TOUT	26.0
:	:	:			
H22	AD5	2.4			
H23	WEB	2.4			
H24	REB	1.0			
H25	CSB	1.0			
H26	TIN	2.4			
H27	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD5	(LH)	2.92	4.54	7.18
→DO0 to DO15	(HH)	2.91	4.51	7.12
	(HL)	2.51	4.51	7.77
	(LL)	2.52	4.54	7.83
CSB	(LL)	2.39	4.32	7.47
→DO0 to DO15	(LH)	2.39	4.32	7.47
	(HL)	1.09	1.78	2.91
REB	(LH)	0.82	1.34	2.19
→DO0 to DO15	(HL)	0.84	1.32	2.10
DI0 to DI15	(HH)	1.75	3.21	5.61
→DO0 to DO15	(LL)	1.61	2.92	5.06

Equivalent Cells	4312	Power (mW/MHz)		Rev.	1

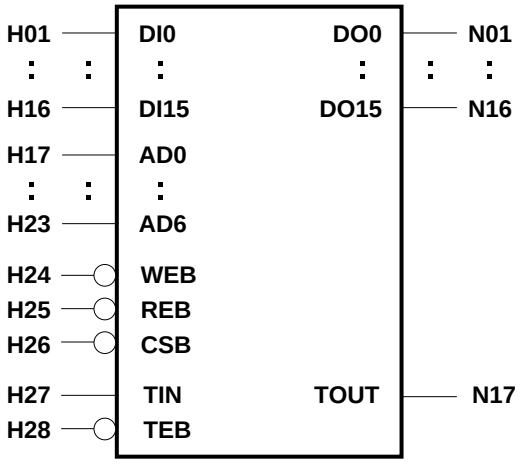
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.83**		
Address access time	**t_{ACA}**			**7.83**
Address output hold time	**t_{OH}**	**2.51**		
CSB access time	**t_{CSC}**			**7.48**
CSB output hold time	**t_{CSL}**	**1.09**		**2.91**
CSB output set time	**t_{CLL}**	**2.39**		
REB access time	**t_{REC}**			**2.20**
REB output hold time	**t_{REL}**	**0.85**		**2.11**
REB output set time	**t_{RLL}**	**0.82**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.72**		
CSB-WEB reset time	**t_{CWR}**	**3.68**		
Write pulse width	**t_{WP}**	**3.68**		
Address setup time	**t_{AS}**	**2.78**		
Address hold time	**t_{AH}**	**0.26**		
Input data setup time	**t_{DS}**	**2.57**		
Input data hold time	**t_{DH}**	**1.60**		
WEB access time	**t_{WEC}**			**4.90**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCD	**128 words × 16 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	AD0	2.4	N17	TOUT	26.0
:	:	:			
H23	AD6	2.4			
H24	WEB	2.4			
H25	REB	1.0			
H26	CSB	1.0			
H27	TIN	2.4			
H28	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD6	(LH)	2.05	4.56	8.67
→DO0 to DO15	(HH)	2.03	4.53	8.60
	(HL)	1.85	4.35	8.44
	(LL)	1.86	4.39	8.52
CSB	(LL)	1.06	3.56	7.64
→DO0 to DO15	(LH)	1.06	3.56	7.64
	(HL)	0.96	1.65	2.77
REB	(LH)	0.84	1.48	2.54
→DO0 to DO15	(HL)	0.72	1.26	2.13
DI0 to DI15	(HH)	1.85	3.46	6.09
→DO0 to DO15	(LL)	1.64	2.99	5.20

Equivalent Cells	7269	Power (mW/MHz)		Rev.	1

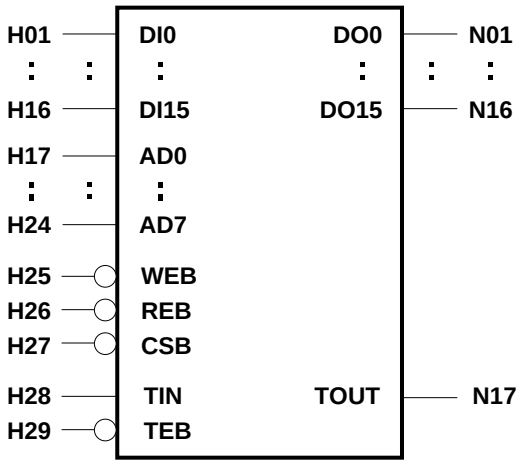
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.13**		
Address access time	**t_{ACA}**			**10.13**
Address output hold time	**t_{OH}**	**2.13**		
CSB access time	**t_{CSC}**			**7.64**
CSB output hold time	**t_{CSL}**	**1.11**		**2.78**
CSB output set time	**t_{CLL}**	**3.18**		
REB access time	**t_{REC}**			**2.54**
REB output hold time	**t_{REL}**	**0.72**		**2.13**
REB output set time	**t_{RLL}**	**0.85**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.89**		
CSB-WEB reset time	**t_{CWR}**	**3.78**		
Write pulse width	**t_{WP}**	**3.78**		
Address setup time	**t_{AS}**	**1.80**		
Address hold time	**t_{AH}**	**1.31**		
Input data setup time	**t_{DS}**	**3.41**		
Input data hold time	**t_{DH}**	**0.85**		
WEB access time	**t_{WEC}**			**5.96**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCF	**256 words × 16 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	AD0	2.4	N17	TOUT	26.0
:	:	:			
H24	AD7	2.4			
H25	WEB	2.4			
H26	REB	1.0			
H27	CSB	1.0			
H28	TIN	2.4			
H29	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD7	(LH)	2.34	5.24	9.96
→DO0 to DO15	(HH)	2.34	5.22	9.92
	(HL)	2.00	4.68	9.04
	(LL)	2.01	4.70	9.10
CSB	(LL)	1.12	4.00	8.70
→DO0 to DO15	(LH)	1.12	4.00	8.70
	(HL)	0.99	1.70	2.85
REB	(LH)	0.96	1.61	2.66
→DO0 to DO15	(HL)	0.73	1.27	2.16
DI0 to DI15	(HH)	1.99	3.70	6.49
→DO0 to DO15	(LL)	1.75	3.23	5.65

Equivalent Cells	12242	Power (mW/MHz)		Rev.	1

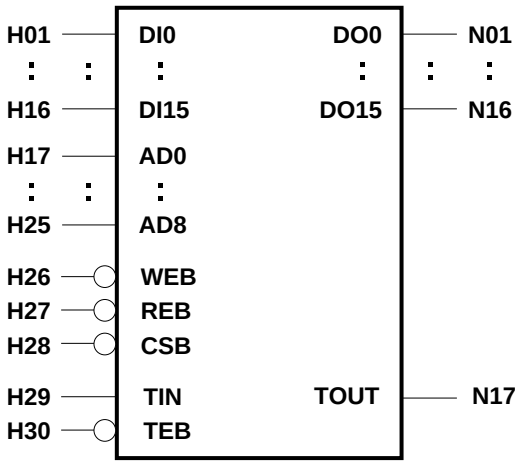
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.97**		
Address access time	**t_{ACA}**			**9.97**
Address output hold time	**t_{OH}**	**2.31**		
CSB access time	**t_{CSC}**			**8.70**
CSB output hold time	**t_{CSL}**	**1.15**		**2.85**
CSB output set time	**t_{CLL}**	**3.34**		
REB access time	**t_{REC}**			**2.68**
REB output hold time	**t_{REL}**	**0.85**		**2.16**
REB output set time	**t_{RLL}**	**1.11**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.47**		
CSB-WEB reset time	**t_{CWR}**	**4.18**		
Write pulse width	**t_{WP}**	**4.18**		
Address setup time	**t_{AS}**	**1.92**		
Address hold time	**t_{AH}**	**1.37**		
Input data setup time	**t_{DS}**	**3.62**		
Input data hold time	**t_{DH}**	**0.97**		
WEB access time	**t_{WEC}**			**7.39**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCH	**512 words × 16 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	24.7
H17	AD0	2.4	N17	TOUT	26.0
:	:	:			
H25	AD8	2.4			
H26	WEB	2.4			
H27	REB	1.0			
H28	CSB	2.4			
H29	TIN	2.4			
H30	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD8	(LH)	1.71	5.06	10.53
→DO0 to DO15	(HH)	1.60	4.97	10.45
	(HL)	1.55	4.75	9.96
	(LL)	1.50	4.74	10.03
CSB	(LL)	1.44	4.55	9.61
→DO0 to DO15	(LH)	1.44	4.55	9.61
	(HL)	1.35	2.36	4.00
REB	(LH)	1.18	1.94	3.20
→DO0 to DO15	(HL)	1.02	1.80	3.06
DI0 to DI15	(HH)	2.18	4.00	6.97
→DO0 to DO15	(LL)	2.03	3.73	6.51

Equivalent Cells	24114	Power (mW/MHz)		Rev.	1

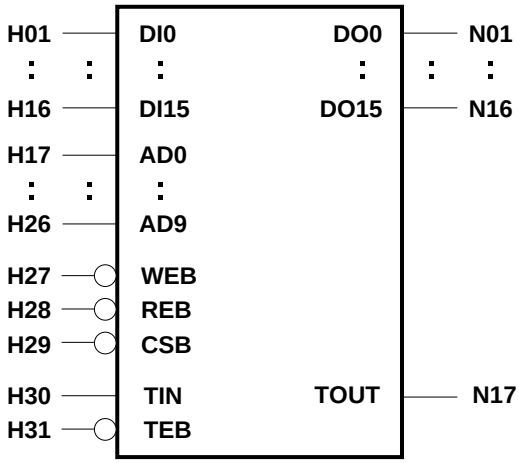
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.53**		
Address access time	**t_{ACA}**			**10.53**
Address output hold time	**t_{OH}**	**1.73**		
CSB access time	**t_{CSC}**			**9.62**
CSB output hold time	**t_{CSL}**	**1.56**		**4.00**
CSB output set time	**t_{CLL}**	**4.33**		
REB access time	**t_{REC}**			**3.20**
REB output hold time	**t_{REL}**	**1.18**		**3.07**
REB output set time	**t_{RLL}**	**1.36**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.64**		
CSB-WEB reset time	**t_{CWR}**	**4.23**		
Write pulse width	**t_{WP}**	**4.23**		
Address setup time	**t_{AS}**	**1.83**		
Address hold time	**t_{AH}**	**0.58**		
Input data setup time	**t_{DS}**	**3.51**		
Input data hold time	**t_{DH}**	**0.97**		
WEB access time	**t_{WEC}**			**7.96**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCM	**1K words × 16 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	AD0	2.4	N17	TOUT	26.0
:	:	:			
H26	AD9	2.4			
H27	WEB	2.4			
H28	REB	1.0			
H29	CSB	1.0			
H30	TIN	2.4			
H31	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD9	(LH)	2.94	7.05	13.76
→DO0 to DO15	(HH)	2.92	7.02	13.72
	(HL)	2.39	6.42	12.99
	(LL)	2.40	6.45	13.04
CSB	(LL)	1.20	4.82	10.73
→DO0 to DO15	(LH)	1.20	4.82	10.73
	(HL)	1.07	1.89	3.22
REB	(LH)	1.02	1.74	2.91
→DO0 to DO15	(HL)	0.76	1.37	2.38
DI0 to DI15	(HH)	2.94	5.58	9.88
→DO0 to DO15	(LL)	2.61	4.86	8.52

Equivalent Cells	44017	Power (mW/MHz)		Rev.	1

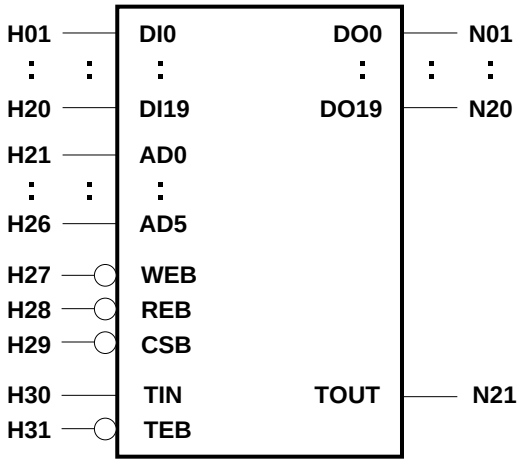
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**13.77**		
Address access time	**t_{ACA}**			**13.77**
Address output hold time	**t_{OH}**	**2.76**		
CSB access time	**t_{CSC}**			**10.73**
CSB output hold time	**t_{CSL}**	**1.23**		**3.22**
CSB output set time	**t_{CLL}**	**3.60**		
REB access time	**t_{REC}**			**2.91**
REB output hold time	**t_{REL}**	**0.87**		**2.39**
REB output set time	**t_{RLL}**	**1.18**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.36**		
CSB-WEB reset time	**t_{CWR}**	**4.86**		
Write pulse width	**t_{WP}**	**4.86**		
Address setup time	**t_{AS}**	**2.62**		
Address hold time	**t_{AH}**	**0.88**		
Input data setup time	**t_{DS}**	**5.20**		
Input data hold time	**t_{DH}**	**0.81**		
WEB access time	**t_{WEC}**			**9.87**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBEB	**64 words × 20 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H20	DI19	2.4	N20	DO19	23.7
H21	AD0	2.4	N21	TOUT	26.0
:	:	:			
H26	AD5	2.4			
H27	WEB	2.4			
H28	REB	1.0			
H29	CSB	1.0			
H30	TIN	2.4			
H31	TEB	5.0			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
AD0 to AD5	(LH)	2.92	4.83	7.93
→DO0 to DO19	(HH)	2.91	4.80	7.86
	(HL)	2.46	4.35	7.43
	(LL)	2.47	4.37	7.48
CSB	(LL)	2.34	4.36	7.66
→DO0 to DO19	(LH)	2.34	4.36	7.66
	(HL)	1.10	1.80	2.94
REB	(LH)	0.82	1.35	2.20
→DO0 to DO19	(HL)	0.84	1.32	2.11
DI0 to DI19	(HH)	1.75	3.21	5.61
→DO0 to DO19	(LL)	1.61	2.93	5.07

Equivalent Cells	5286	Power (mW/MHz)		Rev.	1

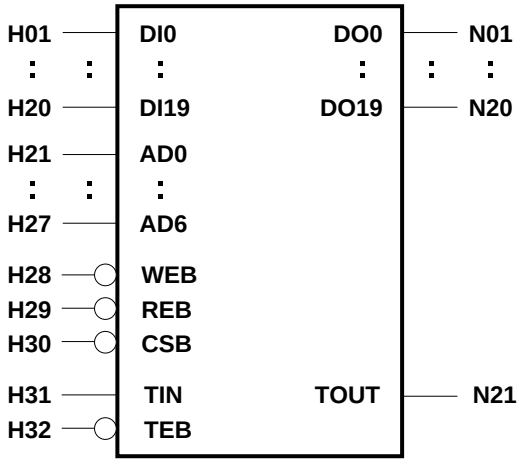
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.93**		
Address access time	**t_{ACA}**			**7.93**
Address output hold time	**t_{OH}**	**2.46**		
CSB access time	**t_{CSC}**			**7.67**
CSB output hold time	**t_{CSL}**	**1.11**		**2.95**
CSB output set time	**t_{CLL}**	**2.35**		
REB access time	**t_{REC}**			**2.21**
REB output hold time	**t_{REL}**	**0.85**		**2.12**
REB output set time	**t_{RLL}**	**0.82**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.10**		
CSB-WEB reset time	**t_{CWR}**	**3.78**		
Write pulse width	**t_{WP}**	**3.78**		
Address setup time	**t_{AS}**	**2.06**		
Address hold time	**t_{AH}**	**0.26**		
Input data setup time	**t_{DS}**	**2.42**		
Input data hold time	**t_{DH}**	**0.83**		
WEB access time	**t_{WEC}**			**4.83**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBED	**128 words × 20 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)	2.95	5.30	9.13
:	:	:	:	:	:	→DO0 to DO19 (HH)	2.86	5.16	8.91
H20	DI19	2.4	N20	DO19	23.7	(HL)	1.68	4.23	8.39
H21	AD0	2.4	N21	TOUT	26.0	(LL)	1.57	4.22	8.54
:	:	:							
H27	AD6	2.4				CSB (LL)	2.69	4.90	8.52
H28	WEB	2.4				→DO0 to DO19 (LH)	2.69	4.90	8.52
H29	REB	1.0				(HL)	1.45	2.39	3.93
H30	CSB	1.0							
H31	TIN	2.4				REB (LH)	1.09	1.76	2.85
H32	TEB	2.5				→DO0 to DO19 (HL)	1.21	1.93	3.09
						DI0 to DI19 (HH)	1.99	3.57	6.15
						→DO0 to DO19 (LL)	1.97	3.48	5.95

Equivalent Cells	10220	Power (mW/MHz)		Rev.	1

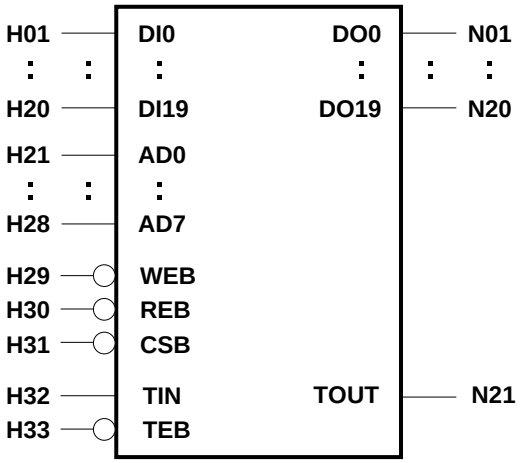
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.14**		
Address access time	**t_{ACA}**			**9.14**
Address output hold time	**t_{OH}**	**1.58**		
CSB access time	**t_{CSC}**			**8.52**
CSB output hold time	**t_{CSL}**	**1.45**		**3.94**
CSB output set time	**t_{CLL}**	**2.69**		
REB access time	**t_{REC}**			**2.85**
REB output hold time	**t_{REL}**	**1.22**		**3.09**
REB output set time	**t_{RLL}**	**1.09**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.56**		
CSB-WEB reset time	**t_{CWR}**	**4.09**		
Write pulse width	**t_{WP}**	**4.09**		
Address setup time	**t_{AS}**	**2.14**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**2.42**		
Input data hold time	**t_{DH}**	**0.95**		
WEB access time	**t_{WEC}**			**5.50**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBEF	**256 words × 20 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD7 (LH)	2.29	5.28	10.17
:	:	:	:	:	:	→DO0 to DO19 (HH)	2.28	5.26	10.11
H20	DI19	2.4	N20	DO19	23.7	(HL)	2.12	4.92	9.49
H21	AD0	2.4	N21	TOUT	26.0	(LL)	2.13	4.95	9.54
:	:	:							
H28	AD7	2.4				CSB (LL)	1.13	3.97	8.59
H29	WEB	2.4				→DO0 to DO19 (LH)	1.13	3.97	8.59
H30	REB	1.0				(HL)	1.01	1.75	2.96
H31	CSB	1.0							
H32	TIN	2.4				REB (LH)	0.98	1.64	2.71
H33	TEB	5.0				→DO0 to DO19 (HL)	0.76	1.33	2.27
						DI0 to DI19 (HH)	1.99	3.70	6.49
						→DO0 to DO19 (LL)	1.75	3.23	5.65

Equivalent Cells	15104	Power (mW/MHz)		Rev.	1

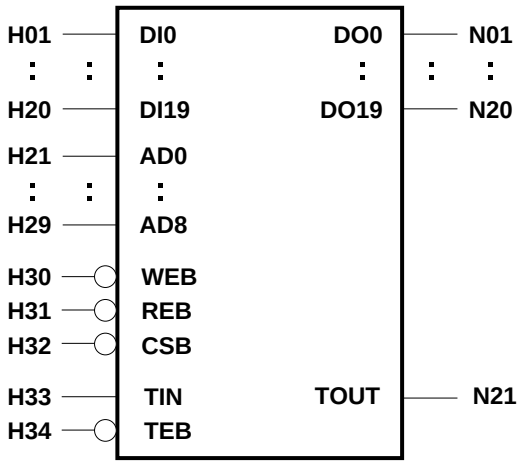
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.17**		
Address access time	**t_{ACA}**			**10.17**
Address output hold time	**t_{OH}**	**2.44**		
CSB access time	**t_{CSC}**			**8.59**
CSB output hold time	**t_{CSL}**	**1.16**		**2.97**
CSB output set time	**t_{CLL}**	**3.41**		
REB access time	**t_{REC}**			**2.71**
REB output hold time	**t_{REL}**	**0.87**		**2.28**
REB output set time	**t_{RLL}**	**1.13**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.71**		
CSB-WEB reset time	**t_{CWR}**	**4.44**		
Write pulse width	**t_{WP}**	**4.44**		
Address setup time	**t_{AS}**	**1.90**		
Address hold time	**t_{AH}**	**1.37**		
Input data setup time	**t_{DS}**	**3.57**		
Input data hold time	**t_{DH}**	**1.03**		
WEB access time	**t_{WEC}**			**7.34**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBEH	**512 words × 20 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H20	DI19	2.4	N20	DO19	24.7
H21	AD0	2.4	N21	TOUT	26.0
:	:	:			
H29	AD8	2.4			
H30	WEB	2.4			
H31	REB	1.0			
H32	CSB	2.4			
H33	TIN	2.4			
H34	TEB	5.0			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
AD0 to AD8	(LH)	1.72	5.14	10.72
→DO0 to DO19	(HH)	1.63	5.06	10.65
	(HL)	1.56	4.92	10.41
	(LL)	1.50	4.91	10.48
CSB	(LL)	1.46	4.52	9.50
→DO0 to DO19	(LH)	1.46	4.52	9.50
	(HL)	1.36	2.41	4.12
REB	(LH)	1.20	1.97	3.23
→DO0 to DO19	(HL)	1.05	1.86	3.18
DI0 to DI19	(HH)	2.18	4.00	6.97
→DO0 to DO19	(LL)	2.03	3.73	6.51

Equivalent Cells	29778	Power (mW/MHz)		Rev.	1

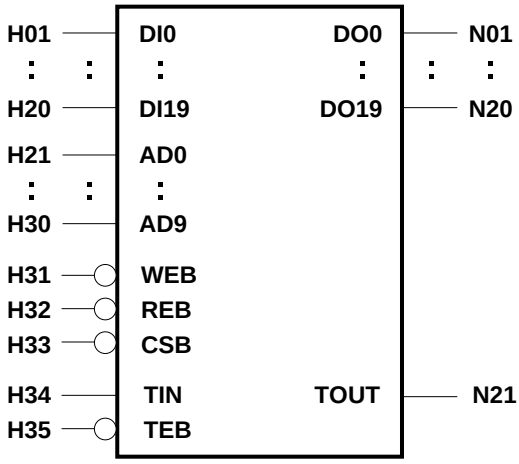
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.72**		
Address access time	**t_{ACA}**			**10.72**
Address output hold time	**t_{OH}**	**1.74**		
CSB access time	**t_{CSC}**			**9.51**
CSB output hold time	**t_{CSL}**	**1.58**		**4.13**
CSB output set time	**t_{CLL}**	**4.39**		
REB access time	**t_{REC}**			**3.24**
REB output hold time	**t_{REL}**	**1.21**		**3.18**
REB output set time	**t_{RLL}**	**1.39**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.89**		
CSB-WEB reset time	**t_{CWR}**	**4.49**		
Write pulse width	**t_{WP}**	**4.49**		
Address setup time	**t_{AS}**	**1.82**		
Address hold time	**t_{AH}**	**0.58**		
Input data setup time	**t_{DS}**	**3.45**		
Input data hold time	**t_{DH}**	**1.02**		
WEB access time	**t_{WEC}**			**7.91**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBEM	**1K words × 20 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD9 (LH)	3.06	7.44	14.58
:	:	:	:	:	:	→DO0 to DO19 (HH)	3.05	7.42	14.54
H20	DI19	2.4	N20	DO19	23.7	(HL)	2.39	6.73	13.81
H21	AD0	2.4	N21	TOUT	26.0	(LL)	2.40	6.76	13.87
:	:	:							
H30	AD9	2.4				CSB (LL)	1.23	5.05	11.29
H31	WEB	2.4				→DO0 to DO19 (LH)	1.23	5.05	11.29
H32	REB	1.0				(HL)	1.08	1.93	3.31
H33	CSB	1.0							
H34	TIN	2.4				REB (LH)	1.03	1.77	2.96
H35	TEB	5.0				→DO0 to DO19 (HL)	0.79	1.42	2.45
						DI0 to DI19 (HH)	2.94	5.58	9.88
						→DO0 to DO19 (LL)	2.61	4.81	8.39

Equivalent Cells	54541	Power (mW/MHz)		Rev.	1

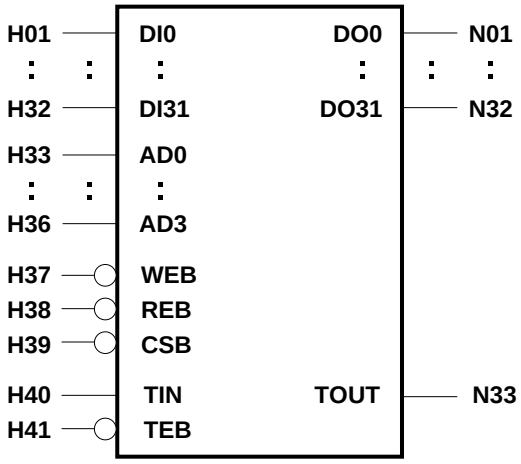
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**14.59**		
Address access time	**t_{ACA}**			**14.59**
Address output hold time	**t_{OH}**	**2.76**		
CSB access time	**t_{CSC}**			**11.29**
CSB output hold time	**t_{CSL}**	**1.25**		**3.31**
CSB output set time	**t_{CLL}**	**3.67**		
REB access time	**t_{REC}**			**2.97**
REB output hold time	**t_{REL}**	**0.91**		**2.45**
REB output set time	**t_{RLL}**	**1.20**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.93**		
CSB-WEB reset time	**t_{CWR}**	**5.06**		
Write pulse width	**t_{WP}**	**5.06**		
Address setup time	**t_{AS}**	**2.95**		
Address hold time	**t_{AH}**	**0.92**		
Input data setup time	**t_{DS}**	**5.15**		
Input data hold time	**t_{DH}**	**0.92**		
WEB access time	**t_{WEC}**			**9.58**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBH7	**16 words × 32 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	23.7
H33	AD0	2.4	N33	TOUT	26.0
:	:	:			
H36	AD3	2.4			
H37	WEB	2.4			
H38	REB	1.0			
H39	CSB	1.0			
H40	TIN	2.4			
H41	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD3	(LH)	2.65	4.34	7.09
→DO0 to DO31	(HH)	2.55	4.16	6.77
	(HL)	2.28	4.05	6.93
	(LL)	2.37	4.23	7.27
CSB	(LL)	2.26	3.81	6.35
→DO0 to DO31	(LH)	2.26	3.81	6.35
	(HL)	1.02	1.55	2.43
REB	(LH)	1.01	1.63	2.64
→DO0 to DO31	(HL)	1.11	1.68	2.61
DI0 to DI31	(HH)	1.86	3.21	5.42
→DO0 to DO31	(LL)	1.73	2.71	4.31

Equivalent Cells	3933	Power (mW/MHz)		Rev.	1

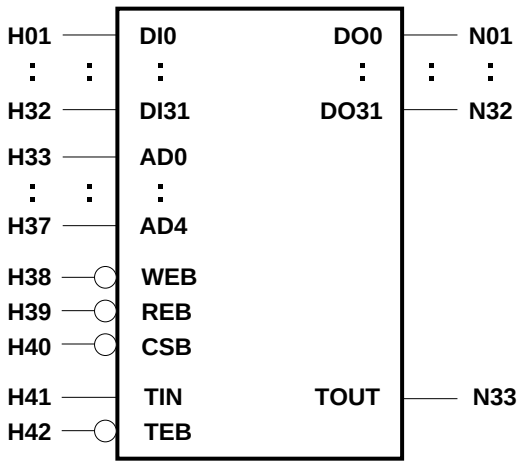
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.27**		
Address access time	**t_{ACA}**			**7.27**
Address output hold time	**t_{OH}**	**2.37**		
CSB access time	**t_{CSC}**			**6.36**
CSB output hold time	**t_{CSL}**	**1.26**		**3.27**
CSB output set time	**t_{CLL}**	**2.50**		
REB access time	**t_{REC}**			**2.64**
REB output hold time	**t_{REL}**	**1.11**		**2.61**
REB output set time	**t_{RLL}**	**1.01**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.72**		
CSB-WEB reset time	**t_{CWR}**	**4.60**		
Write pulse width	**t_{WP}**	**4.60**		
Address setup time	**t_{AS}**	**2.05**		
Address hold time	**t_{AH}**	**0.55**		
Input data setup time	**t_{DS}**	**3.02**		
Input data hold time	**t_{DH}**	**1.09**		
WEB access time	**t_{WEC}**			**6.31**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBH9	**32 words × 32 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	23.7
H33	AD0	2.4	N33	TOUT	26.0
:	:	:			
H37	AD4	2.4			
H38	WEB	2.4			
H39	REB	1.0			
H40	CSB	1.0			
H41	TIN	2.4			
H42	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD4	(LH)	2.98	4.87	7.95
→DO0 to DO31	(HH)	2.89	4.69	7.63
	(HL)	2.62	4.58	7.79
	(LL)	2.70	4.76	8.12
CSB	(LL)	2.51	4.29	7.20
→DO0 to DO31	(LH)	2.51	4.29	7.20
	(HL)	1.27	2.03	3.28
REB	(LH)	1.02	1.64	2.65
→DO0 to DO31	(HL)	1.12	1.69	2.62
DI0 to DI31	(HH)	1.86	3.26	5.53
→DO0 to DO31	(LL)	1.74	2.76	4.42

Equivalent Cells	5694	Power (mW/MHz)		Rev.	1

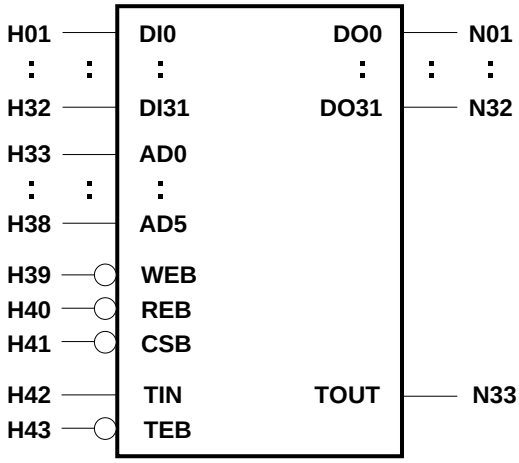
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.12**		
Address access time	**t_{ACA}**			**8.12**
Address output hold time	**t_{OH}**	**2.62**		
CSB access time	**t_{CSC}**			**7.21**
CSB output hold time	**t_{CSL}**	**1.27**		**3.28**
CSB output set time	**t_{CLL}**	**2.51**		
REB access time	**t_{REC}**			**2.65**
REB output hold time	**t_{REL}**	**1.12**		**2.62**
REB output set time	**t_{RLL}**	**1.02**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.72**		
CSB-WEB reset time	**t_{CWR}**	**5.10**		
Write pulse width	**t_{WP}**	**5.10**		
Address setup time	**t_{AS}**	**2.06**		
Address hold time	**t_{AH}**	**0.56**		
Input data setup time	**t_{DS}**	**3.03**		
Input data hold time	**t_{DH}**	**1.10**		
WEB access time	**t_{WEC}**			**6.42**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBHB	**64 words × 32 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	23.7
H33	AD0	2.4	N33	TOUT	26.0
:	:	:			
H38	AD5	2.4			
H39	WEB	2.4			
H40	REB	1.0			
H41	CSB	1.0			
H42	TIN	2.4			
H43	TEB	2.5			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
AD0 to AD5	(LH)	3.05	4.73	7.47
→DO0 to DO31	(HH)	3.01	4.65	7.32
	(HL)	2.60	4.64	7.97
	(LL)	2.65	4.73	8.13
CSB	(LL)	2.47	4.44	7.65
→DO0 to DO31	(LH)	2.47	4.44	7.65
	(HL)	1.18	1.92	3.12
REB	(LH)	0.90	1.46	2.36
→DO0 to DO31	(HL)	0.92	1.45	2.31
DI0 to DI31	(HH)	1.75	3.22	5.62
→DO0 to DO31	(LL)	1.61	2.92	5.06

Equivalent Cells	8411	Power (mW/MHz)		Rev.	1

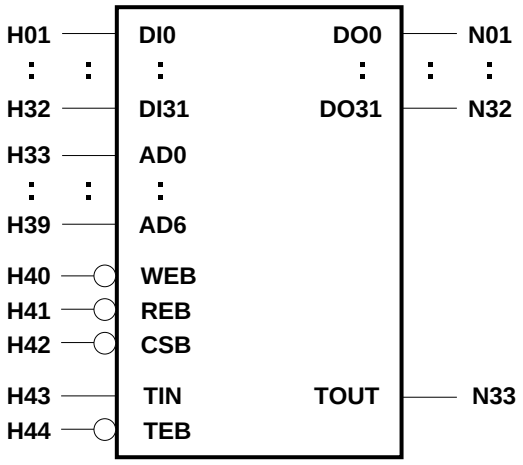
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.13**		
Address access time	**t_{ACA}**			**8.13**
Address output hold time	**t_{OH}**	**2.60**		
CSB access time	**t_{CSC}**			**7.65**
CSB output hold time	**t_{CSL}**	**1.18**		**3.12**
CSB output set time	**t_{CLL}**	**2.47**		
REB access time	**t_{REC}**			**2.38**
REB output hold time	**t_{REL}**	**0.93**		**2.31**
REB output set time	**t_{RLL}**	**0.90**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.31**		
CSB-WEB reset time	**t_{CWR}**	**3.82**		
Write pulse width	**t_{WP}**	**3.82**		
Address setup time	**t_{AS}**	**3.16**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**2.47**		
Input data hold time	**t_{DH}**	**1.80**		
WEB access time	**t_{WEC}**			**5.17**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBHD	**128 words × 32 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)	2.12	4.68	8.86
:	:	:	:	:	:	→DO0 to DO31 (HH)	2.07	4.60	8.72
H32	DI31	2.4	N32	DO31	23.7	(HL)	1.89	4.42	8.56
H33	AD0	2.4	N33	TOUT	26.0	(LL)	1.93	4.51	8.71
:	:	:							
H39	AD6	2.4				CSB (LL)	1.10	3.63	7.75
H40	WEB	2.4				→DO0 to DO31 (LH)	1.10	3.63	7.75
H41	REB	1.0				(HL)	1.02	1.74	2.91
H42	CSB	1.0							
H43	TIN	2.4				REB (LH)	0.88	1.55	2.64
H44	TEB	5.0				→DO0 to DO31 (HL)	0.76	1.33	2.25
						DI0 to DI31 (HH)	1.85	3.46	6.09
						→DO0 to DO31 (LL)	1.64	2.99	5.20

Equivalent Cells	14311	Power (mW/MHz)		Rev.	1

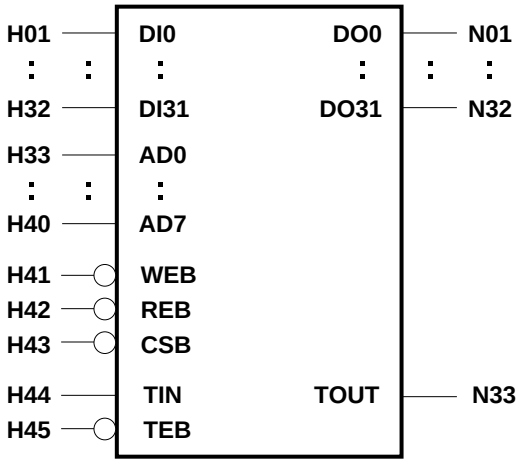
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.41**		
Address access time	**t_{ACA}**			**10.41**
Address output hold time	**t_{OH}**	**2.18**		
CSB access time	**t_{CSC}**			**7.75**
CSB output hold time	**t_{CSL}**	**1.18**		**2.91**
CSB output set time	**t_{CLL}**	**3.31**		
REB access time	**t_{REC}**			**2.64**
REB output hold time	**t_{REL}**	**0.88**		**2.25**
REB output set time	**t_{RLL}**	**1.02**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.81**		
CSB-WEB reset time	**t_{CWR}**	**3.88**		
Write pulse width	**t_{WP}**	**3.88**		
Address setup time	**t_{AS}**	**1.86**		
Address hold time	**t_{AH}**	**1.35**		
Input data setup time	**t_{DS}**	**3.32**		
Input data hold time	**t_{DH}**	**0.97**		
WEB access time	**t_{WEC}**			**6.13**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBHF	**256 words × 32 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	23.7
H33	AD0	2.4	N33	TOUT	26.0
:	:	:			
H40	AD7	2.4			
H41	WEB	2.4			
H42	REB	1.0			
H43	CSB	1.0			
H44	TIN	2.4			
H45	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD7	(LH)	2.38	5.30	10.06
→DO0 to DO31	(HH)	2.36	5.26	9.98
	(HL)	2.02	4.72	9.11
	(LL)	2.04	4.75	9.18
CSB	(LL)	1.13	4.03	8.74
→DO0 to DO31	(LH)	1.13	4.03	8.74
	(HL)	1.02	1.74	2.91
REB	(LH)	0.98	1.65	2.73
→DO0 to DO31	(HL)	0.76	1.31	2.21
DI0 to DI31	(HH)	1.99	3.70	6.49
→DO0 to DO31	(LL)	1.75	3.23	5.65

Equivalent Cells	24189	Power (mW/MHz)		Rev.	1

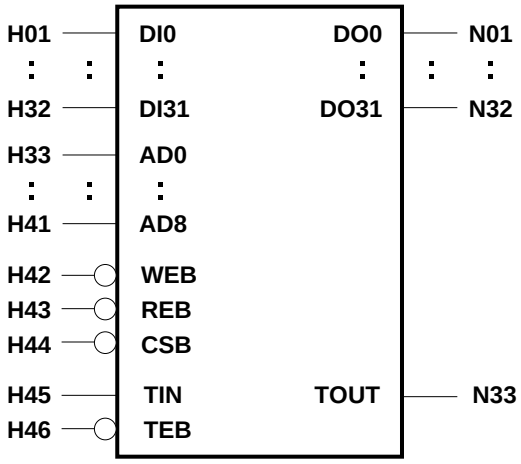
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.06**		
Address access time	**t_{ACA}**			**10.06**
Address output hold time	**t_{OH}**	**2.34**		
CSB access time	**t_{CSC}**			**8.75**
CSB output hold time	**t_{CSL}**	**1.18**		**2.91**
CSB output set time	**t_{CLL}**	**3.41**		
REB access time	**t_{REC}**			**2.73**
REB output hold time	**t_{REL}**	**0.87**		**2.21**
REB output set time	**t_{RLL}**	**1.13**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.55**		
CSB-WEB reset time	**t_{CWR}**	**4.23**		
Write pulse width	**t_{WP}**	**4.23**		
Address setup time	**t_{AS}**	**1.94**		
Address hold time	**t_{AH}**	**1.38**		
Input data setup time	**t_{DS}**	**3.58**		
Input data hold time	**t_{DH}**	**1.03**		
WEB access time	**t_{WEC}**			**6.66**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBHH	**512 words × 32 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7	AD0 to AD8 (LH)	1.74	5.15	10.72
:	:	:	:	:	:	→DO0 to DO31 (HH)	1.64	5.03	10.57
H32	DI31	2.4	N32	DO31	24.7	(HL)	1.57	4.80	10.07
H33	AD0	2.4	N33	TOUT	26.0	(LL)	1.52	4.83	10.22
:	:	:							
H41	AD8	2.4				CSB (LL)	1.48	4.60	9.69
H42	WEB	2.4				→DO0 to DO31 (LH)	1.48	4.60	9.69
H43	REB	1.0				(HL)	1.38	2.40	4.07
H44	CSB	2.4							
H45	TIN	2.4				REB (LH)	1.23	2.02	3.31
H46	TEB	5.0				→DO0 to DO31 (HL)	1.07	1.87	3.18
						DI0 to DI31 (HH)	2.18	4.00	6.97
						→DO0 to DO31 (LL)	2.03	3.73	6.51

Equivalent Cells	47955	Power (mW/MHz)		Rev.	1

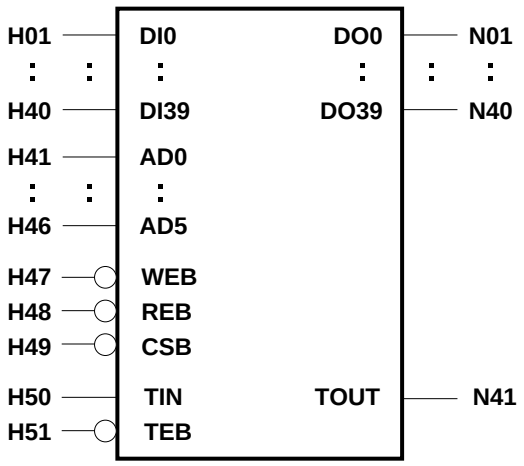
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.72**		
Address access time	**t_{ACA}**			**10.72**
Address output hold time	**t_{OH}**	**1.76**		
CSB access time	**t_{CSC}**			**9.70**
CSB output hold time	**t_{CSL}**	**1.59**		**4.07**
CSB output set time	**t_{CLL}**	**4.43**		
REB access time	**t_{REC}**			**3.31**
REB output hold time	**t_{REL}**	**1.23**		**3.18**
REB output set time	**t_{RLL}**	**1.41**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.79**		
CSB-WEB reset time	**t_{CWR}**	**4.32**		
Write pulse width	**t_{WP}**	**4.32**		
Address setup time	**t_{AS}**	**1.89**		
Address hold time	**t_{AH}**	**0.58**		
Input data setup time	**t_{DS}**	**3.43**		
Input data hold time	**t_{DH}**	**1.03**		
WEB access time	**t_{WEC}**			**8.15**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBKB	**64 words × 40 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD5 (LH)	3.05	5.01	8.22
:	:	:	:	:	:	→DO0 to DO39 (HH)	3.01	4.93	8.06
H40	DI39	2.4	N40	DO39	23.7	(HL)	2.55	4.48	7.63
H41	AD0	2.4	N41	TOUT	26.0	(LL)	2.59	4.56	7.78
:	:	:							
H46	AD5	2.4				CSB (LL)	2.43	4.48	7.83
H47	WEB	2.4				→DO0 to DO39 (LH)	2.43	4.48	7.83
H48	REB	1.0				(HL)	1.20	1.95	3.17
H49	CSB	1.0							
H50	TIN	2.4				REB (LH)	0.90	1.46	2.36
H51	TEB	2.5				→DO0 to DO39 (HL)	0.94	1.47	2.33
						DI0 to DI39 (HH)	1.75	3.21	5.61
						→DO0 to DO39 (LL)	1.61	2.93	5.08

Equivalent Cells	10349	Power (mW/MHz)		Rev.	1

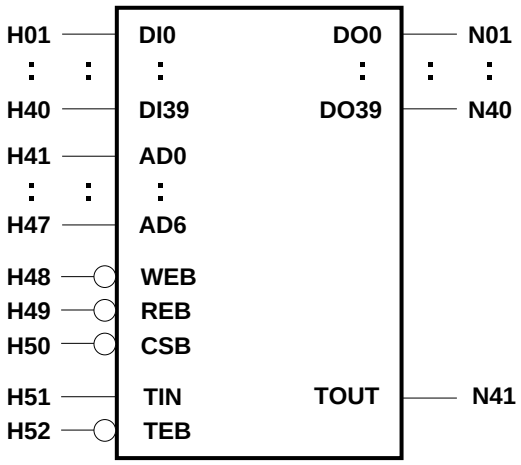
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.22**		
Address access time	**t_{ACA}**			**8.22**
Address output hold time	**t_{OH}**	**2.55**		
CSB access time	**t_{CSC}**			**7.83**
CSB output hold time	**t_{CSL}**	**1.20**		**3.18**
CSB output set time	**t_{CLL}**	**2.43**		
REB access time	**t_{REC}**			**2.38**
REB output hold time	**t_{REL}**	**0.94**		**2.33**
REB output set time	**t_{RLL}**	**0.90**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.86**		
CSB-WEB reset time	**t_{CWR}**	**4.09**		
Write pulse width	**t_{WP}**	**4.09**		
Address setup time	**t_{AS}**	**2.44**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**2.31**		
Input data hold time	**t_{DH}**	**1.03**		
WEB access time	**t_{WEC}**			**5.71**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBKD	**128 words × 40 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H40	DI39	2.4	N40	DO39	23.7
H41	AD0	2.4	N41	TOUT	26.0
:	:	:			
H47	AD6	2.4			
H48	WEB	2.4			
H49	REB	1.0			
H50	CSB	1.0			
H51	TIN	2.4			
H52	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD6	(LH)	3.07	5.50	9.47
→DO0 to DO39	(HH)	2.99	5.36	9.22
	(HL)	1.78	4.46	8.83
	(LL)	1.67	4.53	9.20
CSB	(LL)	2.81	5.10	8.83
→DO0 to DO39	(LH)	2.81	5.10	8.83
	(HL)	1.56	2.55	4.16
REB	(LH)	1.27	1.99	3.18
→DO0 to DO39	(HL)	1.41	2.22	3.53
DI0 to DI39	(HH)	1.99	3.57	6.15
→DO0 to DO39	(LL)	1.97	3.49	5.97

Equivalent Cells	20195	Power (mW/MHz)		Rev.	1

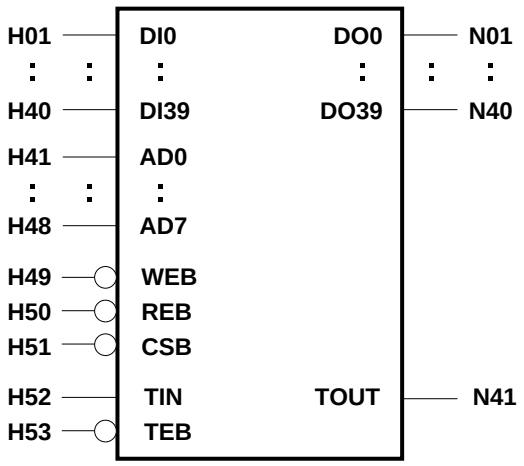
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.47**		
Address access time	**t_{ACA}**			**9.47**
Address output hold time	**t_{OH}**	**1.67**		
CSB access time	**t_{CSC}**			**8.84**
CSB output hold time	**t_{CSL}**	**1.56**		**4.16**
CSB output set time	**t_{CLL}**	**2.82**		
REB access time	**t_{REC}**			**3.18**
REB output hold time	**t_{REL}**	**1.41**		**3.54**
REB output set time	**t_{RLL}**	**1.27**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.91**		
CSB-WEB reset time	**t_{CWR}**	**4.39**		
Write pulse width	**t_{WP}**	**4.39**		
Address setup time	**t_{AS}**	**3.04**		
Address hold time	**t_{AH}**	**0.48**		
Input data setup time	**t_{DS}**	**2.32**		
Input data hold time	**t_{DH}**	**1.40**		
WEB access time	**t_{WEC}**			**6.08**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBKF	**256 words × 40 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD7 (LH)	2.33	5.34	10.25
:	:	:	:	:	:	→DO0 to DO39 (HH)	2.30	5.29	10.18
H40	DI39	2.4	N40	DO39	23.7	(HL)	2.14	4.96	9.57
H41	AD0	2.4	N41	TOUT	26.0	(LL)	2.16	5.00	9.63
:	:	:							
H48	AD7	2.4				CSB (LL)	1.16	4.00	8.63
H49	WEB	2.4				→DO0 to DO39 (LH)	1.16	4.00	8.63
H50	REB	1.0				(HL)	1.02	1.79	3.03
H51	CSB	1.0							
H52	TIN	2.4				REB (LH)	1.01	1.67	2.76
H53	TEB	5.0				→DO0 to DO39 (HL)	0.77	1.37	2.33
						DI0 to DI39 (HH)	1.99	3.70	6.49
						→DO0 to DO39 (LL)	1.75	3.23	5.65

Equivalent Cells	29884	Power (mW/MHz)		Rev.	1

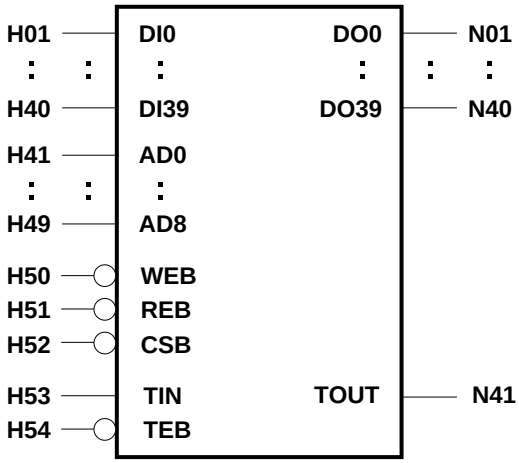
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.25**		
Address access time	**t_{ACA}**			**10.25**
Address output hold time	**t_{OH}**	**2.47**		
CSB access time	**t_{CSC}**			**8.65**
CSB output hold time	**t_{CSL}**	**1.18**		**3.04**
CSB output set time	**t_{CLL}**	**3.48**		
REB access time	**t_{REC}**			**2.77**
REB output hold time	**t_{REL}**	**0.90**		**2.33**
REB output set time	**t_{RLL}**	**1.16**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.80**		
CSB-WEB reset time	**t_{CWR}**	**4.49**		
Write pulse width	**t_{WP}**	**4.49**		
Address setup time	**t_{AS}**	**1.93**		
Address hold time	**t_{AH}**	**1.38**		
Input data setup time	**t_{DS}**	**3.52**		
Input data hold time	**t_{DH}**	**1.09**		
WEB access time	**t_{WEC}**			**6.61**

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBKH	**512 words × 40 bits Single-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H40	DI39	2.4	N40	DO39	24.7
H41	AD0	2.4	N41	TOUT	26.0
:	:	:			
H49	AD8	2.4			
H50	WEB	2.4			
H51	REB	1.0			
H52	CSB	2.4			
H53	TIN	2.4			
H54	TEB	5.0			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
AD0 to AD8	(LH)	1.76	5.24	10.91
→DO0 to DO39	(HH)	1.66	5.12	10.76
	(HL)	1.59	4.99	10.53
	(LL)	1.53	5.00	10.67
CSB	(LL)	1.50	4.57	9.59
→DO0 to DO39	(LH)	1.50	4.57	9.59
	(HL)	1.39	2.45	4.18
REB	(LH)	1.24	2.04	3.34
→DO0 to DO39	(HL)	1.09	1.93	3.30
DI0 to DI39	(HH)	2.18	4.00	6.97
→DO0 to DO39	(LL)	2.03	3.73	6.51

Equivalent Cells	49856	Power (mW/MHz)		Rev.	1

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.91**		
Address access time	**t_{ACA}**			**10.91**
Address output hold time	**t_{OH}**	**1.76**		
CSB access time	**t_{CSC}**			**9.60**
CSB output hold time	**t_{CSL}**	**1.60**		**4.19**
CSB output set time	**t_{CLL}**	**5.57**		
REB access time	**t_{REC}**			**3.35**
REB output hold time	**t_{REL}**	**1.26**		**3.30**
REB output set time	**t_{RLL}**	**1.44**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.05**		
CSB-WEB reset time	**t_{CWR}**	**4.59**		
Write pulse width	**t_{WP}**	**4.59**		
Address setup time	**t_{AS}**	**1.88**		
Address hold time	**t_{AH}**	**0.58**		
Input data setup time	**t_{DS}**	**3.38**		
Input data hold time	**t_{DH}**	**1.08**		
WEB access time	**t_{WEC}**			**8.10**

[MEMO]

CHAPTER 2

HIGH DENSITY

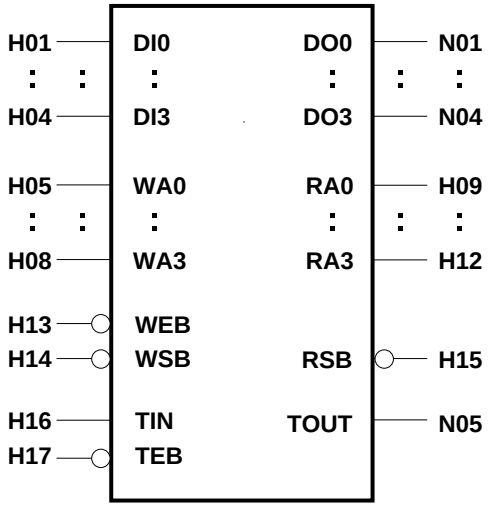
DUAL-PORT RAM BLOCK

(Soft Macro)

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R947	**16 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7				
:	:	:	:	:	:				
H04	DI3	2.4	N04	DO3	23.7	RA0 to RA3 (LH)	1.28	3.48	7.06
H05	WA0	2.4	N05	TOUT	26.0	→DO0 to DO3 (HH)	1.28	3.48	7.06
:	:	:				(HL)	2.20	4.12	7.26
H08	WA3	2.4				(LL)	2.20	4.12	7.26
H09	RA0	2.4							
:	:	:				RSB (LH)	0.61	1.00	1.65
H12	RA3	2.4				→DO0 to DO3 (HL)	0.70	1.05	1.64
H13	WEB	2.4							
H14	WSB	1.0				DI0 to DI3 (HH)	1.47	2.98	5.44
H15	RSB	1.0				→DO0 to DO3 (LL)	1.56	3.13	5.69
H16	TIN	2.4							
H17	TEB	2.5							

Equivalent Cells	883	Power (mW/MHz)		Rev.	1

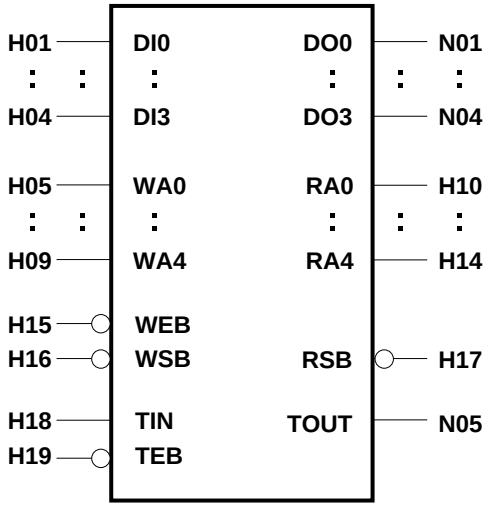
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.26**		
Address access time	**t_{ACA}**			**7.26**
Address output hold time	**t_{OH}**	**1.90**		
RSB access time	**t_{REC}**			**1.65**
RSB output hold time	**t_{REL}**	**0.70**		**2.20**
RSB output set time	**t_{RLL}**	**0.61**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.14**		
WSB-WEB reset time	**t_{CWR}**	**5.10**		
Write pulse width	**t_{WP}**	**5.10**		
Address setup time	**t_{AS}**	**2.83**		
Address hold time	**t_{AH}**	**0.21**		
Input data setup time	**t_{DS}**	**3.34**		
Input data hold time	**t_{DH}**	**0.31**		
WEB access time	**t_{WEC}**			**8.28**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R949	**32 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	23.7
H05	WA0	2.4	N05	TOUT	26.0
:	:	:			
H09	WA5	2.4			
H10	RA0	2.4			
:	:	:			
H14	RA5	2.4			
H15	WEB	2.4			
H16	WSB	1.0			
H17	RSB	1.0			
H18	TIN	2.4			
H19	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA5	(LH)	1.38	3.61	7.26
→DO0 to DO3	(HH)	1.38	3.61	7.26
	(HL)	2.30	4.26	7.46
	(LL)	2.30	4.26	7.46
RSB	(LH)	0.62	1.01	1.66
→DO0 to DO3	(HL)	0.71	1.06	1.65
DI0 to DI3	(HH)	1.48	3.02	5.54
→DO0 to DO3	(LL)	1.57	3.18	5.79

Equivalent Cells	1427	Power (mW/MHz)		Rev.	1

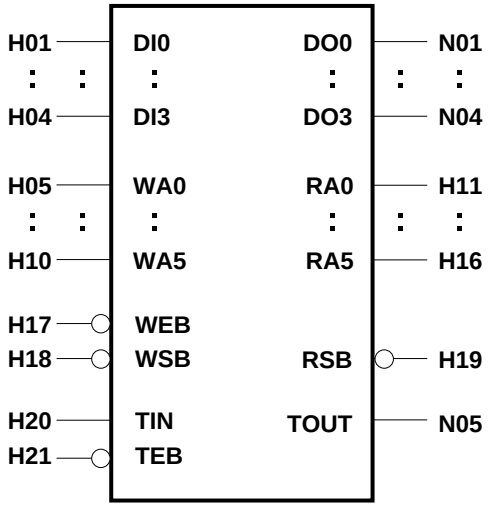
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.46**		
Address access time	**t_{ACA}**			**7.46**
Address output hold time	**t_{OH}**	**1.99**		
RSB access time	**t_{REC}**			**1.66**
RSB output hold time	**t_{REL}**	**0.71**		**2.21**
RSB output set time	**t_{RLL}**	**0.62**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.56**		
WSB-WEB reset time	**t_{CWR}**	**5.50**		
Write pulse width	**t_{WP}**	**5.50**		
Address setup time	**t_{AS}**	**2.84**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.35**		
Input data hold time	**t_{DH}**	**0.32**		
WEB access time	**t_{WEC}**			**8.38**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94B	**64 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	24.7
H05	WA0	2.4	N05	TOUT	26.0
:	:	:			
H10	WA5	2.4			
H11	RA0	2.4			
:	:	:			
H16	RA5	2.4			
H17	WEB	2.4			
H18	WSB	2.4			
H19	RSB	2.4			
H20	TIN	2.4			
H21	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA5	(LH)	0.54	3.22	7.60
→DO0 to DO3	(HH)	0.46	3.17	7.60
	(HL)	1.53	3.91	7.80
	(LL)	1.46	3.87	7.80
RSB	(LH)	0.89	1.38	2.18
→DO0 to DO3	(HL)	1.04	1.53	2.35
DI0 to DI3	(HH)	1.67	3.30	5.96
→DO0 to DO3	(LL)	1.86	3.61	6.45

Equivalent Cells	2636	Power (mW/MHz)		Rev.	1

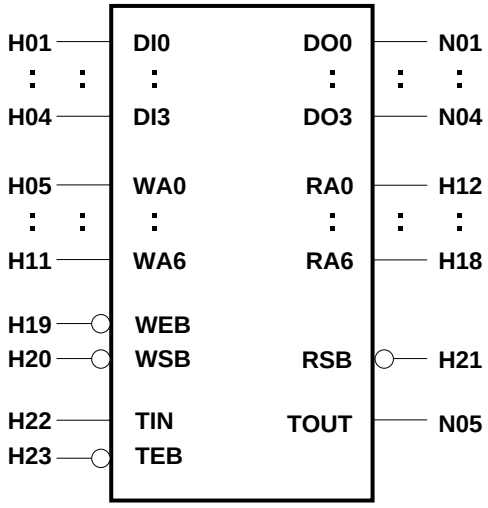
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.80**		
Address access time	**t_{ACA}**			**7.80**
Address output hold time	**t_{OH}**	**2.08**		
RSB access time	**t_{REC}**			**2.23**
RSB output hold time	**t_{REL}**	**1.04**		**2.36**
RSB output set time	**t_{RLL}**	**0.89**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.60**		
WSB-WEB reset time	**t_{CWR}**	**5.54**		
Write pulse width	**t_{WP}**	**5.54**		
Address setup time	**t_{AS}**	**2.74**		
Address hold time	**t_{AH}**	**0.32**		
Input data setup time	**t_{DS}**	**3.35**		
Input data hold time	**t_{DH}**	**0.42**		
WEB access time	**t_{WEC}**			**8.84**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94D	**128 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	23.7
H05	WA0	2.4	N05	TOUT	26.0
:	:	:			
H11	WA6	2.4			
H12	RA0	2.4			
:	:	:			
H18	RA6	2.4			
H19	WEB	2.4			
H20	WSB	1.0			
H21	RSB	1.0			
H22	TIN	2.4			
H23	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA6	(LH)	1.71	4.10	8.01
→DO0 to DO3	(HH)	1.71	4.10	8.01
	(HL)	2.58	4.72	8.21
	(LL)	2.58	4.72	8.21
RSB	(LH)	0.62	1.01	1.66
→DO0 to DO3	(HL)	0.71	1.06	1.65
DI0 to DI3	(HH)	1.77	3.48	6.28
→DO0 to DO3	(LL)	1.81	3.58	6.45

Equivalent Cells	4052	Power (mW/MHz)		Rev.	1

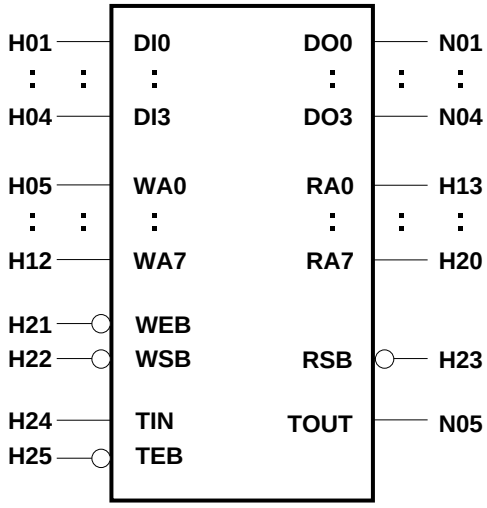
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.21**		
Address access time	**t_{ACA}**			**8.21**
Address output hold time	**t_{OH}**	**2.27**		
RSB access time	**t_{REC}**			**1.66**
RSB output hold time	**t_{REL}**	**0.71**		**1.65**
RSB output set time	**t_{RLL}**	**0.62**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.94**		
WSB-WEB reset time	**t_{CWR}**	**5.38**		
Write pulse width	**t_{WP}**	**5.38**		
Address setup time	**t_{AS}**	**3.34**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.35**		
Input data hold time	**t_{DH}**	**0.32**		
WEB access time	**t_{WEC}**			**9.08**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94F	**256 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	21.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	21.7
H05	WA0	2.4	N05	TOUT	26.0
:	:	:			
H12	WA7	2.4			
H13	RA0	2.4			
:	:	:			
H20	RA7	2.4			
H21	WEB	2.4			
H22	WSB	1.0			
H23	RSB	1.0			
H24	TIN	2.4			
H25	TEB	2.5			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
RA0 to RA7 →DO0 to DO3	(LH)	0.54	3.51	8.35
	(HH)	0.46	3.46	8.35
	(HL)	1.53	4.20	8.55
	(LL)	1.46	4.15	8.55
RSB →DO0 to DO3	(LH)	0.90	1.39	2.18
	(HL)	1.05	1.55	2.37
DI0 to DI3 →DO0 to DO3	(HH)	1.97	3.77	6.70
	(LL)	2.11	4.02	7.12

Equivalent Cells	7837	Power (mW/MHz)		Rev.	1

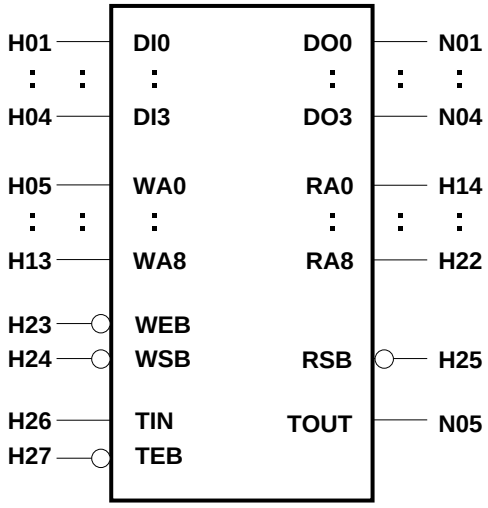
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.55**		
Address access time	**t_{ACA}**			**8.55**
Address output hold time	**t_{OH}**	**2.29**		
RSB access time	**t_{REC}**			**2.23**
RSB output hold time	**t_{REL}**	**1.05**		**2.37**
RSB output set time	**t_{RLL}**	**0.90**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.01**		
WSB-WEB reset time	**t_{CWR}**	**5.44**		
Write pulse width	**t_{WP}**	**5.44**		
Address setup time	**t_{AS}**	**3.24**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**3.36**		
Input data hold time	**t_{DH}**	**0.43**		
WEB access time	**t_{WEC}**			**9.55**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94H	**512 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	23.7
H05	WA0	2.4	N05	TOUT	26.0
:	:	:			
H13	WA8	2.4			
H14	RA0	2.4			
:	:	:			
H22	RA8	2.4			
H23	WEB	2.4			
H24	WSB	1.0			
H25	RSB	1.0			
H26	TIN	2.4			
H27	TEB	2.5			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
RA0 to RA8 →DO0 to DO3	(LH)	0.68	3.83	8.97
	(HH)	0.73	3.86	8.97
	(HL)	1.78	4.59	9.17
	(LL)	1.86	4.64	9.17
RSB →DO0 to DO3	(LH)	1.26	1.94	3.05
	(HL)	1.59	2.41	3.75
DI0 to DI3 →DO0 to DO3	(HH)	2.05	3.88	6.86
	(LL)	2.36	4.43	7.80

Equivalent Cells	15343	Power (mW/MHz)		Rev.	1

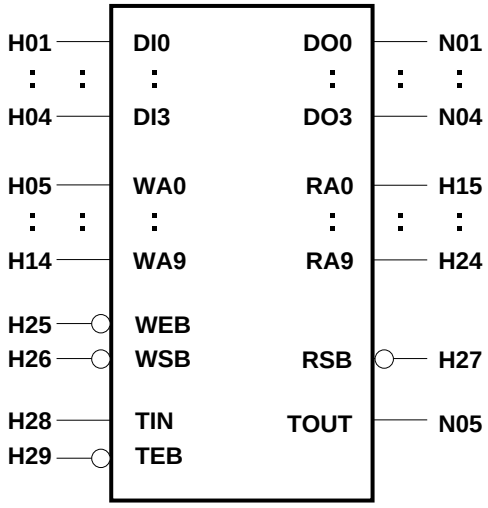
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.17**		
Address access time	**t_{ACA}**			**9.17**
Address output hold time	**t_{OH}**	**2.30**		
RSB access time	**t_{REC}**			**3.62**
RSB output hold time	**t_{REL}**	**1.59**		**3.76**
RSB output set time	**t_{RLL}**	**1.26**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.06**		
WSB-WEB reset time	**t_{CWR}**	**5.56**		
Write pulse width	**t_{WP}**	**5.56**		
Address setup time	**t_{AS}**	**3.32**		
Address hold time	**t_{AH}**	**1.18**		
Input data setup time	**t_{DS}**	**3.47**		
Input data hold time	**t_{DH}**	**1.28**		
WEB access time	**t_{WEC}**			**10.27**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94M	**1K words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	**DI0**	**2.4**	**N01**	**DO0**	**21.7**
:	**:**	**:**	**:**	**:**	**:**
H04	**DI3**	**2.4**	**N04**	**DO3**	**21.7**
H05	**WA0**	**2.4**	**N05**	**TOUT**	**26.0**
:	**:**	**:**			
H14	**WA9**	**2.4**			
H15	**RA0**	**2.4**			
:	**:**	**:**			
H24	**RA9**	**2.4**			
H25	**WEB**	**2.4**			
H26	**WSB**	**1.0**			
H27	**RSB**	**1.0**			
H28	**TIN**	**2.4**			
H29	**TEB**	**2.5**			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA9	**(LH)**	**0.96**	**4.13**	**9.31**
→DO0 to DO3	**(HH)**	**1.01**	**4.16**	**9.31**
	(HL)	**1.86**	**4.77**	**9.51**
	(LL)	**1.92**	**4.80**	**9.51**
RSB	**(LH)**	**1.59**	**2.46**	**3.89**
→DO0 to DO3	**(HL)**	**1.63**	**2.41**	**3.68**
DI0 to DI3	**(HH)**	**2.33**	**4.30**	**7.53**
→DO0 to DO3	**(LL)**	**2.54**	**4.71**	**8.25**

Equivalent Cells	**30396**	Power (mW/MHz)		**Rev.**	**1**

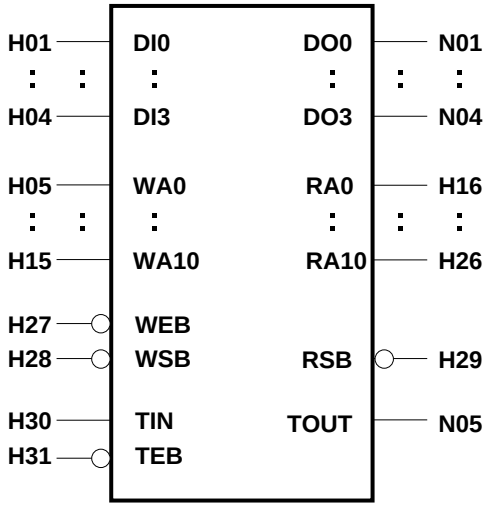
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.51**		
Address access time	**t_{ACA}**			**9.51**
Address output hold time	**t_{OH}**	**2.29**		
RSB access time	**t_{REC}**			**3.89**
RSB output hold time	**t_{REL}**	**1.63**		**3.69**
RSB output set time	**t_{RLL}**	**1.59**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.57**		
WSB-WEB reset time	**t_{CWR}**	**5.88**		
Write pulse width	**t_{WP}**	**5.88**		
Address setup time	**t_{AS}**	**3.47**		
Address hold time	**t_{AH}**	**1.22**		
Input data setup time	**t_{DS}**	**3.73**		
Input data hold time	**t_{DH}**	**1.32**		
WEB access time	**t_{WEC}**			**10.53**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94S	**2K words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	17.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	17.7
H05	WA0	2.4	N05	TOUT	26.0
:	:	:			
H15	WA10	2.4			
H16	RA0	2.4			
:	:	:			
H26	RA10	2.4			
H27	WEB	2.4			
H28	WSB	2.4			
H29	RSB	2.4			
H30	TIN	2.4			
H31	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA10	(LH)	1.20	4.41	9.65
→DO0 to DO3	(HH)	1.14	4.37	9.65
	(HL)	2.14	5.07	9.85
	(LL)	2.03	5.00	9.85
RSB	(LH)	1.76	2.67	4.17
→DO0 to DO3	(HL)	1.81	2.70	4.16
DI0 to DI3	(HH)	2.44	4.45	7.72
→DO0 to DO3	(LL)	2.70	5.00	8.74

Equivalent Cells	60537	Power (mW/MHz)		Rev.	1

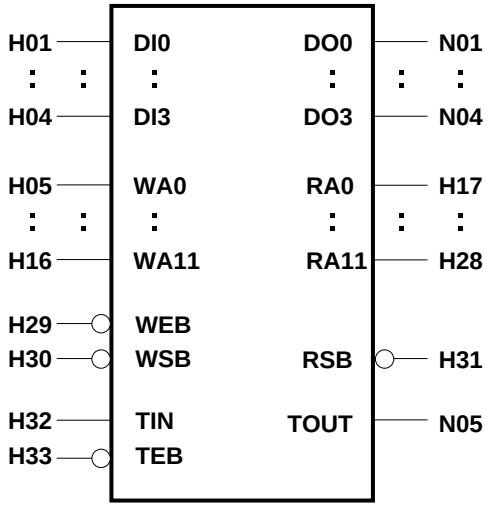
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.85**		
Address access time	**t_{ACA}**			**9.85**
Address output hold time	**t_{OH}**	**2.08**		
RSB access time	**t_{REC}**			**4.17**
RSB output hold time	**t_{REL}**	**1.81**		**4.16**
RSB output set time	**t_{RLL}**	**1.76**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.81**		
WSB-WEB reset time	**t_{CWR}**	**5.93**		
Write pulse width	**t_{WP}**	**5.93**		
Address setup time	**t_{AS}**	**3.53**		
Address hold time	**t_{AH}**	**1.35**		
Input data setup time	**t_{DS}**	**3.78**		
Input data hold time	**t_{DH}**	**1.45**		
WEB access time	**t_{WEC}**			**10.84**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94U	**4K words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	17.7
:	:	:	:	:	:
H04	DI3	2.4	N04	DO3	17.7
H05	WA0	2.4	N05	TOUT	26.0
:	:	:			
H16	WA11	2.4			
H17	RA0	2.4			
:	:	:			
H28	RA11	2.4			
H29	WEB	2.4			
H30	WSB	1.0			
H31	RSB	1.0			
H32	TIN	2.4			
H33	TEB	2.5			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
RA0 to RA11 →DO0 to DO3	(LH)	1.40	4.95	10.73
	(HH)	1.44	4.97	10.73
	(HL)	2.36	5.62	10.93
	(LL)	2.39	5.64	10.93
RSB →DO0 to DO3	(LH)	2.14	3.26	5.09
	(HL)	2.26	3.38	5.22
DI0 to DI3 →DO0 to DO3	(HH)	2.76	4.92	8.44
	(LL)	3.05	5.54	9.59

Equivalent Cells	120704	Power (mW/MHz)		Rev.	1

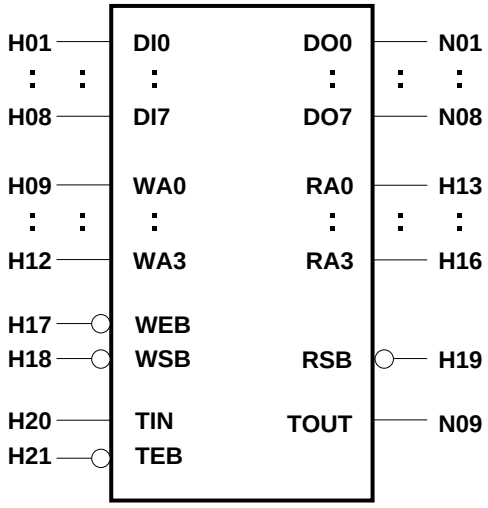
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.93**		
Address access time	**t_{ACA}**			**10.93**
Address output hold time	**t_{OH}**	**2.50**		
RSB access time	**t_{REC}**			**5.09**
RSB output hold time	**t_{REL}**	**2.26**		**5.23**
RSB output set time	**t_{RLL}**	**2.14**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**11.42**		
WSB-WEB reset time	**t_{CWR}**	**5.89**		
Write pulse width	**t_{WP}**	**5.89**		
Address setup time	**t_{AS}**	**3.73**		
Address hold time	**t_{AH}**	**1.80**		
Input data setup time	**t_{DS}**	**3.78**		
Input data hold time	**t_{DH}**	**1.90**		
WEB access time	**t_{WEC}**			**11.70**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R987	**16 words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	23.7
H09	WA0	2.4	N09	TOUT	26.0
:	:	:			
H12	WA3	2.4			
H13	RA0	2.4			
:	:	:			
H16	RA3	2.4			
H17	WEB	2.4			
H18	WSB	1.0			
H19	RSB	1.0			
H20	TIN	2.4			
H21	TEB	2.5			

Switching speed				
Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA3	(LH)	1.30	3.50	7.10
→DO0 to DO7	(HH)	1.30	3.50	7.10
	(HL)	2.21	4.14	7.30
	(LL)	2.22	4.15	7.30
RSB	(LH)	0.64	1.04	1.69
→DO0 to DO7	(HL)	0.72	1.08	1.68
DI0 to DI7	(HH)	1.47	2.98	5.44
→DO0 to DO7	(LL)	1.56	3.13	5.69

Equivalent Cells	1554	Power (mW/MHz)		Rev.	1

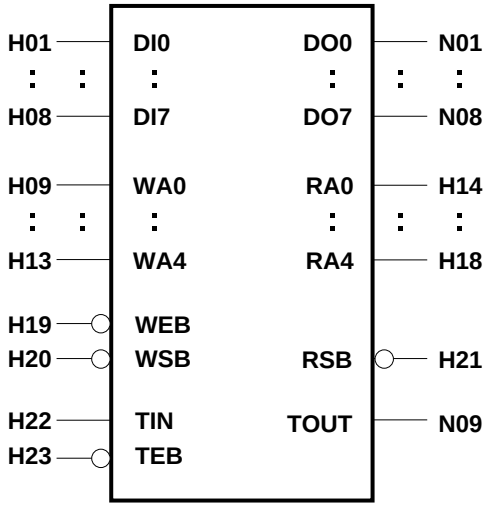
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.30**		
Address access time	**t_{ACA}**			**7.30**
Address output hold time	**t_{OH}**	**1.92**		
RSB access time	**t_{REC}**			**1.70**
RSB output hold time	**t_{REL}**	**0.73**		**1.69**
RSB output set time	**t_{RLL}**	**0.64**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.22**		
WSB-WEB reset time	**t_{CWR}**	**5.14**		
Write pulse width	**t_{WP}**	**5.14**		
Address setup time	**t_{AS}**	**2.86**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.29**		
Input data hold time	**t_{DH}**	**0.36**		
WEB access time	**t_{WEC}**			**8.34**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R989	**32 words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	23.7
H09	WA0	2.4	N09	TOUT	26.0
:	:	:			
H13	WA4	2.4			
H14	RA0	2.4			
:	:	:			
H18	RA4	2.4			
H19	WEB	2.4			
H20	WSB	1.0			
H21	RSB	1.0			
H22	TIN	2.4			
H23	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA4	(LH)	1.40	3.64	7.30
→DO0 to DO7	(HH)	1.40	3.64	7.30
	(HL)	2.31	4.28	7.50
	(LL)	2.32	4.29	7.50
RSB	(LH)	0.65	1.05	1.70
→DO0 to DO7	(HL)	0.73	1.09	1.69
DI0 to DI7	(HH)	1.48	3.02	5.54
→DO0 to DO7	(LL)	1.57	3.18	5.79

Equivalent Cells	2632	Power (mW/MHz)		Rev.	1

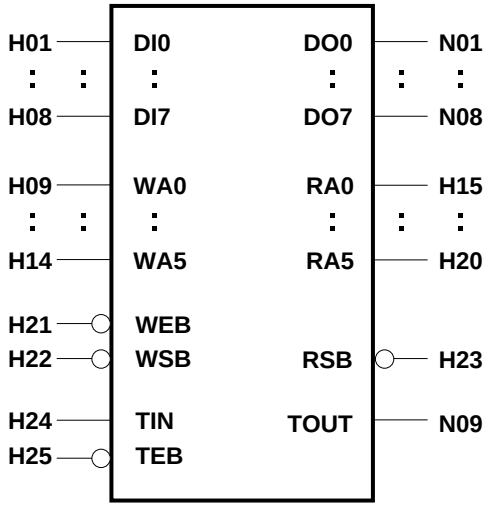
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.50**		
Address access time	**t_{ACA}**			**7.50**
Address output hold time	**t_{OH}**	**2.01**		
RSB access time	**t_{REC}**			**1.71**
RSB output hold time	**t_{REL}**	**0.73**		**1.70**
RSB output set time	**t_{RLL}**	**0.65**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.64**		
WSB-WEB reset time	**t_{CWR}**	**5.54**		
Write pulse width	**t_{WP}**	**5.54**		
Address setup time	**t_{AS}**	**2.87**		
Address hold time	**t_{AH}**	**0.23**		
Input data setup time	**t_{DS}**	**3.30**		
Input data hold time	**t_{DH}**	**0.37**		
WEB access time	**t_{WEC}**			**8.44**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R98B	**64 words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	23.7
H09	WA0	2.4	N09	TOUT	26.0
:	:	:			
H14	WA5	2.4			
H15	RA0	2.4			
:	:	:			
H20	RA5	2.4			
H21	WEB	2.4			
H22	WSB	1.0			
H23	RSB	1.0			
H24	TIN	2.4			
H25	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA5	(LH)	1.56	3.87	7.64
→DO0 to DO7	(HH)	1.56	3.87	7.64
	(HL)	2.47	4.51	7.84
	(LL)	2.47	4.51	7.84
RSB	(LH)	0.65	1.06	1.72
→DO0 to DO7	(HL)	0.75	1.12	1.72
DI0 to DI7	(HH)	1.61	3.23	5.88
→DO0 to DO7	(LL)	1.69	3.38	6.12

Equivalent Cells	3446	Power (mW/MHz)		Rev.	1

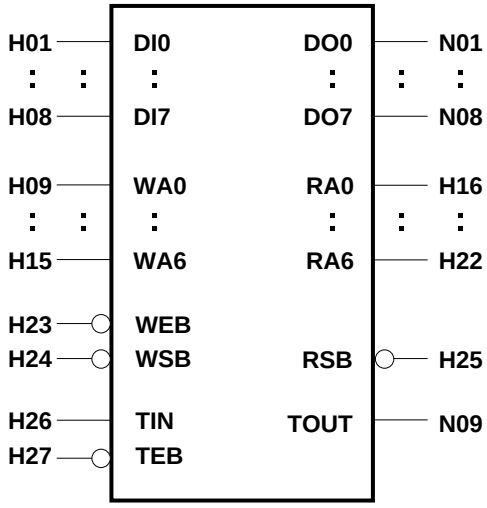
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.84**		
Address access time	**t_{ACA}**			**7.84**
Address output hold time	**t_{OH}**	**2.17**		
RSB access time	**t_{REC}**			**1.73**
RSB output hold time	**t_{REL}**	**0.75**		**1.73**
RSB output set time	**t_{RLL}**	**0.65**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.94**		
WSB-WEB reset time	**t_{CWR}**	**5.38**		
Write pulse width	**t_{WP}**	**5.38**		
Address setup time	**t_{AS}**	**2.34**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.25**		
Input data hold time	**t_{DH}**	**0.32**		
WEB access time	**t_{WEC}**			**8.81**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R98D	**128 words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7				
:	:	:	:	:	:				
H08	DI7	2.4	N08	DO7	24.7	RA0 to RA6 (LH)	0.56	3.38	7.98
H09	WA0	2.4	N09	TOUT	26.0	→DO0 to DO7 (HH)	0.48	3.33	7.98
:	:	:				(HL)	1.56	4.08	8.18
H15	WA6	2.4				(LL)	1.50	4.04	8.18
H16	RA0	2.4							
:	:	:				RSB (LH)	0.93	1.43	2.24
H22	RA6	2.4				→DO0 to DO7 (HL)	1.09	1.60	2.44
H23	WEB	2.4							
H24	WSB	2.4				DI0 to DI7 (HH)	1.81	3.52	6.30
H25	RSB	2.4				→DO0 to DO7 (LL)	1.99	3.82	6.79
H26	TIN	2.4							
H27	TEB	2.5							

Equivalent Cells	6613	Power (mW/MHz)		Rev.	1

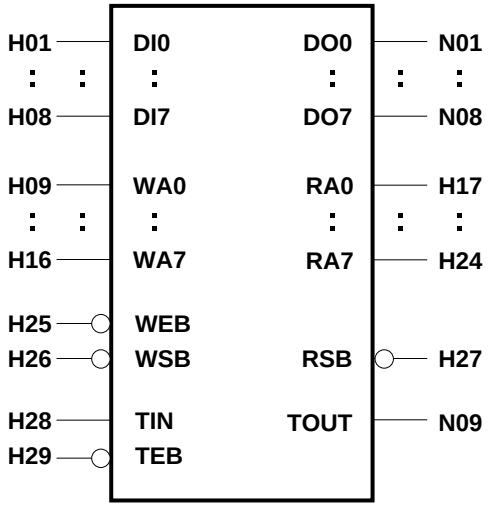
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.18**		
Address access time	**t_{ACA}**			**8.18**
Address output hold time	**t_{OH}**	**2.17**		
RSB access time	**t_{REC}**			**2.25**
RSB output hold time	**t_{REL}**	**1.09**		**2.45**
RSB output set time	**t_{RLL}**	**0.93**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.00**		
WSB-WEB reset time	**t_{CWR}**	**5.43**		
Write pulse width	**t_{WP}**	**5.43**		
Address setup time	**t_{AS}**	**2.24**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**3.26**		
Input data hold time	**t_{DH}**	**0.43**		
WEB access time	**t_{WEC}**			**9.28**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R98F	**256 words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	23.7
H09	WA0	2.4	N09	TOUT	26.0
:	:	:			
H16	WA7	2.4			
H17	RA0	2.4			
:	:	:			
H24	RA7	2.4			
H25	WEB	2.4			
H26	WSB	1.0			
H27	RSB	1.0			
H28	TIN	2.4			
H29	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA7	(LH)	2.16	4.75	8.98
→DO0 to DO7	(HH)	2.16	4.75	8.98
	(HL)	2.87	5.27	9.18
	(LL)	2.87	5.27	9.18
RSB	(LH)	0.67	1.08	1.74
→DO0 to DO7	(HL)	0.80	1.19	1.83
DI0 to DI7	(HH)	2.14	4.09	7.27
→DO0 to DO7	(LL)	2.06	3.99	7.14

Equivalent Cells	10369	Power (mW/MHz)		Rev.	1

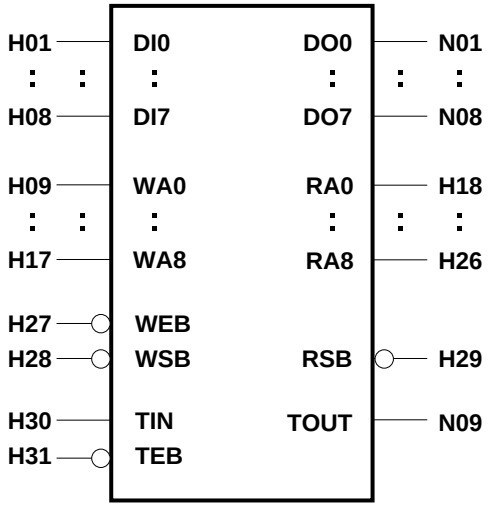
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.18**		
Address access time	**t_{ACA}**			**9.18**
Address output hold time	**t_{OH}**	**2.57**		
RSB access time	**t_{REC}**			**1.75**
RSB output hold time	**t_{REL}**	**0.80**		**1.83**
RSB output set time	**t_{RLL}**	**0.67**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.78**		
WSB-WEB reset time	**t_{CWR}**	**5.62**		
Write pulse width	**t_{WP}**	**5.62**		
Address setup time	**t_{AS}**	**3.94**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.45**		
Input data hold time	**t_{DH}**	**0.42**		
WEB access time	**t_{WEC}**			**10.10**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R98H	**512 words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	24.7
H09	WA0	2.4	N09	TOUT	26.0
:	:	:			
H17	WA8	2.4			
H18	RA0	2.4			
:	:	:			
H26	RA8	2.4			
H27	WEB	2.4			
H28	WSB	2.4			
H29	RSB	2.4			
H30	TIN	2.4			
H31	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA8	(LH)	0.60	3.91	9.32
→DO0 to DO7	(HH)	0.52	3.86	9.32
	(HL)	1.58	4.60	9.52
	(LL)	1.53	4.57	9.52
RSB	(LH)	0.97	1.47	2.30
→DO0 to DO7	(HL)	1.12	1.66	2.54
DI0 to DI7	(HH)	2.34	4.37	7.69
→DO0 to DO7	(LL)	2.36	4.44	7.82

Equivalent Cells	20418	Power (mW/MHz)		Rev.	1

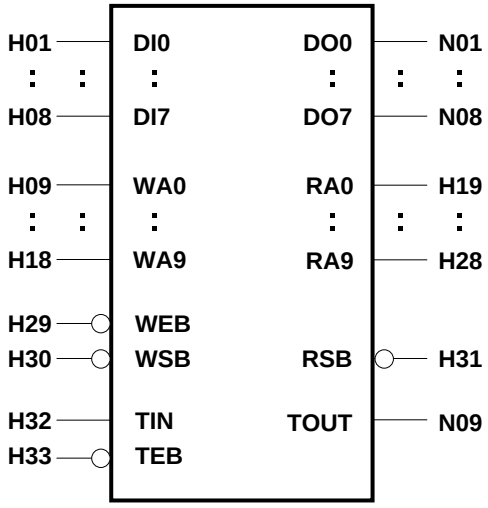
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.52**		
Address access time	**t_{ACA}**			**9.52**
Address output hold time	**t_{OH}**	**2.57**		
RSB access time	**t_{REC}**			**2.41**
RSB output hold time	**t_{REL}**	**1.12**		**2.55**
RSB output set time	**t_{RLL}**	**0.97**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.87**		
WSB-WEB reset time	**t_{CWR}**	**5.68**		
Write pulse width	**t_{WP}**	**5.68**		
Address setup time	**t_{AS}**	**3.85**		
Address hold time	**t_{AH}**	**0.34**		
Input data setup time	**t_{DS}**	**3.46**		
Input data hold time	**t_{DH}**	**0.54**		
WEB access time	**t_{WEC}**			**10.57**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R98M	**1K words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7				
:	:	:	:	:	:				
H08	DI7	2.4	N08	DO7	23.7				
H09	WA0	2.4	N09	TOUT	26.0				
:	:	:							
H18	WA9	2.4							
H19	RA0	2.4							
:	:	:							
H28	RA9	2.4							
H29	WEB	2.4							
H30	WSB	1.0							
H31	RSB	1.0							
H32	TIN	2.4							
H33	TEB	2.5							
						RA0 to RA9 (LH)	4.28	7.23	12.03
						→DO0 to DO7 (HH)	4.28	7.23	12.03
						(HL)	4.14	7.21	12.23
						(LL)	4.14	7.21	12.23
						RSB (LH)	0.74	1.17	1.87
						→DO0 to DO7 (HL)	0.90	1.31	2.00
						DI0 to DI7 (HH)	4.15	6.99	11.63
						→DO0 to DO7 (LL)	3.74	6.75	11.66

Equivalent Cells	37239	Power (mW/MHz)		Rev.	1

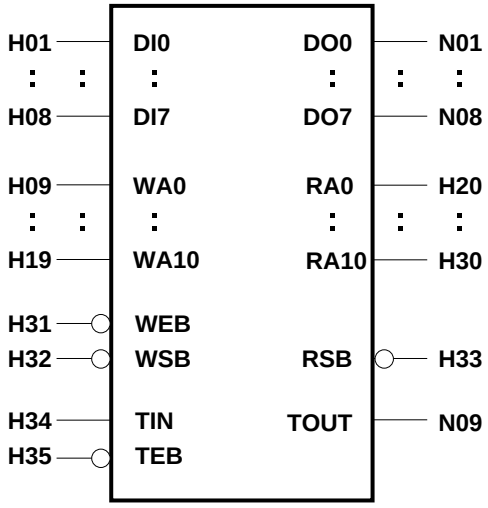
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.23**		
Address access time	**t_{ACA}**			**12.23**
Address output hold time	**t_{OH}**	**3.84**		
RSB access time	**t_{REC}**			**1.87**
RSB output hold time	**t_{REL}**	**0.90**		**2.00**
RSB output set time	**t_{RLL}**	**0.74**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.74**		
WSB-WEB reset time	**t_{CWR}**	**6.58**		
Write pulse width	**t_{WP}**	**6.58**		
Address setup time	**t_{AS}**	**5.94**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**4.05**		
Input data hold time	**t_{DH}**	**0.52**		
WEB access time	**t_{WEC}**			**14.40**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R98S	**2K words × 8 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H08	DI7	2.4	N08	DO7	24.7
H09	WA0	2.4	N09	TOUT	26.0
:	:	:			
H19	WA10	2.4			
H20	RA0	2.4			
:	:	:			
H30	RA10	2.4			
H31	WEB	2.4			
H32	WSB	2.4			
H33	RSB	2.4			
H34	TIN	2.4			
H35	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA10 →DO0 to DO7	(LH)	0.66	5.12	12.40
	(HH)	0.59	5.08	12.40
	(HL)	1.67	5.82	12.60
	(LL)	1.61	5.79	12.60
RSB →DO0 to DO7	(LH)	1.06	1.58	2.44
	(HL)	1.23	1.80	2.73
DI0 to DI7 →DO0 to DO7	(HH)	4.36	7.29	12.07
	(LL)	4.05	7.22	12.38

Equivalent Cells	74136	Power (mW/MHz)		Rev.	1

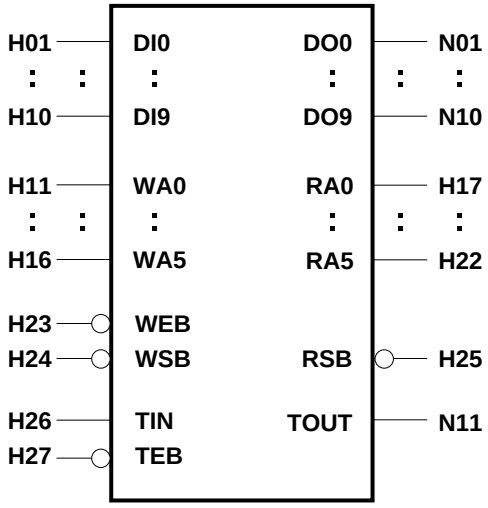
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.60**		
Address access time	**t_{ACA}**			**12.60**
Address output hold time	**t_{OH}**	**1.55**		
RSB access time	**t_{REC}**			**2.60**
RSB output hold time	**t_{REL}**	**1.23**		**2.74**
RSB output set time	**t_{RLL}**	**1.06**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.87**		
WSB-WEB reset time	**t_{CWR}**	**6.66**		
Write pulse width	**t_{WP}**	**6.66**		
Address setup time	**t_{AS}**	**5.86**		
Address hold time	**t_{AH}**	**0.35**		
Input data setup time	**t_{DS}**	**4.08**		
Input data hold time	**t_{DH}**	**0.65**		
WEB access time	**t_{WEC}**			**14.90**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AB	**64 words × 10 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	23.7
H11	WA0	2.4	N11	TOUT	26.0
:	:	:			
H16	WA5	2.4			
H17	RA0	2.4			
:	:	:			
H22	RA5	2.4			
H23	WEB	2.4			
H24	WSB	1.0			
H25	RSB	1.0			
H26	TIN	2.4			
H27	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA5	(LH)	1.56	3.88	7.67
→DO0 to DO9	(HH)	1.56	3.88	7.67
	(HL)	2.49	4.53	7.87
	(LL)	2.49	4.53	7.87
RSB	(LH)	0.66	1.07	1.75
→DO0 to DO9	(HL)	0.77	1.14	1.76
DI0 to DI9	(HH)	1.60	3.23	5.88
→DO0 to DO9	(LL)	1.69	3.38	6.13

Equivalent Cells	4187	Power (mW/MHz)		Rev.	1

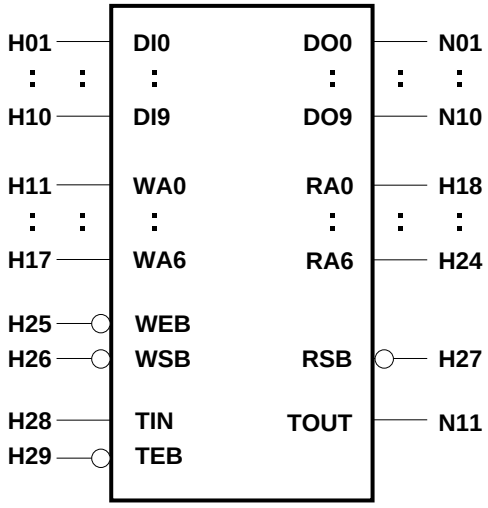
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.87**		
Address access time	**t_{ACA}**			**7.87**
Address output hold time	**t_{OH}**	**2.18**		
RSB access time	**t_{REC}**			**1.76**
RSB output hold time	**t_{REL}**	**0.77**		**1.77**
RSB output set time	**t_{RLL}**	**0.66**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.04**		
WSB-WEB reset time	**t_{CWR}**	**5.38**		
Write pulse width	**t_{WP}**	**5.38**		
Address setup time	**t_{AS}**	**2.44**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.25**		
Input data hold time	**t_{DH}**	**0.32**		
WEB access time	**t_{WEC}**			**8.85**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AD	**128 words × 10 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	**DI0**	**2.4**	**N01**	**DO0**	**24.7**
:	**:**	**:**	**:**	**:**	**:**
H10	**DI9**	**2.4**	**N10**	**DO9**	**24.7**
H11	**WA0**	**2.4**	**N11**	**TOUT**	**26.0**
:	**:**	**:**			
H17	**WA6**	**2.4**			
H18	**RA0**	**2.4**			
:	**:**	**:**			
H24	**RA6**	**2.4**			
H25	**WEB**	**2.4**			
H26	**WSB**	**2.4**			
H27	**RSB**	**2.4**			
H28	**TIN**	**2.4**			
H29	**TEB**	**2.5**			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA6	**(LH)**	**0.57**	**3.40**	**8.02**
→DO0 to DO9	**(HH)**	**0.49**	**3.35**	**8.02**
	(HL)	**1.58**	**4.10**	**8.22**
	(LL)	**1.51**	**4.06**	**8.22**
RSB	**(LH)**	**0.94**	**1.44**	**2.27**
→DO0 to DO9	**(HL)**	**1.11**	**1.63**	**2.49**
DI0 to DI9	**(HH)**	**1.80**	**3.51**	**6.30**
→DO0 to DO9	**(LL)**	**1.99**	**3.82**	**6.80**

Equivalent Cells	**8079**	Power (mW/MHz)		**Rev.**	**1**

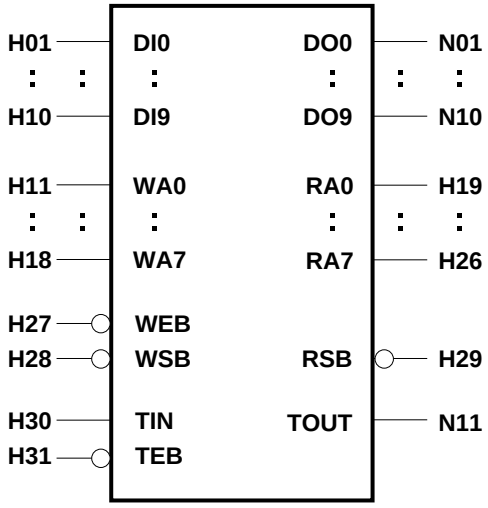
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.22**		
Address access time	**t_{ACA}**			**8.22**
Address output hold time	**t_{OH}**	**2.19**		
RSB access time	**t_{REC}**			**2.35**
RSB output hold time	**t_{REL}**	**1.11**		**2.49**
RSB output set time	**t_{RLL}**	**0.94**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.60**		
WSB-WEB reset time	**t_{CWR}**	**5.44**		
Write pulse width	**t_{WP}**	**5.44**		
Address setup time	**t_{AS}**	**3.94**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.45**		
Input data hold time	**t_{DH}**	**0.42**		
WEB access time	**t_{WEC}**			**10.16**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AF	**256 words × 10 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	23.7
H11	WA0	2.4	N11	TOUT	26.0
:	:	:			
H18	WA7	2.4			
H19	RA0	2.4			
:	:	:			
H26	RA7	2.4			
H27	WEB	2.4			
H28	WSB	1.0			
H29	RSB	1.0			
H30	TIN	2.4			
H31	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA7	(LH)	2.17	4.76	8.99
→DO0 to DO9	(HH)	2.17	4.76	8.99
	(HL)	2.91	5.30	9.19
	(LL)	2.91	5.30	9.19
RSB	(LH)	0.69	1.11	1.79
→DO0 to DO9	(HL)	0.84	1.24	1.90
DI0 to DI9	(HH)	2.14	4.09	7.27
→DO0 to DO9	(LL)	2.06	3.99	7.14

Equivalent Cells	12791	Power (mW/MHz)		Rev.	1

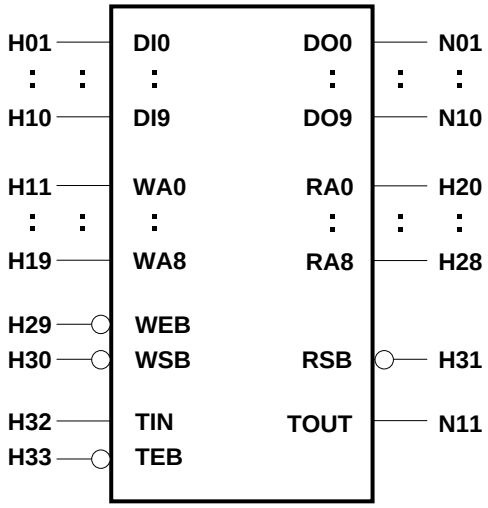
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.19**		
Address access time	**t_{ACA}**			**9.19**
Address output hold time	**t_{OH}**	**2.61**		
RSB access time	**t_{REC}**			**1.80**
RSB output hold time	**t_{REL}**	**1.11**		**1.90**
RSB output set time	**t_{RLL}**	**0.69**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.78**		
WSB-WEB reset time	**t_{CWR}**	**5.62**		
Write pulse width	**t_{WP}**	**5.62**		
Address setup time	**t_{AS}**	**3.94**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.45**		
Input data hold time	**t_{DH}**	**0.42**		
WEB access time	**t_{WEC}**			**10.16**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AH	**512 words × 10 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	24.7
H11	WA0	2.4	N11	TOUT	26.0
:	:	:			
H19	WA8	2.4			
H20	RA0	2.4			
:	:	:			
H28	RA8	2.4			
H29	WEB	2.4			
H30	WSB	2.4			
H31	RSB	2.4			
H32	TIN	2.4			
H33	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA8	(LH)	0.62	3.93	9.34
→DO0 to DO9	(HH)	0.53	3.88	9.34
	(HL)	1.62	4.63	9.54
	(LL)	1.56	4.59	9.54
RSB	(LH)	0.99	1.51	2.35
→DO0 to DO9	(HL)	1.16	1.71	2.61
DI0 to DI9	(HH)	2.34	4.37	7.69
→DO0 to DO9	(LL)	2.37	4.45	7.83

Equivalent Cells	25244	Power (mW/MHz)		Rev.	1

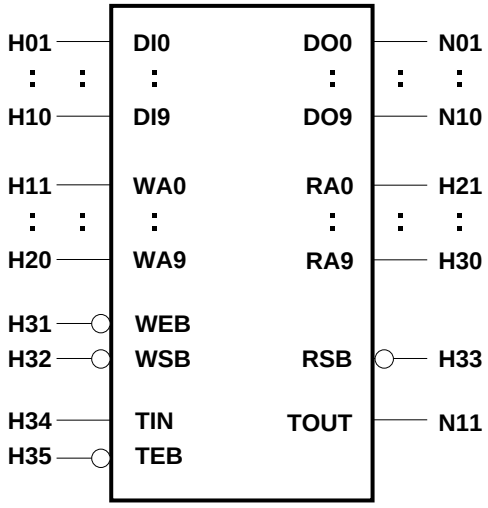
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.54**		
Address access time	**t_{ACA}**			**9.54**
Address output hold time	**t_{OH}**	**2.61**		
RSB access time	**t_{REC}**			**2.48**
RSB output hold time	**t_{REL}**	**1.16**		**2.62**
RSB output set time	**t_{RLL}**	**0.99**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.88**		
WSB-WEB reset time	**t_{CWR}**	**5.69**		
Write pulse width	**t_{WP}**	**5.69**		
Address setup time	**t_{AS}**	**3.85**		
Address hold time	**t_{AH}**	**0.34**		
Input data setup time	**t_{DS}**	**3.47**		
Input data hold time	**t_{DH}**	**0.54**		
WEB access time	**t_{WEC}**			**10.64**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AM	**1K words × 10 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	23.7
H11	WA0	2.4	N11	TOUT	26.0
:	:	:			
H20	WA9	2.4			
H21	RA0	2.4			
:	:	:			
H30	RA9	2.4			
H31	WEB	2.4			
H32	WSB	1.0			
H33	RSB	1.0			
H34	TIN	2.4			
H35	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA9	(LH)	4.39	7.29	12.03
→DO0 to DO9	(HH)	4.39	7.29	12.03
	(HL)	4.18	7.24	12.23
	(LL)	4.18	7.24	12.23
RSB	(LH)	0.79	1.22	1.93
→DO0 to DO9	(HL)	0.94	1.37	2.09
DI0 to DI9	(HH)	4.15	6.99	11.63
→DO0 to DO9	(LL)	3.74	6.75	11.66

Equivalent Cells	46281	Power (mW/MHz)		Rev.	1

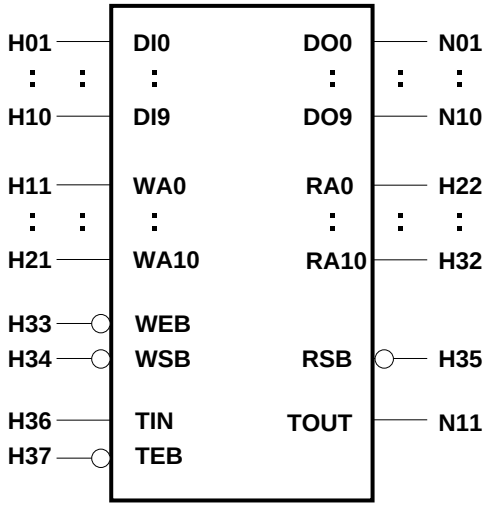
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.23**		
Address access time	**t_{ACA}**			**12.23**
Address output hold time	**t_{OH}**	**3.88**		
RSB access time	**t_{REC}**			**1.95**
RSB output hold time	**t_{REL}**	**0.94**		**2.09**
RSB output set time	**t_{RLL}**	**0.79**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.08**		
WSB-WEB reset time	**t_{CWR}**	**6.82**		
Write pulse width	**t_{WP}**	**6.82**		
Address setup time	**t_{AS}**	**6.04**		
Address hold time	**t_{AH}**	**0.22**		
Input data setup time	**t_{DS}**	**3.85**		
Input data hold time	**t_{DH}**	**0.52**		
WEB access time	**t_{WEC}**			**14.40**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AS	**2K words × 10 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H10	DI9	2.4	N10	DO9	24.7
H11	WA0	2.4	N11	TOUT	26.0
:	:	:			
H21	WA10	2.4			
H22	RA0	2.4			
:	:	:			
H32	RA10	2.4			
H33	WEB	2.4			
H34	WSB	2.4			
H35	RSB	2.4			
H36	TIN	2.4			
H37	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA10	(HH)	0.72	5.16	12.40
→DO0 to DO9	(LH)	0.64	5.11	12.40
	(LL)	1.70	5.84	12.60
	(HL)	1.65	5.81	12.60
RSB	(LH)	1.12	1.65	2.51
→DO0 to DO9	(HL)	1.27	1.86	2.84
DI0 to DI9	(HH)	4.37	7.29	12.07
→DO0 to DO9	(LL)	4.05	7.22	12.38

Equivalent Cells	92206	Power (mW/MHz)		Rev.	1

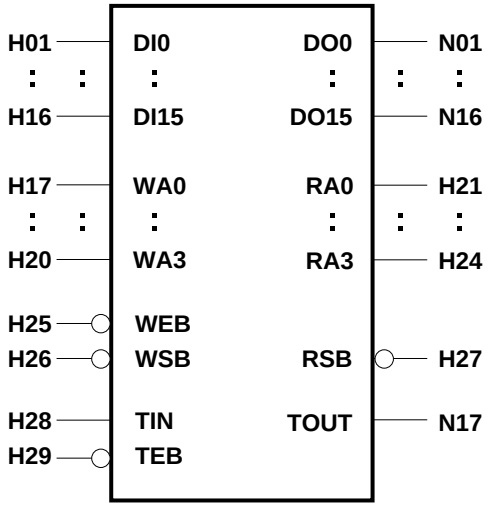
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.60**		
Address access time	**t_{ACA}**			**12.60**
Address output hold time	**t_{OH}**	**1.60**		
RSB access time	**t_{REC}**			**2.70**
RSB output hold time	**t_{REL}**	**1.27**		**2.84**
RSB output set time	**t_{RLL}**	**1.12**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.22**		
WSB-WEB reset time	**t_{CWR}**	**6.90**		
Write pulse width	**t_{WP}**	**6.90**		
Address setup time	**t_{AS}**	**5.96**		
Address hold time	**t_{AH}**	**0.36**		
Input data setup time	**t_{DS}**	**3.88**		
Input data hold time	**t_{DH}**	**0.66**		
WEB access time	**t_{WEC}**			**15.14**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9C7	**16 words × 16 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	WA0	2.4	N17	TOUT	26.0
:	:	:			
H20	WA3	2.4			
H21	RA0	2.4			
:	:	:			
H24	RA3	2.4			
H25	WEB	2.4			
H26	WSB	1.0			
H27	RSB	1.0			
H28	TIN	2.4			
H29	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA3	(LH)	1.36	3.59	7.22
→DO0 to DO15	(HH)	1.34	3.57	7.22
	(HL)	2.25	4.21	7.42
	(LL)	2.28	4.23	7.42
RSB	(LH)	0.69	1.10	1.78
→DO0 to DO15	(HL)	0.78	1.16	1.79
DI0 to DI15	(HH)	1.47	2.98	5.45
→DO0 to DO15	(LL)	1.56	3.14	5.70

Equivalent Cells	2902	Power (mW/MHz)		Rev.	1

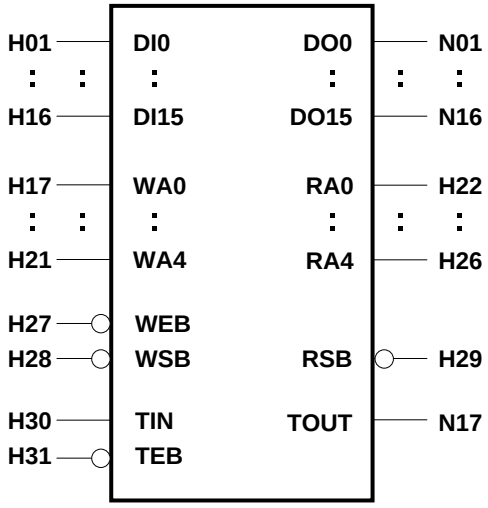
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.42**		
Address access time	**t_{ACA}**			**7.42**
Address output hold time	**t_{OH}**	**1.95**		
RSB access time	**t_{REC}**			**1.79**
RSB output hold time	**t_{REL}**	**0.78**		**1.79**
RSB output set time	**t_{RLL}**	**0.69**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.50**		
WSB-WEB reset time	**t_{CWR}**	**5.26**		
Write pulse width	**t_{WP}**	**5.26**		
Address setup time	**t_{AS}**	**2.97**		
Address hold time	**t_{AH}**	**0.27**		
Input data setup time	**t_{DS}**	**3.21**		
Input data hold time	**t_{DH}**	**0.49**		
WEB access time	**t_{WEC}**			**8.59**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9C9	**32 words × 16 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	WA0	2.4	N17	TOUT	26.0
:	:	:			
H21	WA4	2.4			
H22	RA0	2.4			
:	:	:			
H26	RA4	2.4			
H27	WEB	2.4			
H28	WSB	1.0			
H29	RSB	1.0			
H30	TIN	2.4			
H31	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA4	(LH)	1.46	3.72	7.42
→DO0 to DO15	(HH)	1.44	3.71	7.42
	(HL)	2.35	4.35	7.62
	(LL)	2.38	4.37	7.62
RSB	(LH)	0.70	1.11	1.79
→DO0 to DO15	(HL)	0.79	1.17	1.80
DI0 to DI15	(HH)	1.48	3.03	5.55
→DO0 to DO15	(LL)	1.57	3.18	5.80

Equivalent Cells	5036	Power (mW/MHz)		Rev.	1

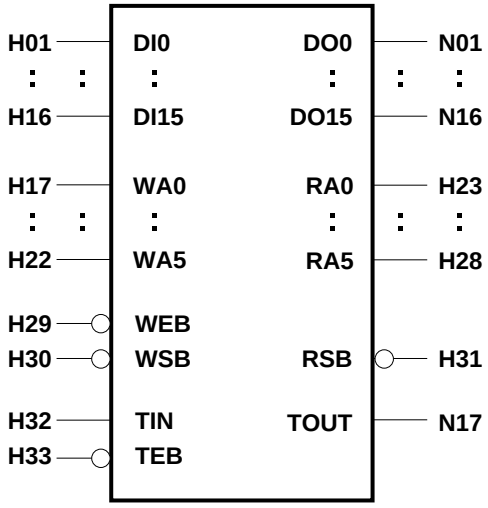
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.62**		
Address access time	**t_{ACA}**			**7.62**
Address output hold time	**t_{OH}**	**2.05**		
RSB access time	**t_{REC}**			**1.80**
RSB output hold time	**t_{REL}**	**0.79**		**1.80**
RSB output set time	**t_{RLL}**	**0.70**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.92**		
WSB-WEB reset time	**t_{CWR}**	**5.66**		
Write pulse width	**t_{WP}**	**5.66**		
Address setup time	**t_{AS}**	**2.98**		
Address hold time	**t_{AH}**	**0.28**		
Input data setup time	**t_{DS}**	**3.22**		
Input data hold time	**t_{DH}**	**0.50**		
WEB access time	**t_{WEC}**			**8.60**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9CB	**64 words × 16 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	WA0	2.4	N17	TOUT	26.0
:	:	:			
H22	WA5	2.4			
H23	RA0	2.4			
:	:	:			
H28	RA5	2.4			
H29	WEB	2.4			
H30	WSB	1.0			
H31	RSB	1.0			
H32	TIN	2.4			
H33	TEB	2.5			

Switching speed				
Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA5	(LH)	1.59	3.91	7.69
→DO0 to DO15	(HH)	1.58	3.90	7.69
	(HL)	2.50	4.55	7.89
	(LL)	2.50	4.55	7.89
RSB	(LH)	0.68	1.10	1.78
→DO0 to DO15	(HL)	0.78	1.16	1.79
DI0 to DI15	(HH)	1.61	3.24	5.89
→DO0 to DO15	(LL)	1.69	3.38	6.13

Equivalent Cells	6635	Power (mW/MHz)		Rev.	1

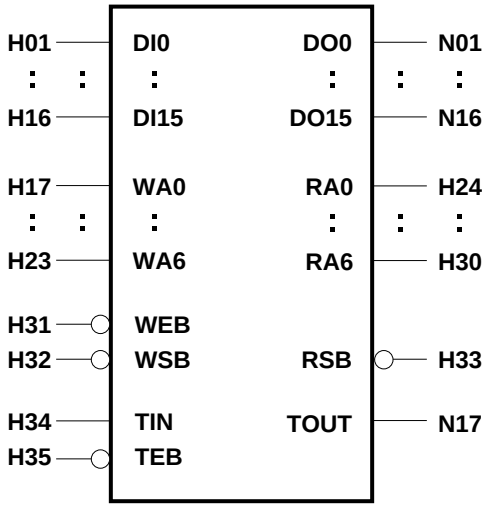
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.89**		
Address access time	**t_{ACA}**			**7.89**
Address output hold time	**t_{OH}**	**2.19**		
RSB access time	**t_{REC}**			**1.78**
RSB output hold time	**t_{REL}**	**0.78**		**1.79**
RSB output set time	**t_{RLL}**	**0.68**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.05**		
WSB-WEB reset time	**t_{CWR}**	**5.44**		
Write pulse width	**t_{WP}**	**5.44**		
Address setup time	**t_{AS}**	**2.37**		
Address hold time	**t_{AH}**	**0.24**		
Input data setup time	**t_{DS}**	**3.21**		
Input data hold time	**t_{DH}**	**0.38**		
WEB access time	**t_{WEC}**			**8.89**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9CD	**128 words × 16 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	24.7
H17	WA0	2.4	N17	TOUT	26.0
:	:	:			
H23	WA6	2.4			
H24	RA0	2.4			
:	:	:			
H30	RA6	2.4			
H31	WEB	2.4			
H32	WSB	2.4			
H33	RSB	2.4			
H34	TIN	2.4			
H35	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA6	(LH)	0.60	3.45	8.11
→DO0 to DO15	(HH)	0.52	3.40	8.11
	(HL)	1.58	4.14	8.31
	(LL)	1.52	4.10	8.31
RSB	(LH)	0.98	1.49	2.33
→DO0 to DO15	(HL)	1.12	1.64	2.51
DI0 to DI15	(HH)	1.82	3.53	6.32
→DO0 to DO15	(LL)	1.99	3.82	6.80

Equivalent Cells	12939	Power (mW/MHz)		Rev.	1

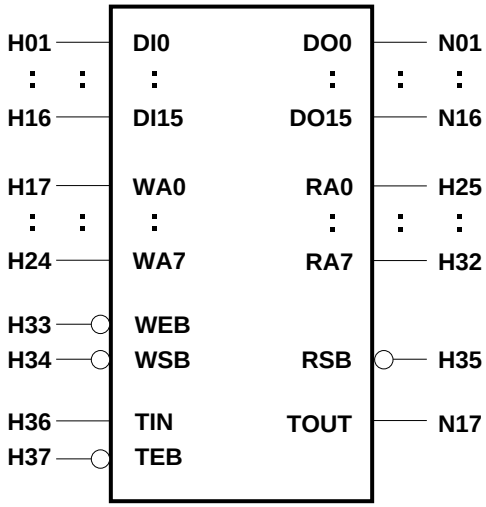
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.31**		
Address access time	**t_{ACA}**			**8.31**
Address output hold time	**t_{OH}**	**2.21**		
RSB access time	**t_{REC}**			**2.34**
RSB output hold time	**t_{REL}**	**1.12**		**2.51**
RSB output set time	**t_{RLL}**	**0.98**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.22**		
WSB-WEB reset time	**t_{CWR}**	**5.56**		
Write pulse width	**t_{WP}**	**5.56**		
Address setup time	**t_{AS}**	**2.34**		
Address hold time	**t_{AH}**	**0.32**		
Input data setup time	**t_{DS}**	**3.17**		
Input data hold time	**t_{DH}**	**0.51**		
WEB access time	**t_{WEC}**			**9.44**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9CF	**256 words × 16 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA7 (LH)	2.20	4.80	9.04
:	:	:	:	:	:	→DO0 to DO15 (HH)	2.19	4.79	9.04
H16	DI15	2.4	N16	DO15	23.7	(HL)	2.90	5.31	9.24
H17	WA0	2.4	N17	TOUT	26.0	(LL)	2.90	5.31	9.24
:	:	:							
H24	WA7	2.4				RSB (LH)	0.71	1.13	1.81
H25	RA0	2.4				→DO0 to DO15 (HL)	0.84	1.24	1.90
:	:	:							
H32	RA7	2.4				DI0 to DI15 (HH)	2.14	4.09	7.28
H33	WEB	2.4				→DO0 to DO15 (LL)	2.06	4.00	7.15
H34	WSB	1.0							
H35	RSB	1.0							
H36	TIN	2.4							
H37	TEB	2.5							

Equivalent Cells	20439	Power (mW/MHz)		Rev.	1

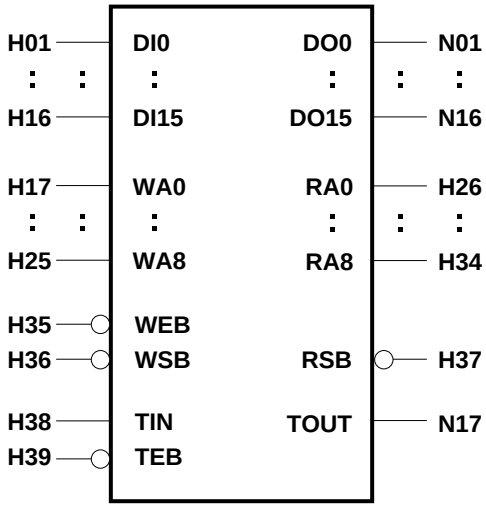
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.24**		
Address access time	**t_{ACA}**			**9.24**
Address output hold time	**t_{OH}**	**2.59**		
RSB access time	**t_{REC}**			**1.81**
RSB output hold time	**t_{REL}**	**0.84**		**1.90**
RSB output set time	**t_{RLL}**	**0.71**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.89**		
WSB-WEB reset time	**t_{CWR}**	**5.68**		
Write pulse width	**t_{WP}**	**5.68**		
Address setup time	**t_{AS}**	**3.97**		
Address hold time	**t_{AH}**	**0.24**		
Input data setup time	**t_{DS}**	**3.39**		
Input data hold time	**t_{DH}**	**0.49**		
WEB access time	**t_{WEC}**			**10.19**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9CH	**512 words × 16 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	24.7
H17	WA0	2.4	N17	TOUT	26.0
:	:	:			
H25	WA8	2.4			
H26	RA0	2.4			
:	:	:			
H34	RA8	2.4			
H35	WEB	2.4			
H36	WSB	2.4			
H37	RSB	2.4			
H38	TIN	2.4			
H39	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA8	(LH)	0.64	4.00	9.48
→DO0 to DO15	(HH)	0.56	3.95	9.48
	(HL)	1.62	4.68	9.68
	(LL)	1.56	4.65	9.68
RSB	(LH)	1.02	1.54	2.40
→DO0 to DO15	(HL)	1.17	1.72	2.62
DI0 to DI15	(HH)	2.34	4.38	7.71
→DO0 to DO15	(LL)	2.37	4.45	7.85

Equivalent Cells	40489	Power (mW/MHz)		Rev.	1

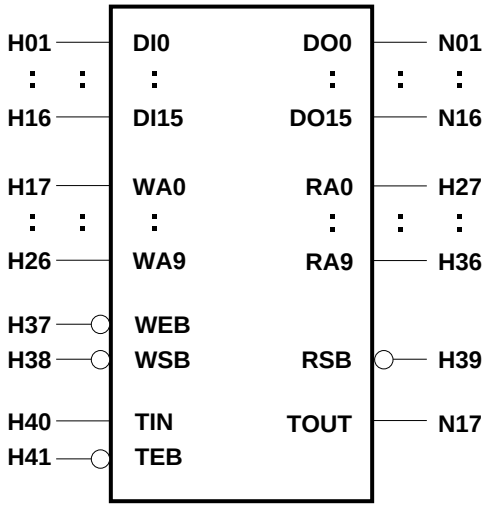
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.68**		
Address access time	**t_{ACA}**			**9.68**
Address output hold time	**t_{OH}**	**2.60**		
RSB access time	**t_{REC}**			**2.48**
RSB output hold time	**t_{REL}**	**1.17**		**2.62**
RSB output set time	**t_{RLL}**	**1.02**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.14**		
WSB-WEB reset time	**t_{CWR}**	**5.83**		
Write pulse width	**t_{WP}**	**5.83**		
Address setup time	**t_{AS}**	**3.98**		
Address hold time	**t_{AH}**	**0.33**		
Input data setup time	**t_{DS}**	**3.37**		
Input data hold time	**t_{DH}**	**0.63**		
WEB access time	**t_{WEC}**			**10.77**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9CM	**1K words × 16 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H16	DI15	2.4	N16	DO15	23.7
H17	WA0	2.4	N17	TOUT	26.0
:	:	:			
H26	WA9	2.4			
H27	RA0	2.4			
:	:	:			
H36	RA9	2.4			
H37	WEB	2.4			
H38	WSB	1.0			
H39	RSB	1.0			
H40	TIN	2.4			
H41	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA9	(LH)	4.33	7.28	12.10
→DO0 to DO15	(HH)	4.32	7.28	12.10
	(HL)	4.18	7.27	12.30
	(LL)	4.19	7.27	12.30
RSB	(LH)	0.79	1.22	1.93
→DO0 to DO15	(HL)	0.95	1.38	2.08
DI0 to DI15	(HH)	4.16	7.00	11.63
→DO0 to DO15	(LL)	3.75	6.76	11.67

Equivalent Cells	74160	Power (mW/MHz)		Rev.	1

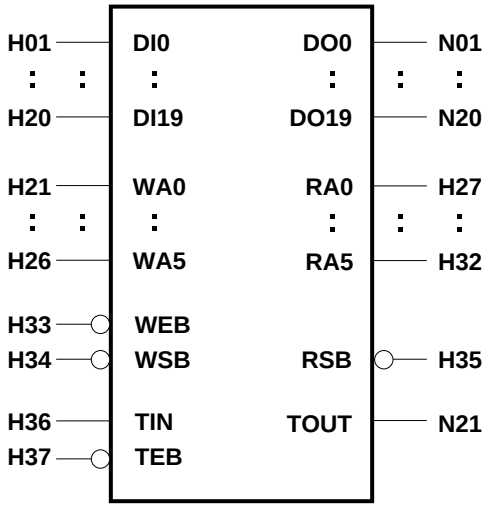
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.30**		
Address access time	**t_{ACA}**			**12.30**
Address output hold time	**t_{OH}**	**3.88**		
RSB access time	**t_{REC}**			**1.94**
RSB output hold time	**t_{REL}**	**0.95**		**2.08**
RSB output set time	**t_{RLL}**	**0.79**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**12.91**		
WSB-WEB reset time	**t_{CWR}**	**6.66**		
Write pulse width	**t_{WP}**	**6.66**		
Address setup time	**t_{AS}**	**6.00**		
Address hold time	**t_{AH}**	**0.25**		
Input data setup time	**t_{DS}**	**3.98**		
Input data hold time	**t_{DH}**	**0.61**		
WEB access time	**t_{WEC}**			**14.51**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9EB	**64 words × 20 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H20	DI19	2.4	N20	DO19	23.7
H21	WA0	2.4	N21	TOUT	26.0
:	:	:			
H26	WA5	2.4			
H27	RA0	2.4			
:	:	:			
H32	RA5	2.4			
H33	WEB	2.4			
H34	WSB	1.0			
H35	RSB	1.0			
H36	TIN	2.4			
H37	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA5	(LH)	1.60	3.93	7.73
→DO0 to DO19	(HH)	1.59	3.92	7.73
	(HL)	2.51	4.57	7.93
	(LL)	2.52	4.58	7.93
RSB	(LH)	0.69	1.11	1.81
→DO0 to DO19	(HL)	0.80	1.19	1.83
DI0 to DI19	(HH)	1.60	3.23	5.89
→DO0 to DO19	(LL)	1.69	3.38	6.14

Equivalent Cells	8125	Power (mW/MHz)		Rev.	1

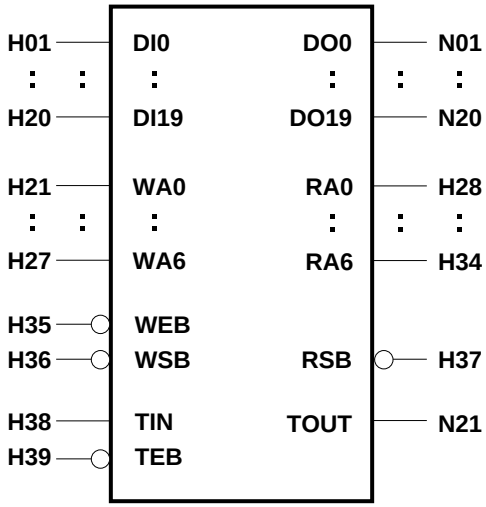
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.93**		
Address access time	**t_{ACA}**			**7.93**
Address output hold time	**t_{OH}**	**2.21**		
RSB access time	**t_{REC}**			**1.81**
RSB output hold time	**t_{REL}**	**0.80**		**1.83**
RSB output set time	**t_{RLL}**	**0.69**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.14**		
WSB-WEB reset time	**t_{CWR}**	**5.43**		
Write pulse width	**t_{WP}**	**5.43**		
Address setup time	**t_{AS}**	**2.47**		
Address hold time	**t_{AH}**	**0.24**		
Input data setup time	**t_{DS}**	**3.20**		
Input data hold time	**t_{DH}**	**0.38**		
WEB access time	**t_{WEC}**			**8.93**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9ED	**128 words × 20 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H20	DI19	2.4	N20	DO19	24.7
H21	WA0	2.4	N21	TOUT	26.0
:	:	:			
H27	WA6	2.4			
H28	RA0	2.4			
:	:	:			
H34	RA6	2.4			
H35	WEB	2.4			
H36	WSB	2.4			
H37	RSB	2.4			
H38	TIN	2.4			
H39	TEB	2.5			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
RA0 to RA6 →DO0 to DO19	(LH)	0.61	3.48	8.15
	(HH)	0.53	3.43	8.15
	(HL)	1.60	4.17	8.35
	(LL)	1.54	4.13	8.35
RSB →DO0 to DO19	(LH)	0.99	1.51	2.36
	(HL)	1.15	1.68	2.55
DI0 to DI19 →DO0 to DO19	(HH)	1.81	3.52	6.32
	(LL)	1.99	3.82	6.81

Equivalent Cells	15878	Power (mW/MHz)		Rev.	1

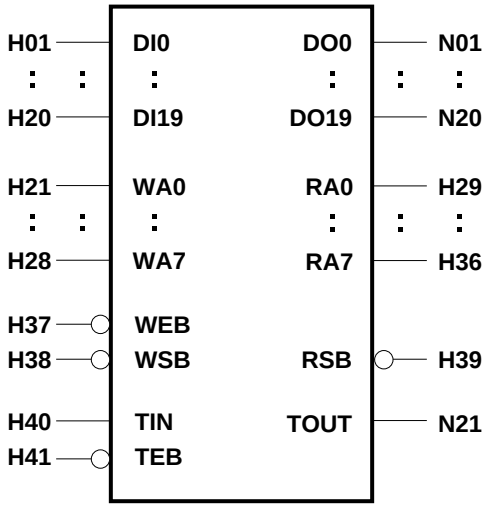
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.35**		
Address access time	**t_{ACA}**			**8.35**
Address output hold time	**t_{OH}**	**2.59**		
RSB access time	**t_{REC}**			**2.41**
RSB output hold time	**t_{REL}**	**1.15**		**2.55**
RSB output set time	**t_{RLL}**	**0.99**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.34**		
WSB-WEB reset time	**t_{CWR}**	**5.57**		
Write pulse width	**t_{WP}**	**5.57**		
Address setup time	**t_{AS}**	**2.45**		
Address hold time	**t_{AH}**	**0.32**		
Input data setup time	**t_{DS}**	**3.17**		
Input data hold time	**t_{DH}**	**0.51**		
WEB access time	**t_{WEC}**			**9.49**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9EF	**256 words × 20 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA7 (LH)	2.21	4.81	9.05
:	:	:	:	:	:	→DO0 to DO19 (HH)	2.20	4.80	9.05
H20	DI19	2.4	N20	DO19	23.7	(HL)	2.94	5.34	9.25
H21	WA0	2.4	N21	TOUT	26.0	(LL)	2.95	5.34	9.25
:	:	:							
H28	WA7	2.4				RSB (LH)	0.73	1.16	1.86
H29	RA0	2.4				→DO0 to DO19 (HL)	0.88	1.29	1.97
:	:	:							
H36	RA7	2.4				DI0 to DI19 (HH)	2.14	4.09	7.28
H37	WEB	2.4				→DO0 to DO19 (LL)	2.06	4.00	7.15
H38	WSB	1.0							
H39	RSB	1.0							
H40	TIN	2.4							
H41	TEB	2.5							

Equivalent Cells	25290	Power (mW/MHz)		Rev.	1

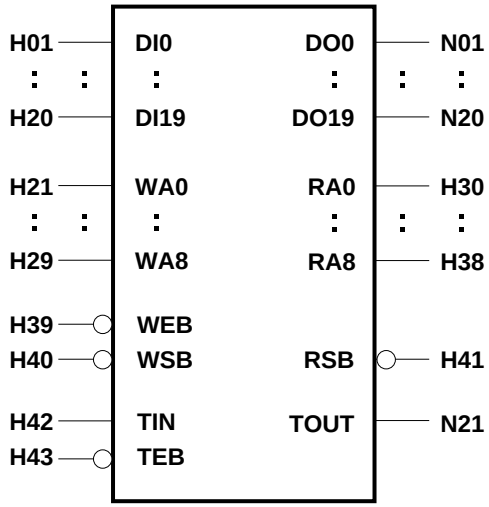
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.25**		
Address access time	**t_{ACA}**			**9.25**
Address output hold time	**t_{OH}**	**2.63**		
RSB access time	**t_{REC}**			**1.86**
RSB output hold time	**t_{REL}**	**0.88**		**1.97**
RSB output set time	**t_{RLL}**	**0.73**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.38**		
WSB-WEB reset time	**t_{CWR}**	**5.69**		
Write pulse width	**t_{WP}**	**5.69**		
Address setup time	**t_{AS}**	**3.98**		
Address hold time	**t_{AH}**	**0.24**		
Input data setup time	**t_{DS}**	**3.39**		
Input data hold time	**t_{DH}**	**0.49**		
WEB access time	**t_{WEC}**			**10.26**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9EH	**512 words × 20 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H20	DI19	2.4	N20	DO19	24.7
H21	WA0	2.4	N21	TOUT	26.0
:	:	:			
H29	WA8	2.4			
H30	RA0	2.4			
:	:	:			
H38	RA8	2.4			
H39	WEB	2.4			
H40	WSB	2.4			
H41	RSB	2.4			
H42	TIN	2.4			
H43	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA8	(LH)	0.65	4.01	9.50
→DO0 to DO19	(HH)	0.58	3.97	9.50
	(HL)	1.66	4.72	9.70
	(LL)	1.59	4.67	9.70
RSB	(LH)	1.04	1.58	2.46
→DO0 to DO19	(HL)	1.21	1.77	2.70
DI0 to DI19	(HH)	2.34	4.38	7.71
→DO0 to DO19	(LL)	2.37	4.45	7.85

Equivalent Cells	50129	Power (mW/MHz)		Rev.	1

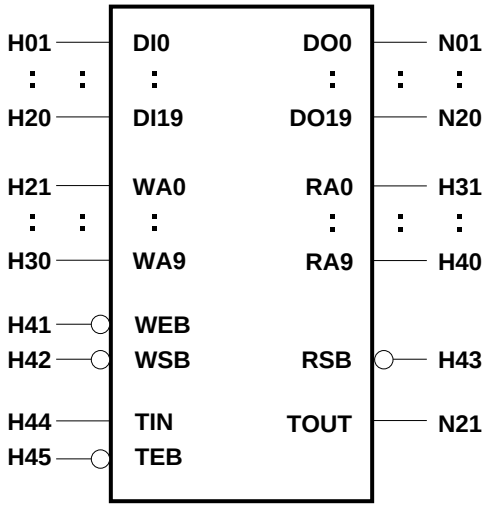
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.70**		
Address access time	**t_{ACA}**			**9.70**
Address output hold time	**t_{OH}**	**2.63**		
RSB access time	**t_{REC}**			**2.56**
RSB output hold time	**t_{REL}**	**1.21**		**2.70**
RSB output set time	**t_{RLL}**	**1.04**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.17**		
WSB-WEB reset time	**t_{CWR}**	**5.84**		
Write pulse width	**t_{WP}**	**5.84**		
Address setup time	**t_{AS}**	**3.99**		
Address hold time	**t_{AH}**	**0.34**		
Input data setup time	**t_{DS}**	**3.37**		
Input data hold time	**t_{DH}**	**0.64**		
WEB access time	**t_{WEC}**			**10.84**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9EM	**1K words × 20 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H20	DI19	2.4	N20	DO19	23.7
H21	WA0	2.4	N21	TOUT	26.0
:	:	:			
H30	WA9	2.4			
H31	RA0	2.4			
:	:	:			
H40	RA9	2.4			
H41	WEB	2.4			
H42	WSB	1.0			
H43	RSB	1.0			
H44	TIN	2.4			
H45	TEB	2.5			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
RA0 to RA9	(LH)	4.44	7.35	12.11
→DO0 to DO19	(HH)	4.43	7.35	12.11
	(HL)	4.22	7.29	12.31
	(LL)	4.22	7.29	12.31
RSB	(LH)	0.84	1.28	2.01
→DO0 to DO19	(HL)	0.99	1.44	2.17
DI0 to DI19	(HH)	4.16	7.00	11.64
→DO0 to DO19	(LL)	3.75	6.76	11.67

Equivalent Cells	92244	Power (mW/MHz)		Rev.	1

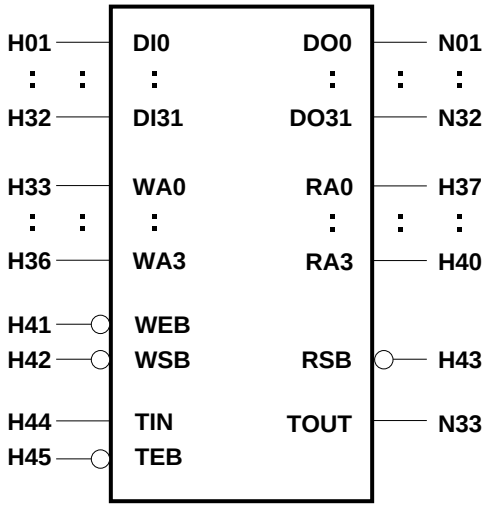
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**12.31**		
Address access time	**t_{ACA}**			**12.31**
Address output hold time	**t_{OH}**	**3.92**		
RSB access time	**t_{REC}**			**2.04**
RSB output hold time	**t_{REL}**	**0.99**		**2.18**
RSB output set time	**t_{RLL}**	**0.84**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**13.25**		
WSB-WEB reset time	**t_{CWR}**	**6.90**		
Write pulse width	**t_{WP}**	**6.90**		
Address setup time	**t_{AS}**	**6.10**		
Address hold time	**t_{AH}**	**0.25**		
Input data setup time	**t_{DS}**	**3.78**		
Input data hold time	**t_{DH}**	**0.61**		
WEB access time	**t_{WEC}**			**14.52**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9H7	**16 words × 32 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	23.7
H33	WA0	2.4	N33	TOUT	26.0
:	:	:			
H36	WA3	2.4			
H37	RA0	2.4			
:	:	:			
H40	RA3	2.4			
H41	WEB	2.4			
H42	WSB	1.0			
H43	RSB	1.0			
H44	TIN	2.4			
H45	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA3	(LH)	1.48	3.76	7.47
→DO0 to DO31	(HH)	1.43	3.73	7.47
	(HL)	2.35	4.37	7.67
	(LL)	2.40	4.40	7.67
RSB	(LH)	0.80	1.23	1.94
→DO0 to DO31	(HL)	0.90	1.31	1.99
DI0 to DI31	(HH)	1.48	2.99	5.45
→DO0 to DO31	(LL)	1.57	3.14	5.70

Equivalent Cells	5606	Power (mW/MHz)		Rev.	1

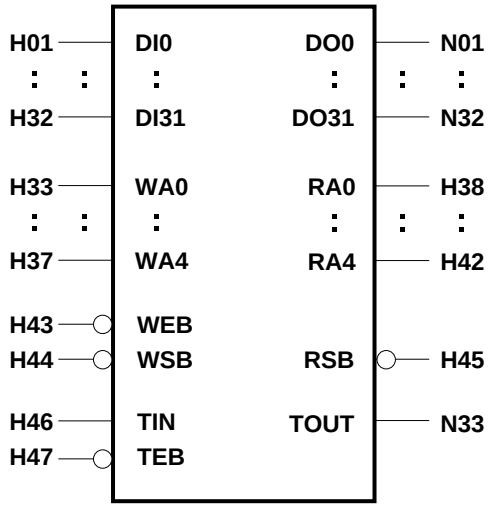
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.67**		
Address access time	**t_{ACA}**			**7.67**
Address output hold time	**t_{OH}**	**2.04**		
RSB access time	**t_{REC}**			**1.94**
RSB output hold time	**t_{REL}**	**0.90**		**2.00**
RSB output set time	**t_{RLL}**	**0.80**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.12**		
WSB-WEB reset time	**t_{CWR}**	**5.54**		
Write pulse width	**t_{WP}**	**5.54**		
Address setup time	**t_{AS}**	**3.23**		
Address hold time	**t_{AH}**	**0.35**		
Input data setup time	**t_{DS}**	**3.01**		
Input data hold time	**t_{DH}**	**0.76**		
WEB access time	**t_{WEC}**			**8.82**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9H9	**32 words × 32 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	23.7
H33	WA0	2.4	N33	TOUT	26.0
:	:	:			
H37	WA4	2.4			
H38	RA0	2.4			
:	:	:			
H42	RA4	2.4			
H43	WEB	2.4			
H44	WSB	1.0			
H45	RSB	1.0			
H46	TIN	2.4			
H47	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA4	(LH)	1.58	3.89	7.67
→DO0 to DO31	(HH)	1.53	3.86	7.67
	(HL)	2.45	4.51	7.87
	(LL)	2.50	4.54	7.87
RSB	(LH)	0.81	1.24	1.95
→DO0 to DO31	(HL)	0.91	1.32	2.00
DI0 to DI31	(HH)	1.49	3.03	5.55
→DO0 to DO31	(LL)	1.58	3.19	5.80

Equivalent Cells	9852	Power (mW/MHz)		Rev.	1

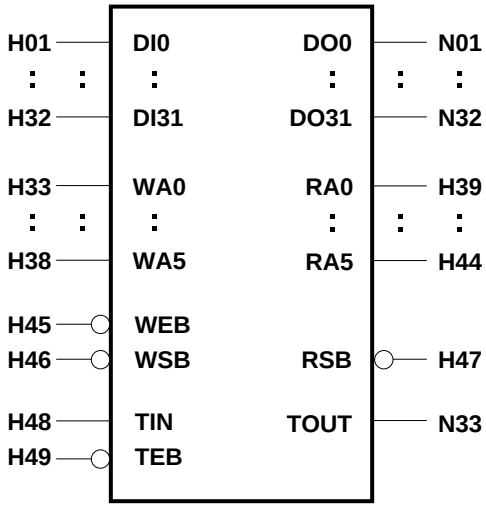
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.87**		
Address access time	**t_{ACA}**			**7.87**
Address output hold time	**t_{OH}**	**2.15**		
RSB access time	**t_{REC}**			**1.95**
RSB output hold time	**t_{REL}**	**0.91**		**2.01**
RSB output set time	**t_{RLL}**	**0.81**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.54**		
WSB-WEB reset time	**t_{CWR}**	**5.94**		
Write pulse width	**t_{WP}**	**5.94**		
Address setup time	**t_{AS}**	**3.24**		
Address hold time	**t_{AH}**	**0.36**		
Input data setup time	**t_{DS}**	**3.02**		
Input data hold time	**t_{DH}**	**0.77**		
WEB access time	**t_{WEC}**			**8.92**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9HB	**64 words × 32 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA5 (LH)	1.65	3.99	7.82
:	:	:	:	:	:	→DO0 to DO31 (HH)	1.63	3.98	7.82
H32	DI31	2.4	N32	DO31	23.7	(HL)	2.54	4.62	8.02
H33	WA0	2.4	N33	TOUT	26.0	(LL)	2.57	4.64	8.02
:	:	:							
H38	WA5	2.4				RSB (LH)	0.75	1.17	1.87
H39	RA0	2.4				→DO0 to DO31 (HL)	0.85	1.24	1.89
:	:	:							
H44	RA5	2.4				DI0 to DI31 (HH)	1.62	3.24	5.89
H45	WEB	2.4				→DO0 to DO31 (LL)	1.70	3.39	6.13
H46	WSB	1.0							
H47	RSB	1.0							
H48	TIN	2.4							
H49	TEB	2.5							

Equivalent Cells	13026	Power (mW/MHz)		Rev.	1

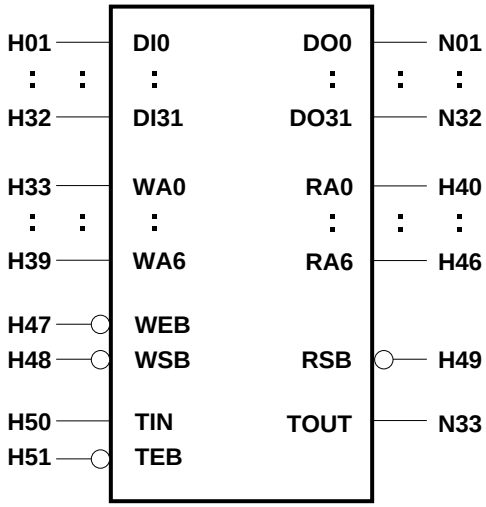
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.02**		
Address access time	**t_{ACA}**			**8.02**
Address output hold time	**t_{OH}**	**2.25**		
RSB access time	**t_{REC}**			**1.87**
RSB output hold time	**t_{REL}**	**0.85**		**1.90**
RSB output set time	**t_{RLL}**	**0.75**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.34**		
WSB-WEB reset time	**t_{CWR}**	**5.56**		
Write pulse width	**t_{WP}**	**5.56**		
Address setup time	**t_{AS}**	**2.50**		
Address hold time	**t_{AH}**	**0.28**		
Input data setup time	**t_{DS}**	**3.10**		
Input data hold time	**t_{DH}**	**0.52**		
WEB access time	**t_{WEC}**			**9.05**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9HD	**128 words × 32 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	24.7
H33	WA0	2.4	N33	TOUT	26.0
:	:	:			
H39	WA6	2.4			
H40	RA0	2.4			
:	:	:			
H46	RA6	2.4			
H47	WEB	2.4			
H48	WSB	2.4			
H49	RSB	2.4			
H50	TIN	2.4			
H51	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA6	(LH)	0.67	3.60	8.39
→DO0 to DO31	(HH)	0.59	3.55	8.39
	(HL)	1.64	4.28	8.59
	(LL)	1.59	4.25	8.59
RSB	(LH)	1.06	1.61	2.50
→DO0 to DO31	(HL)	1.20	1.74	2.63
DI0 to DI31	(HH)	1.82	3.53	6.32
→DO0 to DO31	(LL)	2.01	3.84	6.82

Equivalent Cells	25605	Power (mW/MHz)		Rev.	1

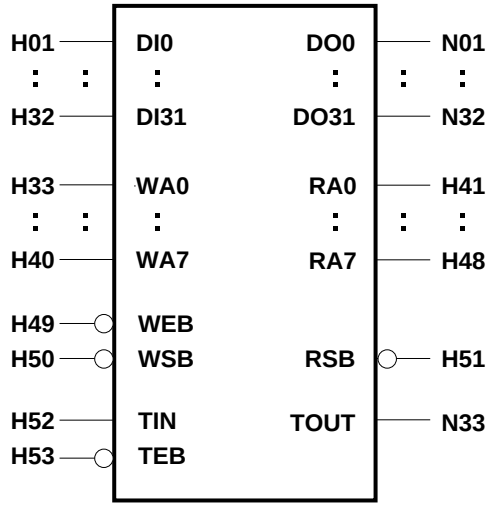
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.59**		
Address access time	**t_{ACA}**			**8.59**
Address output hold time	**t_{OH}**	**2.25**		
RSB access time	**t_{REC}**			**2.50**
RSB output hold time	**t_{REL}**	**1.20**		**2.63**
RSB output set time	**t_{RLL}**	**1.06**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.93**		
WSB-WEB reset time	**t_{CWR}**	**5.87**		
Write pulse width	**t_{WP}**	**5.87**		
Address setup time	**t_{AS}**	**2.67**		
Address hold time	**t_{AH}**	**0.39**		
Input data setup time	**t_{DS}**	**3.05**		
Input data hold time	**t_{DH}**	**0.78**		
WEB access time	**t_{WEC}**			**9.82**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9HF	**256 words × 32 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	23.7
H33	WA0	2.4	N33	TOUT	26.0
:	:	:			
H40	WA7	2.4			
H41	RA0	2.4			
:	:	:			
H48	RA7	2.4			
H49	WEB	2.4			
H50	WSB	1.0			
H51	RSB	1.0			
H52	TIN	2.4			
H53	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA7	(LH)	2.27	4.90	9.19
→DO0 to DO31	(HH)	2.24	4.88	9.19
	(HL)	2.95	5.40	9.39
	(LL)	2.98	5.42	9.39
RSB	(LH)	0.77	1.20	1.91
→DO0 to DO31	(HL)	0.91	1.33	2.02
DI0 to DI31	(HH)	2.14	4.09	7.28
→DO0 to DO31	(LL)	2.06	4.00	7.15

Equivalent Cells	40559	Power (mW/MHz)		Rev.	1

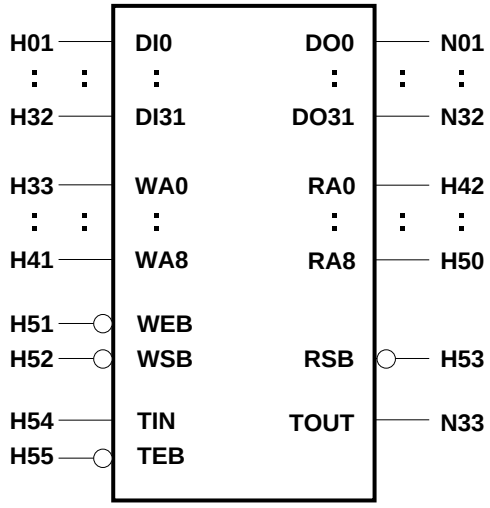
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.39**		
Address access time	**t_{ACA}**			**9.39**
Address output hold time	**t_{OH}**	**2.65**		
RSB access time	**t_{REC}**			**2.50**
RSB output hold time	**t_{REL}**	**1.20**		**2.63**
RSB output set time	**t_{RLL}**	**1.06**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.93**		
WSB-WEB reset time	**t_{CWR}**	**5.87**		
Write pulse width	**t_{WP}**	**5.87**		
Address setup time	**t_{AS}**	**2.67**		
Address hold time	**t_{AH}**	**0.39**		
Input data setup time	**t_{DS}**	**3.05**		
Input data hold time	**t_{DH}**	**0.78**		
WEB access time	**t_{WEC}**			**9.82**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9HH	**512 words × 32 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H32	DI31	2.4	N32	DO31	24.7
H33	WA0	2.4	N33	TOUT	26.0
:	:	:			
H41	WA8	2.4			
H42	RA0	2.4			
:	:	:			
H50	RA8	2.4			
H51	WEB	2.4			
H52	WSB	2.4			
H53	RSB	2.4			
H54	TIN	2.4			
H55	TEB	5.0			

Switching speed				
Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA8	(LH)	0.71	4.17	9.82
→DO0 to DO31	(HH)	0.65	4.13	9.82
	(HL)	1.68	4.85	10.02
	(LL)	1.62	4.81	10.02
RSB	(LH)	1.14	1.70	2.61
→DO0 to DO31	(HL)	1.25	1.82	2.77
DI0 to DI31	(HH)	2.35	4.39	7.72
→DO0 to DO31	(LL)	2.37	4.46	7.86

Equivalent Cells	80657	Power (mW/MHz)		Rev.	1

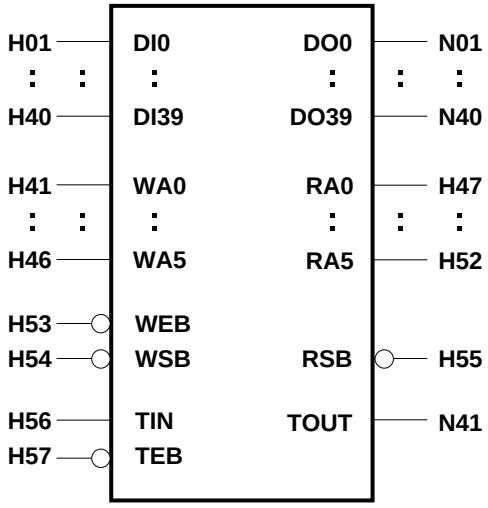
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.02**		
Address access time	**t_{ACA}**			**10.02**
Address output hold time	**t_{OH}**	**2.65**		
RSB access time	**t_{REC}**			**2.63**
RSB output hold time	**t_{REL}**	**1.25**		**2.77**
RSB output set time	**t_{RLL}**	**1.14**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**10.98**		
WSB-WEB reset time	**t_{CWR}**	**6.22**		
Write pulse width	**t_{WP}**	**6.22**		
Address setup time	**t_{AS}**	**4.35**		
Address hold time	**t_{AH}**	**0.41**		
Input data setup time	**t_{DS}**	**3.22**		
Input data hold time	**t_{DH}**	**0.96**		
WEB access time	**t_{WEC}**			**11.23**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KB	**64 words × 40 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7				
:	:	:	:	:	:				
H40	DI39	2.4	N40	DO39	23.7				
H41	WA0	2.4	N41	TOUT	26.0				
:	:	:							
H46	WA5	2.4							
H47	RA0	2.4							
:	:	:							
H52	RA5	2.4							
H53	WEB	2.4							
H54	WSB	1.0							
H55	RSB	1.0							
H56	TIN	2.4							
H57	TEB	2.5							
						RA0 to RA5 (LH)	1.66	4.02	7.86
						→DO0 to DO39 (HH)	1.64	4.00	7.86
						(HL)	2.56	4.65	8.06
						(LL)	2.58	4.66	8.06
						RSB (LH)	0.76	1.20	1.91
						→DO0 to DO39 (HL)	0.87	1.27	1.94
						DI0 to DI39 (HH)	1.61	3.24	5.90
						→DO0 to DO39 (LL)	1.70	3.39	6.14

Equivalent Cells	15994	Power (mW/MHz)		Rev.	1

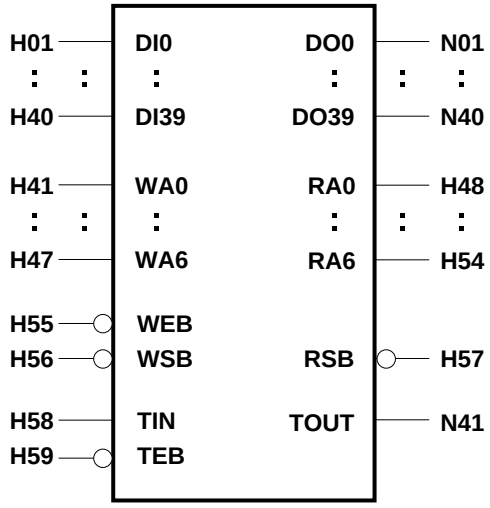
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.06**		
Address access time	**t_{ACA}**			**8.06**
Address output hold time	**t_{OH}**	**2.25**		
RSB access time	**t_{REC}**			**1.91**
RSB output hold time	**t_{REL}**	**0.87**		**1.94**
RSB output set time	**t_{RLL}**	**0.76**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.45**		
WSB-WEB reset time	**t_{CWR}**	**5.57**		
Write pulse width	**t_{WP}**	**5.57**		
Address setup time	**t_{AS}**	**2.60**		
Address hold time	**t_{AH}**	**0.28**		
Input data setup time	**t_{DS}**	**3.10**		
Input data hold time	**t_{DH}**	**0.52**		
WEB access time	**t_{WEC}**			**9.11**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KD	**128 words × 40 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H40	DI39	2.4	N40	DO39	24.7
H41	WA0	2.4	N41	TOUT	26.0
:	:	:			
H47	WA6	2.4			
H48	RA0	2.4			
:	:	:			
H54	RA6	2.4			
H55	WEB	2.4			
H56	WSB	2.4			
H57	RSB	2.4			
H58	TIN	2.4			
H59	TEB	2.5			

Switching speed

Path		t_{LD0} (ns) MIN.	TYP.	MAX.
IN → OUT				
RA0 to RA6	(LH)	0.68	3.63	8.44
→DO0 to DO39	(HH)	0.61	3.59	8.44
	(HL)	1.67	4.32	8.64
	(LL)	1.61	4.28	8.64
RSB	(LH)	1.08	1.63	2.54
→DO0 to DO39	(HL)	1.22	1.77	2.67
DI0 to DI39	(HH)	1.81	3.53	6.33
→DO0 to DO39	(LL)	2.01	3.84	6.82

Equivalent Cells	31469	Power (mW/MHz)		Rev.	1

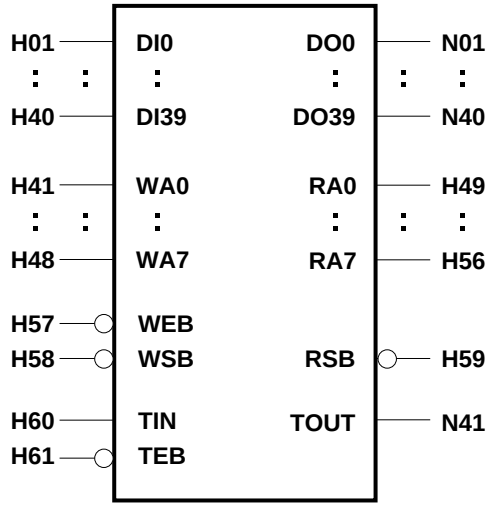
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.64**		
Address access time	**t_{ACA}**			**8.64**
Address output hold time	**t_{OH}**	**2.26**		
RSB access time	**t_{REC}**			**2.55**
RSB output hold time	**t_{REL}**	**1.22**		**2.68**
RSB output set time	**t_{RLL}**	**1.08**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**9.03**		
WSB-WEB reset time	**t_{CWR}**	**5.88**		
Write pulse width	**t_{WP}**	**5.88**		
Address setup time	**t_{AS}**	**2.77**		
Address hold time	**t_{AH}**	**0.38**		
Input data setup time	**t_{DS}**	**3.04**		
Input data hold time	**t_{DH}**	**0.78**		
WEB access time	**t_{WEC}**			**9.88**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KF	**256 words × 40 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	23.7
:	:	:	:	:	:
H40	DI39	2.4	N40	DO39	23.7
H41	WA0	2.4	N41	TOUT	26.0
:	:	:			
H48	WA7	2.4			
H49	RA0	2.4			
:	:	:			
H56	RA7	2.4			
H57	WEB	2.4			
H58	WSB	1.0			
H59	RSB	1.0			
H60	TIN	2.4			
H61	TEB	2.5			

Switching speed

Path		t_{LD0} (ns)		
IN → OUT		MIN.	TYP.	MAX.
RA0 to RA7	(LH)	2.28	4.91	9.21
→DO0 to DO39	(HH)	2.25	4.89	9.21
	(HL)	2.99	5.43	9.41
	(LL)	3.02	5.45	9.41
RSB	(LH)	0.79	1.24	1.97
→DO0 to DO39	(HL)	0.95	1.38	2.09
DI0 to DI39	(HH)	2.14	4.09	7.28
→DO0 to DO39	(LL)	2.06	4.00	7.15

Equivalent Cells	50227	Power (mW/MHz)		Rev.	1

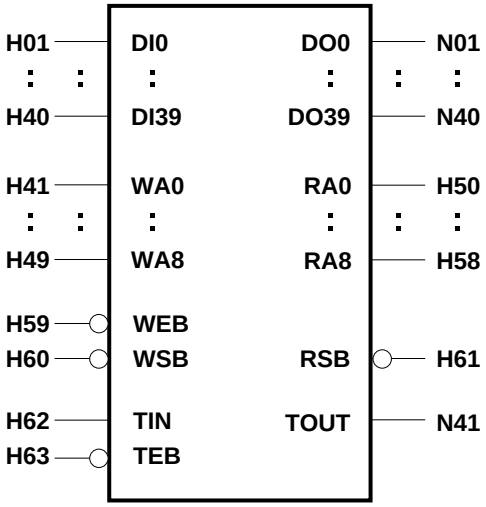
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.41**		
Address access time	**t_{ACA}**			**9.41**
Address output hold time	**t_{OH}**	**2.69**		
RSB access time	**t_{REC}**			**1.97**
RSB output hold time	**t_{REL}**	**0.95**		**2.10**
RSB output set time	**t_{RLL}**	**0.79**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.95**		
WSB-WEB reset time	**t_{CWR}**	**5.84**		
Write pulse width	**t_{WP}**	**5.84**		
Address setup time	**t_{AS}**	**4.13**		
Address hold time	**t_{AH}**	**0.30**		
Input data setup time	**t_{DS}**	**3.27**		
Input data hold time	**t_{DH}**	**0.96**		
WEB access time	**t_{WEC}**			**10.46**

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KH	**512 words × 40 bits Dual-port RAM**	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant
DIn : Input data
WAn : A-port address (Write)
WSB : A-port select
WEB : Write enable
DMn : Memory data
RAn : B-port address (Read)
RSB : B-port select
DOn : Output data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	DI0	2.4	N01	DO0	24.7
:	:	:	:	:	:
H40	DI39	2.4	N40	DO39	24.7
H41	WA0	2.4	N41	TOUT	26.0
:	:	:			
H49	WA8	2.4			
H50	RA0	2.4			
:	:	:			
H58	RA8	2.4			
H59	WEB	2.4			
H60	WSB	2.4			
H61	RSB	2.4			
H62	TIN	2.4			
H63	TEB	5.0			

Switching speed

Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
RA0 to RA8	(LH)	0.75	4.21	9.85
→DO0 to DO39	(HH)	0.68	4.16	9.85
	(HL)	1.71	4.88	10.05
	(LL)	1.66	4.85	10.05
RSB	(LH)	1.17	1.74	2.67
→DO0 to DO39	(HL)	1.29	1.88	2.84
DI0 to DI39	(HH)	2.36	4.40	7.72
→DO0 to DO39	(LL)	2.37	4.46	7.86

Equivalent Cells	99937	Power (mW/MHz)		Rev.	1

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.05**		
Address access time	**t_{ACA}**			**10.05**
Address output hold time	**t_{OH}**	**2.69**		
RSB access time	**t_{REC}**			**2.71**
RSB output hold time	**t_{REL}**	**1.29**		**2.85**
RSB output set time	**t_{RLL}**	**1.17**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**11.01**		
WSB-WEB reset time	**t_{CWR}**	**6.23**		
Write pulse width	**t_{WP}**	**6.23**		
Address setup time	**t_{AS}**	**4.36**		
Address hold time	**t_{AH}**	**0.42**		
Input data setup time	**t_{DS}**	**3.23**		
Input data hold time	**t_{DH}**	**0.98**		
WEB access time	**t_{WEC}**			**11.32**

[MEMO]

★

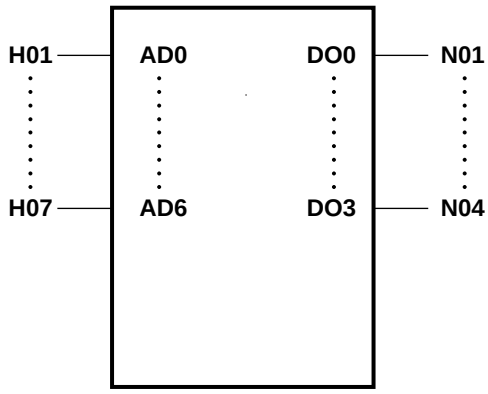
CHAPTER 3

ROM BLOCK

ROM BLOCK

Block Type	Function
J14DK	**128 words × 4 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H07	AD0 : AD6	2.5 : 2.5	N01 : N04	DO0 : DO3	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD6→DO0 to DO3	(HH)	0.207	1.272	3.164	0.541	1.212	1.212
	(HL)	0.444	1.541	3.491	0.359	1.055	1.055
	(LH)	0.207	1.272	3.164	0.541	1.212	1.212
	(LL)	0.444	1.541	3.491	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	3.4907		3.4907
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.2074		

Caution This ROM block is under development in EA-9HD family.

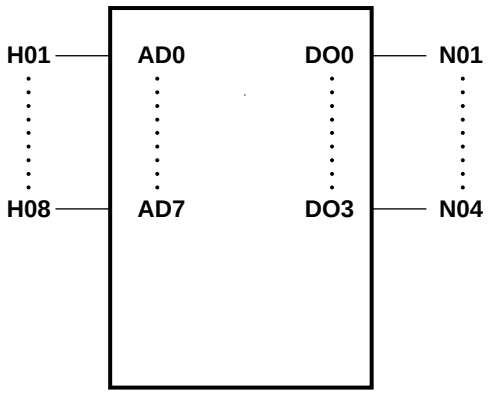
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	1113 (53 × 21)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.018

ROM BLOCK

Block Type	Function
J14FK	**256 words × 4 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	AD0	2.5	N01	DO0	53
:	:	:	:	:	:
H08	AD7	2.5	N04	DO3	53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD7→DO0 to DO3	(HH)	0.314	1.513	3.645	0.541	1.212	1.212
	(HL)	0.538	1.769	3.959	0.359	1.055	1.055
	(LH)	0.314	1.513	3.645	0.541	1.212	1.212
	(LL)	0.538	1.769	3.959	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	3.9593		3.9593
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

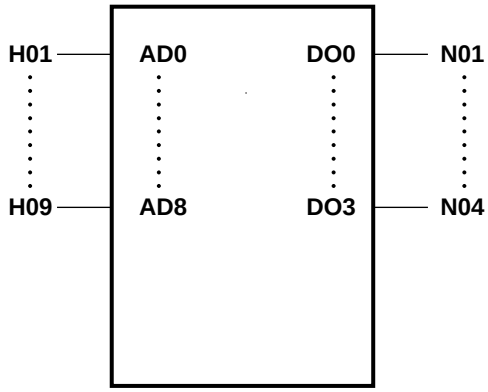
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	2035 (55 × 37)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.036

ROM BLOCK

Block Type	Function
J14HK	**512 words × 4 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H09	AD0 : AD8	2.5 : 2.5	N01 : N04	DO0 : DO3	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD8→DO0 to DO3	(HH)	0.314	1.551	3.752	0.541	1.212	1.212
	(HL)	0.538	1.835	4.142	0.359	1.055	1.055
	(LH)	0.314	1.551	3.752	0.541	1.212	1.212
	(LL)	0.538	1.835	4.142	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.1422		4.1422
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

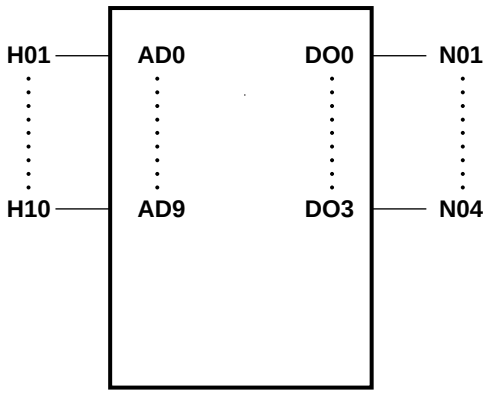
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	3458 (91 × 38)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.072

ROM BLOCK

Block Type	Function
J14MK	**1024 words × 4 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01	AD0	2.5	N01	DO0	53
:	:	:	:	:	:
H10	AD9	2.5	N04	DO3	53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD9→DO0 to DO3	(HH)	0.417	1.828	4.336	0.541	1.212	1.212
	(HL)	0.636	1.963	4.323	0.359	1.055	1.055
	(LH)	0.417	1.828	4.336	0.541	1.212	1.212
	(LL)	0.636	1.963	4.323	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.3363		4.3363
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.4170		

Caution This ROM block is under development in EA-9HD family.

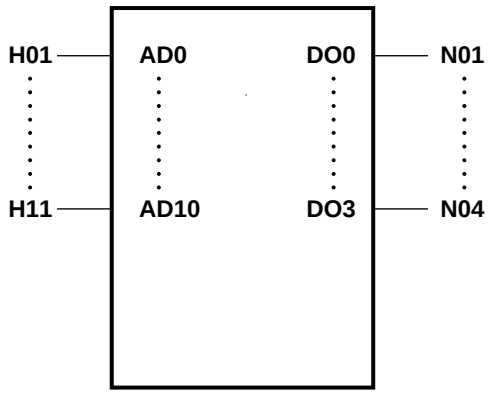
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	6370 (91 × 70)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.144

ROM BLOCK

Block Type	Function
J14SK	**2048 words × 4 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H11	AD0 : AD10	2.5 : 2.5	N01 : N04	DO0 : DO3	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD10→DO0 to DO3	(HH)	0.417	2.198	5.364	0.541	1.212	1.212
	(HL)	0.638	2.220	5.034	0.359	1.055	1.055
	(LH)	0.417	2.198	5.364	0.541	1.212	1.212
	(LL)	0.638	2.220	5.034	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	5.3642		
Address access time	t_{ACC}			5.3642
Address-output hold time	t_{AOH}		0.4170	

Caution This ROM block is under development in EA-9HD family.

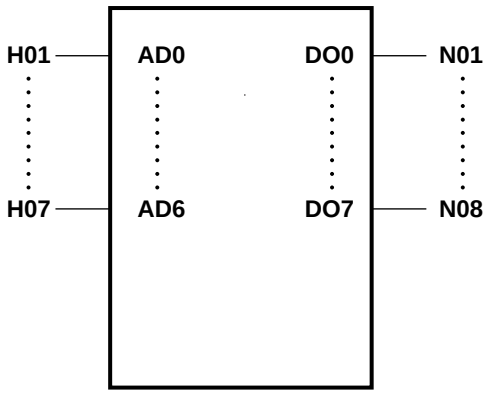
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	12194 (91 × 134)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.288

ROM BLOCK

Block Type	Function
J18DK	**128 words × 8 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H07	AD0 : AD6	2.5 : 2.5	N01 : N08	DO0 : DO7	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD6→DO0 to DO7	(HH)	0.207	1.348	3.376	0.541	1.212	1.212
	(HL)	0.444	1.593	3.636	0.359	1.055	1.055
	(LH)	0.207	1.348	3.376	0.541	1.212	1.212
	(LL)	0.444	1.593	3.636	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	3.6364		3.6364
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}		0.2074	

Caution This ROM block is under development in EA-9HD family.

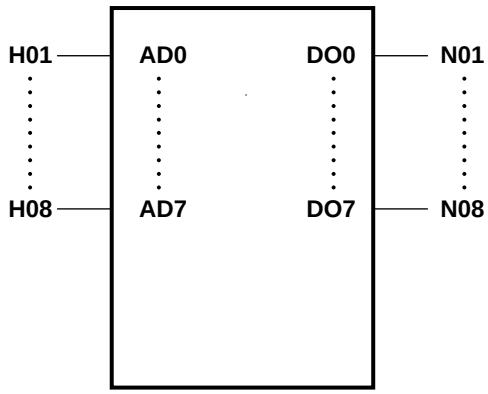
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	1785 (85 × 21)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.036

ROM BLOCK

Block Type	Function
J18FK	**256 words × 8 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H08	AD0 : AD7	2.5 : 2.5	N01 : N08	DO0 : DO7	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD7→DO0 to DO7	(HH)	0.314	1.551	3.752	0.541	1.212	1.212
	(HL)	0.538	1.835	4.142	0.359	1.055	1.055
	(LH)	0.314	1.551	3.752	0.541	1.212	1.212
	(LL)	0.538	1.835	4.142	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.1422		4.1422
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

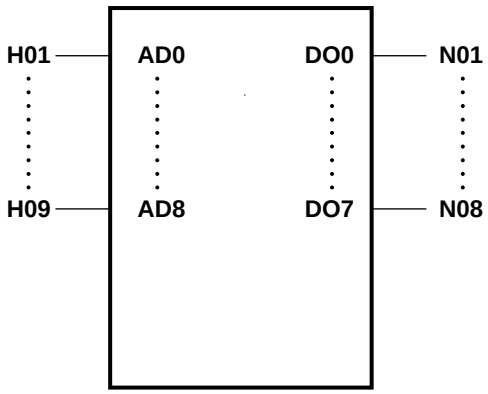
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]		
3219 (87 × 37)	Write cycle	———	
	Read cycle	0.055	

ROM BLOCK

Block Type	Function
J18HK	**512 words × 8 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H09	AD0 : AD8	2.5 : 2.5	N01 : N08	DO0 : DO7	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD8→DO0 to DO7	(HH)	0.314	1.666	4.069	0.541	1.212	1.212
	(HL)	0.538	1.899	4.321	0.359	1.055	1.055
	(LH)	0.314	1.666	4.069	0.541	1.212	1.212
	(LL)	0.538	1.899	4.321	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.3205		4.3205
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

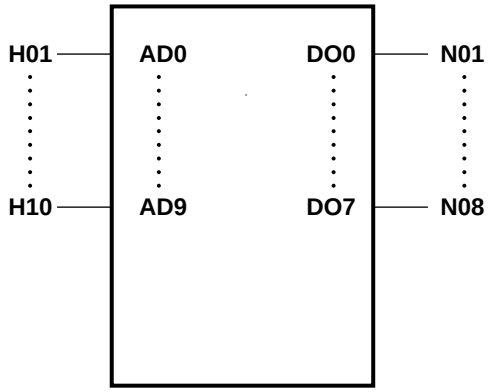
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]	
5890 (155 × 38)	Write cycle	———
	Read cycle	0.110

ROM BLOCK

Block Type	Function
J18MK	**1024 words × 8 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H10	AD0 : AD9	2.5 : 2.5	N01 : N08	DO0 : DO7	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD9→DO0 to DO7	(HH)	0.417	2.019	4.866	0.541	1.212	1.212
	(HL)	0.636	2.201	4.981	0.359	1.055	1.055
	(LH)	0.417	2.019	4.866	0.541	1.212	1.212
	(LL)	0.636	2.201	4.981	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.9813		4.9813
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.4170		

Caution This ROM block is under development in EA-9HD family.

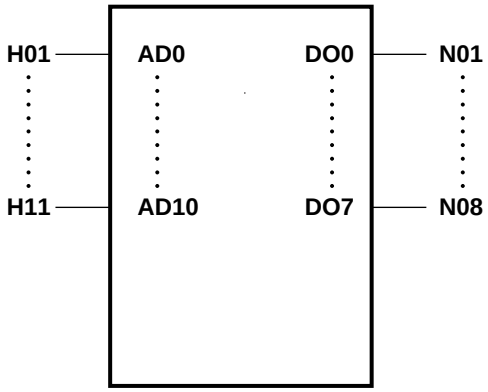
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]		
10850 (155 × 70)	Write cycle	———	
	Read cycle	0.068	

ROM BLOCK

Block Type	Function
J18SK	**2048 words × 8 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H11	AD0 : AD10	2.5 : 2.5	N01 : N08	DO0 : DO7	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD10→DO0 to DO7	(HH)	0.417	2.351	5.788	0.541	1.212	1.212
	(HL)	0.638	2.317	5.303	0.359	1.055	1.055
	(LH)	0.417	2.351	5.788	0.541	1.212	1.212
	(LL)	0.638	2.317	5.303	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	5.7882		5.7882
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.4170		

Caution This ROM block is under development in EA-9HD family.

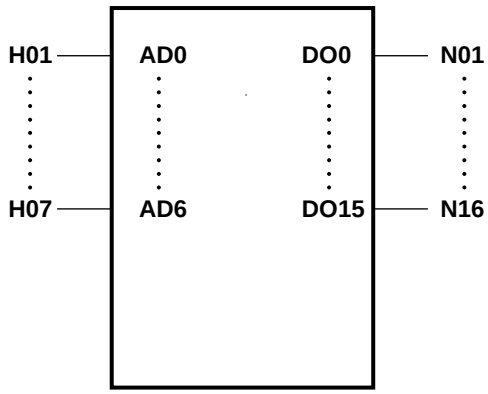
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	20770 (155 × 134)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.136

ROM BLOCK

Block Type	Function
J1CDK	**128 words × 16 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H07	AD0 : AD6	2.5 : 2.5	N01 : N16	DO0 : DO15	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD6→DO0 to DO15	(HH)	0.207	1.460	3.686	0.541	1.212	1.212
	(HL)	0.444	1.702	3.938	0.359	1.055	1.055
	(LH)	0.207	1.460	3.686	0.541	1.212	1.212
	(LL)	0.444	1.702	3.938	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	3.9381		3.9381
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.2074		

Caution This ROM block is under development in EA-9HD family.

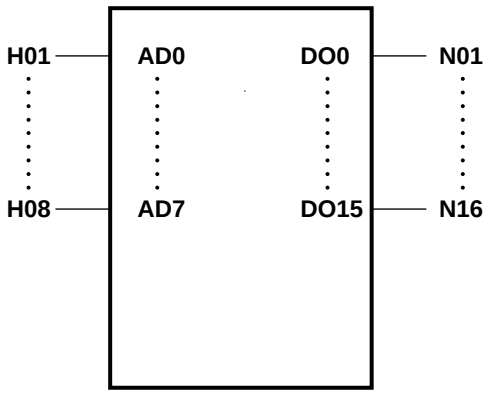
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	3129 (149 × 21)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.072

ROM BLOCK

Block Type	Function
J1CFK	**256 words × 16 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H08	AD0 : AD7	2.5 : 2.5	N01 : N16	DO0 : DO15	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD07→DO0 to DO15	(HH)	0.314	1.666	4.069	0.541	1.212	1.212
	(HL)	0.538	1.899	4.321	0.359	1.055	1.055
	(LH)	0.314	1.666	4.069	0.541	1.212	1.212
	(LL)	0.538	1.899	4.321	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.3205		4.3205
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

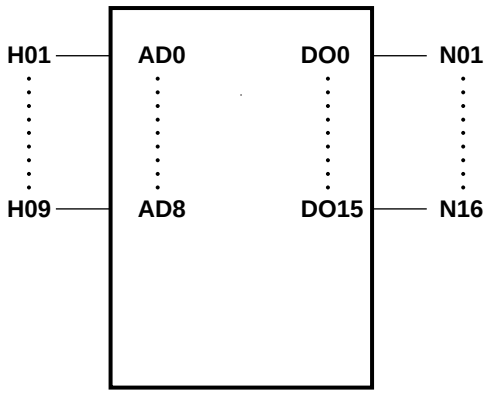
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]		
5587 (151 × 37)		Write cycle	———
		Read cycle	0.110

ROM BLOCK

Block Type	Function
J1CHK	**512 words × 16 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H09	AD0 : AD8	2.5 : 2.5	N01 : N16	DO0 : DO15	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD8→DO0 to DO15	(HH)	0.314	1.959	4.884	0.541	1.212	1.212
	(HL)	0.538	2.021	4.659	0.359	1.055	1.055
	(LH)	0.314	1.959	4.884	0.541	1.212	1.212
	(LL)	0.538	2.021	4.659	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.8836		4.8836
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

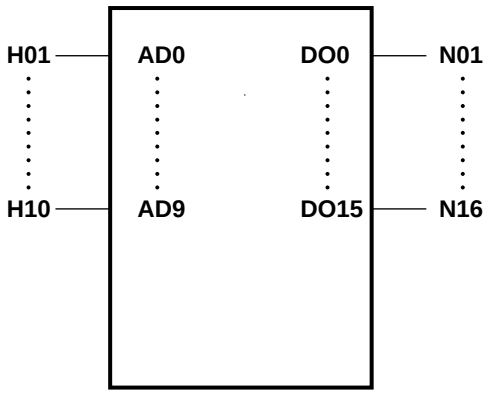
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]		
10754 (283 × 38)	Write cycle	———	
	Read cycle	0.220	

ROM BLOCK

Block Type	Function
J1CMK	**1024 words × 16 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H10	AD0 : AD9	2.5 : 2.5	N01 : N16	DO0 : DO15	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD09→DO0 to DO15	(HH)	0.417	2.279	5.590	0.541	1.212	1.212
	(HL)	0.636	2.329	5.338	0.359	1.055	1.055
	(LH)	0.417	2.279	5.590	0.541	1.212	1.212
	(LL)	0.636	2.329	5.338	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	5.5897		5.5897
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.4170		

Caution This ROM block is under development in EA-9HD family.

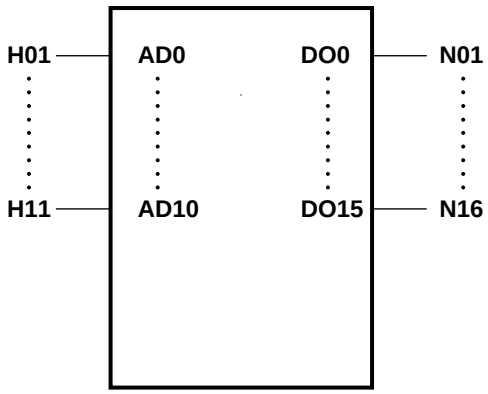
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]		
19810 (283 × 70)	Write cycle	———	
	Read cycle	0.136	

ROM BLOCK

Block Type	Function
J1CSK	**2048 words × 16 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H11	AD0 : AD10	2.5 : 2.5	N01 : N16	DO0 : DO15	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD10→DO0 to DO15	(HH)	0.417	2.558	6.365	0.541	1.212	1.212
	(HL)	0.638	2.615	6.130	0.359	1.055	1.055
	(LH)	0.417	2.558	6.365	0.541	1.212	1.212
	(LL)	0.638	2.615	6.130	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	6.3649		6.3649
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.4170		

Caution This ROM block is under development in EA-9HD family.

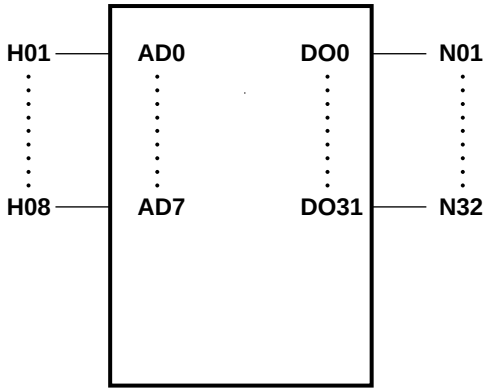
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	37922 (283 × 134)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.272

ROM BLOCK

Block Type	Function
J1HFK	**256 words × 32 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H08	AD0 : AD7	2.5 : 2.5	N01 : N32	DO0 : DO31	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD7→DO0 to DO31	(HH)	0.314	1.959	4.884	0.541	1.212	1.212
	(HL)	0.538	2.021	4.659	0.359	1.055	1.055
	(LH)	0.314	1.959	4.884	0.541	1.212	1.212
	(LL)	0.538	2.021	4.659	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	4.8836		4.8836
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

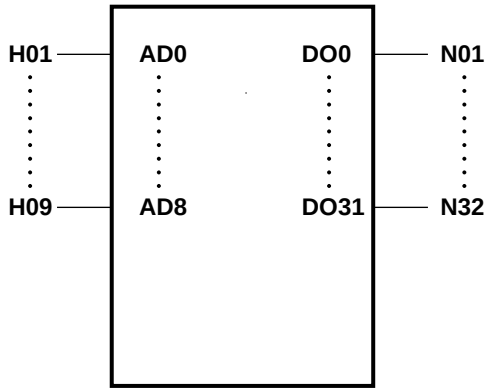
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]		
10323 (279 × 37)	Write cycle	———	
	Read cycle	0.220	

ROM BLOCK

Block Type	Function
J1HHK	**512 words × 32 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H09	AD0 : AD8	2.5 : 2.5	N01 : N32	DO0 : DO31	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD8→DO0 to DO31	(HH)	0.314	2.343	5.951	0.541	1.212	1.212
	(HL)	0.538	2.443	5.829	0.359	1.055	1.055
	(LH)	0.314	2.343	5.951	0.541	1.212	1.212
	(LL)	0.538	2.443	5.829	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	5.9505		
Address access time	t_{ACC}			5.9505
Address-output hold time	t_{AOH}	0.3135		

Caution This ROM block is under development in EA-9HD family.

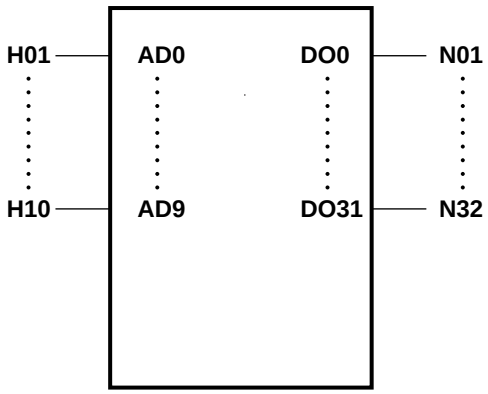
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	20482 (539 × 38)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.440

ROM BLOCK

Block Type	Function
J1HMK	**1024 words × 32 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H10	AD0 : AD9	2.5 : 2.5	N01 : N32	DO0 : DO31	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD9→DO0 to DO31	(HH)	0.417	2.803	7.046	0.541	1.212	1.212
	(HL)	0.636	2.595	6.076	0.359	1.055	1.055
	(LH)	0.417	2.803	7.046	0.541	1.212	1.212
	(LL)	0.636	2.595	6.076	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	7.0459		7.0459
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.4170		

Caution This ROM block is under development in EA-9HD family.

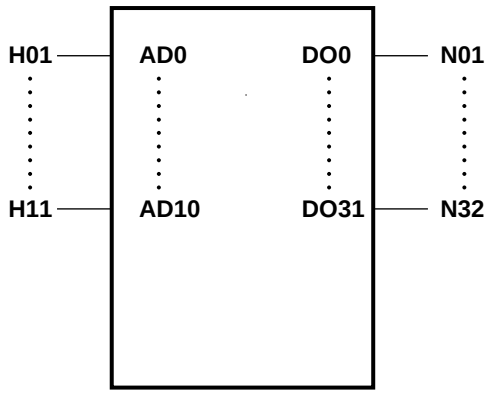
Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	Power (mW/MHz)[Note]		
37730 (539 × 70)	Write cycle	———	
	Read cycle	0.272	

ROM BLOCK

Block Type	Function
J1HSK	**2048 words × 32 bits ROM**

Logic Diagram



Truth Table

ADn	DOn	Operation
ADn	DOn	Read

ADn : Read address
DOn : Read data

Input			Output		
Name	Symbol	Fan-in	Name	Symbol	Fan-out
H01 : H11	AD0 : AD10	2.5 : 2.5	N01 : N32	DO0 : DO31	53 : 53

Switching speed

Path		t_{LD0} (ns)			t_1		
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD10→DO0 to DO31	(HH)	0.417	2.816	7.081	0.541	1.212	1.212
	(HL)	0.638	2.907	6.940	0.359	1.055	1.055
	(LH)	0.417	2.816	7.081	0.541	1.212	1.212
	(LL)	0.638	2.907	6.940	0.359	1.055	1.055

Read cycle timing[Note]

		MIN.	TYP.	MAX.
Cycle time	t_{CYCLE}	7.0812		7.0812
Address access time	t_{ACC}			
Address-output hold time	t_{AOH}	0.4170		

Caution This ROM block is under development in EA-9HD family.

Note Values of power consumption and cycle timing are preliminary values.

Equivalent Cells	73968 (552 × 134)	Power (mW/MHz)[Note]	Write cycle	———
			Read cycle	0.544

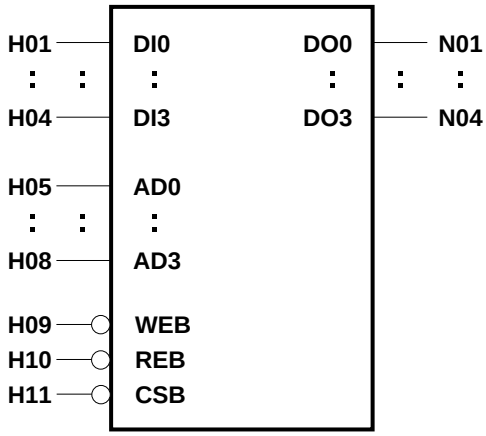
APPENDIX

BASIC RAM BLOCK

BASIC RAM BLOCK

Block Type	Function	SSI Family
K147	**16 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD3 (LH)	1.597	2.966	5.199
:	:	:	:	:	:	→DO0 to DO3 (HH)	1.597	2.966	5.199
H04	DI3	1.0	N04	DO3	26.0	(HL)	1.427	2.658	4.667
H05	AD0	1.0				(LL)	1.427	2.658	4.667
:	:	:				CSB (LL)	1.413	2.619	4.587
H08	AD3	1.0				→DO0 to DO3 (LH)	1.413	2.619	4.587
H09	WEB	1.0				(HL)	0.444	0.810	1.408
H10	REB	1.0				REB (LH)	0.405	0.696	1.170
H11	CSB	1.0				→DO0 to DO3 (HL)	0.254	0.474	0.832
						DI0 to DI3 (HH)	1.260	2.365	4.166
						→DO0 to DO3 (LL)	1.092	1.995	3.468

Equivalent Cells	48 x 9 = 432	Power (mW/MHz)	Read cycle	0.014	Rev.	1
			Write cycle	0.018		

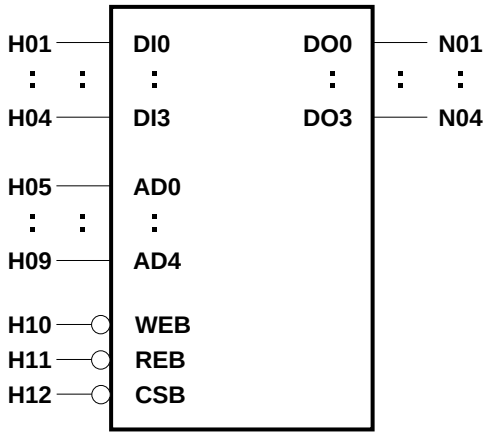
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**5.199**		
Address access time	**t_{ACA}**			**5.199**
Address output hold time	**t_{OH}**	**1.427**		
CSB access time	**t_{CSC}**			**4.587**
CSB output hold time	**t_{CSL}**	**0.444**		**1.408**
CSB output set time	**t_{CLL}**	**1.413**		
REB access time	**t_{REC}**			**1.170**
REB output hold time	**t_{REL}**	**0.254**		**0.832**
REB output set time	**t_{RLL}**	**0.405**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**3.500**		
CSB-WEB reset time	**t_{CWR}**	**2.400**		
Write pulse width	**t_{WP}**	**2.400**		
Address setup time	**t_{AS}**	**0.900**		
Address hold time	**t_{AH}**	**0.200**		
Input data setup time	**t_{DS}**	**2.400**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**2.856**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K149	**32 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**AD0 to AD4 (LH)**	**1.867**	**3.482**	**6.119**
:	:	:	:	:	:	**→DO0 to DO3 (HH)**	**1.867**	**3.482**	**6.119**
H04	**DI3**	**1.0**	**N04**	**DO3**	**26.0**	**(HL)**	**1.784**	**3.358**	**5.925**
H05	**AD0**	**1.0**				**(LL)**	**1.784**	**3.358**	**5.925**
:	:	:							
H09	**AD4**	**1.0**				**CSB (LL)**	**1.691**	**3.165**	**5.570**
H10	**WEB**	**1.0**				**→DO0 to DO3 (LH)**	**1.691**	**3.165**	**5.570**
H11	**REB**	**1.0**				**(HL)**	**0.471**	**0.843**	**1.452**
H12	**CSB**	**1.0**				**REB (LH)**	**0.416**	**0.716**	**1.207**
						→DO0 to DO3 (HL)	**0.264**	**0.489**	**0.856**
						DI0 to DI3 (HH)	**1.274**	**2.398**	**4.233**
						→DO0 to DO3 (LL)	**1.174**	**2.151**	**3.745**

Equivalent Cells	**50 x 13 = 650**	Power (mW/MHz)	Read cycle	0.015	Rev.	**1**
			Write cycle	0.019		

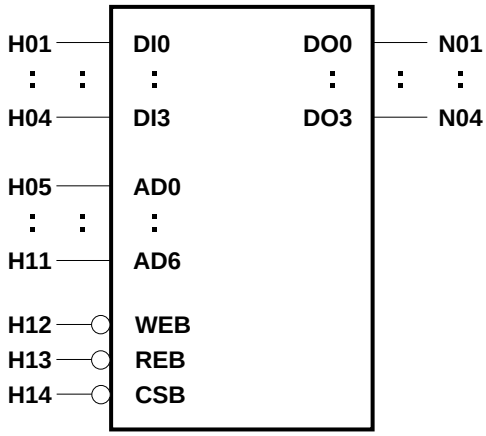
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.119**		
Address access time	**t_{ACA}**			**6.119**
Address output hold time	**t_{OH}**	**1.784**		
CSB access time	**t_{CSC}**			**5.570**
CSB output hold time	**t_{CSL}**	**0.471**		**1.452**
CSB output set time	**t_{CLL}**	**1.691**		
REB access time	**t_{REC}**			**1.207**
REB output hold time	**t_{REL}**	**0.264**		**0.856**
REB output set time	**t_{RLL}**	**0.416**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**4.300**		
CSB-WEB reset time	**t_{CWR}**	**3.200**		
Write pulse width	**t_{WP}**	**3.200**		
Address setup time	**t_{AS}**	**1.100**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.400**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**3.109**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K14D	**128 words × 4 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**AD0 to AD6 (LH)**	**2.102**	**3.880**	**6.781**
:	**:**	**:**	**:**	**:**	**:**	**→DO0 to DO3 (HH)**	**2.102**	**3.880**	**6.781**
H04	**DI3**	**1.0**	**N04**	**DO3**	**26.0**	**(HL)**	**2.053**	**3.784**	**6.609**
H05	**AD0**	**1.0**				**(LL)**	**2.053**	**3.784**	**6.609**
:	**:**	**:**				**CSB (LL)**	**2.001**	**3.725**	**6.537**
H11	**AD6**	**1.0**				**→DO0 to DO3 (LH)**	**2.001**	**3.725**	**6.537**
H12	**WEB**	**1.0**				**(HL)**	**0.503**	**0.910**	**1.574**
H13	**REB**	**1.0**				**REB (LH)**	**0.422**	**0.774**	**1.349**
H14	**CSB**	**1.0**				**→DO0 to DO3 (HL)**	**0.331**	**0.574**	**0.970**
						DI0 to DI3 (HH)	**1.380**	**2.576**	**4.528**
						→DO0 to DO3 (LL)	**1.259**	**2.325**	**4.065**

Equivalent Cells	82 x 21 = 1722	Power (mW/MHz)	Read cycle	0.018	Rev.	1
			Write cycle	0.023		

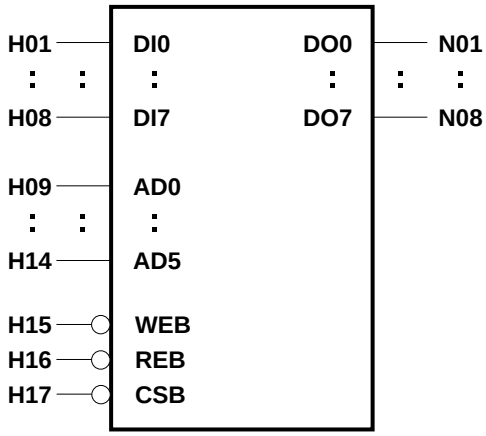
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.781**		
Address access time	**t_{ACA}**			**6.781**
Address output hold time	**t_{OH}**	**2.053**		
CSB access time	**t_{CSC}**			**6.537**
CSB output hold time	**t_{CSL}**	**0.503**		**1.574**
CSB output set time	**t_{CLL}**	**2.001**		
REB access time	**t_{REC}**			**1.349**
REB output hold time	**t_{REL}**	**0.331**		**0.970**
REB output set time	**t_{RLL}**	**0.422**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**4.300**		
CSB-WEB reset time	**t_{CWR}**	**3.300**		
Write pulse width	**t_{WP}**	**3.300**		
Address setup time	**t_{AS}**	**1.000**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.100**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**3.967**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K18B	**64 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD5 (LH)	2.027	3.777	6.632
:	:	:	:	:	:	→DO0 to DO7 (HH)	2.027	3.777	6.632
H08	DI7	1.0	N08	DO7	26.0	(HL)	2.006	3.707	6.481
H09	AD0	1.0				(LL)	2.006	3.707	6.481
:	:	:							
H14	AD5	1.0				CSB (LL)	1.916	3.562	6.246
H15	WEB	1.0				→DO0 to DO7 (LH)	1.916	3.562	6.246
H16	REB	1.0				(HL)	0.526	0.974	1.706
H17	CSB	1.0							
						REB (LH)	0.491	0.860	1.461
						→DO0 to DO7 (HL)	0.369	0.664	1.145
						DI0 to DI7 (HH)	1.345	2.534	4.472
						→DO0 to DO7 (LL)	1.245	2.287	3.987

Equivalent Cells	94 x 21 = 1974	Power (mW/MHz)	Read cycle	0.023	Rev.	1
			Write cycle	0.032		

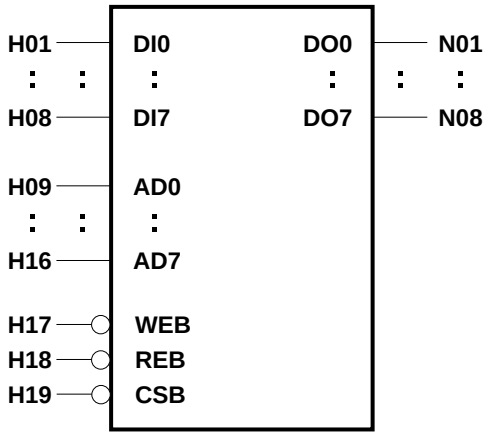
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.632**		
Address access time	**t_{ACA}**			**6.632**
Address output hold time	**t_{OH}**	**2.006**		
CSB access time	**t_{CSC}**			**6.246**
CSB output hold time	**t_{CSL}**	**0.526**		**1.706**
CSB output set time	**t_{CLL}**	**1.916**		
REB access time	**t_{REC}**			**1.461**
REB output hold time	**t_{REL}**	**0.369**		**1.145**
REB output set time	**t_{RLL}**	**0.491**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**4.500**		
CSB-WEB reset time	**t_{CWR}**	**3.200**		
Write pulse width	**t_{WP}**	**3.200**		
Address setup time	**t_{AS}**	**1.300**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.000**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**3.994**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K18F	**256 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD7 (LH)	2.323	4.236	7.357
:	:	:	:	:	:	→DO0 to DO7 (HH)	2.323	4.236	7.357
H08	DI7	1.0	N08	DO7	26.0	(HL)	2.329	4.282	7.470
H09	AD0	1.0				(LL)	2.329	4.282	7.470
:	:	:							
H16	AD7	1.0				CSB (LL)	2.241	4.054	7.012
H17	WEB	1.0				→DO0 to DO7 (LH)	2.241	4.054	7.012
H18	REB	1.0				(HL)	0.591	1.096	1.920
H19	CSB	1.0							
						REB (LH)	0.538	0.968	1.669
						→DO0 to DO7 (HL)	0.420	0.797	1.413
						DI0 to DI7 (HH)	2.267	4.190	7.327
						→DO0 to DO7 (LL)	2.193	4.045	7.066

Equivalent Cells	160 x 37 = 5920	Power (mW/MHz)	Read cycle	0.055	Rev.	1
			Write cycle	0.069		

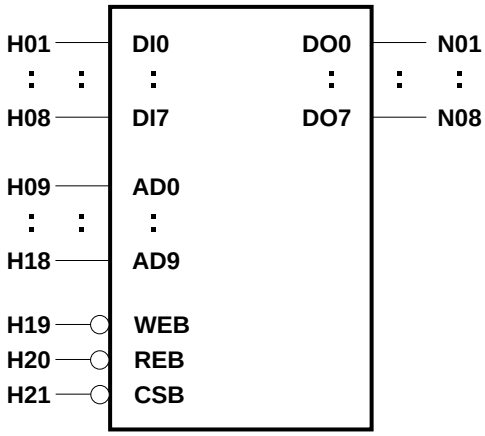
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.470**		
Address access time	**t_{ACA}**			**7.470**
Address output hold time	**t_{OH}**	**2.006**		
CSB access time	**t_{CSC}**			**7.012**
CSB output hold time	**t_{CSL}**	**0.591**		**1.920**
CSB output set time	**t_{CLL}**	**2.241**		
REB access time	**t_{REC}**			**1.669**
REB output hold time	**t_{REL}**	**0.420**		**1.413**
REB output set time	**t_{RLL}**	**0.538**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.000**		
CSB-WEB reset time	**t_{CWR}**	**3.400**		
Write pulse width	**t_{WP}**	**3.400**		
Address setup time	**t_{AS}**	**1.600**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**3.600**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**5.454**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K18M	**1024 words × 8 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD9 (LH)	2.914	5.247	9.052
:	:	:	:	:	:	→DO0 to DO7 (HH)	2.914	5.247	9.052
H08	DI7	1.0	N08	DO7	26.0	(HL)	3.023	5.586	9.769
H09	AD0	1.0				(LL)	3.023	5.586	9.769
:	:	:							
H18	AD9	1.0				CSB (LL)	2.733	5.056	8.845
H19	WEB	1.0				→DO0 to DO7 (LH)	2.733	5.056	8.845
H20	REB	1.0				(HL)	0.755	1.393	2.434
H21	CSB	1.0							
						REB (LH)	0.670	1.169	1.982
						→DO0 to DO7 (HL)	0.559	1.064	1.887
						DI0 to DI7 (HH)	2.830	5.244	9.183
						→DO0 to DO7 (LL)	2.786	5.127	8.946

Equivalent Cells	316 x 69 = 21804	Power (mW/MHz)	Read cycle	0.068	Rev.	1
			Write cycle	0.097		

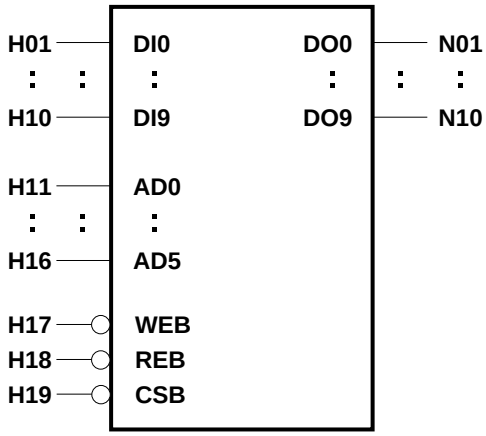
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.769**		
Address access time	**t_{ACA}**			**9.769**
Address output hold time	**t_{OH}**	**2.006**		
CSB access time	**t_{CSC}**			**8.845**
CSB output hold time	**t_{CSL}**	**0.755**		**2.434**
CSB output set time	**t_{CLL}**	**2.733**		
REB access time	**t_{REC}**			**1.982**
REB output hold time	**t_{REL}**	**0.559**		**1.887**
REB output set time	**t_{RLL}**	**0.670**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.600**		
CSB-WEB reset time	**t_{CWR}**	**4.400**		
Write pulse width	**t_{WP}**	**4.400**		
Address setup time	**t_{AS}**	**1.200**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**4.600**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**7.037**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K1AB	**64 words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD5 (LH)	2.097	3.877	6.782
:	:	:	:	:	:	→DO0 to DO9 (HH)	2.097	3.877	6.782
H10	DI9	1.0	N10	DO9	26.0	(HL)	2.027	3.773	6.620
H11	AD0	1.0				(LL)	2.027	3.773	6.620
:	:	:				CSB (LL)	1.936	3.576	6.252
H16	AD5	1.0				→DO0 to DO9 (LH)	1.936	3.576	6.252
H17	WEB	1.0				(HL)	0.588	1.052	1.810
H18	REB	1.0				REB (LH)	0.505	0.886	1.508
H19	CSB	1.0				→DO0 to DO9 (HL)	0.399	0.710	1.216
						DI0 to DI9 (HH)	1.347	2.529	4.457
						→DO0 to DO9 (LL)	1.252	2.299	4.008

Equivalent Cells	116 x 21 = 2436	Power (mW/MHz)	Read cycle	0.029	Rev.	1
			Write cycle	0.040		

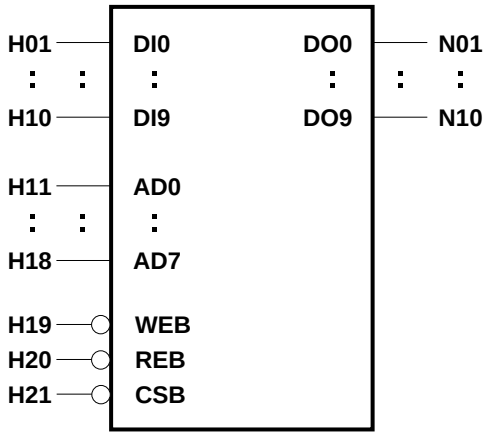
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.782**		
Address access time	**t_{ACA}**			**6.782**
Address output hold time	**t_{OH}**	**2.027**		
CSB access time	**t_{CSC}**			**6.252**
CSB output hold time	**t_{CSL}**	**0.588**		**1.810**
CSB output set time	**t_{CLL}**	**1.936**		
REB access time	**t_{REC}**			**1.508**
REB output hold time	**t_{REL}**	**0.399**		**1.216**
REB output set time	**t_{RLL}**	**0.505**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**4.600**		
CSB-WEB reset time	**t_{CWR}**	**3.300**		
Write pulse width	**t_{WP}**	**3.300**		
Address setup time	**t_{AS}**	**1.300**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.000**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**4.073**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K1AF	**256 words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**AD0 to AD7 (LH)**	**2.353**	**4.389**	**7.711**
:	:	:	:	:	:	**→DO0 to DO9 (HH)**	**2.353**	**4.389**	**7.711**
H10	**DI9**	**1.0**	**N10**	**DO9**	**26.0**	**(HL)**	**2.370**	**4.370**	**7.632**
H11	**AD0**	**1.0**				**(LL)**	**2.370**	**4.370**	**7.632**
:	:	:							
H18	**AD7**	**1.0**				**CSB (LL)**	**2.335**	**4.237**	**7.341**
H19	**WEB**	**1.0**				**→DO0 to DO9 (LH)**	**2.335**	**4.237**	**7.341**
H20	**REB**	**1.0**				**(HL)**	**0.669**	**1.203**	**2.075**
H21	**CSB**	**1.0**							
						REB (LH)	**0.560**	**1.021**	**1.773**
						→DO0 to DO9 (HL)	**0.442**	**0.866**	**1.557**
						DI0 to DI9 (HH)	**2.268**	**4.202**	**7.359**
						→DO0 to DO9 (LL)	**2.244**	**4.095**	**7.114**

Equivalent Cells	**198 x 37 = 7326**	Power (mW/MHz)	Read cycle	0.067	Rev.	**1**
			Write cycle	0.097		

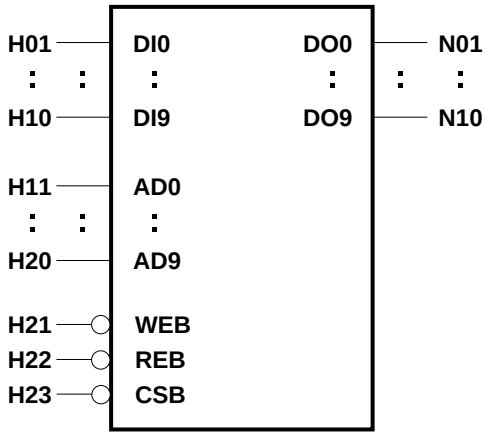
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**7.711**		
Address access time	**t_{ACA}**			**7.711**
Address output hold time	**t_{OH}**	**2.027**		
CSB access time	**t_{CSC}**			**7.341**
CSB output hold time	**t_{CSL}**	**0.669**		**2.075**
CSB output set time	**t_{CLL}**	**2.335**		
REB access time	**t_{REC}**			**1.773**
REB output hold time	**t_{REL}**	**0.442**		**1.557**
REB output set time	**t_{RLL}**	**0.560**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.000**		
CSB-WEB reset time	**t_{CWR}**	**3.400**		
Write pulse width	**t_{WP}**	**3.400**		
Address setup time	**t_{AS}**	**1.600**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**3.600**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**5.593**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K1AM	**1024 words × 10 bits Single-port RAM**	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
DOn : Output data
WEB : Write enable
REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**AD0 to AD9 (LH)**	**2.975**	**5.388**	**9.325**
:	**:**	**:**	**:**	**:**	**:**	**→DO0 to DO9 (HH)**	**2.975**	**5.388**	**9.325**
H10	**DI9**	**1.0**	**N10**	**DO9**	**26.0**	**(HL)**	**3.128**	**5.783**	**10.110**
H11	**AD0**	**1.0**				**(LL)**	**3.128**	**5.783**	**10.110**
:	**:**	**:**				**CSB (LL)**	**2.907**	**5.229**	**9.017**
H20	**AD9**	**1.0**				**→DO0 to DO9 (LH)**	**2.907**	**5.229**	**9.017**
H21	**WEB**	**1.0**				**(HL)**	**0.838**	**1.533**	**2.669**
H22	**REB**	**1.0**				**REB (LH)**	**0.766**	**1.313**	**2.205**
H23	**CSB**	**1.0**				**→DO0 to DO9 (HL)**	**0.638**	**1.172**	**2.042**
						DI0 to DI9 (HH)	**2.831**	**5.226**	**9.134**
						→DO0 to DO9 (LL)	**2.776**	**5.150**	**9.023**

Equivalent Cells	**392 x 69 = 27048**	Power (mW/MHz)	Read cycle	0.082	Rev.	**1**
			Write cycle	0.118		

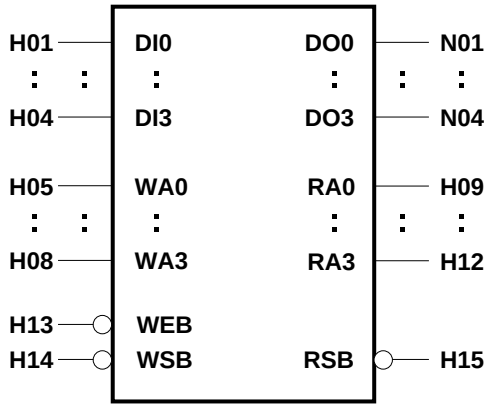
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**10.110**		
Address access time	**t_{ACA}**			**10.110**
Address output hold time	**t_{OH}**	**2.027**		
CSB access time	**t_{CSC}**			**9.017**
CSB output hold time	**t_{CSL}**	**0.838**		**2.669**
CSB output set time	**t_{CLL}**	**2.907**		
REB access time	**t_{REC}**			**2.205**
REB output hold time	**t_{REL}**	**0.638**		**2.042**
REB output set time	**t_{RLL}**	**0.766**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.000**		
CSB-WEB reset time	**t_{CWR}**	**4.400**		
Write pulse width	**t_{WP}**	**4.400**		
Address setup time	**t_{AS}**	**1.400**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**4.600**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**7.269**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K247	**16words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**				
:	:	:	:	:	:				
H04	**DI3**	**1.0**	**N04**	**DO3**	**26.0**				
H05	**WA0**	**1.0**							
:	:	:							
H08	**WA3**	**1.0**							
H09	**RA0**	**1.0**							
:	:	:							
H12	**RA3**	**1.0**							
H13	**WEB**	**1.0**							
H14	**WSB**	**1.0**							
H15	**RSB**	**1.0**							
						RA0 to RA3 (LH)	**0.980**	**1.645**	**2.728**
						→DO0 to DO3 (HH)	**0.980**	**1.645**	**2.728**
						(HL)	**0.982**	**1.796**	**3.125**
						(LL)	**0.982**	**1.796**	**3.125**
						RSB (LH)	**0.275**	**0.460**	**0.762**
						→DO0 to DO3 (HL)	**0.219**	**0.369**	**0.613**
						DI0 to DI3 (HH)	**1.394**	**2.338**	**3.880**
						→DO0 to DO3 (LL)	**1.183**	**2.168**	**3.776**

Equivalent Cells	**58 x 11 = 638**	Power (mW/MHz)	Read cycle	0.016	Rev.	**1**
			Write cycle	0.023		

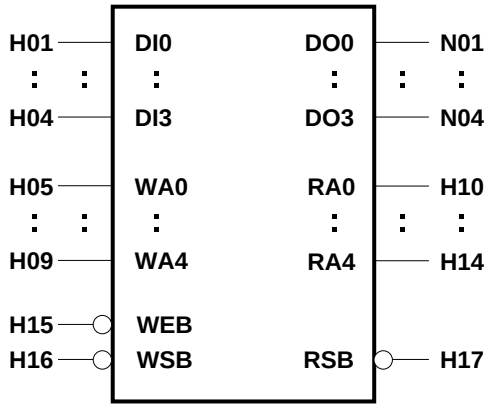
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**3.125**		
Address access time	**t_{ACA}**			**3.125**
Address output hold time	**t_{OH}**	**0.980**		
REB access time	**t_{REC}**			**0.762**
REB output hold time	**t_{REL}**	**0.219**		**0.613**
REB output set time	**t_{RLL}**	**0.275**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**4.000**		
CSB-WEB reset time	**t_{CWR}**	**2.200**		
Write pulse width	**t_{WP}**	**2.200**		
Address setup time	**t_{AS}**	**1.800**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**1.600**		
Input data hold time	**t_{DH}**	**0.100**		
WEB access time	**t_{WEC}**			**4.562**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K249	**32 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**				
:	:	:	:	:	:				
H04	**DI3**	**1.0**	**N04**	**DO3**	**26.0**				
H05	**WA0**	**1.0**				**RA0 to RA4 (LH)**	**1.051**	**1.753**	**2.899**
:	:	:				**→DO0 to DO3 (HH)**	**1.051**	**1.753**	**2.899**
H09	**WA4**	**1.0**				**(HL)**	**1.053**	**1.985**	**3.506**
H10	**RA0**	**1.0**				**(LL)**	**1.053**	**1.985**	**3.506**
:	:	:							
H14	**RA4**	**1.0**				**RSB (LH)**	**0.281**	**0.479**	**0.801**
H15	**WEB**	**1.0**				**→DO0 to DO3 (HL)**	**0.235**	**0.411**	**0.698**
H16	**WSB**	**1.0**							
H17	**RSB**	**1.0**				**DI0 to DI3 (HH)**	**1.194**	**2.050**	**3.446**
						→DO0 to DO3 (LL)	**1.095**	**2.056**	**3.624**

Equivalent Cells	**106 x 11 = 1166**	Power (mW/MHz)	Read cycle	0.020	Rev.	**1**
			Write cycle	0.030		

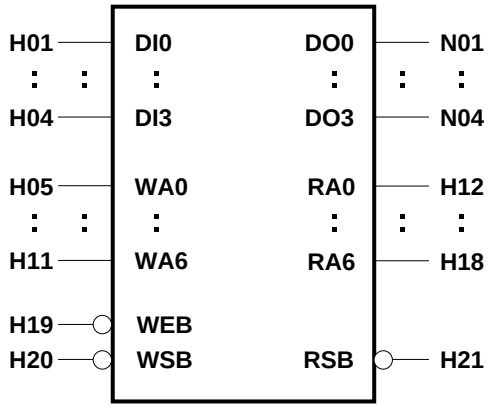
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**3.506**		
Address access time	**t_{ACA}**			**3.506**
Address output hold time	**t_{OH}**	**1.051**		
REB access time	**t_{REC}**			**0.801**
REB output hold time	**t_{REL}**	**0.235**		**0.698**
REB output set time	**t_{RLL}**	**0.281**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**4.600**		
CSB-WEB reset time	**t_{CWR}**	**2.600**		
Write pulse width	**t_{WP}**	**2.600**		
Address setup time	**t_{AS}**	**2.000**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.600**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**4.881**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K24D	**128 words × 4 bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path IN → OUT		t_{LD0} (ns) MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**					
:	:	:	:	:	:					
H04	**DI3**	**1.0**	**N04**	**DO3**	**26.0**					
H05	**WA0**	**1.0**								
:	:	:								
H11	**WA6**	**1.0**								
H12	**RA0**	**1.0**								
:	:	:								
H18	**RA6**	**1.0**								
H19	**WEB**	**1.0**								
H20	**WSB**	**1.0**								
H21	**RSB**	**1.0**								
						RA0 to RA6 →DO0 to DO3	**(LH)**	**1.287**	**2.197**	**3.680**
							(HH)	**1.287**	**2.197**	**3.680**
							(HL)	**1.301**	**2.432**	**4.277**
							(LL)	**1.301**	**2.432**	**4.277**
						RSB →DO0 to DO3	**(LH)**	**0.283**	**0.505**	**0.866**
							(HL)	**0.315**	**0.485**	**0.764**
						DI0 to DI3 →DO0 to DO3	**(HH)**	**1.717**	**2.913**	**4.864**
							(LL)	**1.541**	**2.814**	**4.892**

Equivalent Cells	**208 x 18 = 3744**	Power (mW/MHz)	Read cycle	0.028	Rev.	**1**
			Write cycle	0.040		

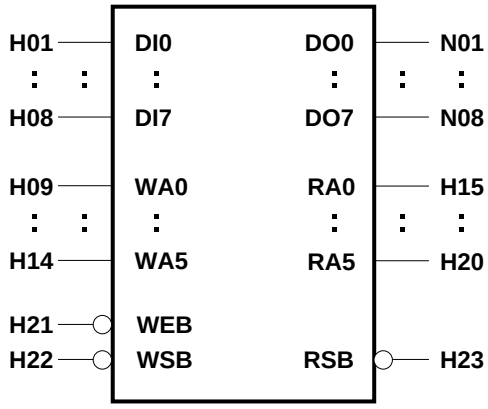
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**4.277**		
Address access time	**t_{ACA}**			**4.277**
Address output hold time	**t_{OH}**	**1.287**		
REB access time	**t_{REC}**			**0.866**
REB output hold time	**t_{REL}**	**0.315**		**0.764**
REB output set time	**t_{RLL}**	**0.283**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.400**		
CSB-WEB reset time	**t_{CWR}**	**2.800**		
Write pulse width	**t_{WP}**	**2.800**		
Address setup time	**t_{AS}**	**2.600**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.700**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**5.463**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K28B	**64 words × 8bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**				
:	:	:	:	:	:				
H08	**DI7**	**1.0**	**N08**	**DO7**	**26.0**				
H09	**WA0**	**1.0**							
:	:	:							
H14	**WA5**	**1.0**							
H15	**RA0**	**1.0**							
:	:	:							
H20	**RA5**	**1.0**							
H21	**WEB**	**1.0**							
H22	**WSB**	**1.0**							
H23	**RSB**	**1.0**							
						RA0 to RA5 (LH)	**1.278**	**2.156**	**3.589**
						→DO0 to DO7 (HH)	**1.278**	**2.156**	**3.589**
						(HL)	**1.233**	**2.366**	**4.213**
						(LL)	**1.233**	**2.366**	**4.213**
						RSB (LH)	**0.370**	**0.603**	**0.983**
						→DO0 to DO7 (HL)	**0.324**	**0.552**	**0.925**
						DI0 to DI7 (HH)	**1.695**	**2.825**	**4.668**
						→DO0 to DO7 (LL)	**1.498**	**2.743**	**4.774**

Equivalent Cells	**208 x 15 = 3120**	Power (mW/MHz)	Read cycle	0.041	Rev.	**1**
			Write cycle	0.054		

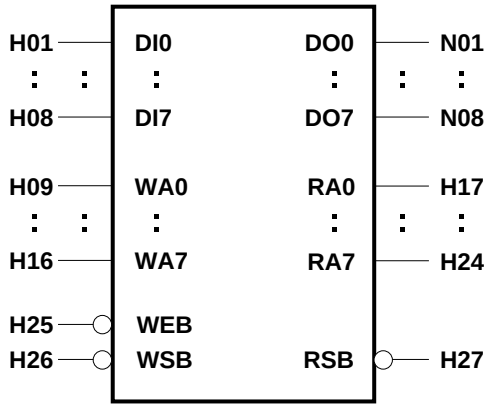
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**4.213**		
Address access time	**t_{ACA}**			**4.213**
Address output hold time	**t_{OH}**	**1.233**		
REB access time	**t_{REC}**			**0.983**
REB output hold time	**t_{REL}**	**0.324**		**0.925**
REB output set time	**t_{RLL}**	**0.370**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.500**		
CSB-WEB reset time	**t_{CWR}**	**2.800**		
Write pulse width	**t_{WP}**	**2.800**		
Address setup time	**t_{AS}**	**2.700**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.400**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**5.450**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K28F	**256 words × 8bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**				
:	:	:	:	:	:				
H08	**DI7**	**1.0**	**N08**	**DO7**	**26.0**				
H09	**WA0**	**1.0**				**RA0 to RA7 (LH)**	**1.774**	**3.014**	**5.036**
:	:	:				**→DO0 to DO7 (HH)**	**1.774**	**3.014**	**5.036**
H16	**WA7**	**1.0**				**(HL)**	**1.880**	**3.400**	**5.879**
H17	**RA0**	**1.0**				**(LL)**	**1.880**	**3.400**	**5.879**
:	:	:							
H24	**RA7**	**1.0**				**RSB (LH)**	**0.392**	**0.687**	**1.169**
H25	**WEB**	**1.0**				**→DO0 to DO7 (HL)**	**0.416**	**0.678**	**1.105**
H26	**WSB**	**1.0**							
H27	**RSB**	**1.0**				**DI0 to DI7 (HH)**	**1.801**	**3.060**	**5.114**
						→DO0 to DO7 (LL)	**1.609**	**2.960**	**5.163**

Equivalent Cells	**400 x25 = 10000**	Power (mW/MHz)	Read cycle	0.091	Rev.	**1**
			Write cycle	0.124		

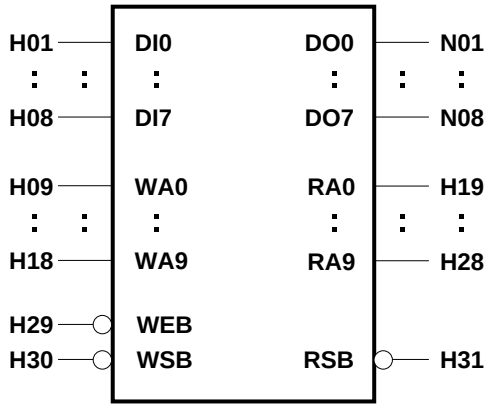
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**5.879**		
Address access time	**t_{ACA}**			**5.879**
Address output hold time	**t_{OH}**	**1.774**		
REB access time	**t_{REC}**			**1.169**
REB output hold time	**t_{REL}**	**0.416**		**1.105**
REB output set time	**t_{RLL}**	**0.392**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.000**		
CSB-WEB reset time	**t_{CWR}**	**3.400**		
Write pulse width	**t_{WP}**	**3.400**		
Address setup time	**t_{AS}**	**2.600**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.200**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**6.644**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K28M	**1024 words × 8bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**RA0 to RA9 (LH)**	**2.481**	**4.142**	**6.852**
:	:	:	:	:	:	**→DO0 to DO7 (HH)**	**2.481**	**4.142**	**6.852**
H08	**DI7**	**1.0**	**N08**	**DO7**	**26.0**	**(HL)**	**2.685**	**4.941**	**8.621**
H09	**WA0**	**1.0**				**(LL)**	**2.685**	**4.941**	**8.621**
:	:	:							
H18	**WA9**	**1.0**				**RSB (LH)**	**0.479**	**0.785**	**1.285**
H19	**RA0**	**1.0**				**→DO0 to DO7 (HL)**	**0.430**	**0.724**	**1.205**
:	:	:							
H28	**RA9**	**1.0**				**DI0 to DI7 (HH)**	**2.175**	**3.676**	**6.127**
H29	**WEB**	**1.0**				**→DO0 to DO7 (LL)**	**1.876**	**3.484**	**6.107**
H30	**WSB**	**1.0**							
H31	**RSB**	**1.0**							

Equivalent Cells	**784 x 47 = 36848**	Power (mW/MHz)	Read cycle	0.105	Rev.	**1**
			Write cycle	0.159		

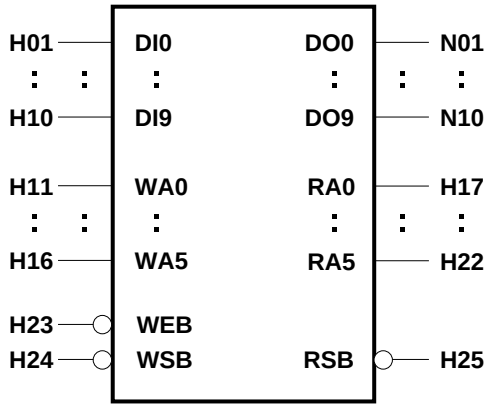
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**8.621**		
Address access time	**t_{ACA}**			**8.621**
Address output hold time	**t_{OH}**	**2.480**		
REB access time	**t_{REC}**			**1.285**
REB output hold time	**t_{REL}**	**0.430**		**1.205**
REB output set time	**t_{RLL}**	**0.479**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**7.400**		
CSB-WEB reset time	**t_{CWR}**	**4.800**		
Write pulse width	**t_{WP}**	**4.800**		
Address setup time	**t_{AS}**	**2.600**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.600**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**9.006**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K2AB	**64 words × 10bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**RA0 to RA5 (LH)**	**1.296**	**2.189**	**3.645**
:	:	:	:	:	:	**→DO0 to DO9 (HH)**	**1.296**	**2.189**	**3.645**
H10	**DI9**	**1.0**	**N10**	**DO9**	**26.0**	**(HL)**	**1.316**	**2.495**	**4.419**
H11	**WA0**	**1.0**				**(LL)**	**1.316**	**2.495**	**4.419**
:	:	:							
H16	**WA5**	**1.0**				**RSB (LH)**	**0.380**	**0.636**	**1.053**
H17	**RA0**	**1.0**				**→DO0 to DO9 (HL)**	**0.363**	**0.613**	**1.022**
:	:	:							
H22	**RA5**	**1.0**				**DI0 to DI9 (HH)**	**1.695**	**2.825**	**4.669**
H23	**WEB**	**1.0**				**→DO0 to DO9 (LL)**	**1.498**	**2.743**	**4.773**
H24	**WSB**	**1.0**							
H25	**RSB**	**1.0**							

Equivalent Cells	**256x 15 = 3840**	Power (mW/MHz)	Read cycle	0.050	Rev.	**1**
			Write cycle	0.065		

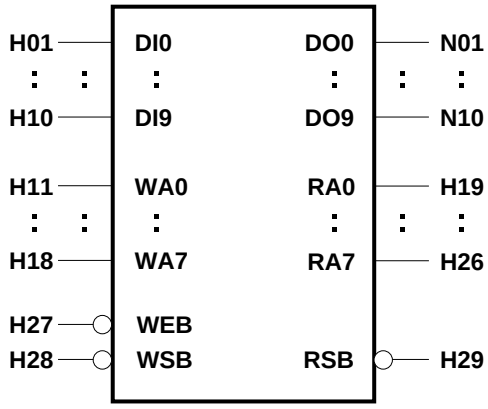
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**4.419**		
Address access time	**t_{ACA}**			**4.419**
Address output hold time	**t_{OH}**	**1.498**		
REB access time	**t_{REC}**			**1.053**
REB output hold time	**t_{REL}**	**0.363**		**1.022**
REB output set time	**t_{RLL}**	**0.380**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**5.700**		
CSB-WEB reset time	**t_{CWR}**	**2.900**		
Write pulse width	**t_{WP}**	**2.900**		
Address setup time	**t_{AS}**	**2.800**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.300**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**5.841**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K2AF	**256words × 10bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**RA0 to RA7 (LH)**	**1.840**	**3.074**	**5.087**
:	:	:	:	:	:	**→DO0 to DO9 (HH)**	**1.840**	**3.074**	**5.087**
H10	**DI9**	**1.0**	**N10**	**DO9**	**26.0**	**(HL)**	**1.985**	**3.629**	**6.311**
H11	**WA0**	**1.0**				**(LL)**	**1.985**	**3.629**	**6.311**
:	:	:							
H18	**WA7**	**1.0**							
H19	**RA0**	**1.0**				**RSB (LH)**	**0.474**	**0.790**	**1.305**
:	:	:				**→DO0 to DO9 (HL)**	**0.493**	**0.771**	**1.226**
H26	**RA7**	**1.0**							
H27	**WEB**	**1.0**				**DI0 to DI9 (HH)**	**1.793**	**3.052**	**5.105**
H28	**WSB**	**1.0**				**→DO0 to DO9 (LL)**	**1.614**	**2.963**	**5.163**
H29	**RSB**	**1.0**							

Equivalent Cells	**496x 25 = 12400**	Power (mW/MHz)	Read cycle	0.109	Rev.	**1**
			Write cycle	0.147		

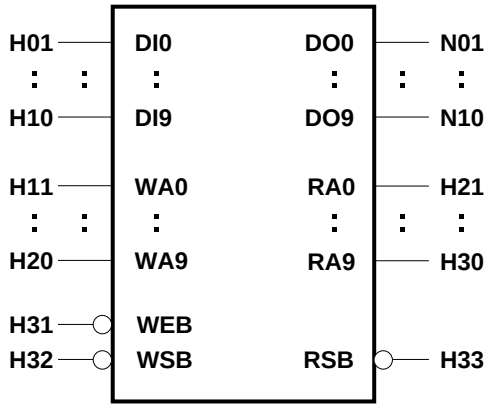
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**6.311**		
Address access time	**t_{ACA}**			**6.311**
Address output hold time	**t_{OH}**	**1.839**		
REB access time	**t_{REC}**			**1.305**
REB output hold time	**t_{REL}**	**0.493**		**1.226**
REB output set time	**t_{RLL}**	**0.474**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**6.800**		
CSB-WEB reset time	**t_{CWR}**	**3.800**		
Write pulse width	**t_{WP}**	**3.800**		
Address setup time	**t_{AS}**	**3.000**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**2.200**		
Input data hold time	**t_{DH}**	**0.000**		
WEB access time	**t_{WEC}**			**7.229**

BASIC RAM BLOCK

Block Type	Function	SSI Family
K2AM	**1024words × 10bits Dual-port RAM**	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant
WAn : A-port address (Write)
WEB : Write enable
RAn : B-port address (Read)
DOn : Output data
DIn : Input data
WSB : A-port select
DMn : Memory data
RSB : B-port select

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	t_{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.
H01	**DI0**	**1.0**	**N01**	**DO0**	**26.0**	**RA0 to RA9 (LH)**	**2.589**	**4.386**	**7.317**
:	:	:	:	:	:	**→DO0 to DO9 (HH)**	**2.589**	**4.386**	**7.317**
H10	**DI9**	**1.0**	**N10**	**DO9**	**26.0**	**(HL)**	**2.894**	**5.337**	**9.324**
H11	**WA0**	**1.0**				**(LL)**	**2.894**	**5.337**	**9.324**
:	:	:							
H20	**WA9**	**1.0**				**RSB (LH)**	**0.484**	**0.832**	**1.401**
H21	**RA0**	**1.0**				**→DO0 to DO9 (HL)**	**0.509**	**0.833**	**1.363**
:	:	:							
H30	**RA9**	**1.0**				**DI0 to DI9 (HH)**	**2.174**	**3.678**	**6.131**
H31	**WEB**	**1.0**				**→DO0 to DO9 (LL)**	**1.876**	**3.484**	**6.107**
H32	**WSB**	**1.0**							
H33	**RSB**	**1.0**							

Equivalent Cells	**976x 47 = 45872**	Power (mW/MHz)	Read cycle	0.123	Rev.	**1**
			Write cycle	0.194		

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{RCA}**	**9.324**		
Address access time	**t_{ACA}**			**9.324**
Address output hold time	**t_{OH}**	**2.589**		
REB access time	**t_{REC}**			**1.401**
REB output hold time	**t_{REL}**	**0.509**		**1.363**
REB output set time	**t_{RLL}**	**0.484**		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	**t_{WC}**	**8.400**		
CSB-WEB reset time	**t_{CWR}**	**5.600**		
Write pulse width	**t_{WP}**	**5.600**		
Address setup time	**t_{AS}**	**2.800**		
Address hold time	**t_{AH}**	**0.000**		
Input data setup time	**t_{DS}**	**3.200**		
Input data hold time	**t_{DH}**	**0.100**		
WEB access time	**t_{WEC}**			**9.778**

お問い合わせ先

【技術的なお問い合わせ先】

ＮＥＣ半導体テクニカルホットライン
（電話：午前 9:00～12:00，午後 1:00～5:00）

電　話　：044−435−9494
FAX　：044−435−9608
E-mail　：s-info@saed.tmg.nec.co.jp

【営業関係お問い合わせ先】

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太　田　(0276)46−4014
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福　岡　(092)261−2806

【資料の請求先】

上記営業関係お問い合わせ先またはNEC特約店へお申しつけください。

【インターネット電子デバイス・ニュース】

NECエレクトロンデバイスの情報がインターネットでご覧になれます。　URL（アドレス）　http://www.ic.nec.co.jp/

アンケート記入のお願い

お手数ですが，このドキュメントに対するご意見をお寄せください。今後のドキュメント作成の参考にさせていただきます。

［ドキュメント名］CMOS-9HD Family, EA-9HD Family Memory Ver.4.0 Block Library
（A13071JJ4V0BL00（4th edition））

［お名前など］（さしつかえのない範囲で）

御社名（学校名，その他）　（　　）
ご住所　（　　）
お電話番号　（　　）
お仕事の内容　（　　）
お名前　（　　）

1．ご評価（各欄に○をご記入ください）

項　　目	大変良い	良　い	普　通	悪　い	大変悪い
全体の構成					
説明内容					
用語解説					
調べやすさ					
デザイン，字の大きさなど					
その他（　　）					
（　　）					

2．わかりやすい所（第　章，第　章，第　章，第　章，その他　　）
理由［　　］

3．わかりにくい所（第　章，第　章，第　章，第　章，その他　　）
理由［　　］

4．ご意見，ご要望

5．このドキュメントをお届けしたのは
NEC販売員，特約店販売員，その他（　　）

ご協力ありがとうございました。
下記あてにFAXで送信いただくか，最寄りの販売員にコピーをお渡しください。

日本電気(株) NEC エレクトロンデバイス
半導体テクニカルホットライン
FAX：（044）435-9608

2000.6

キリトリ