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April 1st, 2010
Renesas Electronics Corporation

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Block Library

CMOS-9HD Family, EA-9HD Family

CMOS Gate Array, CMOS Embedded Array

Memory Ver.4.0

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Date Published October 2000 N CP(K)

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[MEMO]

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- Device availability
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- Availability of related technical literature
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Major Revisions in this Edition

Page	Description
Throughout	Addition of EA-9HD Family
p. 185	Addition of Chapter 3 ROM BLOCK
p. 223 in previous edition	Deletion from previous edition of APPENDIX B BLOCK LIST (by Function)

The mark ★ shows major revised points.

PREFACE

1. Introduction

Memory blocks of CMOS-9HD family and EA-9HD family are listed in this manual.

When carrying out circuit design, it is requested that the **CMOS-9HD Family Design Manual(A12985E)**, **EA-9HD Family Design Manual (A13282E)** should also be read. Furthermore, as there are occasions when this block library is changed without advance notice, please contact your local NEC ASIC design center.

Please observe all items listed in this manual(general matters,cautions,limitations).

If you don't observe these things,degradation in the quality and performance of LSI's or abnormal operation may occur.

This library is composed of Preface, Contents, three chapters, and appendix as explained below.

(1) PREFACE

The usage of this library, meanings of terminologies and some information are described.

(2) CONTENTS

This CONTENTS is useful when searching a block from its name

(3) CHAPTER 1 HIGH DENSITY SINGLE-PORT RAM BLOCK (Soft Macro)

(4) CHAPTER 2 HIGH DENSITY DUAL-PORT RAM BLOCK (Soft Macro)

(5) CHAPTER 3 ROM BLOCK

(6) APPENDIX BASIC RAM BLOCK

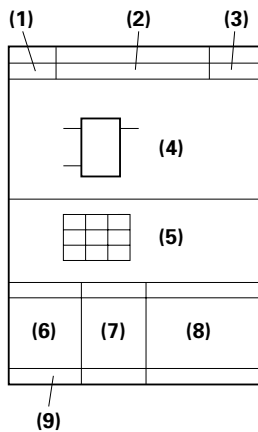
CHAPTER 1 to 3 and APPENDIX list each block in alphanumerical order. Each page describes a logic symbol, a truth table, I/O data and delay time with an integrated format.

High-density RAM blocks of CMOS-9HD family and EA-9HD family are soft macros. A soft macro consists of a test circuit called BIST, selectors, and some hard macros called basic macro which configure bits and words desired.

In addition, be sure to read the **CMOS-9HD Family Design Manual(A12985E)** , **EA-9HD Family Design Manual (A13282E)** before starting design.

Especially when implementing memory blocks, note that some blocks may be impossible to be mounted because of limit of usable gates.

2. Data Entered in the Block Library



- (1) Block Type : Name of function block
- (2) Function : Function of that block
- (3) SSI Family : 74 (LS) series name which has the same function
- (4) Logic Diagram : Symbol of that block
- (5) Truth Table : Truth table of that block
- (6) Input : Name of input pin, fan-in
- (7) Output : Name of output pin, fan-out
- (8) Switching Speed : Switching characteristics
- (9) Equivalent Cells : No. of cells used

Furthermore, the t_{PD} symbols are as follows

$$\begin{array}{c} A \rightarrow Y \text{ (HL)} \\ \uparrow \quad \uparrow\uparrow \\ \text{(10) (11)(12)} \end{array}$$

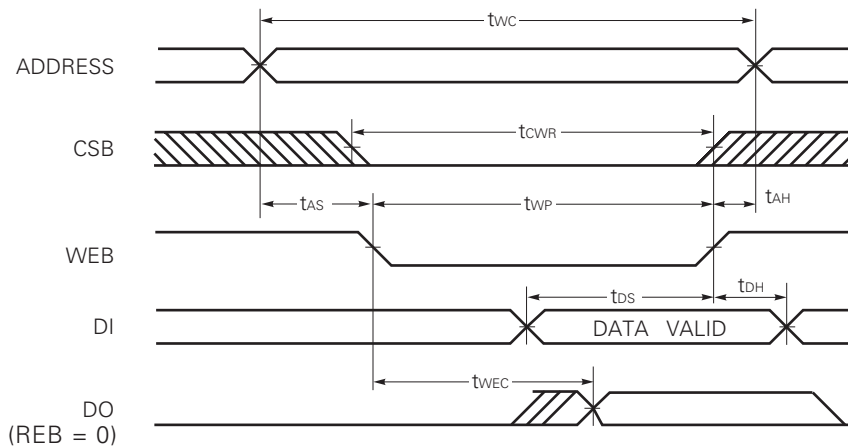
- (10) Signal path (input to output)
- (11) Input signal change (H: rise L: fall Z: High impedance)
- (12) Output signal change (H: rise L: fall Z: High impedance)

3. Memory

The shaded portions changes to high impedance momentarily in the internal circuit when an address or CSB changes, causing output to become undefined.

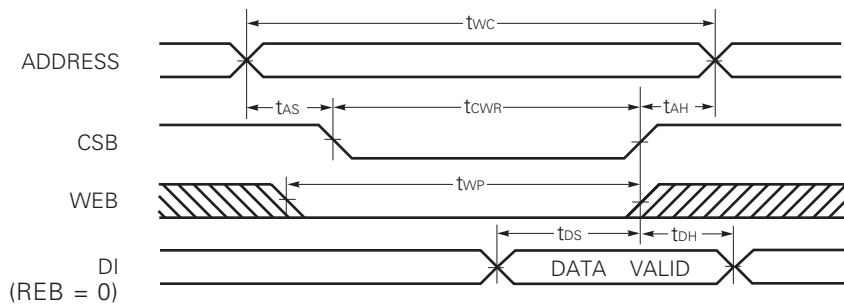
3.1 High Density RAM (Single-port)

(1) Write cycle timing 1 (WEB control mode)



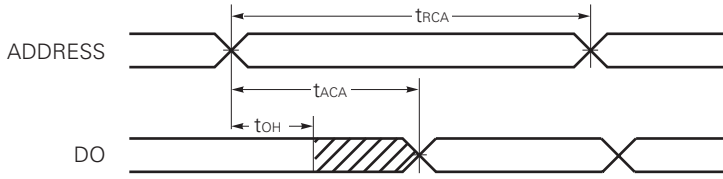
Caution WEB or CSB must be in high level during the address signal is changing. The period during which DATA VALID is output to DO is determined by either the length of time t_{WEC} that elapses from the falling edge of WEB or the time from when DI changes until DO changes, whichever is longer.

(2) Write cycle timing 2 (CSB control mode)



Caution WEB or CSB must be in high level during the address signal is changing.

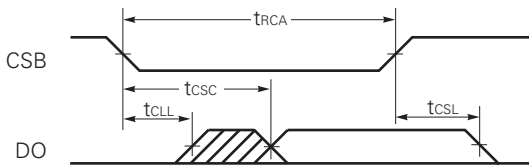
(3) Read cycle timing 1 (CSB=0, WEB=1, REB=0)



t_{ACA} : Time until output is secured after address is determined.

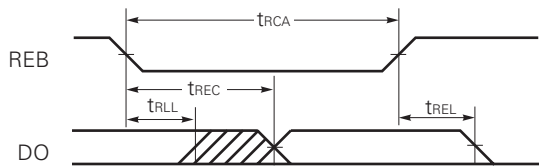
t_{OH} : Time during which data is held before being changed when an address changes.

(4) Read cycle timing 2 (REB=0, WEB=1)



Caution The address signal must remain unchanged at the same time or before the transmission of the low level.

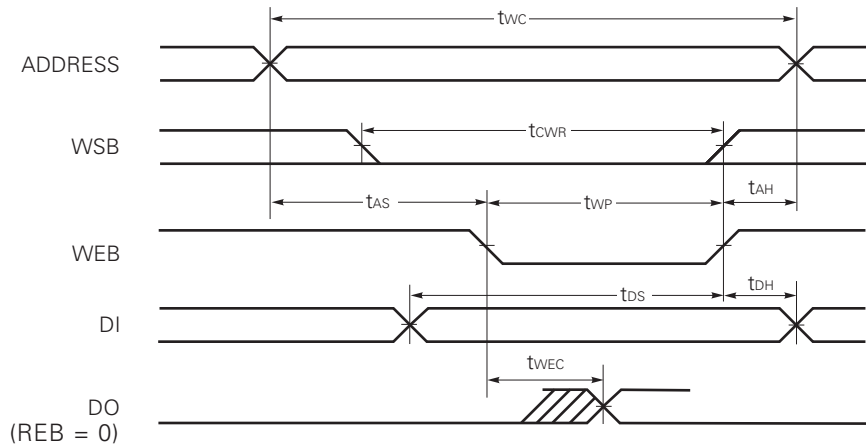
(5) Read cycle timing 3 (CSB=0, WEB=1)



Caution The address signal must remain unchanged at the same time or before the transmission of the low level.

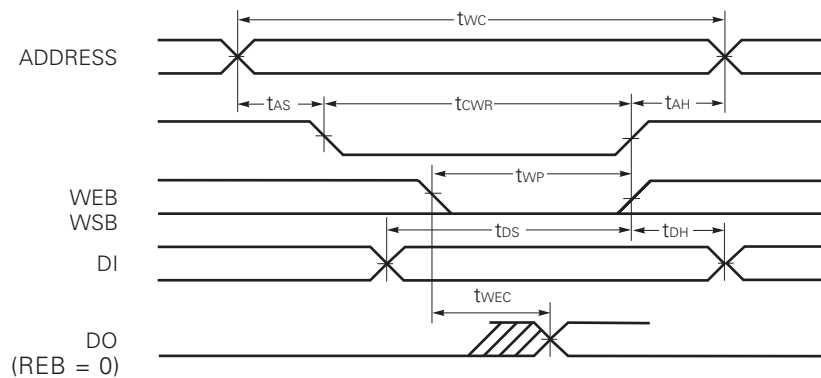
3.2 High Density RAM (Dual-port)

(1) Write cycle timing 1 (WEB control mode)



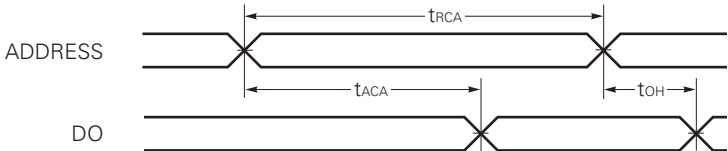
Caution WEB or WSB must be in high level during the address signal is changing. When the READ address and WRITE address are the same, the period during which DI is output to DO is determined by either the length of time t_{WEC} that elapses from the falling edge of WEB or the time from when DI changes until DO changes, whichever is longer.

(2) Write cycle timing 2 (WSB control mode)

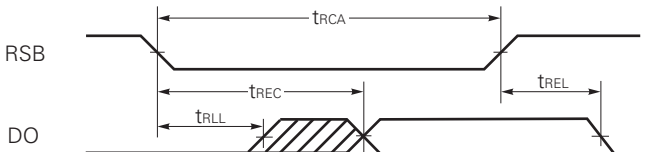


Caution WEB or WSB must be in high level during the address signal is changing. When the READ address and WRITE address are the same, the period during which DI is output to DO is determined by either the length of time t_{WEC} that elapses from the falling edge of WEB or the time from when DI changes until DO changes, whichever is longer.

(3) Read cycle timing 1 (RSB=0)



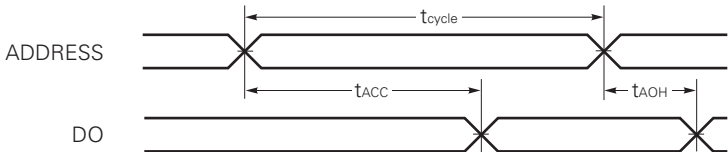
(4) Read cycle timing 2



Caution The address signal must remain unchanged at the same time or before the transmission of the low level.

3.3 ROM

Read cycle timing



4 . BIST (Built In Self Test)

The BIST is the name of the circuit incorporated into each RAM soft macro for testing RAM operation. The BIST consists of test address generator, test data generator, test enable generator, expectation value generator and comparator. Only connecting test pins(TEB, TIN, TOUT) to external pin for testing RAM operation. When mounting plural number of RAM, RAM operation can be tested smoothly. Refer to NEC for details such as circuit configuration of each BIST.

Related Document

The related documents in this publication may include preliminary versions. However, they are not marked as such.

- CMOS-9HD Family and EA-9HD Family
 - CMOS-9HD Family, EA-9HD Family Block Library : A13052E
 - CMOS-9HD Family, EA-9HD Family Memory Block Library : This Manual
 - Design For Test User's Manual : A14357E
- CMOS-9HD Family
 - CMOS-9HD Family Design Manual : A12985E
 - CMOS-9HD Family Mega Macro Design Manual : A13941E
- EA-9HD Family
 - EA-9HD Family Design Manual : A13282E
 - EA-9HD Family Memory Macro Design Manual : A13367E

Before starting design work, contact your local NEC sales representative for the latest information

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CHAPTER 1 HIGH DENSITY SINGLE-PORT RAM BLOCK (Soft Macro)

Page

1

Block Type	Function	Basic RAM	Test Block	Equivalent Cells	Page
<hr/>					
SINGLE-PORT HIGH DENSITY RAM					
RB47	16 words × 4 bits Single-port RAM	K147	RU47	655	2
RB49	32 words × 4 bits Single-port RAM	K149	RU49	884	4
RB4B	64 words × 4 bits Single-port RAM	K149	RU4B	1567	6
RB4D	128 words × 4 bits Single-port RAM	K14D	RU4D	3753	8
RB4F	256 words × 4 bits Single-port RAM	K14D	RU4F	3745	10
RB4H	512 words × 4 bits Single-port RAM	K14D	RU4H	7194	12
RB4M	1 K words × 4 bits Single-port RAM	K14D	RU4M	14155	14
RB4S	2 K words × 4 bits Single-port RAM	K14D	RU4S	28077	16
RB4U	4 K words × 4 bits Single-port RAM	K14D	RU4U	55775	18
RB87	16 words × 8 bits Single-port RAM	K147	RU87	1119	20
RB89	32 words × 8 bits Single-port RAM	K149	RU89	1572	22
RB8B	64 words × 8 bits Single-port RAM	K18B	RU8B	2267	24
RB8D	128 words × 8 bits Single-port RAM	K14D	RU8D	3753	26
RB8F	256 words × 8 bits Single-port RAM	K18F	RU8F	6246	28
RB8H	512 words × 8 bits Single-port RAM	K18F	RU8H	12206	30
RB8M	1 K words × 8 bits Single-port RAM	K18M	RU8M	22140	32
RB8S	2 K words × 8 bits Single-port RAM	K18M	RU8S	43983	34
RBAB	64 words × 10 bits Single-port RAM	K1AB	RUAB	2750	36
RBAD	128 words × 10 bits Single-port RAM	K1AB	RUAD	6863	38
RBAF	256 words × 10 bits Single-port RAM	K1AF	RUAF	7673	40
RBAH	512 words × 10 bits Single-port RAM	K1AF	RUAH	15042	42
RBAM	1 K words × 10 bits Single-port RAM	K1AM	RUAM	27400	44
RBAS	2 K words × 10 bits Single-port RAM	K1AM	RUAS	54491	46
RBC7	16 words × 16 bits Single-port RAM	K147	RUC7	2057	48
RBC9	32 words × 16 bits Single-port RAM	K149	RUC9	2946	50
RBCB	64 words × 16 bits Single-port RAM	K18B	RUCB	4312	52
RBCD	128 words × 16 bits Single-port RAM	K14D	RUCD	7269	54
RBCF	256 words × 16 bits Single-port RAM	K18F	RUCF	12242	56
RBCH	512 words × 16 bits Single-port RAM	K18F	RUCH	24114	58
RBCM	1 K words × 16 bits Single-port RAM	K18M	RUCM	44017	60

SINGLE-PORT HIGH DENSITY RAM

Block Type	Function	Basic RAM	Test Block	Equivalent Cells	Page
RBEB	64 words × 20 bits Single-port RAM	K1AB	RUEB	5286	62
RBED	128 words × 20 bits Single-port RAM	K1AB	RUED	10220	64
RBEF	256 words × 20 bits Single-port RAM	K1AF	RUEF	15104	66
RBEH	512 words × 20 bits Single-port RAM	K1AF	RUEH	29778	68
RBEM	1 K words × 20 bits Single-port RAM	K1AM	RUEM	54541	70
RBH7	16 words × 32 bits Single-port RAM	K147	RUH7	3933	72
RBH9	32 words × 32 bits Single-port RAM	K149	RUH9	5694	74
RBHB	64 words × 32 bits Single-port RAM	K18B	RUHB	8411	76
RBHD	128 words × 32 bits Single-port RAM	K14D	RUHD	14311	78
RBHF	256 words × 32 bits Single-port RAM	K18F	RUHF	24189	80
RBHH	512 words × 32 bits Single-port RAM	K18F	RUHH	47955	82
RBKB	64 words × 40 bits Single-port RAM	K1AB	RUKB	10349	84
RBKD	128 words × 40 bits Single-port RAM	K1AB	RUKD	20195	86
RBKF	256 words × 40 bits Single-port RAM	K1AF	RUKF	29884	88
RBKH	512 words × 40 bits Single-port RAM	K1AF	RUKH	49856	90

DUAL-PORT HIGH DENSITY RAM					
Block Type	Function	Basic RAM	Test Block	Equivalent Cells	Page
R947	16 words × 4 bits Dual-port RAM	K247	RU47	883	94
R949	32 words × 4 bits Dual-port RAM	K249	RU49	1427	96
R94B	64 words × 4 bits Dual-port RAM	K249	RU4B	2636	98
R94D	128 words × 4 bits Dual-port RAM	K24D	RU4D	4052	100
R94F	256 words × 4 bits Dual-port RAM	K24D	RU4F	7837	102
R94H	512 words × 4 bits Dual-port RAM	K24D	RU4H	15343	104
R94M	1 K words × 4 bits Dual-port RAM	K24D	RU4M	30396	106
R94S	2 K words × 4 bits Dual-port RAM	K24D	RU4S	60537	108
R94U	4 K words × 4 bits Dual-port RAM	K24D	RU4U	120704	110
R987	16 words × 8 bits Dual-port RAM	K247	RU87	1554	112
R989	32 words × 8 bits Dual-port RAM	K249	RU89	2632	114
R98B	64 words × 8 bits Dual-port RAM	K28B	RU8B	3446	116
R98D	128 words × 8 bits Dual-port RAM	K24D	RU8D	6613	118
R98F	256 words × 8 bits Dual-port RAM	K28F	RU8F	10369	120
R98H	512 words × 8 bits Dual-port RAM	K28F	RU8H	20418	122
R98M	1 K words × 8 bits Dual-port RAM	K28M	RU8M	37239	124
R98S	2 K words × 8 bits Dual-port RAM	K28M	RU8S	74136	126
R9AB	64 words × 10 bits Dual-port RAM	K2AB	RUAB	4187	128
R9AD	128 words × 10 bits Dual-port RAM	K2AB	RUAD	8079	130
R9AF	256 words × 10 bits Dual-port RAM	K2AF	RUAF	12791	132
R9AH	512 words × 10 bits Dual-port RAM	K2AF	RUAH	25244	134
R9AM	1 K words × 10 bits Dual-port RAM	K2AM	RUAM	46281	136
R9AS	2 K words × 10 bits Dual-port RAM	K2AM	RUAS	92206	138
R9C7	16 words × 16 bits Dual-port RAM	K247	RUC7	2902	140
R9C9	32 words × 16 bits Dual-port RAM	K249	RUC9	5036	142
R9CB	64 words × 16 bits Dual-port RAM	K28B	RUCB	6635	144
R9CD	128 words × 16 bits Dual-port RAM	K24D	RUCD	12939	146
R9CF	256 words × 16 bits Dual-port RAM	K28F	RUCF	20439	148
R9CH	512 words × 16 bits Dual-port RAM	K28F	RUCH	40489	150
R9CM	1 K words × 16 bits Dual-port RAM	K28M	RUCM	74160	152
R9EB	64 words × 20 bits Dual-port RAM	K2AB	RUEB	8125	154
R9ED	128 words × 20 bits Dual-port RAM	K2AB	RUED	15878	156
R9EF	256 words × 20 bits Dual-port RAM	K2AF	RUEF	25290	158
R9EH	512 words × 20 bits Dual-port RAM	K2AF	RUEH	50129	160
R9EM	1 K words × 20 bits Dual-port RAM	K2AM	RUEM	92244	162
R9H7	16 words × 32 bits Dual-port RAM	K247	RUH7	5606	164
R9H9	32 words × 32 bits Dual-port RAM	K249	RUH9	9852	166
R9HB	64 words × 32 bits Dual-port RAM	K28B	RUHB	13026	168
R9HD	128 words × 32 bits Dual-port RAM	K24D	RUHD	25605	170
R9HF	256 words × 32 bits Dual-port RAM	K28F	RUHF	40559	172
R9HH	512 words × 32 bits Dual-port RAM	K28F	RUHH	80657	174
R9KB	64 words × 40 bits Dual-port RAM	K2AB	RUHB	15994	176
R9KD	128 words × 40 bits Dual-port RAM	K2AB	RUKD	31469	178
R9KF	256 words × 40 bits Dual-port RAM	K2AF	RUKF	50227	180
R9KH	512 words × 40 bits Dual-port RAM	K2AF	RUKH	99937	182

Block Type	Function	Equivalent Cells	Page
J14DK	128 words × 4 bits ROM	1113	186
J14FK	256 words × 4 bits ROM	2035	187
J14HK	512 words × 4 bits ROM	3458	188
J14MK	1024 words × 4 bits ROM	6370	189
J14SK	2048 words × 4 bits ROM	12194	190
J18DK	128 words × 8 bits ROM	1785	191
J18FK	256 words × 8 bits ROM	3219	192
J18HK	512 words × 8 bits ROM	5890	193
J18MK	1024 words × 8 bits ROM	10850	194
J18SK	2048 words × 8 bits ROM	20770	195
J1CDK	128 words × 16 bits ROM	3129	196
J1CFK	256 words × 16 bits ROM	5587	197
J1CHK	512 words × 16 bits ROM	10754	198
J1CMK	1024 words × 16 bits ROM	19810	199
J1CSK	2048 words × 16 bits ROM	37922	200
J1HFK	256 words × 32 bits ROM	10323	201
J1HHK	512 words × 32 bits ROM	20482	202
J1HMK	1024 words × 32 bits ROM	37730	203
J1HSK	2048 words × 32 bits ROM	73968	204

SINGLE-PORT BASIC RAM

Block Type	Function	Equivalent Cells	Page
K147	16 words × 4 bits Single-port RAM	432	206
K149	32 words × 4 bits Single-port RAM	650	208
K14D	128 words × 4 bits Single-port RAM	1722	210
K18B	64 words × 8 bits Single-port RAM	1974	212
K18F	256 words × 8 bits Single-port RAM	5920	214
K18M	1024 words × 8 bits Single-port RAM	21804	216
K1AB	64 words × 10 bits Single-port RAM	2436	218
K1AF	256 words × 10 bits Single-port RAM	7326	220
K1AM	1024 words × 10 bits Single-port RAM	27048	222

DUAL-PORT BASIC RAM

Block Type	Function	Equivalent Cells	Page
K247	16 words × 4 bits Dual-port RAM	638	224
K249	32 words × 4 bits Dual-port RAM	1166	226
K24D	128 words × 4 bits Dual-port RAM	3744	228
K28B	64 words × 8 bits Dual-port RAM	3120	230
K28F	256 words × 8 bits Dual-port RAM	10000	232
K28M	1024 words × 8 bits Dual-port RAM	36848	234
K2AB	64 words × 10 bits Dual-port RAM	3840	236
K2AF	256 words × 10 bits Dual-port RAM	12400	238
K2AM	1024 words × 10 bits Dual-port RAM	45872	240

[MEMO]

CHAPTER 1

HIGH DENSITY

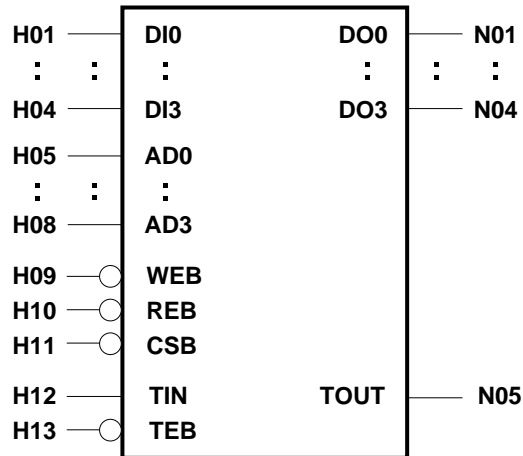
SINGLE-PORT RAM BLOCK

(Soft Macro)

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB47	16 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
 DIn : Input data
 ADn : Address data
 CSB : Chip select
 WEB : Write enable
 REB : Read enable
 DOn : Output data
 TEB : Test enable
 TIN : Test clock
 TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD3	(LH)	2.25	3.73	6.13
:	:	:	:	:	:	→DO0 to DO3	(HH)	2.25	3.72	6.11
H04	DI3	2.4	N04	DO3	23.7		(HL)	1.98	3.62	6.28
H05	AD0	2.4	N05	TOUT	26.0		(LL)	1.98	3.62	6.30
:	:	:				CSB	(LL)	1.99	3.44	5.80
H09	WEB	2.4				→DO0 to DO3	(LH)	1.99	3.44	5.80
H10	REB	1.0					(HL)	0.69	1.09	1.75
H11	CSB	1.0				REB	(LH)	0.73	1.25	2.09
H12	TIN	2.4				→DO0 to DO3	(HL)	0.78	1.22	1.94
H13	TEB	5.0				DI0 to DI3	(HH)	1.85	3.20	5.40
						→DO0 to DO3	(LL)	1.71	2.70	4.30
Equivalent Cells		655		Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

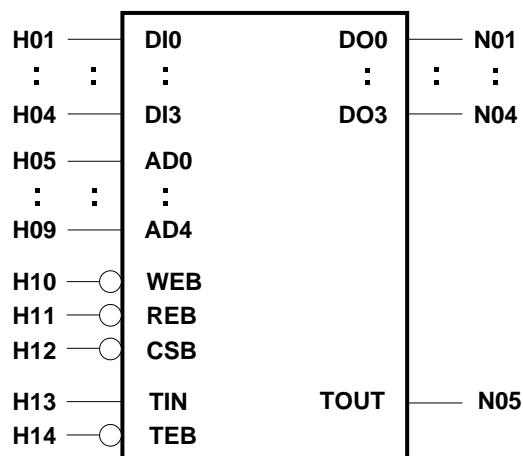
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.30		
Address access time	tACA			6.30
Address output hold time	tOH	1.98		
CSB access time	tCSC			5.80
CSB output hold time	tCSL	0.93		2.60
CSB output set time	tCLL	1.99		
REB access time	tREC			2.10
REB output hold time	tREL	0.78		1.94
REB output set time	tRLL	0.74		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.37		
CSB-WEB reset time	tCWR	4.03		
Write pulse width	tWP	4.03		
Address setup time	tAS	1.01		
Address hold time	tAH	0.33		
Input data setup time	tDS	3.34		
Input data hold time	tDH	0.42		
WEB access time	tWEC			5.45

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB49	32 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed									
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)							
						IN	→ OUT	MIN.	TYP.	MAX.					
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD4 (LH) →DO0 to DO3 (HH)	(LH)	2.59	4.26	6.99					
:	:	:	:	:	:			(HL)	2.32	4.15	7.14				
H04	DI3	2.4	N04	DO3	23.7							(LL)	2.32	4.16	7.16
H05	AD0	2.4	N05	TOUT	26.0										
:	:	:				CSB	(LL)	2.24	3.92	6.66					
H10	WEB	2.4									(LH)	2.24	3.92	6.66	
H11	REB	1.0													(HL)
H12	CSB	1.0				REB	(LH)	0.74	1.26	2.10					
H13	TIN	2.4									(HL)	0.79	1.23	1.95	
H14	TEB	5.0				DI0 to DI3	(HH)	1.86	3.24	5.51					
											(LL)	1.72	2.74	4.41	
Equivalent Cells		884		Power (mW/MHz)		Rev.		1							

HIGH DENSITY SINGLE-PORT RAM BLOCK

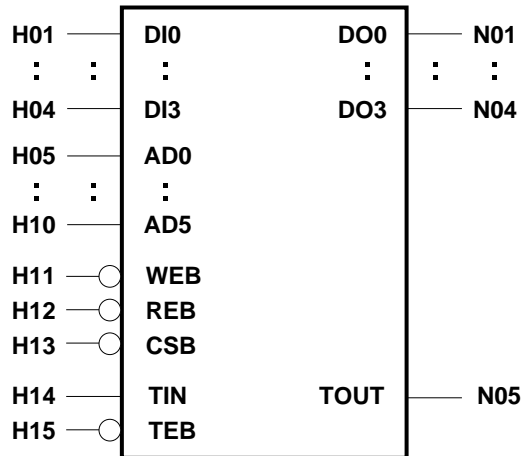
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.16		
Address access time	tACA			7.16
Address output hold time	tOH	2.32		
CSB access time	tCSC			6.66
CSB output hold time	tCSL	0.94		2.61
CSB output set time	tCLL	2.24		
REB access time	tREC			2.11
REB output hold time	tREL	0.79		1.95
REB output set time	tRLL	0.75		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.89		
CSB-WEB reset time	tCWR	4.53		
Write pulse width	tWP	4.53		
Address setup time	tAS	1.02		
Address hold time	tAH	0.34		
Input data setup time	tDS	3.35		
Input data hold time	tDH	0.43		
WEB access time	tWEC			5.55

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4B	64 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
 DIn : Input data
 ADn : Address data
 CSB : Chip select
 WEB : Write enable
 REB : Read enable
 DOn : Output data
 TEB : Test enable
 TIN : Test clock
 TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	24.7	AD0 to AD5 (LH)			2.81	4.80	8.04	
:	:	:	:	:	:	→DO0 to DO3 (HH)			2.72	4.66	7.82	
H04	DI3	2.4	N04	DO3	24.7	(HL)			1.52	3.98	7.99	
H05	AD0	2.4	N05	TOUT	26.0	(LL)			1.41	3.93	8.05	
:	:	:							CSB (LL)	2.55	4.41	7.43
H10	AD5	2.4							→DO0 to DO3 (LH)	2.55	4.41	7.43
H11	WEB	2.4							(HL)	1.30	2.17	3.57
H12	REB	1.0							REB (LH)	0.97	1.61	2.65
H13	CSB	2.4							→DO0 to DO3 (HL)	1.12	1.76	2.81
H14	TIN	2.4							DI0 to DI3 (HH)	2.08	3.58	6.03
H15	TEB	5.0							→DO0 to DO3 (LL)	2.07	3.28	5.26
Equivalent Cells		1567		Power (mW/MHz)		Rev.		1				

HIGH DENSITY SINGLE-PORT RAM BLOCK

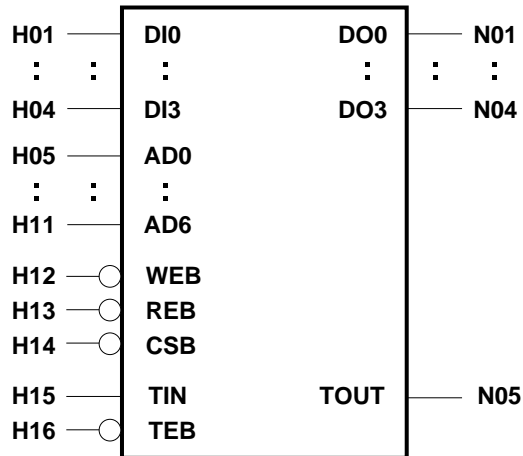
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.06		
Address access time	tACA			8.06
Address output hold time	tOH	1.41		
CSB access time	tCSC			7.43
CSB output hold time	tCSL	1.30		3.57
CSB output set time	tCLL	2.56		
REB access time	tREC			2.65
REB output hold time	tREL	1.12		2.81
REB output set time	tRLL	0.97		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.34		
CSB-WEB reset time	tCWR	4.72		
Write pulse width	tWP	4.72		
Address setup time	tAS	1.18		
Address hold time	tAH	0.44		
Input data setup time	tDS	3.39		
Input data hold time	tDH	0.53		
WEB access time	tWEC			6.09

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4D	128 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed							
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)					
						IN	→	OUT	MIN.	TYP.	MAX.		
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6		(LH)	2.00	4.48	8.53		
:	:	:	:	:	:	→DO0 to DO3		(HH)	2.00	4.47	8.51		
H04	DI3	2.4	N04	DO3	23.7			(HL)	1.81	4.30	8.35		
H05	AD0	2.4	N05	TOUT	26.0			(LL)	1.81	4.31	8.38		
:	:	:											
H11	AD6	2.4							CSB	(LL)	1.02	3.51	7.55
H12	WEB	2.4							→DO0 to DO3	(LH)	1.02	3.51	7.55
H13	REB	1.0								(HL)	0.92	1.59	2.68
H14	CSB	1.0							REB	(LH)	0.81	1.43	2.45
H15	TIN	2.4							→DO0 to DO3	(HL)	0.69	1.20	2.04
H16	TEB	5.0							DI0 to DI3	(HH)	1.85	3.46	6.09
								→DO0 to DO3	(LL)	1.64	2.99	5.20	
Equivalent Cells			3753			Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

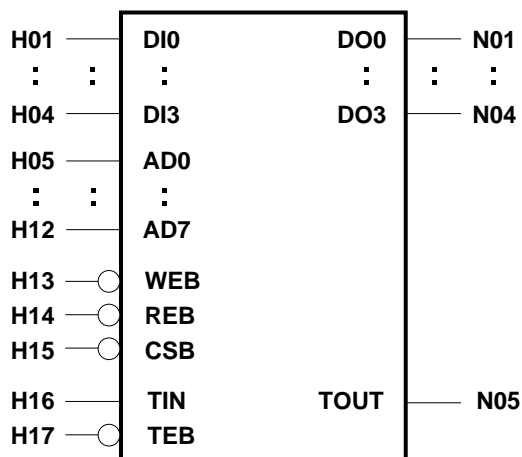
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.95		
Address access time	tACA			9.95
Address output hold time	tOH	2.09		
CSB access time	tCSC			7.56
CSB output hold time	tCSL	1.08		2.69
CSB output set time	tCLL	3.08		
REB access time	tREC			2.45
REB output hold time	tREL	0.80		2.04
REB output set time	tRLL	0.93		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.76		
CSB-WEB reset time	tCWR	3.70		
Write pulse width	tWP	3.70		
Address setup time	tAS	1.77		
Address hold time	tAH	1.29		
Input data setup time	tDS	3.46		
Input data hold time	tDH	0.77		
WEB access time	tWEC			5.83

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4F	256 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7	AD0 to AD7 →DO0 to DO3	(LH)	1.60	4.51	9.24
:	:	:	:	:	:		(HH)	1.50	4.35	9.00
H04	DI3	2.4	N04	DO3	24.7		(HL)	1.49	4.43	9.22
H05	AD0	2.4	N05	TOUT	26.0		(LL)	1.43	4.41	9.28
:	:	:				CSB →DO0 to DO3	(LL)	1.34	4.05	8.45
H12	AD7	2.4					(LH)	1.34	4.05	8.45
H13	WEB	2.4					(HL)	1.29	2.25	3.83
H14	REB	1.0				REB →DO0 to DO3	(LH)	1.02	1.75	2.94
H15	CSB	2.4					(HL)	0.97	1.71	2.92
H16	TIN	2.4				DI0 to DI3 →DO0 to DO3	(HH)	2.04	3.76	6.56
H17	TEB	5.0					(LL)	1.92	3.49	6.05
Equivalent Cells		3745		Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

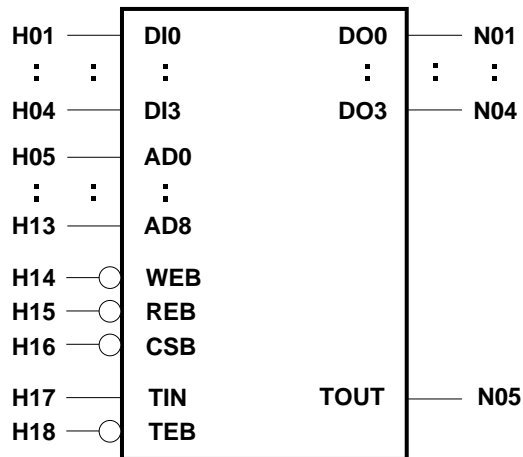
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.28		
Address access time	tACA			9.28
Address output hold time	tOH	1.65		
CSB access time	tCSC			8.46
CSB output hold time	tCSL	1.49		3.84
CSB output set time	tCLL	4.03		
REB access time	tREC			2.95
REB output hold time	tREL	1.13		2.92
REB output set time	tRLL	1.18		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.79		
CSB-WEB reset time	tCWR	3.73		
Write pulse width	tWP	3.73		
Address setup time	tAS	1.68		
Address hold time	tAH	1.38		
Input data setup time	tDS	3.37		
Input data hold time	tDH	0.86		
WEB access time	tWEC			6.49

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4H	512 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD8 →DO0 to DO3	(LH)	1.81	4.90	9.94
:	:	:	:	:	:		(HH)	1.68	4.86	10.05
H04	DI3	2.4	N04	DO3	23.7		(HL)	1.78	5.02	10.30
H05	AD0	2.4	N05	TOUT	26.0		(LL)	1.77	5.04	10.37
:	:	:				CSB →DO0 to DO3	(LL)	1.75	4.73	9.60
H13	AD8	2.4					(LH)	1.75	4.73	9.60
H14	WEB	2.4					(HL)	1.81	3.28	5.68
H15	REB	1.0				REB →DO0 to DO3	(LH)	1.03	1.80	3.06
H16	CSB	1.0					(HL)	1.29	2.31	3.99
H17	TIN	2.4				DI0 to DI3 →DO0 to DO3	(HH)	2.07	3.83	6.69
H18	TEB	5.0					(LL)	2.15	3.91	6.77
Equivalent Cells		7194		Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

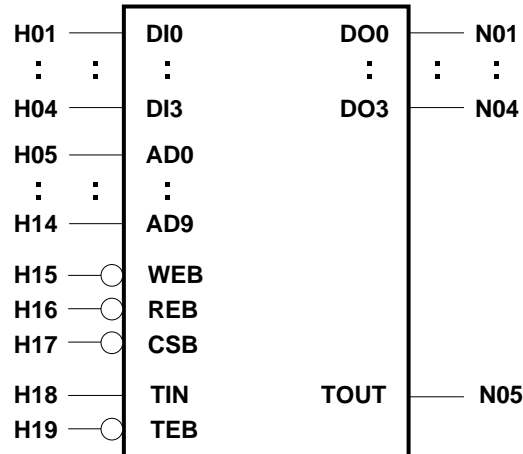
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.38		
Address access time	tACA			10.38
Address output hold time	tOH	1.94		
CSB access time	tCSC			9.61
CSB output hold time	tCSL	2.65		5.68
CSB output set time	tCLL	5.24		
REB access time	tREC			3.07
REB output hold time	tREL	1.49		3.99
REB output set time	tRLL	1.20		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.73		
CSB-WEB reset time	tCWR	4.15		
Write pulse width	tWP	4.15		
Address setup time	tAS	1.69		
Address hold time	tAH	0.89		
Input data setup time	tDS	3.42		
Input data hold time	tDH	1.53		
WEB access time	tWEC			7.48

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4M	1K words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	21.7	AD0 to AD9 →DO0 to DO3	(LH)	2.23	5.65	11.22
:	:	:	:	:	:		(HH)	2.07	5.58	11.32
H04	DI3	2.4	N04	DO3	21.7		(HL)	2.01	5.14	10.24
H05	AD0	2.4	N05	TOUT	26.0		(LL)	1.93	5.14	10.38
:	:	:				CSB →DO0 to DO3	(LL)	2.15	5.45	10.83
H14	AD9	2.4					(LH)	2.15	5.45	10.83
H15	WEB	2.4					(HL)	1.96	3.39	5.74
H16	REB	1.0				REB →DO0 to DO3	(LH)	1.28	2.20	3.71
H17	CSB	1.0					(HL)	1.30	2.30	3.92
H18	TIN	2.4				DI0 to DI3 →DO0 to DO3	(HH)	2.32	4.24	7.37
H19	TEB	5.0					(LL)	2.29	4.16	7.20
Equivalent Cells		14155		Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

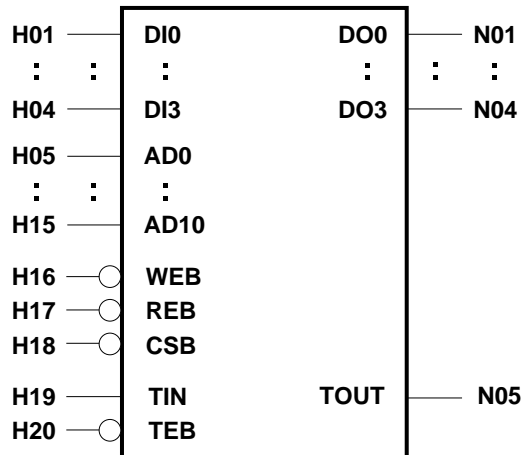
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	11.33		
Address access time	tACA			11.33
Address output hold time	tOH	2.23		
CSB access time	tCSC			10.84
CSB output hold time	tCSL	2.26		5.74
CSB output set time	tCLL	6.46		
REB access time	tREC			3.72
REB output hold time	tREL	1.50		3.93
REB output set time	tRLL	0.89		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.24		
CSB-WEB reset time	tCWR	4.58		
Write pulse width	tWP	4.58		
Address setup time	tAS	1.71		
Address hold time	tAH	0.95		
Input data setup time	tDS	3.52		
Input data hold time	tDH	1.67		
WEB access time	tWEC			8.47

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4S	2K words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
 DIn : Input data
 ADn : Address data
 CSB : Chip select
 WEB : Write enable
 REB : Read enable
 DOn : Output data
 TEB : Test enable
 TIN : Test clock
 TOUT: Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	17.7	AD0 to AD10	→DO0 to DO3	(LH)	2.26	5.99	12.07	
:	:	:	:	:	:			(HH)	2.05	5.74	11.75	
H04	DI3	2.4	N04	DO3	17.7			(HL)	2.12	5.37	10.68	
H05	AD0	2.4	N05	TOUT	26.0	CSB	→DO0 to DO3	(LL)	2.04	5.35	10.74	
:	:	:										
H15	AD10	2.4										
H16	WEB	2.4										
H17	REB	1.0										
H18	CSB	2.4										
H19	TIN	2.4										
H20	TEB	5.0										
						REB	→DO0 to DO3	(LH)	1.29	2.22	3.75	
								(HL)	1.41	2.55	4.42	
						DI0 to DI3	→DO0 to DO3	(HH)	2.32	4.24	7.37	
								(LL)	2.38	4.36	7.60	
Equivalent Cells		28077		Power (mW/MHz)		Rev.		1				

HIGH DENSITY SINGLE-PORT RAM BLOCK

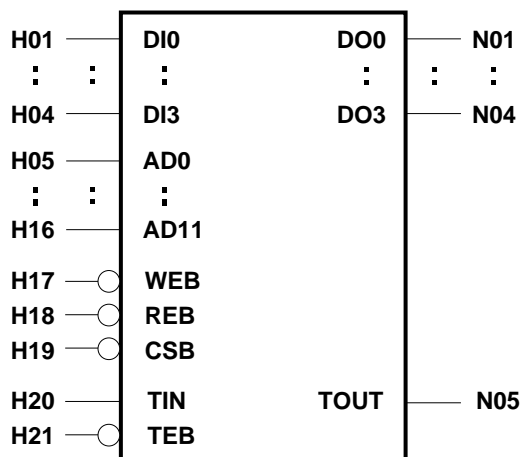
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.07		
Address access time	tACA			12.07
Address output hold time	tOH	2.36		
CSB access time	tCSC			11.26
CSB output hold time	tCSL	2.47		6.52
CSB output set time	tCLL	5.77		
REB access time	tREC			3.77
REB output hold time	tREL	1.63		4.43
REB output set time	tRLL	1.49		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.54		
CSB-WEB reset time	tCWR	4.76		
Write pulse width	tWP	4.76		
Address setup time	tAS	1.70		
Address hold time	tAH	1.08		
Input data setup time	tDS	3.44		
Input data hold time	tDH	1.95		
WEB access time	tWEC			8.86

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB4U	4K words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)	
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	17.7	AD0 to AD11 (LH)	2.28	6.30	12.85
:	:	:	:	:	:	→DO0 to DO3 (HH)	2.11	6.21	12.91
H04	DI3	2.4	N04	DO3	17.7	(HL)	2.25	5.87	11.78
H05	AD0	2.4	N05	TOUT	26.0	(LL)	2.23	5.84	11.73
:	:	:							
H16	AD11	2.4							
H17	WEB	2.4							
H18	REB	2.4							
H19	CSB	1.0							
H20	TIN	2.4							
H21	TEB	5.0							
						REB (LH)	1.39	2.38	3.99
						→DO0 to DO3 (HL)	1.66	3.03	5.26
						DI0 to DI3 (HH)	2.57	4.65	8.04
						→DO0 to DO3 (LL)	2.72	4.95	8.59
Equivalent Cells		55775		Power (mW/MHz)		Rev.		1	

HIGH DENSITY SINGLE-PORT RAM BLOCK

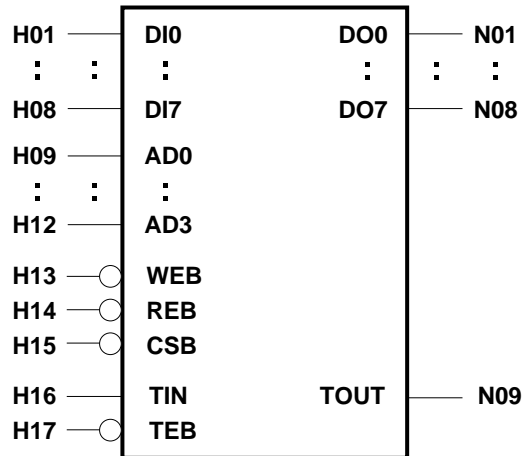
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.91		
Address access time	tACA			12.91
Address output hold time	tOH	2.44		
CSB access time	tCSC			12.51
CSB output hold time	tCSL	3.04		7.95
CSB output set time	tCLL	6.90		
REB access time	tREC			3.99
REB output hold time	tREL	1.92		5.28
REB output set time	tRLL	1.60		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.28		
CSB-WEB reset time	tCWR	5.20		
Write pulse width	tWP	5.20		
Address setup time	tAS	1.78		
Address hold time	tAH	1.30		
Input data setup time	tDS	3.55		
Input data hold time	tDH	2.46		
WEB access time	tWEC			9.80

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB87	16 words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H08	DI7	2.4	N08	DO7	23.7	AD0 to AD3		(LH)	2.31	3.81	6.26
H09	AD0	2.4	N09	TOUT	26.0	→DO0 to DO7		(HH)	2.29	3.78	6.21
:	:	:						(HL)	2.02	3.68	6.38
H12	AD3	2.4						(LL)	2.03	3.70	6.43
H13	WEB	2.4				CSB		(LL)	2.02	3.49	5.89
H14	REB	1.0				→DO0 to DO7		(LH)	2.02	3.49	5.89
H15	CSB	1.0						(HL)	0.74	1.17	1.86
H16	TIN	2.4				REB		(LH)	0.76	1.30	2.17
H17	TEB	5.0				→DO0 to DO7		(HL)	0.83	1.29	2.04
						DI0 to DI7		(HH)	1.85	3.20	5.41
						→DO0 to DO7		(LL)	1.71	2.70	4.31
Equivalent Cells		1119		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

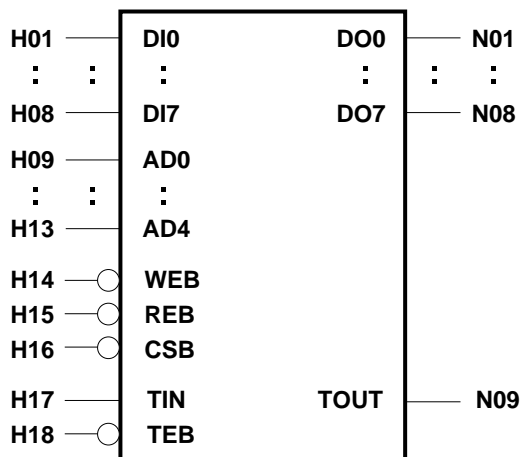
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.44		
Address access time	tACA			6.44
Address output hold time	tOH	2.02		
CSB access time	tCSC			5.89
CSB output hold time	tCSL	0.99		2.71
CSB output set time	tCLL	2.02		
REB access time	tREC			2.14
REB output hold time	tREL	0.84		2.04
REB output set time	tRLL	0.77		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.68		
CSB-WEB reset time	tCWR	4.05		
Write pulse width	tWP	4.05		
Address setup time	tAS	1.27		
Address hold time	tAH	0.36		
Input data setup time	tDS	3.30		
Input data hold time	tDH	0.51		
WEB access time	tWEC			5.57

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB89	32 words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0	→	AD4 (LH)	2.65	4.34	7.12
:	:	:	:	:	:	→	DO0	DO7 (HH)	2.63	4.31	7.06
H08	DI7	2.4	N08	DO7	23.7			(HL)	2.36	4.21	7.23
H09	AD0	2.4	N09	TOUT	26.0			(LL)	2.37	4.24	7.29
:	:	:				CSB		(LL)	2.27	3.97	6.74
H13	AD4	2.4				→	DO0	DO7 (LH)	2.27	3.97	6.74
H14	WEB	2.4						(HL)	0.99	1.65	2.72
H15	REB	1.0				REB		(LH)	0.77	1.31	2.18
H16	CSB	1.0				→	DO0	DO7 (HL)	0.84	1.30	2.05
H17	TIN	2.4				DI0		(HH)	1.86	3.25	5.52
H18	TEB	5.0				→	DO0	DO7 (LL)	1.72	2.75	4.42
Equivalent Cells		1572			Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

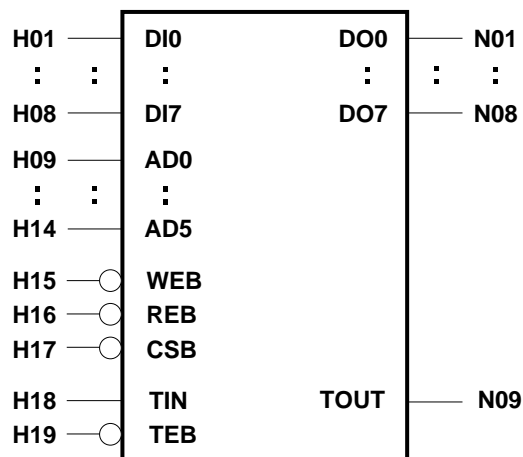
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.30		
Address access time	tACA			7.30
Address output hold time	tOH	2.36		
CSB access time	tCSC			6.74
CSB output hold time	tCSL	1.00		2.72
CSB output set time	tCLL	2.28		
REB access time	tREC			2.15
REB output hold time	tREL	0.85		2.05
REB output set time	tRLL	0.78		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.20		
CSB-WEB reset time	tCWR	4.55		
Write pulse width	tWP	4.55		
Address setup time	tAS	1.28		
Address hold time	tAH	0.37		
Input data setup time	tDS	3.31		
Input data hold time	tDH	0.52		
WEB access time	tWEC			5.68

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8B	64 words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD5	(LH)	→DO0 to DO7	2.86	4.45	7.04
:	:	:	:	:	:				(HH)	2.86	4.44
H08	DI7	2.4	N08	DO7	23.7	CSB	(LL)	→DO0 to DO7	2.46	4.44	7.67
H09	AD0	2.4	N09	TOUT	26.0				(LL)	2.46	4.45
:	:	:				REB	(LH)	→DO0 to DO7	2.34	4.25	7.38
H14	AD5	2.4							(LH)	2.34	4.25
H15	WEB	2.4				DI0 to DI7	(HL)	→DO0 to DO7	1.03	1.71	2.80
H16	REB	1.0							(HL)	1.03	1.71
H17	CSB	1.0				REB	(LH)	→DO0 to DO7	0.76	1.27	2.11
H18	TIN	2.4							(HL)	0.79	1.25
H19	TEB	5.0				DI0 to DI7	(HH)	→DO0 to DO7	1.74	3.17	5.51
									(LL)	1.60	2.92
Equivalent Cells		2267		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

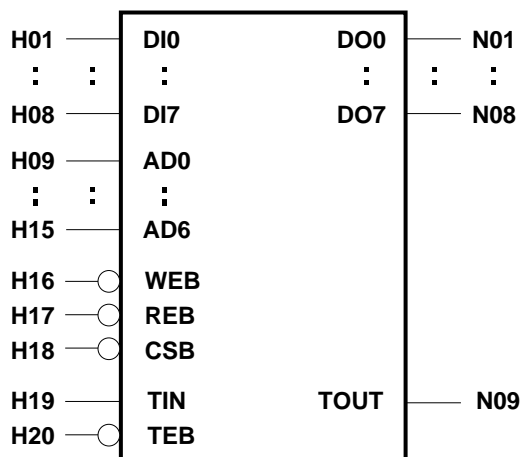
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.85		
Address access time	tACA			6.85
Address output hold time	tOH	2.46		
CSB access time	tCSC			7.39
CSB output hold time	tCSL	1.04		2.80
CSB output set time	tCLL	2.34		
REB access time	tREC			2.12
REB output hold time	tREL	0.79		2.00
REB output set time	tRLL	0.76		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.48		
CSB-WEB reset time	tCWR	3.63		
Write pulse width	tWP	3.63		
Address setup time	tAS	2.62		
Address hold time	tAH	0.23		
Input data setup time	tDS	2.62		
Input data hold time	tDH	1.50		
WEB access time	tWEC			4.78

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8D	128 words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H08	DI7	2.4	N08	DO7	23.7	AD0 to AD6 (LH)		2.02	4.52	8.58	
H09	AD0	2.4	N09	TOUT	26.0	→DO0 to DO7 (HH)		2.01	4.49	8.53	
:	:	:				(HL)		1.82	4.31	8.38	
H15	AD6	2.4				(LL)		1.83	4.34	8.43	
H16	WEB	2.4				CSB (LL)		1.03	3.52	7.59	
H17	REB	1.0				→DO0 to DO7 (LH)		1.03	3.52	7.59	
H18	CSB	1.0				(HL)		0.94	1.61	2.71	
H19	TIN	2.4				REB (LH)		0.82	1.45	2.47	
H20	TEB	5.0				→DO0 to DO7 (HL)		0.70	1.22	2.08	
						DI0 to DI7 (HH)		1.85	3.46	6.09	
						→DO0 to DO7 (LL)		1.64	2.99	5.20	
Equivalent Cells			3753			Power (mW/MHz)		Rev.		1	

HIGH DENSITY SINGLE-PORT RAM BLOCK

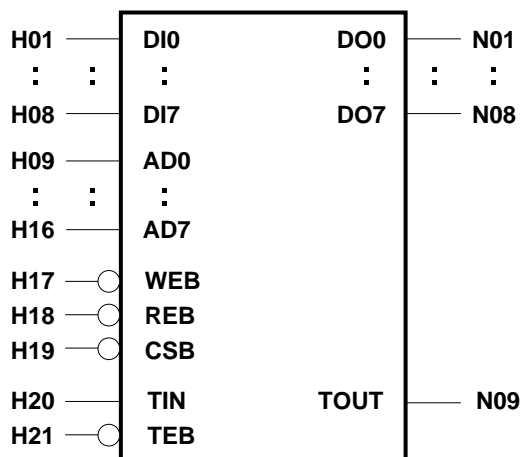
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.02		
Address access time	tACA			10.02
Address output hold time	tOH	2.11		
CSB access time	tCSC			7.60
CSB output hold time	tCSL	1.08		2.71
CSB output set time	tCLL	3.12		
REB access time	tREC			2.48
REB output hold time	tREL	0.71		2.08
REB output set time	tRLL	0.82		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.45		
CSB-WEB reset time	tCWR	3.73		
Write pulse width	tWP	3.73		
Address setup time	tAS	1.78		
Address hold time	tAH	1.29		
Input data setup time	tDS	3.82		
Input data hold time	tDH	0.79		
WEB access time	tWEC			5.87

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8F	256 words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H08	DI7	2.4	N08	DO7	23.7	AD0 to AD7	(LH)		2.33	5.21	9.92
H09	AD0	2.4	N09	TOUT	26.0	→DO0 to DO7	(HH)		2.33	5.20	9.89
:	:	:					(HL)		1.99	4.66	9.01
H16	AD7	2.4					(LL)		1.99	4.67	9.04
H17	WEB	2.4				CSB	(LL)		1.10	3.98	8.67
H18	REB	1.0				→DO0 to DO7	(LH)		1.10	3.98	8.67
H19	CSB	1.0					(HL)		0.98	1.68	2.81
H20	TIN	2.4				REB	(LH)		0.95	1.59	2.64
H21	TEB	5.0				→DO0 to DO7	(HL)		0.72	1.26	2.13
						DI0 to DI7	(HH)		1.99	3.70	6.49
						→DO0 to DO7	(LL)		1.75	3.23	5.65
Equivalent Cells		6246		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.92		
Address access time	tACA			9.92
Address output hold time	tOH	2.29		
CSB access time	tCSC			8.67
CSB output hold time	tCSL	1.13		2.81
CSB output set time	tCLL	3.31		
REB access time	tREC			2.64
REB output hold time	tREL	0.83		2.13
REB output set time	tRLL	1.10		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.43		
CSB-WEB reset time	tCWR	4.15		
Write pulse width	tWP	4.15		
Address setup time	tAS	1.91		
Address hold time	tAH	1.37		
Input data setup time	tDS	3.64		
Input data hold time	tDH	0.95		
WEB access time	tWEC			6.53

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																			
RB8H	512 words × 8 bits Single-port RAM																																																																																																																																																																																																				
<p>Logic Diagram</p> <div style="text-align: center; margin: 20px 0;"> </div>																																																																																																																																																																																																					
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Input			Output			Switching speed																																																																																																																																																																																															
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H21	TIN	2.4							→DO0 to DO7 (HL)	1.01	1.77	3.01																																																																																																																																																																																									
H22	TEB	5.0							DI0 to DI7 (HH)	2.18	4.00	6.97																																																																																																																																																																																									
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Equivalent Cells			12206			Power (mW/MHz)		Rev.		1																																																																																																																																																																																											

HIGH DENSITY SINGLE-PORT RAM BLOCK

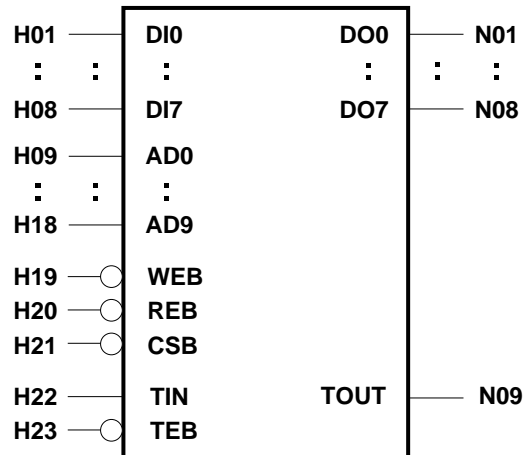
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.44		
Address access time	tACA			10.44
Address output hold time	tOH	1.71		
CSB access time	tCSC			9.57
CSB output hold time	tCSL	1.55		3.97
CSB output set time	tCLL	4.26		
REB access time	tREC			3.15
REB output hold time	tREL	1.16		3.01
REB output set time	tRLL	1.34		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.59		
CSB-WEB reset time	tCWR	4.18		
Write pulse width	tWP	4.18		
Address setup time	tAS	1.82		
Address hold time	tAH	0.59		
Input data setup time	tDS	3.54		
Input data hold time	tDH	0.94		
WEB access time	tWEC			6.99

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8M	1K words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD9	(LH)		2.91	7.02	13.72
:	:	:	:	:	:	→DO0 to DO7	(HH)		2.91	7.01	13.69
H08	DI7	2.4	N08	DO7	23.7		(HL)		2.38	6.40	12.96
H09	AD0	2.4	N09	TOUT	26.0		(LL)		2.38	6.41	12.99
:	:	:				CSB	(LL)		1.19	4.81	10.70
H18	AD9	2.4				→DO0 to DO7	(LH)		1.19	4.81	10.70
H19	WEB	2.4					(HL)		1.06	1.87	3.19
H20	REB	1.0				REB	(LH)		1.01	1.72	2.88
H21	CSB	1.0				→DO0 to DO7	(HL)		0.74	1.35	2.35
H22	TIN	2.4				DI0 to DI7	(HH)		2.94	5.58	9.88
H23	TEB	5.0				→DO0 to DO7	(LL)		2.61	4.86	8.52
Equivalent Cells		22140		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

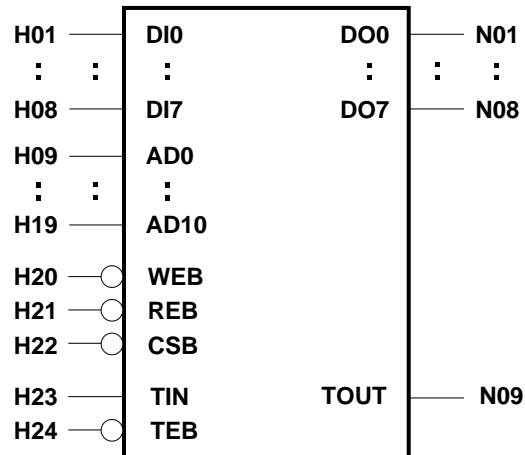
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	13.72		
Address access time	tACA			13.72
Address output hold time	tOH	2.75		
CSB access time	tCSC			10.70
CSB output hold time	tCSL	1.23		3.19
CSB output set time	tCLL	3.58		
REB access time	tREC			2.89
REB output hold time	tREL	0.86		2.35
REB output set time	tRLL	1.16		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.71		
CSB-WEB reset time	tCWR	5.22		
Write pulse width	tWP	5.22		
Address setup time	tAS	2.61		
Address hold time	tAH	0.88		
Input data setup time	tDS	5.22		
Input data hold time	tDH	0.80		
WEB access time	tWEC			9.82

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RB8S	2K words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed							
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)					
						IN	→	OUT	MIN.	TYP.	MAX.		
H01	DI0	2.4	N01	DO0	24.7	AD0 to AD10		(LH)	1.77	6.51	14.23		
:	:	:	:	:	:	→DO0 to DO7		(HH)	1.67	6.43	14.19		
H08	DI7	2.4	N08	DO7	24.7			(HL)	1.61	6.26	13.84		
H09	AD0	2.4	N09	TOUT	26.0			(LL)	1.56	6.25	13.89		
:	:	:											
H19	AD10	2.4							CSB	(LL)	1.50	5.34	11.60
H20	WEB	2.4							→DO0 to DO7	(LH)	1.50	5.34	11.60
H21	REB	1.0								(HL)	1.42	2.53	4.34
H22	CSB	2.4							REB	(LH)	1.21	2.03	3.38
H23	TIN	2.4							→DO0 to DO7	(HL)	1.02	1.86	3.23
H24	TEB	5.0							DI0 to DI7	(HH)	3.13	5.88	10.36
								→DO0 to DO7	(LL)	2.89	5.35	9.36	
Equivalent Cells		43983		Power (mW/MHz)		Rev.		1					

HIGH DENSITY SINGLE-PORT RAM BLOCK

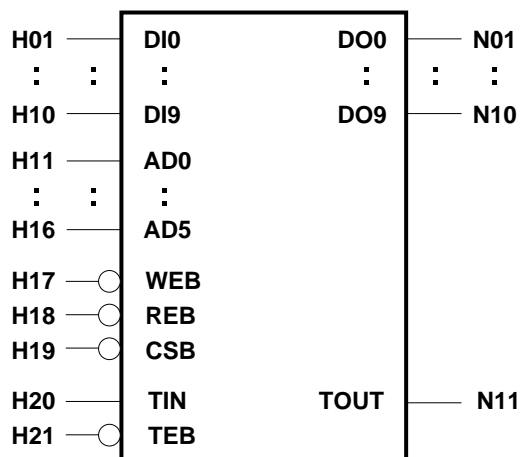
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	14.24		
Address access time	tACA			14.24
Address output hold time	tOH	1.81		
CSB access time	tCSC			11.60
CSB output hold time	tCSL	1.64		4.34
CSB output set time	tCLL	4.53		
REB access time	tREC			3.38
REB output hold time	tREL	1.18		3.23
REB output set time	tRLL	1.40		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.29		
CSB-WEB reset time	tCWR	4.86		
Write pulse width	tWP	4.86		
Address setup time	tAS	2.52		
Address hold time	tAH	0.91		
Input data setup time	tDS	5.12		
Input data hold time	tDH	0.88		
WEB access time	tWEC			10.34

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAB	64 words × 10 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H10	DI9	2.4	N10	DO9	23.7	AD0 to AD5 (LH)		2.86	4.73	7.78	
H11	AD0	2.4	N11	TOUT	26.0	→DO0 to DO9 (HH)		2.86	4.72	7.76	
:	:	:				(HL)		2.40	4.27	7.33	
H16	AD5	2.4				(LL)		2.40	4.28	7.35	
H17	WEB	2.4				CSB (LL)		2.29	4.30	7.56	
H18	REB	1.0				→DO0 to DO9 (LH)		2.29	4.30	7.56	
H19	CSB	1.0				(HL)		1.05	1.73	2.85	
H20	TIN	2.4				REB (LH)		0.76	1.27	2.11	
H21	TEB	5.0				→DO0 to DO9 (HL)		0.79	1.25	2.00	
						DI0 to DI9 (HH)		1.74	3.20	5.60	
						→DO0 to DO9 (LL)		1.60	2.92	5.07	
Equivalent Cells		2750		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

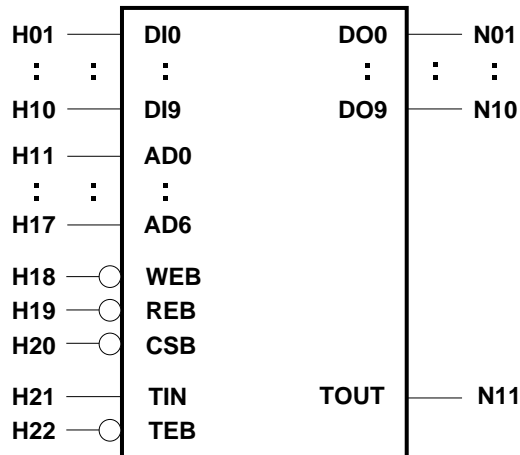
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.79		
Address access time	tACA			7.79
Address output hold time	tOH	2.40		
CSB access time	tCSC			7.58
CSB output hold time	tCSL	1.05		2.85
CSB output set time	tCLL	2.29		
REB access time	tREC			2.12
REB output hold time	tREL	0.79		2.01
REB output set time	tRLL	0.76		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.03		
CSB-WEB reset time	tCWR	3.90		
Write pulse width	tWP	3.90		
Address setup time	tAS	1.90		
Address hold time	tAH	0.23		
Input data setup time	tDS	2.47		
Input data hold time	tDH	0.73		
WEB access time	tWEC			4.70

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAD	128 words × 10 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DO _n	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DO_n : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)	
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)	2.88	5.19	8.97
:	:	:	:	:	:	→DO0 to DO9 (HH)	2.78	5.05	8.74
H10	DI9	2.4	N10	DO9	23.7	(HL)	1.61	4.11	8.19
H11	AD0	2.4	N11	TOUT	26.0	(LL)	1.50	4.06	8.24
:	:	:							
H17	AD6	2.4							
H18	WEB	2.4							
H19	REB	1.0							
H20	CSB	1.0							
H21	TIN	2.4							
H22	TEB	2.5							
						CSB (LL)	2.62	4.80	8.35
						→DO0 to DO9 (LH)	2.62	4.80	8.35
						(HL)	1.39	2.31	3.81
						REB (LH)	1.02	1.64	2.66
						→DO0 to DO9 (HL)	1.10	1.77	2.87
						DI0 to DI9 (HH)	1.97	3.55	6.13
						→DO0 to DO9 (LL)	1.94	3.46	5.93
Equivalent Cells		6383		Power (mW/MHz)		Rev.		1	

HIGH DENSITY SINGLE-PORT RAM BLOCK

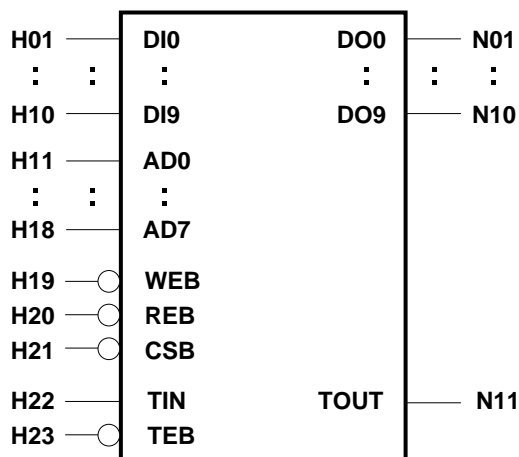
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.97		
Address access time	tACA			8.97
Address output hold time	tOH	1.51		
CSB access time	tCSC			8.36
CSB output hold time	tCSL	1.40		3.81
CSB output set time	tCLL	2.62		
REB access time	tREC			2.68
REB output hold time	tREL	1.11		2.88
REB output set time	tRLL	1.02		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.05		
CSB-WEB reset time	tCWR	3.96		
Write pulse width	tWP	3.96		
Address setup time	tAS	1.76		
Address hold time	tAH	0.33		
Input data setup time	tDS	2.50		
Input data hold time	tDH	0.83		
WEB access time	tWEC			5.23

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBAF	256 words × 10 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H10	DI9	2.4	N10	DO9	23.7	AD0 to AD7 (LH)		2.27	5.25	10.11	
H11	AD0	2.4	N11	TOUT	26.0	→DO0 to DO9 (HH)		2.27	5.24	10.08	
:	:	:				(HL)		2.11	4.91	9.47	
H18	AD7	2.4				(LL)		2.11	4.91	9.49	
H19	WEB	2.4				CSB (LL)		1.13	3.95	8.56	
H20	REB	1.0				→DO0 to DO9 (LH)		1.13	3.95	8.56	
H21	CSB	1.0				(HL)		0.99	1.73	2.94	
H22	TIN	2.4				REB (LH)		0.97	1.62	2.68	
H23	TEB	5.0				→DO0 to DO9 (HL)		0.74	1.31	2.25	
						DI0 to DI9 (HH)		1.99	3.70	6.49	
						→DO0 to DO9 (LL)		1.75	3.23	5.65	
Equivalent Cells		7673		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.21		
Address access time	tACA			10.21
Address output hold time	tOH	2.44		
CSB access time	tCSC			8.57
CSB output hold time	tCSL	1.15		2.94
CSB output set time	tCLL	3.38		
REB access time	tREC			2.69
REB output hold time	tREL	0.86		2.25
REB output set time	tRLL	1.13		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.67		
CSB-WEB reset time	tCWR	4.41		
Write pulse width	tWP	4.41		
Address setup time	tAS	1.89		
Address hold time	tAH	1.37		
Input data setup time	tDS	3.59		
Input data hold time	tDH	1.01		
WEB access time	tWEC			6.48

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																			
RBAH	512 words × 10 bits Single-port RAM																																																																																																																																																																				
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<p>Truth Table</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th>TEB</th> <th>TIN</th> <th>DIn</th> <th>ADn</th> <th>CSB</th> <th>WEB</th> <th>REB</th> <th>DOn</th> <th>TOUT</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>ADn</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>X</td> <td>Write</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>ADn</td> <td>0</td> <td>0</td> <td>0</td> <td>DIn</td> <td>X</td> <td>Write , Read</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>ADn</td> <td>0</td> <td>1</td> <td>0</td> <td>DOn</td> <td>X</td> <td>Read</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>X</td> <td>0</td> <td>X</td> <td>Hold</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>0</td> <td>X</td> <td>Hold</td> </tr> <tr> <td>0</td> <td>CLOCK</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>Result</td> <td>Test Mode</td> </tr> </tbody> </table> <div style="font-size: small;"> <p>X : Irrelevant DIn : Input data ADn : Address data CSB : Chip select WEB : Write enable REB : Read enable DOn : Output data TEB : Test enable TIN : Test clock TOUT: Output test result</p> </div>			TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation	1	X	DIn	ADn	0	0	1	0	X	Write	1	X	DIn	ADn	0	0	0	DIn	X	Write , Read	1	X	X	ADn	0	1	0	DOn	X	Read	1	X	X	X	1	X	X	0	X	Hold	1	X	X	X	X	1	1	0	X	Hold	0	CLOCK	X	X	X	X	X	X	Result	Test Mode																																																																																													
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HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.64		
Address access time	tACA			10.64
Address output hold time	tOH	1.73		
CSB access time	tCSC			9.46
CSB output hold time	tCSL	1.56		4.10
CSB output set time	tCLL	4.33		
REB access time	tREC			3.18
REB output hold time	tREL	1.18		3.12
REB output set time	tRLL	1.36		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.81		
CSB-WEB reset time	tCWR	4.44		
Write pulse width	tWP	4.44		
Address setup time	tAS	1.78		
Address hold time	tAH	0.59		
Input data setup time	tDS	3.49		
Input data hold time	tDH	0.99		
WEB access time	tWEC			6.94

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																			
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HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	14.54		
Address access time	tACA			14.54
Address output hold time	tOH	2.75		
CSB access time	tCSC			11.27
CSB output hold time	tCSL	1.23		3.27
CSB output set time	tCLL	3.64		
REB access time	tREC			2.94
REB output hold time	tREL	0.90		2.42
REB output set time	tRLL	1.18		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.90		
CSB-WEB reset time	tCWR	5.04		
Write pulse width	tWP	5.04		
Address setup time	tAS	2.94		
Address hold time	tAH	0.92		
Input data setup time	tDS	5.17		
Input data hold time	tDH	0.90		
WEB access time	tWEC			9.53

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																
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HIGH DENSITY SINGLE-PORT RAM BLOCK

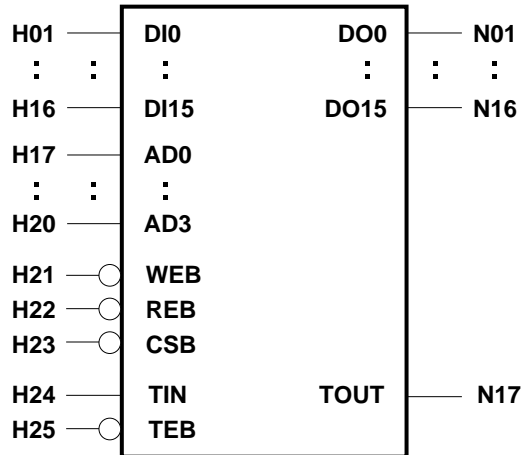
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	15.07		
Address access time	tACA			15.07
Address output hold time	tOH	1.81		
CSB access time	tCSC			12.16
CSB output hold time	tCSL	1.65		4.43
CSB output set time	tCLL	4.59		
REB access time	tREC			3.45
REB output hold time	tREL	1.23		3.30
REB output set time	tRLL	1.43		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	12.85		
CSB-WEB reset time	tCWR	5.06		
Write pulse width	tWP	5.06		
Address setup time	tAS	2.85		
Address hold time	tAH	0.96		
Input data setup time	tDS	5.07		
Input data hold time	tDH	0.99		
WEB access time	tWEC			10.05

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBC7	16 words × 16 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DO _n	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DO_n : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H16	DI15	2.4	N16	DO15	23.7	AD0 to AD3	(LH)		2.43	3.98	6.52
H17	AD0	2.4	N17	TOUT	26.0	→DO0 to DO15	(HH)		2.39	3.90	6.38
:	:	:					(HL)		2.11	3.80	6.55
H20	AD3	2.4					(LL)		2.15	3.88	6.70
H21	WEB	2.4				CSB	(LL)		2.11	3.60	6.03
H22	REB	1.0				→DO0 to DO15	(LH)		2.11	3.60	6.03
H23	CSB	1.0					(HL)		0.83	1.30	2.05
H24	TIN	2.4				REB	(LH)		0.86	1.42	2.33
H25	TEB	2.5				→DO0 to DO15	(HL)		0.92	1.42	2.24
						DI0 to DI15	(HH)		2.21	3.29	5.06
						→DO0 to DO15	(LL)		1.73	2.71	4.31
Equivalent Cells		2057			Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

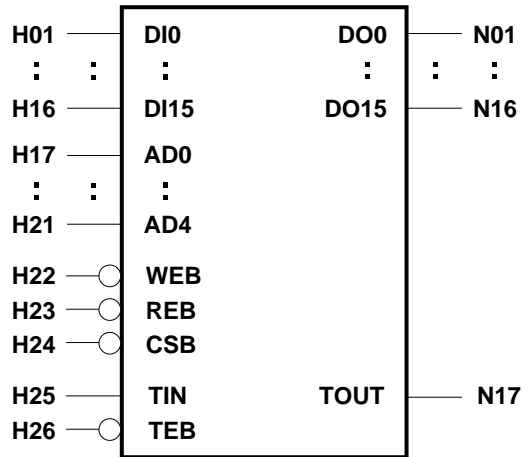
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.70		
Address access time	tACA			6.70
Address output hold time	tOH	2.20		
CSB access time	tCSC			6.05
CSB output hold time	tCSL	1.08		2.90
CSB output set time	tCLL	2.35		
REB access time	tREC			2.33
REB output hold time	tREL	0.92		2.24
REB output set time	tRLL	0.86		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.05		
CSB-WEB reset time	tCWR	4.34		
Write pulse width	tWP	4.34		
Address setup time	tAS	1.29		
Address hold time	tAH	0.42		
Input data setup time	tDS	3.20		
Input data hold time	tDH	0.69		
WEB access time	tWEC			5.80

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBC9	32 words × 16 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD4 (LH)			2.76	4.51	7.37
:	:	:	:	:	:	→DO0 to DO15 (HH)			2.72	4.44	7.23
H16	DI15	2.4	N16	DO15	23.7	(HL)			2.44	4.33	7.40
H17	AD0	2.4	N17	TOUT	26.0	(LL)			2.49	4.41	7.55
:	:	:				CSB (LL)			2.36	4.08	6.89
H21	AD4	2.4				→DO0 to DO15 (LH)			2.36	4.08	6.89
H22	WEB	2.4				(HL)			1.08	1.78	2.91
H23	REB	1.0				REB (LH)			0.87	1.43	2.34
H24	CSB	1.0				→DO0 to DO15 (HL)			0.92	1.43	2.25
H25	TIN	2.4				DI0 to DI15 (HH)			1.86	3.25	5.52
H26	TEB	5.0				→DO0 to DO15 (LL)			1.74	2.76	4.42
Equivalent Cells		2946		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

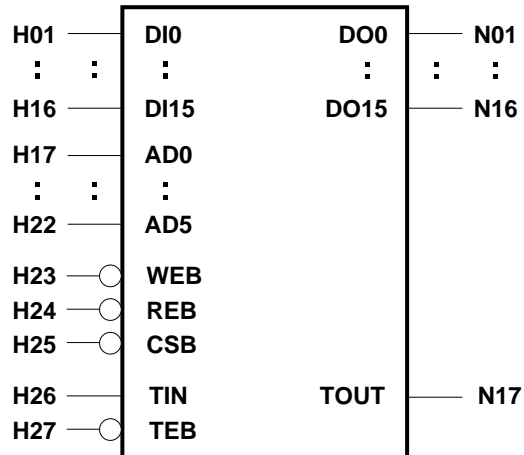
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.55		
Address access time	tACA			7.55
Address output hold time	tOH	2.45		
CSB access time	tCSC			6.90
CSB output hold time	tCSL	1.08		2.91
CSB output set time	tCLL	2.36		
REB access time	tREC			2.34
REB output hold time	tREL	0.93		2.25
REB output set time	tRLL	0.87		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.57		
CSB-WEB reset time	tCWR	4.84		
Write pulse width	tWP	4.84		
Address setup time	tAS	1.30		
Address hold time	tAH	0.43		
Input data setup time	tDS	3.21		
Input data hold time	tDH	0.70		
WEB access time	tWEC			5.91

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCB	64 words × 16 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H16	DI15	2.4	N16	DO15	23.7	AD0 to AD5 (LH)		2.92	4.54	7.18	
H17	AD0	2.4	N17	TOUT	26.0	→DO0 to DO15 (HH)		2.91	4.51	7.12	
:	:	:				(HL)		2.51	4.51	7.77	
H22	AD5	2.4				(LL)		2.52	4.54	7.83	
H23	WEB	2.4				CSB (LL)		2.39	4.32	7.47	
H24	REB	1.0				→DO0 to DO15 (LH)		2.39	4.32	7.47	
H25	CSB	1.0				(HL)		1.09	1.78	2.91	
H26	TIN	2.4				REB (LH)		0.82	1.34	2.19	
H27	TEB	2.5				→DO0 to DO15 (HL)		0.84	1.32	2.10	
						DI0 to DI15 (HH)		1.75	3.21	5.61	
						→DO0 to DO15 (LL)		1.61	2.92	5.06	
Equivalent Cells			4312			Power (mW/MHz)		Rev.		1	

HIGH DENSITY SINGLE-PORT RAM BLOCK

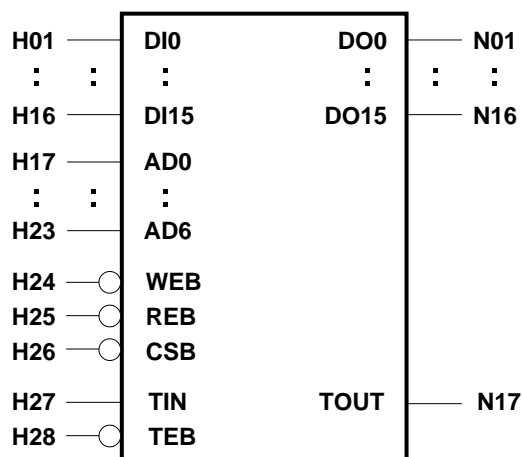
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.83		
Address access time	tACA			7.83
Address output hold time	tOH	2.51		
CSB access time	tCSC			7.48
CSB output hold time	tCSL	1.09		2.91
CSB output set time	tCLL	2.39		
REB access time	tREC			2.20
REB output hold time	tREL	0.85		2.11
REB output set time	tRLL	0.82		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.72		
CSB-WEB reset time	tCWR	3.68		
Write pulse width	tWP	3.68		
Address setup time	tAS	2.78		
Address hold time	tAH	0.26		
Input data setup time	tDS	2.57		
Input data hold time	tDH	1.60		
WEB access time	tWEC			4.90

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCD	128 words × 16 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)			2.05	4.56	8.67
:	:	:	:	:	:	→DO0 to DO15 (HH)			2.03	4.53	8.60
H16	DI15	2.4	N16	DO15	23.7	(HL)			1.85	4.35	8.44
H17	AD0	2.4	N17	TOUT	26.0	(LL)			1.86	4.39	8.52
:	:	:				CSB (LL)			1.06	3.56	7.64
H23	AD6	2.4				→DO0 to DO15 (LH)			1.06	3.56	7.64
H24	WEB	2.4				(HL)			0.96	1.65	2.77
H25	REB	1.0				REB (LH)			0.84	1.48	2.54
H26	CSB	1.0				→DO0 to DO15 (HL)			0.72	1.26	2.13
H27	TIN	2.4				DI0 to DI15 (HH)			1.85	3.46	6.09
H28	TEB	5.0				→DO0 to DO15 (LL)			1.64	2.99	5.20
Equivalent Cells		7269			Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.13		
Address access time	tACA			10.13
Address output hold time	tOH	2.13		
CSB access time	tCSC			7.64
CSB output hold time	tCSL	1.11		2.78
CSB output set time	tCLL	3.18		
REB access time	tREC			2.54
REB output hold time	tREL	0.72		2.13
REB output set time	tRLL	0.85		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.89		
CSB-WEB reset time	tCWR	3.78		
Write pulse width	tWP	3.78		
Address setup time	tAS	1.80		
Address hold time	tAH	1.31		
Input data setup time	tDS	3.41		
Input data hold time	tDH	0.85		
WEB access time	tWEC			5.96

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																							
RBCF	256 words × 16 bits Single-port RAM																																																																																																																																																																																								
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<p>Truth Table</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th>TEB</th> <th>TIN</th> <th>DIn</th> <th>ADn</th> <th>CSB</th> <th>WEB</th> <th>REB</th> <th>DOn</th> <th>TOUT</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>ADn</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>X</td> <td>Write</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>ADn</td> <td>0</td> <td>0</td> <td>0</td> <td>DIn</td> <td>X</td> <td>Write , Read</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>ADn</td> <td>0</td> <td>1</td> <td>0</td> <td>DOn</td> <td>X</td> <td>Read</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>X</td> <td>0</td> <td>X</td> <td>Hold</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>0</td> <td>X</td> <td>Hold</td> </tr> <tr> <td>0</td> <td>CLOCK</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>Result</td> <td>Test Mode</td> </tr> </tbody> </table> <div style="font-size: small;"> <p>X : Irrelevant DIn : Input data ADn : Address data CSB : Chip select WEB : Write enable REB : Read enable DOn : Output data TEB : Test enable TIN : Test clock TOUT: Output test result</p> </div>			TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation	1	X	DIn	ADn	0	0	1	0	X	Write	1	X	DIn	ADn	0	0	0	DIn	X	Write , Read	1	X	X	ADn	0	1	0	DOn	X	Read	1	X	X	X	1	X	X	0	X	Hold	1	X	X	X	X	1	1	0	X	Hold	0	CLOCK	X	X	X	X	X	X	Result	Test Mode																																																																																																																	
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1	X	X	X	1	X	X	0	X	Hold																																																																																																																																																																																
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Input			Output			Switching speed																																																																																																																																																																																			
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H17	AD0	2.4	N17	TOUT	26.0	(LL)			2.01	4.70	9.10																																																																																																																																																																														
:	:	:																																																																																																																																																																																							
H24	AD7	2.4							CSB (LL)	1.12	4.00	8.70																																																																																																																																																																													
H25	WEB	2.4							→DO0 to DO15 (LH)	1.12	4.00	8.70																																																																																																																																																																													
H26	REB	1.0							(HL)	0.99	1.70	2.85																																																																																																																																																																													
H27	CSB	1.0							REB (LH)	0.96	1.61	2.66																																																																																																																																																																													
H28	TIN	2.4							→DO0 to DO15 (HL)	0.73	1.27	2.16																																																																																																																																																																													
H29	TEB	5.0							DI0 to DI15 (HH)	1.99	3.70	6.49																																																																																																																																																																													
						→DO0 to DO15 (LL)			1.75	3.23	5.65																																																																																																																																																																														
Equivalent Cells		12242		Power (mW/MHz)				Rev.		1																																																																																																																																																																															

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.97		
Address access time	tACA			9.97
Address output hold time	tOH	2.31		
CSB access time	tCSC			8.70
CSB output hold time	tCSL	1.15		2.85
CSB output set time	tCLL	3.34		
REB access time	tREC			2.68
REB output hold time	tREL	0.85		2.16
REB output set time	tRLL	1.11		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.47		
CSB-WEB reset time	tCWR	4.18		
Write pulse width	tWP	4.18		
Address setup time	tAS	1.92		
Address hold time	tAH	1.37		
Input data setup time	tDS	3.62		
Input data hold time	tDH	0.97		
WEB access time	tWEC			7.39

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																							
RBCH	512 words × 16 bits Single-port RAM																																																																																																																																																								
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TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation																																																																																																																																																
1	X	DIn	ADn	0	0	1	0	X	Write																																																																																																																																																
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read																																																																																																																																																
1	X	X	ADn	0	1	0	DOn	X	Read																																																																																																																																																
1	X	X	X	1	X	X	0	X	Hold																																																																																																																																																
1	X	X	X	X	1	1	0	X	Hold																																																																																																																																																
0	CLOCK	X	X	X	X	X	X	Result	Test Mode																																																																																																																																																
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Equivalent Cells		24114		Power (mW/MHz)		Rev.		1																																																																																																																																																	

HIGH DENSITY SINGLE-PORT RAM BLOCK

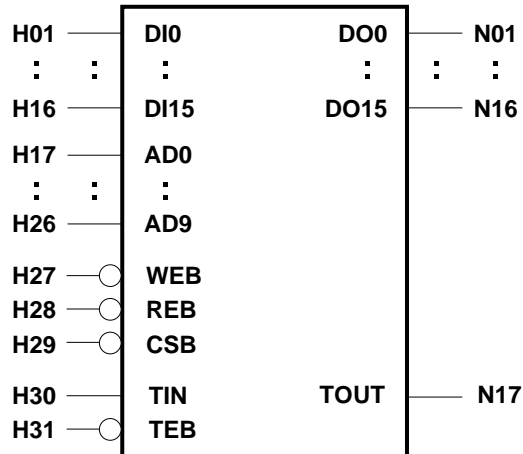
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.53		
Address access time	tACA			10.53
Address output hold time	tOH	1.73		
CSB access time	tCSC			9.62
CSB output hold time	tCSL	1.56		4.00
CSB output set time	tCLL	4.33		
REB access time	tREC			3.20
REB output hold time	tREL	1.18		3.07
REB output set time	tRLL	1.36		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.64		
CSB-WEB reset time	tCWR	4.23		
Write pulse width	tWP	4.23		
Address setup time	tAS	1.83		
Address hold time	tAH	0.58		
Input data setup time	tDS	3.51		
Input data hold time	tDH	0.97		
WEB access time	tWEC			7.96

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBCM	1K words × 16 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD9 (LH)			2.94	7.05	13.76	
:	:	:	:	:	:	→DO0 to DO15 (HH)			2.92	7.02	13.72	
H16	DI15	2.4	N16	DO15	23.7	(HL)			2.39	6.42	12.99	
H17	AD0	2.4	N17	TOUT	26.0	(LL)			2.40	6.45	13.04	
:	:	:										
H26	AD9	2.4							CSB (LL)	1.20	4.82	10.73
H27	WEB	2.4							→DO0 to DO15 (LH)	1.20	4.82	10.73
H28	REB	1.0							(HL)	1.07	1.89	3.22
H29	CSB	1.0							REB (LH)	1.02	1.74	2.91
H30	TIN	2.4							→DO0 to DO15 (HL)	0.76	1.37	2.38
H31	TEB	5.0							DI0 to DI15 (HH)	2.94	5.58	9.88
								→DO0 to DO15 (LL)	2.61	4.86	8.52	
Equivalent Cells		44017		Power (mW/MHz)				Rev.	1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	13.77		
Address access time	tACA			13.77
Address output hold time	tOH	2.76		
CSB access time	tCSC			10.73
CSB output hold time	tCSL	1.23		3.22
CSB output set time	tCLL	3.60		
REB access time	tREC			2.91
REB output hold time	tREL	0.87		2.39
REB output set time	tRLL	1.18		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.36		
CSB-WEB reset time	tCWR	4.86		
Write pulse width	tWP	4.86		
Address setup time	tAS	2.62		
Address hold time	tAH	0.88		
Input data setup time	tDS	5.20		
Input data hold time	tDH	0.81		
WEB access time	tWEC			9.87

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																			
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HIGH DENSITY SINGLE-PORT RAM BLOCK

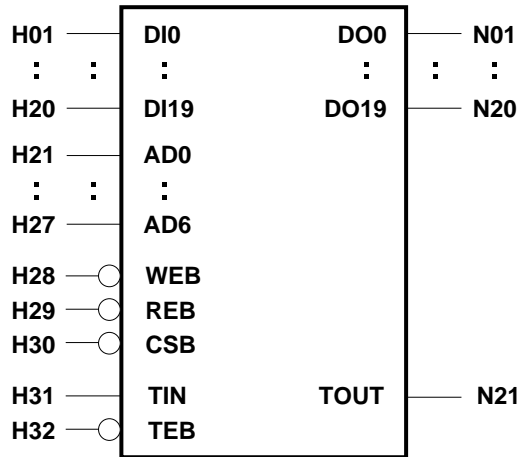
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.93		
Address access time	tACA			7.93
Address output hold time	tOH	2.46		
CSB access time	tCSC			7.67
CSB output hold time	tCSL	1.11		2.95
CSB output set time	tCLL	2.35		
REB access time	tREC			2.21
REB output hold time	tREL	0.85		2.12
REB output set time	tRLL	0.82		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.10		
CSB-WEB reset time	tCWR	3.78		
Write pulse width	tWP	3.78		
Address setup time	tAS	2.06		
Address hold time	tAH	0.26		
Input data setup time	tDS	2.42		
Input data hold time	tDH	0.83		
WEB access time	tWEC			4.83

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBED	128 words × 20 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)			2.95	5.30	9.13	
:	:	:	:	:	:	→DO0 to DO19 (HH)			2.86	5.16	8.91	
H20	DI19	2.4	N20	DO19	23.7	(HL)			1.68	4.23	8.39	
H21	AD0	2.4	N21	TOUT	26.0	(LL)			1.57	4.22	8.54	
:	:	:										
H27	AD6	2.4							CSB (LL)	2.69	4.90	8.52
H28	WEB	2.4							→DO0 to DO19 (LH)	2.69	4.90	8.52
H29	REB	1.0							(HL)	1.45	2.39	3.93
H30	CSB	1.0							REB (LH)	1.09	1.76	2.85
H31	TIN	2.4							→DO0 to DO19 (HL)	1.21	1.93	3.09
H32	TEB	2.5							DI0 to DI19 (HH)	1.99	3.57	6.15
						→DO0 to DO19 (LL)			1.97	3.48	5.95	
Equivalent Cells		10220		Power (mW/MHz)				Rev.	1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

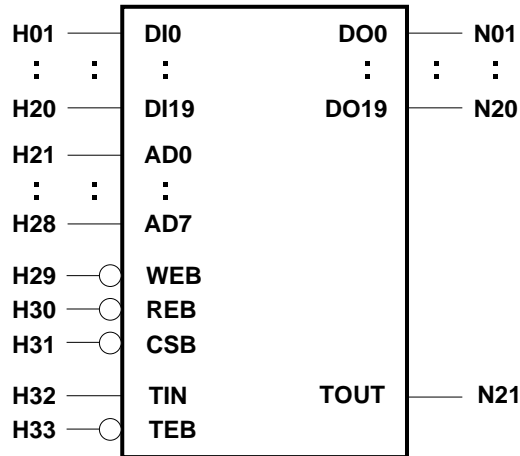
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.14		
Address access time	tACA			9.14
Address output hold time	tOH	1.58		
CSB access time	tCSC			8.52
CSB output hold time	tCSL	1.45		3.94
CSB output set time	tCLL	2.69		
REB access time	tREC			2.85
REB output hold time	tREL	1.22		3.09
REB output set time	tRLL	1.09		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.56		
CSB-WEB reset time	tCWR	4.09		
Write pulse width	tWP	4.09		
Address setup time	tAS	2.14		
Address hold time	tAH	0.33		
Input data setup time	tDS	2.42		
Input data hold time	tDH	0.95		
WEB access time	tWEC			5.50

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBEF	256 words × 20 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DO _n	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DO_n : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD7 (LH)			2.29	5.28	10.17	
:	:	:	:	:	:	→DO0 to DO19 (HH)			2.28	5.26	10.11	
H20	DI19	2.4	N20	DO19	23.7	(HL)			2.12	4.92	9.49	
H21	AD0	2.4	N21	TOUT	26.0	(LL)			2.13	4.95	9.54	
:	:	:										
H28	AD7	2.4							CSB (LL)	1.13	3.97	8.59
H29	WEB	2.4							→DO0 to DO19 (LH)	1.13	3.97	8.59
H30	REB	1.0							(HL)	1.01	1.75	2.96
H31	CSB	1.0							REB (LH)	0.98	1.64	2.71
H32	TIN	2.4							→DO0 to DO19 (HL)	0.76	1.33	2.27
H33	TEB	5.0							DI0 to DI19 (HH)	1.99	3.70	6.49
						→DO0 to DO19 (LL)			1.75	3.23	5.65	
Equivalent Cells		15104		Power (mW/MHz)		Rev.		1				

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.17		
Address access time	tACA			10.17
Address output hold time	tOH	2.44		
CSB access time	tCSC			8.59
CSB output hold time	tCSL	1.16		2.97
CSB output set time	tCLL	3.41		
REB access time	tREC			2.71
REB output hold time	tREL	0.87		2.28
REB output set time	tRLL	1.13		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.71		
CSB-WEB reset time	tCWR	4.44		
Write pulse width	tWP	4.44		
Address setup time	tAS	1.90		
Address hold time	tAH	1.37		
Input data setup time	tDS	3.57		
Input data hold time	tDH	1.03		
WEB access time	tWEC			7.34

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																			
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HIGH DENSITY SINGLE-PORT RAM BLOCK

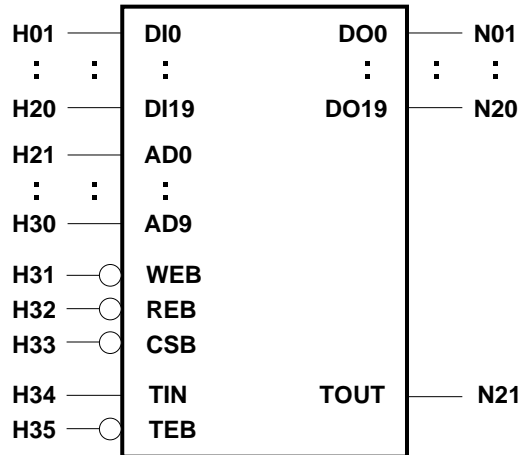
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.72		
Address access time	tACA			10.72
Address output hold time	tOH	1.74		
CSB access time	tCSC			9.51
CSB output hold time	tCSL	1.58		4.13
CSB output set time	tCLL	4.39		
REB access time	tREC			3.24
REB output hold time	tREL	1.21		3.18
REB output set time	tRLL	1.39		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.89		
CSB-WEB reset time	tCWR	4.49		
Write pulse width	tWP	4.49		
Address setup time	tAS	1.82		
Address hold time	tAH	0.58		
Input data setup time	tDS	3.45		
Input data hold time	tDH	1.02		
WEB access time	tWEC			7.91

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBEM	1K words × 20 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD9 (LH)			3.06	7.44	14.58	
:	:	:	:	:	:	→DO0 to DO19 (HH)			3.05	7.42	14.54	
H20	DI19	2.4	N20	DO19	23.7	(HL)			2.39	6.73	13.81	
H21	AD0	2.4	N21	TOUT	26.0	(LL)			2.40	6.76	13.87	
:	:	:										
H30	AD9	2.4							CSB (LL)	1.23	5.05	11.29
H31	WEB	2.4							→DO0 to DO19 (LH)	1.23	5.05	11.29
H32	REB	1.0							(HL)	1.08	1.93	3.31
H33	CSB	1.0							REB (LH)	1.03	1.77	2.96
H34	TIN	2.4							→DO0 to DO19 (HL)	0.79	1.42	2.45
H35	TEB	5.0							DI0 to DI19 (HH)	2.94	5.58	9.88
								→DO0 to DO19 (LL)	2.61	4.81	8.39	
Equivalent Cells		54541		Power (mW/MHz)				Rev.	1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

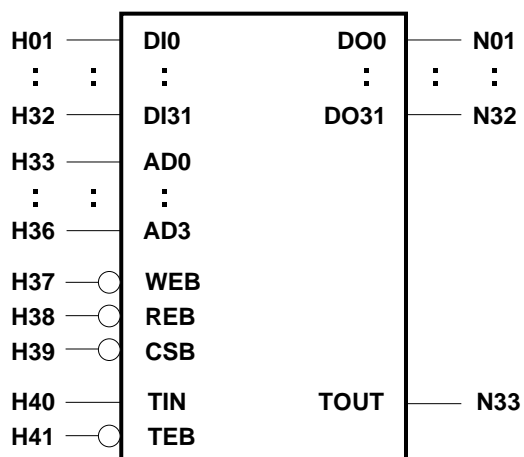
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	14.59		
Address access time	tACA			14.59
Address output hold time	tOH	2.76		
CSB access time	tCSC			11.29
CSB output hold time	tCSL	1.25		3.31
CSB output set time	tCLL	3.67		
REB access time	tREC			2.97
REB output hold time	tREL	0.91		2.45
REB output set time	tRLL	1.20		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.93		
CSB-WEB reset time	tCWR	5.06		
Write pulse width	tWP	5.06		
Address setup time	tAS	2.95		
Address hold time	tAH	0.92		
Input data setup time	tDS	5.15		
Input data hold time	tDH	0.92		
WEB access time	tWEC			9.58

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBH7	16 words × 32 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H32	DI31	2.4	N32	DO31	23.7	AD0 to AD3	(LH)		2.65	4.34	7.09
H33	AD0	2.4	N33	TOUT	26.0	→DO0 to DO31	(HH)		2.55	4.16	6.77
:	:	:					(HL)		2.28	4.05	6.93
H36	AD3	2.4					(LL)		2.37	4.23	7.27
H37	WEB	2.4				CSB	(LL)		2.26	3.81	6.35
H38	REB	1.0				→DO0 to DO31	(LH)		2.26	3.81	6.35
H39	CSB	1.0					(HL)		1.02	1.55	2.43
H40	TIN	2.4				REB	(LH)		1.01	1.63	2.64
H41	TEB	2.5				→DO0 to DO31	(HL)		1.11	1.68	2.61
						DI0 to DI31	(HH)		1.86	3.21	5.42
						→DO0 to DO31	(LL)		1.73	2.71	4.31
Equivalent Cells		3933			Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

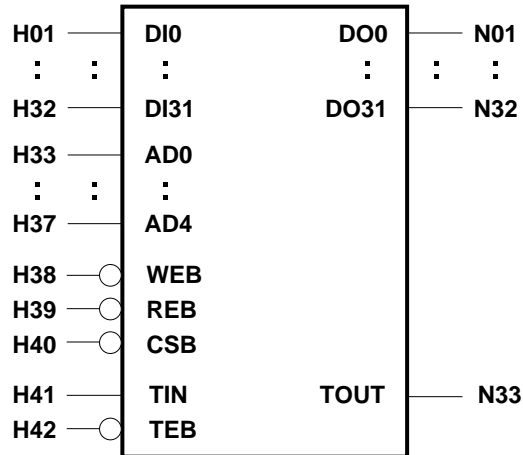
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.27		
Address access time	tACA			7.27
Address output hold time	tOH	2.37		
CSB access time	tCSC			6.36
CSB output hold time	tCSL	1.26		3.27
CSB output set time	tCLL	2.50		
REB access time	tREC			2.64
REB output hold time	tREL	1.11		2.61
REB output set time	tRLL	1.01		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.72		
CSB-WEB reset time	tCWR	4.60		
Write pulse width	tWP	4.60		
Address setup time	tAS	2.05		
Address hold time	tAH	0.55		
Input data setup time	tDS	3.02		
Input data hold time	tDH	1.09		
WEB access time	tWEC			6.31

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBH9	32 words × 32 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DOn	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DOn : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD4 (LH)			2.98	4.87	7.95
:	:	:	:	:	:	→DO0 to DO31 (HH)			2.89	4.69	7.63
H32	DI31	2.4	N32	DO31	23.7	(HL)			2.62	4.58	7.79
H33	AD0	2.4	N33	TOUT	26.0	(LL)			2.70	4.76	8.12
:	:	:				CSB (LL)			2.51	4.29	7.20
H37	AD4	2.4				→DO0 to DO31 (LH)			2.51	4.29	7.20
H38	WEB	2.4				(HL)			1.27	2.03	3.28
H39	REB	1.0				REB (LH)			1.02	1.64	2.65
H40	CSB	1.0				→DO0 to DO31 (HL)			1.12	1.69	2.62
H41	TIN	2.4				DI0 to DI31 (HH)			1.86	3.26	5.53
H42	TEB	2.5				→DO0 to DO31 (LL)			1.74	2.76	4.42
Equivalent Cells		5694		Power (mW/MHz)		Rev.		1			

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.12		
Address access time	tACA			8.12
Address output hold time	tOH	2.62		
CSB access time	tCSC			7.21
CSB output hold time	tCSL	1.27		3.28
CSB output set time	tCLL	2.51		
REB access time	tREC			2.65
REB output hold time	tREL	1.12		2.62
REB output set time	tRLL	1.02		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.72		
CSB-WEB reset time	tCWR	5.10		
Write pulse width	tWP	5.10		
Address setup time	tAS	2.06		
Address hold time	tAH	0.56		
Input data setup time	tDS	3.03		
Input data hold time	tDH	1.10		
WEB access time	tWEC			6.42

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																	
RBHB	64 words × 32 bits Single-port RAM																																																																																																																																																																																		
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Equivalent Cells		8411		Power (mW/MHz)		Rev.		1																																																																																																																																																																											

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.13		
Address access time	tACA			8.13
Address output hold time	tOH	2.60		
CSB access time	tCSC			7.65
CSB output hold time	tCSL	1.18		3.12
CSB output set time	tCLL	2.47		
REB access time	tREC			2.38
REB output hold time	tREL	0.93		2.31
REB output set time	tRLL	0.90		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.31		
CSB-WEB reset time	tCWR	3.82		
Write pulse width	tWP	3.82		
Address setup time	tAS	3.16		
Address hold time	tAH	0.33		
Input data setup time	tDS	2.47		
Input data hold time	tDH	1.80		
WEB access time	tWEC			5.17

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																			
RBHD	128 words × 32 bits Single-port RAM																																																																																																																																																																																																				
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HIGH DENSITY SINGLE-PORT RAM BLOCK

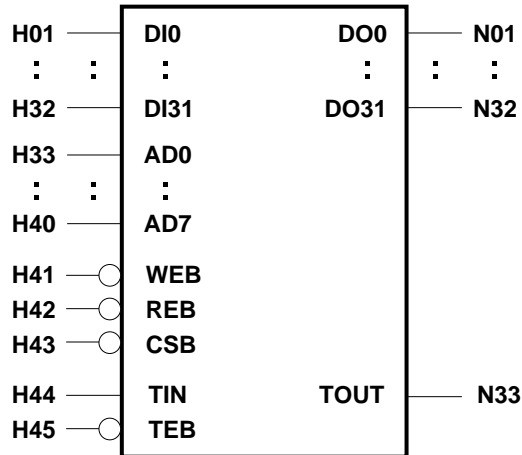
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.41		
Address access time	tACA			10.41
Address output hold time	tOH	2.18		
CSB access time	tCSC			7.75
CSB output hold time	tCSL	1.18		2.91
CSB output set time	tCLL	3.31		
REB access time	tREC			2.64
REB output hold time	tREL	0.88		2.25
REB output set time	tRLL	1.02		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.81		
CSB-WEB reset time	tCWR	3.88		
Write pulse width	tWP	3.88		
Address setup time	tAS	1.86		
Address hold time	tAH	1.35		
Input data setup time	tDS	3.32		
Input data hold time	tDH	0.97		
WEB access time	tWEC			6.13

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBHF	256 words × 32 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DO _n	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DO_n : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD7	(LH)	2.38	5.30	10.06
:	:	:	:	:	:		→DO0 to DO31	(HH)	2.36	5.26
H32	DI31	2.4	N32	DO31	23.7	CSB	(HL)	2.02	4.72	9.11
H33	AD0	2.4	N33	TOUT	26.0		(LL)	2.04	4.75	9.18
:	:	:					(LL)	1.13	4.03	8.74
H40	AD7	2.4				→DO0 to DO31	(LH)	1.13	4.03	8.74
H41	WEB	2.4					(HL)	1.02	1.74	2.91
H42	REB	1.0				REB	(LH)	0.98	1.65	2.73
H43	CSB	1.0					→DO0 to DO31	(HL)	0.76	1.31
H44	TIN	2.4				DI0 to DI31	(HH)	1.99	3.70	6.49
H45	TEB	5.0					→DO0 to DO31	(LL)	1.75	3.23
Equivalent Cells		24189		Power (mW/MHz)		Rev.		1		

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.06		
Address access time	tACA			10.06
Address output hold time	tOH	2.34		
CSB access time	tCSC			8.75
CSB output hold time	tCSL	1.18		2.91
CSB output set time	tCLL	3.41		
REB access time	tREC			2.73
REB output hold time	tREL	0.87		2.21
REB output set time	tRLL	1.13		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.55		
CSB-WEB reset time	tCWR	4.23		
Write pulse width	tWP	4.23		
Address setup time	tAS	1.94		
Address hold time	tAH	1.38		
Input data setup time	tDS	3.58		
Input data hold time	tDH	1.03		
WEB access time	tWEC			6.66

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																			
RBHH	512 words × 32 bits Single-port RAM																																																																																																																																																																				
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TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation																																																																																																																																																												
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1	X	X	ADn	0	1	0	DO _n	X	Read																																																																																																																																																												
1	X	X	X	1	X	X	0	X	Hold																																																																																																																																																												
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HIGH DENSITY SINGLE-PORT RAM BLOCK

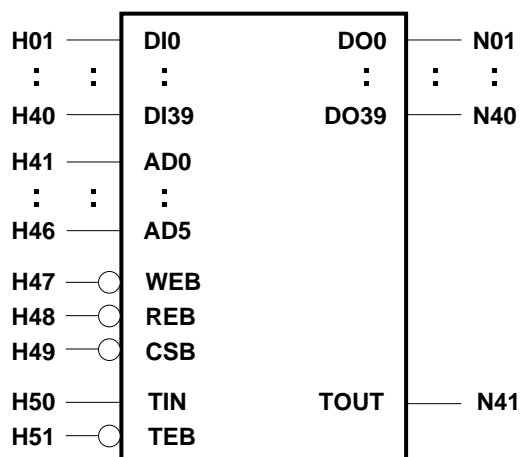
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.72		
Address access time	tACA			10.72
Address output hold time	tOH	1.76		
CSB access time	tCSC			9.70
CSB output hold time	tCSL	1.59		4.07
CSB output set time	tCLL	4.43		
REB access time	tREC			3.31
REB output hold time	tREL	1.23		3.18
REB output set time	tRLL	1.41		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.79		
CSB-WEB reset time	tCWR	4.32		
Write pulse width	tWP	4.32		
Address setup time	tAS	1.89		
Address hold time	tAH	0.58		
Input data setup time	tDS	3.43		
Input data hold time	tDH	1.03		
WEB access time	tWEC			8.15

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBKB	64 words × 40 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DO _n	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DO_n : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD5 (LH)			3.05	5.01	8.22	
:	:	:	:	:	:	→DO0 to DO39 (HH)			3.01	4.93	8.06	
H40	DI39	2.4	N40	DO39	23.7	(HL)			2.55	4.48	7.63	
H41	AD0	2.4	N41	TOUT	26.0	(LL)			2.59	4.56	7.78	
:	:	:										
H46	AD5	2.4							CSB (LL)	2.43	4.48	7.83
H47	WEB	2.4							→DO0 to DO39 (LH)	2.43	4.48	7.83
H48	REB	1.0							(HL)	1.20	1.95	3.17
H49	CSB	1.0							REB (LH)	0.90	1.46	2.36
H50	TIN	2.4							→DO0 to DO39 (HL)	0.94	1.47	2.33
H51	TEB	2.5							DI0 to DI39 (HH)	1.75	3.21	5.61
						→DO0 to DO39 (LL)			1.61	2.93	5.08	
Equivalent Cells		10349		Power (mW/MHz)		Rev.		1				

HIGH DENSITY SINGLE-PORT RAM BLOCK

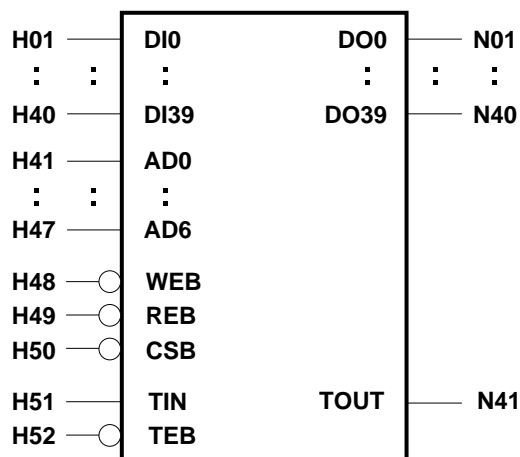
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.22		
Address access time	tACA			8.22
Address output hold time	tOH	2.55		
CSB access time	tCSC			7.83
CSB output hold time	tCSL	1.20		3.18
CSB output set time	tCLL	2.43		
REB access time	tREC			2.38
REB output hold time	tREL	0.94		2.33
REB output set time	tRLL	0.90		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.86		
CSB-WEB reset time	tCWR	4.09		
Write pulse width	tWP	4.09		
Address setup time	tAS	2.44		
Address hold time	tAH	0.33		
Input data setup time	tDS	2.31		
Input data hold time	tDH	1.03		
WEB access time	tWEC			5.71

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBKD	128 words × 40 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DO _n	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DO_n : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)	
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	AD0 to AD6 (LH)	3.07	5.50	9.47
:	:	:	:	:	:	→DO0 to DO39 (HH)	2.99	5.36	9.22
H40	DI39	2.4	N40	DO39	23.7	(HL)	1.78	4.46	8.83
H41	AD0	2.4	N41	TOUT	26.0	(LL)	1.67	4.53	9.20
:	:	:							
H47	AD6	2.4							
H48	WEB	2.4	CSB (LL)	2.81	5.10	8.83			
H49	REB	1.0	→DO0 to DO39 (LH)	2.81	5.10	8.83			
H50	CSB	1.0	(HL)	1.56	2.55	4.16			
H51	TIN	2.4	REB (LH)	1.27	1.99	3.18			
H52	TEB	2.5	→DO0 to DO39 (HL)	1.41	2.22	3.53			
						DI0 to DI39 (HH)	1.99	3.57	6.15
						→DO0 to DO39 (LL)	1.97	3.49	5.97
Equivalent Cells		20195		Power (mW/MHz)		Rev.		1	

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.47		
Address access time	tACA			9.47
Address output hold time	tOH	1.67		
CSB access time	tCSC			8.84
CSB output hold time	tCSL	1.56		4.16
CSB output set time	tCLL	2.82		
REB access time	tREC			3.18
REB output hold time	tREL	1.41		3.54
REB output set time	tRLL	1.27		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.91		
CSB-WEB reset time	tCWR	4.39		
Write pulse width	tWP	4.39		
Address setup time	tAS	3.04		
Address hold time	tAH	0.48		
Input data setup time	tDS	2.32		
Input data hold time	tDH	1.40		
WEB access time	tWEC			6.08

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																
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HIGH DENSITY SINGLE-PORT RAM BLOCK

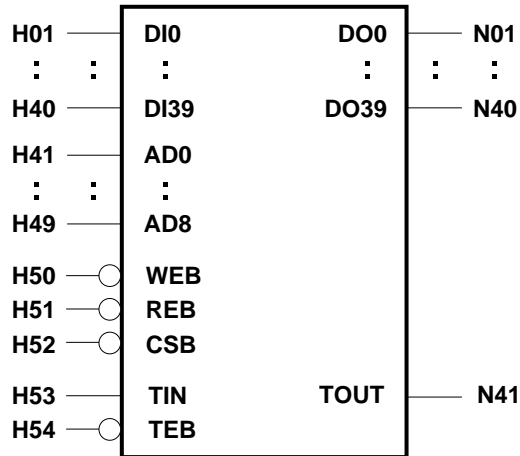
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.25		
Address access time	tACA			10.25
Address output hold time	tOH	2.47		
CSB access time	tCSC			8.65
CSB output hold time	tCSL	1.18		3.04
CSB output set time	tCLL	3.48		
REB access time	tREC			2.77
REB output hold time	tREL	0.90		2.33
REB output set time	tRLL	1.16		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.80		
CSB-WEB reset time	tCWR	4.49		
Write pulse width	tWP	4.49		
Address setup time	tAS	1.93		
Address hold time	tAH	1.38		
Input data setup time	tDS	3.52		
Input data hold time	tDH	1.09		
WEB access time	tWEC			6.61

HIGH DENSITY SINGLE-PORT RAM BLOCK

Block Type	Function	SSI Family
RBKH	512 words × 40 bits Single-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	ADn	CSB	WEB	REB	DO _n	TOUT	Operation
1	X	DIn	ADn	0	0	1	0	X	Write
1	X	DIn	ADn	0	0	0	DIn	X	Write , Read
1	X	X	ADn	0	1	0	DO _n	X	Read
1	X	X	X	1	X	X	0	X	Hold
1	X	X	X	X	1	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	Result	Test Mode

X : Irrelevant
DIn : Input data
ADn : Address data
CSB : Chip select
WEB : Write enable
REB : Read enable
DO_n : Output data
TEB : Test enable
TIN : Test clock
TOUT : Output test result

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)	
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7	AD0 to AD8 (LH)	1.76	5.24	10.91
:	:	:	:	:	:	→DO0 to DO39 (HH)	1.66	5.12	10.76
H40	DI39	2.4	N40	DO39	24.7	(HL)	1.59	4.99	10.53
H41	AD0	2.4	N41	TOUT	26.0	(LL)	1.53	5.00	10.67
:	:	:				CSB (LL)	1.50	4.57	9.59
H49	AD8	2.4				→DO0 to DO39 (LH)	1.50	4.57	9.59
H50	WEB	2.4				(HL)	1.39	2.45	4.18
H51	REB	1.0				REB (LH)	1.24	2.04	3.34
H52	CSB	2.4				→DO0 to DO39 (HL)	1.09	1.93	3.30
H53	TIN	2.4				DI0 to DI39 (HH)	2.18	4.00	6.97
H54	TEB	5.0				→DO0 to DO39 (LL)	2.03	3.73	6.51
Equivalent Cells		49856		Power (mW/MHz)		Rev.		1	

HIGH DENSITY SINGLE-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.91		
Address access time	tACA			10.91
Address output hold time	tOH	1.76		
CSB access time	tCSC			9.60
CSB output hold time	tCSL	1.60		4.19
CSB output set time	tCLL	5.57		
REB access time	tREC			3.35
REB output hold time	tREL	1.26		3.30
REB output set time	tRLL	1.44		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.05		
CSB-WEB reset time	tCWR	4.59		
Write pulse width	tWP	4.59		
Address setup time	tAS	1.88		
Address hold time	tAH	0.58		
Input data setup time	tDS	3.38		
Input data hold time	tDH	1.08		
WEB access time	tWEC			8.10

[MEMO]

CHAPTER 2

HIGH DENSITY

DUAL-PORT RAM BLOCK

(Soft Macro)

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																																																								
R947	16 words × 4 bits Dual-port RAM																																																																																																																																																																																																																																																																																																																									
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Equivalent Cells			883			Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																																																																																

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.26		
Address access time	tACA			7.26
Address output hold time	tOH	1.90		
RSB access time	tREC			1.65
RSB output hold time	tREL	0.70		2.20
RSB output set time	tRLL	0.61		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.14		
WSB-WEB reset time	tCWR	5.10		
Write pulse width	tWP	5.10		
Address setup time	tAS	2.83		
Address hold time	tAH	0.21		
Input data setup time	tDS	3.34		
Input data hold time	tDH	0.31		
WEB access time	tWEC			8.28

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																				
R949	32 words × 4 bits Dual-port RAM																																																																																																																																																																																																																																																																																					
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TYP.	MAX.	H01	DI0	2.4	N01	DO0	23.7							:	:	:	:	:	:							H04	DI3	2.4	N04	DO3	23.7	RA0 to RA5 (LH)		1.38	3.61	7.26	H05	WA0	2.4	N05	TOUT	26.0	→DO0 to DO3 (HH)		1.38	3.61	7.26	:	:	:				(HL)		2.30	4.26	7.46	H09	WA5	2.4				(LL)		2.30	4.26	7.46	H10	RA0	2.4				RSB (LH)		0.62	1.01	1.66	:	:	:				→DO0 to DO3 (HL)		0.71	1.06	1.65	H14	RA5	2.4									H15	WEB	2.4				DI0 to DI3 (HH)		1.48	3.02	5.54	H16	WSB	1.0				→DO0 to DO3 (LL)		1.57	3.18	5.79	H17	RSB	1.0									H18	TIN	2.4									H19	TEB	2.5								
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1	X	X	X	0	1	Hold	X	X	X	X																																																																																																																																																																																																																																																																												
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X																																																																																																																																																																																																																																																																												
1	X	X	X	X	X	X	X	1	0	X																																																																																																																																																																																																																																																																												
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																																												
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0	CLOCK	X	X	X	X	X	X	X	X	RESULT																																																																																																																																																																																																																																																																												
Input			Output			Switching speed																																																																																																																																																																																																																																																																																
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)																																																																																																																																																																																																																																																																														
						IN	→	OUT	MIN.	TYP.	MAX.																																																																																																																																																																																																																																																																											
H01	DI0	2.4	N01	DO0	23.7																																																																																																																																																																																																																																																																																	
:	:	:	:	:	:																																																																																																																																																																																																																																																																																	
H04	DI3	2.4	N04	DO3	23.7	RA0 to RA5 (LH)		1.38	3.61	7.26																																																																																																																																																																																																																																																																												
H05	WA0	2.4	N05	TOUT	26.0	→DO0 to DO3 (HH)		1.38	3.61	7.26																																																																																																																																																																																																																																																																												
:	:	:				(HL)		2.30	4.26	7.46																																																																																																																																																																																																																																																																												
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H16	WSB	1.0				→DO0 to DO3 (LL)		1.57	3.18	5.79																																																																																																																																																																																																																																																																												
H17	RSB	1.0																																																																																																																																																																																																																																																																																				
H18	TIN	2.4																																																																																																																																																																																																																																																																																				
H19	TEB	2.5																																																																																																																																																																																																																																																																																				
Equivalent Cells	1427		Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																																															

HIGH DENSITY DUAL-PORT RAM BLOCK

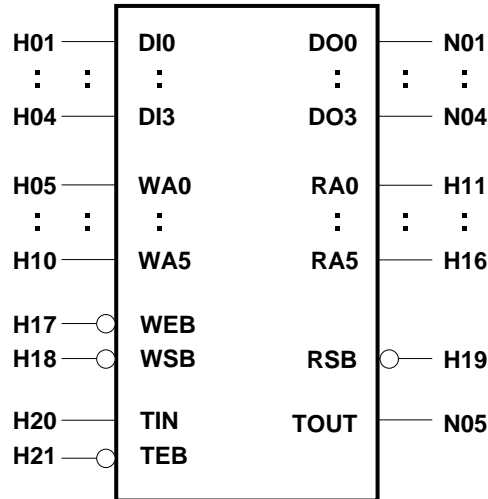
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.46		
Address access time	tACA			7.46
Address output hold time	tOH	1.99		
RSB access time	tREC			1.66
RSB output hold time	tREL	0.71		2.21
RSB output set time	tRLL	0.62		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.56		
WSB-WEB reset time	tCWR	5.50		
Write pulse width	tWP	5.50		
Address setup time	tAS	2.84		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.35		
Input data hold time	tDH	0.32		
WEB access time	tWEC			8.38

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94B	64 words × 4 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7					
:	:	:	:	:	:					
H04	DI3	2.4	N04	DO3	24.7	RA0 to RA5 (LH)		0.54	3.22	7.60
H05	WA0	2.4	N05	TOUT	26.0	→DO0 to DO3 (HH)		0.46	3.17	7.60
:	:	:				(HL)		1.53	3.91	7.80
H10	WA5	2.4				(LL)		1.46	3.87	7.80
H11	RA0	2.4				RSB (LH)		0.89	1.38	2.18
:	:	:				→DO0 to DO3 (HL)		1.04	1.53	2.35
H16	RA5	2.4								
H17	WEB	2.4				DI0 to DI3 (HH)		1.67	3.30	5.96
H18	WSB	2.4				→DO0 to DO3 (LL)		1.86	3.61	6.45
H19	RSB	2.4								
H20	TIN	2.4								
H21	TEB	2.5								
Equivalent Cells		2636		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

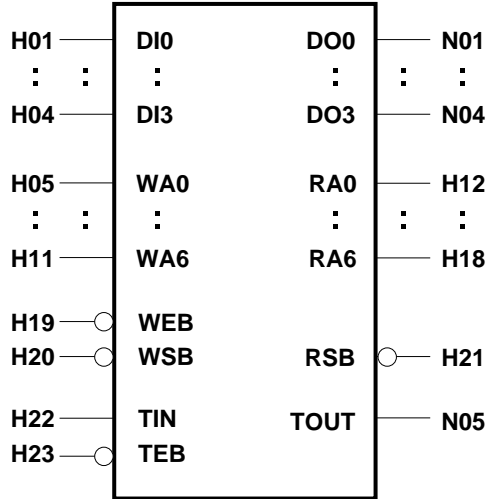
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.80		
Address access time	tACA			7.80
Address output hold time	tOH	2.08		
RSB access time	tREC			2.23
RSB output hold time	tREL	1.04		2.36
RSB output set time	tRLL	0.89		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.60		
WSB-WEB reset time	tCWR	5.54		
Write pulse width	tWP	5.54		
Address setup time	tAS	2.74		
Address hold time	tAH	0.32		
Input data setup time	tDS	3.35		
Input data hold time	tDH	0.42		
WEB access time	tWEC			8.84

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94D	128 words × 4 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN	→	OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7						
:	:	:	:	:	:						
H04	DI3	2.4	N04	DO3	23.7						
H05	WA0	2.4	N05	TOUT	26.0						
:	:	:									
H11	WA6	2.4									
H12	RA0	2.4									
:	:	:									
H18	RA6	2.4									
H19	WEB	2.4									
H20	WSB	1.0									
H21	RSB	1.0									
H22	TIN	2.4									
H23	TEB	2.5									
Equivalent Cells			4052			Power (mW/MHz)		Rev.		1	

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.21		
Address access time	tACA			8.21
Address output hold time	tOH	2.27		
RSB access time	tREC			1.66
RSB output hold time	tREL	0.71		1.65
RSB output set time	tRLL	0.62		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.94		
WSB-WEB reset time	tCWR	5.38		
Write pulse width	tWP	5.38		
Address setup time	tAS	3.34		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.35		
Input data hold time	tDH	0.32		
WEB access time	tWEC			9.08

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																	
R94F	256 words × 4 bits Dual-port RAM																																																																																																																																																																																																																																																		
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1	X	X	X	0	1	Hold	X	X	X	X																																																																																																																																																																																																																																									
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Equivalent Cells		7837	Power (mW/MHz)			Rev.		1																																																																																																																																																																																																																																											

HIGH DENSITY DUAL-PORT RAM BLOCK

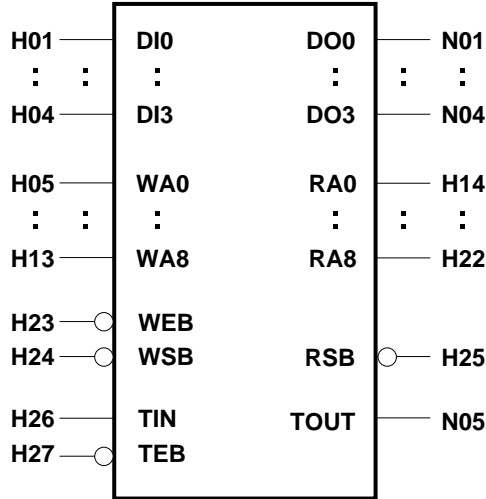
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.55		
Address access time	tACA			8.55
Address output hold time	tOH	2.29		
RSB access time	tREC			2.23
RSB output hold time	tREL	1.05		2.37
RSB output set time	tRLL	0.90		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.01		
WSB-WEB reset time	tCWR	5.44		
Write pulse width	tWP	5.44		
Address setup time	tAS	3.24		
Address hold time	tAH	0.33		
Input data setup time	tDS	3.36		
Input data hold time	tDH	0.43		
WEB access time	tWEC			9.55

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94H	512 words × 4 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7					
:	:	:	:	:	:					
H04	DI3	2.4	N04	DO3	23.7	RA0 to RA8	(LH)	0.68	3.83	8.97
H05	WA0	2.4	N05	TOUT	26.0	→DO0 to DO3	(HH)	0.73	3.86	8.97
:	:	:					(HL)	1.78	4.59	9.17
H13	WA8	2.4					(LL)	1.86	4.64	9.17
H14	RA0	2.4				RSB	(LH)	1.26	1.94	3.05
:	:	:				→DO0 to DO3	(HL)	1.59	2.41	3.75
H22	RA8	2.4								
H23	WEB	2.4				DI0 to DI3	(HH)	2.05	3.88	6.86
H24	WSB	1.0				→DO0 to DO3	(LL)	2.36	4.43	7.80
H25	RSB	1.0								
H26	TIN	2.4								
H27	TEB	2.5								
Equivalent Cells		15343		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.17		
Address access time	tACA			9.17
Address output hold time	tOH	2.30		
RSB access time	tREC			3.62
RSB output hold time	tREL	1.59		3.76
RSB output set time	tRLL	1.26		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	10.06		
WSB-WEB reset time	tCWR	5.56		
Write pulse width	tWP	5.56		
Address setup time	tAS	3.32		
Address hold time	tAH	1.18		
Input data setup time	tDS	3.47		
Input data hold time	tDH	1.28		
WEB access time	tWEC			10.27

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																	
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Equivalent Cells	30396		Power (mW/MHz)		Rev.	1																																																																																																																																																																																																																																																													

HIGH DENSITY DUAL-PORT RAM BLOCK

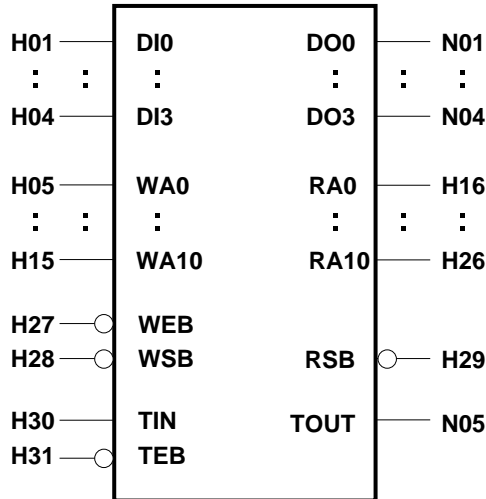
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.51		
Address access time	tACA			9.51
Address output hold time	tOH	2.29		
RSB access time	tREC			3.89
RSB output hold time	tREL	1.63		3.69
RSB output set time	tRLL	1.59		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	10.57		
WSB-WEB reset time	tCWR	5.88		
Write pulse width	tWP	5.88		
Address setup time	tAS	3.47		
Address hold time	tAH	1.22		
Input data setup time	tDS	3.73		
Input data hold time	tDH	1.32		
WEB access time	tWEC			10.53

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R94S	2K words × 4 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	17.7	RA0 to RA10 (LH) →DO0 to DO3 (HH) (HL) (LL)		1.20	4.41	9.65
⋮	⋮	⋮	⋮	⋮	⋮			1.14	4.37	9.65
H04	DI3	2.4	N04	DO3	17.7			2.14	5.07	9.85
H05	WA0	2.4	N05	TOUT	26.0			2.03	5.00	9.85
⋮	⋮	⋮				RSB →DO0 to DO3 (LH) (HL)		1.76	2.67	4.17
H15	WA10	2.4						1.81	2.70	4.16
H16	RA0	2.4				DI0 to DI3 (HH) →DO0 to DO3 (LL)		2.44	4.45	7.72
⋮	⋮	⋮						2.70	5.00	8.74
H26	RA10	2.4								
H27	WEB	2.4								
H28	WSB	2.4								
H29	RSB	2.4								
H30	TIN	2.4								
H31	TEB	2.5								
Equivalent Cells		60537		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.85		
Address access time	tACA			9.85
Address output hold time	tOH	2.08		
RSB access time	tREC			4.17
RSB output hold time	tREL	1.81		4.16
RSB output set time	tRLL	1.76		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	10.81		
WSB-WEB reset time	tCWR	5.93		
Write pulse width	tWP	5.93		
Address setup time	tAS	3.53		
Address hold time	tAH	1.35		
Input data setup time	tDS	3.78		
Input data hold time	tDH	1.45		
WEB access time	tWEC			10.84

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																				
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TYP.	MAX.	H01	DI0	2.4	N01	DO0	17.7							:	:	:	:	:	:							H04	DI3	2.4	N04	DO3	17.7	RA0 to RA11 (LH)		1.40	4.95	10.73	H05	WA0	2.4	N05	TOUT	26.0	→DO0 to DO3 (HH)		1.44	4.97	10.73	:	:	:				(HL)		2.36	5.62	10.93	H16	WA11	2.4				(LL)		2.39	5.64	10.93	H17	RA0	2.4				RSB (LH)		2.14	3.26	5.09	:	:	:				→DO0 to DO3 (HL)		2.26	3.38	5.22	H28	RA11	2.4				DI0 to DI3 (HH)		2.76	4.92	8.44	H29	WEB	2.4				→DO0 to DO3 (LL)		3.05	5.54	9.59	H30	WSB	1.0									H31	RSB	1.0									H32	TIN	2.4									H33	TEB	2.5								
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HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.93		
Address access time	tACA			10.93
Address output hold time	tOH	2.50		
RSB access time	tREC			5.09
RSB output hold time	tREL	2.26		5.23
RSB output set time	tRLL	2.14		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	11.42		
WSB-WEB reset time	tCWR	5.89		
Write pulse width	tWP	5.89		
Address setup time	tAS	3.73		
Address hold time	tAH	1.80		
Input data setup time	tDS	3.78		
Input data hold time	tDH	1.90		
WEB access time	tWEC			11.70

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																						
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0	CLOCK	X	X	X	X	X	X	X	X	RESULT																																																																																																																																																																																																																																																														
Input			Output			Switching speed																																																																																																																																																																																																																																																																		
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)																																																																																																																																																																																																																																																																
						IN	→ OUT	MIN.	TYP.	MAX.																																																																																																																																																																																																																																																														
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA3 →DO0 to DO7	(LH)	1.30	3.50	7.10																																																																																																																																																																																																																																																														
⋮	⋮	⋮	⋮	⋮	⋮		(HH)	1.30	3.50	7.10																																																																																																																																																																																																																																																														
H08	DI7	2.4	N08	DO7	23.7		(HL)	2.21	4.14	7.30																																																																																																																																																																																																																																																														
H09	WA0	2.4	N09	TOUT	26.0		(LL)	2.22	4.15	7.30																																																																																																																																																																																																																																																														
⋮	⋮	⋮	⋮	⋮	⋮	RSB →DO0 to DO7	(LH)	0.64	1.04	1.69																																																																																																																																																																																																																																																														
H12	WA3	2.4	⋮	⋮	⋮		(HL)	0.72	1.08	1.68																																																																																																																																																																																																																																																														
H13	RA0	2.4	⋮	⋮	⋮	DI0 to DI7 →DO0 to DO7	(HH)	1.47	2.98	5.44																																																																																																																																																																																																																																																														
⋮	⋮	⋮	⋮	⋮	⋮		(LL)	1.56	3.13	5.69																																																																																																																																																																																																																																																														
H16	RA3	2.4	⋮	⋮	⋮																																																																																																																																																																																																																																																																			
H17	WEB	2.4	⋮	⋮	⋮																																																																																																																																																																																																																																																																			
H18	WSB	1.0	⋮	⋮	⋮																																																																																																																																																																																																																																																																			
H19	RSB	1.0	⋮	⋮	⋮																																																																																																																																																																																																																																																																			
H20	TIN	2.4	⋮	⋮	⋮																																																																																																																																																																																																																																																																			
H21	TEB	2.5	⋮	⋮	⋮																																																																																																																																																																																																																																																																			
Equivalent Cells	1554		Power (mW/MHz)				Rev.		1																																																																																																																																																																																																																																																															

HIGH DENSITY DUAL-PORT RAM BLOCK

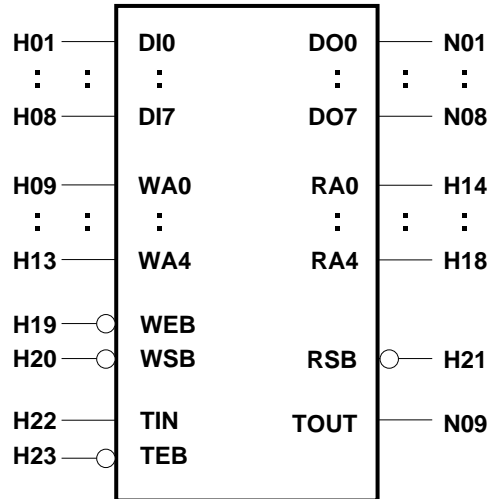
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.30		
Address access time	tACA			7.30
Address output hold time	tOH	1.92		
RSB access time	tREC			1.70
RSB output hold time	tREL	0.73		1.69
RSB output set time	tRLL	0.64		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.22		
WSB-WEB reset time	tCWR	5.14		
Write pulse width	tWP	5.14		
Address setup time	tAS	2.86		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.29		
Input data hold time	tDH	0.36		
WEB access time	tWEC			8.34

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R989	32 words × 8 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)	
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA4 (LH)	1.40	3.64	7.30
:	:	:	:	:	:	→DO0 to DO7 (HH)	1.40	3.64	7.30
H08	DI7	2.4	N08	DO7	23.7	(HL)	2.31	4.28	7.50
H09	WA0	2.4	N09	TOUT	26.0	(LL)	2.32	4.29	7.50
:	:	:				RSB (LH)	0.65	1.05	1.70
H13	WA4	2.4				→DO0 to DO7 (HL)	0.73	1.09	1.69
H14	RA0	2.4				DI0 to DI7 (HH)	1.48	3.02	5.54
:	:	:				→DO0 to DO7 (LL)	1.57	3.18	5.79
H18	RA4	2.4							
H19	WEB	2.4							
H20	WSB	1.0							
H21	RSB	1.0							
H22	TIN	2.4							
H23	TEB	2.5							
Equivalent Cells		2632		Power (mW/MHz)		Rev.		1	

HIGH DENSITY DUAL-PORT RAM BLOCK

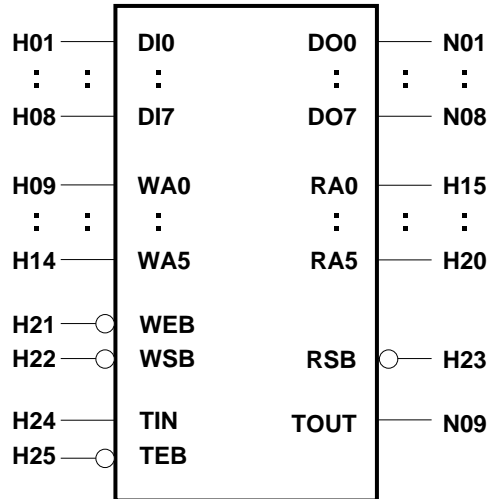
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.50		
Address access time	tACA			7.50
Address output hold time	tOH	2.01		
RSB access time	tREC			1.71
RSB output hold time	tREL	0.73		1.70
RSB output set time	tRLL	0.65		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.64		
WSB-WEB reset time	tCWR	5.54		
Write pulse width	tWP	5.54		
Address setup time	tAS	2.87		
Address hold time	tAH	0.23		
Input data setup time	tDS	3.30		
Input data hold time	tDH	0.37		
WEB access time	tWEC			8.44

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R98B	64 words × 8 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA5 →DO0 to DO7	(LH)	1.56	3.87	7.64
:	:	:	:	:	:		(HH)	1.56	3.87	7.64
H08	DI7	2.4	N08	DO7	23.7		(HL)	2.47	4.51	7.84
H09	WA0	2.4	N09	TOUT	26.0		(LL)	2.47	4.51	7.84
:	:	:								
H14	WA5	2.4				RSB →DO0 to DO7	(LH)	0.65	1.06	1.72
H15	RA0	2.4					(HL)	0.75	1.12	1.72
:	:	:				DI0 to DI7 →DO0 to DO7	(HH)	1.61	3.23	5.88
H20	RA5	2.4					(LL)	1.69	3.38	6.12
H21	WEB	2.4								
H22	WSB	1.0								
H23	RSB	1.0								
H24	TIN	2.4								
H25	TEB	2.5								
Equivalent Cells		3446		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.84		
Address access time	tACA			7.84
Address output hold time	tOH	2.17		
RSB access time	tREC			1.73
RSB output hold time	tREL	0.75		1.73
RSB output set time	tRLL	0.65		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.94		
WSB-WEB reset time	tCWR	5.38		
Write pulse width	tWP	5.38		
Address setup time	tAS	2.34		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.25		
Input data hold time	tDH	0.32		
WEB access time	tWEC			8.81

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																	
R98D	128 words × 8 bits Dual-port RAM																																																																																																																																																																																																																																																																																		
<p>Logic Diagram</p> <div style="text-align: center; margin: 20px 0;"> </div>																																																																																																																																																																																																																																																																																			
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H24	WSB	2.4				DI0 to DI7 (HH)		1.81	3.52	6.30																																																																																																																																																																																																																																																																									
H25	RSB	2.4				→DO0 to DO7 (LL)		1.99	3.82	6.79																																																																																																																																																																																																																																																																									
H26	TIN	2.4																																																																																																																																																																																																																																																																																	
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Equivalent Cells		6613	Power (mW/MHz)			Rev.		1																																																																																																																																																																																																																																																																											

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.18		
Address access time	tACA			8.18
Address output hold time	tOH	2.17		
RSB access time	tREC			2.25
RSB output hold time	tREL	1.09		2.45
RSB output set time	tRLL	0.93		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.00		
WSB-WEB reset time	tCWR	5.43		
Write pulse width	tWP	5.43		
Address setup time	tAS	2.24		
Address hold time	tAH	0.33		
Input data setup time	tDS	3.26		
Input data hold time	tDH	0.43		
WEB access time	tWEC			9.28

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																					
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HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.18		
Address access time	tACA			9.18
Address output hold time	tOH	2.57		
RSB access time	tREC			1.75
RSB output hold time	tREL	0.80		1.83
RSB output set time	tRLL	0.67		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.78		
WSB-WEB reset time	tCWR	5.62		
Write pulse width	tWP	5.62		
Address setup time	tAS	3.94		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.45		
Input data hold time	tDH	0.42		
WEB access time	tWEC			10.10

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																									
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HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.52		
Address access time	tACA			9.52
Address output hold time	tOH	2.57		
RSB access time	tREC			2.41
RSB output hold time	tREL	1.12		2.55
RSB output set time	tRLL	0.97		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.87		
WSB-WEB reset time	tCWR	5.68		
Write pulse width	tWP	5.68		
Address setup time	tAS	3.85		
Address hold time	tAH	0.34		
Input data setup time	tDS	3.46		
Input data hold time	tDH	0.54		
WEB access time	tWEC			10.57

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																																																																																											
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TYP.	MAX.	H01	DI0	2.4	N01	DO0	23.7					:	:	:	:	:	:					H08	DI7	2.4	N08	DO7	23.7					H09	WA0	2.4	N09	TOUT	26.0					:	:	:								H18	WA9	2.4								H19	RA0	2.4								:	:	:								H28	RA9	2.4								H29	WEB	2.4								H30	WSB	1.0								H31	RSB	1.0								H32	TIN	2.4								H33	TEB	2.5														RA0 to RA9 (LH)		4.28	7.23	12.03							→DO0 to DO7 (HH)		4.28	7.23	12.03							(HL)		4.14	7.21	12.23							(LL)		4.14	7.21	12.23							RSB (LH)		0.74	1.17	1.87							→DO0 to DO7 (HL)		0.90	1.31	2.00							DI0 to DI7 (HH)		4.15	6.99	11.63							→DO0 to DO7 (LL)		3.74	6.75	11.66
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H09	WA0	2.4	N09	TOUT	26.0																																																																																																																																																																																																																																																																																																																																																								
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H28	RA9	2.4																																																																																																																																																																																																																																																																																																																																																											
H29	WEB	2.4																																																																																																																																																																																																																																																																																																																																																											
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H33	TEB	2.5																																																																																																																																																																																																																																																																																																																																																											
						RA0 to RA9 (LH)		4.28	7.23	12.03																																																																																																																																																																																																																																																																																																																																																			
						→DO0 to DO7 (HH)		4.28	7.23	12.03																																																																																																																																																																																																																																																																																																																																																			
						(HL)		4.14	7.21	12.23																																																																																																																																																																																																																																																																																																																																																			
						(LL)		4.14	7.21	12.23																																																																																																																																																																																																																																																																																																																																																			
						RSB (LH)		0.74	1.17	1.87																																																																																																																																																																																																																																																																																																																																																			
						→DO0 to DO7 (HL)		0.90	1.31	2.00																																																																																																																																																																																																																																																																																																																																																			
						DI0 to DI7 (HH)		4.15	6.99	11.63																																																																																																																																																																																																																																																																																																																																																			
						→DO0 to DO7 (LL)		3.74	6.75	11.66																																																																																																																																																																																																																																																																																																																																																			
Equivalent Cells		37239		Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																																																																																																																					

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.23		
Address access time	tACA			12.23
Address output hold time	tOH	3.84		
RSB access time	tREC			1.87
RSB output hold time	tREL	0.90		2.00
RSB output set time	tRLL	0.74		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	12.74		
WSB-WEB reset time	tCWR	6.58		
Write pulse width	tWP	6.58		
Address setup time	tAS	5.94		
Address hold time	tAH	0.22		
Input data setup time	tDS	4.05		
Input data hold time	tDH	0.52		
WEB access time	tWEC			14.40

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																													
R98S	2K words × 8 bits Dual-port RAM																																																																																																																																																																																																																																																														
<p>Logic Diagram</p> <div style="text-align: center; margin: 20px 0;"> </div>																																																																																																																																																																																																																																																															
<p>Truth Table</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>TEB</th> <th>TIN</th> <th>DIn</th> <th>WAn</th> <th>WSB</th> <th>WEB</th> <th>DMn</th> <th>RAn</th> <th>RSB</th> <th>DOn</th> <th>TOUT</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>DMn</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>0</td> <td>CLOCK</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>RESULT</td> </tr> </tbody> </table> <p>Caution WEB or WSB must be high during all address transition.</p> <p>X : Irrelevant WSB : A-port select RAn : B-port address (Read) DIn : Input data WEB : Write enable RSB : B-port select WAn : A-port address (Write) DMn : Memory data DOn : Output data</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="3">Input</th> <th colspan="3">Output</th> <th colspan="4">Switching speed</th> </tr> <tr> <th>Name</th> <th>Symbol</th> <th>Fan-in</th> <th>Name</th> <th>Symbol</th> <th>Fan-out</th> <th colspan="2">Path</th> <th colspan="2">t_{LD0} (ns)</th> </tr> <tr> <th colspan="6"></th> <th>IN → OUT</th> <th>MIN.</th> <th>TYP.</th> <th>MAX.</th> </tr> </thead> <tbody> <tr> <td>H01</td> <td>DI0</td> <td>2.4</td> <td>N01</td> <td>DO0</td> <td>24.7</td> <td rowspan="4">RA0 to RA10 (LH) →DO0 to DO7 (HH) (HL) (LL)</td> <td>0.66</td> <td>5.12</td> <td>12.40</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>0.59</td> <td>5.08</td> <td>12.40</td> </tr> <tr> <td>H08</td> <td>DI7</td> <td>2.4</td> <td>N08</td> <td>DO7</td> <td>24.7</td> <td>1.67</td> <td>5.82</td> <td>12.60</td> </tr> <tr> <td>H09</td> <td>WA0</td> <td>2.4</td> <td>N09</td> <td>TOUT</td> <td>26.0</td> <td>1.61</td> <td>5.79</td> <td>12.60</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td rowspan="2">RSB →DO0 to DO7 (LH) (HL)</td> <td>1.06</td> <td>1.58</td> <td>2.44</td> </tr> <tr> <td>H19</td> <td>WA10</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>1.23</td> <td>1.80</td> <td>2.73</td> </tr> <tr> <td>H20</td> <td>RA0</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td rowspan="2">DI0 to DI7 (HH) →DO0 to DO7 (LL)</td> <td>4.36</td> <td>7.29</td> <td>12.07</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>4.05</td> <td>7.22</td> <td>12.38</td> </tr> <tr> <td>H30</td> <td>RA10</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H31</td> <td>WEB</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H32</td> <td>WSB</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H33</td> <td>RSB</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H34</td> <td>TIN</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H35</td> <td>TEB</td> <td>2.5</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> </tbody> </table>			TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	1	X	X	X	1	X	Hold	X	X	X	X	1	X	X	X	0	1	Hold	X	X	X	X	1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X	1	X	X	X	X	X	X	X	1	0	X	1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X	1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X	0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Input			Output			Switching speed				Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)								IN → OUT	MIN.	TYP.	MAX.	H01	DI0	2.4	N01	DO0	24.7	RA0 to RA10 (LH) →DO0 to DO7 (HH) (HL) (LL)	0.66	5.12	12.40	⋮	⋮	⋮	⋮	⋮	⋮	0.59	5.08	12.40	H08	DI7	2.4	N08	DO7	24.7	1.67	5.82	12.60	H09	WA0	2.4	N09	TOUT	26.0	1.61	5.79	12.60	⋮	⋮	⋮	⋮	⋮	⋮	RSB →DO0 to DO7 (LH) (HL)	1.06	1.58	2.44	H19	WA10	2.4	⋮	⋮	⋮	1.23	1.80	2.73	H20	RA0	2.4	⋮	⋮	⋮	DI0 to DI7 (HH) →DO0 to DO7 (LL)	4.36	7.29	12.07	⋮	⋮	⋮	⋮	⋮	⋮	4.05	7.22	12.38	H30	RA10	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H31	WEB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H32	WSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H33	RSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H34	TIN	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H35	TEB	2.5	⋮	⋮	⋮	⋮	⋮	⋮	⋮
TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT																																																																																																																																																																																																																																																					
1	X	X	X	1	X	Hold	X	X	X	X																																																																																																																																																																																																																																																					
1	X	X	X	0	1	Hold	X	X	X	X																																																																																																																																																																																																																																																					
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X																																																																																																																																																																																																																																																					
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1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																					
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																					
0	CLOCK	X	X	X	X	X	X	X	X	RESULT																																																																																																																																																																																																																																																					
Input			Output			Switching speed																																																																																																																																																																																																																																																									
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)																																																																																																																																																																																																																																																							
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H01	DI0	2.4	N01	DO0	24.7	RA0 to RA10 (LH) →DO0 to DO7 (HH) (HL) (LL)	0.66	5.12	12.40																																																																																																																																																																																																																																																						
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H08	DI7	2.4	N08	DO7	24.7		1.67	5.82	12.60																																																																																																																																																																																																																																																						
H09	WA0	2.4	N09	TOUT	26.0		1.61	5.79	12.60																																																																																																																																																																																																																																																						
⋮	⋮	⋮	⋮	⋮	⋮	RSB →DO0 to DO7 (LH) (HL)	1.06	1.58	2.44																																																																																																																																																																																																																																																						
H19	WA10	2.4	⋮	⋮	⋮		1.23	1.80	2.73																																																																																																																																																																																																																																																						
H20	RA0	2.4	⋮	⋮	⋮	DI0 to DI7 (HH) →DO0 to DO7 (LL)	4.36	7.29	12.07																																																																																																																																																																																																																																																						
⋮	⋮	⋮	⋮	⋮	⋮		4.05	7.22	12.38																																																																																																																																																																																																																																																						
H30	RA10	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H31	WEB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H32	WSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H33	RSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
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H35	TEB	2.5	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
Equivalent Cells	74136		Power (mW/MHz)		Rev.	1																																																																																																																																																																																																																																																									

HIGH DENSITY DUAL-PORT RAM BLOCK

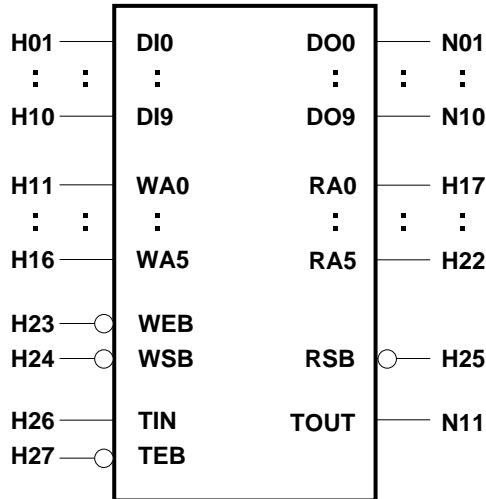
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.60		
Address access time	tACA			12.60
Address output hold time	tOH	1.55		
RSB access time	tREC			2.60
RSB output hold time	tREL	1.23		2.74
RSB output set time	tRLL	1.06		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	12.87		
WSB-WEB reset time	tCWR	6.66		
Write pulse width	tWP	6.66		
Address setup time	tAS	5.86		
Address hold time	tAH	0.35		
Input data setup time	tDS	4.08		
Input data hold time	tDH	0.65		
WEB access time	tWEC			14.90

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AB	64 words × 10 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7					
:	:	:	:	:	:					
H10	DI9	2.4	N10	DO9	23.7	RA0 to RA5 (LH)		1.56	3.88	7.67
H11	WA0	2.4	N11	TOUT	26.0	→DO0 to DO9 (HH)		1.56	3.88	7.67
:	:	:				(HL)		2.49	4.53	7.87
H16	WA5	2.4				(LL)		2.49	4.53	7.87
H17	RA0	2.4				RSB (LH)		0.66	1.07	1.75
:	:	:				→DO0 to DO9 (HL)		0.77	1.14	1.76
H22	RA5	2.4								
H23	WEB	2.4				DI0 to DI9 (HH)		1.60	3.23	5.88
H24	WSB	1.0				→DO0 to DO9 (LL)		1.69	3.38	6.13
H25	RSB	1.0								
H26	TIN	2.4								
H27	TEB	2.5								
Equivalent Cells		4187		Power (mW/MHz)				Rev.		1

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.87		
Address access time	tACA			7.87
Address output hold time	tOH	2.18		
RSB access time	tREC			1.76
RSB output hold time	tREL	0.77		1.77
RSB output set time	tRLL	0.66		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.04		
WSB-WEB reset time	tCWR	5.38		
Write pulse width	tWP	5.38		
Address setup time	tAS	2.44		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.25		
Input data hold time	tDH	0.32		
WEB access time	tWEC			8.85

HIGH DENSITY DUAL-PORT RAM BLOCK

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TYP.	MAX.	H01	DI0	2.4	N01	DO0	24.7							:	:	:	:	:	:							H10	DI9	2.4	N10	DO9	24.7	RA0 to RA6		(LH)	0.57	3.40	8.02	H11	WA0	2.4	N11	TOUT	26.0	→DO0 to DO9		(HH)	0.49	3.35	8.02	:	:	:						(HL)	1.58	4.10	8.22	H17	WA6	2.4						(LL)	1.51	4.06	8.22	H18	RA0	2.4				RSB		(LH)	0.94	1.44	2.27	:	:	:				→DO0 to DO9		(HL)	1.11	1.63	2.49	H24	RA6	2.4				DI0 to DI9		(HH)	1.80	3.51	6.30	H25	WEB	2.4				→DO0 to DO9		(LL)	1.99	3.82	6.80	H26	WSB	2.4										H27	RSB	2.4										H28	TIN	2.4										H29	TEB	2.5									
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HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.22		
Address access time	tACA			8.22
Address output hold time	tOH	2.19		
RSB access time	tREC			2.35
RSB output hold time	tREL	1.11		2.49
RSB output set time	tRLL	0.94		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.60		
WSB-WEB reset time	tCWR	5.44		
Write pulse width	tWP	5.44		
Address setup time	tAS	3.94		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.45		
Input data hold time	tDH	0.42		
WEB access time	tWEC			10.16

HIGH DENSITY DUAL-PORT RAM BLOCK

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TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT																																																																																																																																																																																																																																																																									
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1	X	X	X	0	1	Hold	X	X	X	X																																																																																																																																																																																																																																																																									
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X																																																																																																																																																																																																																																																																									
1	X	X	X	X	X	X	X	1	0	X																																																																																																																																																																																																																																																																									
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																																									
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																																									
0	CLOCK	X	X	X	X	X	X	X	X	RESULT																																																																																																																																																																																																																																																																									
Input			Output			Switching speed																																																																																																																																																																																																																																																																													
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)																																																																																																																																																																																																																																																																											
						IN	→ OUT	MIN.	TYP.	MAX.																																																																																																																																																																																																																																																																									
H01	DI0	2.4	N01	DO0	23.7																																																																																																																																																																																																																																																																														
:	:	:	:	:	:																																																																																																																																																																																																																																																																														
H10	DI9	2.4	N10	DO9	23.7	RA0 to RA7 (LH)		2.17	4.76	8.99																																																																																																																																																																																																																																																																									
H11	WA0	2.4	N11	TOUT	26.0	→DO0 to DO9 (HH)		2.17	4.76	8.99																																																																																																																																																																																																																																																																									
:	:	:				(HL)		2.91	5.30	9.19																																																																																																																																																																																																																																																																									
H18	WA7	2.4				(LL)		2.91	5.30	9.19																																																																																																																																																																																																																																																																									
H19	RA0	2.4				RSB (LH)		0.69	1.11	1.79																																																																																																																																																																																																																																																																									
:	:	:				→DO0 to DO9 (HL)		0.84	1.24	1.90																																																																																																																																																																																																																																																																									
H26	RA7	2.4																																																																																																																																																																																																																																																																																	
H27	WEB	2.4																																																																																																																																																																																																																																																																																	
H28	WSB	1.0				DI0 to DI9 (HH)		2.14	4.09	7.27																																																																																																																																																																																																																																																																									
H29	RSB	1.0				→DO0 to DO9 (LL)		2.06	3.99	7.14																																																																																																																																																																																																																																																																									
H30	TIN	2.4																																																																																																																																																																																																																																																																																	
H31	TEB	2.5																																																																																																																																																																																																																																																																																	
Equivalent Cells	12791		Power (mW/MHz)			Rev.	1																																																																																																																																																																																																																																																																												

HIGH DENSITY DUAL-PORT RAM BLOCK

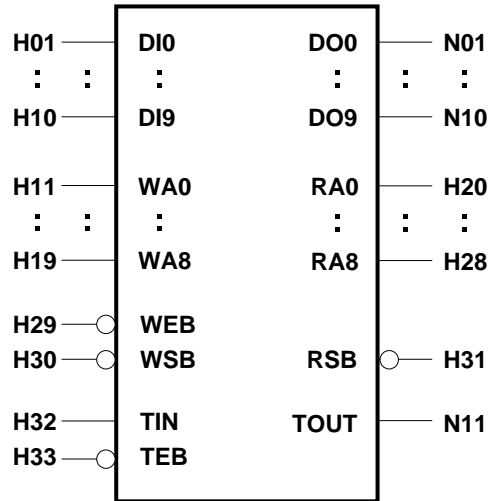
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.19		
Address access time	tACA			9.19
Address output hold time	tOH	2.61		
RSB access time	tREC			1.80
RSB output hold time	tREL	1.11		1.90
RSB output set time	tRLL	0.69		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.78		
WSB-WEB reset time	tCWR	5.62		
Write pulse width	tWP	5.62		
Address setup time	tAS	3.94		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.45		
Input data hold time	tDH	0.42		
WEB access time	tWEC			10.16

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AH	512 words × 10 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7	RA0 to RA8 →DO0 to DO9	(LH)	0.62	3.93	9.34
⋮	⋮	⋮	⋮	⋮	⋮		(HH)	0.53	3.88	9.34
H10	DI9	2.4	N10	DO9	24.7		(HL)	1.62	4.63	9.54
H11	WA0	2.4	N11	TOUT	26.0		(LL)	1.56	4.59	9.54
H19	WA8	2.4				RSB →DO0 to DO9	(LH)	0.99	1.51	2.35
H20	RA0	2.4					(HL)	1.16	1.71	2.61
H28	RA8	2.4				DI0 to DI9 →DO0 to DO9	(HH)	2.34	4.37	7.69
H29	WEB	2.4					(LL)	2.37	4.45	7.83
H30	WSB	2.4								
H31	RSB	2.4								
H32	TIN	2.4								
H33	TEB	2.5								
Equivalent Cells		25244		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

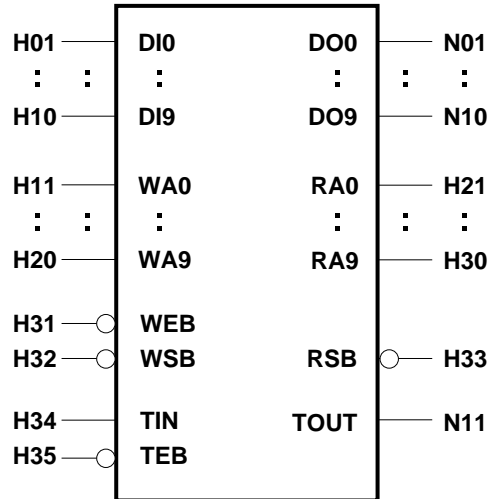
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.54		
Address access time	tACA			9.54
Address output hold time	tOH	2.61		
RSB access time	tREC			2.48
RSB output hold time	tREL	1.16		2.62
RSB output set time	tRLL	0.99		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.88		
WSB-WEB reset time	tCWR	5.69		
Write pulse width	tWP	5.69		
Address setup time	tAS	3.85		
Address hold time	tAH	0.34		
Input data setup time	tDS	3.47		
Input data hold time	tDH	0.54		
WEB access time	tWEC			10.64

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9AM	1K words × 10 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7					
:	:	:	:	:	:					
H10	DI9	2.4	N10	DO9	23.7	RA0 to RA9	(LH)	4.39	7.29	12.03
H11	WA0	2.4	N11	TOUT	26.0	→DO0 to DO9	(HH)	4.39	7.29	12.03
:	:	:					(HL)	4.18	7.24	12.23
H20	WA9	2.4					(LL)	4.18	7.24	12.23
H21	RA0	2.4				RSB	(LH)	0.79	1.22	1.93
:	:	:				→DO0 to DO9	(HL)	0.94	1.37	2.09
H30	RA9	2.4								
H31	WEB	2.4				DI0 to DI9	(HH)	4.15	6.99	11.63
H32	WSB	1.0				→DO0 to DO9	(LL)	3.74	6.75	11.66
H33	RSB	1.0								
H34	TIN	2.4								
H35	TEB	2.5								
Equivalent Cells		46281		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.23		
Address access time	tACA			12.23
Address output hold time	tOH	3.88		
RSB access time	tREC			1.95
RSB output hold time	tREL	0.94		2.09
RSB output set time	tRLL	0.79		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	13.08		
WSB-WEB reset time	tCWR	6.82		
Write pulse width	tWP	6.82		
Address setup time	tAS	6.04		
Address hold time	tAH	0.22		
Input data setup time	tDS	3.85		
Input data hold time	tDH	0.52		
WEB access time	tWEC			14.40

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																													
R9AS	2K words × 10 bits Dual-port RAM																																																																																																																																																																																																																																																														
<p>Logic Diagram</p> <div style="text-align: center; margin: 20px 0;"> </div>																																																																																																																																																																																																																																																															
<p>Truth Table</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>TEB</th> <th>TIN</th> <th>DIn</th> <th>WAn</th> <th>WSB</th> <th>WEB</th> <th>DMn</th> <th>RAn</th> <th>RSB</th> <th>DOn</th> <th>TOUT</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>DMn</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>0</td> <td>CLOCK</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>RESULT</td> </tr> </tbody> </table> <p>Caution WEB or WSB must be high during all address transition.</p> <p>X : Irrelevant WSB : A-port select RAn : B-port address (Read) DIn : Input data WEB : Write enable RSB : B-port select WAn : A-port address (Write) DMn : Memory data DOn : Output data</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="3">Input</th> <th colspan="3">Output</th> <th colspan="4">Switching speed</th> </tr> <tr> <th>Name</th> <th>Symbol</th> <th>Fan-in</th> <th>Name</th> <th>Symbol</th> <th>Fan-out</th> <th colspan="2">Path</th> <th colspan="2">t_{LD0} (ns)</th> </tr> <tr> <th colspan="6"></th> <th>IN → OUT</th> <th>MIN.</th> <th>TYP.</th> <th>MAX.</th> </tr> </thead> <tbody> <tr> <td>H01</td> <td>DI0</td> <td>2.4</td> <td>N01</td> <td>DO0</td> <td>24.7</td> <td rowspan="4">RA0 to RA10 (HH) →DO0 to DO9 (LH) (LL) (HL)</td> <td>0.72</td> <td>5.16</td> <td>12.40</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>0.64</td> <td>5.11</td> <td>12.40</td> </tr> <tr> <td>H10</td> <td>DI9</td> <td>2.4</td> <td>N10</td> <td>DO9</td> <td>24.7</td> <td>1.70</td> <td>5.84</td> <td>12.60</td> </tr> <tr> <td>H11</td> <td>WA0</td> <td>2.4</td> <td>N11</td> <td>TOUT</td> <td>26.0</td> <td>1.65</td> <td>5.81</td> <td>12.60</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td rowspan="2">RSB →DO0 to DO9 (LH) (HL)</td> <td>1.12</td> <td>1.65</td> <td>2.51</td> </tr> <tr> <td>H21</td> <td>WA10</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>1.27</td> <td>1.86</td> <td>2.84</td> </tr> <tr> <td>H22</td> <td>RA0</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td rowspan="2">DI0 to DI9 (HH) →DO0 to DO9 (LL)</td> <td>4.37</td> <td>7.29</td> <td>12.07</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>4.05</td> <td>7.22</td> <td>12.38</td> </tr> <tr> <td>H32</td> <td>RA10</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H33</td> <td>WEB</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H34</td> <td>WSB</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H35</td> <td>RSB</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H36</td> <td>TIN</td> <td>2.4</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> <tr> <td>H37</td> <td>TEB</td> <td>2.5</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> </tr> </tbody> </table>			TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	1	X	X	X	1	X	Hold	X	X	X	X	1	X	X	X	0	1	Hold	X	X	X	X	1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X	1	X	X	X	X	X	X	X	1	0	X	1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X	1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X	0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Input			Output			Switching speed				Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)								IN → OUT	MIN.	TYP.	MAX.	H01	DI0	2.4	N01	DO0	24.7	RA0 to RA10 (HH) →DO0 to DO9 (LH) (LL) (HL)	0.72	5.16	12.40	⋮	⋮	⋮	⋮	⋮	⋮	0.64	5.11	12.40	H10	DI9	2.4	N10	DO9	24.7	1.70	5.84	12.60	H11	WA0	2.4	N11	TOUT	26.0	1.65	5.81	12.60	⋮	⋮	⋮	⋮	⋮	⋮	RSB →DO0 to DO9 (LH) (HL)	1.12	1.65	2.51	H21	WA10	2.4	⋮	⋮	⋮	1.27	1.86	2.84	H22	RA0	2.4	⋮	⋮	⋮	DI0 to DI9 (HH) →DO0 to DO9 (LL)	4.37	7.29	12.07	⋮	⋮	⋮	⋮	⋮	⋮	4.05	7.22	12.38	H32	RA10	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H33	WEB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H34	WSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H35	RSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H36	TIN	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮	H37	TEB	2.5	⋮	⋮	⋮	⋮	⋮	⋮	⋮
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1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																					
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⋮	⋮	⋮	⋮	⋮	⋮		0.64	5.11	12.40																																																																																																																																																																																																																																																						
H10	DI9	2.4	N10	DO9	24.7		1.70	5.84	12.60																																																																																																																																																																																																																																																						
H11	WA0	2.4	N11	TOUT	26.0		1.65	5.81	12.60																																																																																																																																																																																																																																																						
⋮	⋮	⋮	⋮	⋮	⋮	RSB →DO0 to DO9 (LH) (HL)	1.12	1.65	2.51																																																																																																																																																																																																																																																						
H21	WA10	2.4	⋮	⋮	⋮		1.27	1.86	2.84																																																																																																																																																																																																																																																						
H22	RA0	2.4	⋮	⋮	⋮	DI0 to DI9 (HH) →DO0 to DO9 (LL)	4.37	7.29	12.07																																																																																																																																																																																																																																																						
⋮	⋮	⋮	⋮	⋮	⋮		4.05	7.22	12.38																																																																																																																																																																																																																																																						
H32	RA10	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H33	WEB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H34	WSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H35	RSB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H36	TIN	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
H37	TEB	2.5	⋮	⋮	⋮	⋮	⋮	⋮	⋮																																																																																																																																																																																																																																																						
Equivalent Cells	92206		Power (mW/MHz)		Rev.	1																																																																																																																																																																																																																																																									

HIGH DENSITY DUAL-PORT RAM BLOCK

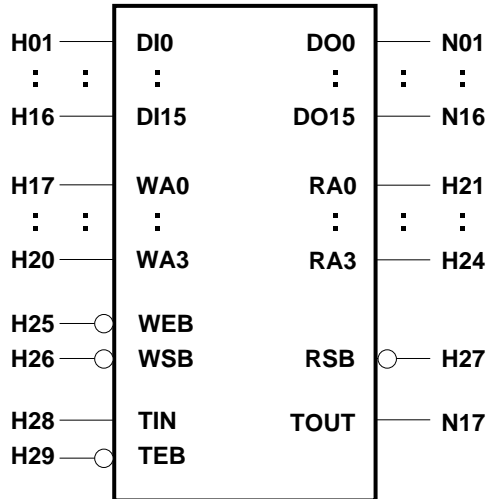
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.60		
Address access time	tACA			12.60
Address output hold time	tOH	1.60		
RSB access time	tREC			2.70
RSB output hold time	tREL	1.27		2.84
RSB output set time	tRLL	1.12		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	13.22		
WSB-WEB reset time	tCWR	6.90		
Write pulse width	tWP	6.90		
Address setup time	tAS	5.96		
Address hold time	tAH	0.36		
Input data setup time	tDS	3.88		
Input data hold time	tDH	0.66		
WEB access time	tWEC			15.14

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9C7	16 words × 16 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed									
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)							
						IN → OUT		MIN.	TYP.	MAX.					
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA3 (LH) →DO0 to DO15 (HH)		1.36	3.59	7.22					
:	:	:	:	:	:										
H16	DI15	2.4	N16	DO15	23.7						(HL)		2.25	4.21	7.42
H17	WA0	2.4	N17	TOUT	26.0										
:	:	:				RSB (LH) →DO0 to DO15 (HL)		0.69	1.10	1.78					
H20	WA3	2.4									(HL)		0.78	1.16	1.79
H21	RA0	2.4				DI0 to DI15 (HH) →DO0 to DO15 (LL)		1.47	2.98	5.45					
:	:	:									(LL)		1.56	3.14	5.70
H24	RA3	2.4													
H25	WEB	2.4													
H26	WSB	1.0													
H27	RSB	1.0													
H28	TIN	2.4													
H29	TEB	2.5													
Equivalent Cells		2902		Power (mW/MHz)				Rev.		1					

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.42		
Address access time	tACA			7.42
Address output hold time	tOH	1.95		
RSB access time	tREC			1.79
RSB output hold time	tREL	0.78		1.79
RSB output set time	tRLL	0.69		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.50		
WSB-WEB reset time	tCWR	5.26		
Write pulse width	tWP	5.26		
Address setup time	tAS	2.97		
Address hold time	tAH	0.27		
Input data setup time	tDS	3.21		
Input data hold time	tDH	0.49		
WEB access time	tWEC			8.59

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																													
R9C9	32 words × 16 bits Dual-port RAM																																																																																																																																																																																																																																																														
<p>Logic Diagram</p> <div style="text-align: center; margin: 20px 0;"> </div>																																																																																																																																																																																																																																																															
<p>Truth Table</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>TEB</th> <th>TIN</th> <th>DIn</th> <th>WAn</th> <th>WSB</th> <th>WEB</th> <th>DMn</th> <th>RAn</th> <th>RSB</th> <th>DOn</th> <th>TOUT</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>DMn</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>0</td> <td>CLOCK</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>RESULT</td> </tr> </tbody> </table> <p>Caution WEB or WSB must be high during all address transition.</p> <p>X : Irrelevant WSB : A-port select RAn : B-port address (Read) DIn : Input data WEB : Write enable RSB : B-port select WAn : A-port address (Write) DMn : Memory data DOn : Output data</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="3">Input</th> <th colspan="3">Output</th> <th colspan="4">Switching speed</th> </tr> <tr> <th>Name</th> <th>Symbol</th> <th>Fan-in</th> <th>Name</th> <th>Symbol</th> <th>Fan-out</th> <th colspan="2">Path</th> <th colspan="2">t_{LD0} (ns)</th> </tr> <tr> <th colspan="6"></th> <th>IN → OUT</th> <th>MIN.</th> <th>TYP.</th> <th>MAX.</th> </tr> </thead> <tbody> <tr> <td>H01</td> <td>DI0</td> <td>2.4</td> <td>N01</td> <td>DO0</td> <td>23.7</td> <td rowspan="4">RA0 to RA4 (LH) →DO0 to DO15 (HH) (HL) (LL)</td> <td>1.46</td> <td>3.72</td> <td>7.42</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>1.44</td> <td>3.71</td> <td>7.42</td> </tr> <tr> <td>H16</td> <td>DI15</td> <td>2.4</td> <td>N16</td> <td>DO15</td> <td>23.7</td> <td>2.35</td> <td>4.35</td> <td>7.62</td> </tr> <tr> <td>H17</td> <td>WA0</td> <td>2.4</td> <td>N17</td> <td>TOUT</td> <td>26.0</td> <td>2.38</td> <td>4.37</td> <td>7.62</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td rowspan="2">RSB →DO0 to DO15 (HL)</td> <td>0.70</td> <td>1.11</td> <td>1.79</td> </tr> <tr> <td>H21</td> <td>WA4</td> <td>2.4</td> <td></td> <td></td> <td></td> <td>0.79</td> <td>1.17</td> <td>1.80</td> </tr> <tr> <td>H22</td> <td>RA0</td> <td>2.4</td> <td></td> <td></td> <td></td> <td rowspan="2">DI0 to DI15 (HH) →DO0 to DO15 (LL)</td> <td>1.48</td> <td>3.03</td> <td>5.55</td> </tr> <tr> <td>⋮</td> <td>⋮</td> <td>⋮</td> <td></td> <td></td> <td></td> <td>1.57</td> <td>3.18</td> <td>5.80</td> </tr> <tr> <td>H26</td> <td>RA4</td> <td>2.4</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H27</td> <td>WEB</td> <td>2.4</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H28</td> <td>WSB</td> <td>1.0</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H29</td> <td>RSB</td> <td>1.0</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H30</td> <td>TIN</td> <td>2.4</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H31</td> <td>TEB</td> <td>2.5</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>			TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	1	X	X	X	1	X	Hold	X	X	X	X	1	X	X	X	0	1	Hold	X	X	X	X	1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X	1	X	X	X	X	X	X	X	1	0	X	1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X	1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X	0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Input			Output			Switching speed				Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)								IN → OUT	MIN.	TYP.	MAX.	H01	DI0	2.4	N01	DO0	23.7	RA0 to RA4 (LH) →DO0 to DO15 (HH) (HL) (LL)	1.46	3.72	7.42	⋮	⋮	⋮	⋮	⋮	⋮	1.44	3.71	7.42	H16	DI15	2.4	N16	DO15	23.7	2.35	4.35	7.62	H17	WA0	2.4	N17	TOUT	26.0	2.38	4.37	7.62	⋮	⋮	⋮	⋮	⋮	⋮	RSB →DO0 to DO15 (HL)	0.70	1.11	1.79	H21	WA4	2.4				0.79	1.17	1.80	H22	RA0	2.4				DI0 to DI15 (HH) →DO0 to DO15 (LL)	1.48	3.03	5.55	⋮	⋮	⋮				1.57	3.18	5.80	H26	RA4	2.4								H27	WEB	2.4								H28	WSB	1.0								H29	RSB	1.0								H30	TIN	2.4								H31	TEB	2.5							
TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT																																																																																																																																																																																																																																																					
1	X	X	X	1	X	Hold	X	X	X	X																																																																																																																																																																																																																																																					
1	X	X	X	0	1	Hold	X	X	X	X																																																																																																																																																																																																																																																					
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X																																																																																																																																																																																																																																																					
1	X	X	X	X	X	X	X	1	0	X																																																																																																																																																																																																																																																					
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																					
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																					
0	CLOCK	X	X	X	X	X	X	X	X	RESULT																																																																																																																																																																																																																																																					
Input			Output			Switching speed																																																																																																																																																																																																																																																									
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)																																																																																																																																																																																																																																																							
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H01	DI0	2.4	N01	DO0	23.7	RA0 to RA4 (LH) →DO0 to DO15 (HH) (HL) (LL)	1.46	3.72	7.42																																																																																																																																																																																																																																																						
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H16	DI15	2.4	N16	DO15	23.7		2.35	4.35	7.62																																																																																																																																																																																																																																																						
H17	WA0	2.4	N17	TOUT	26.0		2.38	4.37	7.62																																																																																																																																																																																																																																																						
⋮	⋮	⋮	⋮	⋮	⋮	RSB →DO0 to DO15 (HL)	0.70	1.11	1.79																																																																																																																																																																																																																																																						
H21	WA4	2.4					0.79	1.17	1.80																																																																																																																																																																																																																																																						
H22	RA0	2.4				DI0 to DI15 (HH) →DO0 to DO15 (LL)	1.48	3.03	5.55																																																																																																																																																																																																																																																						
⋮	⋮	⋮					1.57	3.18	5.80																																																																																																																																																																																																																																																						
H26	RA4	2.4																																																																																																																																																																																																																																																													
H27	WEB	2.4																																																																																																																																																																																																																																																													
H28	WSB	1.0																																																																																																																																																																																																																																																													
H29	RSB	1.0																																																																																																																																																																																																																																																													
H30	TIN	2.4																																																																																																																																																																																																																																																													
H31	TEB	2.5																																																																																																																																																																																																																																																													
Equivalent Cells		5036		Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																							

HIGH DENSITY DUAL-PORT RAM BLOCK

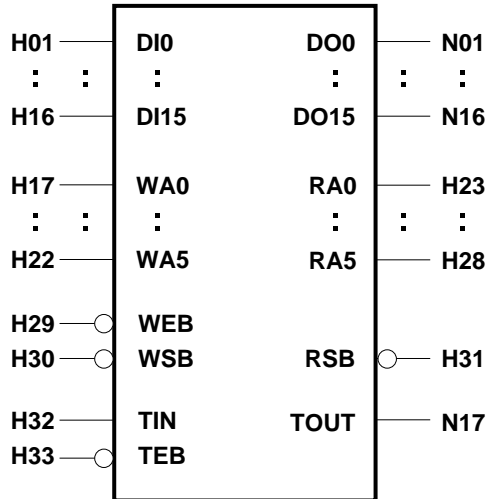
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.62		
Address access time	tACA			7.62
Address output hold time	tOH	2.05		
RSB access time	tREC			1.80
RSB output hold time	tREL	0.79		1.80
RSB output set time	tRLL	0.70		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.92		
WSB-WEB reset time	tCWR	5.66		
Write pulse width	tWP	5.66		
Address setup time	tAS	2.98		
Address hold time	tAH	0.28		
Input data setup time	tDS	3.22		
Input data hold time	tDH	0.50		
WEB access time	tWEC			8.60

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9CB	64 words × 16 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7					
:	:	:	:	:	:					
H16	DI15	2.4	N16	DO15	23.7	RA0 to RA5 (LH)		1.59	3.91	7.69
H17	WA0	2.4	N17	TOUT	26.0	→DO0 to DO15 (HH)		1.58	3.90	7.69
:	:	:				(HL)		2.50	4.55	7.89
H22	WA5	2.4				(LL)		2.50	4.55	7.89
H23	RA0	2.4				RSB (LH)		0.68	1.10	1.78
:	:	:				→DO0 to DO15 (HL)		0.78	1.16	1.79
H28	RA5	2.4								
H29	WEB	2.4				DI0 to DI15 (HH)		1.61	3.24	5.89
H30	WSB	1.0				→DO0 to DO15 (LL)		1.69	3.38	6.13
H31	RSB	1.0								
H32	TIN	2.4								
H33	TEB	2.5								
Equivalent Cells		6635		Power (mW/MHz)				Rev.		1

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.89		
Address access time	tACA			7.89
Address output hold time	tOH	2.19		
RSB access time	tREC			1.78
RSB output hold time	tREL	0.78		1.79
RSB output set time	tRLL	0.68		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.05		
WSB-WEB reset time	tCWR	5.44		
Write pulse width	tWP	5.44		
Address setup time	tAS	2.37		
Address hold time	tAH	0.24		
Input data setup time	tDS	3.21		
Input data hold time	tDH	0.38		
WEB access time	tWEC			8.89

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																																																																																											
R9CD	128 words × 16 bits Dual-port RAM																																																																																																																																																																																																																																																																																																																																																												
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TYP.	MAX.	H01	DI0	2.4	N01	DO0	24.7					:	:	:	:	:	:					H16	DI15	2.4	N16	DO15	24.7					H17	WA0	2.4	N17	TOUT	26.0					:	:	:								H23	WA6	2.4								H24	RA0	2.4								:	:	:								H30	RA6	2.4								H31	WEB	2.4								H32	WSB	2.4								H33	RSB	2.4								H34	TIN	2.4								H35	TEB	2.5														RA0 to RA6 (LH)		0.60	3.45	8.11							→DO0 to DO15 (HH)		0.52	3.40	8.11							(HL)		1.58	4.14	8.31							(LL)		1.52	4.10	8.31							RSB (LH)		0.98	1.49	2.33							→DO0 to DO15 (HL)		1.12	1.64	2.51							DI0 to DI15 (HH)		1.82	3.53	6.32							→DO0 to DO15 (LL)		1.99	3.82	6.80
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Equivalent Cells		12939		Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																																																																																																																					

HIGH DENSITY DUAL-PORT RAM BLOCK

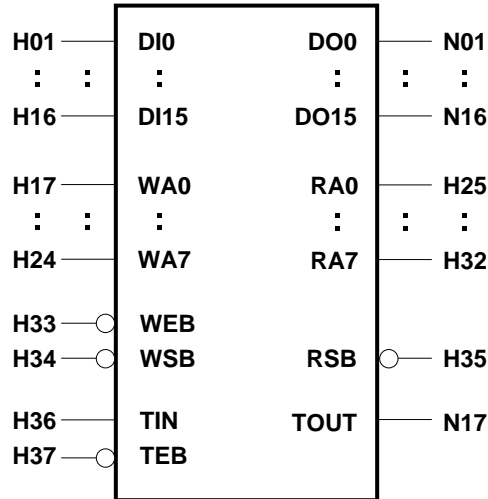
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.31		
Address access time	tACA			8.31
Address output hold time	tOH	2.21		
RSB access time	tREC			2.34
RSB output hold time	tREL	1.12		2.51
RSB output set time	tRLL	0.98		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.22		
WSB-WEB reset time	tCWR	5.56		
Write pulse width	tWP	5.56		
Address setup time	tAS	2.34		
Address hold time	tAH	0.32		
Input data setup time	tDS	3.17		
Input data hold time	tDH	0.51		
WEB access time	tWEC			9.44

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9CF	256 words × 16 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)			
						IN → OUT		MIN.	TYP.	MAX.	
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA7 (LH) →DO0 to DO15 (HH)	(HL)	2.20	4.80	9.04	
:	:	:	:	:	:			(HL)	2.19	4.79	9.04
H16	DI15	2.4	N16	DO15	23.7			(LL)	2.90	5.31	9.24
H17	WA0	2.4	N17	TOUT	26.0			(LL)	2.90	5.31	9.24
:	:	:				RSB	(LH)	0.71	1.13	1.81	
H24	WA7	2.4						(HL)	0.84	1.24	1.90
H25	RA0	2.4				DI0 to DI15 (HH)	(LL)	2.14	4.09	7.28	
:	:	:						(LL)	2.06	4.00	7.15
H32	RA7	2.4									
H33	WEB	2.4									
H34	WSB	1.0									
H35	RSB	1.0									
H36	TIN	2.4									
H37	TEB	2.5									
Equivalent Cells		20439		Power (mW/MHz)		Rev.		1			

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.24		
Address access time	tACA			9.24
Address output hold time	tOH	2.59		
RSB access time	tREC			1.81
RSB output hold time	tREL	0.84		1.90
RSB output set time	tRLL	0.71		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.89		
WSB-WEB reset time	tCWR	5.68		
Write pulse width	tWP	5.68		
Address setup time	tAS	3.97		
Address hold time	tAH	0.24		
Input data setup time	tDS	3.39		
Input data hold time	tDH	0.49		
WEB access time	tWEC			10.19

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																				
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HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.68		
Address access time	tACA			9.68
Address output hold time	tOH	2.60		
RSB access time	tREC			2.48
RSB output hold time	tREL	1.17		2.62
RSB output set time	tRLL	1.02		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	10.14		
WSB-WEB reset time	tCWR	5.83		
Write pulse width	tWP	5.83		
Address setup time	tAS	3.98		
Address hold time	tAH	0.33		
Input data setup time	tDS	3.37		
Input data hold time	tDH	0.63		
WEB access time	tWEC			10.77

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																													
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H17	WA0	2.4	N17	TOUT	26.0																																																																																																																																																																																																																																																																																										
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H41	TEB	2.5																																																																																																																																																																																																																																																																																													
Equivalent Cells			74160			Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																																																					

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.30		
Address access time	tACA			12.30
Address output hold time	tOH	3.88		
RSB access time	tREC			1.94
RSB output hold time	tREL	0.95		2.08
RSB output set time	tRLL	0.79		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	12.91		
WSB-WEB reset time	tCWR	6.66		
Write pulse width	tWP	6.66		
Address setup time	tAS	6.00		
Address hold time	tAH	0.25		
Input data setup time	tDS	3.98		
Input data hold time	tDH	0.61		
WEB access time	tWEC			14.51

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																													
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H01	DI0	2.4	N01	DO0	23.7	RA0 to RA5 (LH) →DO0 to DO19 (HH) (HL) (LL)	1.60	3.93	7.73																																																																																																																																																																																																																																																						
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Equivalent Cells	8125	Power (mW/MHz)	Rev.	1																																																																																																																																																																																																																																																											

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.93		
Address access time	tACA			7.93
Address output hold time	tOH	2.21		
RSB access time	tREC			1.81
RSB output hold time	tREL	0.80		1.83
RSB output set time	tRLL	0.69		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.14		
WSB-WEB reset time	tCWR	5.43		
Write pulse width	tWP	5.43		
Address setup time	tAS	2.47		
Address hold time	tAH	0.24		
Input data setup time	tDS	3.20		
Input data hold time	tDH	0.38		
WEB access time	tWEC			8.93

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																																																																																	
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HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.35		
Address access time	tACA			8.35
Address output hold time	tOH	2.59		
RSB access time	tREC			2.41
RSB output hold time	tREL	1.15		2.55
RSB output set time	tRLL	0.99		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.34		
WSB-WEB reset time	tCWR	5.57		
Write pulse width	tWP	5.57		
Address setup time	tAS	2.45		
Address hold time	tAH	0.32		
Input data setup time	tDS	3.17		
Input data hold time	tDH	0.51		
WEB access time	tWEC			9.49

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																			
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Equivalent Cells		25290		Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																													

HIGH DENSITY DUAL-PORT RAM BLOCK

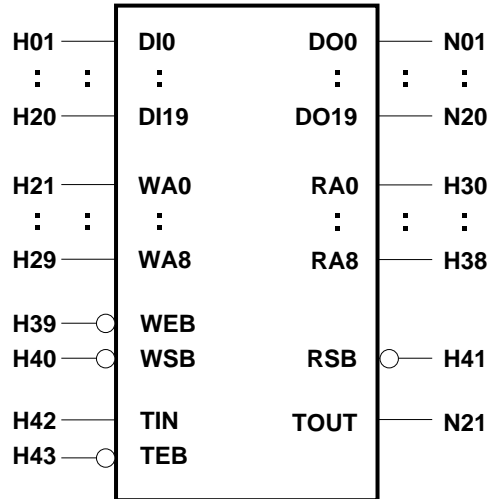
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.25		
Address access time	tACA			9.25
Address output hold time	tOH	2.63		
RSB access time	tREC			1.86
RSB output hold time	tREL	0.88		1.97
RSB output set time	tRLL	0.73		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.38		
WSB-WEB reset time	tCWR	5.69		
Write pulse width	tWP	5.69		
Address setup time	tAS	3.98		
Address hold time	tAH	0.24		
Input data setup time	tDS	3.39		
Input data hold time	tDH	0.49		
WEB access time	tWEC			10.26

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9EH	512 words × 20 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7					
:	:	:	:	:	:					
H20	DI19	2.4	N20	DO19	24.7	RA0 to RA8	(LH)	0.65	4.01	9.50
H21	WA0	2.4	N21	TOUT	26.0	→DO0 to DO19	(HH)	0.58	3.97	9.50
:	:	:					(HL)	1.66	4.72	9.70
H29	WA8	2.4					(LL)	1.59	4.67	9.70
H30	RA0	2.4				RSB	(LH)	1.04	1.58	2.46
:	:	:				→DO0 to DO19	(HL)	1.21	1.77	2.70
H38	RA8	2.4								
H39	WEB	2.4				DI0 to DI19	(HH)	2.34	4.38	7.71
H40	WSB	2.4				→DO0 to DO19	(LL)	2.37	4.45	7.85
H41	RSB	2.4								
H42	TIN	2.4								
H43	TEB	2.5								
Equivalent Cells		50129		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

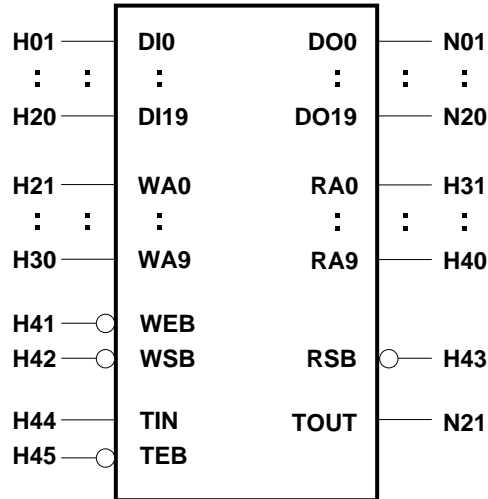
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.70		
Address access time	tACA			9.70
Address output hold time	tOH	2.63		
RSB access time	tREC			2.56
RSB output hold time	tREL	1.21		2.70
RSB output set time	tRLL	1.04		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	10.17		
WSB-WEB reset time	tCWR	5.84		
Write pulse width	tWP	5.84		
Address setup time	tAS	3.99		
Address hold time	tAH	0.34		
Input data setup time	tDS	3.37		
Input data hold time	tDH	0.64		
WEB access time	tWEC			10.84

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9EM	1K words × 20 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7					
:	:	:	:	:	:					
H20	DI19	2.4	N20	DO19	23.7	RA0 to RA9 (LH)		4.44	7.35	12.11
H21	WA0	2.4	N21	TOUT	26.0	→DO0 to DO19 (HH)		4.43	7.35	12.11
:	:	:				(HL)		4.22	7.29	12.31
						(LL)		4.22	7.29	12.31
H30	WA9	2.4				RSB (LH)		0.84	1.28	2.01
H31	RA0	2.4				→DO0 to DO19 (HL)		0.99	1.44	2.17
:	:	:								
H40	RA9	2.4				DI0 to DI19 (HH)		4.16	7.00	11.64
H41	WEB	2.4				→DO0 to DO19 (LL)		3.75	6.76	11.67
H42	WSB	1.0								
H43	RSB	1.0								
H44	TIN	2.4								
H45	TEB	2.5								
Equivalent Cells		92244		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	12.31		
Address access time	tACA			12.31
Address output hold time	tOH	3.92		
RSB access time	tREC			2.04
RSB output hold time	tREL	0.99		2.18
RSB output set time	tRLL	0.84		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	13.25		
WSB-WEB reset time	tCWR	6.90		
Write pulse width	tWP	6.90		
Address setup time	tAS	6.10		
Address hold time	tAH	0.25		
Input data setup time	tDS	3.78		
Input data hold time	tDH	0.61		
WEB access time	tWEC			14.52

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																																																																																											
R9H7	16 words × 32 bits Dual-port RAM																																																																																																																																																																																																																																																																																																																																																												
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TYP.	MAX.	H01	DI0	2.4	N01	DO0	23.7					:	:	:	:	:	:					H32	DI31	2.4	N32	DO31	23.7					H33	WA0	2.4	N33	TOUT	26.0					:	:	:								H36	WA3	2.4								H37	RA0	2.4								:	:	:								H40	RA3	2.4								H41	WEB	2.4								H42	WSB	1.0								H43	RSB	1.0								H44	TIN	2.4								H45	TEB	2.5														RA0 to RA3 (LH)		1.48	3.76	7.47							→DO0 to DO31 (HH)		1.43	3.73	7.47							(HL)		2.35	4.37	7.67							(LL)		2.40	4.40	7.67							RSB (LH)		0.80	1.23	1.94							→DO0 to DO31 (HL)		0.90	1.31	1.99							DI0 to DI31 (HH)		1.48	2.99	5.45							→DO0 to DO31 (LL)		1.57	3.14	5.70
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						RA0 to RA3 (LH)		1.48	3.76	7.47																																																																																																																																																																																																																																																																																																																																																			
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						(HL)		2.35	4.37	7.67																																																																																																																																																																																																																																																																																																																																																			
						(LL)		2.40	4.40	7.67																																																																																																																																																																																																																																																																																																																																																			
						RSB (LH)		0.80	1.23	1.94																																																																																																																																																																																																																																																																																																																																																			
						→DO0 to DO31 (HL)		0.90	1.31	1.99																																																																																																																																																																																																																																																																																																																																																			
						DI0 to DI31 (HH)		1.48	2.99	5.45																																																																																																																																																																																																																																																																																																																																																			
						→DO0 to DO31 (LL)		1.57	3.14	5.70																																																																																																																																																																																																																																																																																																																																																			
Equivalent Cells		5606		Power (mW/MHz)		Rev.		1																																																																																																																																																																																																																																																																																																																																																					

HIGH DENSITY DUAL-PORT RAM BLOCK

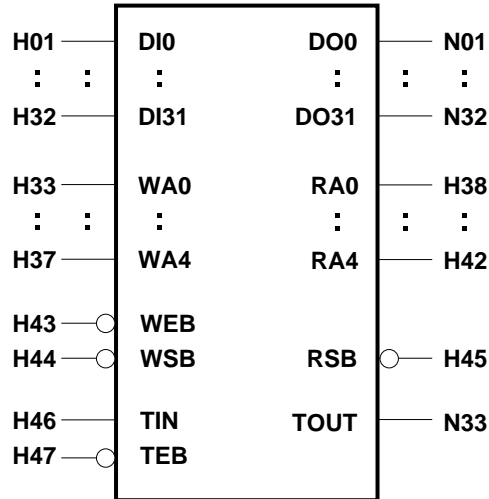
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.67		
Address access time	tACA			7.67
Address output hold time	tOH	2.04		
RSB access time	tREC			1.94
RSB output hold time	tREL	0.90		2.00
RSB output set time	tRLL	0.80		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.12		
WSB-WEB reset time	tCWR	5.54		
Write pulse width	tWP	5.54		
Address setup time	tAS	3.23		
Address hold time	tAH	0.35		
Input data setup time	tDS	3.01		
Input data hold time	tDH	0.76		
WEB access time	tWEC			8.82

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9H9	32 words × 32 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA4 (LH) →DO0 to DO31 (HH) (HL) (LL)	1.58	3.89	7.67	
⋮	⋮	⋮	⋮	⋮	⋮		1.53	3.86	7.67	
H32	DI31	2.4	N32	DO31	23.7		2.45	4.51	7.87	
H33	WA0	2.4	N33	TOUT	26.0		2.50	4.54	7.87	
⋮	⋮	⋮				RSB (LH) →DO0 to DO31 (HL)	0.81	1.24	1.95	
H37	WA4	2.4					0.91	1.32	2.00	
H38	RA0	2.4				DI0 to DI31 (HH) →DO0 to DO31 (LL)	1.49	3.03	5.55	
⋮	⋮	⋮					1.58	3.19	5.80	
H42	RA4	2.4								
H43	WEB	2.4								
H44	WSB	1.0								
H45	RSB	1.0								
H46	TIN	2.4								
H47	TEB	2.5								
Equivalent Cells		9852		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.87		
Address access time	tACA			7.87
Address output hold time	tOH	2.15		
RSB access time	tREC			1.95
RSB output hold time	tREL	0.91		2.01
RSB output set time	tRLL	0.81		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.54		
WSB-WEB reset time	tCWR	5.94		
Write pulse width	tWP	5.94		
Address setup time	tAS	3.24		
Address hold time	tAH	0.36		
Input data setup time	tDS	3.02		
Input data hold time	tDH	0.77		
WEB access time	tWEC			8.92

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family																																																																																																																																																																																																																																																																																				
R9HB	64 words × 32 bits Dual-port RAM																																																																																																																																																																																																																																																																																					
<p>Logic Diagram</p> <div style="text-align: center; margin: 20px 0;"> </div>																																																																																																																																																																																																																																																																																						
<p>Truth Table</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>TEB</th> <th>TIN</th> <th>DIn</th> <th>WAn</th> <th>WSB</th> <th>WEB</th> <th>DMn</th> <th>RAn</th> <th>RSB</th> <th>DOn</th> <th>TOUT</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>Hold</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>DMn</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>1</td> <td>X</td> <td>DIn</td> <td>WAn</td> <td>0</td> <td>0</td> <td>DIn(WAn)</td> <td>RAn</td> <td>0</td> <td>DMn(RAn)</td> <td>X</td> </tr> <tr> <td>0</td> <td>CLOCK</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>RESULT</td> </tr> </tbody> </table> <p>Caution WEB or WSB must be high during all address transition.</p> <p>X : Irrelevant WSB : A-port select RAn : B-port address (Read) DIn : Input data WEB : Write enable RSB : B-port select WAn : A-port address (Write) DMn : Memory data DOn : Output data</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th colspan="3">Input</th> <th colspan="3">Output</th> <th colspan="4">Switching speed</th> </tr> <tr> <th>Name</th> <th>Symbol</th> <th>Fan-in</th> <th>Name</th> <th>Symbol</th> <th>Fan-out</th> <th colspan="2">Path</th> <th colspan="2">t_{LD0} (ns)</th> </tr> <tr> <th colspan="6"></th> <th>IN</th> <th>→</th> <th>OUT</th> <th>MIN.</th> <th>TYP.</th> <th>MAX.</th> </tr> </thead> <tbody> <tr> <td>H01</td> <td>DI0</td> <td>2.4</td> <td>N01</td> <td>DO0</td> <td>23.7</td> <td colspan="2"></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td colspan="2"></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H32</td> <td>DI31</td> <td>2.4</td> <td>N32</td> <td>DO31</td> <td>23.7</td> <td colspan="2">RA0 to RA5 (LH)</td> <td>1.65</td> <td>3.99</td> <td>7.82</td> </tr> <tr> <td>H33</td> <td>WA0</td> <td>2.4</td> <td>N33</td> <td>TOUT</td> <td>26.0</td> <td colspan="2">→DO0 to DO31 (HH)</td> <td>1.63</td> <td>3.98</td> <td>7.82</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td colspan="2"></td> <td></td> <td colspan="2">(HL)</td> <td>2.54</td> <td>4.62</td> <td>8.02</td> </tr> <tr> <td>H38</td> <td>WA5</td> <td>2.4</td> <td colspan="2"></td> <td></td> <td colspan="2">(LL)</td> <td>2.57</td> <td>4.64</td> <td>8.02</td> </tr> <tr> <td>H39</td> <td>RA0</td> <td>2.4</td> <td colspan="2"></td> <td></td> <td colspan="2">RSB (LH)</td> <td>0.75</td> <td>1.17</td> <td>1.87</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td colspan="2"></td> <td></td> <td colspan="2">→DO0 to DO31 (HL)</td> <td>0.85</td> <td>1.24</td> <td>1.89</td> </tr> <tr> <td>H44</td> <td>RA5</td> <td>2.4</td> <td colspan="2"></td> <td></td> <td colspan="2"></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H45</td> <td>WEB</td> <td>2.4</td> <td colspan="2"></td> <td></td> <td colspan="2"></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H46</td> <td>WSB</td> <td>1.0</td> <td colspan="2"></td> <td></td> <td colspan="2">DI0 to DI31 (HH)</td> <td>1.62</td> <td>3.24</td> <td>5.89</td> </tr> <tr> <td>H47</td> <td>RSB</td> <td>1.0</td> <td colspan="2"></td> <td></td> <td colspan="2">→DO0 to DO31 (LL)</td> <td>1.70</td> <td>3.39</td> <td>6.13</td> </tr> <tr> <td>H48</td> <td>TIN</td> <td>2.4</td> <td colspan="2"></td> <td></td> <td colspan="2"></td> <td></td> <td></td> <td></td> </tr> <tr> <td>H49</td> <td>TEB</td> <td>2.5</td> <td colspan="2"></td> <td></td> <td colspan="2"></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>			TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	1	X	X	X	1	X	Hold	X	X	X	X	1	X	X	X	0	1	Hold	X	X	X	X	1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X	1	X	X	X	X	X	X	X	1	0	X	1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X	1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X	0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Input			Output			Switching speed				Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)								IN	→	OUT	MIN.	TYP.	MAX.	H01	DI0	2.4	N01	DO0	23.7							:	:	:	:	:	:							H32	DI31	2.4	N32	DO31	23.7	RA0 to RA5 (LH)		1.65	3.99	7.82	H33	WA0	2.4	N33	TOUT	26.0	→DO0 to DO31 (HH)		1.63	3.98	7.82	:	:	:				(HL)		2.54	4.62	8.02	H38	WA5	2.4				(LL)		2.57	4.64	8.02	H39	RA0	2.4				RSB (LH)		0.75	1.17	1.87	:	:	:				→DO0 to DO31 (HL)		0.85	1.24	1.89	H44	RA5	2.4									H45	WEB	2.4									H46	WSB	1.0				DI0 to DI31 (HH)		1.62	3.24	5.89	H47	RSB	1.0				→DO0 to DO31 (LL)		1.70	3.39	6.13	H48	TIN	2.4									H49	TEB	2.5								
TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT																																																																																																																																																																																																																																																																												
1	X	X	X	1	X	Hold	X	X	X	X																																																																																																																																																																																																																																																																												
1	X	X	X	0	1	Hold	X	X	X	X																																																																																																																																																																																																																																																																												
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X																																																																																																																																																																																																																																																																												
1	X	X	X	X	X	X	X	1	0	X																																																																																																																																																																																																																																																																												
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																																												
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X																																																																																																																																																																																																																																																																												
0	CLOCK	X	X	X	X	X	X	X	X	RESULT																																																																																																																																																																																																																																																																												
Input			Output			Switching speed																																																																																																																																																																																																																																																																																
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)																																																																																																																																																																																																																																																																														
						IN	→	OUT	MIN.	TYP.	MAX.																																																																																																																																																																																																																																																																											
H01	DI0	2.4	N01	DO0	23.7																																																																																																																																																																																																																																																																																	
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H32	DI31	2.4	N32	DO31	23.7	RA0 to RA5 (LH)		1.65	3.99	7.82																																																																																																																																																																																																																																																																												
H33	WA0	2.4	N33	TOUT	26.0	→DO0 to DO31 (HH)		1.63	3.98	7.82																																																																																																																																																																																																																																																																												
:	:	:				(HL)		2.54	4.62	8.02																																																																																																																																																																																																																																																																												
H38	WA5	2.4				(LL)		2.57	4.64	8.02																																																																																																																																																																																																																																																																												
H39	RA0	2.4				RSB (LH)		0.75	1.17	1.87																																																																																																																																																																																																																																																																												
:	:	:				→DO0 to DO31 (HL)		0.85	1.24	1.89																																																																																																																																																																																																																																																																												
H44	RA5	2.4																																																																																																																																																																																																																																																																																				
H45	WEB	2.4																																																																																																																																																																																																																																																																																				
H46	WSB	1.0				DI0 to DI31 (HH)		1.62	3.24	5.89																																																																																																																																																																																																																																																																												
H47	RSB	1.0				→DO0 to DO31 (LL)		1.70	3.39	6.13																																																																																																																																																																																																																																																																												
H48	TIN	2.4																																																																																																																																																																																																																																																																																				
H49	TEB	2.5																																																																																																																																																																																																																																																																																				
Equivalent Cells	13026	Power (mW/MHz)	Rev.	1																																																																																																																																																																																																																																																																																		

HIGH DENSITY DUAL-PORT RAM BLOCK

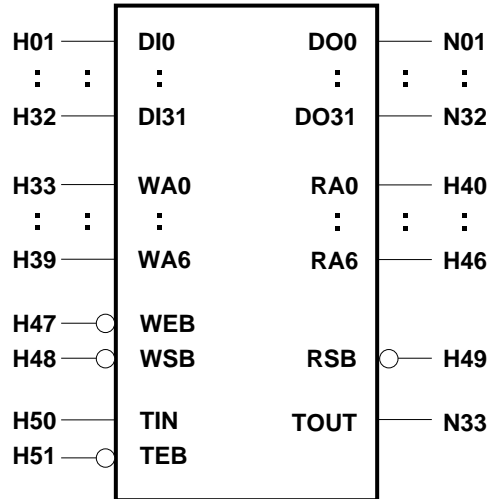
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.02		
Address access time	tACA			8.02
Address output hold time	tOH	2.25		
RSB access time	tREC			1.87
RSB output hold time	tREL	0.85		1.90
RSB output set time	tRLL	0.75		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.34		
WSB-WEB reset time	tCWR	5.56		
Write pulse width	tWP	5.56		
Address setup time	tAS	2.50		
Address hold time	tAH	0.28		
Input data setup time	tDS	3.10		
Input data hold time	tDH	0.52		
WEB access time	tWEC			9.05

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9HD	128 words × 32 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7					
:	:	:	:	:	:					
H32	DI31	2.4	N32	DO31	24.7	RA0 to RA6 (LH)		0.67	3.60	8.39
H33	WA0	2.4	N33	TOUT	26.0	→DO0 to DO31 (HH)		0.59	3.55	8.39
:	:	:				(HL)		1.64	4.28	8.59
H39	WA6	2.4				(LL)		1.59	4.25	8.59
H40	RA0	2.4				RSB (LH)		1.06	1.61	2.50
:	:	:				→DO0 to DO31 (HL)		1.20	1.74	2.63
H46	RA6	2.4								
H47	WEB	2.4				DI0 to DI31 (HH)		1.82	3.53	6.32
H48	WSB	2.4				→DO0 to DO31 (LL)		2.01	3.84	6.82
H49	RSB	2.4								
H50	TIN	2.4								
H51	TEB	2.5								
Equivalent Cells		25605		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

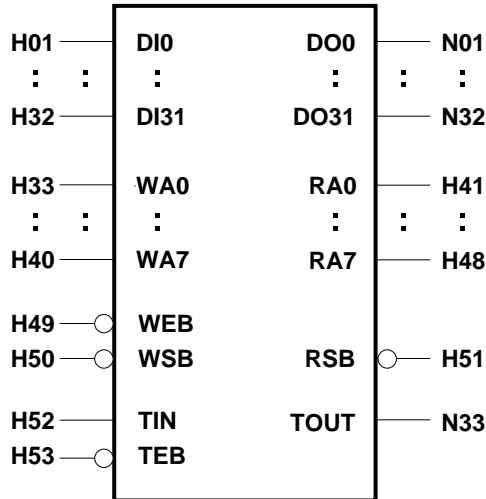
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.59		
Address access time	tACA			8.59
Address output hold time	tOH	2.25		
RSB access time	tREC			2.50
RSB output hold time	tREL	1.20		2.63
RSB output set time	tRLL	1.06		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.93		
WSB-WEB reset time	tCWR	5.87		
Write pulse width	tWP	5.87		
Address setup time	tAS	2.67		
Address hold time	tAH	0.39		
Input data setup time	tDS	3.05		
Input data hold time	tDH	0.78		
WEB access time	tWEC			9.82

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9HF	256 words × 32 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed			
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)	
						IN → OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7	RA0 to RA7 (LH) →DO0 to DO31 (HH)	2.27	4.90	9.19
⋮	⋮	⋮	⋮	⋮	⋮		2.24	4.88	9.19
H32	DI31	2.4	N32	DO31	23.7		→DO0 to DO31 (HL) (LL)	2.95	5.40
H33	WA0	2.4	N33	TOUT	26.0	2.98		5.42	9.39
⋮	⋮	⋮	⋮	⋮	⋮	RSB (LH) →DO0 to DO31 (HL)	0.77	1.20	1.91
H40	WA7	2.4	⋮	⋮	⋮		0.91	1.33	2.02
H41	RA0	2.4	⋮	⋮	⋮	DI0 to DI31 (HH) →DO0 to DO31 (LL)	2.14	4.09	7.28
⋮	⋮	⋮	⋮	⋮	⋮		2.06	4.00	7.15
H48	RA7	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H49	WEB	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H50	WSB	1.0	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H51	RSB	1.0	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H52	TIN	2.4	⋮	⋮	⋮	⋮	⋮	⋮	⋮
H53	TEB	2.5	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Equivalent Cells		40559		Power (mW/MHz)		Rev.		1	

HIGH DENSITY DUAL-PORT RAM BLOCK

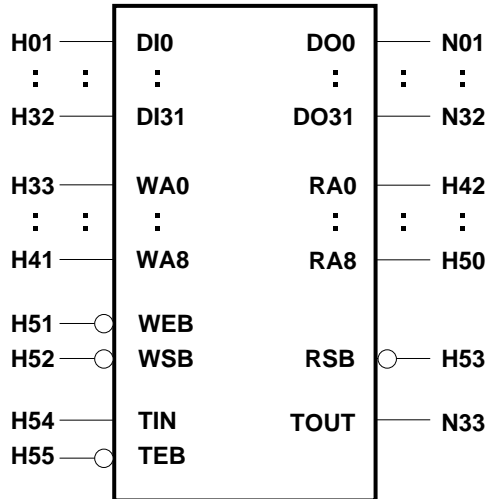
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.39		
Address access time	tACA			9.39
Address output hold time	tOH	2.65		
RSB access time	tREC			2.50
RSB output hold time	tREL	1.20		2.63
RSB output set time	tRLL	1.06		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.93		
WSB-WEB reset time	tCWR	5.87		
Write pulse width	tWP	5.87		
Address setup time	tAS	2.67		
Address hold time	tAH	0.39		
Input data setup time	tDS	3.05		
Input data hold time	tDH	0.78		
WEB access time	tWEC			9.82

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9HH	512 words × 32 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)				
						IN → OUT		MIN.	TYP.	MAX.		
H01	DI0	2.4	N01	DO0	24.7	RA0 to RA8 (LH) →DO0 to DO31 (HH)		0.71	4.17	9.82		
:	:	:	:	:	:			(HL) (LL)		0.65	4.13	9.82
H32	DI31	2.4	N32	DO31	24.7					1.68	4.85	10.02
H33	WA0	2.4	N33	TOUT	26.0	1.62	4.81			10.02		
H41	WA8	2.4				RSB (LH) →DO0 to DO31 (HL)		1.14	1.70	2.61		
H42	RA0	2.4						1.25	1.82	2.77		
H50	RA8	2.4				DI0 to DI31 (HH) →DO0 to DO31 (LL)		2.35	4.39	7.72		
H51	WEB	2.4						2.37	4.46	7.86		
H52	WSB	2.4										
H53	RSB	2.4										
H54	TIN	2.4										
H55	TEB	5.0										
Equivalent Cells		80657		Power (mW/MHz)		Rev.		1				

HIGH DENSITY DUAL-PORT RAM BLOCK

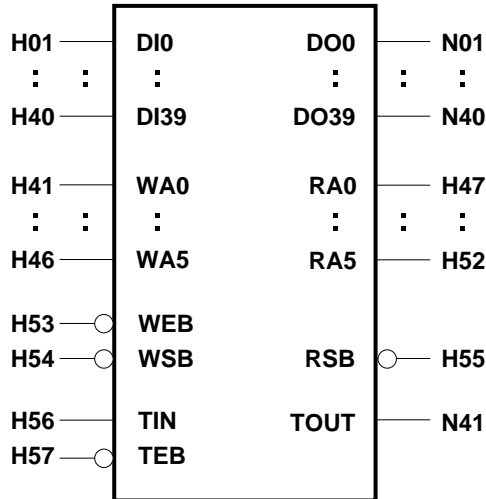
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.02		
Address access time	tACA			10.02
Address output hold time	tOH	2.65		
RSB access time	tREC			2.63
RSB output hold time	tREL	1.25		2.77
RSB output set time	tRLL	1.14		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	10.98		
WSB-WEB reset time	tCWR	6.22		
Write pulse width	tWP	6.22		
Address setup time	tAS	4.35		
Address hold time	tAH	0.41		
Input data setup time	tDS	3.22		
Input data hold time	tDH	0.96		
WEB access time	tWEC			11.23

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KB	64 words × 40 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7					
:	:	:	:	:	:					
H40	DI39	2.4	N40	DO39	23.7	RA0 to RA5 (LH)	1.66	4.02	7.86	
H41	WA0	2.4	N41	TOUT	26.0	→DO0 to DO39 (HH)	1.64	4.00	7.86	
:	:	:				(HL)	2.56	4.65	8.06	
H46	WA5	2.4				(LL)	2.58	4.66	8.06	
H47	RA0	2.4				RSB (LH)	0.76	1.20	1.91	
:	:	:				→DO0 to DO39 (HL)	0.87	1.27	1.94	
H52	RA5	2.4								
H53	WEB	2.4				DI0 to DI39 (HH)	1.61	3.24	5.90	
H54	WSB	1.0				→DO0 to DO39 (LL)	1.70	3.39	6.14	
H55	RSB	1.0								
H56	TIN	2.4								
H57	TEB	2.5								
Equivalent Cells		15994		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

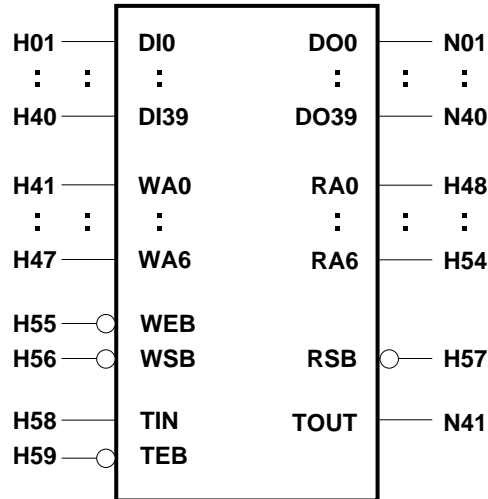
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.06		
Address access time	tACA			8.06
Address output hold time	tOH	2.25		
RSB access time	tREC			1.91
RSB output hold time	tREL	0.87		1.94
RSB output set time	tRLL	0.76		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.45		
WSB-WEB reset time	tCWR	5.57		
Write pulse width	tWP	5.57		
Address setup time	tAS	2.60		
Address hold time	tAH	0.28		
Input data setup time	tDS	3.10		
Input data hold time	tDH	0.52		
WEB access time	tWEC			9.11

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KD	128 words × 40 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT		MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7					
:	:	:	:	:	:					
H40	DI39	2.4	N40	DO39	24.7	RA0 to RA6 (LH)		0.68	3.63	8.44
H41	WA0	2.4	N41	TOUT	26.0	→DO0 to DO39 (HH)		0.61	3.59	8.44
:	:	:				(HL)		1.67	4.32	8.64
H47	WA6	2.4				(LL)		1.61	4.28	8.64
H48	RA0	2.4				RSB (LH)		1.08	1.63	2.54
:	:	:				→DO0 to DO39 (HL)		1.22	1.77	2.67
H54	RA6	2.4								
H55	WEB	2.4				DI0 to DI39 (HH)		1.81	3.53	6.33
H56	WSB	2.4				→DO0 to DO39 (LL)		2.01	3.84	6.82
H57	RSB	2.4								
H58	TIN	2.4								
H59	TEB	2.5								
Equivalent Cells		31469		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

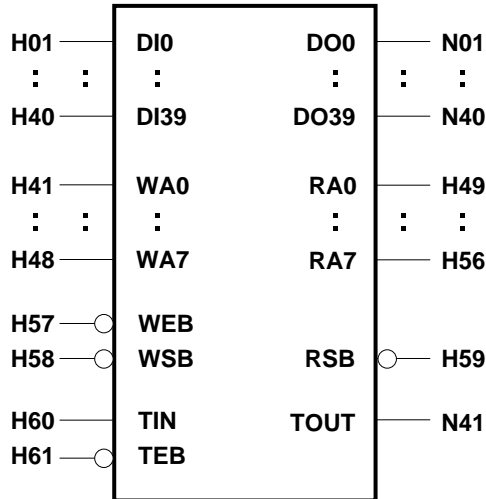
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.64		
Address access time	tACA			8.64
Address output hold time	tOH	2.26		
RSB access time	tREC			2.55
RSB output hold time	tREL	1.22		2.68
RSB output set time	tRLL	1.08		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	9.03		
WSB-WEB reset time	tCWR	5.88		
Write pulse width	tWP	5.88		
Address setup time	tAS	2.77		
Address hold time	tAH	0.38		
Input data setup time	tDS	3.04		
Input data hold time	tDH	0.78		
WEB access time	tWEC			9.88

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KF	256 words × 40 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	23.7					
:	:	:	:	:	:					
H40	DI39	2.4	N40	DO39	23.7	RA0 to RA7	(LH)	2.28	4.91	9.21
H41	WA0	2.4	N41	TOUT	26.0	→DO0 to DO39	(HH)	2.25	4.89	9.21
:	:	:					(HL)	2.99	5.43	9.41
H48	WA7	2.4					(LL)	3.02	5.45	9.41
H49	RA0	2.4				RSB	(LH)	0.79	1.24	1.97
:	:	:				→DO0 to DO39	(HL)	0.95	1.38	2.09
H56	RA7	2.4				DI0 to DI39	(HH)	2.14	4.09	7.28
H57	WEB	2.4				→DO0 to DO39	(LL)	2.06	4.00	7.15
H58	WSB	1.0								
H59	RSB	1.0								
H60	TIN	2.4								
H61	TEB	2.5								
Equivalent Cells		50227		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

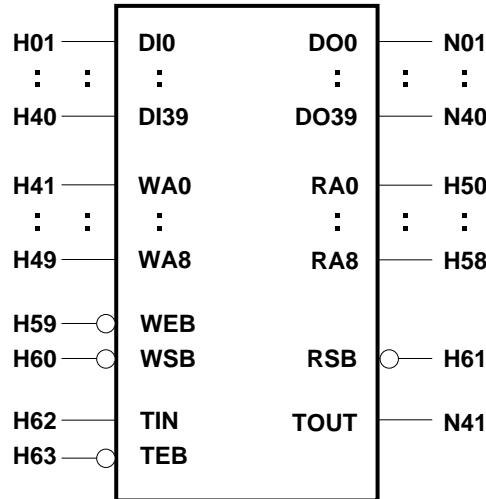
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.41		
Address access time	tACA			9.41
Address output hold time	tOH	2.69		
RSB access time	tREC			1.97
RSB output hold time	tREL	0.95		2.10
RSB output set time	tRLL	0.79		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.95		
WSB-WEB reset time	tCWR	5.84		
Write pulse width	tWP	5.84		
Address setup time	tAS	4.13		
Address hold time	tAH	0.30		
Input data setup time	tDS	3.27		
Input data hold time	tDH	0.96		
WEB access time	tWEC			10.46

HIGH DENSITY DUAL-PORT RAM BLOCK

Block Type	Function	SSI Family
R9KH	512 words × 40 bits Dual-port RAM	

Logic Diagram



Truth Table

TEB	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT
1	X	X	X	1	X	Hold	X	X	X	X
1	X	X	X	0	1	Hold	X	X	X	X
1	X	DIn	WAn	0	0	DIn(WAn)	X	X	X	X
1	X	X	X	X	X	X	X	1	0	X
1	X	X	X	1	1	DMn	RAn	0	DMn(RAn)	X
1	X	DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)	X
0	CLOCK	X	X	X	X	X	X	X	X	RESULT

Caution WEB or WSB must be high during all address transition.

X : Irrelevant WSB : A-port select RAn : B-port address (Read)
 DIn : Input data WEB : Write enable RSB : B-port select
 WAn : A-port address (Write) DMn : Memory data DOn : Output data

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN	→ OUT	MIN.	TYP.	MAX.
H01	DI0	2.4	N01	DO0	24.7					
:	:	:	:	:	:					
H40	DI39	2.4	N40	DO39	24.7	RA0 to RA8	(LH)	0.75	4.21	9.85
H41	WA0	2.4	N41	TOUT	26.0	→DO0 to DO39	(HH)	0.68	4.16	9.85
:	:	:					(HL)	1.71	4.88	10.05
H49	WA8	2.4					(LL)	1.66	4.85	10.05
H50	RA0	2.4				RSB	(LH)	1.17	1.74	2.67
:	:	:				→DO0 to DO39	(HL)	1.29	1.88	2.84
H58	RA8	2.4								
H59	WEB	2.4				DI0 to DI39	(HH)	2.36	4.40	7.72
H60	WSB	2.4				→DO0 to DO39	(LL)	2.37	4.46	7.86
H61	RSB	2.4								
H62	TIN	2.4								
H63	TEB	5.0								
Equivalent Cells		99937		Power (mW/MHz)		Rev.		1		

HIGH DENSITY DUAL-PORT RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.05		
Address access time	tACA			10.05
Address output hold time	tOH	2.69		
RSB access time	tREC			2.71
RSB output hold time	tREL	1.29		2.85
RSB output set time	tRLL	1.17		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	11.01		
WSB-WEB reset time	tCWR	6.23		
Write pulse width	tWP	6.23		
Address setup time	tAS	4.36		
Address hold time	tAH	0.42		
Input data setup time	tDS	3.23		
Input data hold time	tDH	0.98		
WEB access time	tWEC			11.32

[MEMO]



CHAPTER 3

ROM BLOCK

ROM BLOCK

Block Type	Function													
J14DK	128 words × 4 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H07	AD6	2.5	N04	DO3	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD6 → DO0 to DO3		(HH)	0.207	1.272	3.164	0.541	1.212	1.212						
		(HL)	0.444	1.541	3.491	0.359	1.055	1.055						
		(LH)	0.207	1.272	3.164	0.541	1.212	1.212						
		(LL)	0.444	1.541	3.491	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.				MAX.							
Cycle time	t _{CYCLE}	3.4907					3.4907							
Address access time	t _{ACC}													
Address-output hold time	t _{AOH}	0.2074												
Equivalent Cells	1113 (53 × 21)	Power (mW/MHz) ^{Note}		Write cycle										
				Read cycle	0.018									

ROM BLOCK

Block Type	Function								
J14FK	256 words × 4 bits ROM								
Logic Diagram									
Truth Table			Input		Output				
			Name	Symbol	Fan-in	Name	Symbol	Fan-out	
ADn	DON	Operation	H01	AD0	2.5	N01	DO0	53	
ADn	DON	Read	:	:	:	:	:	:	
ADn	DON	Read	H08	AD7	2.5	N04	DO3	53	
ADn : Read address DON : Read data									
Switching speed									
Path		t _{LD0} (ns)			t ₁				
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
AD0 to AD7→DO0 to DO3		(HH) 0.314	1.513	3.645	0.541	1.212	1.212		
		(HL) 0.538	1.769	3.959	0.359	1.055	1.055		
		(LH) 0.314	1.513	3.645	0.541	1.212	1.212		
		(LL) 0.538	1.769	3.959	0.359	1.055	1.055		
Read cycle timing ^{Note}						Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.			
		MIN.	TYP.	MAX.					
Cycle time	t _{CYCLE}	3.9593		3.9593					
Address access time	t _{ACC}								
Address-output hold time	t _{AOH}	0.3135							
Equivalent Cells	2035 (55 × 37)	Power (mW/MHz) ^{Note}		Write cycle					
				Read cycle	0.036				

ROM BLOCK

Block Type	Function								
J14HK	512 words × 4 bits ROM								
Logic Diagram									
Truth Table			Input			Output			
			Name	Symbol	Fan-in	Name	Symbol	Fan-out	
ADn	DOn	Operation	H01	AD0	2.5	N01	DO0	53	
:	:	:	:	:	:	:	:	:	
ADn	DOn	Read	H09	AD8	2.5	N04	DO3	53	
ADn : Read address DOn : Read data									
Switching speed									
Path		t_{LD0} (ns)				t_1			
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
AD0 to AD8 → DO0 to DO3	(HH)	0.314	1.551	3.752	0.541	1.212	1.212		
	(HL)	0.538	1.835	4.142	0.359	1.055	1.055		
	(LH)	0.314	1.551	3.752	0.541	1.212	1.212		
	(LL)	0.538	1.835	4.142	0.359	1.055	1.055		
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.					
		MIN.	TYP.						MAX.
Cycle time	t_{CYCLE}	4.1422							
Address access time	t_{ACC}								4.1422
Address-output hold time	t_{AOH}	0.3135							
Equivalent Cells	3458 (91 × 38)	Power (mW/MHz) ^{Note}		Write cycle					
				Read cycle	0.072				

ROM BLOCK

Block Type	Function																																									
J14MK	1024 words × 4 bits ROM																																									
Logic Diagram 																																										
Truth Table <table border="1" style="margin: auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">ADn</th> <th style="width: 20%;">DON</th> <th style="width: 60%;">Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p style="margin-left: 20px;"> ADn : Read address DOn : Read data </p>				ADn	DON	Operation	ADn	DOn	Read	<table border="1" style="margin: auto; border-collapse: collapse;"> <thead> <tr> <th colspan="3">Input</th> <th colspan="3">Output</th> </tr> <tr> <th>Name</th> <th>Symbol</th> <th>Fan-in</th> <th>Name</th> <th>Symbol</th> <th>Fan-out</th> </tr> </thead> <tbody> <tr> <td>H01</td> <td>AD0</td> <td>2.5</td> <td>N01</td> <td>DO0</td> <td>53</td> </tr> <tr> <td style="text-align: center;">⋮</td> <td style="text-align: center;">⋮</td> <td style="text-align: center;">⋮</td> <td style="text-align: center;">⋮</td> <td style="text-align: center;">⋮</td> <td style="text-align: center;">⋮</td> </tr> <tr> <td>H10</td> <td>AD9</td> <td>2.5</td> <td>N04</td> <td>DO3</td> <td>53</td> </tr> </tbody> </table>			Input			Output			Name	Symbol	Fan-in	Name	Symbol	Fan-out	H01	AD0	2.5	N01	DO0	53	⋮	⋮	⋮	⋮	⋮	⋮	H10	AD9	2.5	N04	DO3	53
ADn	DON	Operation																																								
ADn	DOn	Read																																								
Input			Output																																							
Name	Symbol	Fan-in	Name	Symbol	Fan-out																																					
H01	AD0	2.5	N01	DO0	53																																					
⋮	⋮	⋮	⋮	⋮	⋮																																					
H10	AD9	2.5	N04	DO3	53																																					
Switching speed																																										
Path		t _{LD0} (ns)			t ₁																																					
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.																																			
AD0 to AD9 → DO0 to DO3		(HH)	0.417	1.828	4.336	0.541	1.212	1.212																																		
		(HL)	0.636	1.963	4.323	0.359	1.055	1.055																																		
		(LH)	0.417	1.828	4.336	0.541	1.212	1.212																																		
		(LL)	0.636	1.963	4.323	0.359	1.055	1.055																																		
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.																																						
		MIN.	TYP.				MAX.																																			
Cycle time	t _{CYCLE}	4.3363																																								
Address access time	t _{ACC}						4.3363																																			
Address-output hold time	t _{AOH}	0.4170																																								
Equivalent Cells	6370 (91 × 70)	Power (mW/MHz) ^{Note}		Write cycle	—————																																					
				Read cycle	0.144																																					

ROM BLOCK

Block Type	Function													
J14SK	2048 words × 4 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H11	AD10	2.5	N04	DO3	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD10 → DO0 to DO3		(HH)	0.417	2.198	5.364	0.541	1.212	1.212						
		(HL)	0.638	2.220	5.034	0.359	1.055	1.055						
		(LH)	0.417	2.198	5.364	0.541	1.212	1.212						
		(LL)	0.638	2.220	5.034	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.				MAX.							
Cycle time	t _{CYCLE}	5.3642					5.3642							
Address access time	t _{ACC}		0.4170											
Address-output hold time	t _{AOH}													
Equivalent Cells	12194 (91 × 134)	Power (mW/MHz) ^{Note}		Write cycle										
				Read cycle	0.288									

ROM BLOCK

Block Type	Function								
J18DK	128 words × 8 bits ROM								
Logic Diagram									
Truth Table				Input			Output		
				Name	Symbol	Fan-in	Name	Symbol	Fan-out
ADn	DO_n	Operation		H01	AD0	2.5	N01	DO0	53
:	:			:	:	:	:	:	:
ADn	DO_n	Read		H07	AD6	2.5	N08	DO7	53
				AD_n : Read address DO_n : Read data					
Switching speed									
Path			t_{LD0} (ns)			t_1			
IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
AD0 to AD6 → DO0 to DO7			(HH)	0.207	1.348	3.376	0.541	1.212	1.212
			(HL)	0.444	1.593	3.636	0.359	1.055	1.055
			(LH)	0.207	1.348	3.376	0.541	1.212	1.212
			(LL)	0.444	1.593	3.636	0.359	1.055	1.055
Read cycle timing ^{Note}									
			MIN.	TYP.	MAX.	Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.			
Cycle time t_{CYCLE}			3.6364		3.6364				
Address access time t_{ACC}				0.2074					
Address-output hold time t_{AOH}									
Equivalent Cells		1785 (85 × 21)	Power (mW/MHz) ^{Note}		Write cycle	—			
					Read cycle	0.036			

ROM BLOCK

Block Type	Function													
J18FK	256 words × 8 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H08	AD7	2.5	N08	DO7	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD7 → DO0 to DO7		(HH)	0.314	1.551	3.752	0.541	1.212	1.212						
		(HL)	0.538	1.835	4.142	0.359	1.055	1.055						
		(LH)	0.314	1.551	3.752	0.541	1.212	1.212						
		(LL)	0.538	1.835	4.142	0.359	1.055	1.055						
Read cycle timing ^{Note}				<p>Caution This ROM block is under development in EA-9HD family.</p> <p>Note Values of power consumption and cycle timing are preliminary values.</p>										
		MIN.	TYP.					MAX.						
Cycle time	t _{CYCLE}	4.1422						4.1422						
Address access time	t _{ACC}													
Address-output hold time	t _{AOH}	0.3135												
Equivalent Cells	3219 (87 × 37)	Power (mW/MHz) ^{Note}		Write cycle										
				Read cycle	0.055									

ROM BLOCK

Block Type	Function											
J18HK	512 words × 8 bits ROM											
Logic Diagram												
Truth Table				Input			Output					
				Name	Symbol	Fan-in	Name	Symbol	Fan-out			
AD_n	DO_n	Operation		H01	AD0	2.5	N01	DO0	53			
			:									
AD_n	DO_n	Read		H09	AD8	2.5	N08	DO7	53			
				AD_n : Read address DO_n : Read data								
Switching speed												
Path			t _{LD0} (ns)			t ₁						
IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
AD0 to AD8 → DO0 to DO7			(HH)	0.314	1.666	4.069	0.541	1.212	1.212			
			(HL)	0.538	1.899	4.321	0.359	1.055	1.055			
			(LH)	0.314	1.666	4.069	0.541	1.212	1.212			
			(LL)	0.538	1.899	4.321	0.359	1.055	1.055			
Read cycle timing ^{Note}						Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.						
			MIN.	TYP.	MAX.							
Cycle time			t _{CYCLE}	4.3205								
Address access time			t _{ACC}		4.3205							
Address-output hold time			t _{AOH}	0.3135								
Equivalent Cells	5890 (155 × 38)		Power (mW/MHz) ^{Note}		Write cycle	_____						
					Read cycle	0.110						

ROM BLOCK

Block Type	Function													
J18MK	1024 words × 8 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th style="width: 20%;">ADn</th> <th style="width: 20%;">DOn</th> <th style="width: 60%;">Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p style="margin-left: 40px;">ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H10	AD9	2.5	N08	DO7	53						
Switching speed														
Path		t_{LD0} (ns)			t_1									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD9 → DO0 to DO7		(HH)	0.417	2.019	4.866	0.541	1.212	1.212						
		(HL)	0.636	2.201	4.981	0.359	1.055	1.055						
		(LH)	0.417	2.019	4.866	0.541	1.212	1.212						
		(LL)	0.636	2.201	4.981	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.				MAX.							
Cycle time	t_{CYCLE}	4.9813												
Address access time				4.9813										
Address-output hold time		t_{AOH}	0.4170											
Equivalent Cells		10850 (155 × 70)		Power (mW/MHz) ^{Note}		Write cycle	———							
						Read cycle	0.068							

ROM BLOCK

Block Type	Function													
J18SK	2048 words × 8 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H11	AD10	2.5	N08	DO7	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD10 → DO0 to DO7		(HH)	0.417	2.351	5.788	0.541	1.212	1.212						
		(HL)	0.638	2.317	5.303	0.359	1.055	1.055						
		(LH)	0.417	2.351	5.788	0.541	1.212	1.212						
		(LL)	0.638	2.317	5.303	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.					MAX.						
Cycle time	t _{CYCLE}	5.7882												
Address access time	t _{ACC}		5.7882											
Address-output hold time	t _{AOH}	0.4170												
Equivalent Cells	20770 (155 × 134)	Power (mW/MHz) ^{Note}		Write cycle	—									
				Read cycle	0.136									

ROM BLOCK

Block Type	Function													
J1CDK	128 words × 16 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H07	AD6	2.5	N16	DO15	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD6 → DO0 to DO15		(HH)	0.207	1.460	3.686	0.541	1.212	1.212						
		(HL)	0.444	1.702	3.938	0.359	1.055	1.055						
		(LH)	0.207	1.460	3.686	0.541	1.212	1.212						
		(LL)	0.444	1.702	3.938	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.				MAX.							
Cycle time	t _{CYCLE}	3.9381					3.9381							
Address access time	t _{ACC}			3.9381										
Address-output hold time	t _{AOH}	0.2074												
Equivalent Cells	3129 (149 × 21)	Power (mW/MHz) ^{Note}		Write cycle										
				Read cycle	0.072									

ROM BLOCK

Block Type	Function													
J1CFK	256 words × 16 bits ROM													
Logic Diagram														
Truth Table				Input										
				Name	Symbol	Fan-in	Output							
				H01	AD0	2.5	N01	DO0	53					
				:	:	:	:	:	:					
				H08	AD7	2.5	N16	DO15	53					
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <td style="width: 33%;">ADn</td> <td style="width: 33%;">DON</td> <td style="width: 33%;">Operation</td> </tr> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </table> <p>ADn : Read address DON : Read data</p>			ADn	DON	Operation	ADn	DOn	Read						
ADn	DON	Operation												
ADn	DOn	Read												
Switching speed														
Path			t _{LD0} (ns)				t ₁							
IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
AD0 to AD07 → DO0 to DO15			(HH)	0.314	1.666	4.069	0.541	1.212	1.212					
			(HL)	0.538	1.899	4.321	0.359	1.055	1.055					
			(LH)	0.314	1.666	4.069	0.541	1.212	1.212					
			(LL)	0.538	1.899	4.321	0.359	1.055	1.055					
Read cycle timing ^{Note}						Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.								
			MIN.	TYP.	MAX.									
Cycle time			4.3205							4.3205				
Address access time														
Address-output hold time			0.3135											
Equivalent Cells		5587 (151 × 37)	Power (mW/MHz) ^{Note}		Write cycle			Read cycle	0.110					

ROM BLOCK

Block Type	Function							
J1CHK	512 words × 16 bits ROM							
Logic Diagram								
Truth Table			Input			Output		
			Name	Symbol	Fan-in	Name	Symbol	Fan-out
ADn	DOn	Operation	H01	AD0	2.5	N01	DO0	53
:	:	:	:	:	:	:	:	:
ADn	DOn	Read	H09	AD8	2.5	N16	DO15	53
ADn : Read address DOn : Read data								
Switching speed								
Path			t_{LD0} (ns)			t_1		
IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
AD0 to AD8→DO0 to DO15	(HH)	0.314	1.959	4.884	0.541	1.212	1.212	
	(HL)	0.538	2.021	4.659	0.359	1.055	1.055	
	(LH)	0.314	1.959	4.884	0.541	1.212	1.212	
	(LL)	0.538	2.021	4.659	0.359	1.055	1.055	
Read cycle timing ^{Note}						Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.		
			MIN.	TYP.	MAX.			
Cycle time	t_{CYCLE}	4.8836						
Address access time	t_{ACC}	4.8836						
Address-output hold time	t_{AOH}	0.3135						
Equivalent Cells	10754 (283 × 38)	Power (mW/MHz) ^{Note}		Write cycle	———			
				Read cycle	0.220			

ROM BLOCK

Block Type	Function											
J1CMK	1024 words × 16 bits ROM											
Logic Diagram												
Truth Table				Input			Output					
				Name	Symbol	Fan-in	Name	Symbol	Fan-out			
ADn	DO_n	Operation		H01	AD0	2.5	N01	DO0	53			
:	:			:	:	:	:	:	:			
ADn	DO_n	Read		H10	AD9	2.5	N16	DO15	53			
AD_n : Read address												
DO_n : Read data												
Switching speed												
Path			t_{LD0} (ns)				t_1					
IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
AD0 to AD09 → DO0 to DO15			(HH)	0.417	2.279	5.590	0.541	1.212	1.212			
			(HL)	0.636	2.329	5.338	0.359	1.055	1.055			
			(LH)	0.417	2.279	5.590	0.541	1.212	1.212			
			(LL)	0.636	2.329	5.338	0.359	1.055	1.055			
Read cycle timing ^{Note}						Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.						
			MIN.	TYP.	MAX.							
Cycle time t_{CYCLE}			5.5897									
Address access time t_{ACC}			5.5897									
Address-output hold time t_{AOH}			0.4170									
Equivalent Cells		19810 (283 × 70)		Power (mW/MHz) ^{Note}		Write cycle		—				
						Read cycle		0.136				

ROM BLOCK

Block Type	Function													
J1CSK	2048 words × 16 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H11	AD10	2.5	N16	DO15	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD10 → DO0 to DO15		(HH)	0.417	2.558	6.365	0.541	1.212	1.212						
		(HL)	0.638	2.615	6.130	0.359	1.055	1.055						
		(LH)	0.417	2.558	6.365	0.541	1.212	1.212						
		(LL)	0.638	2.615	6.130	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.				MAX.							
Cycle time	t _{CYCLE}	6.3649					6.3649							
Address access time	t _{ACC}													
Address-output hold time	t _{AOH}	0.4170												
Equivalent Cells	37922 (283 × 134)	Power (mW/MHz) ^{Note}		Write cycle										
				Read cycle	0.272									

ROM BLOCK

Block Type	Function							
J1HFK	256 words × 32 bits ROM							
Logic Diagram								
Truth Table			Input			Output		
			Name	Symbol	Fan-in	Name	Symbol	Fan-out
ADn	DO_n	Operation	H01	AD0	2.5	N01	DO0	53
:	:	:	:	:	:	:	:	:
ADn	DO_n	Read	H08	AD7	2.5	N32	DO31	53
AD_n : Read address								
DO_n : Read data								
Switching speed								
Path		t_{LD0} (ns)			t_1			
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
AD0 to AD7 → DO0 to DO31		(HH)	0.314	1.959	4.884	0.541	1.212	1.212
		(HL)	0.538	2.021	4.659	0.359	1.055	1.055
		(LH)	0.314	1.959	4.884	0.541	1.212	1.212
		(LL)	0.538	2.021	4.659	0.359	1.055	1.055
Read cycle timing ^{Note}								
		MIN.	TYP.	MAX.	Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.			
Cycle time		t_{CYCLE}	4.8836					
Address access time		t_{ACC}	4.8836					
Address-output hold time		t_{AOH}	0.3135					
Equivalent Cells	10323 (279 × 37)		Power (mW/MHz) ^{Note}		Write cycle	———		
					Read cycle	0.220		

ROM BLOCK

Block Type	Function													
J1HHK	512 words × 32 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H09	AD8	2.5	N32	DO31	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD8 → DO0 to DO31		(HH)	0.314	2.343	5.951	0.541	1.212	1.212						
		(HL)	0.538	2.443	5.829	0.359	1.055	1.055						
		(LH)	0.314	2.343	5.951	0.541	1.212	1.212						
		(LL)	0.538	2.443	5.829	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.				MAX.							
Cycle time	t _{CYCLE}	5.9505					5.9505							
Address access time	t _{ACC}			5.9505										
Address-output hold time	t _{AOH}	0.3135												
Equivalent Cells	20482 (539 × 38)	Power (mW/MHz) ^{Note}		Write cycle										
				Read cycle	0.440									

ROM BLOCK

Block Type	Function												
J1HMK	1024 words × 32 bits ROM												
Logic Diagram													
Truth Table				Input			Output						
				Name	Symbol	Fan-in	Name	Symbol	Fan-out				
				H01 : H10	AD0 : AD9	2.5 : 2.5	N01 : N32	DO0 : DO31	53 : 53				
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 20%;">ADn</th> <th style="width: 20%;">DON</th> <th style="width: 60%;">Operation</th> </tr> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </table> <p>ADn : Read address DOn : Read data</p>	ADn	DON	Operation	ADn	DOn	Read							
ADn	DON	Operation											
ADn	DOn	Read											
Switching speed													
Path		t_{LD0} (ns)			t_1								
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
AD0 to AD9 → DO0 to DO31		(HH)	0.417	2.803	7.046	0.541	1.212	1.212					
		(HL)	0.636	2.595	6.076	0.359	1.055	1.055					
		(LH)	0.417	2.803	7.046	0.541	1.212	1.212					
		(LL)	0.636	2.595	6.076	0.359	1.055	1.055					
Read cycle timing ^{Note}				MIN.	TYP.	MAX.	Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.						
		MIN.	TYP.						MAX.				
		7.0459							7.0459				
Cycle time		t_{CYCLE}											
Address access time		t_{ACC}											
Address-output hold time		t_{AOH}	0.4170										
Equivalent Cells		37730 (539 × 70)		Power (mW/MHz) ^{Note}		Write cycle		—————					
						Read cycle		0.272					

ROM BLOCK

Block Type	Function													
J1HSK	2048 words × 32 bits ROM													
Logic Diagram														
Truth Table			Input			Output								
			Name	Symbol	Fan-in	Name	Symbol	Fan-out						
<table border="1" style="margin: auto;"> <thead> <tr> <th>ADn</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>ADn</td> <td>DOn</td> <td>Read</td> </tr> </tbody> </table> <p>ADn : Read address DOn : Read data</p>			ADn	DOn	Operation	ADn	DOn	Read	H01	AD0	2.5	N01	DO0	53
ADn	DOn	Operation												
ADn	DOn	Read												
			:	:	:	:	:							
			H11	AD10	2.5	N32	DO31	53						
Switching speed														
Path		t _{LD0} (ns)			t ₁									
IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
AD0 to AD10 → DO0 to DO31		(HH)	0.417	2.816	7.081	0.541	1.212	1.212						
		(HL)	0.638	2.907	6.940	0.359	1.055	1.055						
		(LH)	0.417	2.816	7.081	0.541	1.212	1.212						
		(LL)	0.638	2.907	6.940	0.359	1.055	1.055						
Read cycle timing ^{Note}				Caution This ROM block is under development in EA-9HD family. Note Values of power consumption and cycle timing are preliminary values.										
		MIN.	TYP.					MAX.						
Cycle time	t _{CYCLE}	7.0812						7.0812						
Address access time	t _{ACC}													
Address-output hold time	t _{AOH}	0.4170												
Equivalent Cells	73968 (552 × 134)	Power (mW/MHz) ^{Note}		Write cycle										
				Read cycle	0.544									

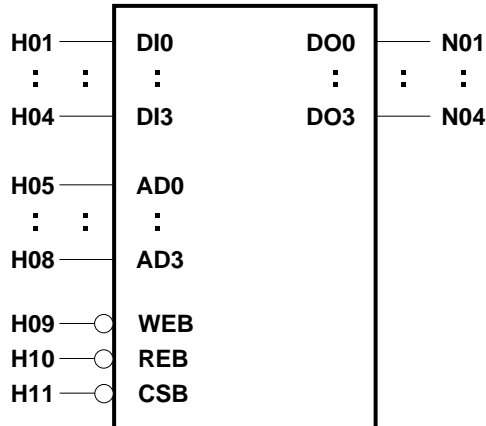
APPENDIX

BASIC RAM BLOCK

BASIC RAM BLOCK

Block Type	Function	SSI Family
K147	16 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DO _n	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DO _n	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant DO_n : Output data
 DIn : Input data WEB : Write enable
 ADn : Address data REB : Read enable
 CSB : Chip select

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD3 (LH) →DO0 to DO3 (HH)	1.597	2.966	5.199	
⋮	⋮	⋮	⋮	⋮	⋮		1.597	2.966	5.199	
H04	DI3	1.0	N04	DO3	26.0	AD0 to AD3 (HL) →DO0 to DO3 (LL)	1.427	2.658	4.667	
H05	AD0	1.0					1.427	2.658	4.667	
⋮	⋮	⋮								
H08	AD3	1.0				CSB →DO0 to DO3 (LL) (LH) (HL)	1.413	2.619	4.587	
H09	WEB	1.0					1.413	2.619	4.587	
H10	REB	1.0					0.444	0.810	1.408	
H11	CSB	1.0				REB (LH) →DO0 to DO3 (HL)	0.405	0.696	1.170	
							0.254	0.474	0.832	
						DI0 to DI3 (HH) →DO0 to DO3 (LL)	1.260	2.365	4.166	
							1.092	1.995	3.468	
Equivalent Cells		48 x 9 = 432		Power (mW/MHz)		Read cycle	0.014		Rev.	1
						Write cycle	0.018			

BASIC RAM BLOCK

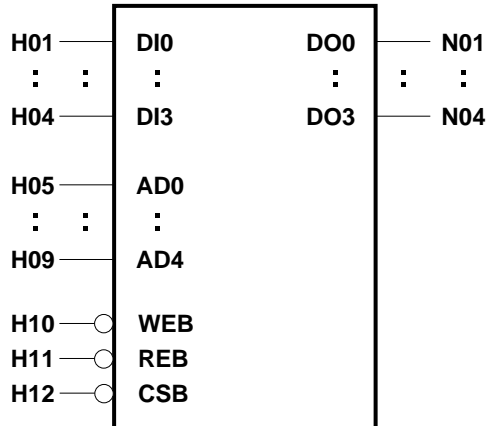
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	5.199		
Address access time	tACA			5.199
Address output hold time	tOH	1.427		
CSB access time	tCSC			4.587
CSB output hold time	tCSL	0.444		1.408
CSB output set time	tCLL	1.413		
REB access time	tREC			1.170
REB output hold time	tREL	0.254		0.832
REB output set time	tRLL	0.405		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	3.500		
CSB-WEB reset time	tCWR	2.400		
Write pulse width	tWP	2.400		
Address setup time	tAS	0.900		
Address hold time	tAH	0.200		
Input data setup time	tDS	2.400		
Input data hold time	tDH	0.000		
WEB access time	tWEC			2.856

BASIC RAM BLOCK

Block Type	Function	SSI Family
K149	32 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DO _n	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DO _n	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant DO_n : Output data
 DIn : Input data WEB : Write enable
 ADn : Address data REB : Read enable
 CSB : Chip select

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD4 →DO0 to DO3	(LH)	1.867	3.482	6.119
:	:	:	:	:	:		(HH)	1.867	3.482	6.119
H04	DI3	1.0	N04	DO3	26.0		(HL)	1.784	3.358	5.925
H05	AD0	1.0					(LL)	1.784	3.358	5.925
:	:	:				CSB →DO0 to DO3	(LL)	1.691	3.165	5.570
H09	AD4	1.0					(LH)	1.691	3.165	5.570
H10	WEB	1.0					(HL)	0.471	0.843	1.452
H11	REB	1.0				REB →DO0 to DO3	(LH)	0.416	0.716	1.207
H12	CSB	1.0					(HL)	0.264	0.489	0.856
						DI0 to DI3 →DO0 to DO3	(HH)	1.274	2.398	4.233
							(LL)	1.174	2.151	3.745
Equivalent Cells		50 x 13 = 650		Power (mW/MHz)		Read cycle	0.015		Rev.	1
						Write cycle	0.019			

BASIC RAM BLOCK

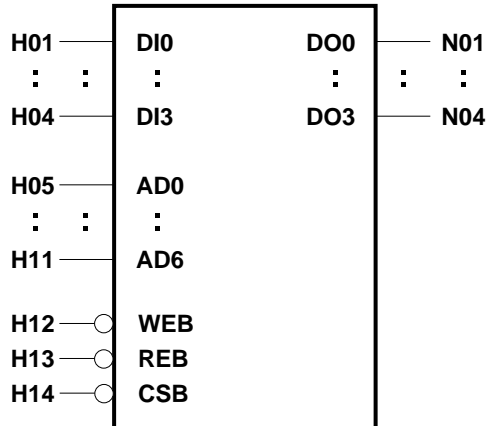
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.119		
Address access time	tACA			6.119
Address output hold time	tOH	1.784		
CSB access time	tCSC			5.570
CSB output hold time	tCSL	0.471		1.452
CSB output set time	tCLL	1.691		
REB access time	tREC			1.207
REB output hold time	tREL	0.264		0.856
REB output set time	tRLL	0.416		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	4.300		
CSB-WEB reset time	tCWR	3.200		
Write pulse width	tWP	3.200		
Address setup time	tAS	1.100		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.400		
Input data hold time	tDH	0.000		
WEB access time	tWEC			3.109

BASIC RAM BLOCK

Block Type	Function	SSI Family
K14D	128 words × 4 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DO _n	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DO _n	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant DO_n : Output data
 DIn : Input data WEB : Write enable
 ADn : Address data REB : Read enable
 CSB : Chip select

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD6 →DO0 to DO3	(LH)	2.102	3.880	6.781
:	:	:	:	:	:		(HH)	2.102	3.880	6.781
H04	DI3	1.0	N04	DO3	26.0		(HL)	2.053	3.784	6.609
H05	AD0	1.0					(LL)	2.053	3.784	6.609
:	:	:				CSB →DO0 to DO3	(LL)	2.001	3.725	6.537
H11	AD6	1.0					(LH)	2.001	3.725	6.537
H12	WEB	1.0					(HL)	0.503	0.910	1.574
H13	REB	1.0				REB →DO0 to DO3	(LH)	0.422	0.774	1.349
H14	CSB	1.0					(HL)	0.331	0.574	0.970
						DI0 to DI3 →DO0 to DO3	(HH)	1.380	2.576	4.528
							(LL)	1.259	2.325	4.065
Equivalent Cells		82 x 21 = 1722		Power (mW/MHz)		Read cycle	0.018		Rev.	1
						Write cycle	0.023			

BASIC RAM BLOCK

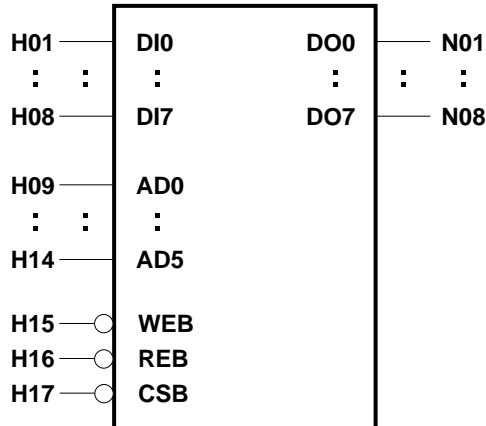
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.781		
Address access time	tACA			6.781
Address output hold time	tOH	2.053		
CSB access time	tCSC			6.537
CSB output hold time	tCSL	0.503		1.574
CSB output set time	tCLL	2.001		
REB access time	tREC			1.349
REB output hold time	tREL	0.331		0.970
REB output set time	tRLL	0.422		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	4.300		
CSB-WEB reset time	tCWR	3.300		
Write pulse width	tWP	3.300		
Address setup time	tAS	1.000		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.100		
Input data hold time	tDH	0.000		
WEB access time	tWEC			3.967

BASIC RAM BLOCK

Block Type	Function	SSI Family
K18B	64 words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant DOn : Output data
 DIn : Input data WEB : Write enable
 ADn : Address data REB : Read enable
 CSB : Chip select

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD5 →DO0 to DO7	(LH)	2.027	3.777	6.632
:	:	:	:	:	:		(HH)	2.027	3.777	6.632
H08	DI7	1.0	N08	DO7	26.0		(HL)	2.006	3.707	6.481
H09	AD0	1.0					(LL)	2.006	3.707	6.481
:	:	:				CSB →DO0 to DO7	(LL)	1.916	3.562	6.246
H14	AD5	1.0					(LH)	1.916	3.562	6.246
H15	WEB	1.0					(HL)	0.526	0.974	1.706
H16	REB	1.0				REB →DO0 to DO7	(LH)	0.491	0.860	1.461
H17	CSB	1.0					(HL)	0.369	0.664	1.145
						DI0 to DI7 →DO0 to DO7	(HH)	1.345	2.534	4.472
							(LL)	1.245	2.287	3.987
Equivalent Cells		94 x 21 = 1974		Power (mW/MHz)		Read cycle	0.023		Rev.	1
						Write cycle	0.032			

BASIC RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.632		
Address access time	tACA			6.632
Address output hold time	tOH	2.006		
CSB access time	tCSC			6.246
CSB output hold time	tCSL	0.526		1.706
CSB output set time	tCLL	1.916		
REB access time	tREC			1.461
REB output hold time	tREL	0.369		1.145
REB output set time	tRLL	0.491		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	4.500		
CSB-WEB reset time	tCWR	3.200		
Write pulse width	tWP	3.200		
Address setup time	tAS	1.300		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.000		
Input data hold time	tDH	0.000		
WEB access time	tWEC			3.994

BASIC RAM BLOCK

Block Type	Function	SSI Family																																																																																																																												
K18F	256 words × 8 bits Single-port RAM																																																																																																																													
<p>Logic Diagram</p> <div style="text-align: center; margin: 20px 0;"> <pre> graph LR subgraph Inputs H01 --- DI0 H08 --- DI7 H09 --- AD0 H16 --- AD7 H17 --- WEB H18 --- REB H19 --- CSB end subgraph Block [] DI0 --- DO0 DI7 --- DO7 AD0 --- DO0 AD7 --- DO7 WEB --- DO0 REB --- DO7 CSB --- DO0 end subgraph Outputs DO0 --- N01 DO7 --- N08 end </pre> </div>																																																																																																																														
<p>Truth Table</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th>DIn</th> <th>ADn</th> <th>CSB</th> <th>WEB</th> <th>REB</th> <th>DOn</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>DIn</td> <td>ADn</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Write</td> </tr> <tr> <td>DIn</td> <td>ADn</td> <td>0</td> <td>0</td> <td>0</td> <td>DIn</td> <td>Write , Read</td> </tr> <tr> <td>X</td> <td>ADn</td> <td>0</td> <td>1</td> <td>0</td> <td>DOn</td> <td>Read</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>X</td> <td>0</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>0</td> <td>Hold</td> </tr> </tbody> </table> <p> X : Irrelevant DOn : Output data DIn : Input data WEB : Write enable ADn : Address data REB : Read enable CSB : Chip select </p> <p>Caution WEB or CSB must be high during all address transition.</p>			DIn	ADn	CSB	WEB	REB	DOn	Operation	DIn	ADn	0	0	1	0	Write	DIn	ADn	0	0	0	DIn	Write , Read	X	ADn	0	1	0	DOn	Read	X	X	1	X	X	0	Hold	X	X	X	1	1	0	Hold																																																																																		
DIn	ADn	CSB	WEB	REB	DOn	Operation																																																																																																																								
DIn	ADn	0	0	1	0	Write																																																																																																																								
DIn	ADn	0	0	0	DIn	Write , Read																																																																																																																								
X	ADn	0	1	0	DOn	Read																																																																																																																								
X	X	1	X	X	0	Hold																																																																																																																								
X	X	X	1	1	0	Hold																																																																																																																								
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="3">Input</th> <th colspan="3">Output</th> <th colspan="4">Switching speed</th> </tr> <tr> <th>Name</th> <th>Symbol</th> <th>Fan-in</th> <th>Name</th> <th>Symbol</th> <th>Fan-out</th> <th colspan="2">Path</th> <th colspan="2">t_{LD0} (ns)</th> </tr> <tr> <th colspan="6"></th> <th>IN → OUT</th> <th>MIN.</th> <th>TYP.</th> <th>MAX.</th> </tr> </thead> <tbody> <tr> <td>H01</td> <td>DI0</td> <td>1.0</td> <td>N01</td> <td>DO0</td> <td>26.0</td> <td rowspan="2">AD0 to AD7 →DO0 to DO7</td> <td>(LH)</td> <td>2.323</td> <td>4.236</td> <td>7.357</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>(HH)</td> <td>2.323</td> <td>4.236</td> <td>7.357</td> </tr> <tr> <td>H08</td> <td>DI7</td> <td>1.0</td> <td>N08</td> <td>DO7</td> <td>26.0</td> <td rowspan="3">CSB →DO0 to DO7</td> <td>(HL)</td> <td>2.329</td> <td>4.282</td> <td>7.470</td> </tr> <tr> <td>H09</td> <td>AD0</td> <td>1.0</td> <td></td> <td></td> <td></td> <td>(LL)</td> <td>2.329</td> <td>4.282</td> <td>7.470</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td></td> <td></td> <td></td> <td>(LH)</td> <td>2.241</td> <td>4.054</td> <td>7.012</td> </tr> <tr> <td>H16</td> <td>AD7</td> <td>1.0</td> <td></td> <td></td> <td></td> <td rowspan="2">REB →DO0 to DO7</td> <td>(LH)</td> <td>0.538</td> <td>0.968</td> <td>1.669</td> </tr> <tr> <td>H17</td> <td>WEB</td> <td>1.0</td> <td></td> <td></td> <td></td> <td>(HL)</td> <td>0.420</td> <td>0.797</td> <td>1.413</td> </tr> <tr> <td>H18</td> <td>REB</td> <td>1.0</td> <td></td> <td></td> <td></td> <td rowspan="2">DI0 to DI7 →DO0 to DO7</td> <td>(HH)</td> <td>2.267</td> <td>4.190</td> <td>7.327</td> </tr> <tr> <td>H19</td> <td>CSB</td> <td>1.0</td> <td></td> <td></td> <td></td> <td>(LL)</td> <td>2.193</td> <td>4.045</td> <td>7.066</td> </tr> </tbody> </table>			Input			Output			Switching speed				Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)								IN → OUT	MIN.	TYP.	MAX.	H01	DI0	1.0	N01	DO0	26.0	AD0 to AD7 →DO0 to DO7	(LH)	2.323	4.236	7.357	:	:	:	:	:	:	(HH)	2.323	4.236	7.357	H08	DI7	1.0	N08	DO7	26.0	CSB →DO0 to DO7	(HL)	2.329	4.282	7.470	H09	AD0	1.0				(LL)	2.329	4.282	7.470	:	:	:				(LH)	2.241	4.054	7.012	H16	AD7	1.0				REB →DO0 to DO7	(LH)	0.538	0.968	1.669	H17	WEB	1.0				(HL)	0.420	0.797	1.413	H18	REB	1.0				DI0 to DI7 →DO0 to DO7	(HH)	2.267	4.190	7.327	H19	CSB	1.0				(LL)	2.193	4.045	7.066
Input			Output			Switching speed																																																																																																																								
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H19	CSB	1.0					(LL)	2.193	4.045	7.066																																																																																																																				
Equivalent Cells		160 x 37 = 5920		Power (mW/MHz)		Read cycle	0.055		Rev.	1																																																																																																																				
						Write cycle	0.069																																																																																																																							

BASIC RAM BLOCK

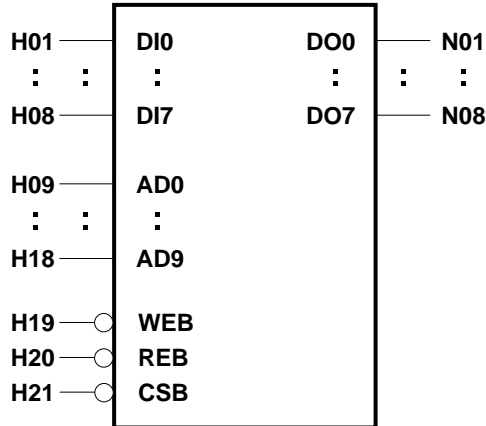
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.470		
Address access time	tACA			7.470
Address output hold time	tOH	2.006		
CSB access time	tCSC			7.012
CSB output hold time	tCSL	0.591		1.920
CSB output set time	tCLL	2.241		
REB access time	tREC			1.669
REB output hold time	tREL	0.420		1.413
REB output set time	tRLL	0.538		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.000		
CSB-WEB reset time	tCWR	3.400		
Write pulse width	tWP	3.400		
Address setup time	tAS	1.600		
Address hold time	tAH	0.000		
Input data setup time	tDS	3.600		
Input data hold time	tDH	0.000		
WEB access time	tWEC			5.454

BASIC RAM BLOCK

Block Type	Function	SSI Family
K18M	1024 words × 8 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DO _n	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DO _n	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
 DIn : Input data
 ADn : Address data
 CSB : Chip select
 DO_n : Output data
 WEB : Write enable
 REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DIO	1.0	N01	DO0	26.0	AD0 to AD9 →DO0 to DO7	(LH)	2.914	5.247	9.052
:	:	:	:	:	:		(HH)	2.914	5.247	9.052
H08	DI7	1.0	N08	DO7	26.0		(HL)	3.023	5.586	9.769
H09	AD0	1.0					(LL)	3.023	5.586	9.769
:	:	:				CSB →DO0 to DO7	(LL)	2.733	5.056	8.845
H18	AD9	1.0					(LH)	2.733	5.056	8.845
H19	WEB	1.0					(HL)	0.755	1.393	2.434
H20	REB	1.0				REB →DO0 to DO7	(LH)	0.670	1.169	1.982
H21	CSB	1.0					(HL)	0.559	1.064	1.887
						DI0 to DI7 →DO0 to DO7	(HH)	2.830	5.244	9.183
							(LL)	2.786	5.127	8.946
Equivalent Cells		316 x 69 = 21804		Power (mW/MHz)		Read cycle	0.068		Rev.	1
						Write cycle	0.097			

BASIC RAM BLOCK

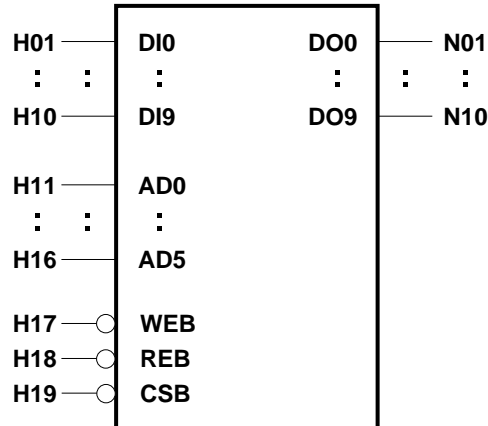
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.769		
Address access time	tACA			9.769
Address output hold time	tOH	2.006		
CSB access time	tCSC			8.845
CSB output hold time	tCSL	0.755		2.434
CSB output set time	tCLL	2.733		
REB access time	tREC			1.982
REB output hold time	tREL	0.559		1.887
REB output set time	tRLL	0.670		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.600		
CSB-WEB reset time	tCWR	4.400		
Write pulse width	tWP	4.400		
Address setup time	tAS	1.200		
Address hold time	tAH	0.000		
Input data setup time	tDS	4.600		
Input data hold time	tDH	0.000		
WEB access time	tWEC			7.037

BASIC RAM BLOCK

Block Type	Function	SSI Family
K1AB	64 words × 10 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant
 DIn : Input data
 ADn : Address data
 CSB : Chip select
 DOn : Output data
 WEB : Write enable
 REB : Read enable

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD5 →DO0 to DO9	(LH)	2.097	3.877	6.782
:	:	:	:	:	:		(HH)	2.097	3.877	6.782
H10	DI9	1.0	N10	DO9	26.0	CSB →DO0 to DO9	(HL)	2.027	3.773	6.620
H11	AD0	1.0					(LL)	2.027	3.773	6.620
:	:	:					(LH)	1.936	3.576	6.252
H16	AD5	1.0				REB →DO0 to DO9	(LH)	1.936	3.576	6.252
H17	WEB	1.0					(HL)	0.588	1.052	1.810
H18	REB	1.0				DI0 to DI9 →DO0 to DO9	(LH)	0.505	0.886	1.508
H19	CSB	1.0					(HL)	0.399	0.710	1.216
						(HH)	1.347	2.529	4.457	
						(LL)	1.252	2.299	4.008	
Equivalent Cells		116 x 21 = 2436		Power (mW/MHz)		Read cycle	0.029		Rev.	1
						Write cycle	0.040			

BASIC RAM BLOCK

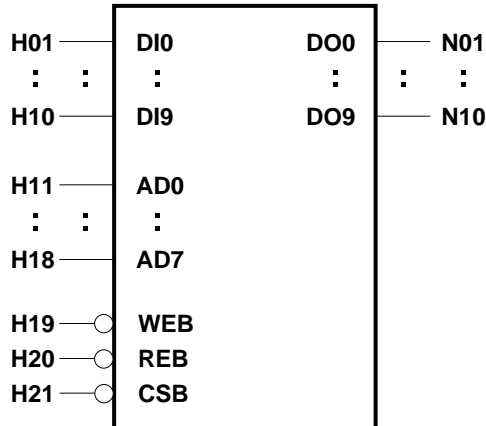
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.782		
Address access time	tACA			6.782
Address output hold time	tOH	2.027		
CSB access time	tCSC			6.252
CSB output hold time	tCSL	0.588		1.810
CSB output set time	tCLL	1.936		
REB access time	tREC			1.508
REB output hold time	tREL	0.399		1.216
REB output set time	tRLL	0.505		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	4.600		
CSB-WEB reset time	tCWR	3.300		
Write pulse width	tWP	3.300		
Address setup time	tAS	1.300		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.000		
Input data hold time	tDH	0.000		
WEB access time	tWEC			4.073

BASIC RAM BLOCK

Block Type	Function	SSI Family
K1AF	256 words × 10 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DOn	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DOn	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant DOn : Output data
 DIn : Input data WEB : Write enable
 ADn : Address data REB : Read enable
 CSB : Chip select

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD7 →DO0 to DO9	(LH)	2.353	4.389	7.711
:	:	:	:	:	:		(HH)	2.353	4.389	7.711
H10	DI9	1.0	N10	DO9	26.0		(HL)	2.370	4.370	7.632
H11	AD0	1.0					(LL)	2.370	4.370	7.632
H18	AD7	1.0				CSB →DO0 to DO9	(LL)	2.335	4.237	7.341
H19	WEB	1.0					(LH)	2.335	4.237	7.341
H20	REB	1.0					(HL)	0.669	1.203	2.075
H21	CSB	1.0				REB →DO0 to DO9	(LH)	0.560	1.021	1.773
							(HL)	0.442	0.866	1.557
						DI0 to DI9 →DO0 to DO9	(HH)	2.268	4.202	7.359
							(LL)	2.244	4.095	7.114
Equivalent Cells		198 x 37 = 7326		Power (mW/MHz)		Read cycle	0.067		Rev.	1
						Write cycle	0.097			

BASIC RAM BLOCK

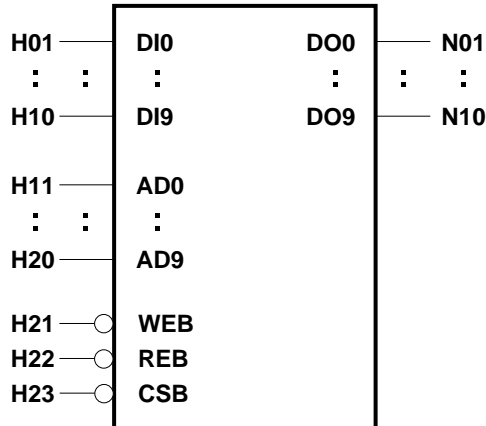
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	7.711		
Address access time	tACA			7.711
Address output hold time	tOH	2.027		
CSB access time	tCSC			7.341
CSB output hold time	tCSL	0.669		2.075
CSB output set time	tCLL	2.335		
REB access time	tREC			1.773
REB output hold time	tREL	0.442		1.557
REB output set time	tRLL	0.560		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.000		
CSB-WEB reset time	tCWR	3.400		
Write pulse width	tWP	3.400		
Address setup time	tAS	1.600		
Address hold time	tAH	0.000		
Input data setup time	tDS	3.600		
Input data hold time	tDH	0.000		
WEB access time	tWEC			5.593

BASIC RAM BLOCK

Block Type	Function	SSI Family
K1AM	1024 words × 10 bits Single-port RAM	

Logic Diagram



Truth Table

DIn	ADn	CSB	WEB	REB	DO _n	Operation
DIn	ADn	0	0	1	0	Write
DIn	ADn	0	0	0	DIn	Write , Read
X	ADn	0	1	0	DO _n	Read
X	X	1	X	X	0	Hold
X	X	X	1	1	0	Hold

X : Irrelevant DO_n : Output data
 DIn : Input data WEB : Write enable
 ADn : Address data REB : Read enable
 CSB : Chip select

Caution WEB or CSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		t _{LD0} (ns)		
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	AD0 to AD9 →DO0 to DO9	(LH)	2.975	5.388	9.325
:	:	:	:	:	:		(HH)	2.975	5.388	9.325
H10	DI9	1.0	N10	DO9	26.0		(HL)	3.128	5.783	10.110
:	:	:					(LL)	3.128	5.783	10.110
H20	AD9	1.0				CSB →DO0 to DO9	(LL)	2.907	5.229	9.017
H21	WEB	1.0					(LH)	2.907	5.229	9.017
H22	REB	1.0					(HL)	0.838	1.533	2.669
H23	CSB	1.0				REB →DO0 to DO9	(LH)	0.766	1.313	2.205
							(HL)	0.638	1.172	2.042
						DI0 to DI9 →DO0 to DO9	(HH)	2.831	5.226	9.134
							(LL)	2.776	5.150	9.023
Equivalent Cells		392 x 69 = 27048		Power (mW/MHz)		Read cycle	0.082		Rev.	1
						Write cycle	0.118			

BASIC RAM BLOCK

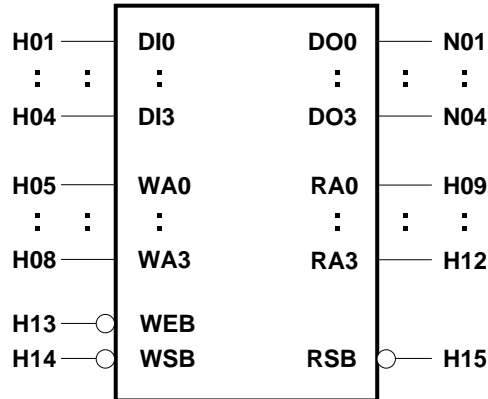
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	10.110		
Address access time	tACA			10.110
Address output hold time	tOH	2.027		
CSB access time	tCSC			9.017
CSB output hold time	tCSL	0.838		2.669
CSB output set time	tCLL	2.907		
REB access time	tREC			2.205
REB output hold time	tREL	0.638		2.042
REB output set time	tRLL	0.766		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.000		
CSB-WEB reset time	tCWR	4.400		
Write pulse width	tWP	4.400		
Address setup time	tAS	1.400		
Address hold time	tAH	0.000		
Input data setup time	tDS	4.600		
Input data hold time	tDH	0.000		
WEB access time	tWEC			7.269

BASIC RAM BLOCK

Block Type	Function	SSI Family
K247	16words × 4 bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)		
H01	DI0	1.0	N01	DO0	26.0	IN → OUT		MIN.	TYP.	MAX.
:	:	:	:	:	:					
H04	DI3	1.0	N04	DO3	26.0	RA0 to RA3 (LH)	0.980	1.645	2.728	
H05	WA0	1.0				→DO0 to DO3 (HH)	0.980	1.645	2.728	
:	:	:				(HL)	0.982	1.796	3.125	
H08	WA3	1.0				(LL)	0.982	1.796	3.125	
H09	RA0	1.0				RSB (LH)	0.275	0.460	0.762	
:	:	:				→DO0 to DO3 (HL)	0.219	0.369	0.613	
H12	RA3	1.0								
H13	WEB	1.0				DI0 to DI3 (HH)	1.394	2.338	3.880	
H14	WSB	1.0				→DO0 to DO3 (LL)	1.183	2.168	3.776	
H15	RSB	1.0								
Equivalent Cells		58 x 11 = 638		Power (mW/MHz)		Read cycle	0.016		Rev.	1
						Write cycle	0.023			

BASIC RAM BLOCK

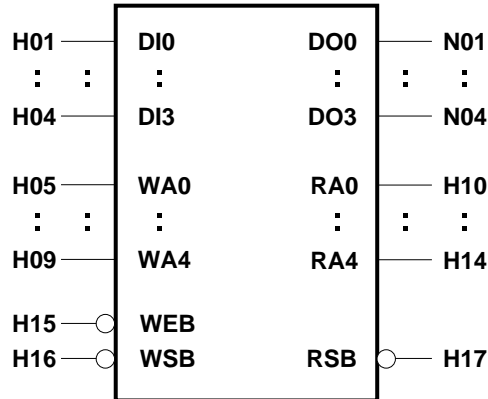
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	3.125		
Address access time	tACA			3.125
Address output hold time	tOH	0.980		
REB access time	tREC			0.762
REB output hold time	tREL	0.219		0.613
REB output set time	tRLL	0.275		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	4.000		
CSB-WEB reset time	tCWR	2.200		
Write pulse width	tWP	2.200		
Address setup time	tAS	1.800		
Address hold time	tAH	0.000		
Input data setup time	tDS	1.600		
Input data hold time	tDH	0.100		
WEB access time	tWEC			4.562

BASIC RAM BLOCK

Block Type	Function	SSI Family
K249	32 words × 4 bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed						
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)				
						IN	→	OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	RA0 to RA4 (LH) →DO0 to DO3 (HH)		1.051	1.753	2.899		
⋮	⋮	⋮	⋮	⋮	⋮			⋮	⋮	⋮	⋮	
H04	DI3	1.0	N04	DO3	26.0			RSB (LH) →DO0 to DO3 (HL)		0.281	0.479	0.801
H05	WA0	1.0								0.235	0.411	0.698
⋮	⋮	⋮				DI0 to DI3 (HH) →DO0 to DO3 (LL)		1.194	2.050	3.446		
H09	WA4	1.0						1.095	2.056	3.624		
H10	RA0	1.0										
⋮	⋮	⋮										
H14	RA4	1.0										
H15	WEB	1.0										
H16	WSB	1.0										
H17	RSB	1.0										
Equivalent Cells		106 x 11 = 1166		Power (mW/MHz)		Read cycle		0.020		Rev.	1	
						Write cycle		0.030				

BASIC RAM BLOCK

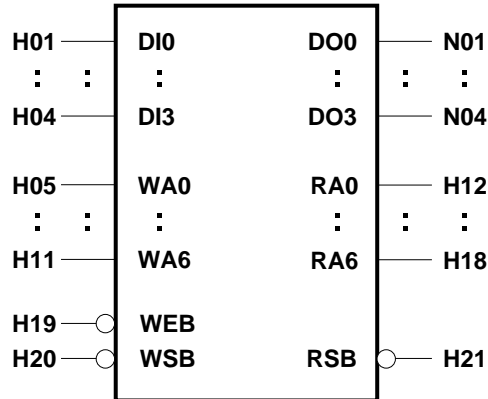
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	3.506		
Address access time	tACA			3.506
Address output hold time	tOH	1.051		
REB access time	tREC			0.801
REB output hold time	tREL	0.235		0.698
REB output set time	tRLL	0.281		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	4.600		
CSB-WEB reset time	tCWR	2.600		
Write pulse width	tWP	2.600		
Address setup time	tAS	2.000		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.600		
Input data hold time	tDH	0.000		
WEB access time	tWEC			4.881

BASIC RAM BLOCK

Block Type	Function	SSI Family
K24D	128 words × 4 bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)			
H01	DI0	1.0	N01	DO0	26.0	IN → OUT		MIN.	TYP.	MAX.	
⋮	⋮	⋮	⋮	⋮	⋮						
H04	DI3	1.0	N04	DO3	26.0	RA0 to RA6 (LH)		1.287	2.197	3.680	
H05	WA0	1.0				→DO0 to DO3 (HH)		1.287	2.197	3.680	
⋮	⋮	⋮				(HL)		1.301	2.432	4.277	
H11	WA6	1.0				(LL)		1.301	2.432	4.277	
H12	RA0	1.0				RSB (LH)		0.283	0.505	0.866	
⋮	⋮	⋮				→DO0 to DO3 (HL)		0.315	0.485	0.764	
H18	RA6	1.0				(HH)		1.717	2.913	4.864	
H19	WEB	1.0				(LL)		1.541	2.814	4.892	
H20	WSB	1.0									
H21	RSB	1.0									
Equivalent Cells		208 x 18 = 3744		Power (mW/MHz)		Read cycle		0.028		Rev.	1
						Write cycle		0.040			

BASIC RAM BLOCK

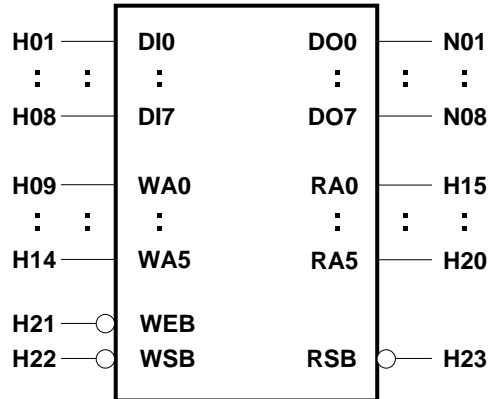
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	4.277		
Address access time	tACA			4.277
Address output hold time	tOH	1.287		
REB access time	tREC			0.866
REB output hold time	tREL	0.315		0.764
REB output set time	tRLL	0.283		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.400		
CSB-WEB reset time	tCWR	2.800		
Write pulse width	tWP	2.800		
Address setup time	tAS	2.600		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.700		
Input data hold time	tDH	0.000		
WEB access time	tWEC			5.463

BASIC RAM BLOCK

Block Type	Function	SSI Family
K28B	64 words × 8bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)		
H01	DI0	1.0	N01	DO0	26.0	IN → OUT		MIN.	TYP.	MAX.
:	:	:	:	:	:					
H08	DI7	1.0	N08	DO7	26.0	RA0 to RA5 (LH) →DO0 to DO7 (HH) (HL) (LL)		1.278	2.156	3.589
H09	WA0	1.0						1.278	2.156	3.589
:	:	:						1.233	2.366	4.213
H14	WA5	1.0						1.233	2.366	4.213
H15	RA0	1.0				RSB (LH) →DO0 to DO7 (HL)		0.370	0.603	0.983
:	:	:						0.324	0.552	0.925
H20	RA5	1.0				DI0 to DI7 (HH) →DO0 to DO7 (LL)		1.695	2.825	4.668
H21	WEB	1.0						1.498	2.743	4.774
H22	WSB	1.0								
H23	RSB	1.0								
Equivalent Cells		208 x 15 = 3120		Power (mW/MHz)		Read cycle	0.041		Rev.	1
						Write cycle	0.054			

BASIC RAM BLOCK

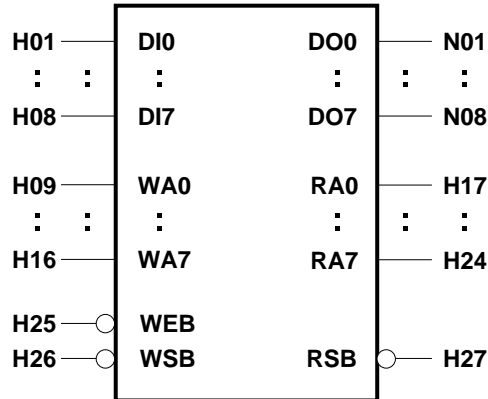
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	4.213		
Address access time	tACA			4.213
Address output hold time	tOH	1.233		
REB access time	tREC			0.983
REB output hold time	tREL	0.324		0.925
REB output set time	tRLL	0.370		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.500		
CSB-WEB reset time	tCWR	2.800		
Write pulse width	tWP	2.800		
Address setup time	tAS	2.700		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.400		
Input data hold time	tDH	0.000		
WEB access time	tWEC			5.450

BASIC RAM BLOCK

Block Type	Function	SSI Family
K28F	256 words × 8bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed									
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)							
						IN	→	OUT	MIN.	TYP.	MAX.				
H01	DI0	1.0	N01	DO0	26.0	RA0 to RA7 →DO0 to DO7	(LH)		1.774	3.014	5.036				
:	:	:	:	:	:							(HH)	1.774	3.014	5.036
H08	DI7	1.0	N08	DO7	26.0	RSB →DO0 to DO7	(HL)		1.880	3.400	5.879				
H09	WA0	1.0										(LL)	1.880	3.400	5.879
:	:	:													
H16	WA7	1.0				DI0 to DI7 →DO0 to DO7	(HH)		1.801	3.060	5.114				
H17	RA0	1.0										(LL)	1.609	2.960	5.163
:	:	:													
H24	RA7	1.0													
H25	WEB	1.0													
H26	WSB	1.0													
H27	RSB	1.0													
Equivalent Cells		400 x25 = 10000		Power (mW/MHz)		Read cycle	0.091		Rev.	1					
						Write cycle	0.124								

BASIC RAM BLOCK

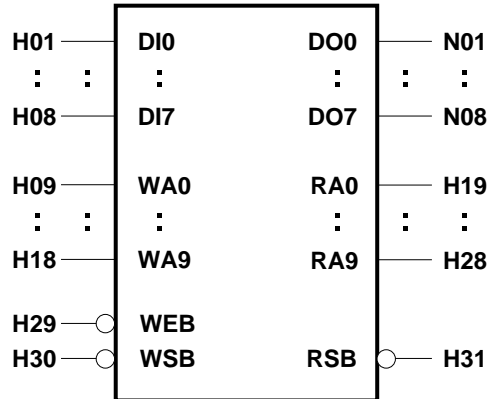
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	5.879		
Address access time	tACA			5.879
Address output hold time	tOH	1.774		
REB access time	tREC			1.169
REB output hold time	tREL	0.416		1.105
REB output set time	tRLL	0.392		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.000		
CSB-WEB reset time	tCWR	3.400		
Write pulse width	tWP	3.400		
Address setup time	tAS	2.600		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.200		
Input data hold time	tDH	0.000		
WEB access time	tWEC			6.644

BASIC RAM BLOCK

Block Type	Function	SSI Family
K28M	1024 words × 8bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed					
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)			
H01	DI0	1.0	N01	DO0	26.0	IN → OUT		MIN.	TYP.	MAX.	
⋮	⋮	⋮	⋮	⋮	⋮						
H08	DI7	1.0	N08	DO7	26.0	RA0 to RA9 (LH) →DO0 to DO7 (HH)		2.481	4.142	6.852	
H09	WA0	1.0						(HL)	2.685	4.941	8.621
⋮	⋮	⋮						(LL)	2.685	4.941	8.621
H18	WA9	1.0									
H19	RA0	1.0				RSB →DO0 to DO7		(LH)	0.479	0.785	1.285
⋮	⋮	⋮						(HL)	0.430	0.724	1.205
H28	RA9	1.0				DI0 to DI7 →DO0 to DO7		(HH)	2.175	3.676	6.127
H29	WEB	1.0						(LL)	1.876	3.484	6.107
H30	WSB	1.0									
H31	RSB	1.0									
Equivalent Cells		784 × 47 = 36848		Power (mW/MHz)		Read cycle	0.105		Rev.	1	
						Write cycle	0.159				

BASIC RAM BLOCK

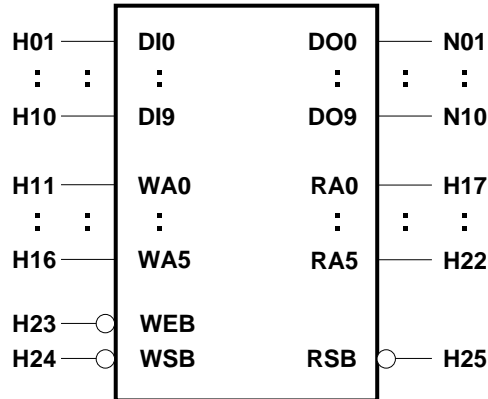
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	8.621		
Address access time	tACA			8.621
Address output hold time	tOH	2.480		
REB access time	tREC			1.285
REB output hold time	tREL	0.430		1.205
REB output set time	tRLL	0.479		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	7.400		
CSB-WEB reset time	tCWR	4.800		
Write pulse width	tWP	4.800		
Address setup time	tAS	2.600		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.600		
Input data hold time	tDH	0.000		
WEB access time	tWEC			9.006

BASIC RAM BLOCK

Block Type	Function	SSI Family
K2AB	64 words × 10bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)		
H01	DI0	1.0	N01	DO0	26.0	IN → OUT		MIN.	TYP.	MAX.
:	:	:	:	:	:					
H10	DI9	1.0	N10	DO9	26.0	RA0 to RA5 →DO0 to DO9	(LH)	1.296	2.189	3.645
H11	WA0	1.0					(HH)	1.296	2.189	3.645
:	:	:					(HL)	1.316	2.495	4.419
H16	WA5	1.0					(LL)	1.316	2.495	4.419
H17	RA0	1.0				RSB →DO0 to DO9	(LH)	0.380	0.636	1.053
:	:	:					(HL)	0.363	0.613	1.022
H22	RA5	1.0				DI0 to DI9 →DO0 to DO9	(HH)	1.695	2.825	4.669
H23	WEB	1.0					(LL)	1.498	2.743	4.773
H24	WSB	1.0								
H25	RSB	1.0								
Equivalent Cells		256x 15 = 3840		Power (mW/MHz)		Read cycle	0.050		Rev.	1
						Write cycle	0.065			

BASIC RAM BLOCK

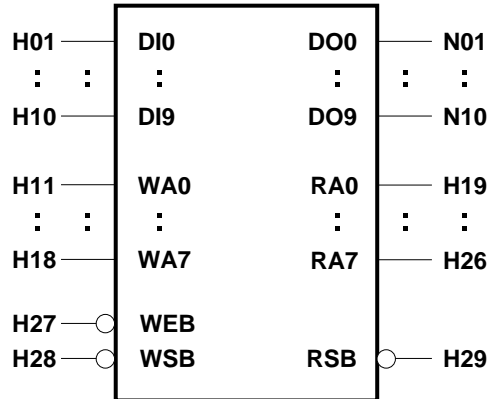
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	4.419		
Address access time	tACA			4.419
Address output hold time	tOH	1.498		
REB access time	tREC			1.053
REB output hold time	tREL	0.363		1.022
REB output set time	tRLL	0.380		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	5.700		
CSB-WEB reset time	tCWR	2.900		
Write pulse width	tWP	2.900		
Address setup time	tAS	2.800		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.300		
Input data hold time	tDH	0.000		
WEB access time	tWEC			5.841

BASIC RAM BLOCK

Block Type	Function	SSI Family
K2AF	256words × 10bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path	tLD0 (ns)			
						IN → OUT	MIN.	TYP.	MAX.	
H01	DI0	1.0	N01	DO0	26.0	RA0 to RA7 (LH) →DO0 to DO9 (HH) (HL) (LL)	1.840	3.074	5.087	
:	:	:	:	:	:		1.840	3.074	5.087	
H10	DI9	1.0	N10	DO9	26.0		1.985	3.629	6.311	
:	:	:	:	:	:		1.985	3.629	6.311	
H11	WA0	1.0				RSB (LH) →DO0 to DO9 (HL)	0.474	0.790	1.305	
:	:	:					0.493	0.771	1.226	
H18	WA7	1.0				DI0 to DI9 (HH) →DO0 to DO9 (LL)	1.793	3.052	5.105	
H19	RA0	1.0					1.614	2.963	5.163	
:	:	:								
H26	RA7	1.0								
H27	WEB	1.0								
H28	WSB	1.0								
H29	RSB	1.0								
Equivalent Cells		496x 25 = 12400		Power (mW/MHz)		Read cycle	0.109		Rev.	1
						Write cycle	0.147			

BASIC RAM BLOCK

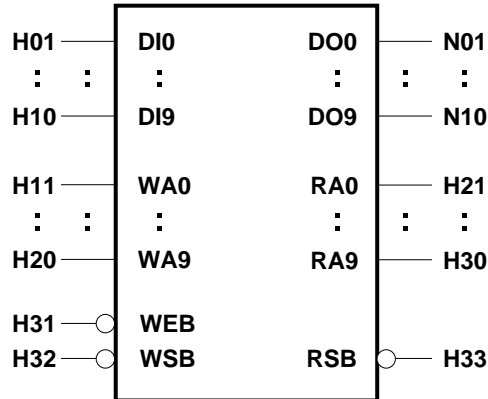
Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	6.311		
Address access time	tACA			6.311
Address output hold time	tOH	1.839		
REB access time	tREC			1.305
REB output hold time	tREL	0.493		1.226
REB output set time	tRLL	0.474		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	6.800		
CSB-WEB reset time	tCWR	3.800		
Write pulse width	tWP	3.800		
Address setup time	tAS	3.000		
Address hold time	tAH	0.000		
Input data setup time	tDS	2.200		
Input data hold time	tDH	0.000		
WEB access time	tWEC			7.229

BASIC RAM BLOCK

Block Type	Function	SSI Family
K2AM	1024words × 10bits Dual-port RAM	

Logic Diagram



Truth Table

DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn
X	X	1	X	Hold	X	X	X
X	X	0	1	Hold	X	X	X
DIn	WAn	0	0	DIn(WAn)	X	X	X
X	X	X	X	X	X	1	0
X	X	1	1	DMn	RAn	0	DMn(RAn)
DIn	WAn	0	0	DIn(WAn)	RAn	0	DMn(RAn)

X : Irrelevant	DIn : Input data
WAn : A-port address (Write)	WSB : A-port select
WEB : Write enable	DMn : Memory data
RAn : B-port address (Read)	RSB : B-port select
DOn : Output data	

Caution WEB or WSB must be high during all address transition.

Input			Output			Switching speed				
Name	Symbol	Fan-in	Name	Symbol	Fan-out	Path		tLD0 (ns)		
H01	DI0	1.0	N01	DO0	26.0	IN → OUT		MIN.	TYP.	MAX.
:	:	:	:	:	:					
H10	DI9	1.0	N10	DO9	26.0	RA0 to RA9 (LH)	2.589	4.386	7.317	
H11	WA0	1.0				→DO0 to DO9 (HH)	2.589	4.386	7.317	
:	:	:				(HL)	2.894	5.337	9.324	
H20	WA9	1.0				(LL)	2.894	5.337	9.324	
H21	RA0	1.0				RSB (LH)	0.484	0.832	1.401	
:	:	:				→DO0 to DO9 (HL)	0.509	0.833	1.363	
H30	RA9	1.0								
H31	WEB	1.0				DI0 to DI9 (HH)	2.174	3.678	6.131	
H32	WSB	1.0				→DO0 to DO9 (LL)	1.876	3.484	6.107	
H33	RSB	1.0								
Equivalent Cells		976x 47 = 45872		Power (mW/MHz)		Read cycle	0.123		Rev.	1
						Write cycle	0.194			

BASIC RAM BLOCK

Read Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tRCA	9.324		
Address access time	tACA			9.324
Address output hold time	tOH	2.589		
REB access time	tREC			1.401
REB output hold time	tREL	0.509		1.363
REB output set time	tRLL	0.484		

Write Cycle Timing (ns)				
Parameters	Symbols	MIN.	TYP.	MAX.
Cycle time	tWC	8.400		
CSB-WEB reset time	tCWR	5.600		
Write pulse width	tWP	5.600		
Address setup time	tAS	2.800		
Address hold time	tAH	0.000		
Input data setup time	tDS	3.200		
Input data hold time	tDH	0.100		
WEB access time	tWEC			9.778

[MEMO]

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