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RENESAS

Design Manual

CMOS-9HD Series

CMOS Gate Array

Ver. 9.0

Document No. A12985EJ9V0DM00 (9th edition)
Date Published December 2009 NS

[MEMO]

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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(M8E0909E)

Major Revisions in This Edition

Page	Description
Throughout	Delection of μPD66943, 66944, 65969, 65970, and 65971.
p.46	Modification of **2.3.1 (3) No connection (NC) pins**.
p.46	Modification of **2.3.1 (5) Digital PLL (digital phase locked loop) pin placement**.
p.54	Modification of **2.7 List of Interface Data**.
pp.55 to 96 (previous edition)	Delection of **2.8 ASIC Product Development Information**.
p.56	Modification of **Table 3-4. Absolute Maximum Rating Values**.
p.64	Modification of **Table 3-10. Capacitance of Packages (C_P)**.
pp.275 to 285 (previous edition)	Delection of **7.7 SSCG**.

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

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INTRODUCTION

This manual explains the limits and points to be noted when designing LSIs using NEC Electronics' CMOS-9HD Series high-speed, high-density CMOS gate arrays.

Thoroughly read this manual to ensure smooth LSI design.

Be sure to observe the items (general items, cautions, and limitations) described in this manual; otherwise, the quality and performance of the LSI may be affected and the operation of the LSI may be abnormal.

The following abbreviations are used for the package names in this manual.

Abbreviation	Standard Package Name
QFP	Plastic QFP
PBGA	Plastic BGA
FPBGA®	Fine pitch plastic BGA

Target Readers This manual is intended for user engineers who wish to design an LSI using the CMOS-9HD Series.

Purpose This manual explains general information, limitations, and points to be noted when designing an LSI using the CMOS-9HD Series.

How to Read This Manual It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcomputers.

- To understand the overall functions of the CMOS-9HD Series:
  → Read this manual in the order of the contents.

See **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)** for the following items.

- List of packages
- Maximum allowable power consumption
- Thermal resistance
- Assignment of V_{DD}, GND, NC, SCAN test pins
- Pins that can be used for oscillators
- Package drawings
- Package markings
- Mounting rank (Recommended soldering conditions)

Conventions

Note: Footnote for item marked with **Note** in the text
Caution: Information requiring particular attention
Remark: Supplementary information

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

• CMOS-9HD Series Design Manual	(This manual)
• CMOS-9HD Series, EA-9HD Series Block Library	(A13052E)
• CMOS-9HD Series, EA-9HD Series Memory Block Library	(A13071E)
• CMOS-9HD Series Megamacro Design Manual	(A13941E)
• CMOS Gate Array, Embedded Array Package Design Manual	(A16400E)
• SYSTEM LSI DESIGN OPENCAD™ OPC_VSHELL User's Manual	(A16306E)
• SYSTEM LSI DESIGN OPENCAD Static Timing Analyzer Tiara User's Manual	(A16210E)
• SYSTEM LSI DESIGN Design For Test TESTACT, NEC_SCAN2 User's Manual	(A16437E)
• SYSTEM LSI DESIGN Design For Test SCAN Tool Interface User's Manual	(A14964E)
• SYSTEM LSI DESIGN Design For Test NEC_BIST, NEC_TESTBUS, NEC_SCAN/SCAN2, NEC_BSCAN/BSCAN2 User's Manual	(A15168E)
• SEMICONDUCTOR SELECTION GUIDE -Products and Packages-	(X13769X)

CONTENTS

LIST OF FIGURES (1/4)

LIST OF FIGURES (2/4)

LIST OF FIGURES (3/4)

LIST OF FIGURES (4/4)

LIST OF TABLES (1/2)

LIST OF TABLES (1/2)

CHAPTER 1 OVERVIEW

1.1 Features

The CMOS-9HD Series features are shown below.

High-speed operation	t_{PD} = 94 ps	(2-input NAND, fan-outs: 1, wiring length: 0 mm)
	t_{PD} = 131 ps	(2-input NAND, fan-outs: 1, standard wiring length)
	t_{PD} = 108 ps	(2-input NAND, standard load)
	t_{PD} = 107 ps	(2-input NAND (power gate), fan-outs: 1, standard wiring length)
	t_{PD} = 94 ps	(2-input NAND (power gate), standard load)
	t_{PD} = 229 ps	(input buffer, fan-outs: 1, standard wiring length)
	t_{PD} = 222 ps	(input buffer, standard load)
	t_{PD} = 1,396 ps	(output buffer, C_L = 15 pF, I_{OL} = 18 mA)
Maximum clock frequency	$f_{MAX.}$ = 670 MHz (internal toggle F/F, fan-outs: 2)	
Very large-scale integration (VLSI)	15 K to 2.5 M gates	
Technology	0.35 μm rule Si gates, 3-layer metalization, 4-layer metalization	
Input interface	LVTTL compatible	
Internal blocks	More than 190 types of function blocks Includes high-speed/low power; compatible with CMOS-8L Series Scan path block Driver for clock tree synthesis	
Memory blocks	High-density single-port RAM High-density dual-port RAM Compiled high-speed RAM ROM	

Variety of peripheral blocks	LVTTL input/5 V tolerant input buffer LVTTL input buffer with fail-safe function 5 V tolerant output buffer for CMOS TTL 5 V tolerant output buffer LVTTL output buffer Buffer for PCI bus specification High drive capability buffer (I_{OL} = 24.0 mA) Low-noise output buffer Buffer with internal pull-up resistor (5 kΩ/50 kΩ) Buffer with internal pull-down resistor (50 kΩ) Clock driver dedicated input block Digital PLL (for phase control) Digital PLL (for multiplication) GTL+

Caution It must be noted that there are buffers in which placement cannot be performed due to the master. For the details, refer to 2.4 I/O Interface and 7.1 LVTTL and 5 V Tolerant Blocks.

Power consumption	0.16 μW/MHz/cell (internal gate, operating factor: 0.3)
Power supply voltage	3.3 ±0.3 V
Other	High latch-up immunity EMI noise reduction design (contact NEC Electronics for details)

1.2 CMOS-9HD Series Products

<R>

Table 1-1. Products

(a) 3-layer routing products

Master	Number of Row Gates	Number of Usable Gates
μPD65941,	14,942	11,207
μPD65942, 66942	37,338	28,004
μPD65943	75,740	53,018
μPD65944	100,602	70,421
μPD65945	128,338	89,836
μPD65946	202,630	141,841
μPD65948	312,684	218,879
μPD65949	437,136	262,281
μPD65951	585,390	321,964
μPD65954	835,664	459,615
μPD65956	1,096,452	603,048
μPD65958	1,015,646	807,823

Remark Total number of gates integrated on the chip in terms of 2-input NAND (1 cell = 1 gate)
Usable cell rate: μPD65941, 65942, 66942 ..... 75%
μPD65943, 65944, 65945, 65946, 65948 ..... 70%
μPD65949 ..... 60%
μPD65951, 65954, 65956 ..... 55%
μPD65958 ..... 50%

(b) 4-layer routing products

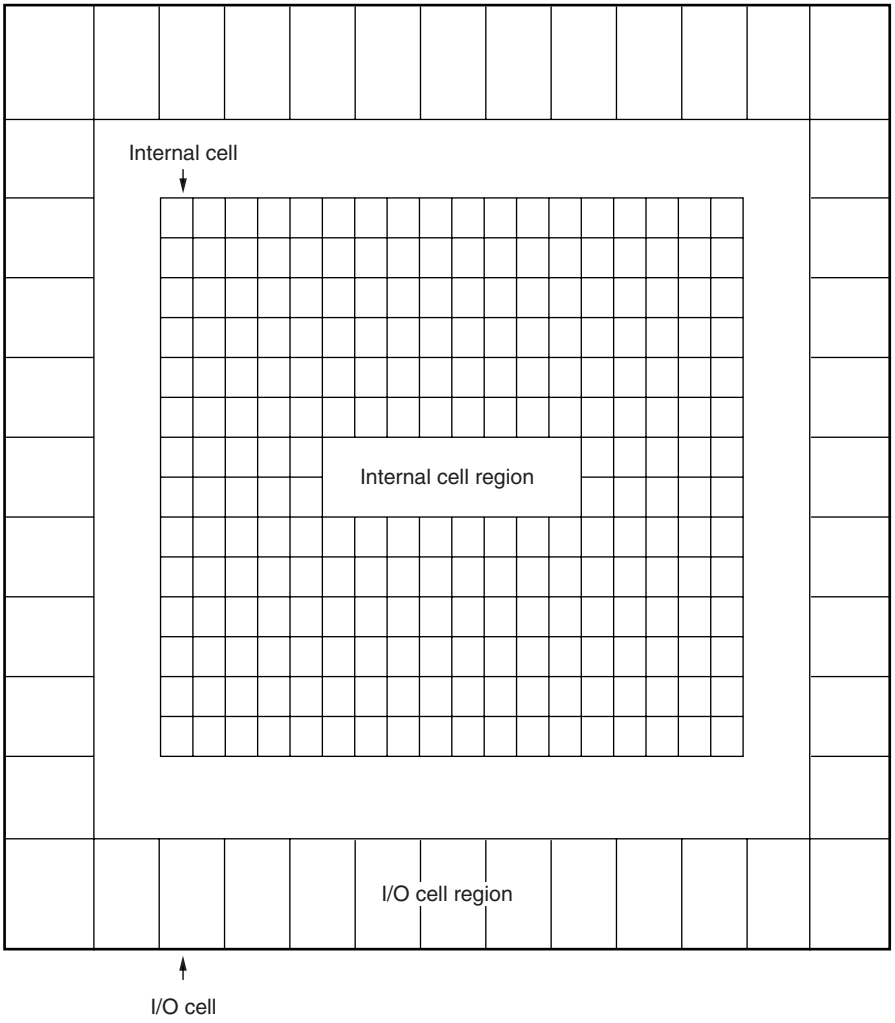
Master	Number of Row Gates	Number of Usable Gates
μPD65961	585,390	380,503
μPD65964	835,664	543,181
μPD65966	1,096,452	712,693
μPD65968	1,615,646	969,387

Remark Total number of gates integrated on the chip in terms of 2-input NAND (1 cell = 1 gate)
Usable cell rate: μPD65961, 65964, 65966 ..... 65%
μPD65968 ..... 60%

1.3 Internal Structure of CMOS-9HD Series

Figure 1-1 shows the internal structure of CMOS-9HD Series, which is comprised of an internal cell region and an outer I/O cell region.

Figure 1-1. Gate Array Configuration



As shown in Figure 1-1, the CMOS-9HD Series does not have fixed routing regions in the internal cell region, and the entire surface of the internal cell region is filled with basic cells.

The internal cell region consists of various function blocks (such as NAND gates and D-F/F) and memory that are connected via routing layers to implement the desired circuit functions.

Input and output buffers are placed in the I/O cell region, and are used to adjust the input-level conversion and output drive capability. Some internal cells are also part of the I/O buffer implementation.

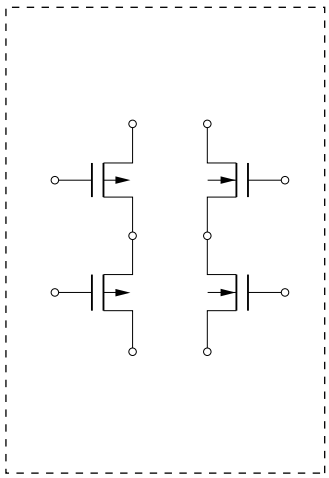
1.4 Internal Cell Structure

Figure 1-2 represents a CMOS-9HD Series internal cell equivalent circuit.

Each cell of the CMOS-9HD Series can be configured as a device such as a two-input NAND/NOR gate, an inverter, or a buffer.

A CMOS circuit consists of a P-channel MOS transistor (P-Ch.Tr) and an N-channel MOS transistor (N-Ch.Tr). Normally, either the P-Ch.Tr or the N-Ch.Tr is in the OFF state.

Figure 1-2. Internal Cell Equivalent Circuit



Because virtually no power flows in the steady state, power consumption for a CMOS circuit is extremely low.

A CMOS circuit consumes current mostly during switching. Because a high transient current flows during switching, a high-speed capacitor with a high capacitance must be inserted between the power supply and ground, or the impedance of the power supply lowered.

In addition, if a waveform with a slow rise/fall time is applied to a CMOS circuit, both the P-Ch.Tr and N-Ch.Tr will remain in the ON state for a period of time, causing a through current to flow between the P-Ch.Tr and N-Ch.Tr. Consequently, the current consumption increases, and may cause malfunctioning.

Figure 1-3 (a) and (b) shows the equivalent circuits of a 2-input NOR gate and a 2-input NAND gate. Because the ON resistance of the N-Ch.Tr is about fifty percent less than that of the P-Ch.Tr, a large current can be sent through the N-Ch.Tr.

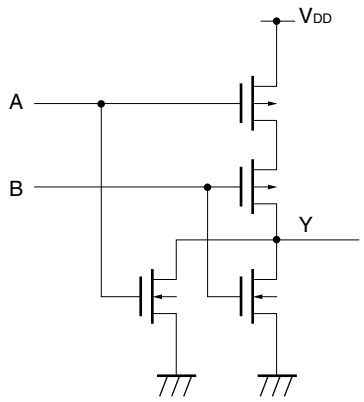
Therefore, as shown in Figure 1-3 (a), the ON resistance of the output rise side at the NOR gate, which is serially connected to the P-Ch.Tr, becomes larger, and the drive capability of the load drops.

In CMOS gate arrays, the NOR fan-out drive is slower than the NAND fan-out drive. Because of this, the NAND blocks should be used as much as possible to increase the speed and stability of the circuit.

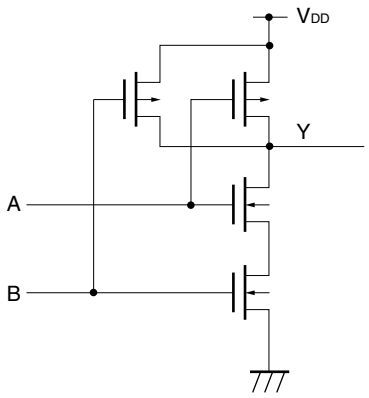
For the same reason, complex gates that serially connect many transistors tend to be slow, and therefore should not be used in high-speed circuits. You may use complex gates when speed is not as important to improve cell utilization.

Figure 1-3. Equivalent Circuits

(a) 2-input NOR equivalent circuit



(b) 2-input NAND equivalent circuit



1.5 3.3 V and 5 V I/O Interface

Low-voltage implementations for microprocessors and memories have advanced in recent years.

Ultramicroscopic fabrication of transistors and low-voltage design have proved essential for these high-speed, low-power LSIs. The CMOS-9HD Series, which uses leading-edge transistor fabrication techniques, has a standard power supply voltage of 3.3 V. Not all LSIs, however, support a standard power supply voltage of 3.3 V. Therefore, the CMOS-9HD Series is provided with an interface block capable of connection with conventional 5 V LSIs.

Because the LVTTL input block of the CMOS-9HD Series inputs 3.3 V signals, it cannot receive 5 V signals. The 5 V signals are received by a 5 V tolerant input block. Assuming that the power supply voltage of future gate array peripheral circuits will be 3.3 V, this 5 V tolerant input block can also receive 3.3 V signals. In addition, the LVTTL input block is also available with a fail-safe function that can be used for hot insertion and removal.

For output buffers, the high output level of the LVTTL output block is the same as for the conventional gate array V_{DD}. In addition, a 5 V tolerant output block is also available. The 5 V tolerant output block differs from the conventional one in that it can pull up a pin at 5 V, which is higher than the LSI power supply voltage. It therefore becomes possible to connect the pin to a 5 V bus line. See **7.1 LVTTL and 5 V Tolerant Blocks** for details of each block.

1.6 Packages

This Series is provided with a variety of packages such as QFP (Quad Flat Package), BGA (Ball Grid Array) and other packages.

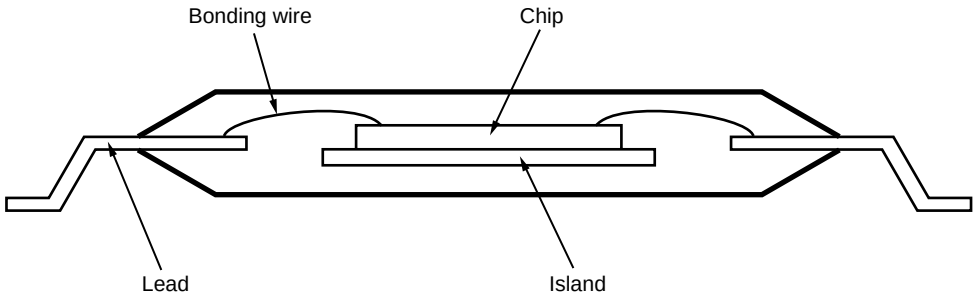
Each Series has no input-only or output-only pins. The number of I/O pins and the number of power supply pins differ depending on the master used. In addition, the position of power supply pins and the number of signal pins differ depending on the package, consult NEC Electronics.

1.6.1 QFP (Quad Flat Package)

Figure 1-4 shows a cross-section of a normal QFP. In a normal QFP, the chip is placed on a metal plate called an island. The leads and chip are connected by fine bonding wires measuring only several 10 μm in diameter.

In a low thermal resistance type QFP, the lead and island materials have increased thermal dissipation properties. The construction itself is the same as a normal QFP.

Figure 1-4. Cross-section of QFP



1.6.2 PBGA (Plastic Ball Grid Array)

Figure 1-5 shows a cross-section of a PBGA package and Figure 1-6 shows the ball arrangements of a BGA package. PBGA is a basic BGA package that uses a glass epoxy board for the interposer, and a wire bonding method. It has an outstanding cost performance.

Figure 1-5. Cross-section of PBGA

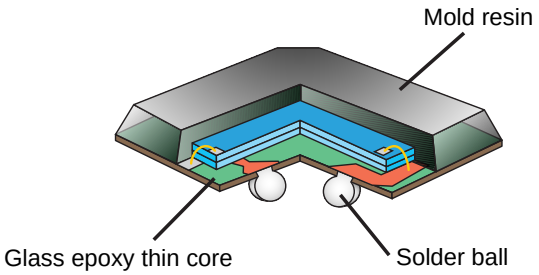
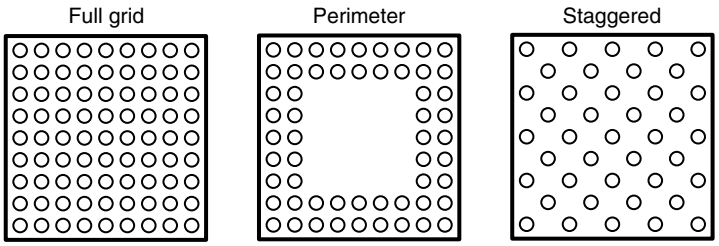


Figure 1-6. Ball Arrangement of BGA Package

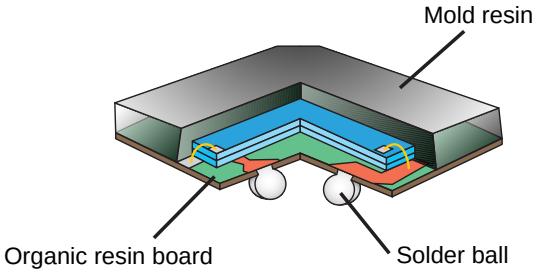


1.6.3 FPBGA (Fine pitch Plastic BGA)

Figure 1-7 shows a cross-section of a FPBGA package.

FPBGA is a basic chip size package (CSP) that uses an organic resin board for the interposer, and a wire bonding method. It provides superior solder connection reliability after being mounted on a motherboard.

Figure 1-7. Cross-section of FPBGA



CHAPTER 2 IMPLEMENTING THE SYSTEM USING THE GATE ARRAY

Be sure to read this chapter since information that is important when starting design is described.

When developing an LSI using gate arrays, to implementing some or all of a system designed by the user, the specifications must be determined so that the circuit scale and the number of I/O pins of the gate arrays are optional.

As the circuit scale increases, designing the circuit becomes more difficult and the cost of the LSI increases. However, because the number of I/O pins decreases, the mounting area on a printed wiring board can be reduced. In addition, because the number of LSIs used decreases, the propagation delay time is shortened.

As the circuit scale decreases, many separate gate arrays are required to configure the system. This is disadvantageous in terms of printed circuit board mounting. Moreover, because signals are transferred between many LSIs, it is difficult to shorten the propagation delay time.

Therefore, when selecting a gate array, take into consideration the propagation delay time and circuit scale.

Select a gate array via the following steps.

“Circuit selection steps”

(1) Estimate circuit scale and master size
↓
(2) Select package
↓
(3) Verify power consumption
↓
(4) Verify pin placement
↓
(5) Verify I/O interface level
↓
(6) Design circuit
↓
(7) Interface
↓
(8) Check using check item list

2.1 Estimating Circuit Scale

2.1.1 Cell utilization rate, usable cell and pin pair number limits

In a channel architecture gate array, the internal cell region is divided into two regions.

- Region where transistors that implement the function block are placed
- Routing dedicated region

In a channelless architecture gate array, the region for implementing the function blocks cannot be clearly distinguished from the routing region because the transistors that implement the function blocks are laid out over the entire internal cell region. Consequently, there is a stronger correlation between the number of cells utilized and the number of nets.

The CMOS-9HD Series uses a channelless architecture (sea-of-gates). This means that not all cells in the internal cell region can be used for function blocks such as gates, flip-flops, and memory. The number of cells actually used is the difference between the total number of cells and the routing cell region used by the number of wires between blocks (number of pin pairs).

The maximum cell utilization rates for the CMOS-9HD Series are roughly as follows:

	• 3-layer routing products	
	μPD65941, 65942, 66942:	75%
<R>	μPD65943, 65944, 65945, 65946, 65948:	70%
	μPD65949:	60%
	μPD65951, 65954, 65956:	55%
	μPD65958:	50%
	• 4-layer routing products	
	μPD65961, 65964, 65966:	65%
<R>	μPD65968:	60%

However, if a large-scale block, such as memory, is mounted, it may be that the total cell utilization rate is further limited, depending on the type of macro (see **2.1.3 Large-scale macro placement** for details).

The pin-pair number is limited by the cell utilization rate and can be calculated by the following formula:

• 3-layer routing products

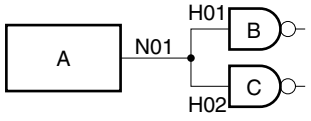
Pin-pair count = 112 × number of raw cells × {(100 – cell utilization rate)/100}^{2} /74.69

• 4-layer routing products

Pin-pair count = 150 × number of raw cells × {(100 – cell utilization rate)/100}^{2} /74.69

"Pin-pair count" is the number of wires connecting the output pins and input pins between blocks (see **Figure 2-1**).

Figure 2-1. Pin-Pair Count



Block A N01-Block B H01
Block A N01-Block C H02

Total of 2 pairs (pin pair count = 2)

If many small-scale blocks such as inverters are used, routing between blocks increases compared with the number of cells used, which increases the number of routing channels.

Conversely, if many large-scale blocks such as memory are used, routing between blocks decreases compared with the number of cells used, which decreases the number of channels required.

Consequently, when placing large-scale blocks, such as memory, the cell utilization rate is further limited. Circuits that do not include memory are limited by the pin-pair count.

<R>

Table 2-1. Number of Cells Placed

(a) 3-layer routing products

Master	X	Y	Cells Placed
μPD65941	241	62	14,942
μPD65942, 66942	381	98	37,338
μPD65943	541	140	75,740
μPD65944	621	162	100,602
μPD65945	721	178	128,338
μPD65946	881	230	202,630
μPD65948	1,101	284	312,684
μPD65949	1,301	336	437,136
μPD65951	1,501	390	585,390
μPD65954	1,801	464	835,664
μPD65956	2,061	532	1,096,452
μPD65958	2,501	646	1,615,646

(b) 4-layer routing products

Master	X	Y	Cells Placed
μPD65961	1,501	390	585,390
μPD65964	1,801	464	835,664
μPD65966	2,061	532	1,096,452
μPD65968	2,501	646	1,615,646

Remark X × Y under the heading “Cells Placed” indicates that the master has a cell space of X in the horizontal direction and a cell space of Y in the vertical direction.

If the actual cell utilization rate and pin-pair count can be satisfied, placement and routing can be guaranteed in the standard schedule in most cases. On the other hand, in cases where the limits are exceeded, placement and routing requires a longer time and, in the worst case, becomes impossible.

Table 2-2 shows the number of usable gates and the corresponding pin-pair count with respect to the cell utilization rate.

<R>

Table 2-2. Usable Gates and Pin-Pair Count (1/2)

(a) 3-layer routing products (1/2)

Master	35% Cell Utilization		40% Cell Utilization		45% Cell Utilization	
	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs
μPD65941	5,230	9,467	5,977	8,066	6,724	6,778
μPD65942, 66942	13,068	23,656	14,935	20,156	16,802	16,937
μPD65943	26,509	47,985	30,296	40,887	34,083	34,356
μPD65944	35,211	63,737	40,241	54,308	45,271	45,634
μPD65945	44,918	81,309	51,335	69,281	57,752	58,215
μPD65946	70,921	128,377	81,052	109,386	91,184	91,915
μPD65948	109,439	198,102	125,074	168,797	140,708	141,836
μPD65949	152,998	276,948	174,854	235,980	196,711	198,288
μPD65951	204,887	370,875	234,156	316,012	263,426	265,538
μPD65954	292,482	529,437	334,266	451,118	376,049	379,064
μPD65956	383,758	694,659	438,581	591,899	493,403	497,360
μPD65958	565,476	1,023,596	646,258	872,176	727,041	732,870

(a) 3-layer routing products (2/2)

Master	50% Cell Utilization		60% Cell Utilization		70% Cell Utilization		75% Cell Utilization	
	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs
μPD65941	7,471	5,601	8,965	3,585	10,459	2,017	11,207	1,400
μPD65942, 66942	18,669	13,997	22,403	8,958	26,137	5,039	28,004	3,499
μPD65943	37,870	28,394	45,444	18,172	53,018	10,222	56,805	7,098
μPD65944	50,301	37,714	60,361	24,137	70,421	13,577	75,452	9,428
μPD65945	64,169	48,112	77,003	30,791	89,837	17,320	96,254	12,028
μPD65946	101,315	75,963	121,578	48,616	141,841	27,347	151,973	18,991
μPD65948	156,342	117,220	187,610	75,021	218,879	42,199	234,513	29,305
μPD65949	218,568	163,875	262,281	104,880	305,995	58,995	327,852	40,969
μPD65951	292,695	219,453	351,234	140,450	409,773	79,003	439,043	54,863
μPD65954	417,832	313,276	501,398	200,497	584,965	112,779	626,748	78,319
μPD65956	548,226	411,041	657,871	263,066	767,516	147,975	822,339	102,760
μPD65958	807,823	605,678	969,388	387,634	1,130,952	218,044	1,211,735	151,419

<R>

Table 2-2. Usable Gates and Pin-Pair Count (2/2)

(b) 4-layer routing products (1/2)

Master	35% Cell Utilization		40% Cell Utilization		45% Cell Utilization	
	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs
μPD65961	204,886	494,654	234,156	421,480	263,425	354,161
μPD65964	292,482	706,136	334,265	601,678	376,048	505,576
μPD65966	383,758	926,501	438,580	789,445	493,403	663,353
μPD65968	565,476	1,365,221	646,258	1,163,265	727,040	977,465

(b) 4-layer routing products (2/2)

Master	50% Cell Utilization		60% Cell Utilization		70% Cell Utilization	
	Usable	Pin Pairs	Usable	Pin Pairs	Usable	Pin Pairs
μPD65961	292,695	292,695	351,234	187,324	–	–
μPD65964	417,832	417,832	501,398	267,412	–	–
μPD65966	548,226	548,226	657,871	350,864	–	–
μPD65968	807,823	807,823	969,387	517,006	–	–

2.1.2 Notes on estimating number of cells used

(1) Input/output/bidirectional buffer blocks

Not only I/O cells but also internal cells are used to configure external interface blocks such as input, output, and bidirectional blocks. Therefore, add the number of internal cells used for input, output, and bidirectional buffer blocks described in **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)** when calculating the total number of cells used.

(2) Critical paths

If there is a path in which speed is a problem, measures can be taken in some cases to shorten the propagation delay of that path. However, routability drops dramatically when such measures are taken. In such a case, the cell utilization rate and maximum pin-pair count should be reduced by a further 10 to 20%.

(3) Macro configuration

Placement and routing are performed for each hierarchical macro (first hierarchy) in the circuit.
Therefore, the hierarchical configuration calls for adequate consideration when a macro is created.
Keep in mind the following points when performing hierarchical design.

(a) Because the routing between macros of the first hierarchy is long, avoid hierarchical design that implements one function between macros.
(b) If possible, avoid placing a small-scale macro that is used to facilitate circuit design in the first hierarchy.

2.1.3 Large-scale macro placement

Large-scale macro placeability is determined by whether or not it is possible to achieve the range (X × Y) of cells needed to implement the macros on the physical space of the internal cells indicated by (X × Y). For soft macros configured by small and medium-scale blocks, virtually no problems of placement arise as long as the cell utilization rate is satisfied. However, there are cases in which large-scale hard macros such as RAM blocks (basic macro) cannot be physically placed due to the size of the master.

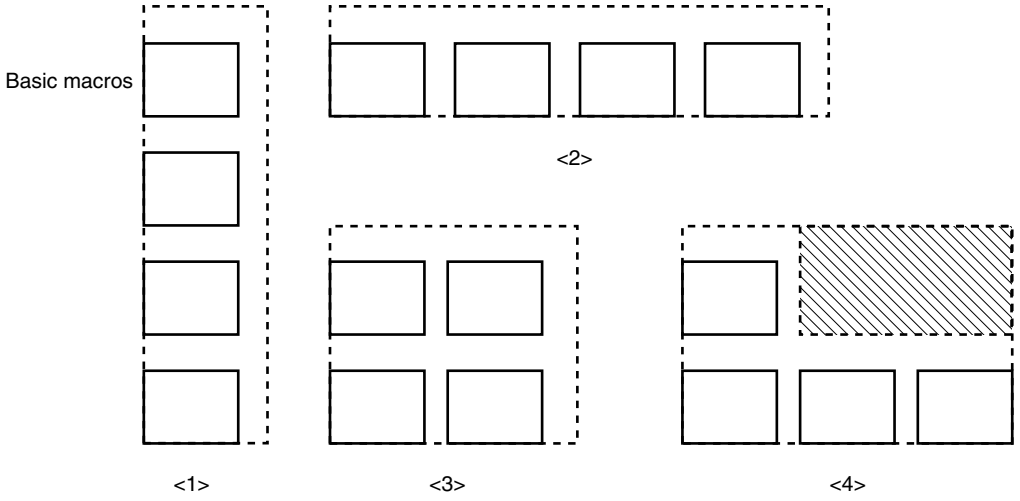
Whether macros can be placed is determined by the range of the cells necessary for implementing each macro on the chip, and the range of cells that can be implemented on the master.

(1) Range of cells occupied by each macro on chip

(a) Soft macro RAM

An NEC Electronics RAM is implemented by soft macros that consist of a basic macro and a logic area. The shape of the cell area occupied to implement a macro depends on how the basic macro is placed. The cell area occupied is limited by the master selected.

Figure 2-2. Shape of Cell Range Occupied by Macros (with 4 Basic Macros)

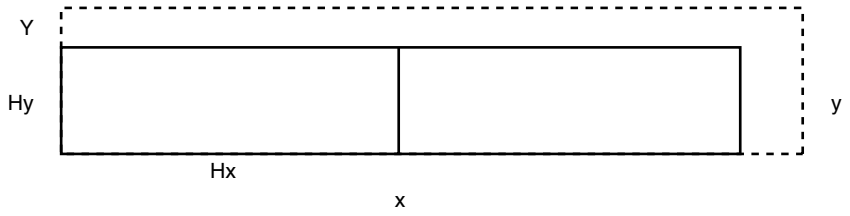


<1> Limited by the number of vertical cells of the master.
<2> Limited by the number of horizontal cells of the master.
<3> Effective if the number of basic blocks used becomes large.
<4> Physically possible but ineffective (because the placement range that can be set up during placement and routing is square or rectangular, the diagonally shaded area is wasted).

Table 2-4 lists examples of the cell ranges occupied by macros. However, it is possible to re-define cell ranges for a RAM outside those in Table 2-4.

To define cell ranges for soft macro RAM, first find the basic macro name and the number of cells required to configure the soft macro RAM in Table 2-4. Next, find the number of cells occupied by the basic macro (X and Y values) in Table 2-3. Then calculate the cell range by substituting in the variables in the following equation with the values from Tables 2-3 and 2-4.

Figure 2-3. Cell Range Occupied by Macro



$y = 2^n \times Hy + Y$

x = soft/uty/y

In the above equation, $x \geq N/2^n \times Hx$ must be satisfied.

soft Number of cells in the soft macro RAM

uty 0.75 (in the μPD65941, 65942, and 66942)

<R> 0.70 (in the μPD65943, 65944, 65945, 65946, and 65948)

0.65 (in the μPD65961, 65964, and 65966)

<R> 0.60 (in the μPD65949 and 65968)

0.55 (in the μPD65951, 65954, and 65956)

0.50 (in the μPD65958)

Hx Minimum number of cells occupied in the horizontal direction needed for placing basic macros.

Hy Minimum number of cells occupied in the vertical direction needed for placing basic macros.

N Number of basic macros used

n When the number of basic macros is 1, n = 0

When the number of basic macros is 2, n = 0, 1

When the number of basic macros is 4, n = 0, 1, 2

When the number of basic macros is 8, n = 0, 1, 2, 3

When the number of basic macros is 16, n = 0, 1, 2, 3, 4

When the number of basic macros is 32, n = 0, 1, 2, 3, 4, 5

Y Arbitrary integer (Y = 0, 1, 2, ...)

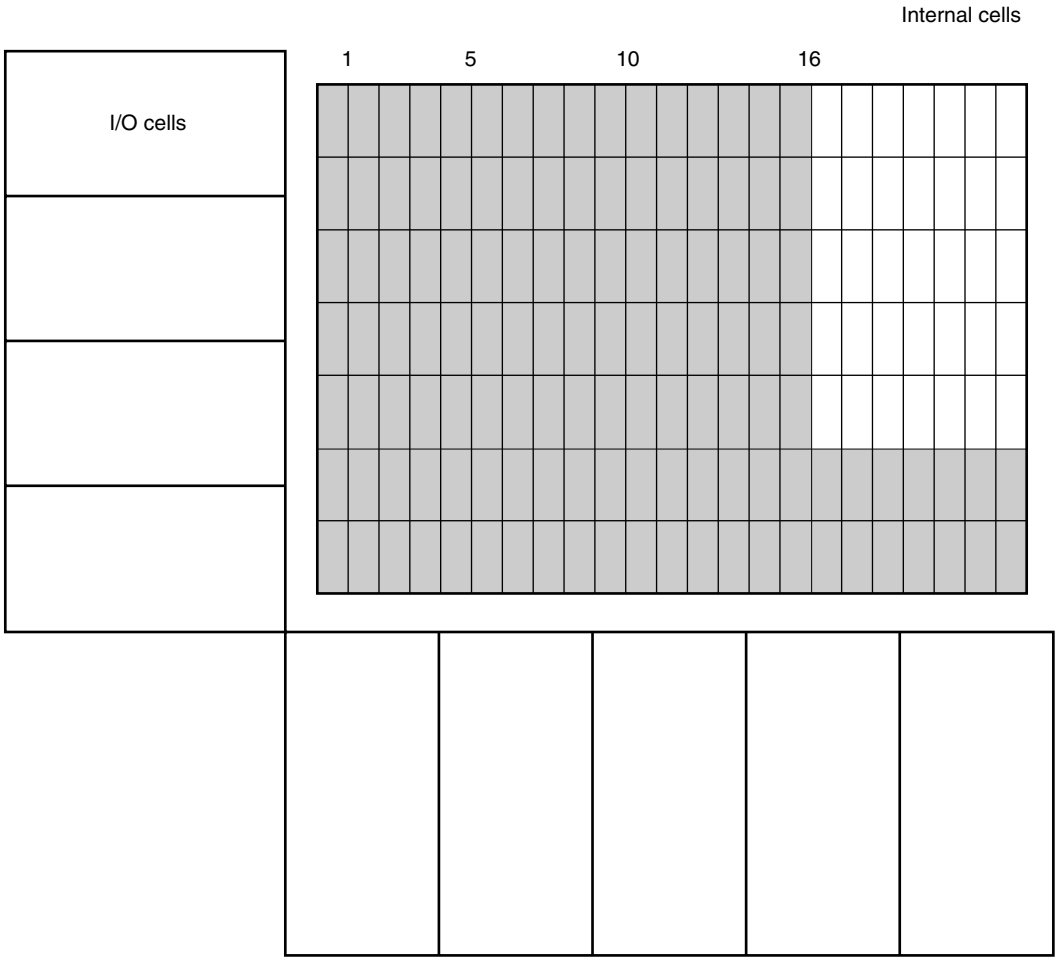
(b) Clock input drivers

The X × Y structure of cells used in a clock input driver differs from normal macros in its very long vertical dimensions. Because the vertical direction of some masters and place cells is much reduced compared with the horizontal direction, there are cases in which placement cannot be performed due to the master. Because the clock input driver requires a routing channel, it is necessary to consult with NEC Electronics if it is to be placed with other large-scale macros.

(2) Array of internal cells of master selected (see **Table 2-1)**

Internal cells are also used for interface blocks and are limited as closely as possible to the I/O cell range. The area of internal cells used by the interface block is 16 internal cells from the left edge to the right edge and 2 cells from the top edge to the bottom edge. Therefore the cell area that the macro can placed in must be within the 16 × 2 range (white part in Figure 2-4.)

Figure 2-4. Area Where Macros Cannot Be Implemented



(3) Determining placeability

Macros are placeable if they can all be placed without overlapping, within the allowable area for implementing macros on the chip. If they are unplaceable, modification of the shape of the macro-occupied area must be considered. If more than one cell overlaps, consult NEC Electronics to determine placeability taking the pin configuration and macro placement position into consideration.

Table 2-3. Minimum Number of Cells Occupied by Basic Macro

(a) High-density single-port RAM

Basic Macro	Words	Bits	X	Y
K147	16	4	48	9
K149	32	4	50	13
K18B	64	8	94	21
K1AB	64	10	116	21
K14D	128	4	82	21
K18F	256	8	160	37
K1AF	256	10	198	37
K18M	1,024	8	316	69
K1AM	1,024	10	392	69

(b) High-density dual-port RAM

Basic Macro	Words	Bits	X	Y
K247	16	4	58	11
K249	32	4	106	11
K28B	64	8	208	15
K2AB	64	10	256	15
K24D	128	4	208	18
K28F	256	8	400	25
K2AF	256	10	496	25
K28M	1,024	8	784	47
K2AM	1,024	10	976	47

Table 2-4 shows the block names and cell ranges occupied by each RAM macro on the chip.

Table 2-4. Occupied Cell Ranges (1/6)

High-density single-port RAM (70% cell utilization)

RAM Type	Words	Bits	Basic RAM	Q'ty	Cell Area Occupied by RAM							
					Type A		Type B		Type C		Type D	
					X	Y	X	Y	X	Y	X	Y
RB47	16	4	K147	1	51	12						
RB49	32	4	K149	1	58	16						
RB4B	64	4	K149	2	58	32	116	16				
RB4D	128	4	K14D	1	103	24						
RB4F	256	4	K14D	2	103	48	205	24				
RB4H	512	4	K14D	4	103	96	205	48	410	24		
RB4M	1,024	4	K14D	8	103	192	205	96	410	48	820	24
RB4S	2,048	4	K14D	16	103	384	205	192	410	96	820	48
RB4U	4,096	4	K14D	32	103	768	205	384	410	192	820	96
RB87	16	8	K147	2	51	24	103	12				
RB89	32	8	K149	2	58	32	116	16				
RB8B	64	8	K18B	1	118	24						
RB8D	128	8	K14D	2	103	48	205	24				
RB8F	256	8	K18F	1	211	40						
RB8H	512	8	K18F	2	211	80	423	40				
RB8M	1,024	8	K18M	1	433	72						
RB8S	2,048	8	K18M	2	433	144	865	72				
RBAB	64	10	K1AB	1	145	24						
RBAD	128	10	K1AB	2	145	48	290	24				
RBAF	256	10	K1AF	1	262	40						
RBAH	512	10	K1AF	2	262	80	523	40				
RBAM	1,024	10	K1AM	1	537	72						
RBAS	2,048	10	K1AM	2	537	144	1,073	72				
RBC7	16	16	K147	4	51	48	103	24	206	12		
RBC9	32	16	K149	4	58	64	116	32	232	16		
RBCB	64	16	K18B	2	118	48	235	24				
RBCD	128	16	K14D	4	103	96	205	48	410	24		
RBCF	256	16	K18F	2	211	80	423	40				
RBCH	512	16	K18F	4	211	160	423	80	846	40		
RBCM	1,024	16	K18M	2	433	144	865	72				
RBEB	64	20	K18B	2	118	48	235	24				
RBED	128	20	K1AB	4	145	96	290	48	580	24		
RBEF	256	20	K1AF	2	262	80	523	40				
RBEH	512	20	K1AF	4	262	160	523	80	1,047	40		
RBEM	1,024	20	K1AM	2	537	144	1,073	72				
RBH7	16	32	K147	8	51	96	103	48	206	24	411	12
RBH9	32	32	K149	8	58	128	116	64	232	32	464	16
RBHB	64	32	K18B	4	118	96	235	48	470	24		
RBHD	128	32	K14D	8	103	192	205	96	410	48	820	24
RBHF	256	32	K18F	4	211	160	423	80	846	40		
RBHH	512	32	K18F	8	211	320	423	160	846	80	1,691	40
RBKB	64	40	K18B	4	118	96	235	48	470	24		
RBKD	128	40	K1AB	8	145	192	290	96	580	48	1,160	24
RBKF	256	40	K1AF	4	262	160	523	80	1,047	40		
RBKH	512	40	K1AF	8	262	320	523	160	1,047	80	2,093	40

Table 2-4. Occupied Cell Ranges (2/6)

High-density single-port RAM (60% cell utilization)

RAM Type	Words	Bits	Basic RAM	Q'ty	Cell Area Occupied by RAM							
					Type A		Type B		Type C		Type D	
					X	Y	X	Y	X	Y	X	Y
RB47	16	4	K147	1	60	12						
RB49	32	4	K149	1	68	16						
RB4B	64	4	K149	2	68	32	135	16				
RB4D	128	4	K14D	1	120	24						
RB4F	256	4	K14D	2	120	48	239	24				
RB4H	512	4	K14D	4	120	96	239	48	478	24		
RB4M	1,024	4	K14D	8	120	192	239	96	478	48	957	24
RB4S	2,048	4	K14D	16	120	384	239	192	478	96	957	48
RB4U	4,096	4	K14D	32	120	768	239	384	478	192	957	96
RB87	16	8	K147	2	60	24	120	12				
RB89	32	8	K149	2	68	32	135	16				
RB8B	64	8	K18B	1	137	24						
RB8D	128	8	K14D	2	120	48	239	24				
RB8F	256	8	K18F	1	247	40						
RB8H	512	8	K18F	2	247	80	493	40				
RB8M	1,024	8	K18M	1	505	72						
RB8S	2,048	8	K18M	2	505	144	1,009	72				
RBAB	64	10	K1AB	1	169	24						
RBAD	128	10	K1AB	2	169	48	338	24				
RBAF	256	10	K1AF	1	305	40						
RBAH	512	10	K1AF	2	305	80	611	40				
RBAM	1,024	10	K1AM	1	626	72						
RBAS	2,048	10	K1AM	2	626	144	1,252	72				
RBC7	16	16	K147	4	60	48	120	24	240	12		
RBC9	32	16	K149	4	68	64	135	32	271	16		
RBCB	64	16	K18B	2	137	48	274	24				
RBCD	128	16	K14D	4	120	96	239	48	478	24		
RBCF	256	16	K18F	2	247	80	493	40				
RBCH	512	16	K18F	4	247	160	493	80	987	40		
RBCM	1,024	16	K18M	2	505	144	1,009	72				
RBEB	64	20	K18B	2	137	48	274	24				
RBED	128	20	K1AB	4	169	96	338	48	677	24		
RBEF	256	20	K1AF	2	305	80	611	40				
RBEH	512	20	K1AF	4	305	160	611	80	1,221	40		
RBEM	1,024	20	K1AM	2	626	144	1,252	72				
RBH7	16	32	K147	8	60	96	120	48	240	24	480	12
RBH9	32	32	K149	8	68	128	135	64	271	32	542	16
RBHB	64	32	K18B	4	137	96	274	48	548	24		
RBHD	128	32	K14D	8	120	192	239	96	478	48	957	24
RBHF	256	32	K18F	4	247	160	493	80	987	40		
RBHH	512	32	K18F	8	247	320	493	160	987	80	1,973	40
RBKB	64	40	K18B	4	137	96	274	48	548	24		
RBKD	128	40	K1AB	8	139	192	338	96	677	48	1,353	24
RBKF	256	40	K1AF	4	305	160	611	80	1,221	40		
RBKH	512	40	K1AF	8	305	320	611	160	1,221	80	2,442	40

Table 2-4. Occupied Cell Ranges (3/6)

High-density single-port RAM (50% cell utilization)

RAM Type	Words	Bits	Basic RAM	Q'ty	Cell Area Occupied by RAM							
					Type A		Type B		Type C		Type D	
					X	Y	X	Y	X	Y	X	Y
RB47	16	4	K147	1	72	12						
RB49	32	4	K149	1	81	16						
RB4B	64	4	K149	2	81	32	163	16				
RB4D	128	4	K14D	1	144	24						
RB4F	256	4	K14D	2	144	48	287	24				
RB4H	512	4	K14D	4	144	96	287	48	574	24		
RB4M	1,024	4	K14D	8	144	192	287	96	574	48	1,148	24
RB4S	2,048	4	K14D	16	144	384	287	192	574	96	1,148	48
RB4U	4,096	4	K14D	32	144	768	287	384	574	192	1,148	96
RB87	16	8	K147	2	72	24	144	12				
RB89	32	8	K149	2	81	32	163	16				
RB8B	64	8	K18B	1	165	24						
RB8D	128	8	K14D	2	144	48	287	24				
RB8F	256	8	K18F	1	296	40						
RB8H	512	8	K18F	2	296	80	592	40				
RB8M	1,024	8	K18M	1	606	72						
RB8S	2,048	8	K18M	2	606	144	1,211	72				
RBAB	64	10	K1AB	1	203	24						
RBAD	128	10	K1AB	2	203	48	406	24				
RBAF	256	10	K1AF	1	366	40						
RBAH	512	10	K1AF	2	366	80	733	40				
RBAM	1,024	10	K1AM	1	751	72						
RBAS	2,048	10	K1AM	2	751	144	1,503	72				
RBC7	16	16	K147	4	72	48	144	24	288	12		
RBC9	32	16	K149	4	81	64	163	32	325	16		
RBCB	64	16	K18B	2	165	48	329	24				
RBCD	128	16	K14D	4	144	96	287	48	574	24		
RBCF	256	16	K18F	2	296	80	592	40				
RBCH	512	16	K18F	4	296	160	592	80	1,184	40		
RBCM	1,024	16	K18M	2	606	144	1,211	72				
RBEB	64	20	K18B	2	165	48	329	24				
RBED	128	20	K1AB	4	203	96	406	48	812	24		
RBEF	256	20	K1AF	2	366	80	733	40				
RBEH	512	20	K1AF	4	366	160	733	80	1,465	40		
RBEM	1,024	20	K1AM	2	751	144	1,503	72				
RBH7	16	32	K147	8	72	96	144	48	288	24	576	12
RBH9	32	32	K149	8	81	128	163	64	325	32	650	16
RBHB	64	32	K18B	4	165	96	329	48	658	24		
RBHD	128	32	K14D	8	144	192	287	96	574	48	1,148	24
RBHF	256	32	K18F	4	296	160	592	80	1,184	40		
RBHH	512	32	K18F	8	296	320	592	160	1,184	80	2,368	40
RBKB	64	40	K18B	4	165	96	329	48	658	24		
RBKD	128	40	K1AB	8	203	192	406	96	812	48	1,624	24
RBKF	256	40	K1AF	4	366	160	733	80	1,465	40		
RBKH	512	40	K1AF	8	366	320	733	160	1,465	80	2,930	40

Table 2-4. Occupied Cell Ranges (4/6)

High-density dual-port RAM (70% cell utilization)

RAM Type	Words	Bits	Basic RAM	Q'ty	Cell Area Occupied by RAM							
					Type A		Type B		Type C		Type D	
					X	Y	X	Y	X	Y	X	Y
R947	16	4	K247	1	65	14						
R949	32	4	K249	1	119	14						
R94B	64	4	K249	2	119	28	238	14				
R94D	128	4	K24D	1	255	21						
R94F	256	4	K24D	2	255	42	509	21				
R94H	512	4	K24D	4	255	84	509	42	1,019	21		
R94M	1,024	4	K24D	8	255	168	509	84	1,019	42	2,038	21
R94S	2,048	4	K24D	16	255	336	509	168	1,019	84	2,038	42
R94U	4,096	4	K24D	32	255	672	509	336	1,019	168	2,038	84
R987	16	8	K247	2	65	28	130	14				
R989	32	8	K249	2	119	28	238	14				
R98B	64	8	K28B	1	248	18						
R98D	128	8	K24D	2	255	42	509	21				
R98F	256	8	K28F	1	510	28						
R98H	512	8	K28F	2	510	56	1,020	28				
R98M	1,024	8	K28M	1	1,053	50						
R98S	2,048	8	K28M	2	1,053	100	2,106	50				
R9AB	64	10	K2AB	1	305	18						
R9AD	128	10	K2AB	2	305	36	610	18				
R9AF	256	10	K2AF	1	633	28						
R9AH	512	10	K2AF	2	633	56	1,265	28				
R9AM	1,024	10	K2AM	1	1,311	50						
R9AS	2,048	10	K2AM	2	1,311	100	2,621	50				
R9C7	16	16	K247	4	65	56	130	28	260	14		
R9C9	32	16	K249	4	119	56	238	28	476	14		
R9CB	64	16	K28B	2	248	36	495	18				
R9CD	128	16	K24D	4	255	84	509	42	1,019	21		
R9CF	256	16	K28F	2	510	56	1,020	28				
R9CH	512	16	K28F	4	510	112	1,020	56	2,041	28		
R9CM	1,024	16	K28M	2	1,053	100	2,106	50				
R9EB	64	20	K28B	2	248	36	495	18				
R9ED	128	20	K2AB	4	305	72	610	36	1,219	18		
R9EF	256	20	K2AF	2	633	56	1,265	28				
R9EH	512	20	K2AF	4	633	112	1,265	56	2,531	28		
R9EM	1,024	20	K2AM	2	1,311	100	2,621	50				
R9H7	16	32	K247	8	65	112	130	56	260	28	521	14
R9H9	32	32	K249	8	119	112	238	56	476	28	952	14
R9HB	64	32	K28B	4	248	72	495	36	990	18		
R9HD	128	32	K24D	8	255	168	509	84	1,019	42	2,038	21
R9HF	256	32	K28F	4	510	112	1,020	56	2,041	28		
R9HH	512	32	K28F	8	510	224	1,020	112	2,041	56	4,082	28
R9KB	64	40	K28B	4	248	72	495	36	990	18		
R9KD	128	40	K2AB	8	305	144	610	72	1,219	36	2,438	18
R9KF	256	40	K2AF	4	633	112	1,265	56	2,531	28		
R9KH	512	40	K2AF	8	633	224	1,265	112	2,531	56	5,061	28

Table 2-4. Occupied Cell Ranges (5/6)

High-density dual-port RAM (60% cell utilization)

RAM Type	Words	Bits	Basic RAM	Q'ty	Cell Area Occupied by RAM							
					Type A		Type B		Type C		Type D	
					X	Y	X	Y	X	Y	X	Y
R947	16	4	K247	1	76	14						
R949	32	4	K249	1	139	14						
R94B	64	4	K249	2	139	28	278	14				
R94D	128	4	K24D	1	297	21						
R94F	256	4	K24D	2	297	42	594	21				
R94H	512	4	K24D	4	297	84	594	42	1,189	21		
R94M	1,024	4	K24D	8	297	168	594	84	1,189	42	2,377	21
R94S	2,048	4	K24D	16	297	336	594	168	1,189	84	2,377	42
R94U	4,096	4	K24D	32	297	672	594	336	1,189	168	2,377	84
R987	16	8	K247	2	76	28	152	14				
R989	32	8	K249	2	139	28	278	14				
R98B	64	8	K28B	1	289	18						
R98D	128	8	K24D	2	297	42	594	21				
R98F	256	8	K28F	1	595	28						
R98H	512	8	K28F	2	595	56	1,190	28				
R98M	1,024	8	K28M	1	1,228	50						
R98S	2,048	8	K28M	2	1,228	100	2,457	50				
R9AB	64	10	K2AB	1	356	48						
R9AD	128	10	K2AB	2	356	36	711	18				
R9AF	256	10	K2AF	1	738	28						
R9AH	512	10	K2AF	2	738	56	1,476	28				
R9AM	1,024	10	K2AM	1	1,529	50						
R9AS	2,048	10	K2AM	2	1,529	100	3,058	50				
R9C7	16	16	K247	4	76	56	152	28	304	14		
R9C9	32	16	K249	4	139	56	278	28	555	14		
R9CB	64	16	K28B	2	289	36	578	18				
R9CD	128	16	K24D	4	297	84	594	42	1,189	21		
R9CF	256	16	K28F	2	595	56	1,190	28				
R9CH	512	16	K28F	4	595	112	1,190	56	2,381	28		
R9CM	1,024	16	K28M	2	1,228	100	2,457	50				
R9EB	64	20	K28B	2	289	36	578	18				
R9ED	128	20	K2AB	4	356	72	711	36	1,422	18		
R9EF	256	20	K2AF	2	738	56	1,476	28				
R9EH	512	20	K2AF	4	738	112	1,476	56	2,952	28		
R9EM	1,024	20	K2AM	2	1,529	100	3,058	50				
R9H7	16	32	K247	8	76	112	152	56	304	28	608	14
R9H9	32	32	K249	8	139	112	278	56	555	28	1,110	14
R9HB	64	32	K28B	4	289	72	578	36	1,156	18		
R9HD	128	32	K24D	8	297	168	594	84	1,189	42	2,377	21
R9HF	256	32	K28F	4	595	112	1,190	56	2,381	28		
R9HH	512	32	K28F	8	595	224	1,190	112	2,381	56	4,762	28
R9KB	64	40	K28B	4	289	72	578	36	1,156	18		
R9KD	128	40	K2AB	8	356	144	711	72	1,422	36	2,844	18
R9KF	256	40	K2AF	4	738	112	1,476	56	2,952	28		
R9KH	512	40	K2AF	8	738	224	1,476	112	2,952	56	5,905	28

Table 2-4. Occupied Cell Ranges (6/6)

High-density dual-port RAM (50% cell utilization)

RAM Type	Words	Bits	Basic RAM	Q'ty	Cell Area Occupied by RAM							
					Type A		Type B		Type C		Type D	
					X	Y	X	Y	X	Y	X	Y
R947	16	4	K247	1	91	14						
R949	32	4	K249	1	167	14						
R94B	64	4	K249	2	167	28	333	14				
R94D	128	4	K24D	1	357	21						
R94F	256	4	K24D	2	357	42	713	21				
R94H	512	4	K24D	4	357	84	713	42	1,426	21		
R94M	1,024	4	K24D	8	357	168	713	84	1,426	42	2,853	21
R94S	2,048	4	K24D	16	357	336	713	168	1,426	84	2,853	42
R94U	4,096	4	K24D	32	357	672	713	336	1,426	168	2,853	84
R987	16	8	K247	2	91	28	182	14				
R989	32	8	K249	2	167	28	333	14				
R98B	64	8	K28B	1	347	18						
R98D	128	8	K24D	2	357	42	713	21				
R98F	256	8	K28F	1	714	28						
R98H	512	8	K28F	2	714	56	1,429	28				
R98M	1,024	8	K28M	1	1,474	50						
R98S	2,048	8	K28M	2	1,474	100	2,948	50				
R9AB	64	10	K2AB	1	427	18						
R9AD	128	10	K2AB	2	427	36	853	18				
R9AF	256	10	K2AF	1	886	28						
R9AH	512	10	K2AF	2	886	56	1,771	28				
R9AM	1,024	10	K2AM	1	1,835	50						
R9AS	2,048	10	K2AM	2	1,835	100	3,670	50				
R9C7	16	16	K247	4	91	56	182	28	365	14		
R9C9	32	16	K249	4	167	56	333	28	666	14		
R9CB	64	16	K28B	2	347	36	693	18				
R9CD	128	16	K24D	4	357	84	713	42	1,426	21		
R9CF	256	16	K28F	2	714	56	1,429	28				
R9CH	512	16	K28F	4	714	112	1,429	56	2,857	28		
R9CM	1,024	16	K28M	2	1,474	100	2,948	50				
R9EB	64	20	K28B	2	347	36	693	18				
R9ED	128	20	K2AB	4	427	72	853	36	1,707	18		
R9EF	256	20	K2AF	2	886	56	1,771	28				
R9EH	512	20	K2AF	4	886	112	1,771	56	3,543	28		
R9EM	1,024	20	K2AM	2	1,835	100	3,670	50				
R9H7	16	32	K247	8	91	112	182	56	365	28	729	14
R9H9	32	32	K249	8	167	112	333	56	666	28	1,333	14
R9HB	64	32	K28B	4	347	72	693	36	1,387	18		
R9HD	128	32	K24D	8	357	168	713	84	1,426	42	2,853	21
R9HF	256	32	K28F	4	714	112	1,429	56	2,857	28		
R9HH	512	32	K28F	8	714	224	1,429	112	2,857	56	5,714	28
R9KB	64	40	K28B	4	347	72	693	36	1,387	18		
R9KD	128	40	K2AB	8	427	144	853	72	1,707	36	3,413	18
R9KF	256	40	K2AF	4	886	112	1,771	56	3,543	28		
R9KH	512	40	K2AF	8	886	224	1,771	112	3,543	56	7,086	28

2.1.4 Limits of number of usable cells and pin-pair counts for macros other than large-scale macros (such as memory)

Calculate the number of cells usable for gates other than the large-scale macros (memory) by using the following equations.

• 3-layer routing products

μPD65941, 65942, and 66942

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.75

<R> μPD65943, 65944, 65945, 65946, and 65948

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.70

μPD65949

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.60

μPD65951, 65954, and 65956

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.55

μPD65958

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.50

• 4-layer routing products

μPD65961, 65964, 65966

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.65

<R> μPD65968

Number of usable cells = (number of raw cells – cell area occupied by all macros) × 0.60

Because the total cell utilization rate changes when large-scale macros (memory) are placed, the pin-pair count limit also changes.

Cell utilization rate = (number of usable cells + number of cells used for all macros)/number of raw cells × 100

• 3-layer routing products

Pin-pair count = 112 × number of raw cells × {(100 – cell utilization rate)/100}^{2} /74.69

• 4-layer routing products

Pin-pair count = 150 × number of raw cells × {(100 – cell utilization rate)/100}^{2} /74.69

2.1.5 Notes on placing large-scale macros (memory)

The following points must be noted when using large-scale macros:

- External pin placement
- Block type used for circuits other than macros

(1) External pin placement

Place related external pins close to macros if two or more large-scale macros are placed. If no consideration is given to pin placement, the routing of external pins is long, wasting routing channels.

As a result, routing may not be completed. When placing two or more large-scale macros, consult NEC Electronics for macro placement method.

(2) Block type used for circuits other than macros

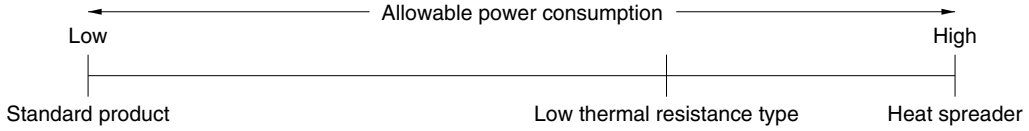
When the number of cells that can be used for logic is reduced because of large-scale macros, medium-scale macros, such as 8-bit latches, may not fit in the available space.

2.2 Verifying Power Consumption

Although CMOS gate arrays are of a low-power consumption type, a considerable amount of power is consumed when they are operated at speeds greater than 50 MHz. Because the temperature of the LSI increases with the amount of power used and the functionality of the product is not guaranteed as the temperature increases beyond the maximum values specified here, it is necessary to hold the power consumption of the LSI below a maximum.

The maximum power consumption is limited by the package type. To improve the allowable power consumption, special QFPs with low thermal resistance and heat spreaders are provided. Figure 2-5 shows the relationship between the QFP type and the allowable power consumption. For detailed data, see **4.3 Power Consumption**.

Figure 2-5. Allowable Power Consumption vs. QFP Type



2.3 Pin Placement

<R> The positions of the package power supply pins is predetermined. The points noted below must be considered in determining pin layout (pin placement).

There are cases where the power requirement will increase, depending on the results of investigating items such as the number of simultaneous switching output pins.

For details, see **4.6 Limits of Simultaneous Switching of Output Buffers**.

2.3.1 Notes on pin placement

(1) Clock pins, control (set, reset) pins

Because these pins are subject to noise, they must be placed close to ground (GND) pins.

(2) Output pins

Because output pins are subject to clock pin noise, they should be isolated as much as possible. If a large group of output pins has many simultaneous switching pins, the group should be surrounded by V_{DD} and GND pins.

<R> **(3) No connection (NC) pins**

Even in the case of unused pins, do not leave pins that are usable as signals unconnected, and be sure to process them in one of the following manners.

(a) Place an additional power supply or additional GND.
(b) Place a 3-state output buffer which is fixed to high impedance output.
(c) Place an input buffer and fix its level on the mounting board, or place an input buffer with pull-up/pull-down resistor.

(4) Scan path I/O pins

The placement of test pins for each package is predetermined. If scan path is used, be sure to specify scan path I/O pins for the specified pin number.

For details, see **SYSTEM LSI DESIGN Design For Test User's Manual**.

(5) Digital PLL (digital phase locked loop) pin placement

There are no physical limits for pin placement. However, to sufficiently draw out the capabilities of digital PLLs, it is necessary to study pin placement, including the placement of PLL macros. NEC Electronics should be consulted regarding pin placement.

Applicable blocks:

<R> F9E4, F9H2, F9H3, FI0P, FI0Q

(6) Placing oscillator block

For the locations where the oscillation pin can be placed, refer to **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**.

Do not place pins that may malfunction when noise is superimposed on them (such as a reset pin) in the vicinity of the oscillator pins.

2.4 I/O Interface

2.4.1 Input blocks

Signal Level
LVTTL
5 V tolerant

Function
Buffer
Fail safe

Input Format
Normal
Schmitt trigger
Clock driver

Pull-Up/Pull-Down Resistor
No resistor
With 50 kΩ pull-up resistor
With 5 kΩ pull-up resistor
With 50 kΩ pull-down resistor

Signal Level	Function	Input Format
GTL+	Buffer	Normal

Signal Level	Function	Input Format
LVTTL	Digital PLL	Special

There are three types of input interface blocks:

<1> LVTTL input level block

This block connects a 3.3 V input signal to the LSI. Blocks with fail-safe functions are also available. A block with fail-safe function has a protection function against excess voltage. There is no continuity to the gate array power supply when the gate array power supply voltage is in the OFF state, even if a signal is applied.

<2> 5 V tolerant input block

This block connects a 5 V input signal to the LSI.

<3> GTL+ (gunning transceiver logic: small amplitude interface)

Because GTL+ is a differential circuit, similar to ECL, it can accept super high-speed signals.

In addition, digital PLL (digital phase locked loop) is also available for minimizing the clock skew between chips.

<R> **Caution μPD66942 can support the LVTTL input buffer only, excluding the buffers with fail-safe function. LVTTL input buffers with fail-safe function and 5 V tolerant input buffers cannot be placed.**

2.4.2 Output blocks

Signal Level	Function	Output Format	Pull-Up/Pull-Down Resistor	Load Drive Capability I_{OL}	
LVTTL	Buffer	Normal	No resistor	$I_{OL} = I_{OH}$	1.0 mA
5 V tolerant	Three-state	Low noise	With 50 kΩ pull-up resistor		2.0 mA
	Open-drain	TTL/CMOS	With 5 kΩ pull-up resistor		3.0 mA
			With 50 kΩ pull-down resistor		6.0 mA
					9.0 mA
					12.0 mA
					18.0 mA
					24.0 mA

Signal Level	Function	Output Format	Pull-Up/Pull-Down Resistor	Load Drive Capability I_{OL}	
GTL+	Open-drain	Normal	No resistor		40.0 mA

There are three types of output interface-level blocks:

<1> LVTTL output interface block

This block connects a 3.3 V input signal to the LSI.

<2> 5 V tolerant output interface block

This block outputs a 5 V signal from the LSI. There are two types, CMOS and TTL. The CMOS block must be clamped with a pull-up resistor, the same as for an open-drain output. Also, the TTL block supports 5 and 3.3 V LSIs that drive the gate array.

<3> GTL+

The GTL+ output part is an open-drain buffer with enable function.

In addition, a low-noise type buffer for holding down generated noise is also available. The output drive capability I_{OL} is equal to I_{OH}. The following types of buffers are available:

- LVTTL output buffer (Normal type: 6 types, low-noise type: 5 types)
- TTL 5 V tolerant output buffer (Normal type: 8 types, low-noise type: 3 types)
- CMOS 5 V tolerant output buffer (Normal type: 6 types, low-noise type: 3 types)

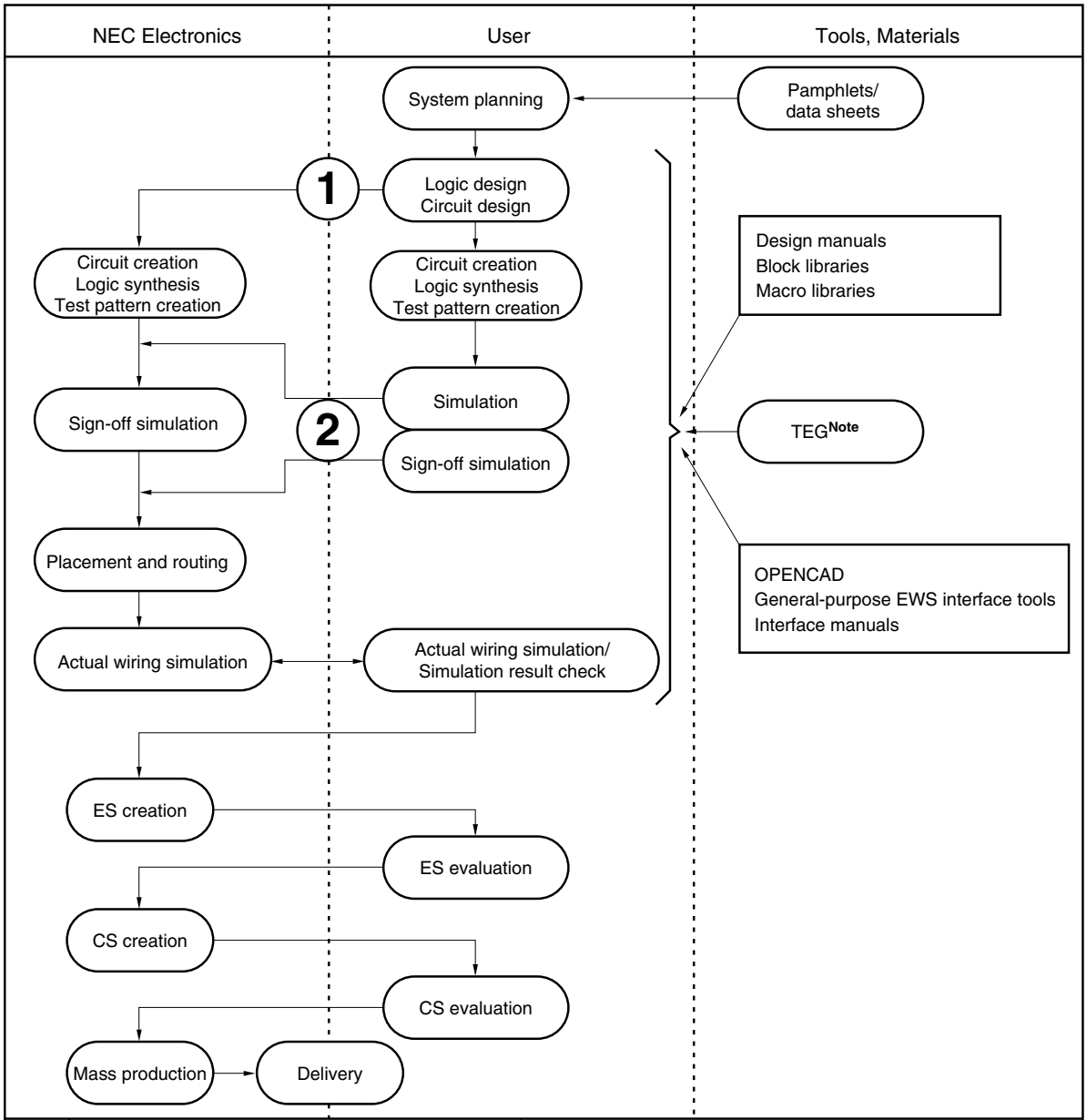
If an input signal is at a floating level in a CMOS circuit, excessive current will flow, and noise will affect the circuit, resulting in possible malfunction. A buffer with a pull-up or pull-down resistor must be used for pins whose level may float in the circuit board.

<R> **Caution μPD66942 can place the LVTTL output buffer only.**
5 V tolerant output buffer cannot be placed.

2.5 Development Flow

The following figure shows the development flow of a CMOS gate array.

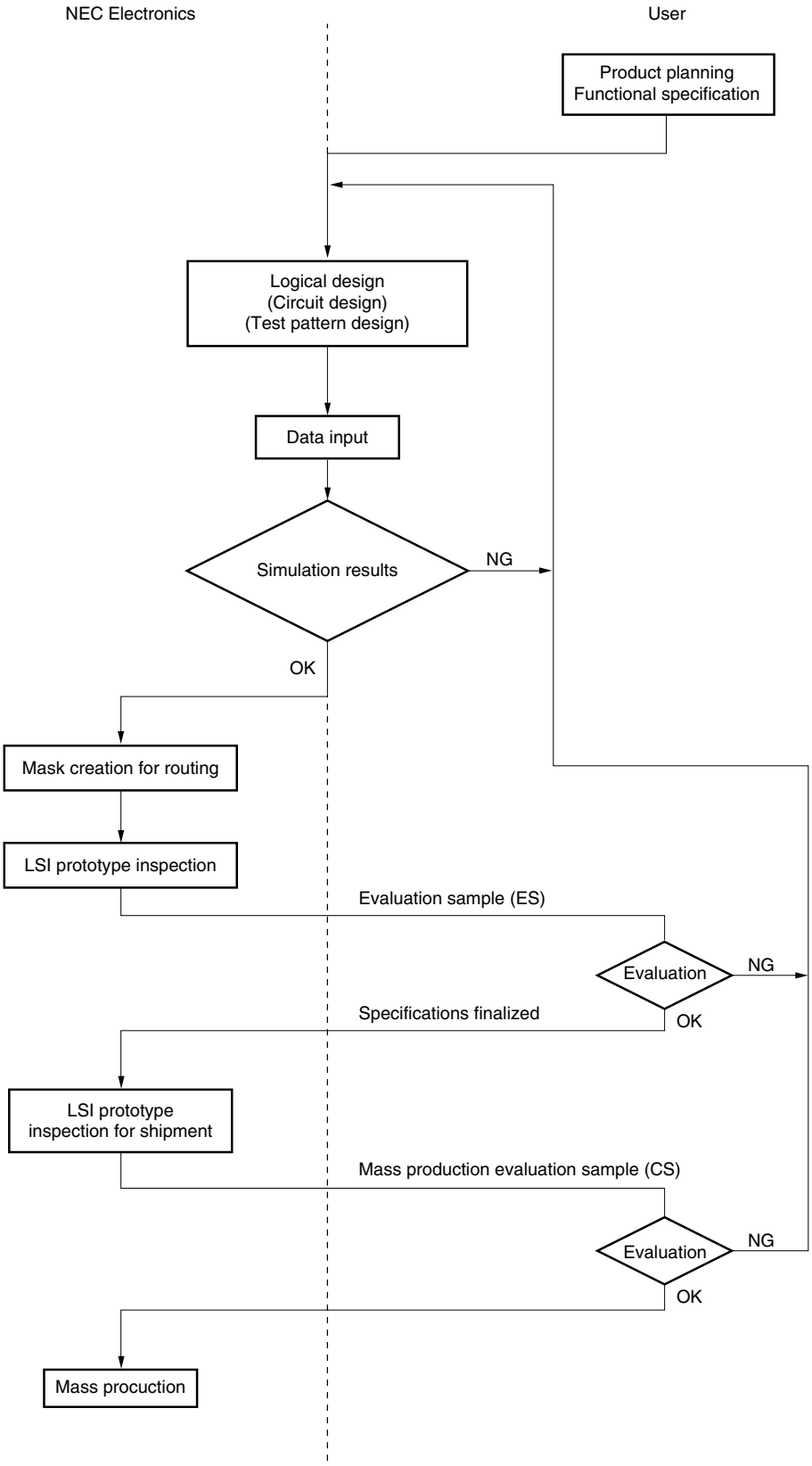
Flow 1: Development procedure and interfacing



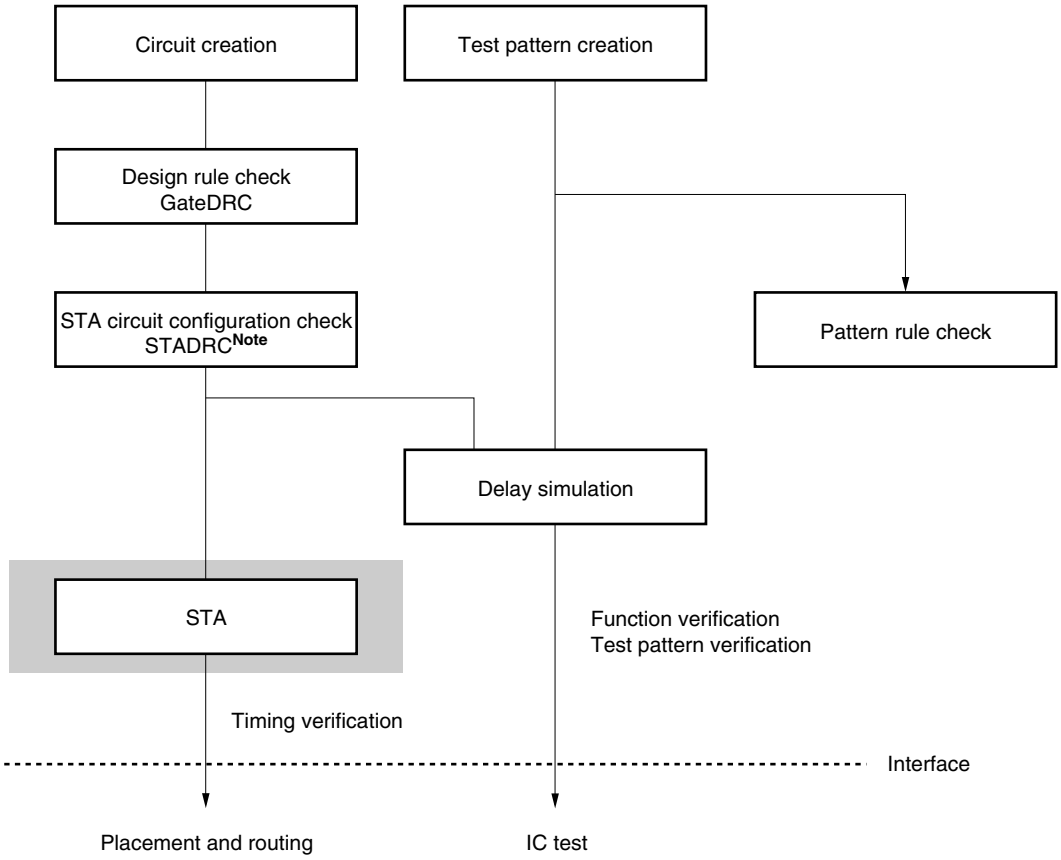
1	Circuit diagram level interface	
2	Simulation level interface	• When using NEC Electronics' sign-off simulator, placement and routing is performed immediately after user confirmation. If another simulator is used, simulation will be executed again by NEC Electronics.

Note Only when necessary.

Flow 2: Development flow



Flow 3: Front-end detailed flow



Note STADRC is only required when sign-off performed by STA.

2.6 OPENCAD Configuration Tools

The following tools can be selected in accordance with the user environment.

Caution 1. Refer to the user's manuals in the OPENCAD Series for the latest versions of the OPENCAD configuration tools.

Caution 2. Some functions may not be supported, so check before using OPENCAD.

Function	NEC Electronics Tools	I/F Data	Commercial Tool I/F
Function simulator	—	• Netlist PWC/EDIF (2.0.0)/ Verilog® HDL • Test pattern ALBA • Delay data file • Constraint file	ModelSim®/Verilog-XL™/ NC-Verilog®/VCS®
Schematic editor	Vdraw		—
Logic synthesis	—		Design Compiler®
Gate level simulator[Note 1]	V.sim		ModelSim/Verilog-XL/ NC-Verilog/VCS
Formal verifier	—		Formality®/Tuxedo™-LEC/ Conformal™-LEC
STA[Note 1]	Tiara		PrimeTime®
Fault simulator[Note 2]	C.FGRADE		—
Design for test	NEC_SCAN2/NEC_BSCAN/ NEC_BIST/TESTBUS		DFTCompiler/TetraMAX®
Floor planner[Note 3]	CBIC: ace_floorplan GA: Galet		—
Placement and wiring[Note 3]	Galet		Silicon Ensemble™

Note 1. Sign-off tool

Note 2. Tool not supported in HP™ version

Note 3. Tool supported individually

Remark Platform: Sun™ (Solaris™)/HP (HP-UX™)
GUI: X11R5/Motif™1.2

Gate array development is a cooperative effort by the user and NEC Electronics. The user is responsible for the steps from system and circuit design through simulation. NEC Electronics is responsible for providing design information, supporting the user in designing the circuit, and the steps after simulation.

The transfer of development work from the user to NEC Electronics is called interfacing. The interface level is divided into the following two depending on what data is to be provided from the user to NEC Electronics.

(1) Circuit diagram level interface

A circuit diagram designed with 74LS or NEC Electronics' gate array blocks is submitted to NEC Electronics and NEC Electronics performs the steps after circuit simulation.

NEC Electronics will provide the user with the results of design rule checking and circuit simulation, which must be confirmed and approved by the user.

(2) Simulation level interface

The user performs circuit design and simulation work using various EWS (engineering work stations) and CAD system simulators, and NEC Electronics takes over the rest of the development work (such as automatic placement and routing and final simulation).

At either interface level, the user may consult NEC Electronics about items NEC Electronics has provided, as well as which tools are presently available.

2.7 List of Interface Data

Embedded array and cell-based IC descriptions should be disregarded when referencing this list.

Caution There may be changes to the data depending on the edition of OPENCAD, so be sure to contact NEC Electronics before commencing design.

			File Type and Name	SIMULATOR	
				V.sim	Verilog
NETLIST			PWC (.pwc)	◎Note 3 (t1)	◎Note 3 (t1)
			Verilog HDL (.v)	–	◎Note 3 (t1)
			EDIF (.edif)	◎Note 3 (t1)	◎Note 3 (t1)
PIN ASSIGN			DIF (.dif)	◎ (t1)	◎ (t1)
EMC Check	CB10, EA10 or later		EMC check file (.emc)	◎	◎
CROSS Talk	CB10 or later (except EA10)		pcs file (.pcs)	○	○
TEST Pattern	Without I/O modulation specification Note 1		ALBATROSS (.alb)	◎Note 4 (t3)	◎Note 6 (t3)
	With I/O modulation specification Note 1		ALBATROSS (.alb) Note 2	◎Note 5 (t3)	◎Note 7 (t3)
MACRO	RAM	BIST	RAMPIN file (.rpi)	○	○
			BIST separation file (.bist.scn) (when used with SCAN)	○ (t1)	○ (t1)
	ROM		NINCF (.nin)	○ (t3)	○ (t3)
			ROM.cmd	○ (t3)	○ (t3)
	Mega Macro		Megamacro unit test specifications	○	○
			Initial Pattern	○	○
	Digital PLL		Initial Pattern	○	○
DFT	BSCAN		SCAN+BSCAN Initial Pattern (scan.init.alb)	○	○
			SET file (.set)	○ (t1)	○ (t1)
			Circuit verification pattern (.bspat.alb)	◎	◎
			Order file (.bsorder)	○ (t1)	○ (t1)
			BSDL file (.bsdl)	○ (t1)	○ (t1)
	SCAN		User macro separation file	○ (t1)	○ (t1)
			Pin location file	○	○
Other	CRITICAL PATH		tiara comand file	○ (t2)	○ (t2)
			Critical path guidelines (paper)	○ (t2)	○ (t2)
	Floorplan		Floorplan specification document (paper)	○Note 8 (t1)	○Note 9 (t1)
			Def file (.floorplan.def)	○Note 8 (t1)	○Note 9 (t1)
	CTS		CTS Check report (.rpt)	◎ (t1)	◎ (t1)

Rev.1.8 12 Dec 2000

<R>

		File Type and Name	SIMULATOR							
			V.sim			Verilog				
Other	ASIC product development information	ASIC product development information check list (paper)	◎			◎				
Check result file	Netlist rule check	(.gatedrc)	◎ (t1)			◎ (t1)				
	alb check	(.ALBchk)	◎Note 10 (t3)			◎Note 11 (t3)				
	PIN check	"NO ERR" screen copy	◎ (t1)			◎ (t1)				
	SCAN check	(.scanchk)	○ (t1)			○ (t1)				
	BSCAN check	(.bscanchk)	○ (t1)			○ (t1)				
	Sim result MIN. & MAX. (fraction of pattern number)		.slg	.tpe	.iomoduchk	.log	.bus	.ovprd	.iochk	.trcpr
		DC test pattern (up to 32 K patterns)	◎Note 12	◎Note 12	◎Note 12	◎Note 15	◎Note 15	◎Note 15	◎Note 15	◎Note 15
		Function test pattern	○Note 13	○Note 13	○Note 13	○Note 16	○Note 16	○Note 16	○Note 16	○Note 16
		High-speed function test pattern	○Note 14	○Note 14	○Note 14	○Note 17	○Note 17	○Note 17	○Note 17	○Note 17
TESTACT	DFT database file	(dft_db)	○			○				
	DFT pin location file	(dft-set)	○			○				
	Test bus connection check pattern	testbus.cpt	○			○				
	BSCAN circuit verification pattern	bspat.cpt	○			○				

Rev.1.8 12 Dec 2000

Note 1. There must be a description of I/O modulation in the timing of ALBATROSS.

Note 2. Refers to input modulation and high-speed function test.

Note 3 to 11. Select one for each.

Note 12 and 14 or 15 and 17. Required if high-speed function test is requested.

Note 12 and 13 or 15 and 16. Required if test patterns exceed 32 K.

Remark 1. ◎: Required, ○: When necessary

Remark 2. (t1): When test run is requested (P&R → SDF)
(t2): When test run is requested ((t1) → Critical path confirmation)
(t3): When test run is requested ((t1) → Simulation)

CHAPTER 3 PRODUCT SPECIFICATIONS

The CMOS-9HD Series has input/output interface blocks that can be connected not only to 3.3 V LSIs but also to conventional 5 V LSIs.

This chapter describes the product specifications of the CMOS-9HD Series.

3.1 Terminology

Table 3-1. Terminology for Absolute Maximum Ratings

Item	Symbol	Definition
Power supply voltage	V_{DD}	Range of voltages which will not damage or reduce reliability when applied to the V_{DD} pin.
Input voltage	V_I	Range of voltages which will not damage or reduce reliability when applied to the input pin.
Output voltage	V_O	Range of voltages which will not damage or reduce reliability when applied to the output pin.
Input current	I_I	Allowable absolute value of current which will not cause latchup when applied to the input pin.
Output current	I_O	Allowable absolute value of DC current which will not cause damage or reduce reliability when flowing to or from the output pin.
Operating temperature	T_A	Range of ambient temperatures for normal logical operation.
Storage temperature	T_{stg}	Range of element temperatures which will not damage or reduce reliability in the state where neither voltage nor current is applied.

Table 3-2. Terminology for Recommended Operating Conditions

Item	Symbol	Definition
Power supply voltage	V_{DD}	Range of voltages for normal logical operation when V_{SS} = 0 V.
High-level input voltage	V_{IH}	For voltage applied to the input of the gate array, this value indicates the voltage of the high-level state in which the input buffer operates normally. • If voltage greater than the MIN value is applied, the input voltage is assured to be high-level.
Low-level input voltage	V_{IL}	For voltage applied to the input of the gate array, this value indicates the voltage of the low-level state in which the input buffer operates normally. • If a voltage less than the MAX value is applied, the input voltage is assured to be low-level.
Positive trigger voltage	V_P	Input level that inverts the output level when the input of the gate array is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Input level that inverts the output level when the input of the gate array is changed from the high-level side to the low-level side.
Hysteresis voltage	V_H	Difference between the positive- and negative-trigger voltage.
Input rise time	t_{ri}	Limit value for the rise time from 10% to 90% of the input voltage applied to the input of the gate array.
Input fall time	t_{fi}	Limit value for the fall time from 90% to 10% of the input voltage applied to the input of the gate array.

Table 3-3. Terminology for DC Characteristics

Item	Symbol	Definition
Static current consumption	I_{DDS}	In the state where there is no voltage change in the input and output pins, indicates the current that flows in from the power supply pin at the specified power supply voltage.
OFF state output current	I_{OZ}	For a three-state output, this value indicates the current that flows through the output pin at the specified voltage when the output is at high impedance.
Output short-circuit current	I_{OS}	Current that flows out if the output pin is short-circuited to GND when output is at the high level.
Input leakage current	I_I	Current that flows through the input pin when voltage is applied to the input pin.
Low-level output current	I_{OL}	Current that flows to the output pin at the specified low-level output voltage.
High-level output current	I_{OH}	Current that flows from the output pin at the specified high-level output voltage.
Low-level output voltage	V_{OL}	Output voltage when output is open in the low-level state.
High-level output voltage	V_{OH}	Output voltage when output is open in the high-level state.

3.2 Absolute Maximum Rating Values

Table 3-4. Absolute Maximum Rating Values

Item	Symbol	Conditions	Ratings	Units
Power supply voltage	V_{DD}		–0.5 to +4.6	V
<R> Input voltage	V_I			
LVTTL input buffer		$V_I < V_{DD} + 0.5$ V	–0.5 to +4.6	V
5 V tolerant input buffer		$V_I < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Output voltage	V_O			
LVTTL output buffer		$V_O < V_{DD} + 0.5$ V	–0.5 to +4.6	V
TTL 5 V tolerant output buffer		$V_O < V_{DD} + 3.0$ V	–0.5 to +6.6	V
CMOS 5 V tolerant output buffer		$V_O < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Output current	I_O			
I_{OL} = 1.0 mA		FV0A	3	mA
I_{OL} = 2.0 mA		FV0B	7	mA
I_{OL} = 3.0 mA		FO09, FV09, FY09	10	mA
I_{OL} = 6.0 mA		FO04, FV04, FY04	20	mA
I_{OL} = 9.0 mA		FO01, FV01, FY01	30	mA
I_{OL} = 12.0 mA		FO02, FV02, FY02, FW02, FZ02	40	mA
I_{OL} = 18.0 mA		FO03, FV03, FY03, FW03, FZ03	60	mA
I_{OL} = 24.0 mA		FO06, FV06, FY06, FW06, FZ06	75	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Except for buffers with the fail-safe function, 5 V or 3.3 V must be applied to the I/O pins only after applying the power supply voltage.

3.3 Standard Specification 1 V_{DD} = 3.3 ±0.3 V; T_A = –40 to +85°C (T_J = –40 to +125°C)

3.3.1 Recommended operating range

Table 3-5. Recommended Operating Range

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Units
Power supply voltage	V_{DD}			3.0	3.3	3.6	V
High-level input voltage	V_{IH}	LVTTL input buffer LVTTL input buffer with fail-safe function		2.0		V_{DD}	V
Low-level input voltage	V_{IL}			0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.4		2.4	V
Negative trigger voltage	V_N			0.8		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	5 V tolerant input buffer		2.0		5.5	V
Low-level input voltage	V_{IL}			0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.4		2.4	V
Negative trigger voltage	V_N			0.8		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
Input rise time (data)	t_{ri}	Normal input		0		200	ns
Input fall time (data)	t_{fi}			0		200	ns
Input rise time (clock)	t_{ri}	Normal input		0		4	ns
Input fall time (clock)	t_{fi}			0		4	ns
Input rise time	t_{ri}	Schmitt input		0		10	ms
Input fall time	t_{fi}			0		10	ms

Remark If a signal that rises or falls dully or a signal with noise exceeding the threshold value is to be input, use a Schmitt trigger input buffer because noise on the internal signal line of the chip may cause malfunctioning. Clock input in particular is easily influenced by noise, so that a separate recommended operating range is specified. If the rise or fall time increases beyond this range, likewise use a Schmitt trigger input buffer. Note that, if a noise exceeding the hysteresis voltage is input, malfunctioning may occur. Exercise care in laying out pins as fluctuation on the power supply due to simultaneous switching of output buffers which degrades the capability of the Schmitt trigger input buffer.

3.3.2 DC characteristics

Table 3-6. DC Characteristics (1/2)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
<R> Static current consumption[Note 1]						
μPD65941, 65942, μPD65943, 65944, μPD65945, 65946, μPD65948, 65949, μPD66942	I_{DDS}	$V_I = V_{DD}$ or GND		2.0	300	μA
μPD65951, 65954, μPD65956, 65961, μPD65964, 65966	I_{DDS}	$V_I = V_{DD}$ or GND		3.0	400	μA
μPD65958, 65968	I_{DDS}	$V_I = V_{DD}$ or GND		4.0	800	μA
OFF-state output current[Note 2]						
LVTTL output	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
TTL 5 V tolerant output	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
CMOS 5 V tolerant output	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
Output influx current[Note 3]	I_R	V_{PU} = 5.5 V R_{PU} = 2 kΩ			0.1	μA
CMOS 5 V tolerant output		V_O = 3.0 V				
Output short-circuit current[Note 4]	I_{OS}	V_O = GND			−250	mA
Input leakage current						
Normal input	I_I	$V_I = V_{DD}$ or GND			±1.0	μA
With pull-up resistor (50 kΩ)	I_I	V_I = GND	−28	−83	−190	μA
With pull-up resistor (5 kΩ)	I_I	V_I = GND	−280	−700	−1,900	μA
With pull-down resistor (50 kΩ)	I_I	$V_I = V_{DD}$	28	83	190	μA
Pull-up resistor (50 kΩ)[Note 5]	R_{PU}	V_I = GND	18.9	39.8	107.1	kΩ
Pull-up resistor (5 kΩ)[Note 5]	R_{PU}	V_I = GND	1.9	4.7	10.7	kΩ
Pull-down resistor (50 kΩ)[Note 5]	R_{PD}	$V_I = V_{DD}$	18.9	39.8	107.1	kΩ
Low-level output current[Note 6]						
LVTTL output						
3.0 mA type FO09	I_{OL}	V_{OL} = 0.4 V	3.00[Note 7]			mA
6.0 mA type FO04	I_{OL}	V_{OL} = 0.4 V	6.00			mA
9.0 mA type FO01	I_{OL}	V_{OL} = 0.4 V	9.00			mA
12.0 mA type FO02	I_{OL}	V_{OL} = 0.4 V	12.00			mA
18.0 mA type FO03	I_{OL}	V_{OL} = 0.4 V	18.00			mA
24.0 mA type FO06	I_{OL}	V_{OL} = 0.4 V	24.00			mA

Table 3-6. DC Characteristics (2/2)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Low-level output current[Note 6]						
TTL 5 V tolerant output						
1.0 mA type FV0A	I_{OL}	V_{OL} = 0.4 V	1.00			mA
2.0 mA type FV0B	I_{OL}	V_{OL} = 0.4 V	2.00			mA
3.0 mA type FV09	I_{OL}	V_{OL} = 0.4 V	3.00			mA
6.0 mA type FV04	I_{OL}	V_{OL} = 0.4 V	6.00			mA
9.0 mA type FV01	I_{OL}	V_{OL} = 0.4 V	9.00			mA
12.0 mA type FV02	I_{OL}	V_{OL} = 0.4 V	12.00			mA
18.0 mA type FV03	I_{OL}	V_{OL} = 0.4 V	18.00			mA
24.0 mA type FV06	I_{OL}	V_{OL} = 0.4 V	24.00			mA
Low-level output current[Note 6]						
CMOS 5 V tolerant output						
3.0 mA type FY09	I_{OL}	V_{OL} = 0.4 V	3.00			mA
6.0 mA type FY04	I_{OL}	V_{OL} = 0.4 V	6.00			mA
9.0 mA type FY01	I_{OL}	V_{OL} = 0.4 V	9.00			mA
12.0 mA type FY02	I_{OL}	V_{OL} = 0.4 V	12.00			mA
18.0 mA type FY03	I_{OL}	V_{OL} = 0.4 V	18.00			mA
24.0 mA type FY06	I_{OL}	V_{OL} = 0.4 V	24.00			mA
High-level output current[Note 6]						
LVTTL output						
3.0 mA type FO09	I_{OH}	V_{OH} = 2.4 V	−3.00			mA
6.0 mA type FO04	I_{OH}	V_{OH} = 2.4 V	−6.00			mA
9.0 mA type FO01	I_{OH}	V_{OH} = 2.4 V	−9.00			mA
12.0 mA type FO02	I_{OH}	V_{OH} = 2.4 V	−12.00			mA
18.0 mA type FO03	I_{OH}	V_{OH} = 2.4 V	−18.00			mA
24.0 mA type FO06	I_{OH}	V_{OH} = 2.4 V	−24.00			mA
High-level output current[Note 6]						
TTL 5 V tolerant output						
1.0 mA type FV0A	I_{OH}	V_{OH} = 2.4 V	−1.00			mA
2.0 mA type FV0B	I_{OH}	V_{OH} = 2.4 V	−1.00			mA
3.0 mA type FV09	I_{OH}	V_{OH} = 2.4 V	−3.00			mA
6.0 mA type FV04	I_{OH}	V_{OH} = 2.4 V	−3.00			mA
9.0 mA type FV01	I_{OH}	V_{OH} = 2.4 V	−3.00			mA
12.0 mA type FV02	I_{OH}	V_{OH} = 2.4 V	−3.00			mA
18.0 mA type FV03	I_{OH}	V_{OH} = 2.4 V	−6.00			mA
24.0 mA type FV06	I_{OH}	V_{OH} = 2.4 V	−6.00			mA
Low-level output voltage						
LVTTL output type	V_{OL}	I_{OL} = 0 mA			0.1	V
LVTTL output (with 5 kΩ pull-up resistor)	V_{OL}	I_{OL} = 0 mA			0.2	V
TTL 5 V tolerant output	V_{OL}	I_{OL} = 0 mA			0.1	V
CMOS 5 V tolerant output	V_{OL}	I_{OL} = 0 mA			0.1	V
High-level output voltage						
LVTTL output type	V_{OH}	I_{OH} = 0 mA	V_{DD} − 0.1			V
TTL 5 V tolerant output	V_{OH}	I_{OH} = 0 mA	V_{DD} − 0.2			V

Note 1. Static current consumption increases when an I/O block with an on-chip pull-up/pull-down resistor is used (see **CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS** for details).

Note 2. For TTL 5 V tolerant and CMOS 5 V tolerant three-state output buffers and I/O buffers, the OFF state current of the output increases slightly in order to bias the 5 V protection circuit.

Note 3. If the TTL 5 V tolerant and CMOS 5 V tolerant output buffers are pulled up at a voltage higher than the supply voltage of the LSI, a sink current flows from the output pins to the internal circuitry of the LSI.

Note 4. The output short-circuit time is 1 second or less per pin of the LSI.

Note 5. The pull-up and pull-down resistances vary depending on the input and output voltages.

Note 6. All the buffers with the same output drive capability have the same specifications.

Note 7. 2.00 mA for the buffer with 5 kΩ pull-up resistor.

Remark The + and − signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by −.

The CMOS 5 V tolerant output buffer structurally has no direct-current output high level.

3.4 Standard Specification 2 V_{DD} = 3.3 ±0.165 V; T_A = 0 to +70°C (T_J = 0 to +100°C)

3.4.1 Recommended operating range

Table 3-7. Recommended Operating Range

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Units
Power supply voltage	V_{DD}			3.135	3.3	3.465	V
High-level input voltage	V_{IH}	LVTTL input buffer LVTTL input buffer with fail-safe function		2.0		V_{DD}	V
Low-level input voltage	V_{IL}			0.0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.5		2.3	V
Negative trigger voltage	V_N			0.9		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
High-level input voltage	V_{IH}	5 V tolerant input buffer		2.0		5.5	V
Low-level input voltage	V_{IL}			0.0		0.8	V
Positive trigger voltage	V_P		Schmitt input	1.5		2.3	V
Negative trigger voltage	V_N			0.9		1.6	V
Hysteresis voltage	V_H			0.3		1.5	V
Input rise time (data)	t_{ri}	Normal input		0		200	ns
Input fall time (data)	t_{fi}			0		200	ns
Input rise time (clock)	t_{ri}	Normal input		0		4	ns
Input fall time (clock)	t_{fi}			0		4	ns
Input rise time	t_{ri}	Schmitt input		0		10	ms
Input fall time	t_{fi}			0		10	ms

Remark If a signal that rises or falls dully or a signal with noise exceeding the threshold value is to be input, use a Schmitt trigger input buffer because noise on the internal signal line of the chip may cause malfunctioning. Clock input in particular is easily influenced by noise, so that a separate recommended operating range is specified. If the rise or fall time increases beyond this range, likewise use a Schmitt trigger input buffer. Note that, if a noise exceeding the hysteresis voltage is input, malfunctioning may occur. Exercise care in laying out pins as fluctuation on the power supply due to simultaneous switching of output buffers which degrades the capability of the Schmitt trigger input buffer.

3.4.2 DC characteristics

The values of each item are the same as the values in **Table 3-6 DC Characteristics**.

See **Table 3-6**.

3.5 AC Characteristics

Table 3-8 shows the AC characteristics.

The maximum operating clock frequency ($f_{MAX.}$) of the internal cell toggle flip-flop is the value of the toggle frequency (f_{tog}) in the table. Note that the maximum operating clock frequency ($f_{MAX.}$) varies in the actual circuit according to the circuit configuration.

Table 3-8. AC Characteristics (V_{DD} = 3.3 ±0.3 V; T_A = –40 to +85°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Maximum toggle frequency	f_{tog}	Internal toggle F/F (Fan-outs = 2)	670			MHz
Propagation delay time	t_{PD}	Internal gate				
		Fan-outs = 1; Wiring length = 0 mm		94		ps
		Fan-outs = 1; Standard wiring length		131		ps
		Standard load		108		ps
		Internal gate (power gate)				
		Fan-outs = 1; Standard wiring length		107		ps
		Standard load		94		ps
		Input buffer				
		Fan-outs = 1; Standard wiring length		229		ps
		Standard load		222		ps
		Output buffer (FO01) C_L = 15 pF		1,396		ps
Output rise time	t_r	Output buffer (FO01) C_L = 15 pF		2,391		ps
Output fall time	t_f	Output buffer (FO01) C_L = 15 pF		1,872		ps

Remark Standard load: Fan-outs = 2; Wiring length = 0 mm
Standard wiring length: 145 μm/1 pin-pair

3.6 Pin Capacitance

Pin capacitance (C_T) is the sum of the interface block capacitance and the package characteristic capacitance. Table 3-9 shows the capacitance of the interface blocks (C_B). Table 3-10 shows the capacitance of each package (C_P).

The pin capacitance is calculated by the following formula:

Pin capacitance (C_T) = interface block capacitance (C_B) + capacitance of each package (C_P)

Table 3-9. Capacitance of Interface Block (C_B)

(a) Input buffer

Interface Level	$C_{B(MIN.)}$ (pF)		$C_{B(MAX.)}$ (pF)	
	Normal	With Fail-Safe	Normal	With Fail-Safe
LVTTL	3.25	2.84	3.97	3.48
5 V tolerant	6.25	–	6.97	–

Remark V_{DD} = 0 V; T_J = 25°C; f = 1 MHz

(b) Output buffer/bidirectional buffer

Interface Level		C_B (pF)							
		1 mA	2 mA	3 mA	6 mA	9 mA	12 mA	18 mA	24 mA
LVTTL	MIN.	–	–	3.25	3.25	3.25	3.25	3.25	3.25
	MAX.	–	–	3.97	3.97	3.97	3.97	3.97	3.97
TTL 5 V tolerant	MIN.	6.25	6.25	6.25	6.25	6.25	6.25	6.25	6.25
	MAX.	6.97	6.97	6.97	6.97	6.97	6.97	6.97	6.97
CMOS 5 V tolerant	MIN.	–	–	6.25	6.25	6.25	6.25	6.25	6.25
	MAX.	–	–	6.97	6.97	6.97	6.97	6.97	6.97

Remark V_{DD} = 0 V; T_J = 25°C; f = 1 MHz

<R>

Table 3-10. Capacitance of Packages (C_P)

Package		Lead Pitch	Body Size	C_P (pF)
TQFP	48	0.5 mm	7 × 7 mm	0.9
	64	0.5 mm	10 × 10 mm	0.9
LQFP	44	0.8 mm	10 × 10 mm	0.7
	100	0.5 mm	14 × 14 mm	1.0
	144	0.5 mm	20 × 20 mm	1.5
	160	0.5 mm	24 × 24 mm	1.5
	176	0.5 mm	24 × 24 mm	1.5
	216	0.4 mm	24 × 24 mm	1.5
PBGA	256	1.00 mm, full grid	17 × 17 mm	0.6 to 1.2
	676	1.00 mm, full grid	27 × 27 mm	0.6 to 1.2
FPBGA	80	0.8 mm, perimeter	9 × 9 mm	0.6 to 1.1
	108	0.8 mm, perimeter	11 × 11 mm	0.6 to 1.1
	160	0.8 mm, perimeter	13 × 13 mm	0.8 to 1.3
	161	0.65 mm, perimeter	10 × 10 mm	0.6 to 1.1
	208	0.8 mm, perimeter	15 × 15 mm	0.8 to 1.3
	304	0.8 mm, perimeter	19 × 19 mm	0.8 to 1.3
FPBGA (0.5 mm pitch)	48	0.5 mm	4.38 × 4.38 mm	Under development
	65	0.5 mm	6 × 6 mm	Under development
	97	0.5 mm	6 × 6 mm	Under development
	144	0.5 mm	7 × 7 mm	Under development
SSOP	20	0.65 mm	6.65 × 6.1 mm	Under evaluation
	30	0.65 mm	9.85 × 6.1 mm	Under evaluation

CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS

This chapter explains the methodology for calculating power consumption and propagation delay time.

4.1 Estimating Static Current Consumption

4.1.1 Estimating static current consumption

Only a minute leakage current flows from the power supply to GND in the standby state. If a 5 V output block or an I/O buffer with an on-chip pull-up/pull-down resistor is not used, the static current consumption is equal to the leakage current. On the other hand, if an I/O buffer with an on-chip pull-up/pull-down resistor is used, the static current consumption increases due to direct current flowing through that resistor according to the signal level.

Moreover, for TTL 5 V tolerant and CMOS 5 V tolerant output buffers, current flows from the output pin into the LSI if the output buffer is pulled up at the 5 V power supply, even if the output level is high.

To calculate static current consumption, use the following equation:

$$I_{DDS\,(MAX.)} = I_L + I_{U50} \times \ell + I_{D50} \times m + I_{U5} \times n + I_{RT} \times p + I_{RC} \times q \quad (\mu A)$$

where:

<R>

- I_L: Leakage current: μPD65941, 65942, 65943, 65944, 65945, 65946, 65948, 65949, 66942 (300 μA)
  μPD65951, 65954, 65956, 65961, 65964, 65966 (400 μA)
  μPD65958, 65968 (800 μA)
- I_{U50}: Current consumption of 50 kΩ on-chip pull-up resistor (190 μA)
- I_{D50}: Current consumption of 50 kΩ on-chip pull-down resistor (190 μA)
- I_{U5}: Current consumption of 5 kΩ on-chip pull-up resistor (1,900 μA)
- I_{RT}: Current flowing into TTL 5 V tolerant output buffer output
  Output level
  Low level (V_{PU}/R_{PU} A)
  High level (see **4.1.2 Output influx current (I_R)**)
  High impedance (14 μA)
- I_{RC}: Current flowing into CMOS 5 V tolerant output buffer output
  Output level
  Low level (V_{PU}/R_{PU} A)
  High level (see **4.1.2 Output influx current (I_R)**)
  High impedance (18 μA)
- ℓ: Number of signal low levels in an I/O buffer with 50 kΩ on-chip pull-up resistor
- m: Number of signal high levels in an I/O buffer with 50 kΩ on-chip pull-up resistor
- n: Number of signal low levels in an I/O buffer with 5 kΩ on-chip pull-up resistor
- p Number of TTL 5 V tolerant output buffers pulled up by the 5 V power supply
- q Number of CMOS 5 V tolerant output buffers pulled up by the 5 V power supply
- V_{PU} 5 V pull-up voltage
- R_{PU} Pull-up resistance

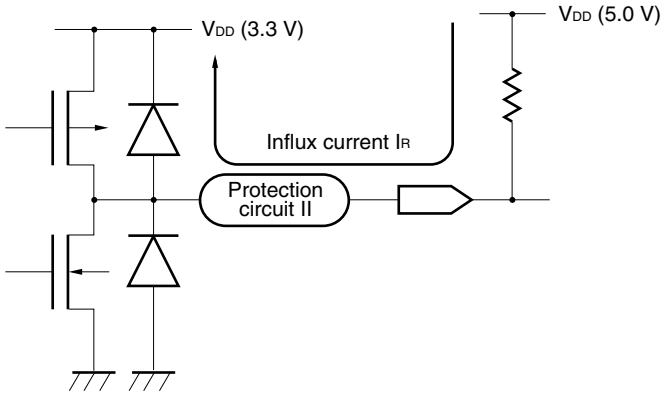
If a 3-state circuit is included in the circuitry, the effect of the OFF-state output current must also be considered.

4.1.2 Output influx current (I_R)

The TTL 5 V tolerant and CMOS 5 V tolerant output buffers are blocks used when a 5 V output level is required. In a TTL 5 V tolerant output block, current flows into the LSI if pulled up at 5 V to make the output a direct-current flow. A direct-current high level cannot be implemented for the CMOS 5 V tolerant output buffer, but a small influx current is generated. (However, an influx current outside the OFF state leakage cannot flow if the output is at high impedance.)

Figure 4-1. Output Influx Current (I_R) Influx Route

(a) CMOS 5 V tolerant output buffer



(b) TTL 5 V tolerant output buffer

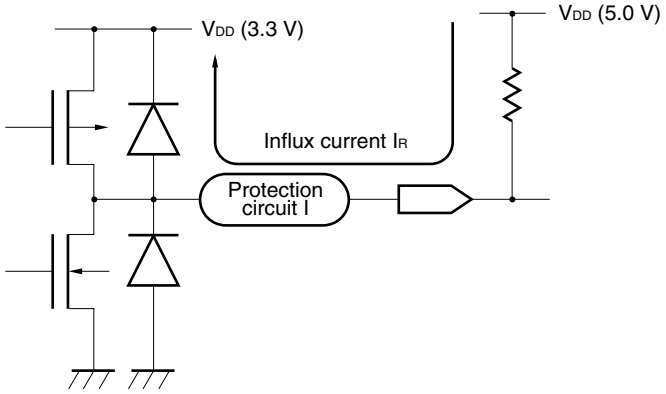
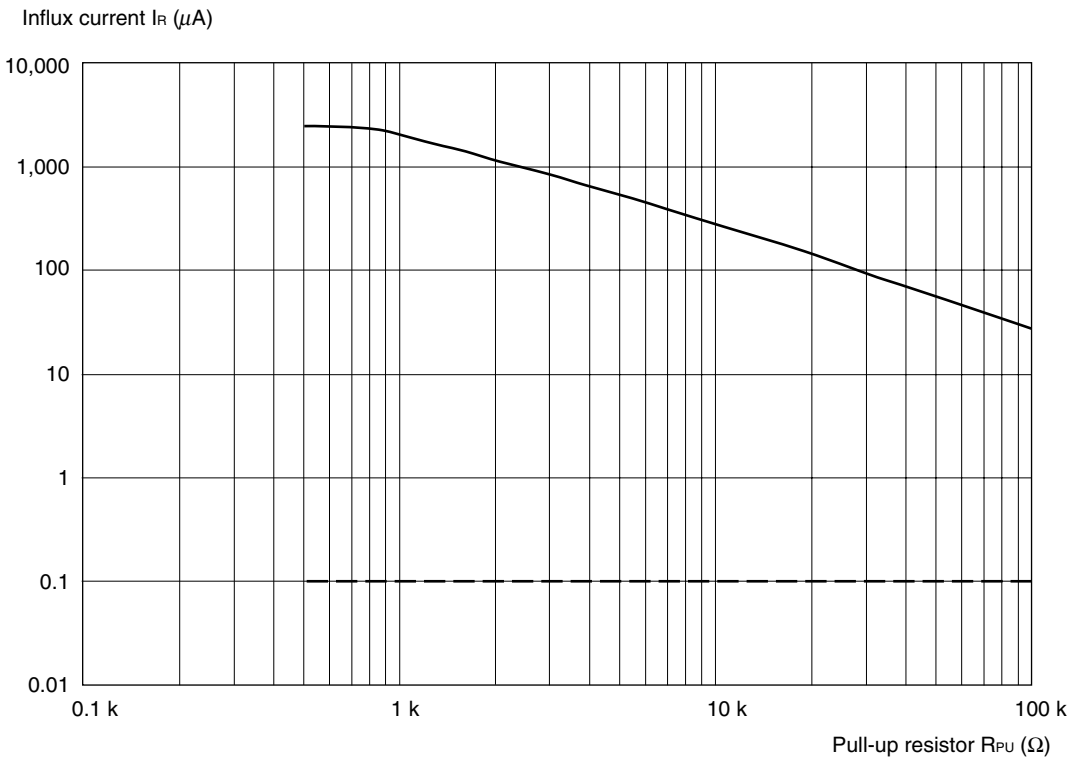


Figure 4-2 shows the influx current determined by the pull-up resistor. Figure 4-3 shows an output waveform based on a representative pull-up resistance value. The measurement circuit for the output waveform and the conditions are shown in Figure 4-4.

Figure 4-2. Output Influx Current

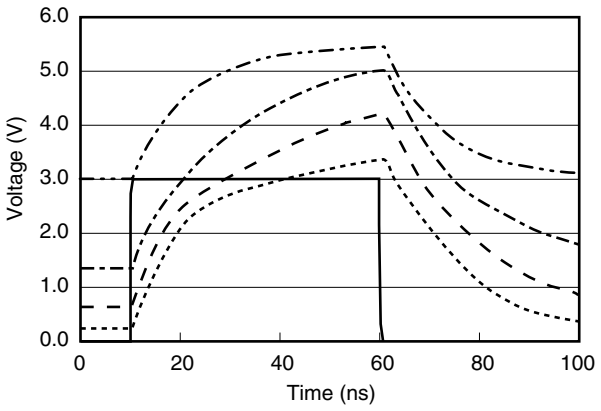


Conditions

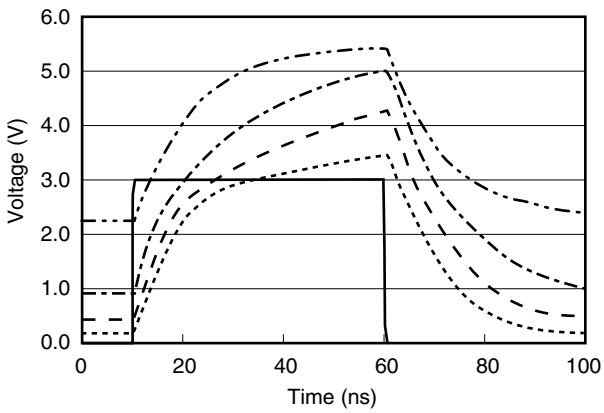
V_{DD} = 3.0 V, V_{PU} = 5.5 V
T_J = 125°C
Worst case

Figure 4-3. 5 V Tolerant Output Buffer Output Waveform (1/3)

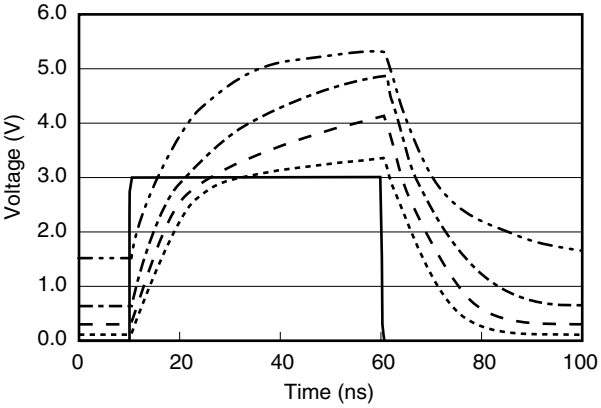
(a) TTL 1 mA buffer



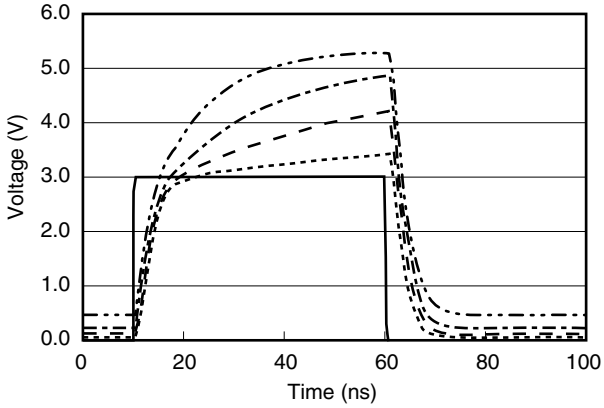
(b) TTL 2 mA buffer



(c) TTL 3 mA buffer



(d) TTL 6 mA buffer



Remark 1. ——— Input waveform

- ·-·-·-·- R_{PU} = 0.5 kΩ
- —·—·— R_{PU} = 1.0 kΩ
- – – – – R_{PU} = 2.0 kΩ
- -------- R_{PU} = 5.0 kΩ

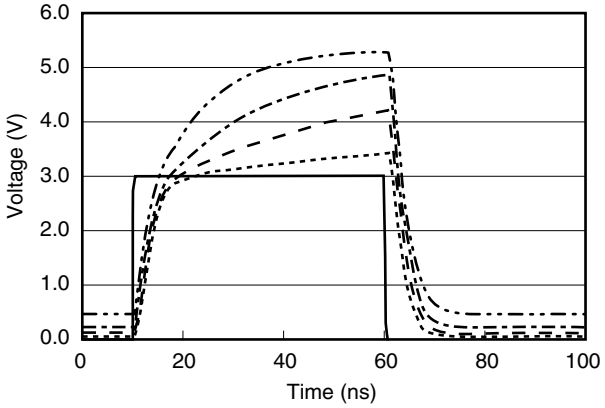
Remark 2. Measurement conditions

V_{DD} = 3.0 V, T_J = 125°C

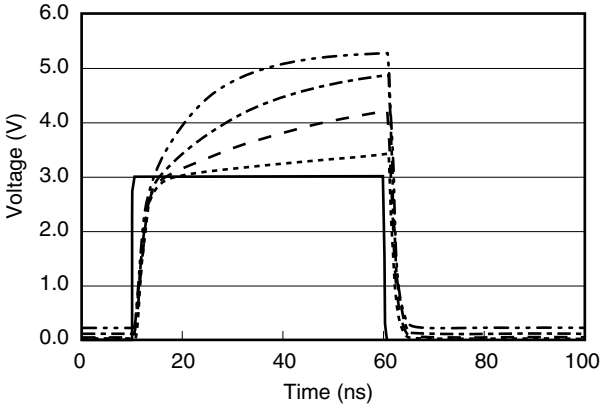
V_{PU} = 5.5 V

Figure 4-3. 5 V Tolerant Output Buffer Output Waveform (2/3)

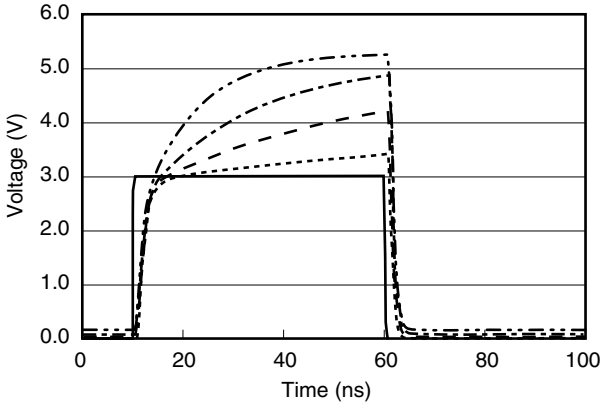
(e) TTL 9 mA buffer



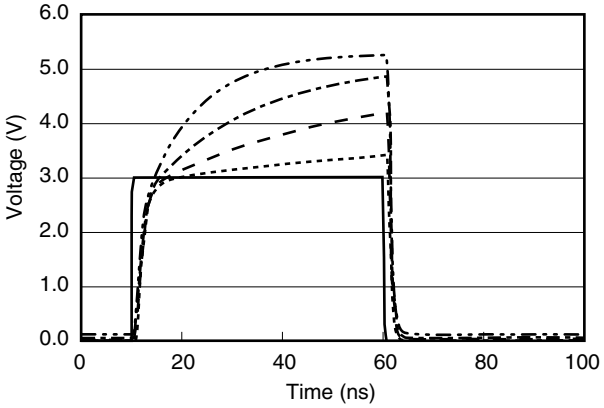
(f) TTL 12 mA buffer



(g) TTL 18 mA buffer



(h) TTL 24 mA buffer



Remark 1. ——— Input waveform

- ·-·-·- R_{PU} = 0.5 kΩ
- —·—·— R_{PU} = 1.0 kΩ
- – – – – R_{PU} = 2.0 kΩ
- -------- R_{PU} = 5.0 kΩ

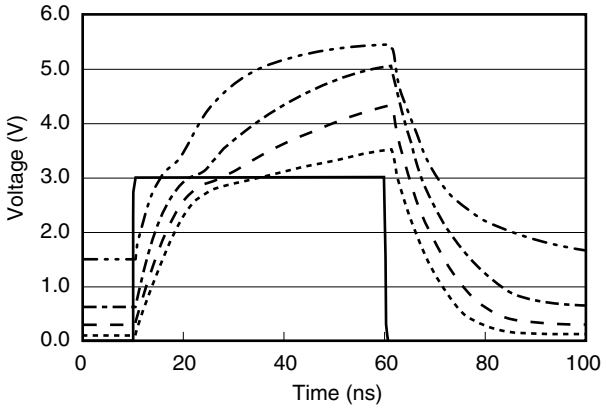
Remark 2. Measurement conditions

V_{DD} = 3.0 V, T_J = 125°C

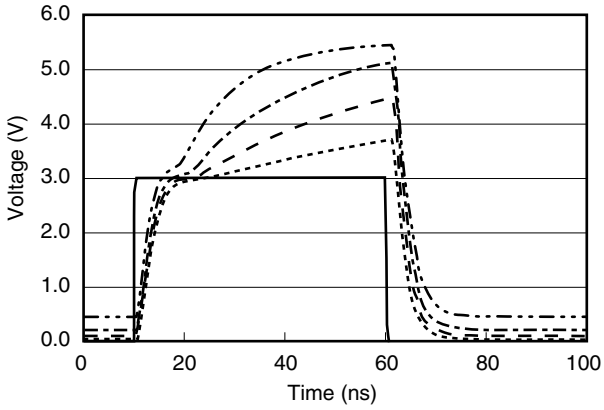
V_{PU} = 5.5 V

Figure 4-3. 5 V Tolerant Output Buffer Output Waveform (3/3)

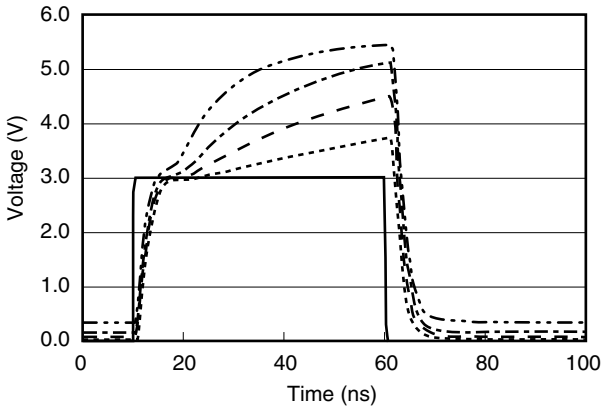
(i) CMOS 3 mA buffer



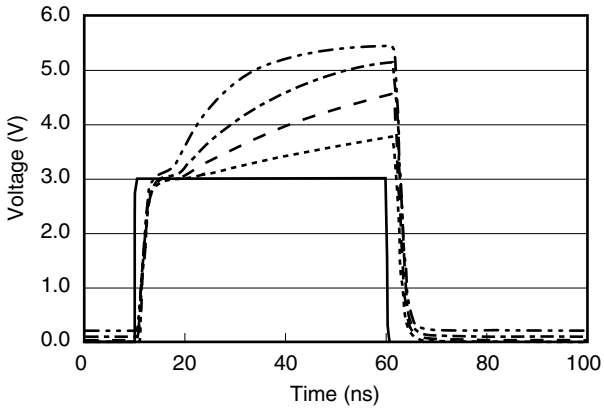
(j) CMOS 6 mA buffer



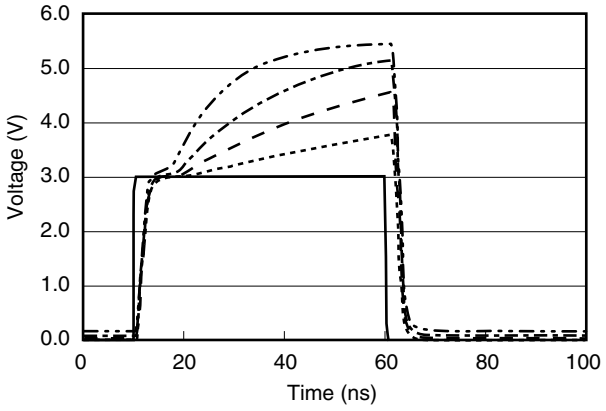
(k) CMOS 9 mA buffer



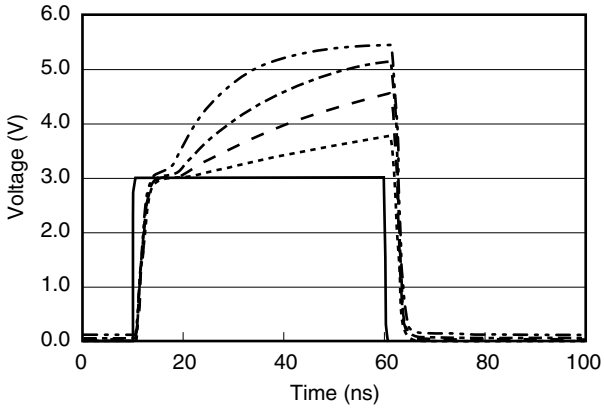
(l) CMOS 12 mA buffer



(m) CMOS 18 mA buffer



(n) CMOS 24 mA buffer



Remark 1. ——— Input waveform

-·-·-·- R_{PU} = 0.5 kΩ

-·-·-·- R_{PU} = 1.0 kΩ

– – – – R_{PU} = 2.0 kΩ

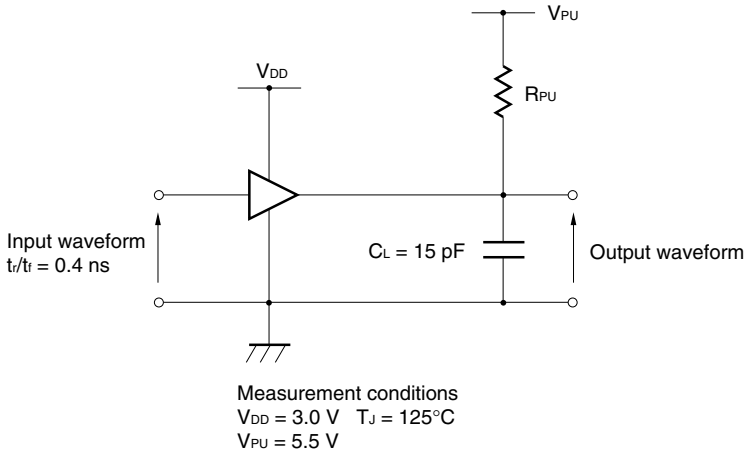
--------- R_{PU} = 5.0 kΩ

Remark 2. Measurement conditions

V_{DD} = 3.0 V, T_J = 125°C

V_{PU} = 5.5 V

Figure 4-4. Measurement Circuit



4.2 Input Through Current

If the input voltage V_{IN} is the same as the power supply voltage V_{DD}, the input leakage current will be the same as the value listed in **CHAPTER 3 PRODUCT SPECIFICATIONS**. However, if the input voltage is lower than the power supply voltage, or if the input voltage is higher than the GND level, then a current will flow from the P-channel via the N-channel. This current is called the input through current. Figures 4-5 to 4-8 show the input through current (reference value) of a LVTTL interface with V_{DD} = 3.6 V, of a LVTTL Schmitt interface with V_{DD} = 3.6 V, of a 5 V tolerant interface with V_{DD} = 6.0 V, and of a 5 V tolerant Schmitt interface with V_{DD} = 6.0 V, respectively.

Figure 4-5. Input Through Current (3.3 V Input)

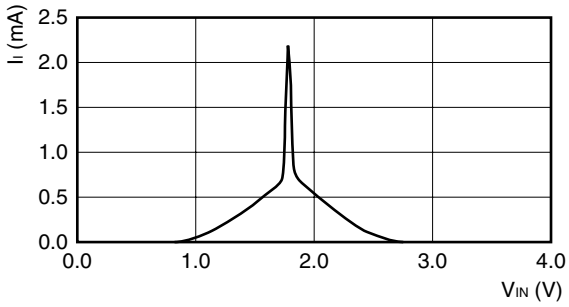


Figure 4-6. Input Through Current (3.3 V Schmitt Input)

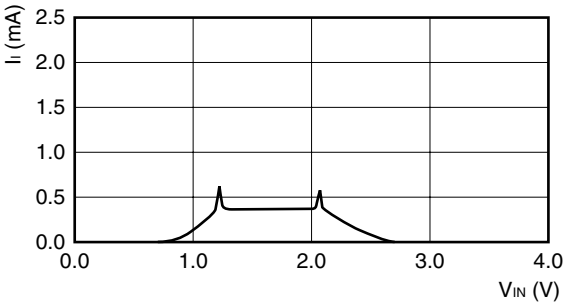


Figure 4-7. Input Through Current (5 V Input)

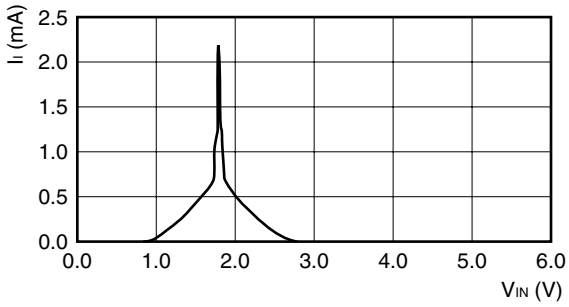
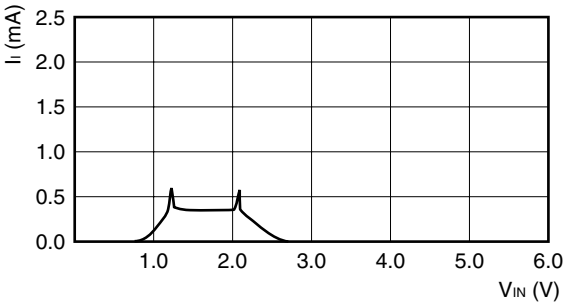


Figure 4-8. Input Through Current (5 V Schmitt Input)



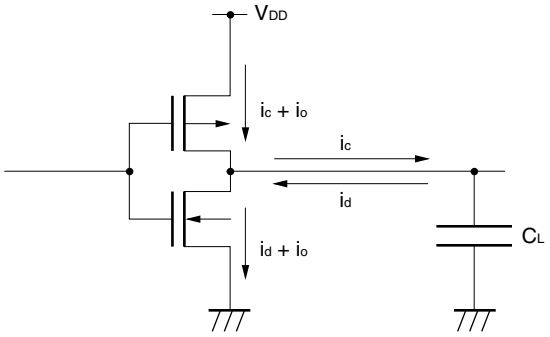
4.3 Power Consumption

Although CMOS device transistors consume less power than bipolar devices, they still consume a considerable amount of power if the circuit scale is large and the operating frequency is high. Because the temperature of an LSI (chip), which has a significant influence on the reliability (life) of the LSI, rises with power consumption, it is necessary to hold the power consumption of the LSI below a maximum.

4.3.1 Causes of power consumption

The current consumption is the sum of the following values, like the standard CMOS devices:

- Charge current of load capacitance connected to each transistor: i_c
- Discharge current of load capacitance connected to each transistor: i_d
- Through current when each transistor is switching: i_o
- Leakage current of the device: I_L



Because there is no charge, discharge, or through current when the LSI is not operating, the power consumption of the chip is determined by the leakage current of the entire device. Inasmuch as the charge, discharge, and through currents become extremely large compared with the leakage current when the LSI is operating, the effect of leakage current can be ignored in the chip power consumption.

When the output rise (fall) time of each transistor is extremely fast compared with the input rise (fall) time, the through current increases greatly. However, through current is normally proportional to the charge and discharge currents.

4.3.2 Estimating power consumption

Power consumption is determined by the charge, discharge, and through currents of each transistor.

However, as it is problematic to define each transistor state, a rough calculation of power consumption is made for each type of block.

The calculated results of the formulas shown below are values at V_{DD} = 3.3 V and T_A = 25°C; thus, adjustments must be made if the power supply or the temperature is different.

Total power consumed $P_D = \Sigma P_{DCELL} + \Sigma P_{RAM} + \Sigma P_{DI} + \Sigma P_{CTS} + \Sigma P_{PLL} + \Sigma P_{GTL} + \Sigma P_{DO} + \Sigma P_{OSC}$

(a) ΣP_{DCELL} Internal cell power consumption (excluding the cells used by memory, clock tree synthesis, and interface block)

$$\Sigma P_{DCELL} = \Sigma P_{DGate} + \Sigma P_{DLatch} + \Sigma P_{DF/F} + \Sigma P_{DT} \quad (\mu W)$$

See **APPENDIX A POWER CONSUMPTION** for details.

(b) ΣP_{RAM} Memory block power consumption

RAM block power consumption

$$\Sigma P_{RAM} = \Sigma(P_{RM} \times f_{RM} \times R_{RM} \times P_{WM} \times f_{WM} \times R_{WM}) \quad (mW)$$

where:

- P_{RM}: Unit power consumption during read (mW/MHz)[Note 1]
- f_{RM}: Operating frequency during read
- R_{RM}: Operating rate during read[Note 2]
- P_{WM}: Unit power consumption during write (mW/MHz)[Note 1]
- f_{WM}: Operating frequency during write
- R_{WM}: Operating rate during write[Note 2]

(c) ΣP_{DI} Input buffer and bidirectional buffer power consumption

The following pertains to the input part.

$$\Sigma P_{DI} = \Sigma(P_I \times f + P_{CONST}) \times Buffer \quad (\mu W)$$

where:

- f: Operating frequency (MHz)
- Buffer: Number of operating input buffers and bidirectional buffer inputs at frequency f
  If input buffer operation is intermittent, use the average operating frequency (f_A)[Note 3]
- P_I: Power consumption for each input buffer (μW/Buffer/MHz)
  See **Table 4-1**.
- P_{CONST}: Constant power consumption[Note 4]

Table 4-1. Power Consumption by Input Buffer

Representative Block Type	P_I
FI01, FIA1, FIV1, BP3I, BP5I, FI0P, FI0Q	3.95
FIS1, FIE1, FIF1	7.85

Remark The same types of buffers have the same value.

(d) ΣP_{CTS} Clock tree synthesis power consumption

$$\Sigma P_{CTS} = \Sigma(28.32 + 0.786 \times 10^{-1} \times FF) \times f \times 10.86 \times 10^{-6} \quad (W)$$

where:

f: Operating frequency (MHz)

FF: Flip-flop

Remark See **Table 5-3**.

(e) ΣP_{PLL} Digital PLL power consumption

$$\Sigma P_{PLL} = \Sigma(P_{PL} \times f) \quad (mW)$$

where:

f: Operating frequency (MHz)

P_{PL}: Digital PLL power consumption (See **Table 4-2**)

Table 4-2. Digital PLL Power Consumption

Block Type	P_{PL}
F9E4	1.18 mW

(f) ΣP_{DO} Output and bidirectional buffer power consumption

$$\Sigma P_{DO} = \Sigma\{(P_O + P_{CO} \times C_L) \times f + P_{CONST}\} \times Buffer \quad (mW)$$

where:

P_O: Power consumption for each output buffer (without load) (mW/MHz)
See **Table 4-3**.

P_{CO}: Power consumption for each output buffer (load dependent) (mW/MHz/pF)
See **Table 4-3**.

C_L: Load capacitance (pF)

f: Operating frequency (MHz). Use the average operating frequency (f_A) when output buffers are operated intermittently[Note 3].

Buffer: Number of output buffers and bidirectional buffers operating at frequency f (output part)

P_{CONST}: Constant power consumption[Note 4]

Table 4-3. Output Buffer Power Consumption

LVTTL Output			TTL 5 V Tolerant Output			CMOS 5 V Tolerant Output		
Representative Block	P_O	P_{CO}	Representative Block	P_O	P_{CO}	Representative Block	P_O	P_{CO}
FO09	0.099	0.011	FV0A	0.277	0.011	FY09	0.338	0.010
FO04	0.117	0.012	FV0B	0.252	0.011	FY04	0.346	0.011
FO01	0.121	0.012	FV09	0.272	0.011	FY01	0.346	0.011
FO02	0.124	0.012	FV04	0.295	0.011	FY02	0.359	0.012
FO03	0.134	0.012	FV01	0.301	0.011	FY03	0.368	0.011
FO06	0.144	0.011	FV02	0.310	0.011	FY06	0.381	0.011
BP3O	0.134	0.012	FV03	0.321	0.011			
			FV06	0.332	0.011			
			BP5O	0.332	0.011			
FE04	0.114	0.012	FW02	0.310	0.011	FZ02	0.350	0.011
FE01	0.117	0.012	FW03	0.312	0.011	FZ03	0.354	0.011
FE02	0.121	0.012	FW06	0.317	0.011	FZ06	0.360	0.011
FE03	0.128	0.012						
FE06	0.132	0.011						

Remark The same types of buffers have the same value.

The output level of TTL 5 V tolerant output is defined to be 3.3 V, and that of the CMOS 5 V tolerant output is defined to be 5.0 V.

The following equation should be used when 5 V are used to pull up the TTL 5 V output.

$$P_{DO\ (5.0\ V)} = 1.65 \times P_{DO} \quad (mW)$$

The following equation should be used when 3.3 V are used to pull up the CMOS 5 V tolerant output.

$$P_{DO\ (3.3\ V)} = P_{DO}/1.65 \quad (mW)$$

(g) ΣP_{GTL} GTL+ power consumption

$$\Sigma P_{GTL} = \Sigma P_{GI} \times \text{Buffer} + \Sigma P_{GO} \times \text{Buffer} \quad (mW)$$

where:

P_{GI}: Input part power consumption (mW/Buffer)
See **Table 4-4**.

P_{GO}: Output part power consumption (mW/Buffer)

Table 4-4. Power Consumption of GTL+ Input

Condition	Current Consumption (mA)	P_{GI} (mW/Buffer)
IEN = 1, A = 0		
IEN = 1, A = 1		
IEN = 0		

Remark Values are under study.

GTL+ output power consumption

P_{GO} = (mW/Buffer)	(Under study)

(h) ΣPosc Oscillator power consumption (Reference value)

The power consumption (reference value) is shown in Table 4-5, and circuit diagram is shown in Figure 4-9.

Table 4-5. Oscillator Power Consumption (Reference Values)

Frequency	External Constant Used				Duty (%)	Vstart (V)	Vhold (V)	P_{OSC} (mW)
	C_{IN} (pF)	C_{OUT} (pF)	LT (μH)	CT (μF)				
4 MHz	13	23	–	–	51.8	1.73	1.31	16.64
24 MHz	13	13	–	–	51.4	1.83	1.50	21.21
32 MHz	3	13	4.7	0.1	51.7	2.22	1.75	24.99
48 MHz	3	13	4.7	0.1	52.8	2.37	2.04	30.14

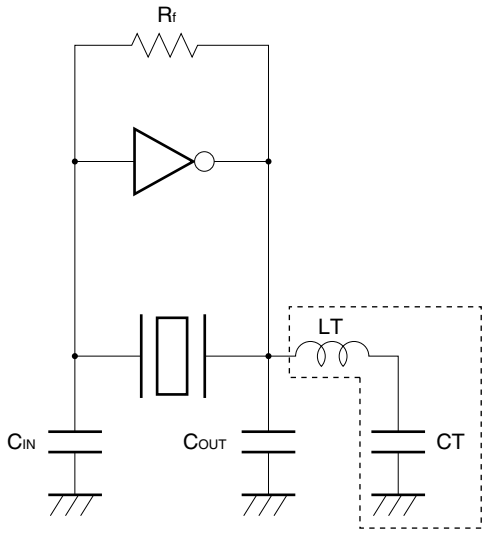
Caution The values in the table are for reference only because the actual values vary greatly depending on the resonator and constant.
To determine the power consumption, evaluation using an evaluation sample is necessary.

Remark 1. The values indicated for Duty, Vstart, Vhold, and P_{OSC} (power consumption) are the worst-case values (V_{DD} = 3.6 V, T_A = 125°C).

Remark 2. The 32 MHz or 48 MHz resonator is used in overtone mode.

Remark 3. The values of external constants C_{IN} and C_{OUT} include a jig capacitance of 3 pF.

Figure 4-9. Oscillator Circuit Diagram

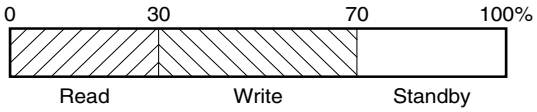


Remark The section within the broken lines is the overtone circuit.

Note 1. Unit power consumption

The numerical values are listed in **4.3.3 Unit power consumption of memory** and **CMOS-9HD Series, EA-9HD Series Memory Block Library (A13071E)**.

Note 2. Write and read operating factors



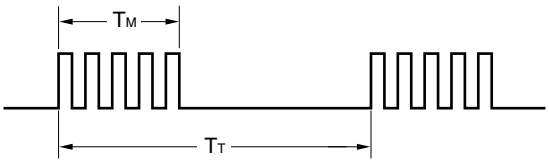
For example, if the RAM operating percentage is as shown in the figure above, then,

R_{RM} = 0.3 and R_{WM} = 0.4

Note 3. Average operating frequency (f_A)

If operation is intermittent, the average operating frequency (f_A) can be investigated.

$$f_A = f_M \times T_M \div T_T$$



where:

T_M: Actual operating interval

T_T: Intermittent operating cycle

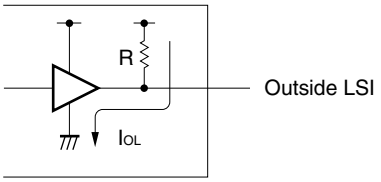
f_M: Operating frequency of actual operating interval

Note 4. Constant power consumption

If direct current is flowing through the input, output, and bidirectional buffers, a constant power consumption is added.

Example 1. Direct current via the pull-up/pull-down resistor

$$P_{CONST} = (V_{DD}^2/R) \times A$$



where:

V_{DD}: Power supply voltage

R: Pull-up/pull-down resistance. Use a typical value if the resistor is on board the LSI

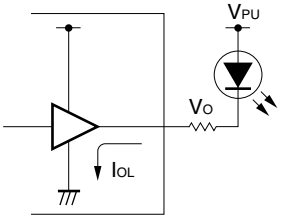
A: Operating factor

Low-level percentage when using a pull-up resistor, or high-level percentage when using a pull-down resistor

The user should specify the operating factor based on the circuit specification

Example 2. To drive for items that require a large current, such as LEDs

$$P_{CONST} = V_O \times I_O \times A$$



where:

A: Percentage of LED ON time

V_{PU}: Pull-up voltage

4.3.3 Unit power consumption of memory

(1) High-density single-port RAM

Refer to **Table 4-6 Unit Power Consumption of High-Density Single-port RAM**.

Table 4-6. Unit Power Consumption of High-Density Single-port RAM

(Unit: mW/MHz)

RAM	Word	bit	P_{WM}	P_{RM}	RAM	Word	bit	P_{WM}	P_{RM}
RB47	16	4	0.018	0.014	RBC7	16	16	0.072	0.056
RB49	32	4	0.019	0.015	RBC9	32	16	0.076	0.060
RB4B	64	4	0.038	0.030	RBCB	64	16	0.064	0.046
RB4D	128	4	0.023	0.018	RBCD	128	16	0.092	0.072
RB4F	256	4	0.046	0.036	RBCF	256	16	0.138	0.110
RB4H	512	4	0.092	0.072	RBCH	512	16	0.276	0.220
RB4M	1,024	4	0.184	0.144	RBCM	1,024	16	0.194	0.136
RB4S	2,048	4	0.368	0.288	RBEB	64	20	0.080	0.058
RB4U	4,096	4	0.736	0.576	RBED	128	20	0.160	0.116
RB87	16	8	0.036	0.028	RBEF	256	20	0.194	0.134
RB89	32	8	0.038	0.030	RBEH	512	20	0.388	0.268
RB8B	64	8	0.032	0.023	RBEM	1,024	20	0.236	0.164
RB8D	128	8	0.046	0.036	RBH7	16	32	0.144	0.112
RB8F	256	8	0.069	0.055	RBH9	32	32	0.152	0.120
RB8H	512	8	0.138	0.110	RBHB	64	32	0.128	0.092
RB8M	1,024	8	0.097	0.068	RBHD	128	32	0.184	0.144
RB8S	2,048	8	0.194	0.136	RBHF	256	32	0.276	0.220
RBAB	64	10	0.040	0.029	RBHH	512	32	0.552	0.440
RBAD	128	10	0.080	0.058	RBKB	64	40	0.160	0.116
RBAF	256	10	0.097	0.067	RBKD	128	40	0.320	0.232
RBAH	512	10	0.194	0.138	RBKF	256	40	0.388	0.268
RBAM	1,024	10	0.118	0.082	RBKH	512	40	0.776	0.536
RBAS	2,048	10	0.236	0.164					

Remark P_{WM}: Power consumed during write
P_{RM}: Power consumed during read

(2) High-density dual-port RAM

Refer to **Table 4-7 Unit Power Consumption of High-Density Dual-port RAM**.

Table 4-7. Unit Power Consumption of High-Density Dual-port RAM

(Unit: mW/MHz)

RAM	Word	bit	P_{WM}	P_{RM}	RAM	Word	bit	P_{WM}	P_{RM}
R947	16	4	0.023	0.016	R9C7	16	16	0.092	0.064
R949	32	4	0.030	0.020	R9C9	32	16	0.120	0.080
R94B	64	4	0.060	0.040	R9CB	64	16	0.108	0.082
R94D	128	4	0.040	0.028	R9CD	128	16	0.160	0.112
R94F	256	4	0.080	0.056	R9CF	256	16	0.248	0.182
R94H	512	4	0.160	0.112	R9CH	512	16	0.496	0.364
R94M	1,024	4	0.320	0.224	R9CM	1,024	16	0.318	0.210
R94S	2,048	4	0.640	0.448	R9EB	64	20	0.130	0.100
R94U	4,096	4	1.280	0.896	R9ED	128	20	0.260	0.200
R987	16	8	0.046	0.032	R9EF	256	20	0.294	0.218
R989	32	8	0.060	0.040	R9EH	512	20	0.588	0.436
R98B	64	8	0.054	0.041	R9EM	1,024	20	0.388	0.246
R98D	128	8	0.080	0.056	R9H7	16	32	0.184	0.128
R98F	256	8	0.124	0.091	R9H9	32	32	0.240	0.160
R98H	512	8	0.248	0.182	R9HB	64	32	0.216	0.164
R98M	1,024	8	0.159	0.105	R9HD	128	32	0.320	0.224
R98S	2,048	8	0.318	0.210	R9HF	256	32	0.496	0.364
R9AB	64	10	0.065	0.050	R9HH	512	32	0.992	0.728
R9AD	128	10	0.130	0.100	R9KB	64	40	0.260	0.200
R9AF	256	10	0.147	0.109	R9KD	128	40	0.520	0.400
R9AH	512	10	0.294	0.218	R9KF	256	40	0.588	0.436
R9AM	1,024	10	0.194	0.123	R9KH	512	40	1.176	0.872
R9AS	2,048	10	0.388	0.246					

Remark P_{WM}: Power consumed during write
P_{RM}: Power consumed during read

(3) Compiled RAM (Single-port RAM, Dual-port RAM)

If memory is created by OPENCAD, a data sheet will be created in the PostScript format (the file name is <RAM block name>.ps). For the power consumption, see the data sheet.

4.3.4 Compensation method

The results calculated by the formulas in **4.3.2 Estimating power consumption** are values for V_{DD} = 3.3 V and T_A = 25°C. If different power supply or temperature specifications are used, adjustments must be calculated using the following equation.

$$P_W = P_D \times K_1 + \Sigma P_{CONST} \times K_2$$

where:

- P_D: Calculated result of total power consumption (including constant power consumption)
- ΣP_{CONST}: Sum of constant power consumption only
- K_1: Compensation coefficient (See **Table 4-8**)
- K_2: Compensation coefficient (See **Table 4-8**)

The TYP. value is usually used to determine the power consumption.

However, the MAX. value is used when high reliability is demanded.

The MAX. value can also be used to calculate the maximum power consumption value in each power supply and temperature specification range.

Table 4-8. Compensation Coefficient

(V_{DD} = 3.3 ±0.3 V, T_A = –40 to +85°C)

Compensation Coefficient	TYP. Value	MAX. Value
K_1	1.00	1.28
K_2	0.00	0.15

4.3.5 Determining power consumption

The power consumption is determined on the basis of whether or not the calculated power consumption (P_D) is within the maximum allowable power consumption (P_{WL}) specified for each package and master.

The maximum allowable power consumption (P_{WL}) specified for each package and master is listed in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)** (Since packages under development are included, be sure to confirm that the package has been released).

$$P_D \leq P_{WL}$$

The values in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)** are for T_A = –40 to +85°C with natural convection. If a different maximum operating ambient temperature is used, the maximum allowable power consumption for the environment used must be calculated by means of the maximum junction temperature ($T_{J\,(MAX.)}$), the maximum ambient temperature ($T_{A\,(MAX.)}$), and the thermal resistance (θ_{ja}) specified for each package and master.

The thermal resistance (θ_{ja}) for each package and master is listed in the tables concerning thermal resistance in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)** (Since packages under development are included, be sure to confirm that the package has been released).

Thermal resistance was measured under the condition of a 90 × 90 mm by 1.6 mm thick sample mounted on a glass-epoxy circuit board.

$$P_{WL} = (T_{J\,(MAX.)} - T_{A\,(MAX.)})/\theta_{ja} \quad (W)$$

Condition: $T_{A\,(MAX.)} \geq 40°C$

4.4 Estimating Propagation Delay Time

4.4.1 Accuracy of propagation delay time

The propagation delay time, t_{PD}, of a CMOS gate array fluctuates due to I/O buffers, internal function blocks, and the following factors:

Factors fluctuating propagation delay time

- Load capacitance (number of fan-outs, wiring capacitance)
- Power supply voltage
- Operating ambient temperature
- Manufacturing variation
- Other circuit-based factors

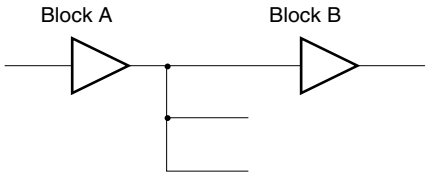
Circuit-based causes other than those related to power supply voltage, operating ambient temperature, and load capacitance include: fluctuation due to the input signal waveform, fluctuation in the equivalent input capacitance of the transfer gate, the Miller effect, and fluctuation in the input threshold voltage. NEC Electronics has introduced delay simulators and static delay calculators, taking these fluctuation factors into consideration as much as possible, so that a more precise propagation delay can be calculated. Thus, rough calculations of propagation delay time made by the user may not match the numerical values listed in the separately published **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

4.4.2 Calculation of propagation delay time

The calculation formula shown below is rough and simplified. The calculation results are comparatively accurate for a load range that satisfies the following conditions. The larger the load capacitance, the larger the error becomes and the smaller the calculated numerical result of the simulator becomes. With this prior understanding, this formula can be used as a guide.

Condition: The sum of the pre-stage F/I of the block, which is the object of the delay calculation, is within 15% of the F/O limit of the pre-stage drive block.

Example



Let Block B be the object of the propagation calculation. The accuracy of the simplified calculation formula is high when the sum of the F/I connected to the output of block A is within 15% of the block A F/O limit.

If these details or the above conditions are not applicable, see **APPENDIX B PROPAGATION DELAY TIME** for methods to improve the calculation accuracy. The propagation data for each block that is needed for the calculation is listed in the **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

(1) Input buffer and internal function block delay

The delay time of the internal function block and memory blocks can be calculated roughly from the load (number of fan-outs) connected to that output pin and the wiring length (wiring capacitance).

$$t_{PD} = t_{LD0} + (\Sigma F/O + \ell) \times t_1 \quad (ns)$$

where:

- t_{LD0}: Delay time of the block itself with F/O = 0 and ℓ = 0
- $\Sigma F/O$: Number of fan-outs of the relevant output pins
- ℓ: Wiring capacitance connected to the relevant output pins (see **4.4.3 Estimating wiring capacitance**.)
- t_1: Delay coefficient of the relevant output pins

(2) Internal path delay

$$t_{PD} = t_{LD0} + \{\Sigma F/O + \ell + (N - 1) \times 0.96\} \times t_1 \quad (ns)$$

where:

- t_{LD0}: Delay time of the block itself with F/O = 0 and ℓ = 0
- $\Sigma F/O$: Number of fan-outs connected to the bus
- N: Sum of three-state output buffers (F531, F532) connected to the bus
- ℓ: Wiring capacitance connected to the relevant output pins (see **4.4.3 Estimating wiring capacitance**.)
- t_1: Delay coefficient of the relevant output pins

(3) Output buffer delay

Using the following equation, the output buffer delay can be roughly calculated from the load capacitance connected to the output pin.

$$t_{PD} = t_{LD0} + T \times C_L \quad (ns)$$

where:

- t_{LD0}: Delay time of the block itself with C_L = 0 pF
- C_L: Load capacitance connected to the relevant output pin
- T: Delay coefficient of the relevant output pin

The delay time of the I/O buffer is calculated based on the following conditions:

- LVTTL output: Threshold voltage = 1.5 V, output swing = 0 to V_{DD}
- 5 V tolerant output: Threshold voltage = 1.5 V, output swing = 0 to V_{DD}

Even in the 5 V tolerant output, the delay time is specified based on the condition of no output pull-up.

4.4.3 Estimating wiring capacitance

In gate arrays, because the placement and routing is performed on the master based on circuit connection data, the physical length of the wiring to be connected as the function block load is not known at the pre-placement/routing stage. The wiring length is therefore assumed and calculated so as to enable calculation of the propagation time before the placement and routing stage. When the actual layout results are statistically processed, the majority of the generated wiring lengths (about 70% of the total wiring) tend to be shorter than the values determined by the assumed wiring length calculation.

Table 4-9 shows the estimated values of the assumed wiring capacitance in the CMOS-9HD Series.

Placement and routing are executed for each macro (in the top hierarchy only) within a determined placement range. Therefore there are considerable differences between intra- and inter-macro wiring lengths. The assumed wiring length in the pre-placement/routing stage is treated by the delay simulator in two categories: intra-macro and inter-macro. Therefore be aware that the values will differ slightly from those in Table 4-9.

<R> **Table 4-9. Wiring Capacitance Estimate (Wiring Length Converted to F/I Value) (1/2)**

(a) 3-layer routing products (1/2)

Master	Pin-Pair Count					
	1	2	3	4	5	6
μPD65941	3.14	5.69	8.24	10.79	13.35	15.90
μPD65942, 66942	3.35	6.56	9.77	12.98	16.18	19.39
μPD65943	3.70	7.59	11.49	15.39	19.28	23.18
μPD65944	3.83	8.01	12.19	16.37	20.56	24.74
μPD65945	3.93	8.38	12.82	17.27	21.71	26.16
μPD65946	4.21	9.19	14.17	19.16	24.14	29.12
μPD65948	4.50	10.06	15.61	21.16	26.72	32.27
μPD65949	4.80	11.08	17.35	23.63	29.91	36.18
μPD65951	5.10	12.00	18.90	25.80	32.70	39.60
μPD65954	5.52	13.06	20.61	28.15	35.69	43.23
μPD65956	5.90	13.98	22.05	30.12	38.19	46.26
μPD65958	6.54	15.65	24.75	33.86	42.97	52.08

(a) 3-layer routing products (2/2)

Master	Pin-Pair Count					
	7	8	9	10	15	20
μPD65941	18.45	21.00	23.55	26.11	38.87	51.63
μPD65942, 66942	22.60	25.81	29.02	32.23	48.27	64.32
μPD65943	27.08	30.97	34.87	38.76	58.24	77.73
μPD65944	28.92	33.10	37.29	41.47	62.38	83.30
μPD65945	30.60	35.05	39.49	43.94	66.16	88.39
μPD65946	34.10	39.09	44.07	49.05	73.97	98.88
μPD65948	37.83	43.38	48.93	54.49	82.26	110.02
μPD65949	42.46	48.73	55.01	61.29	92.67	124.05
μPD65951	46.50	53.40	60.30	67.20	101.70	136.20
μPD65954	50.77	58.32	65.86	73.40	111.11	148.82
μPD65956	54.34	62.41	70.48	78.55	118.91	159.27
μPD65958	61.19	70.29	79.40	88.51	134.05	179.59

<R> **Table 4-9. Wiring Capacitance Estimate (Wiring Length Converted to F/I Value) (2/2)**

(b) 4-layer routing products (1/2)

Master	Pin-Pair Count					
	1	2	3	4	5	6
μPD65961	5.10	11.72	18.33	24.95	31.57	38.19
μPD65964	5.52	12.76	19.99	27.22	34.46	41.69
μPD65966	5.90	13.64	21.39	29.13	36.87	44.61
μPD65968	6.54	15.24	23.94	32.65	41.35	50.05

(b) 4-layer routing products (2/2)

Master	Pin-Pair Count					
	7	8	9	10	15	20
μPD65961	44.80	51.42	58.04	64.66	97.75	130.84
μPD65964	48.92	56.16	63.39	70.62	106.79	142.96
μPD65966	52.35	60.10	67.84	75.58	114.29	153.00
μPD65968	58.75	67.45	76.16	84.86	128.37	171.88

4.4.4 Fluctuation in propagation delay time

The propagation delay time (t_{PD}) of I/O buffers and internal function block fluctuates for a variety of reasons as described in **4.4.1 Accuracy of propagation delay time**. The **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)** indicates the minimum and maximum values under the conditions:

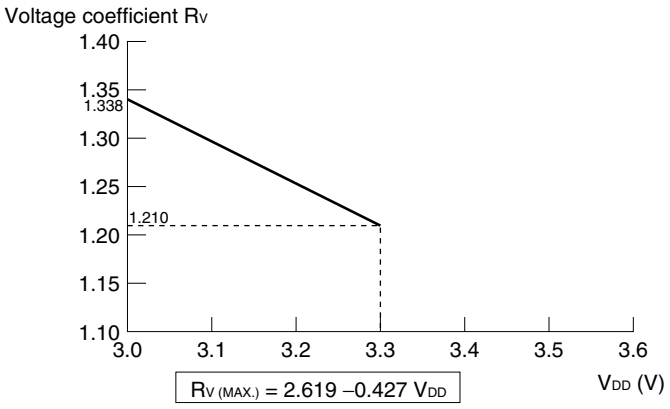
V_{DD} = 3.3 ±0.3 V and T_A = –40 to +85°C (T_J = –40 to +125°C)

The difference between the typical value and these values is called the absolute distribution. The propagation delay is listed for the minimum, typical, and maximum specifications.

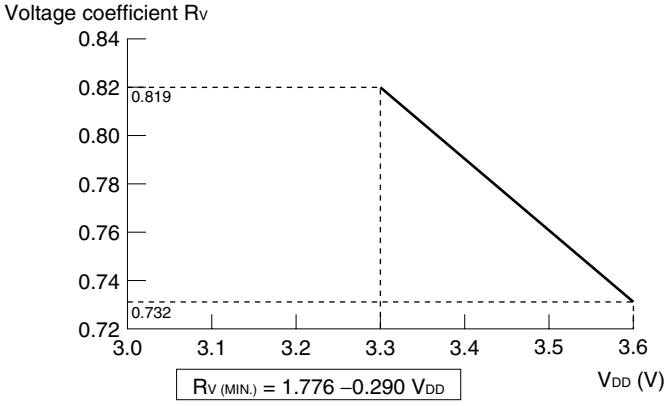
With the CMOS-9HD Series, the absolute distribution of each block is studied to improve the accuracy of calculation of the propagation delay time. Therefore, a uniform absolute distribution cannot be used unlike with conventional products. However, Figure 4-10 (a) through (c) shows, for reference, the dependency of the delay coefficient on power supply voltage and operating junction temperature.

Figure 4-10. Propagation Delay Time (Preliminary)

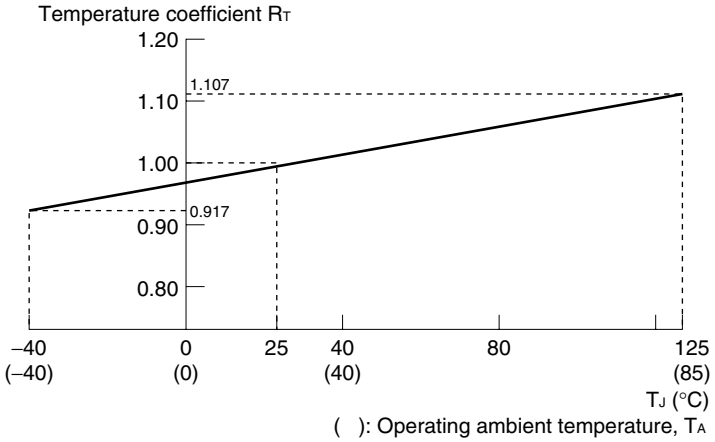
(a) V_{DD} dependency (MAX.)



(b) V_{DD} dependency (MIN.)



(c) T_J dependency



$-40 \leq T_J \leq 25°C$	$R_{T\,(MIN.)} = 0.968 + 0.00128T_J$
$25 \leq T_J \leq 125°C$	$R_{T\,(MAX.)} = 0.974 + 0.00106T_J$

The coefficient of the absolute distribution can be recalculated by limiting the operating ambient temperature and power consumption (for example, by limiting the temperature rise due to power consumption to about 10°C). The operating junction temperature when the operating ambient temperature or power consumption is limited can be calculated by the formula below. The lower the operating junction temperature, the closer to 1 the coefficient of the absolute distribution (if the operating junction temperature is limited to 100°C, the delay time is 5% shorter than when the operating junction temperature is limited to 125°C).

$T_J = T_{A\,(MAX.)} + P_D \times \theta_{ja}$ (°C)

where:

T_J: Operating junction temperature

$T_{A\,(MAX.)}$: Maximum value of operating ambient temperature

P_D: Power consumption estimated by the calculation formula in **4.3.2 Estimating power consumption**

θ_{ja}: Thermal resistance (See the tables concerning thermal resistance in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**)

Please note that since Figure 4-10 (a) through (c) shows the average values of the delay distribution (variations in the process are already included in the value of the power supply voltage), the guaranteed values are the result of simulation.

Reference data

$R_{MAX.} = R_{V\,(MAX.)} \times R_{T\,(MAX.)}$

$R_{MIN.} = R_{V\,(MIN.)} \times R_{T\,(MIN.)}$

$t_{PD\,(MAX.)} = t_{PD\,(TYP.)} \times R_{MAX.}$

$t_{PD\,(MIN.)} = t_{PD\,(TYP.)} \times R_{MIN.}$

Standard specification: 3.3 V condition (V_{DD} = 3.3 ±0.3 V; T_A = –40 to +85°C; T_J = –40 to +125°C)

$R_{MAX.} = 1.48$

$R_{MIN.} = 0.67$

Calculation example

Derive $R_{MAX.}/R_{MIN.}$ for V_{DD} = 3.3 ±0.3 V and T_J = –40 to +120°C.

(1) Derive R_V from Figure 4-10 (a) and (b):

$R_{V\,(MAX.)} = 1.34$

$R_{V\,(MIN.)} = 0.73$

(2) Next, derive R_T from Figure 4-10 (c):

$R_{T\,(MAX.)} = 1.10$

$R_{T\,(MIN.)} = 0.92$

(3) Accordingly, it follows that,

$R_{MAX.} = R_{V\,(MAX.)} \times R_{T\,(MAX.)} = 1.34 \times 1.10$

$R_{MIN.} = R_{V\,(MIN.)} \times R_{T\,(MIN.)} = 0.73 \times 0.92$

$R_{MAX.} = 1.474$

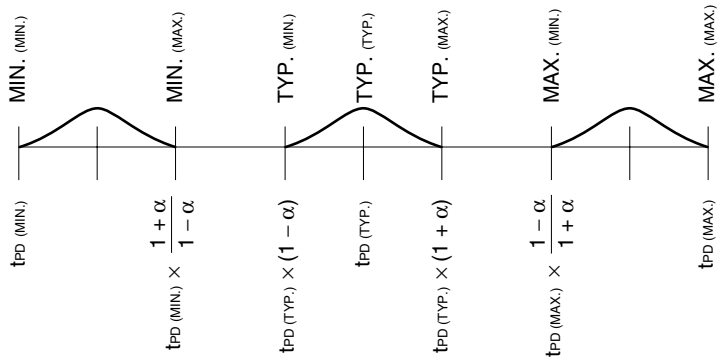
$R_{MIN.} = 0.672$

In addition to the absolute distribution applicable from the device specification, there is also the relative distribution generated by the chip's internal paths and by the manufacture of the P-ch and N-ch transistors. This relative distribution is an important factor in verifying the timing of the circuit. The relative distribution of CMOS-9HD Series is as follows.

Relative distribution α = 10%

Figure 4-11 shows the distribution with $t_{PD\ (TYP.)}$ as the median.

Figure 4-11. t_{PD} Distribution



4.5 Output Buffer Characteristics

4.5.1 Rise/fall times

The rise and fall times of the output buffer vary greatly by differences in the drive capability due to the output level and by the connected load capacitance. The output buffer rise/fall times, t_r and t_f, can be calculated as follows:

$$t_r = t_{r0} + F_{tr} \times C_L \quad \text{(ns)}$$
$$t_f = t_{f0} + F_{tf} \times C_L \quad \text{(ns)}$$

where:

- t_{r0}: Reference rise time (load capacitance, C_L = 0 pF)
- t_{f0}: Reference fall time (load capacitance, C_L = 0 pF)
- F_{tr}, F_{tf}: Load capacitance coefficient
- C_L: Load capacitance ($0 < C_L \leq 300$ pF)

See **Tables 4-10** through **4-12** for output buffer coefficients.

Table 4-10. t_r and t_f Calculation Coefficients of LVTTL Output Buffer

(a) Output level = $V_{DD} \times 10\%$ to $V_{DD} \times 90\%$

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FO09	I_{OL} = 3.0 mA	2.68	0.312	2.26	0.261
	FO04	I_{OL} = 6.0 mA	1.43	0.170	1.08	0.138
	FO01	I_{OL} = 9.0 mA	1.02	0.117	0.77	0.098
	FO02	I_{OL} = 12.0 mA	0.73	0.092	0.66	0.074
	FO03	I_{OL} = 18.0 mA	0.53	0.060	0.45	0.051
	FO06	I_{OL} = 24.0 mA	0.48	0.046	0.38	0.036
Low-noise type	FE04	I_{OL} = 6.0 mA	2.93	0.181	3.71	0.140
	FE01	I_{OL} = 9.0 mA	2.58	0.125	3.30	0.100
	FE02	I_{OL} = 12.0 mA	2.45	0.093	3.12	0.077
	FE03	I_{OL} = 18.0 mA	2.40	0.065	2.97	0.053
	FE06	I_{OL} = 24.0 mA	2.37	0.033	2.93	0.040

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

(b) Output level = 0.8 to 2.0 V

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FO09	I_{OL} = 3.0 mA	0.85	0.105	0.87	0.101
	FO04	I_{OL} = 6.0 mA	0.42	0.056	0.41	0.055
	FO01	I_{OL} = 9.0 mA	0.30	0.039	0.29	0.038
	FO02	I_{OL} = 12.0 mA	0.23	0.029	0.23	0.028
	FO03	I_{OL} = 18.0 mA	0.18	0.019	0.16	0.019
	FO06	I_{OL} = 24.0 mA	0.14	0.014	0.13	0.015
Low-noise type	FE04	I_{OL} = 6.0 mA	2.13	0.087	3.18	0.101
	FE01	I_{OL} = 9.0 mA	1.99	0.061	2.96	0.069
	FE02	I_{OL} = 12.0 mA	1.92	0.046	2.82	0.053
	FE03	I_{OL} = 18.0 mA	1.96	0.031	2.74	0.037
	FE06	I_{OL} = 24.0 mA	1.96	0.024	2.69	0.030

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Table 4-11. t_r and t_f Calculation Coefficients of TTL 5 V Tolerant Output Buffer

(a) Output level = $V_{DD} \times 10\%$ to $V_{DD} \times 90\%$

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FV0A	I_{OL} = 1.0 mA	9.65	0.482	9.90	0.473
	FV0B	I_{OL} = 2.0 mA	7.18	0.371	7.05	0.349
	FV09	I_{OL} = 3.0 mA	7.15	0.319	5.45	0.275
	FV04	I_{OL} = 6.0 mA	2.75	0.124	1.95	0.100
	FV01	I_{OL} = 9.0 mA	2.17	0.095	1.55	0.075
	FV02	I_{OL} = 12.0 mA	1.34	0.064	0.87	0.042
	FV03	I_{OL} = 18.0 mA	1.35	0.064	0.70	0.035
	FV06	I_{OL} = 24.0 mA	1.40	0.065	0.60	0.028
Low-noise type	FW02	I_{OL} = 12.0 mA	1.83	0.074	1.95	0.042
	FW03	I_{OL} = 18.0 mA	2.10	0.074	1.85	0.035
	FW06	I_{OL} = 24.0 mA	1.93	0.074	1.85	0.028

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

(b) Output level = 0.8 to 2.0 V

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FV0A	I_{OL} = 1.0 mA	2.90	0.130	3.85	0.181
	FV0B	I_{OL} = 2.0 mA	2.41	0.116	2.87	0.143
	FV09	I_{OL} = 3.0 mA	2.49	0.111	2.48	0.111
	FV04	I_{OL} = 6.0 mA	0.88	0.041	0.79	0.042
	FV01	I_{OL} = 9.0 mA	0.66	0.030	0.59	0.031
	FV02	I_{OL} = 12.0 mA	0.37	0.018	0.34	0.018
	FV03	I_{OL} = 18.0 mA	0.37	0.017	0.27	0.014
	FV06	I_{OL} = 24.0 mA	0.38	0.017	0.22	0.011
Low-noise type	FW02	I_{OL} = 12.0 mA	0.61	0.015	0.70	0.016
	FW03	I_{OL} = 18.0 mA	0.67	0.016	0.64	0.013
	FW06	I_{OL} = 24.0 mA	0.63	0.016	0.58	0.011

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

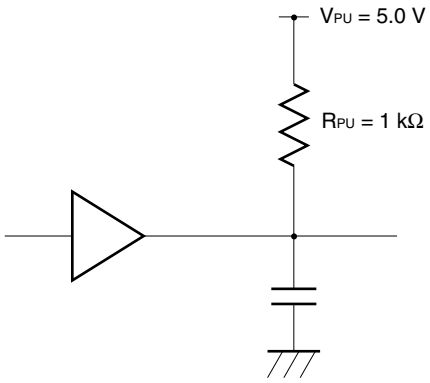
Table 4-12. t_r and t_f Calculation Coefficients of CMOS 5 V Tolerant Output Buffer

Output level = 0.8 to 2.0 V

Buffer Type	Example	Drive Capability	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FY09	I_{OL} = 3.0 mA	1.52	0.085	3.45	0.140
	FY04	I_{OL} = 6.0 mA	0.70	0.035	0.65	0.048
	FY01	I_{OL} = 9.0 mA	0.55	0.027	0.45	0.035
	FY02	I_{OL} = 12.0 mA	0.35	0.021	0.30	0.018
	FY03	I_{OL} = 18.0 mA	0.35	0.015	0.25	0.016
	FY06	I_{OL} = 24.0 mA	0.34	0.015	0.23	0.012
Low-noise type	FZ02	I_{OL} = 12.0 mA	2.55	0.026	3.40	0.026
	FZ03	I_{OL} = 18.0 mA	2.56	0.026	3.51	0.024
	FZ06	I_{OL} = 24.0 mA	2.58	0.018	3.61	0.016

Remark The rise and fall time of the output buffer is specified by the following conditions:
V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Evaluation circuit



4.5.2 Load capacitance range

The maximum allowable load capacitance $C_{L\ (MAX.)}$ of the output buffer should be $C_{L\ (MAX.)} \leq 300$ pF. In addition, Table 4-13 shows the recommended load capacitance range for each drive capability of the output buffer. The optimal output buffer based on Table 4-13 should be selected.

The recommended load capacitance range of the 5 V tolerant buffer for CMOS depends on the pull-up resistance value.

In particular, if a load capacitance outside the recommended range is used, it must be noted that the overshoot and undershoot generated in the output signal increases if a lower load capacitance is used.

Table 4-13. Recommended Load Capacitance Ranges for Output Buffers

Buffer Type	Example	Drive Capability	Recommended Load Capacitance Range (pF)
LVTTL Normal type	FO09	I_{OL} = 3.0 mA	0 to 40
	FO04	I_{OL} = 6.0 mA	0 to 80
	FO01	I_{OL} = 9.0 mA	10 to 110
	FO02	I_{OL} = 12.0 mA	20 to 155
	FO03	I_{OL} = 18.0 mA	100 to 230
	FO06	I_{OL} = 24.0 mA	120 to 300
LVTTL Low-noise type	FE04	I_{OL} = 6.0 mA	0 to 90
	FE01	I_{OL} = 9.0 mA	0 to 135
	FE02	I_{OL} = 12.0 mA	20 to 180
	FE03	I_{OL} = 18.0 mA	25 to 200
	FE06	I_{OL} = 24.0 mA	35 to 250
TTL 5 V tolerant Normal type	FV0A	I_{OL} = 1.0 mA	0 to 20
	FV0B	I_{OL} = 2.0 mA	0 to 35
	FV09	I_{OL} = 3.0 mA	0 to 40
	FV04	I_{OL} = 6.0 mA	0 to 75
	FV01	I_{OL} = 9.0 mA	15 to 110
	FV02	I_{OL} = 12.0 mA	20 to 155
	FV03	I_{OL} = 18.0 mA	100 to 230
	FV06	I_{OL} = 24.0 mA	120 to 300
TTL 5 V tolerant Low-noise type	FW02	I_{OL} = 12.0 mA	20 to 170
	FW03	I_{OL} = 18.0 mA	20 to 170
	FW06	I_{OL} = 24.0 mA	20 to 170

4.5.3 Maximum operating frequency

The maximum operating frequency of the output buffer is determined by the drive capability and the load capacitance. As explained in **4.5.2 Load capacitance range**, there are recommended ranges for load capacitance.

The diagonally shaded parts of the graphs in Figures 4-12 through 4-15 correspond to these ranges.

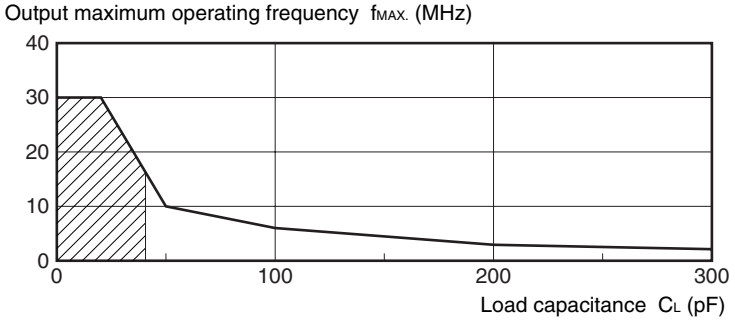
The right sides of the diagonally shaded parts can be used if there are no problems with the propagation delay time, rise time, and fall time. On the other hand, there is large overshoot and undershoot in the left sides.

Moreover, the output maximum operating frequencies shown in Figures 4-12 through 4-15 are specified assuming that only capacitances are connected to the output pins. Consequently, there is a slight fluctuation if inductance is taken into consideration. In addition, because the waveform of the CMOS 5 V tolerant interface changes greatly according to the pull-up resistance value, the output waveform is shown for stated conditions.

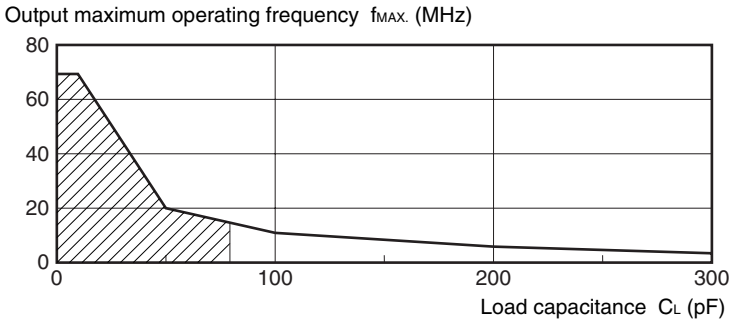
Caution Calculate t_r and t_f of the output signal to confirm that the output pulse width satisfies the input specifications of the other device.

Figure 4-12. Restrictions for $f_{MAX.}$ vs. C_L (LVTTL Output, Normal Type) (1/2)

(a) I_{OL} = 3.0 mA



(b) I_{OL} = 6.0 mA



(c) I_{OL} = 9.0 mA

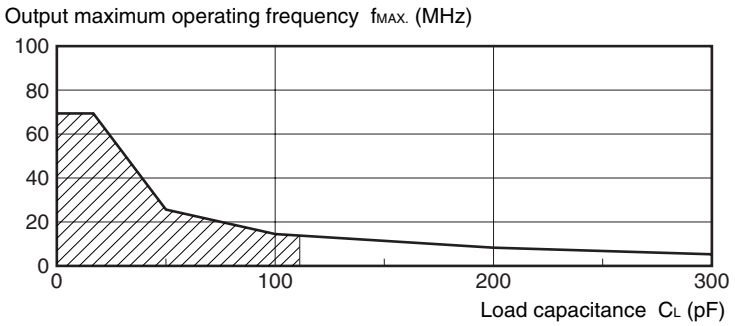
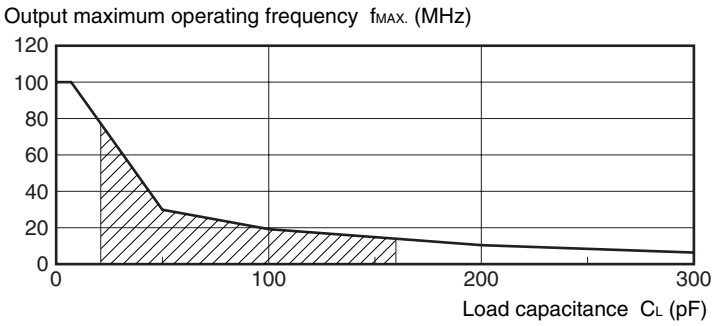
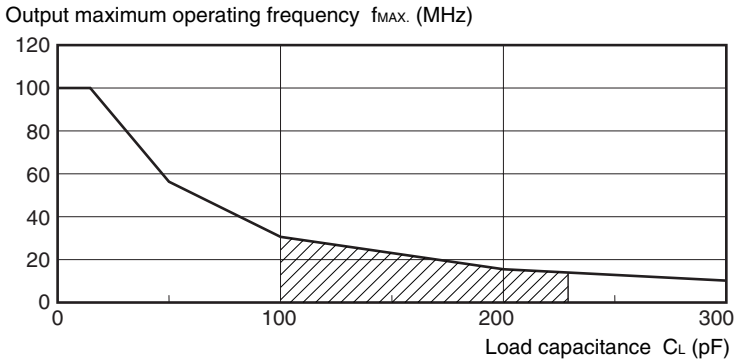


Figure 4-12. Restrictions for $f_{MAX.}$ vs. C_L (LVTTL Output, Normal Type) (2/2)

(d) I_{OL} = 12.0 mA



(e) I_{OL} = 18.0 mA



(f) I_{OL} = 24.0 mA

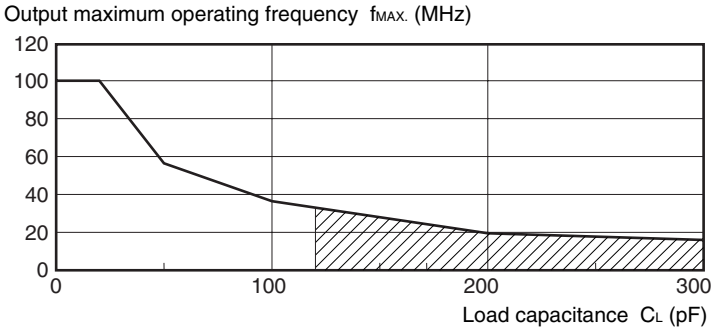
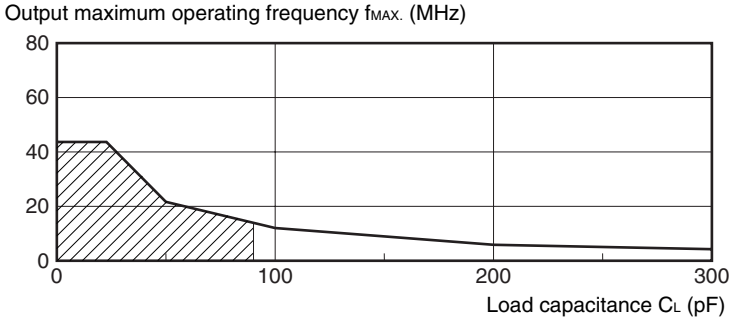
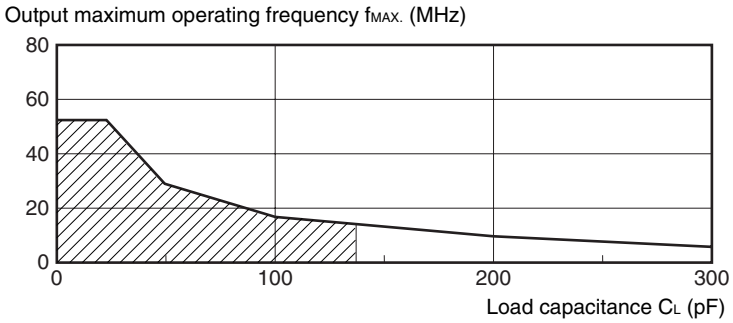


Figure 4-13. Restrictions for $f_{MAX.}$ vs. C_L (LVTTL Output, Low-Noise Type) (1/2)

(a) I_{OL} = 6.0 mA (FE04)



(b) I_{OL} = 9.0 mA (FE01)



(c) I_{OL} = 12.0 mA (FE02)

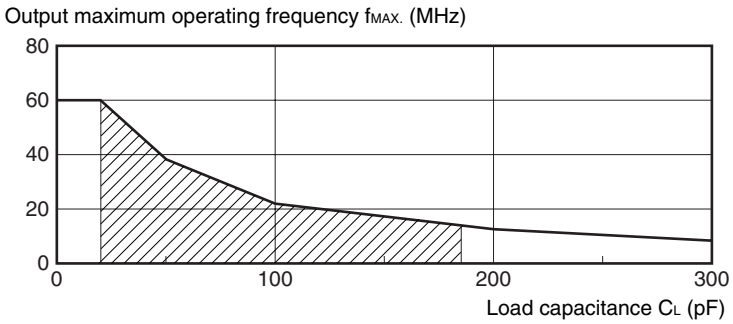
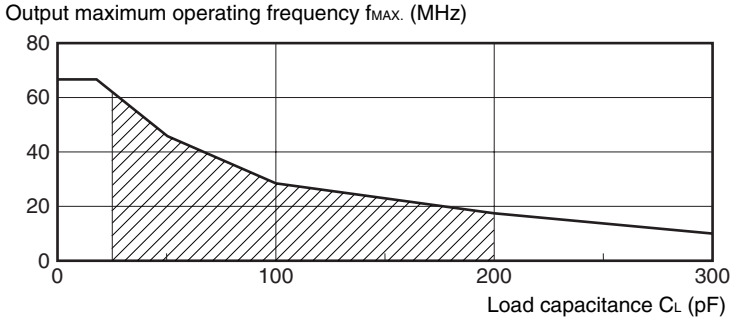


Figure 4-13. Restrictions for $f_{MAX.}$ vs. C_L (LVTTL Output, Low-Noise Type) (2/2)

(d) I_{OL} = 18.0 mA (FE03)



(e) I_{OL} = 24.0 mA (FE06)

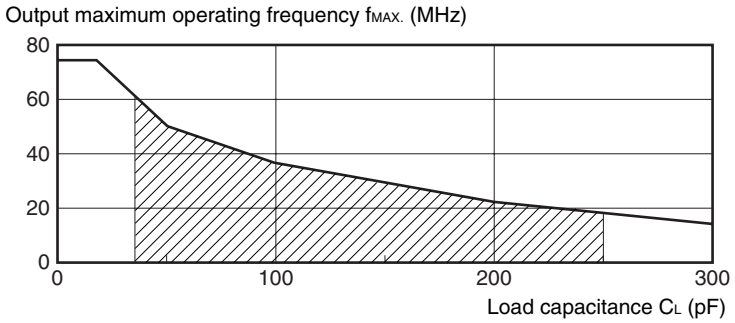
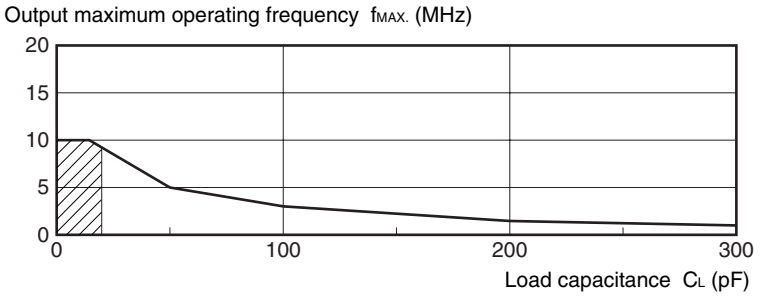
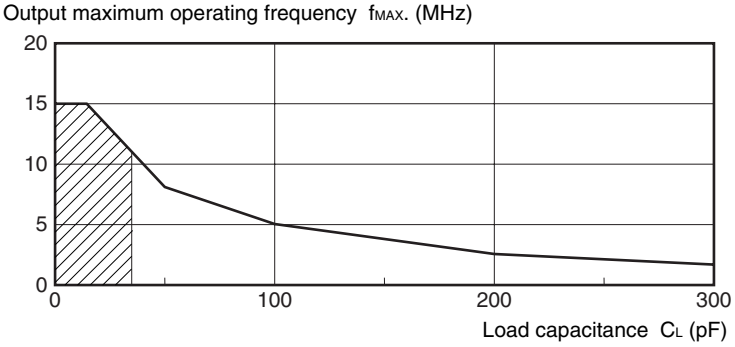


Figure 4-14. Restrictions for $f_{MAX.}$ vs. C_L (TTL 5 V Tolerant Output, Normal Type) (1/3)

(a) I_{OL} = 1.0 mA



(b) I_{OL} = 2.0 mA



(c) I_{OL} = 3.0 mA

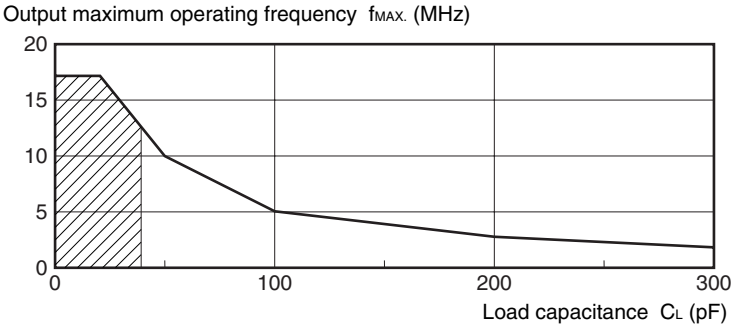
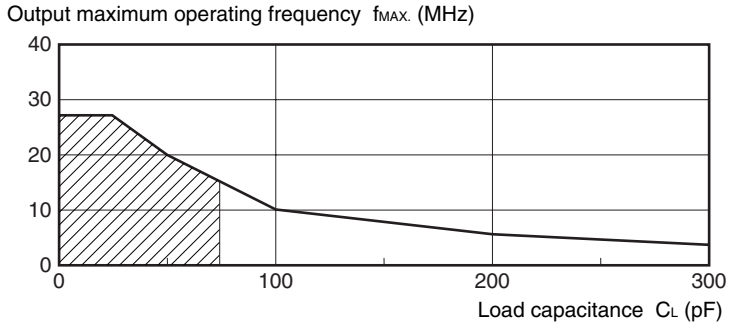
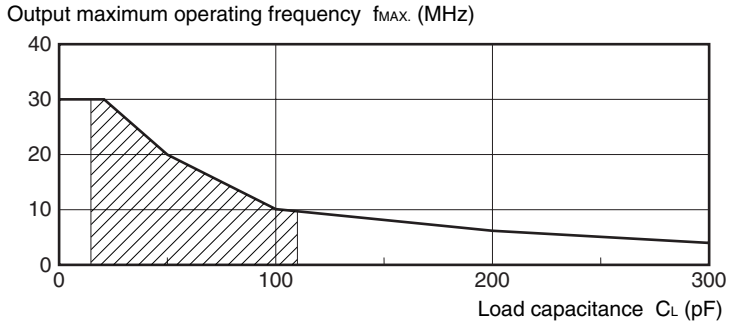


Figure 4-14. Restrictions for $f_{MAX.}$ vs. C_L (TTL 5 V Tolerant Output, Normal Type) (2/3)

(d) I_{OL} = 6.0 mA



(e) I_{OL} = 9.0 mA



(f) I_{OL} = 12.0 mA

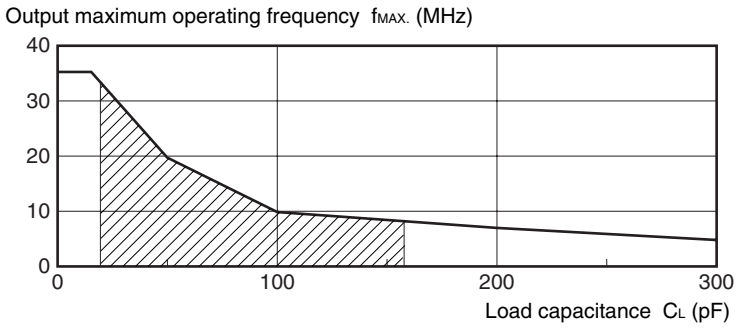
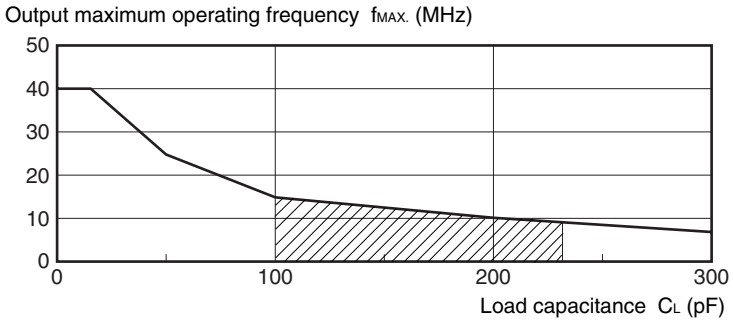


Figure 4-14. Restrictions for $f_{MAX.}$ vs. C_L (TTL 5 V Tolerant Output, Normal Type) (3/3)

(g) I_{OL} = 18.0 mA



(h) I_{OL} = 24.0 mA

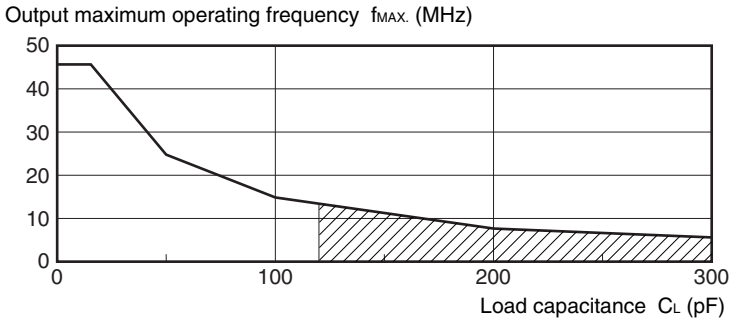
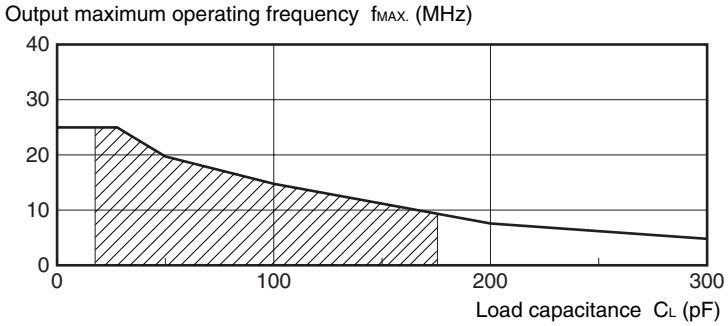
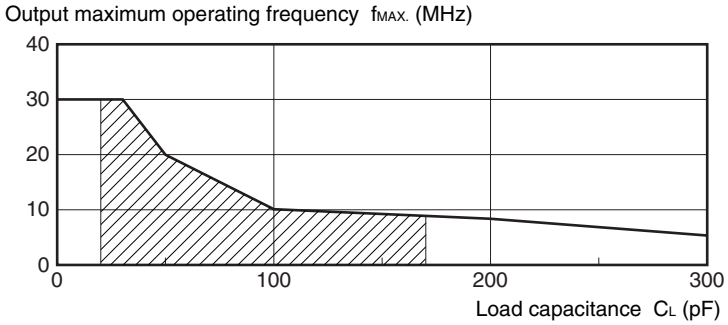


Figure 4-15. Restrictions for $f_{MAX.}$ vs. C_L (TTL 5 V Tolerant Output, Low-Noise Type)

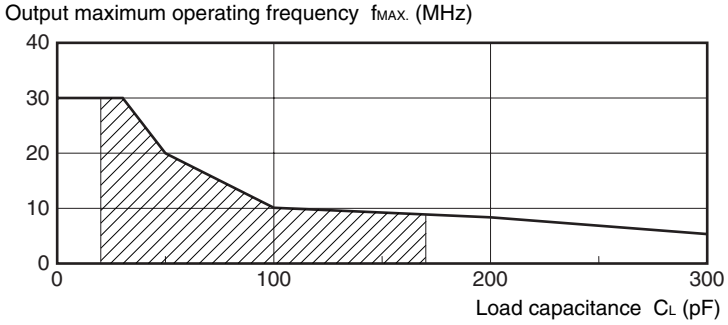
(a) I_{OL} = 12.0 mA



(b) I_{OL} = 18.0 mA



(c) I_{OL} = 24.0 mA



The CMOS 5 V tolerant output waveforms shown in Figures 4-16 and 4-17 show the output waveform for the following conditions:

V_{DD} = 3.3 V, T_J = 25°C, input signal t_r, t_f = 0.4 ns (V_{DD} = 3.3 V)

Evaluation circuit

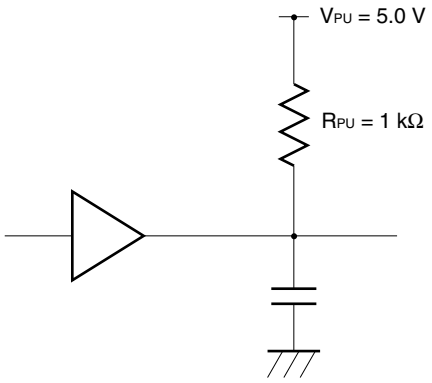
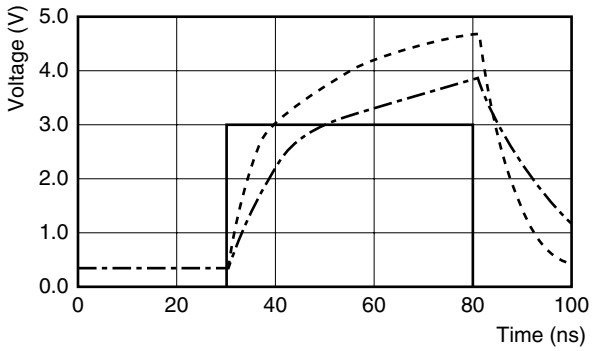
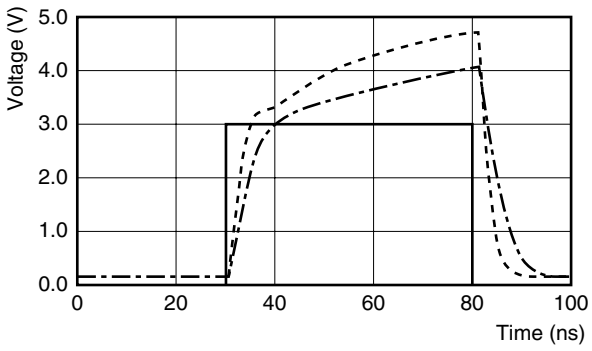


Figure 4-16. Output Waveforms (CMOS 5 V Tolerant Output, Normal Type)

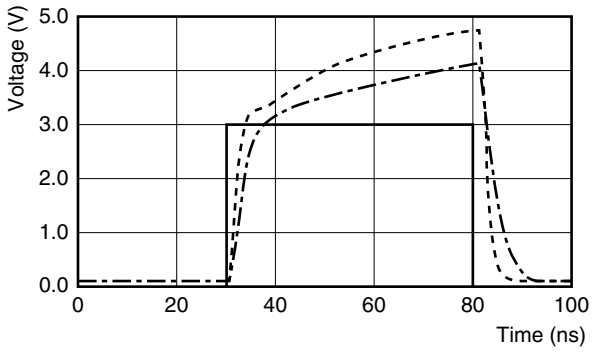
(a) I_{OL} = 3.0 mA (FY09)



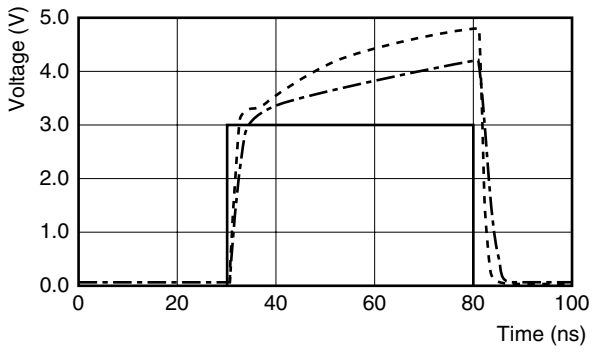
(b) I_{OL} = 6.0 mA (FY04)



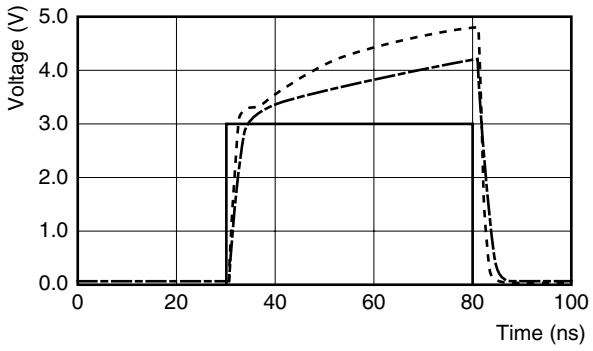
(c) I_{OL} = 9.0 mA (FY01)



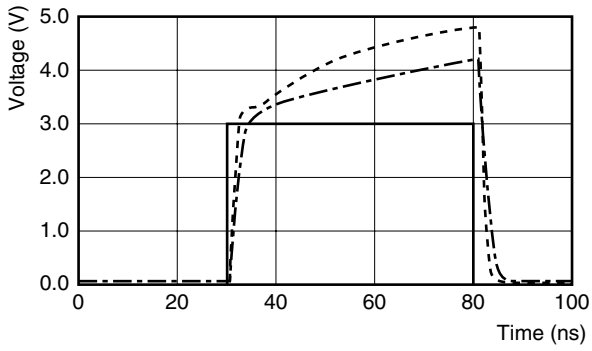
(d) I_{OL} = 12.0 mA (FY02)



(e) I_{OL} = 18.0 mA (FY03)



(f) I_{OL} = 24.0 mA (FY06)



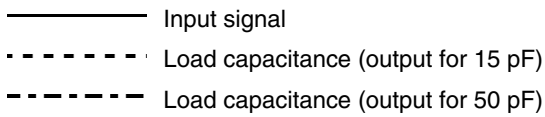
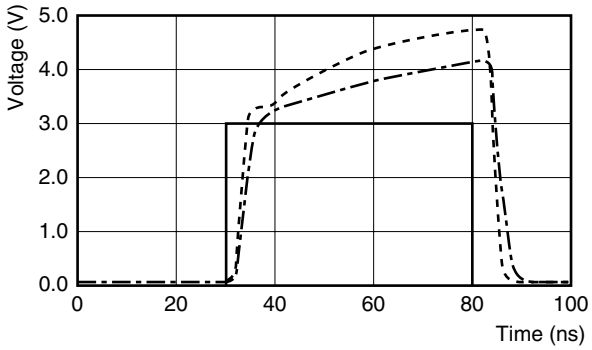
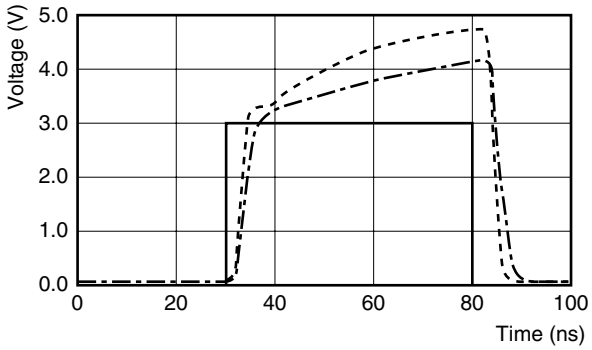


Figure 4-17. Output Waveforms (CMOS 5 V Tolerant Output, Low-Noise Type)

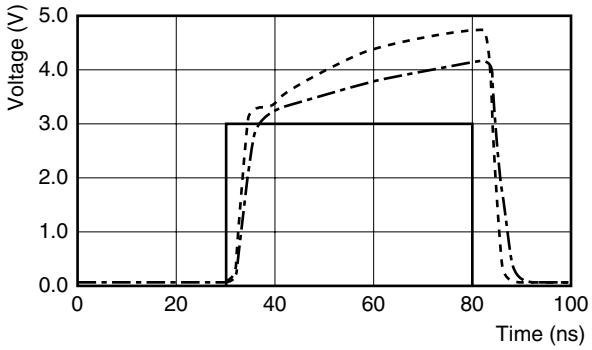
(a) I_{OL} = 12.0 mA (FZ02)

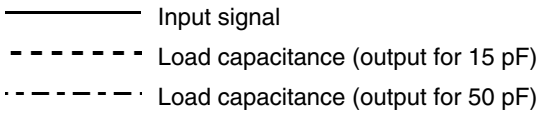


(b) I_{OL} = 18.0 mA (FZ03)



(c) I_{OL} = 24.0 mA (FZ06)





4.5.4 Output buffer output current (I_{OL}, I_{OH})

NEC Electronics defines the output current of a CMOS gate array at V_{OL} = 0.4 V and V_{OH} = 2.4 V. However, there are cases in which the V_{OL} and V_{OH} used differ for actual applications. In such cases, the coefficients shown below should be used in estimating the I_{OL} and I_{OH} characteristics in accordance with the actual conditions.

- **Dependency on output voltage**

  V_{OL} = 0.4 to 0.6 V, V_{OH} = (V_{DD} – 0.4 V) to (V_{DD} – 0.6 V)

  Because I_{OL} and I_{OH} vary almost proportionately to the output voltage, a direct approximation is possible. However, this excludes the I_{OH} of the TTL level output buffer.

  Equations for estimating the output buffer current

  $$I_{OL}' = I_{OL} \times V_{OL}/0.4 \quad (mA)$$
  $$I_{OH}' = I_{OH} \times (V_{DD} - V_{OH})/0.6 \quad (mA)$$

  where:

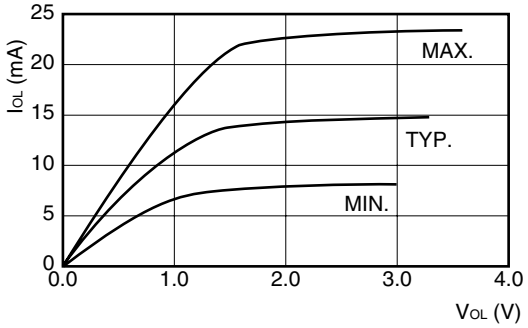
  - I_{OL}: I_{OL} specification when V_{OL} = 0.4 V
  - V_{OL}: V_{OL} value used
  - I_{OH}: I_{OH} specification when V_{OH} = 2.4 V
  - V_{OH}: V_{OH} value used

The I_O vs. V_O curves are shown in Figure 4-18. The MIN. curve is shown for the conditions V_{DD} = 3.0 V and T_J = 125°C. The TYP. curve is shown for the conditions V_{DD} = 3.3 V and T_J = 25°C. The MAX. curve is shown for the conditions V_{DD} = 3.6 V and T_J = –40°C. The direct currents I_{OH} and I_{OL} that can actually be used should be within the absolute maximum ratings. Furthermore, the CMOS 5 V output buffer is configured to cut off the direct current I_{OH}, and the V_O vs. I_O curve cannot be shown for the MIN. and MAX. conditions.

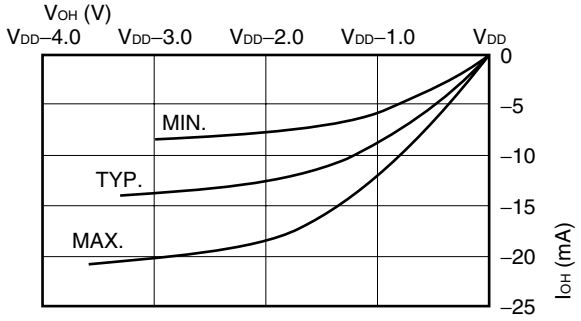
Figure 4-18. I_O vs. V_O (1/9)

(1) LVTTL output type; I_{OL} = 3 mA (Representative block type: FO09)

(a) I_{OL} vs. V_{OL}

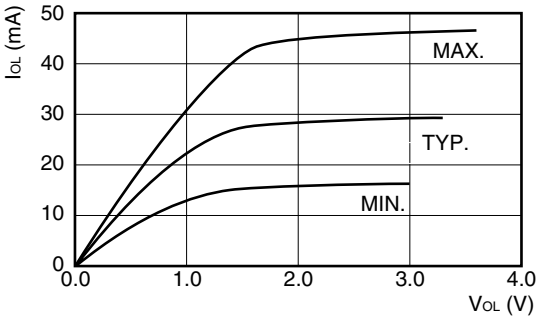


(b) I_{OH} vs. V_{OH}

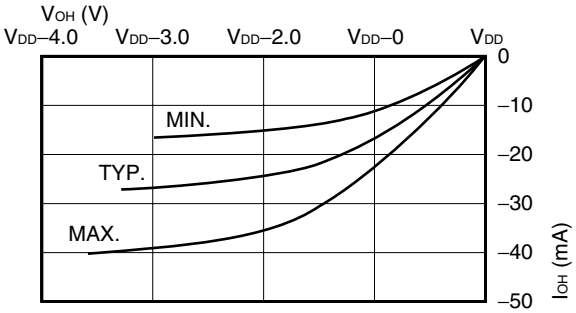


(2) LVTTL output type; I_{OL} = 6 mA (Representative block type: FO04, FE04)

(a) I_{OL} vs. V_{OL}

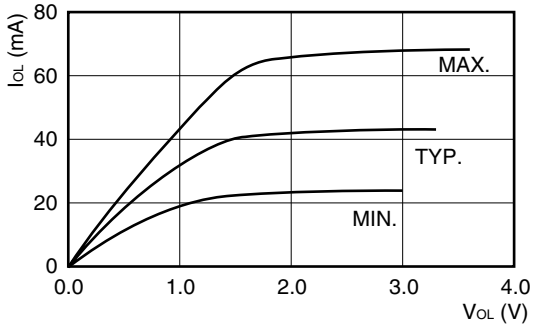


(b) I_{OH} vs. V_{OH}



(3) LVTTL output type; I_{OL} = 9 mA (Representative block type: FO01, FE01)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

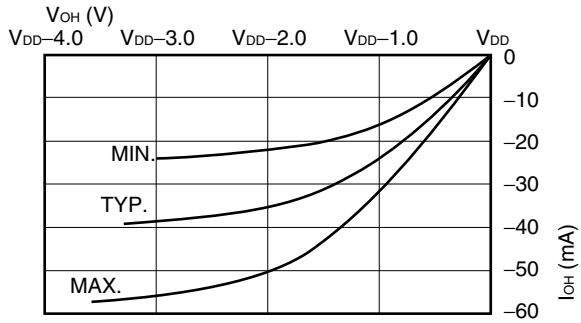
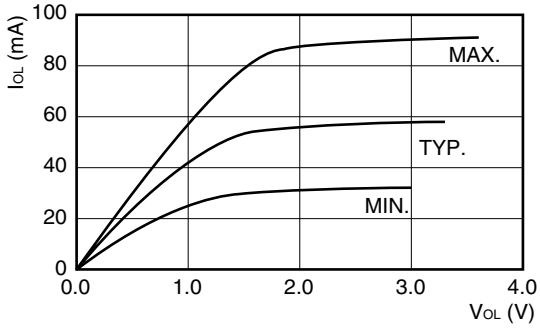


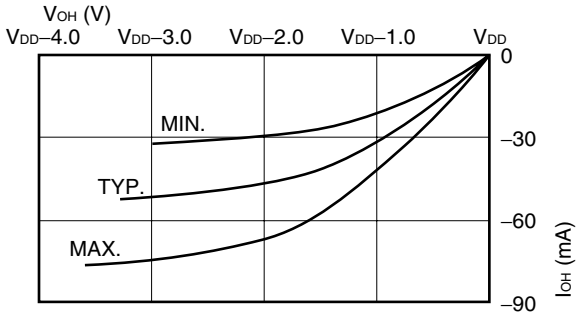
Figure 4-18. I_O vs. V_O (2/9)

(4) LVTTL output type; I_{OL} = 12 mA (Representative block type: FO02, FE02)

(a) I_{OL} vs. V_{OL}

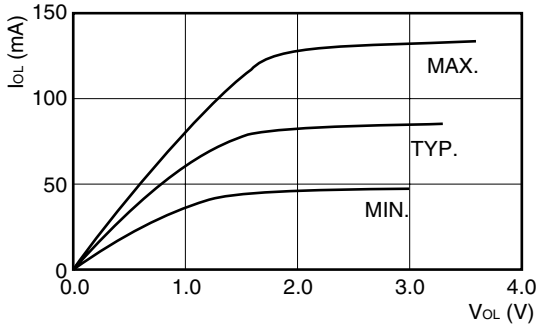


(b) I_{OH} vs. V_{OH}

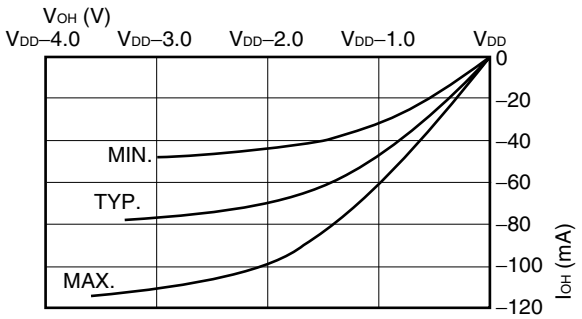


(5) LVTTL output type; I_{OL} = 18 mA (Representative block type: FO03, FE03)

(a) I_{OL} vs. V_{OL}

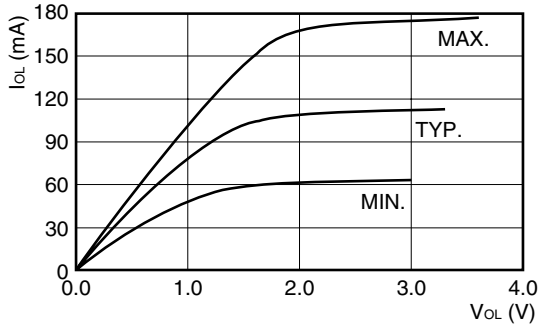


(b) I_{OH} vs. V_{OH}



(6) LVTTL output type; I_{OL} = 24 mA (Representative block type: FO06, FE06)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

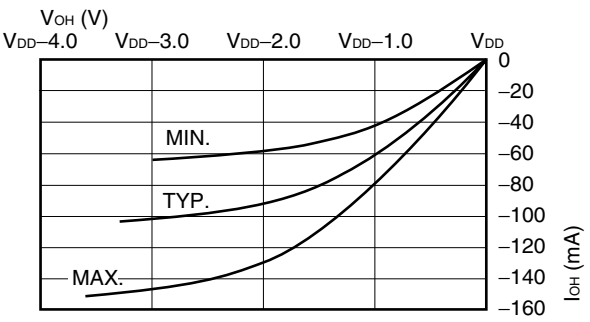
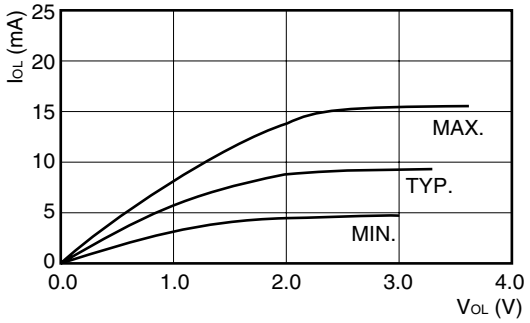


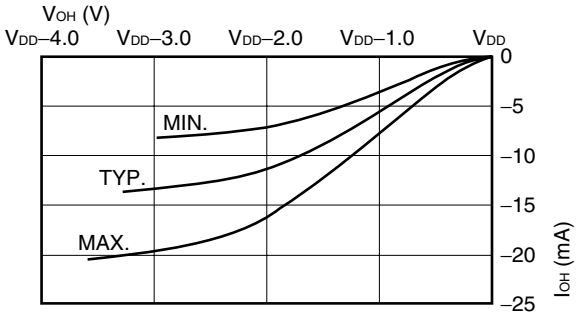
Figure 4-18. I_O vs. V_O (3/9)

(7) TTL 5 V tolerant output, normal type; I_{OL} = 1 mA (Representative block type: FV0A)

(a) I_{OL} vs. V_{OL}

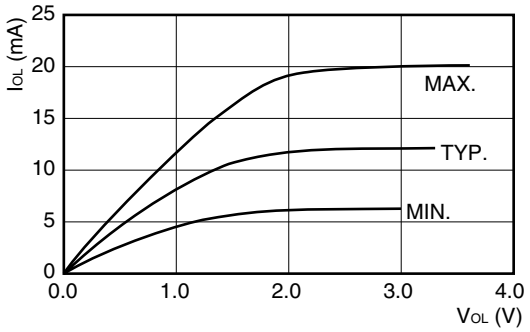


(b) I_{OH} vs. V_{OH}

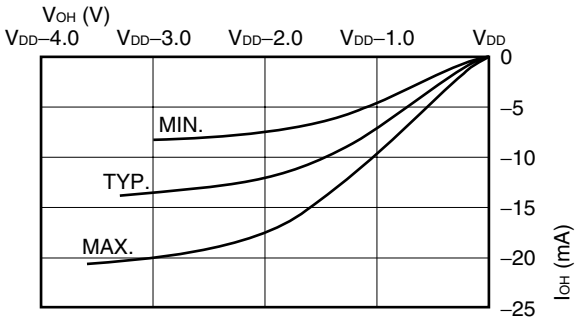


(8) TTL 5 V tolerant output, normal type; I_{OL} = 2 mA (Representative block type: FV0B)

(a) I_{OL} vs. V_{OL}

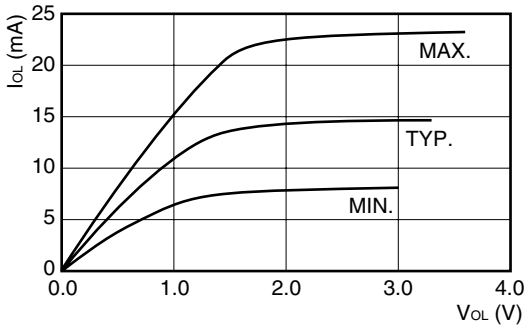


(b) I_{OH} vs. V_{OH}



(9) TTL 5 V tolerant output, normal type; I_{OL} = 3 mA (Representative block type: FV09)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

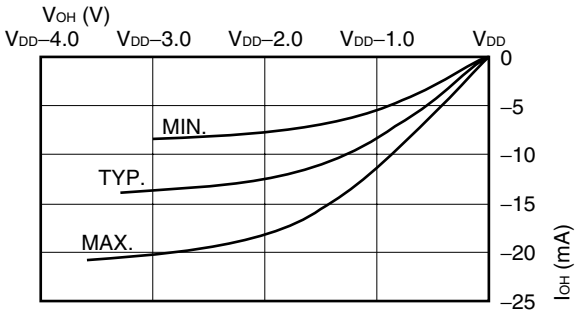
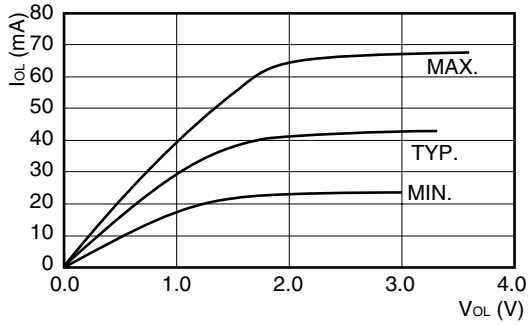


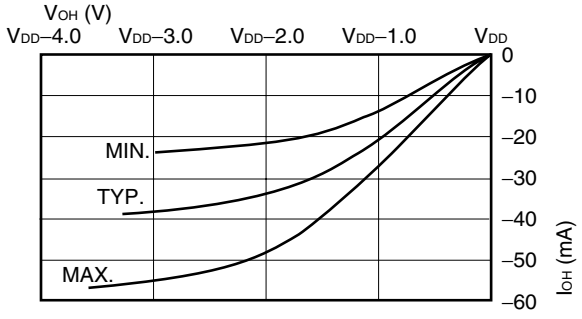
Figure 4-18. I_O vs. V_O (4/9)

(10) TTL 5 V tolerant output, normal type; I_{OL} = 6 mA (Representative block type: FV04)

(a) I_{OL} vs. V_{OL}

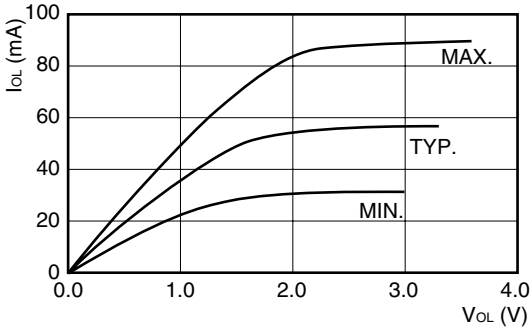


(b) I_{OH} vs. V_{OH}

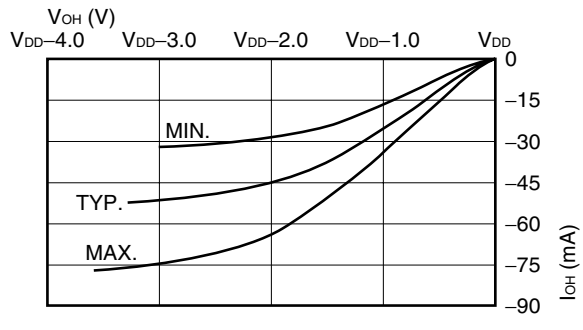


(11) TTL 5 V tolerant output, normal type; I_{OL} = 9 mA (Representative block type: FV01)

(a) I_{OL} vs. V_{OL}

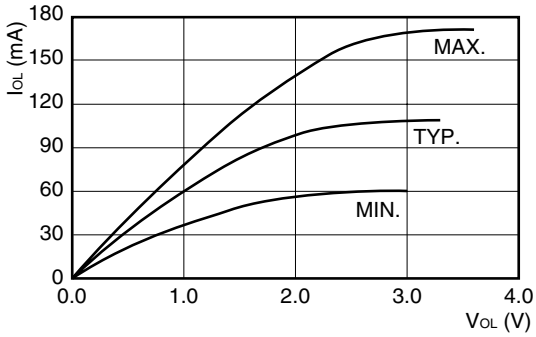


(b) I_{OH} vs. V_{OH}



(12) TTL 5 V tolerant output, normal type; I_{OL} = 12 mA (Representative block type: FV02)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

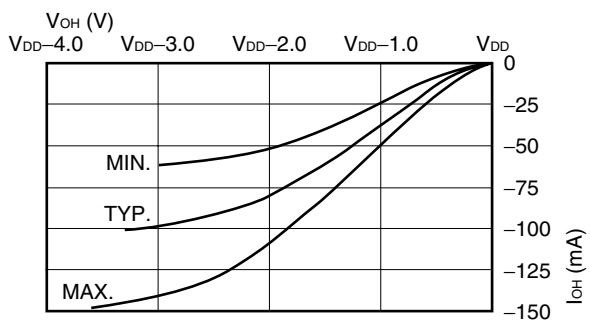
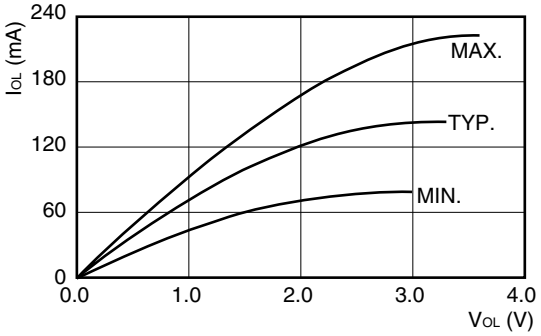


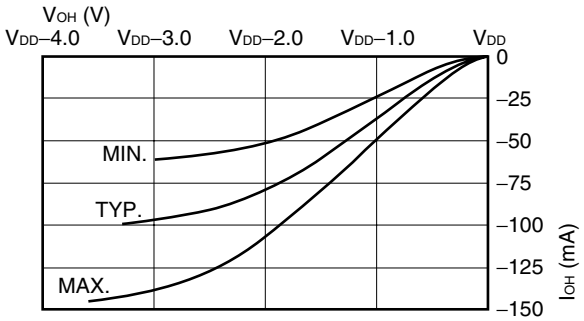
Figure 4-18. I_O vs. V_O (5/9)

(13) TTL 5 V tolerant output, normal type; I_{OL} = 18 mA (Representative block type: FV03)

(a) I_{OL} vs. V_{OL}

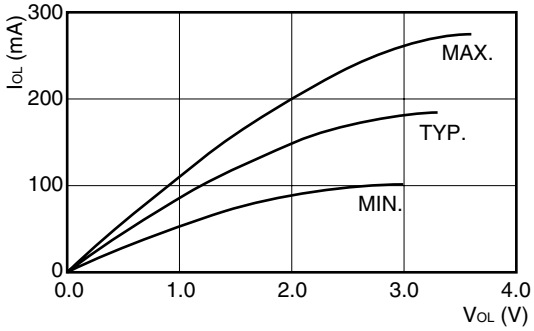


(b) I_{OH} vs. V_{OH}

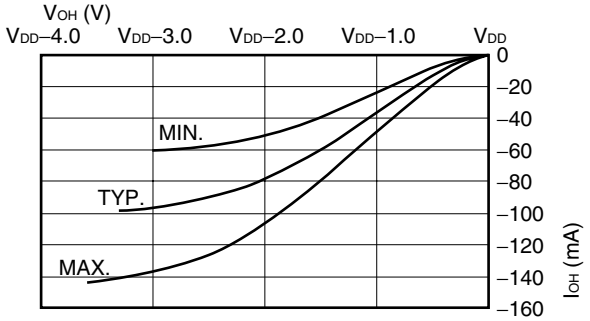


(14) TTL 5 V tolerant output, normal type; I_{OL} = 24 mA (Representative block type: FV06)

(a) I_{OL} vs. V_{OL}

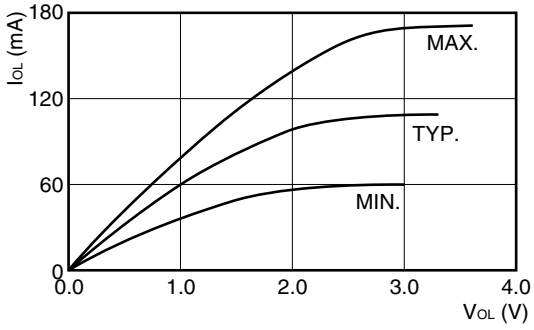


(b) I_{OH} vs. V_{OH}



(15) TTL 5 V tolerant output, low-noise type; I_{OL} = 12 mA (Representative block type: FW02)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

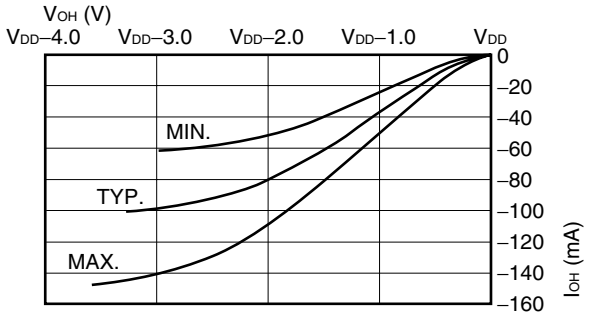
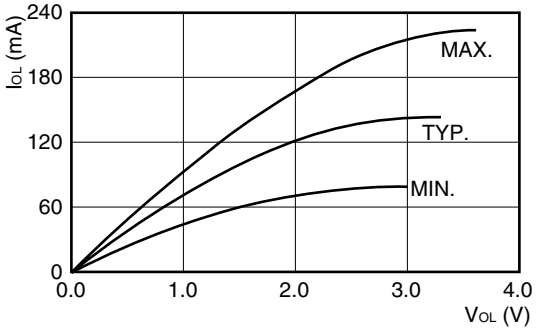


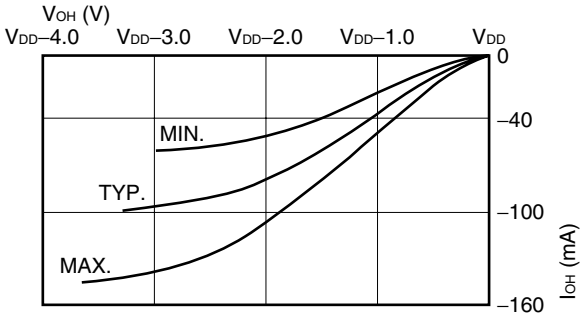
Figure 4-18. I_O vs. V_O (6/9)

(16) TTL 5 V tolerant output, low-noise type; I_{OL} = 18 mA (Representative block type: FW03)

(a) I_{OL} vs. V_{OL}

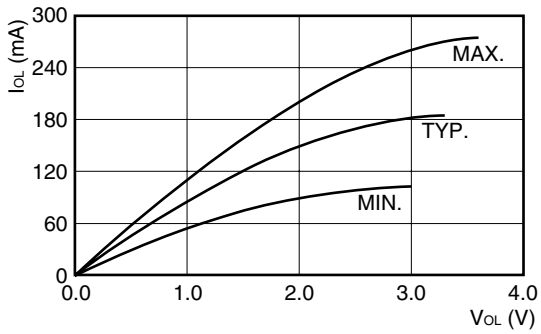


(b) I_{OH} vs. V_{OH}

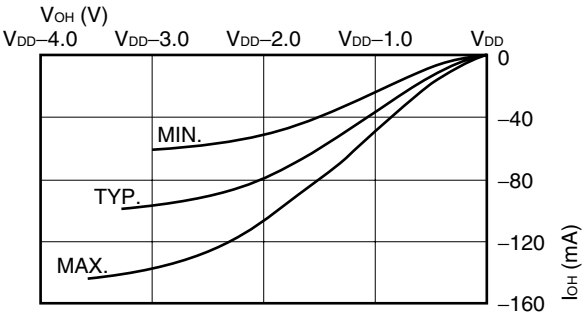


(17) TTL 5 V tolerant output, low-noise type; I_{OL} = 24 mA (Representative block type: FW06)

(a) I_{OL} vs. V_{OL}

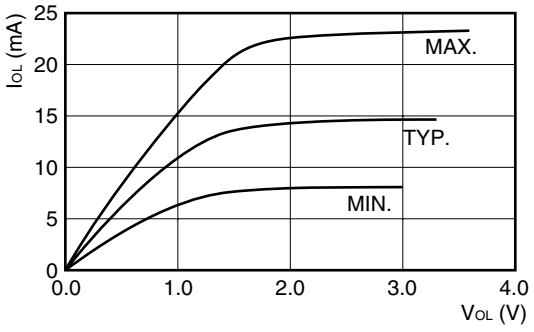


(b) I_{OH} vs. V_{OH}



(18) CMOS 5 V tolerant output, normal type; I_{OL} = 3 mA (Representative block type: FY09)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

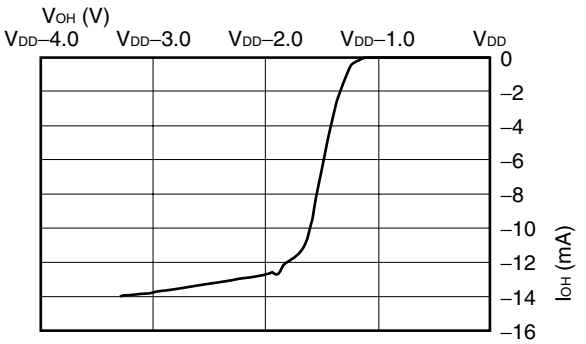
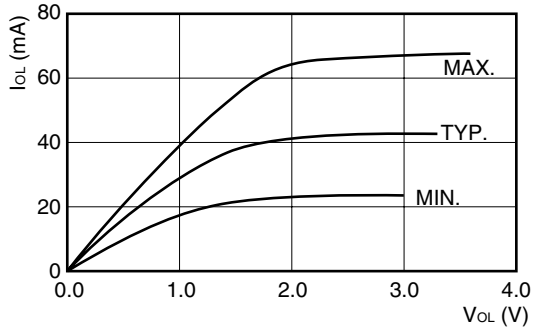


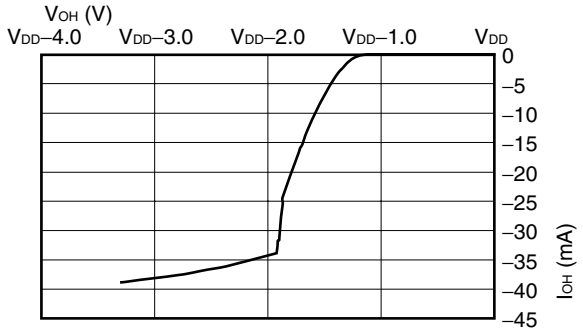
Figure 4-18. I_O vs. V_O (7/9)

(19) CMOS 5 V tolerant output, normal type; I_{OL} = 6 mA (Representative block type: FY04)

(a) I_{OL} vs. V_{OL}

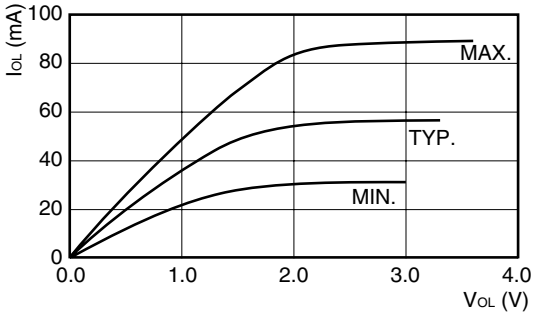


(b) I_{OH} vs. V_{OH}

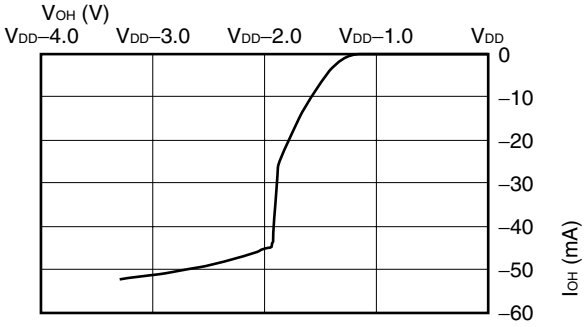


(20) CMOS 5 V tolerant output, normal type; I_{OL} = 9 mA (Representative block type: FY01)

(a) I_{OL} vs. V_{OL}

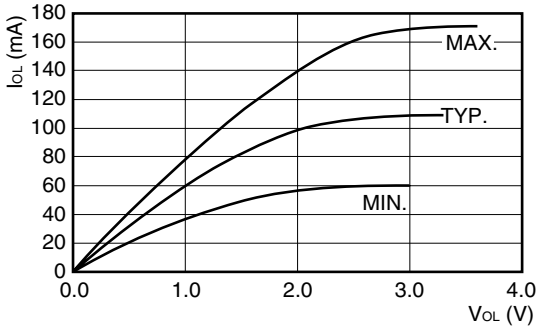


(b) I_{OH} vs. V_{OH}



(21) CMOS 5 V tolerant output, normal type; I_{OL} = 12 mA (Representative block type: FY02)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

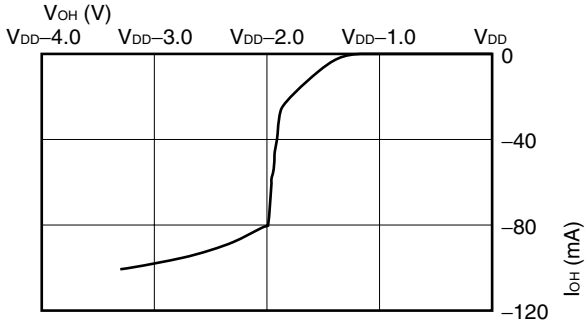
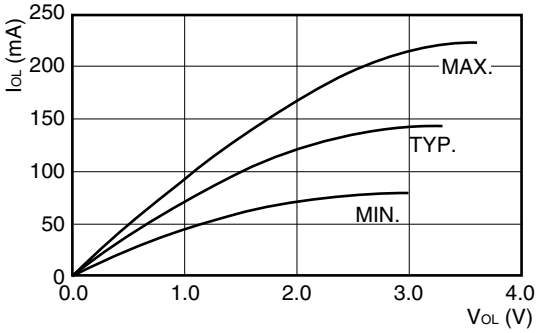


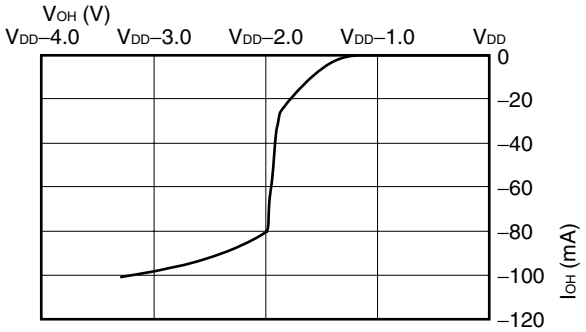
Figure 4-18. I_O vs. V_O (8/9)

(22) CMOS 5 V tolerant output, normal type; I_{OL} = 18 mA (Representative block type: FY03)

(a) I_{OL} vs. V_{OL}

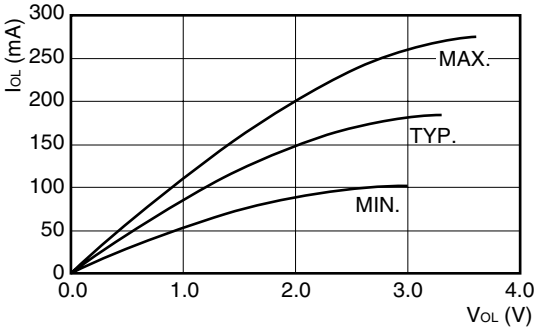


(b) I_{OH} vs. V_{OH}

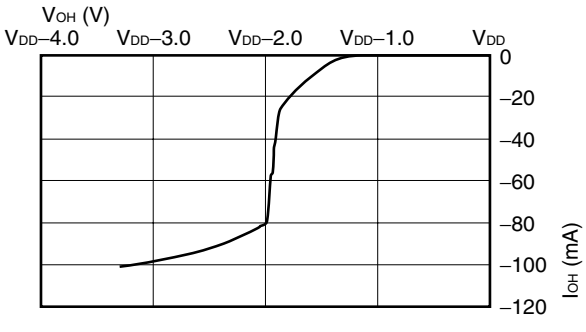


(23) CMOS 5 V tolerant output, normal type; I_{OL} = 24 mA (Representative block type: FY06)

(a) I_{OL} vs. V_{OL}

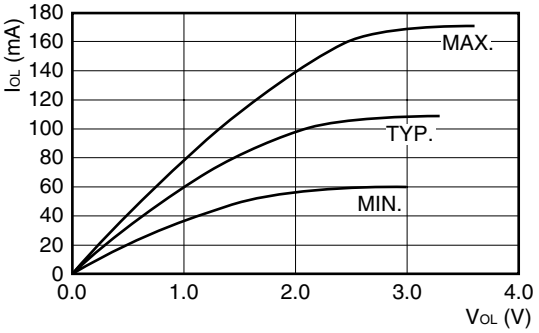


(b) I_{OH} vs. V_{OH}



(24) CMOS 5 V tolerant output, low-noise type; I_{OL} = 12 mA (Representative block type: FZ02)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}

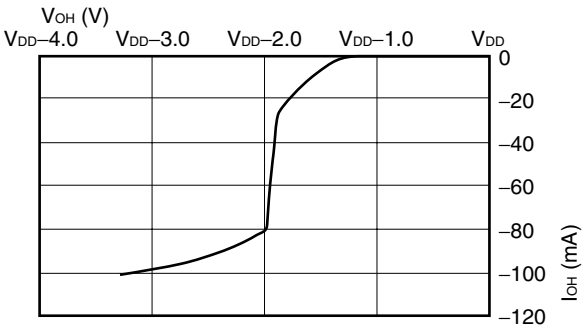
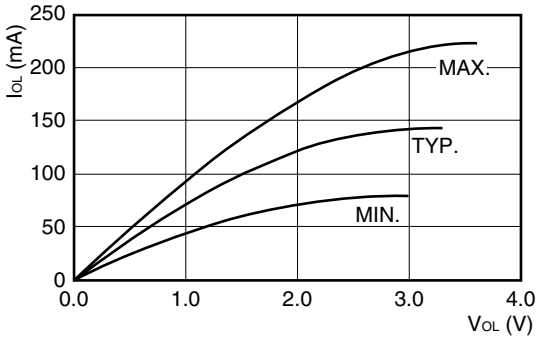


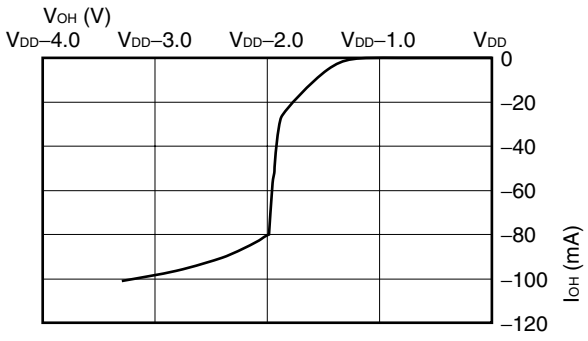
Figure 4-18. I_O vs. V_O (9/9)

(25) CMOS 5 V tolerant output, low-noise type; I_{OL} = 18 mA (Representative block type: FZ03)

(a) I_{OL} vs. V_{OL}

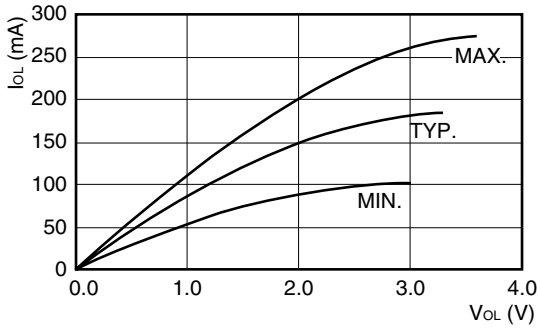


(b) I_{OH} vs. V_{OH}

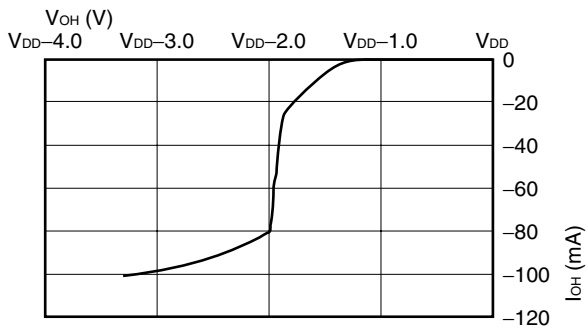


(26) CMOS 5 V tolerant output, low-noise type; I_{OL} = 24 mA (Representative block type: FZ06)

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}



4.6 Limits of Simultaneous Switching of Output Buffers

In recent years, the number of bus lines in systems has increased from 32 to more than 64. In addition, the trend towards high-speed systems has resulted in higher signal operating speeds on the bus line.

Consequently, the frequency with which simultaneous switching is generated has increased greatly, resulting in the problem of system malfunction due to noise. This section considers issues related to simultaneous switching.

4.6.1 Malfunction due to simultaneous switching of outputs

When the output buffer switches from low to high or from high to low, the current that charges/discharges the output load capacitance flows instantaneously to the power supply or GND line via the output buffer. Let i be charge/discharge currents and L the power supply inductance, then, the generated noise is expressed by $L \times \Delta i/\Delta t$. It can be seen from this that the generated noise increases proportionately with changes in the charge/discharge currents and with the power supply inductance. The value of $\Delta i/\Delta t$ is determined by the output buffer type, and generally is larger for output buffers with large drive capability (more accurately, because the slew rate di/dt value is determined by the drive capability of the large output transistors and by the input rise time (t_r) and input fall time (t_f) to those transistors, the value is smaller than for an output buffer that has the same drive capability). As the number of pins that switch simultaneously increases, the excessive charge/discharge currents increase, and sizable noise is generated in the power supply or GND line. This results in malfunction of the system.

There are two types of malfunctions as follows:

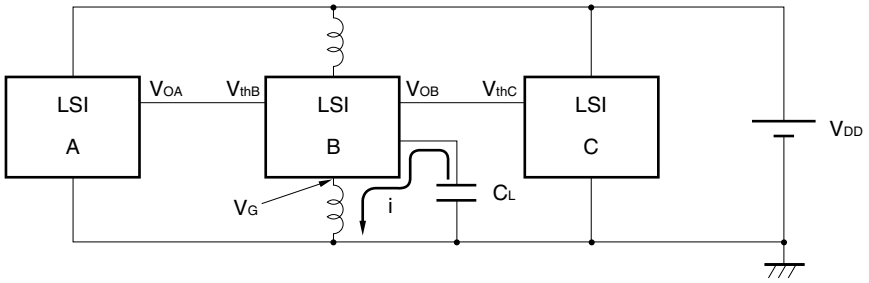
<1> The LSI malfunctions due to fluctuation of the LSI input threshold level

<2> The next stage circuit malfunctions due to noise appearing at the LSI output pin

The circuit in Figure 4-19 (a) can be considered when the LSI's B output buffer is switched from H $\rightarrow$ L. When this happens, the load discharge current flows to the GND line on the mounted circuit board via the LSI B output buffer and the LSI internal GND line. As a result of this discharge current, inverse power arises in the inductance of the GND line, and the LSI internal GND level V_G rises, causing the malfunctions shown in Figure 4-19 (b) and (c). Furthermore, if the output buffer switches from L $\rightarrow$ H, charge current flows to the load capacitance, noise is generated in the power supply line, and the LSI internal V_{DD} level drops momentarily.

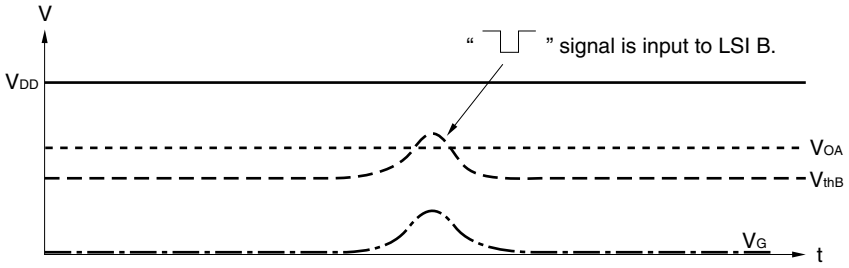
Figure 4-19. Malfunction Caused by Simultaneous Switching

(a) Circuit diagram

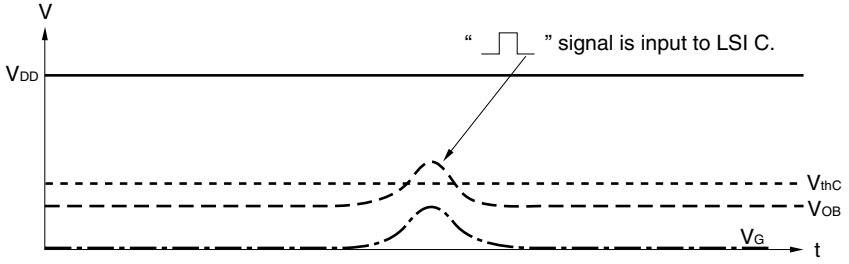


V_{OA}: Output level of LSI A
V_{OB}: Output level of LSI B
V_{thB}: Input threshold level of LSI B
V_{thC}: Input threshold level of LSI C
V_G: GND level of LSI B

(b) Fluctuation in input threshold level of LSI B



(c) Noise generated to the output pin of LSI B



4.6.2 Definitions

Output simultaneous switching is the switching of multiple output buffers in the same direction (H → L, HZ → L or L → H, HZ → H) within a fixed time (see **Table 4-14**) as a result of conditions such as the buffer type and load capacitance. Output simultaneous switching is counted for each switching, and the respective simultaneous switching limits apply independently. The following switching of signals is considered one output simultaneous switching group.

(1) Output signal switching from H → L, HZ → L, X → L, H → X
(2) Output signal switching from L → H, HZ → H, X → H, L → X

Remark HZ is high impedance, and X is indeterminate.

Output signal switching from L → HZ and H → HZ is not counted as simultaneous switching.
For bidirectional pins, switching that occurs during switching from input to output must also be considered.

Table 4-14. Reference Time Ranges for Simultaneous Switching (TYP.)

Buffer Type	Load Capacitance C_L [pF]		
	$0 \leq C_L \leq 50$	$50 < C_L \leq 200$	$200 < C_L \leq 300$
1.0 mA	≤ 2.5 ns	≤ 4.0 ns	≤ 6.0 ns
2.0 mA	≤ 2.5 ns	≤ 4.0 ns	≤ 6.0 ns
3.0 mA	≤ 2.5 ns	≤ 4.0 ns	≤ 6.0 ns
6.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
9.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
12.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
18.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
24.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns

4.6.3 Factors for the determination of simultaneous switching

Because noise generated by charge/discharge currents is the cause of malfunction, the number of simultaneous switching output pins is limited by the following factors:

(1) Drive capability of the output buffers
(2) Load capacitance
(3) Number of output simultaneous switching pins
(4) Number of LSI power supply pins
(5) Routing pattern of GND and power supply on the circuit board
(6) Placement of the simultaneous switching pins
(7) Input buffer types

Items (1) to (3) specify to charge/discharge currents and item (7) specifies the noise margin due to the input buffer interface for the LSI. Items (4) and (5) are restrictions for the closed inductance through which discharged current flows. Thus, these items cannot be specified quantitatively. The simultaneous switching limit specified by NEC Electronics has a default value for the impedance of this loop.

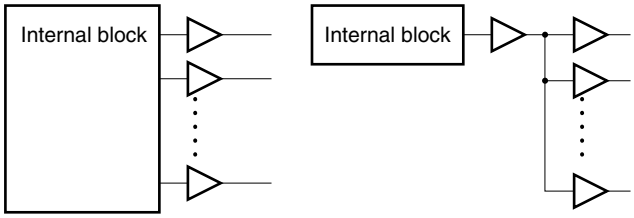
Caution It is possible that noise will be generated, depending on the particular user's circuit board layout. Adequate noise countermeasures must be incorporated into the design of the circuit board.

4.6.4 Simultaneous switching pins to be checked

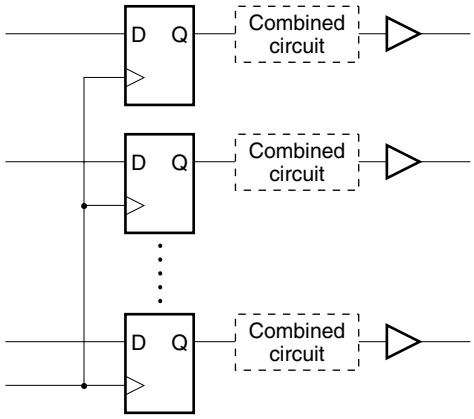
Simultaneous switching of outputs should be checked for output buffer groups that meet the conditions explained below.

Conditions

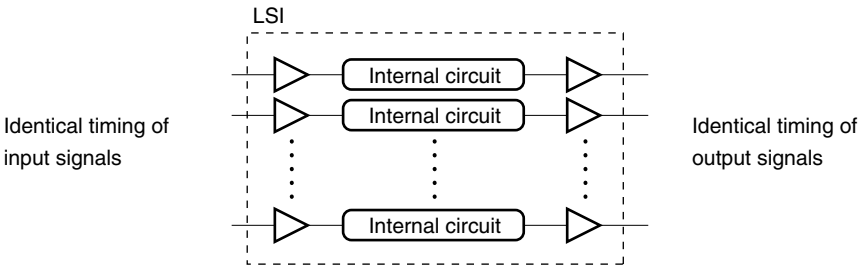
(1) When buffers are driven in parallel by a shared internal block, or one signal output from a shared internal block is split into multiple buffers due to the fan-out limit, and the buffers are driven in parallel.



(2) When the output buffers are driven by sequential circuits switched by a shared control signal. Also, when the switching timing differential of the distributed output buffers, due to the delay time of the combined circuits, is less than the simultaneous switching reference time for each buffer and load capacitance shown in Table 4-14.



(3) When, due to identical timing of the external input, the timing differential of output buffer switching is less than the simultaneous switching reference time for each buffer and load capacitance shown in Table 4-14.



Determination of the simultaneous switching reference time (described in Table 4-14) is performed by the simple summed value of the t_{LD0} (TYP.) values listed in **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

However, checking for simultaneous switching of outputs is not performed in those cases for which the following conditions apply:

- The switching timing differential of the output buffer is greater than the simultaneous switching reference time for each buffer and load capacitance shown in Table 4-14.
- Switching is not generated other than during initialization (set and reset), because malfunctions due to simultaneous switching are absorbed by initialization.

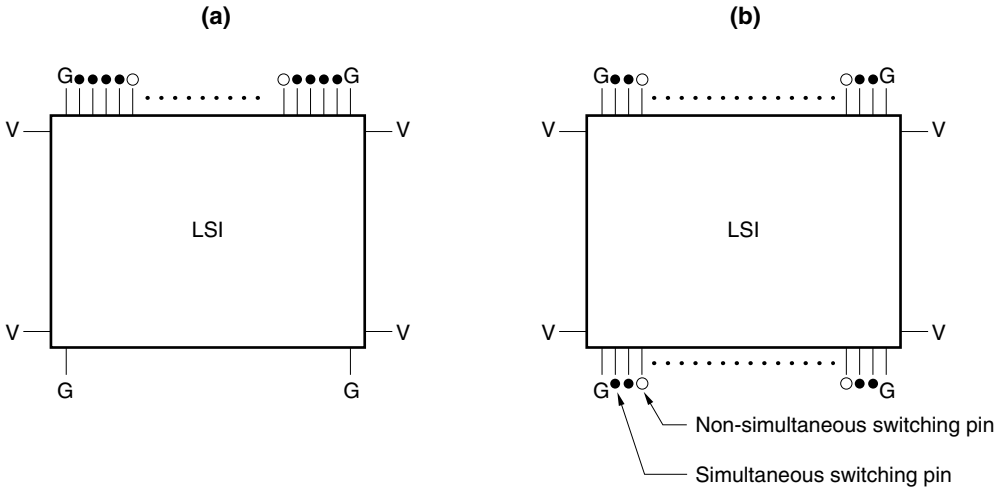
4.6.5 Pin placement and simultaneous switching

The size of closed loop inductance, through which the charge/discharge currents of the output buffers flow, determines the size of the generated noise. The inductance of this closed loop depends on the LSI pin placement and the circuit board on which the LSI is mounted. Care must be taken in placing pins in order to control noise caused by simultaneous switching.

(1) Number of effective GND and power supply pins

If the pins for simultaneous switching of outputs are placed unevenly with respect to the placement of the power supply and GND pins, some of the power supply and GND pins become ineffective for suppressing noise generated by simultaneous switching.

Figure 4-20. Pin Placement for Simultaneous Switching

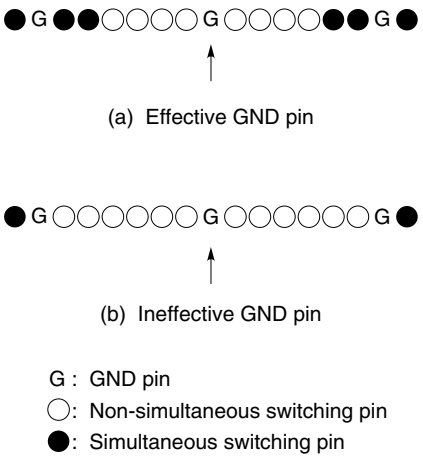


Because the simultaneous switching output pins in Figure 4-20 (a) are concentrated at the top of the chip, the GND pins at the bottom are not very effective in suppressing noise due to simultaneous switching. The number of effective GND pins is therefore equal to two. However, the simultaneous switching output pins in Figure 4-20 (b) are placed equally close to all the GND pins. Therefore, all the GND pins are effective in controlling noise due to simultaneous switching.

In this manner, the number of GND and power supply pins that can be considered effective varies with the placement of simultaneous switching pins. Effective GND and power supply pins are defined as follows:

> If on both sides of a given GND or power supply pin there is a simultaneous switching output pin between that GND or power supply pin and the next ground or power supply pin, then that GND or power supply pin is an effective GND or power supply pin (see **Figure 4-21**).

Figure 4-21. Effective GND Pins



Note that the number of effective power supply pins must be greater than half the number of effective GND pins.

(2) Cautions on pin placement

- Locate input pins (especially clock input pins) susceptible to noise as close to the GND pin as possible. Separate these pins as far as possible from output buffers that switch simultaneously.
- Separate output buffers that switch simultaneously as far as possible from the input pins, and enclose them with GND pins.
- If it is difficult to enclose output buffers that switch simultaneously with GND pins, disperse the buffers as much as possible. In any case, separate the output buffers as far as possible from the input pins.
- Increase the number of GND/V_{DD} pins at a rate of one V_{DD} to two GND.

4.6.6 3 GND pin determination

By this method, a determination is made not for the number of GND and V_{DD} pins of the LSI, but for three GND pins. Therefore, locations at which simultaneous switching are concentrated can be taken into consideration.

Simultaneous switching are assessed by the output buffer type, output load capacitance, and the number of valid GND pins. Table 4-15 shows the number of pins that can switch simultaneously between three contiguous GND pins. Because the allowable number of simultaneous switching pins when a 12 mA 3 V output buffer is used is shown in this table, calculate the allowable number of pins by using the coefficient shown in Table 4-16 if a buffer with a different driving capability and output level is used.

If the driving capability is the same with I_{OL} higher or lower than 12 mA, divide the values in Table 4-15 by the coefficient in Table 4-16.

I_{OL} = Allowable number of simultaneous switching pins between 3 GND pins at 12 mA/Coefficient

Criteria if drive capability or load capacitance is different

In the case of buffers with different driving capabilities, whether the simultaneous switching limit is satisfied is judged using the expression below. The value m_i is number of simultaneous switching pins for each driving capability, and β_i is the simultaneous switching pins conversion coefficient for each buffer. The value of M_i is the allowable number of simultaneous switching pins in Table 4-15.

$\Sigma(m_i \times \beta/M_i) \leq 1$

Calculation example I_{OL} = 18 mA 3.3 V output buffer 15 pF 5 pcs.
I_{OL} = 24 mA 3.3 V output buffer 30 pF 2 pcs.
$5 \times 1.30 \div 15 + 2 \times 1.48 \div 8.9 \leq 1$

Determining BGA packages

The BGA package is determined by the internal chip. For the allocation of internal chip pins, see the tables concerning assignment of V_{DD}, GND, NC, and SCAN test pins in **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**.

Table 4-15. Allowable Number of Simultaneous Switching Pins Between 3 GND Pins (LVTTL Output Buffer, I_{OL} = 12 mA)

Valid Number of GND	Output Load Capacitance C_L					
	15 pF	30 pF	50 pF	100 pF	150 pF	200 pF
1[Note]	9.9	6.0	3.9	2.8	2.5	2.2
3	15.0	8.9	6.4	4.6	4.0	3.7

Note For small pin package

Remark 1. The values in this table are calculated as follows:
Allowable number of simultaneous switching pins (M) = 2.76 + 183.2/load [pF]

Remark 2. Count adjacent GND pins, including those sandwiching a corner on layout, as one.

Table 4-16. Coefficient of Number of Simultaneous Switching Pins

Output Level	I_{OL} (mA)	Coefficient	Example of Corresponding Block
LVTTL output Normal type	3.0 6.0 9.0 12.0 18.0 24.0	0.34 0.63 0.86 1.00 1.30 1.48	FO09, B00T, EXTH FO04, B00E, EXTJ FO01, B008, EXT1 FO02, B007, EXT9 FO03, B009, BP3O, EXT5 FO06, B00H, EXTD
LVTTL output Low-noise type	6.0 9.0 12.0 18.0 24.0	0.22 0.28 0.32 0.36 0.37	FE04, BE0E FE01, BE08 FE02, BE07 FE03, BE09 FE06, BE0H
5 V tolerant output Normal type	1.0 2.0 3.0 6.0 9.0 12.0 18.0 24.0	0.30 0.53 0.82 1.03 1.39 1.87 1.87 1.98	FV0A, EVTT FV0B, EVTK FV09, FY09, EVTH FV04, FY04, EVTJ FV01, FY01, EVT1 FV02, FY02, EVT9 FV03, FY03, EVT5 FV06, FY06, BP5O, EVTD
5 V tolerant output Low-noise type	12.0 18.0 24.0	0.94 0.94 0.99	FW02, FZ02 FW03, FZ03 FW06, FZ06

4.6.7 Cautions for the determination method

The determination of simultaneous switching is also affected significantly by the power supply and GND pins of the circuit board.

It is assumed by the determination method that simultaneous switching is considered for standard circuit board and LSI pin placements. The reference values are determined based on this assumption. Consequently, if the routing pattern of a circuit board is narrow (especially the power supply and GND routing), or if the loop from the power supply wiring on the circuit board through the LSI and GND wiring on the circuit board and back to the power supply wiring is long, and the impedance is large, and the noise generated by simultaneous switching will become greater than the noise level specified by the determination method. This must be kept in mind in order to avoid problems.

In such a case, it is effective to shorten the above closed loop by means of a bypass capacitor.

4.6.8 Other determination methods

The methods explained below must be used if the determination reference cannot be satisfied by the standard power supply and number of GND pins.

(1) Increasing V_{DD} and GND pins

Increase the V_{DD} and GND pins so that the condition of the number of simultaneous switching pins is satisfied. Increase the number of pins at a ratio of one V_{DD} pin to two GND pins.

(2) Re-examine the applicable environment.

<1> Reduction of output load capacitance

The size of the noise generated by charge/discharge currents that flow when the output changes depends on the size of the output load capacitance. Consequently, the size of the generated noise can be reduced by reducing the load capacitance, thereby reducing the allowable number of simultaneous switchings.

<2> Modification of buffer type

The peak values of the output charge/discharge currents depend on the buffer drive capability and the buffer function. By changing to a buffer type with a lower drive capability or to a slew rate buffer, the generated noise can be controlled and the allowable number of simultaneous switching pins can be reduced.

<3> Reduce simultaneous switching pins by adding delay time

Output simultaneous switching is the switching of multiple output buffers in the same direction (H $\rightarrow$ L, HZ $\rightarrow$ L or L $\rightarrow$ H, HZ $\rightarrow$ H) within a fixed time (see **Table 4-14**), as determined by conditions such as the buffer type and load capacitance. Consequently, if delay time is added to the simultaneously operating output pins and the switching time does not fall within the time specified in Table 4-14, then it becomes unnecessary to consider these pins as switching simultaneously, and the number of simultaneous switching pins is thereby reduced.

Remark HZ: High impedance

CHAPTER 5 CIRCUIT DESIGN GUIDELINES

This chapter explains the points to be noted and limits to be applied in designing a circuit.

When designing an LSI using CMOS gate arrays, once a circuit has been designed it cannot be easily modified, unlike when designing a circuit using standard TTL or CMOS ICs.

Therefore, take care to design your LSI without errors by observing the limits and following the design rules described in **CHAPTER 2 IMPLEMENTING THE SYSTEM USING THE GATE ARRAY**, **CHAPTER 4 ESTIMATING ELECTRICAL CHARACTERISTICS**, and this chapter.

If an LSI is designed without observing the design rules, not only is the development period after interfacing with NEC Electronics extended, but also the product you develop may need to be reworked.

5.1 Basic Circuit Configuration

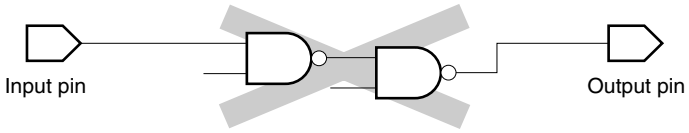
5.1.1 Using I/O buffers

When designing an LSI with gate arrays, place input/output buffers between the LSI and the I/O pins (see **Figure 5-1**).

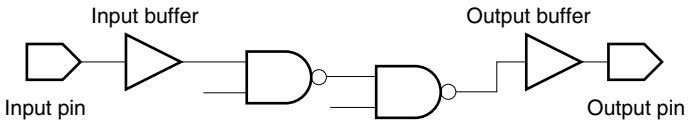
Reasons: <1> To protect the LSI from destruction due to static electricity
<2> To obtain sufficient output drive capability

Figure 5-1. Basic Circuit Configuration

(a) Incorrect example



(b) Correct example



5.1.2 Unused pins

With gate arrays, unused input pins cannot be left open (the state where they are not connected to anything).

The pins must be input at either a high or low level by using F091 (H- and L-level generator). If a block's input pins are open, it cannot function correctly since the input level is undetermined. This condition also becomes a source of I_L (leak current). In addition, large fan-outs should be avoided when F091 is used.

If several blocks are clamped to a single block, the wiring becomes concentrated, making placement and routing difficult. Avoid wiring concentrations for the sake of circuit simplification.

A warning error will be posted by the tester during a design rule check if the block's output pins are open.

Discard unnecessary blocks.

5.1.3 Fan-out limitations

There are limitations on the fan-out capacitance that can be connected to a block's output pins (the fan-out number). The allowable load capacitance for each block is given in **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

Because signal rise and fall times increase (accompanied by a deterioration of accuracy) when the load capacitance to be driven increases, propagation delay time has to be reevaluated. Moreover, if rise and fall times become very long, data-through develops in the flip-flops causing abnormal logic operation.

Therefore, do not exceed the fan-out capacitance limit when designing.

Finally, design with a load capacitance that is 1/3 of the limit in circuits that have strict speed specifications.

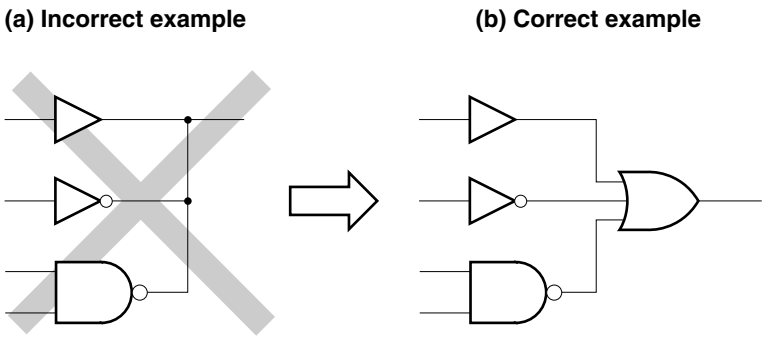
Caution Note that not only the fan-in capacitance of the block connected in the subsequent stage, but also the wiring capacitance is included in the load capacitance.

5.1.4 Wired logic

Other than the case for the bus, do not configure wired logic as mutually connected block outputs.

The P-channel transistors and the N-channel transistors become conductive at the same time as a function of the logic state regardless of the outputs that are connected. Pay attention to this since the steady low-power characteristics can be lost for feature CMOS circuits when the output is at an intermediate level because current can flow from V_{DD} to ground.

Figure 5-2. Wired Logic Prohibitions



5.1.5 Notes on using bidirectional buffer

If an output signal is input as is to the internal circuit with a bidirectional buffer, the internal circuit that receives this input signal may malfunction due to distortion of the output waveform and ringing as shown in Figure 5-3. In the output mode, make sure that the signal immediately before the output buffer is input to the internal circuit as shown in Figure 5-4. In particular, do not employ the design method in which the input signal is input to the flip-flop clock.

Figure 5-3. Ringing

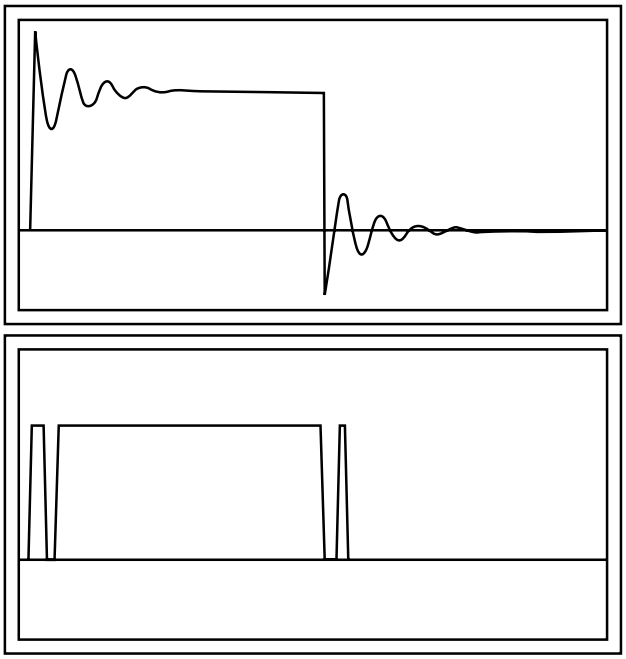
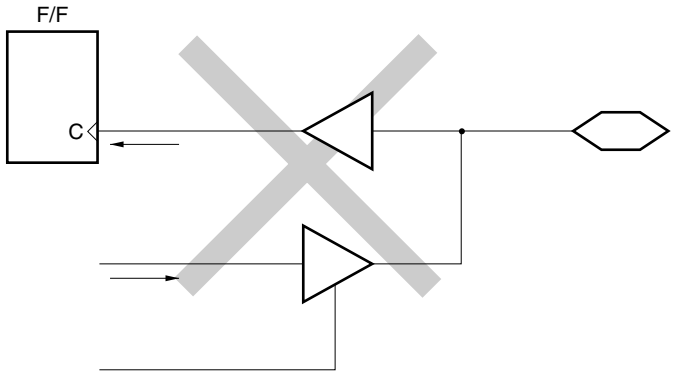
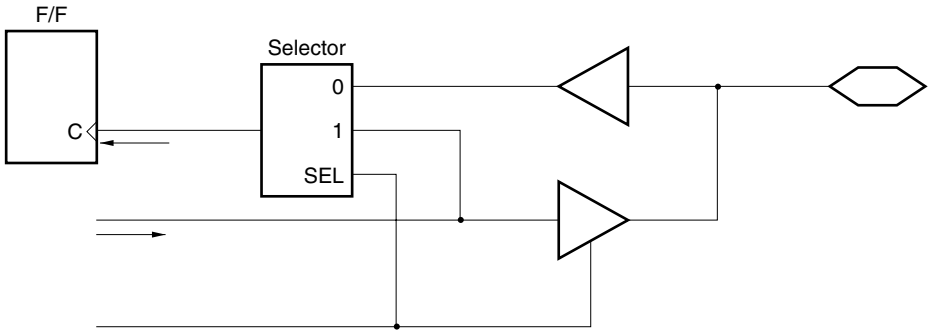


Figure 5-4. Example of Preventive Circuit

(a) Incorrect example



(b) Correct example

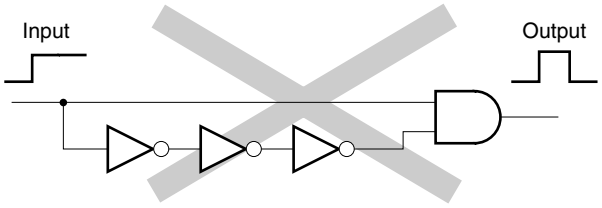


5.2 Differential Circuits

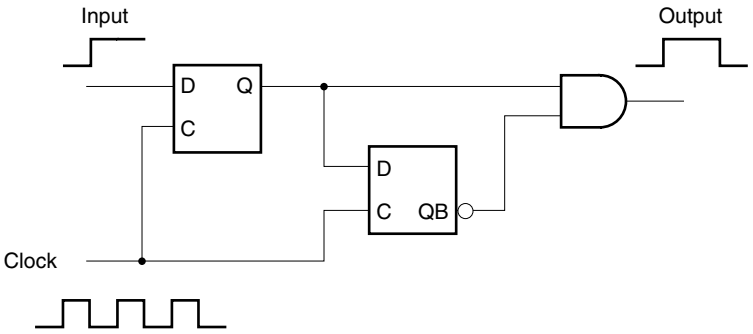
As a rule, differential circuits should not be configured from gate arrays. Since gate-array routing placement and design is done automatically, the range of waveforms that are internally generated cannot be guaranteed with gate arrays, and the desired functions will not materialize. Therefore, avoid structuring the circuit shown in Figure 5-5 (a), and structure the circuit as shown in Figure 5-5 (b).

Figure 5-5. Differential Circuit Prohibitions

(a) Incorrect example



(b) Correct example

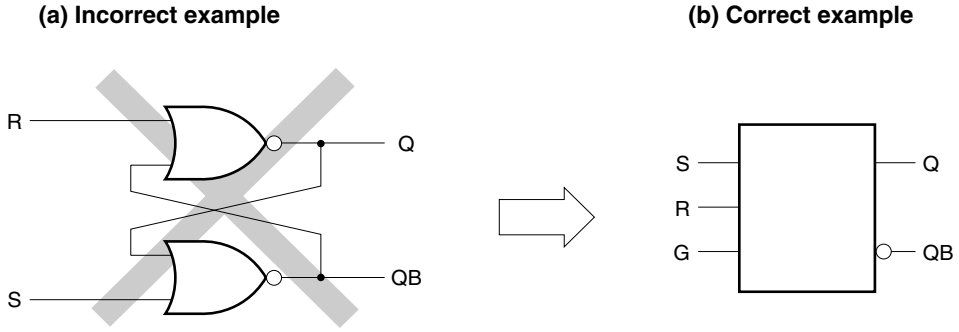


5.3 RS Latch and Loop Circuits

5.3.1 RS latch

Gate-configured asynchronous RS latches should not be used with gate arrays. This is due to cases when initialization cannot take place via simulation or high variation in circuit path speed due to routing location effects.

Figure 5-6. Asynchronous RS Latches

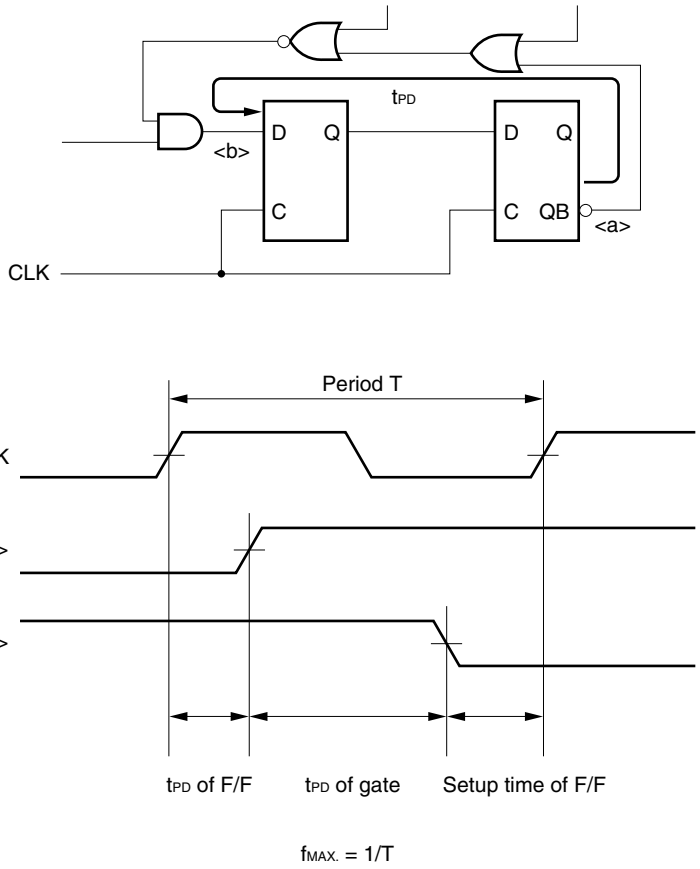


5.3.2 Loop circuit

The following points must be noted when loop circuits, such as feedback loops, are used.

(1) As shown in Figure 5-7, if gates lie between feedback loops in divider circuits, the frequency characteristics will drop due to the delay time caused by these gates. The delay times of these loops must be determined beforehand and the frequency characteristics must be verified (see **5.6 Delay Time Margin** for the verification method).

Figure 5-7. Loop Circuit



(2) A loop circuit cannot be formed when the scan path is formed. In this case, isolate the loop circuit by using gates as a countermeasure.

5.3.3 Prohibited state of flip-flops

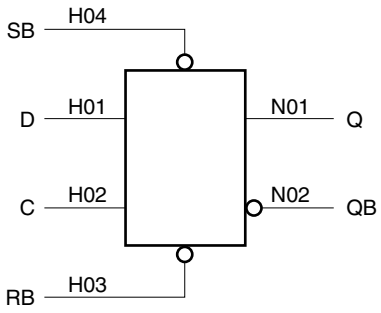
The state in which both the set and reset inputs of an RS latch or flip-flop are enabled at the same time is prohibited. This is because the retained data becomes unstable if both the set and reset inputs are disabled simultaneously. What value the retained data will take is influenced by delicate timing such as the timing of the set and reset signal input and delay of the internal signal of the flip-flop and cannot be guaranteed.

Consequently, be aware of the following when using flip-flops with set/reset inputs.

<1> Do not enable set and reset inputs at the same time.

<2> When it is necessary to enable set and reset inputs simultaneously, disable one side first and then disable the other side. By doing this, the state that the flip-flop was in when it was disabled will be maintained.

Table 5-1. F617 (D-F/F with RB, SB)



D	C	RB	SB	Q	QB	
0	↑	1	1	0	1	
1	↑	1	1	1	0	
X	↓	1	1	Hold	Hold	
X	X	0	1	0	1	
X	X	1	0	1	0	
X	X	0	0	0	0	← Prohibited state

X: Undefined

5.4 Clock Signal Design

This section refers to those gate arrays which are basically designed as synchronous circuits.

5.4.1 Synchronous circuit design

Synchronous circuits consist of single-phase circuits, which are used for circuit design using general-purpose LSIs, as well as multiphase circuits used in CPU design. The characteristics of single-phase and multiphase synchronous circuit design are shown in Table 5-2.

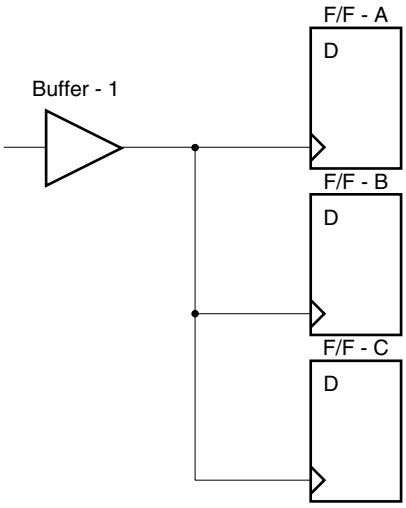
Table 5-2. Features of Single-Phase and Multiphase Synchronous Circuit Design

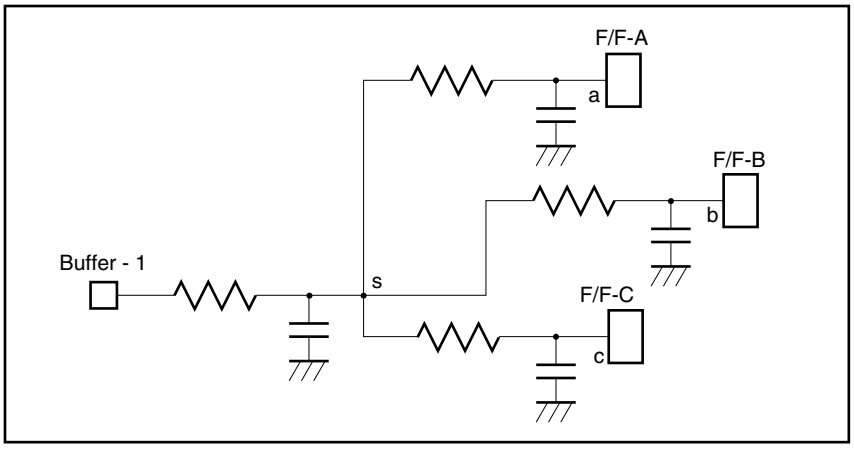
Circuit Design Method	Advantages	Disadvantages
Single-phase synchronous circuit design	• Circuit is simple. • Generally suited to high-speed circuits.	• Signal skew on the clock line must be considered in configuring shift registers
Multiphase synchronous circuit design	• Timing tests for shift registers are unnecessary.	• A multiphase clock signal must be generated. • Number of gates increases. • Generally unsuited to high-speed operation.

(1) Single-phase synchronous circuit design

Single-phase circuits should be designed when sequential circuits will operate with a single clock signal. This relatively simple design method is necessary to adjust for clock skew timing.

Figure 5-8. Clock Skew





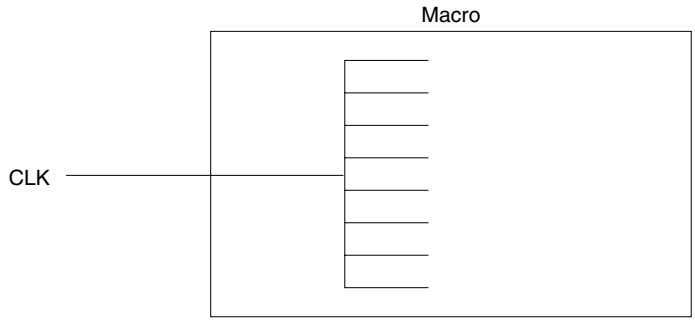
The s-a delay time differs from the s-b and s-c delay times due to wiring resistance.

Clock skew, a shift of the clock signal between sequential circuits, is dependent on the wiring length from the point of divergence of the circuits. Follow these measures in consideration of clock skew when performing single-phase circuit design.

(A) Try to allocate similar macros to the same clock line (see **Figure 5-9 (a)**).
(B) When allocating a large number of clock lines, allocate the lines so that errors due to clock skew do not occur (see **Figure 5-9 (b)**).
(C) Accelerate the operation of the final-stage register by structuring the synchronous counters and shift registers (see **Figure 5-10**).
(D) Use clock tree synthesis (see **5.4.3 Clock tree synthesis**).

Figure 5-9. Clock Skew Countermeasure 1

(a)



(b)

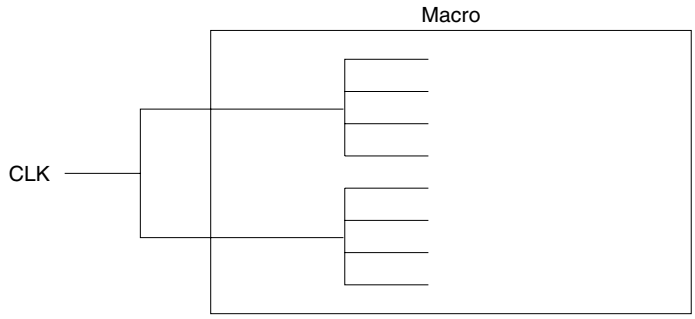
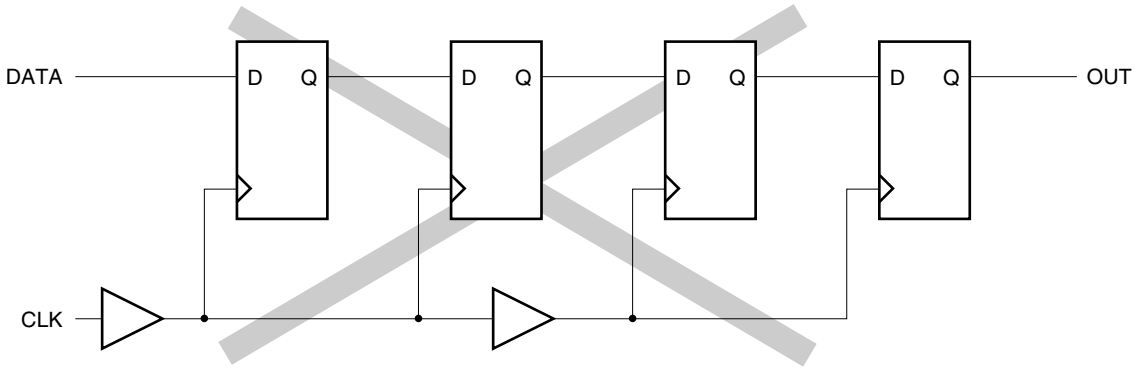
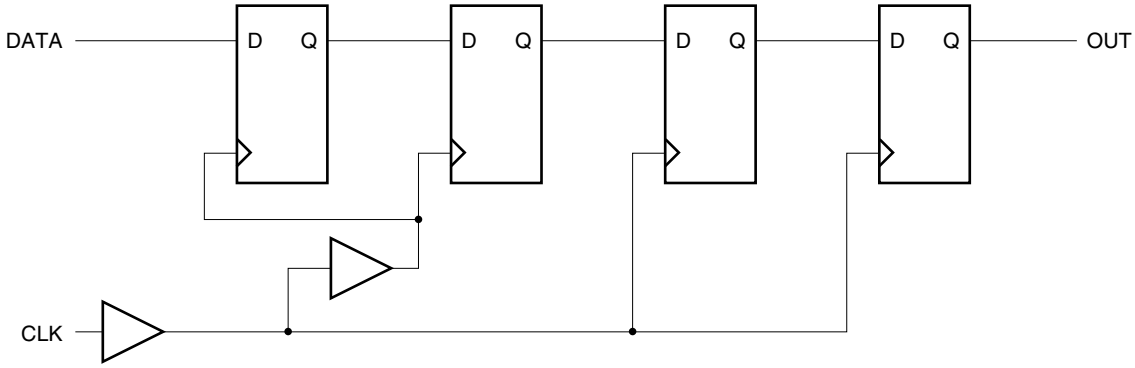


Figure 5-10. Clock Skew Countermeasure 2

(a) Circuits with potential for error



(b) Circuit with a clock skew countermeasure



If buffers are inserted in the clock line due to the fan-out limitation, the countermeasures illustrated in Figure 5-10 (b) must be taken.

(2) Multiphase synchronous circuit design

The operation of sequential circuits in multiphase design normally involves two or more clock signals with a constant relationship. This method avoids contention of clock operation between sequential circuits.

Figure 5-11. Double-Phase Synchronous Circuit

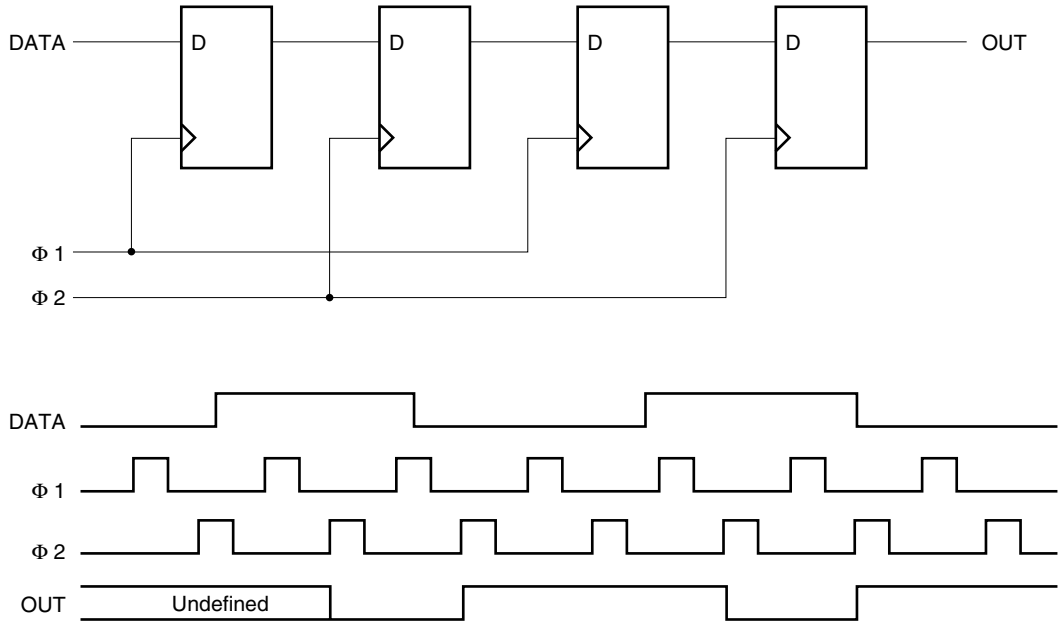


Figure 5-11 is an example of a double-phase clock circuit. The two clock signals (Φ1 and Φ2) vary in timing. This avoids hold time errors between two sequential circuits. Even if there is interaction between complex sequential circuits, testing for timing contention can be curtailed. In addition, since the number of gates is reduced in this circuit example, a latch can be used instead of a flip-flop. In multiphase synchronous circuit design, configure the several clock signals from the basic clock signal. This will result in a lower clock frequency than that needed for a normal single-phase circuit (high speed is possible with a pipeline structure).

5.4.2 Clock skew

Clock skew is generated by wiring length variations as a function of macro placement. Hold timing errors in sequential circuits can result from clock skew. Usually, however, it is impossible to take any errors due to these variations into consideration in the simulation before placement and routing. Therefore, the following guidelines are provided to minimize this problem.

(A) Clock line design in a macro

One clock line should be supplied in single-phase synchronous circuit design.

It is basically not necessary to test for clock skew in multiphase synchronous circuit design.

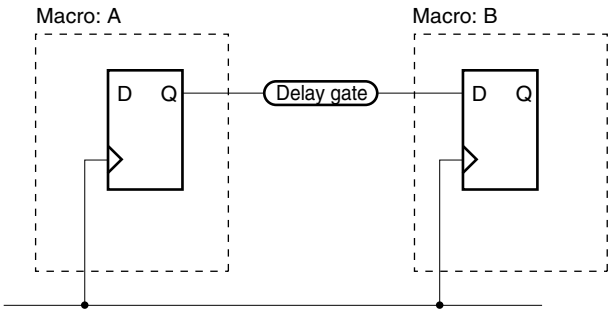
However, it is necessary to check operating frequency.

(B) Clock line design between macros

There are special clock skew problems between macros associated with single-phase synchronous design. Examples of a countermeasure are shown in Figure 5-12.

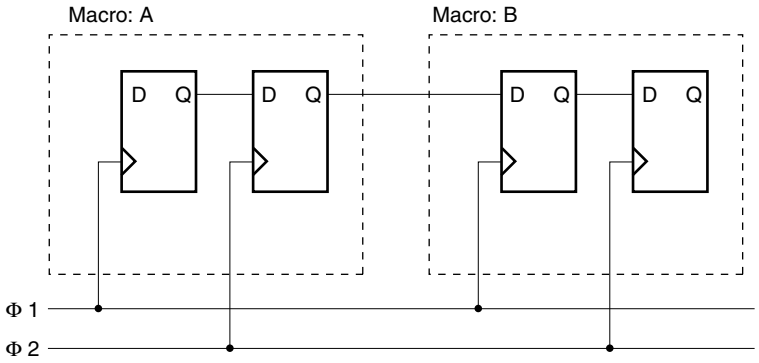
Figure 5-12. Clock Line Countermeasure

(a) Insert delay gates



A delay gate must be inserted in order to gain flip-flop hold time in Macro: B.

(b) Make circuit multiphase



(c) Receive signal by inverse-phase clock

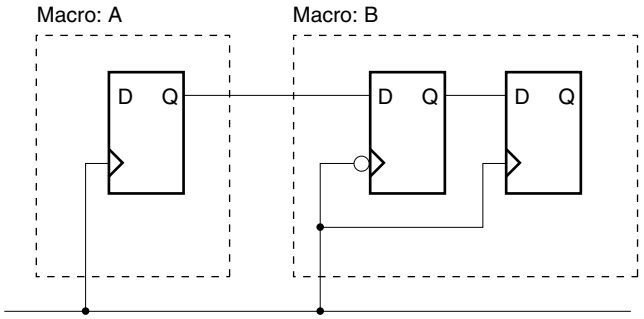


Figure 5-12 (b) is a measure using a multiphase clock. In this case, it is necessary to keep the clock frequency in mind.

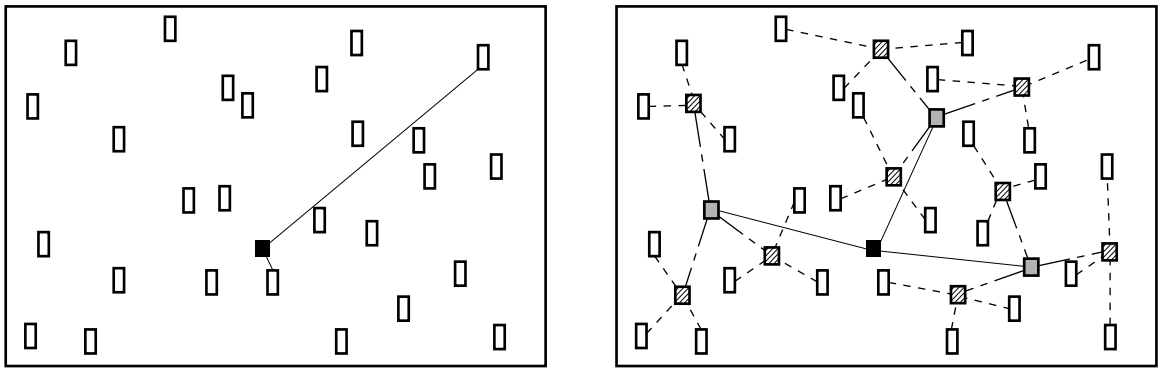
Figure 5-12 (c) uses inverse phase so that there is a hold time margin. With this method, it is necessary to keep the clock frequency and duty cycle in mind.

5.4.3 Clock tree synthesis

Clock tree synthesis is a technique that minimizes clock skew between flip-flops that are connected to the clock line. As shown in Figure 5-13 (a), the distance between the clock driver and each flip-flop is not constant. In addition, wiring resistance increases due to shrink processing. Because of this, the variations in wiring length are linked to clock skew. With clock tree synthesis, a buffer is inserted in the clock line. This uniformly distributes the clock line, as shown in Figure 5-13 (b).

Figure 5-13. Concept of Clock Tree Synthesis

(a) Conventional **(b) Clock tree synthesis**



- First-level driver
- Second-level driver
- Third-level driver
- Flip-flop

(1) Benefits of clock tree synthesis

In clock tree synthesis, a clock tree synthesis block is substituted for the clock drivers that are usually used. The block names and the number of inserted stages is shown in Table 5-3. The selection of the blocks to be used is based on the number of clock line branches.

Caution The recommended number of CTSs used is one per chip. Two or more CTSs can be used, however, there is a risk of lowering the cell utilization rate and causing clock skew to increase due to the increase in the number of CTSs used. The more CTSs are used the more time is required for clock tree synthesis and routing.
Therefore, take this into account when determining the schedule.

Table 5-3. Reference List of Buffer Type CTS Delay, Skew Values (with 1 CTS Incorporated)

Block Name	Layer	Input Block	Number of Clock Line Branches				
			32 to 128 [127]	129 to 1280 [560]	1281 to 2560 [1978]	2561 to 5120 [3854]	Maximum Number of Branches
FC52	2	F154	(0.43 to 1.29) 0.05 ns	Δ	×	×	139 to 256
FC53	3	F154	(0.45 to 1.49) 0.15 ns	(0.56 to 1.85) 0.19 ns	(0.91 to 2.92) 0.28 ns	Δ	2653 to 5035
FC54	4	F154	(0.54 to 1.76) 0.10 ns	(0.54 to 1.86) 0.23 ns	(0.97 to 3.03) 0.27 ns	(0.98 to 3.11) 0.38 ns	50412 to 95664
FC92	2	F158BR	(0.29 to 0.98) 0.05 ns	Δ	×	×	176 to 334
FC93	3	F158BR	(0.37 to 1.21) 0.08 ns	(0.38 to 1.31) 0.12 ns	Δ	Δ	2111 to 4007
FC94	4	F158BR	(0.44 to 1.46) 0.08 ns	(0.45 to 1.57) 0.13 ns	(0.62 to 2.10) 0.21 ns	(0.71 to 2.37) 0.34 ns	25340 to 48086

Caution 1. The values in the above list are for reference only, and may change depending on the master and number of cells, and the circuit configuration (presence/absence of macros), etc.

Caution 2. It does not necessarily follow that the number of clock branches increases proportionate to FC52 to FC94.

Caution 3. The maximum number of clock branches differs depending on the master.

Caution 4. The maximum number of clock branches is the value when flip-flops at fan-in 1:0 are used.

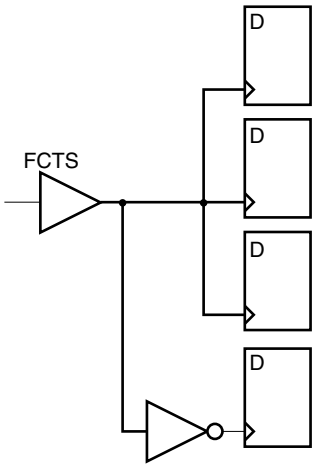
Remark This expansion block differs from the conventional inverter type CTS block.
The meanings of the symbols in the table are as follows.
×: Reserved
Δ: Can be used depending on the master and circuit configuration.
Values in parentheses ( ) in the table indicate the minimum delay time (left) and maximum delay time (right) of when the number of branches is the number in the brackets [ ], and the number underneath indicates the maximum clock skew time.

(2) Clock tree synthesis guidelines

The following precautions apply when using clock tree synthesis.

(a) The section from the output of the clock tree synthesis block (FCTS) to the block that requires optimized clock skew must be written by one net.
If a function block is inserted in the path, the clock skew up to the function block is optimized.

Figure 5-14. Clock Skew Optimization



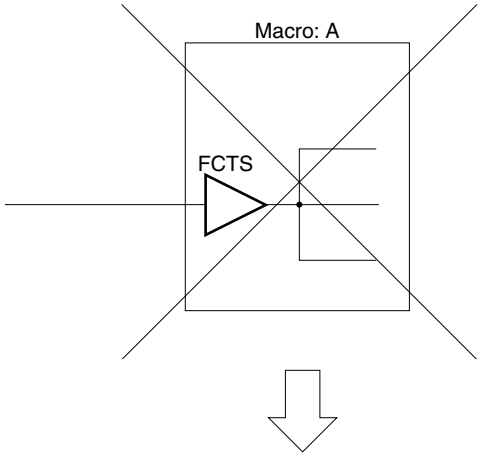
In clock tree synthesis, the clock skew is optimized as far as the thick lines.

(b) Describe FCTS in TOP layer.

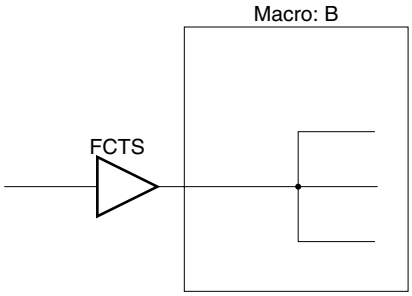
FCTS can be described even in macro unless fed back to upper layer.

Figure 5-15. Example of CTS Block Writing

(a) Incorrect example



(b) Correct example



(c) Routing detours increase with large macros and high use rates, and there are cases where clock skew cannot be sufficiently optimized.

(d) Since delay times increase, use a digital PLL (see **7.6 Digital PLL**) when there are timing problems between chips.

5.5 Notes on Configuring High-Speed Circuits

Generally, an N-channel transistor can pass a higher current than a P-channel transistor. Therefore, a NOR gate consisting of P-channel transistors connected in series has a reduced load drive capability at the rising of the output. For example, a NOR block in a CMOS gate array is slower than a NAND block, and has poor fan-out characteristics.

The guidelines for structuring a circuit that will run at high speed are shown below.

(1) Structure the circuit by using logic conversion techniques and standard NAND blocks.

- The circuit's speed will improve, as will the circuit's stability (see **Figure 5-16 (a)**).

(2) Structure the circuit so that the fan-out is as small as possible to lighten the load.

- As a rule of thumb, stick to 1/3 to 1/2 the fan-out limit (see **Figure 5-16 (b)**).

(3) Convert from low-power blocks to standard blocks.

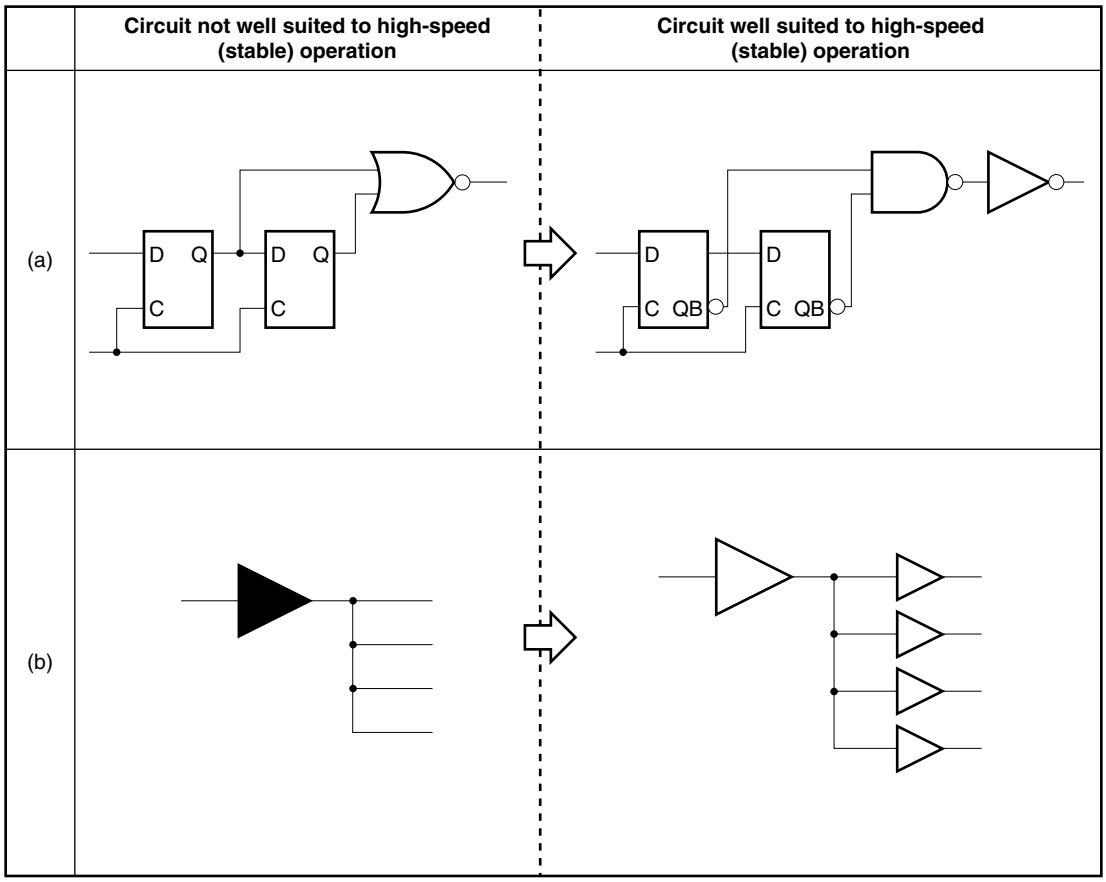
(4) Use complex blocks.

(5) Select the high-speed BLC method when a macro is used while using NEC Design Ware

(6) Closely place macros between which high-speed signals are transferred.

(7) Execute a test run once in advance if possible.

Figure 5-16. Configuring High-Speed Operational (Stable) Circuits



(8) Designing in modules (piecemeal)

When designing high-speed, large scale circuits, it is generally possible to improve efficiency by dividing the device into several modules and designing in layers.

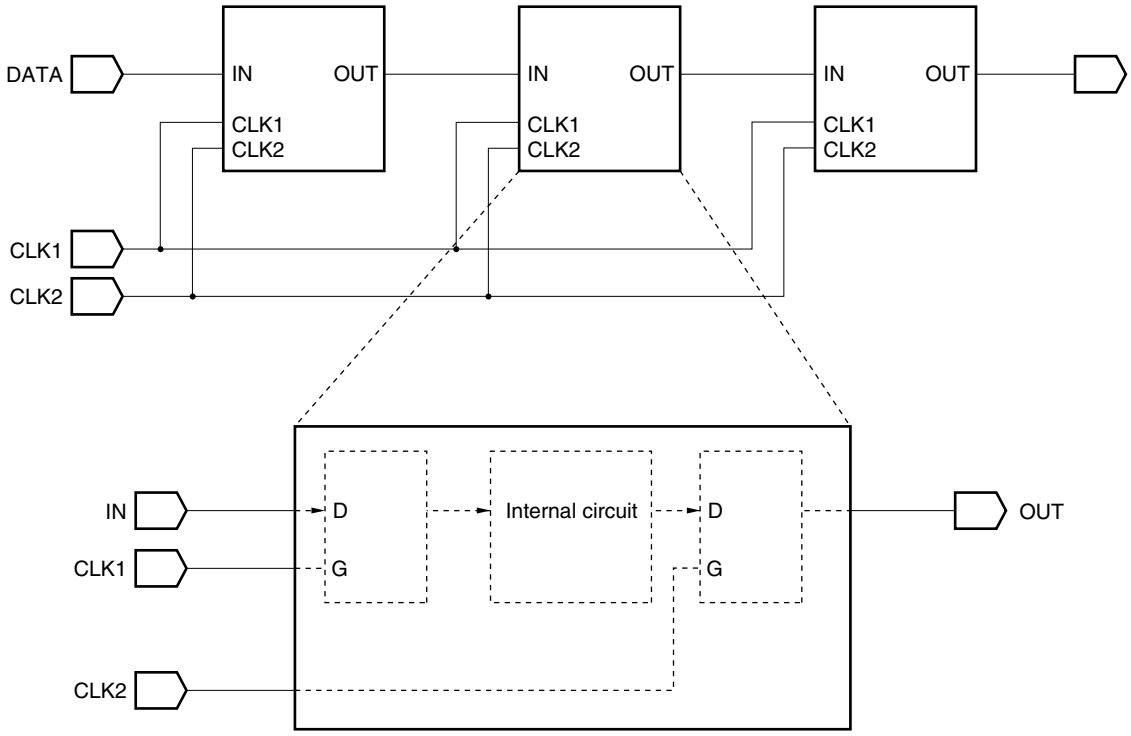
Standardization of inter-macro interfaces

The largest obstacle to overcome in layer designing is the inability to complete circuit design due to the lack of compatibility between inter-macro interfaces when macros are joined on a single chip.

The solution to this problem lies in the standardization of the inter-macro interfaces.

A simple example of this is shown in Figure 5-17 below. In this example, it has been decided to first latch all the output data of the respective macros with CLK2 before being output, and latch all the input data with CLK1 before being received. As a result, it has been possible to avoid contention when receiving inter-macro data, and at the same time standardize the interfaces related to this process.

Figure 5-17. Standardization of Inter-Macro Interfaces



5.6 Delay Time Margin

The logic circuits consist of combination circuits whose output is determined uniquely by the state at their inputs and sequential circuits whose output is determined by the state at their inputs and their previous state. Specifically, sequential circuits consist of gate circuits that have feedback, flip-flops, and latches.

Taking into consideration the testability and delay times, it is clear that individual combination and sequential circuits can not be too large. Also, a majority of the sequential circuits are operated in synchronization with the system clock which has an adequate margin with respect to the delay times of the combination circuits.

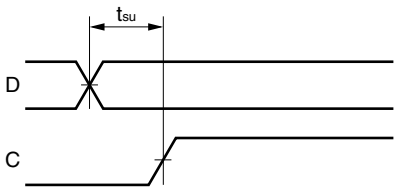
At the portion where adequate margin cannot be secured by the clock, timing of the entry of the sequential circuit, i.e., each input of flip-flops and latches, must be secured.

5.6.1 Timing definitions

(1) Setup time (t_{su})

In latches or flip-flops, the data setup time needed to read in data by the active edge of the clock.

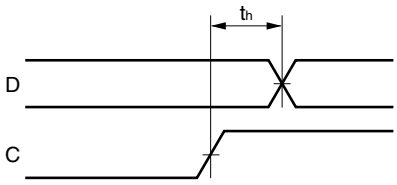
Figure 5-18. Setup Time



(2) Hold time (t_h)

In latches or flip-flops, the data hold time needed to read in data by the active edge of the clock.

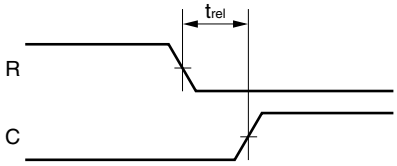
Figure 5-19. Hold Time



(3) Release time (t_{rel})

In latches or flip-flops, release time is the time needed from release of the reset (or set) until the active edge of the next clock becomes valid.

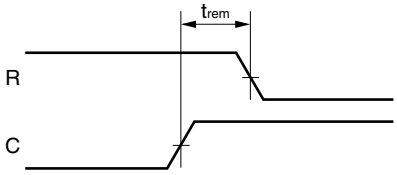
Figure 5-20. Release Time



(4) Removal time (t_{rem})

In latches or flip-flops, removal time is the time needed to make the active edge of the clock invalid when the reset (or set) is cancelled.

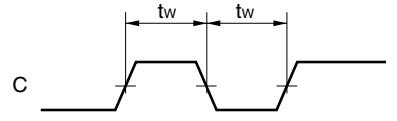
Figure 5-21. Removal Time



(5) Minimum pulse width (t_w)

In latches or flip-flops, minimum pulse width is the minimum time of the clock (or reset and set) pulse width needed in order to read in data correctly.

Figure 5-22. Minimum Pulse Width



5.6.2 Delay time margin (asynchronous circuits)

As an example of calculating the delay time margin, we will look at the setup time and the hold time for the circuit in Figure 5-23. Here, the variation and wiring length establish the specifications for decreasing the margin. If the fixed standard values that are determined by each block (t_{su} and t_h) are satisfied, decisions about normal operation can be ascertained.

Figure 5-23. Delay Time Margin Calculation

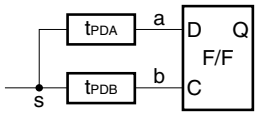
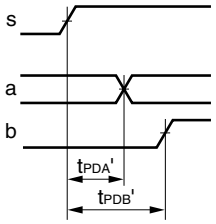
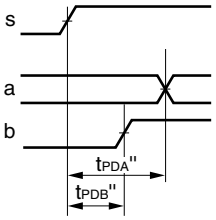


Figure 5-24. Timing Estimate

(a) Setup time (t_{su})



(b) Hold time (t_h)



Calculation equations:

$$t_{SU} < t_{PDB}' - t_{PDA}'$$
$$= t_{PDB\,(MIN.)} - t_{PDA\,[MIN.\,(MAX.)]}$$
$$= t_{PDB\,(MIN.)} - t_{PDA\,(MIN.)} \times \frac{1+\alpha}{1-\alpha}$$

$$t_h < t_{PDA}'' - t_{PDB}''$$
$$= t_{PDA\,(MIN.)} - t_{PDB\,[MIN.\,(MAX.)]}$$
$$= t_{PDA\,(MIN.)} - t_{PDB\,(MIN.)} \times \frac{1+\alpha}{1-\alpha}$$

α: Distribution coefficient (0.1)

5.6.3 Delay time margin (high-speed circuits)

In circuits operating at high frequencies, the operating margin for an internal functional block's delay time is small since the single-cycle time is short.

Here, we show the delay time margin calculation for both in-phase and inverse-phase circuits.

(1) In-phase clock

Consider the shift register operation containing delay A between flip-flops F1 and F2 in Figure 5-25.

As shown in Figure 5-26, the points at which this circuit is inspected are where the output data (Q of F1) passes through delay A to F2 (sampling timing <1>) and at sampling timing <2>, where a check is made to see if the data is read normally.

Therefore, the value resulting from adding the maximum delay at point a to the setup time of F2 must be obtained within one time period T.

Figure 5-25. In-Phase Clock Circuit

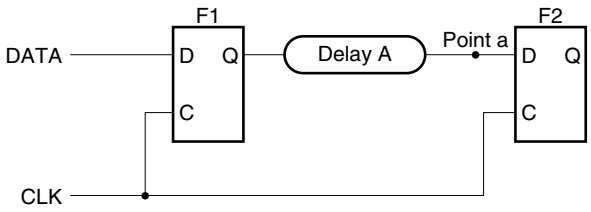
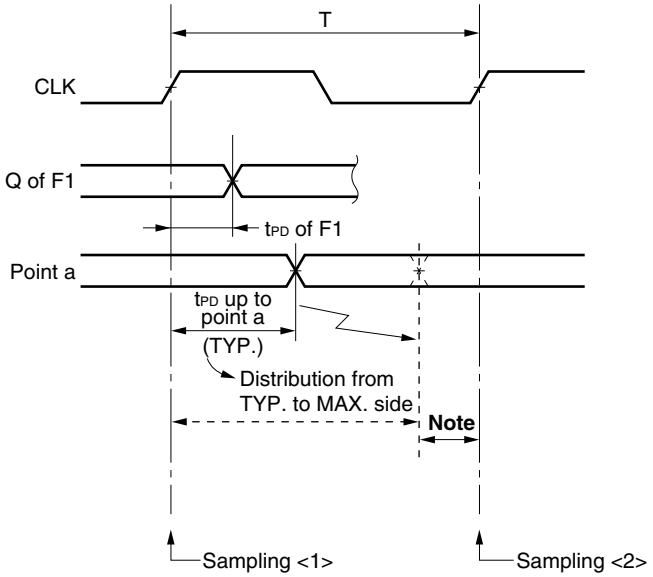


Figure 5-26. In-Phase Clock Timing



Note Considering the F2 setup time, do not cross into the next sampling timing.

Calculation equation:

$T - (t_{PD\ (F1)\ (MAX.)} + t_{PDA\ (MAX.)}) > t_{SU\ (F2)}$

The following countermeasures are necessary if this relationship is not satisfied:

- Reduce the amount of delay of delay A
- Lower the operating frequency (lengthen period T)

(2) Inverse-phase clock

Figure 5-27 is an inverse modification of the F2 clock's active edge shown in Figure 5-25. Since both the rising and falling edges are used, the operating margin varies as a function of the clock's duty cycle. The circuit normally operates under the following conditions.

Figure 5-27. Inverse-Phase Clock Circuit

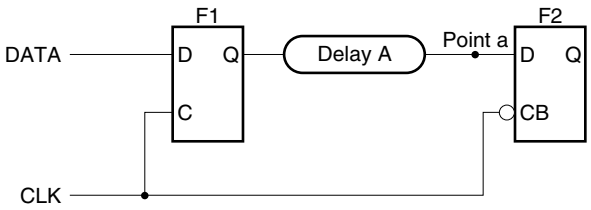
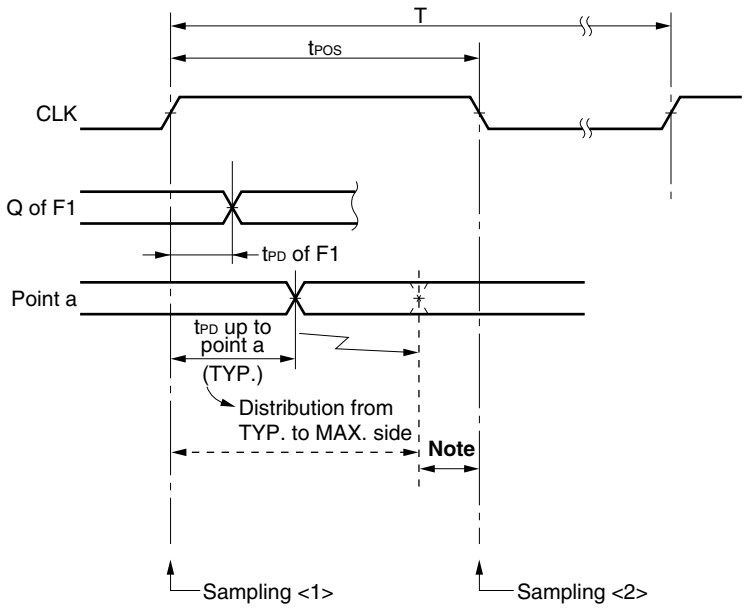


Figure 5-28. Inverse-Phase Clock Timing



Note Considering the F2 setup time, do not cross into the next sampling timing.

Calculation equation:

$t_{POS} - (t_{PD\ (F1)\ (MAX.)} + t_{PDA\ (MAX.)}) > t_{SU\ (F2)}$

The following countermeasures are necessary if this relationship is not satisfied:

- Reduce the amount of delay of delay A
- Lower the operating frequency (lengthen period T)
- Increase the CLK duty

5.6.4 Minimum pulse width

With circuits operating at high speed, there are cases when the minimum pulse width for a flip-flop input block is not satisfied due to the delay difference between the rise of the signal and its fall and the relative variation of identical pulses.

For example, in Figure 5-29, the signal input by the clock passes through delay B and is input to the flip-flop. The timing is shown in Figure 5-30. In regard to delay B, when the fall time delay $t_{PDB\ (LL)}$ is greater than the rise time delay $t_{PDB\ (HH)}$, t_{NEG} becomes greater than $t_{NEG\ (MIN.)}$, and the pulse becomes narrow.

$t_{NEG\ (MIN.)}$ is estimated by specifications established by the relative variation between the maximum $t_{PDB\ (LL)}$ and $t_{PDB\ (HH)}$.

Figure 5-29. Minimum Pulse Width Estimate

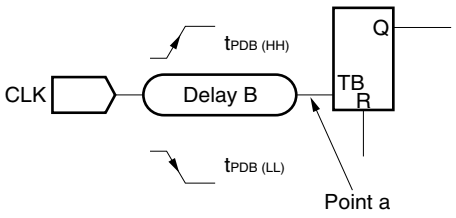
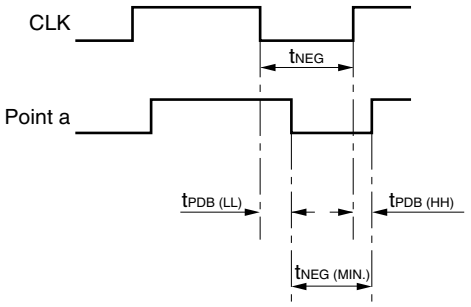


Figure 5-30. Pulse Narrowing



Calculation equations:

$$t_{NEG\ (MIN.)} = t_{NEG} + (t_{PDB\ (HH)\ (MAX.)} - t_{PDB\ (LL)\ [MAX.\ (min.)]}) > t_W$$

$$\rightarrow t_{NEG\ (MIN.)} = t_{NEG} + (t_{PDB\ (HH)\ (MAX.)} - t_{PDB\ (LL)\ (MAX.)} \times \frac{1-\beta}{1+\beta}) > t_W$$

β: Distribution coefficient (0.1)

The ratio $t_{PDB\ (HH)}/t_{PDB\ (LL)}$ is controlled in order to regulate the minimum pulse width of the signal that is input to the flip-flop. This increases the duty cycle. In the example above, the fall is at the functional block that contains delay B and the delay $t_{PDB\ (LL)}$ is short. If the rise delay $t_{PDB\ (HH)}$ is converted to be slow, $t_{NEG\ (MIN)}$ increases. In addition, be aware that a high-level pulse width standard must be satisfied.

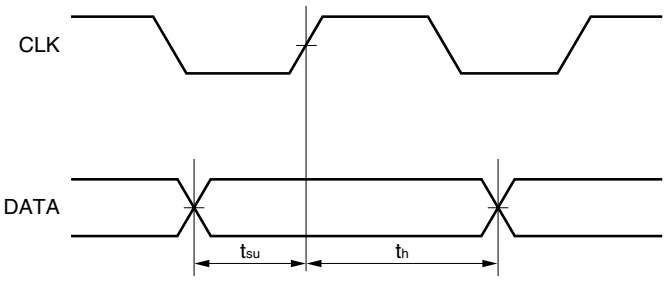
5.6.5 Metastability

If the setup and hold time standards are satisfied, an output is generated at the flip-flop and latch if a block and data as well as a block and set/reset are changed simultaneously. It then becomes possible to obtain an intermediate level that is neither high nor low. This unstable condition is called metastability.

The metastable state is finalized after a certain time, and the output settles into a high or low level. However, an unstable state results since the level that is defined has no relationship to the data input level.

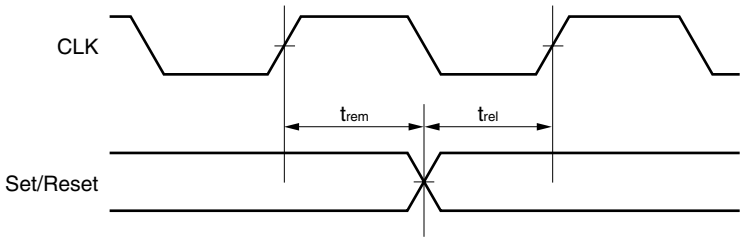
In the cases where the setup, hold, release and removal times cannot be satisfied, take the countermeasures shown below to prevent this unstable state from spreading over the entire circuit.

Remark Setup time (t_{su}) .....Time that the data signal must secure before the clock changes
Hold time (t_h) .....Time that the data signal must be held after the clock changes



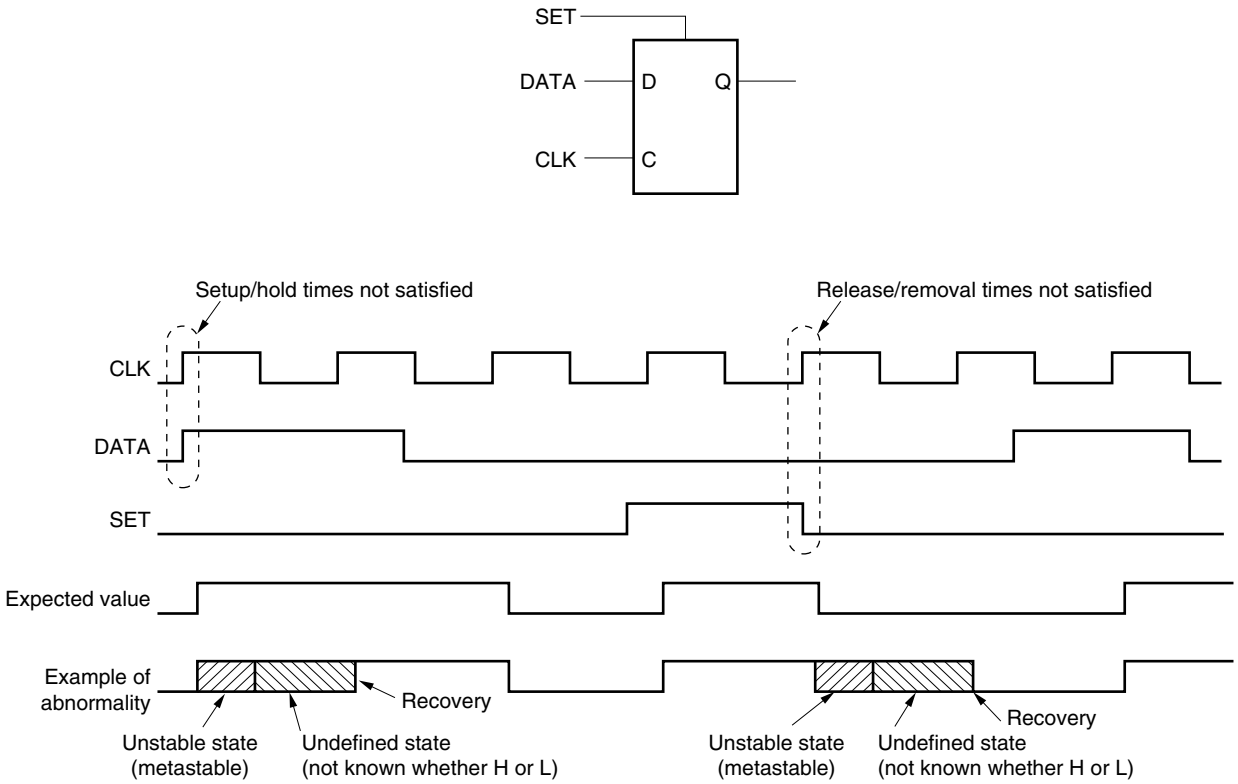
Caution The specified time must be satisfied for t_{su} and t_h (see CMOS-9HD Series, EA-9HD Series Block Library (A13052E)).

Release time (t_{rel}) .....Time after the set/reset signal changes until the clock becomes valid
Removal time (t_{rem}) ...Time needed in order to make the clock invalid



Caution Do not cancel the set or reset signals in the vicinity of the active edge of the clock.

(1) Metastability and recovery time



In the CMOS-9HD Series, the time of the metastable state is specified as shown below. After this time, it is not clear whether the state is H or L, but it is one of them (it is shown as “Undefined” in the above figure).

Metastable time = $t_{PD\ (MAX.)} \times 6$

where:

$t_{PD\ (MAX.)}$ ..... Maximum value of the delay time from the active edge of the clock until the output changes (when the ratings of the setup/hold times could not be satisfied); or, release/removal time (when the ratings of the release/removal times could not be satisfied).

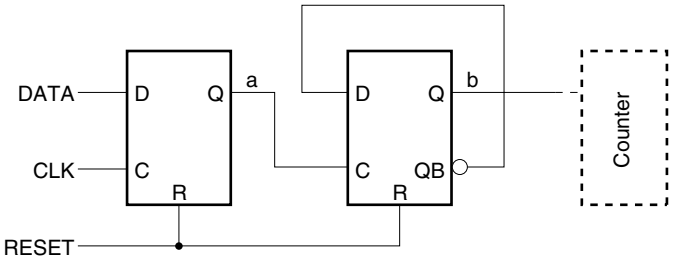
There is no problem even if $t_{PD0\ (MAX.)}$ is used in FXXX-type sequential circuits. Their respective values are listed in **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

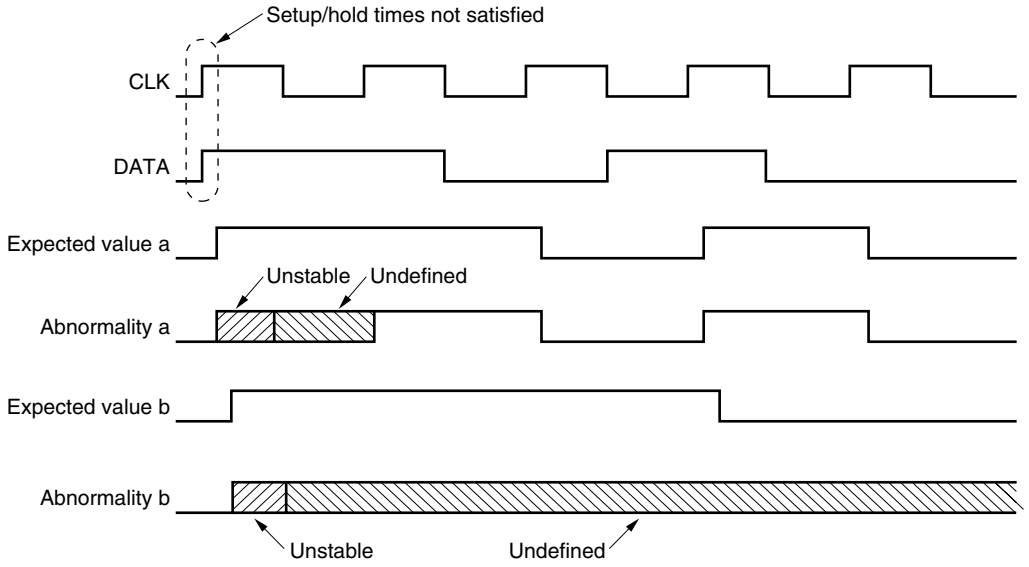
(2) Avoiding metastability

When the stipulated times cannot be satisfied (asynchronous input signals), take the following steps to avoid abnormalities.

Example of an abnormality

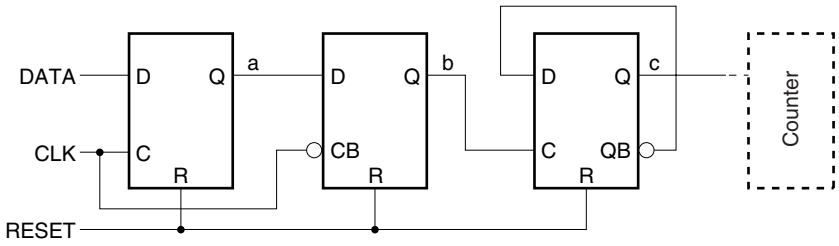
When the output from b in the figure below is input to the counter there is an excess number of counts.

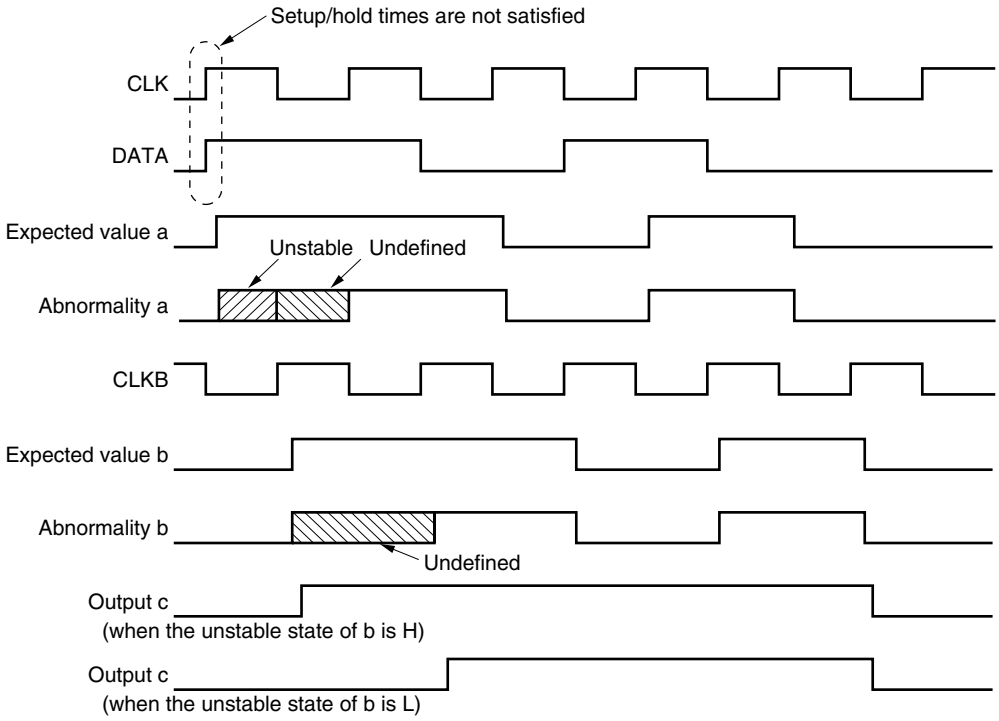




Example of avoiding abnormality

Output c is stable due to the insertion of a 1-step flip-flop. However, although the initial clock at c can have two values as a function of the instability of b, there is no effect on the counter in the following example.





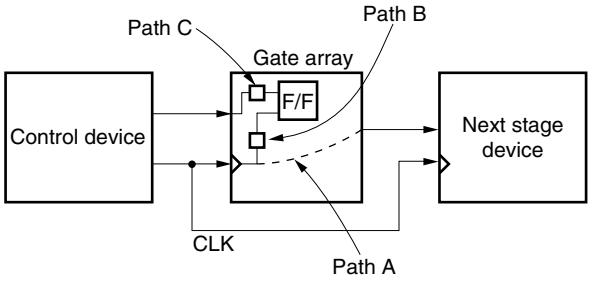
Remark Clock width > $t_{PD\ (MAX.)} \times 6 + (t_{su}$ or $t_h)$

5.6.6 Critical path guidelines

A critical path relates to the system timing contained in the gate array. It is a path that establishes the delay time for the gate array (see Figure 5-31). In this example, a detailed investigation of the path (the critical path) is necessary.

- Path A: Is the timing of the device in the next stage satisfied for gate array output sampling by the clock?
- Path B, C: Is the sampling timing satisfied in the gate array by the controlling device's output timing?

Figure 5-31. System with Critical Path



The following are the three types of critical paths:

<1> Input to output
<2> Input to input
<3> Output to output

The inspection and specification methods for these critical paths are explained in the following sections.

(1) Calculating and designing a critical path

As described in **4.4.3 Estimating wiring capacitance**, placement and routing are executed by determining the placement range for each macro hierarchy (first hierarchy only). Consequently, the intra-macro and inter-macro wiring lengths differ significantly. The following points must be noted when the propagation delay time of the critical path is estimated using the assumed wiring capacitance listed in Table 4-9.

<1> The critical path can be terminated in one macro hierarchy (first hierarchy) (excluding the I/O buffer).
<2> The load connected to the path can be reduced by making the critical path as simple as possible (limiting the fan-out value to 1/3).
<3> Except as given above, the input and output pins should be placed as close together as possible in regard to critical paths from the input to output pins.
<4> Circuits other than critical paths should not be included within macro hierarchies.

(2) Critical path between input and output

Path A in the circuit example of Figure 5-31 is not influenced by the other inputs. The maximum t_{PD} value is designed to be smaller than that required by the system.

In addition, keep in mind the large dependency of the output buffer's propagation delay time on the external load capacitance (C_L).

Calculation equation:

$t_{PD\ (MAX.)}$ < System specification value

(3) Critical path between two inputs

We will look at calculations for the circuit in Figure 5-32 by studying the input sampling timing. In inspecting this timing, we are assuming the input signal timing shown in Figure 5-33 since the relative timing specifications between the input pins must be well-defined in order to make the calculation.

Figure 5-32. Example of Input-Input Critical Path

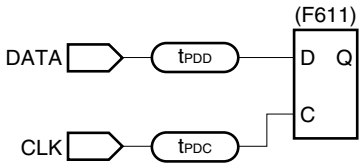
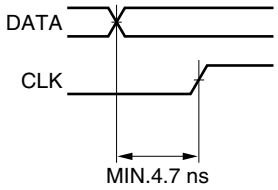


Figure 5-33. Inspection of Setup Time



The following points must be taken into consideration with respect to the conditions used:

- Absolute distribution is in the direction of the smaller margin
- Relative distribution is in the direction of the largest t_{PDD} and the smallest t_{PDC}

The method for making these decisions is shown below.

Calculation equations:

DATA is assumed to be a time differential of 4.7 ns (MIN.) from the clock, as shown in Figure 5-33.

$$t_{PDC\ (MIN.)} - t_{PDD}\ [MIN.\ (max.)] + 4.7 > t_{SU}$$

$$\rightarrow t_{PDC\ (MIN.)} - t_{PDD\ (MIN.)} \times \frac{1+\alpha}{1-\alpha} + 4.7 > t_{SU}$$

where:

α: Distribution coefficient (0.1)

5.6.7 Ensuring operating margin

When the operating margin of a circuit is found to be insufficient from the results of a delay margin check and a critical path check, there are several things that can be done, depending on the circuit configuration.

Generally, the following methods are taken.

<1> Reassess input and output specifications

- Decrease the input $f_{MAX.}$ and lower the input $f_{MAX.}$ duty distribution
- Relax the input and output timing and decrease the output capacitive load

<2> Reassess pin placement

- Shorten the wiring length to decrease the delay between input and output (adjacent placement of pins)

<3> Modify the circuit

- Decrease delay time by simplifying the circuit
- Decrease delay time by decreasing the load on the circuit
- Obtain the margin by inserting a delay gate

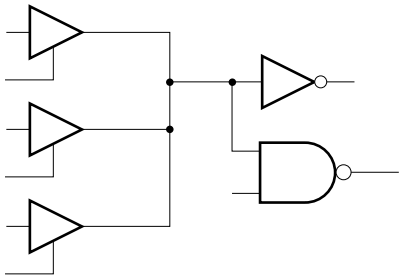
Delay calculations (or recalculations) are necessary when modifying a circuit, so, in particular, estimate the inserted gate output wiring length as 0 mm in regard to delay gate insertion.

5.7 Internal Bus Configuration

5.7.1 Configuring internal bus

Typical data selection techniques include the data selector format and the bus format. The circuit configuration of a selector (multiplexer) can become very complex. On the other hand, the bus format is comparatively simpler than the circuit configuration so it is easier to understand. Further, the propagation delay time increases although there may not be an increase in the number of cells used. Therefore it is important to select the optimum circuit configuration.

Figure 5-34. Internal Bus Configuration

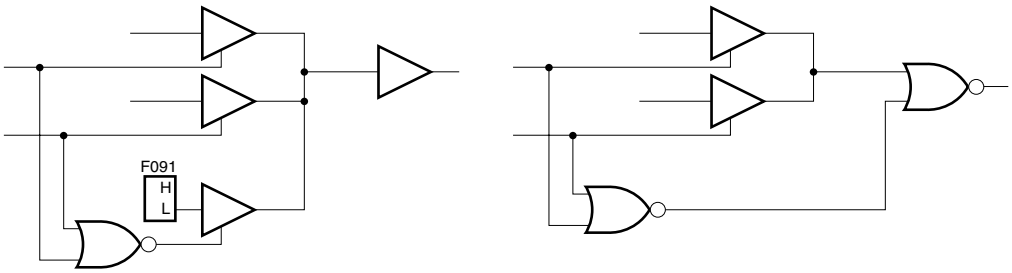


5.7.2 Preventing internal bus floating

As a basic rule when using an internal bus, a block configured on the same bus line should be in only one output enable state. This is necessary to avoid a floating state in the input of the next stage block. Examples of a good internal bus circuit configuration are shown in Figure 5-35.

Figure 5-35. Examples of Internal Bus Floating Prevention Circuit

(a) Example 1 **(b) Example 2**



5.7.3 Precautions

Although several connected blocks can operate on the same bus line when using an internal bus, the signal rise and fall times may increase due to an increase in wiring length and an increase in the fan-in loading of the previous block. Since problems such as operating stability and reliability may result, the following constraints must be observed. For further information, see **5.8 External Bus Contention**.

(1) Observe the bus constraints in the following formula:

$$F/O + N \leq 50$$
$$(1.4 \times F/O + 1.1 \times N + 1.9) \times f < 410$$

where:

F/O: Sum of the fan-in loading (F/I) of the gates connected to the bus
N: Sum of the three-state output buffers (F531, F532) connected to the bus
f: Operating frequency (MHz) of the bus

Contact NEC Electronics when you wish to use a device under conditions that exceed the above restrictions.

(2) Basically, the following states are prohibited for the bus line.

(a) More than two outputs are enabled on the same bus line.
(b) All outputs are disabled on the same bus line.

Consider enable-signal skew such as that which occurs when the signals converge, even though the conditions lie within the 20 ns maximum.

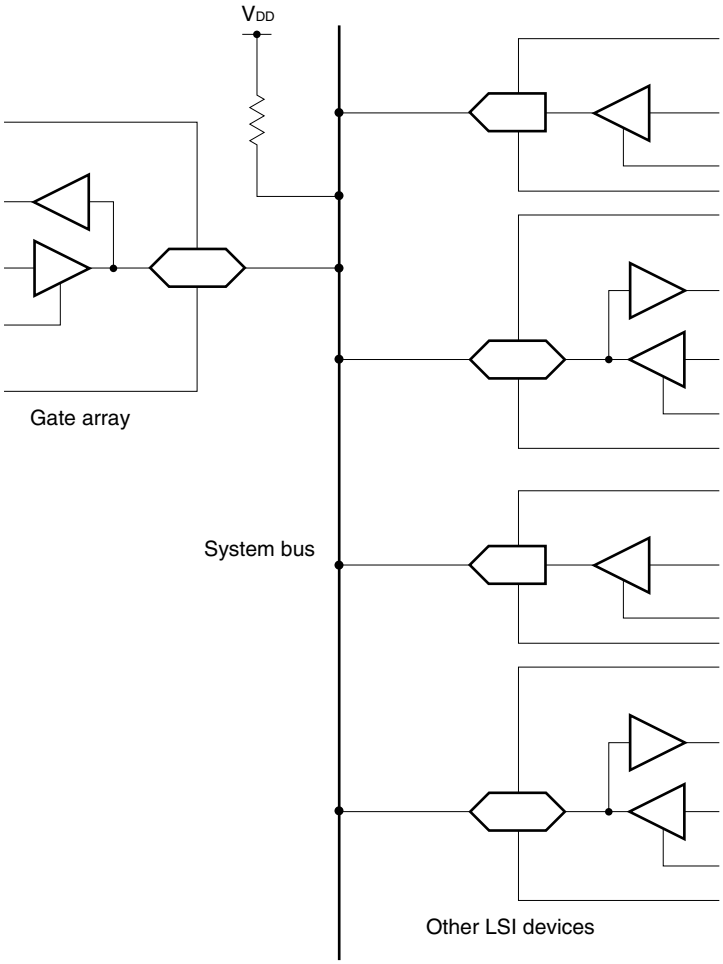
5.8 External Bus Contention

In addition to the explanation in **5.7.3 Precautions**, bus contention and float should be noted when connecting to a bus in a system that uses gate arrays and other LSIs.

Take measures with timing design and pull-up/pull-down resistors in order to avoid these problems.

In addition, in order to avoid external bus floating, there are I/O blocks with pull-up and pull-down resistors. For further information, see **CHAPTER 7 MULTIFUNCTION BLOCKS**.

Figure 5-36. External Bus Floating Prevention Countermeasure



5.9 Testability

There is more than just logic design when designing a gate array. Test circuits are also necessary. Consider the points shown below when designing the circuit and when making a test pattern. For more information, see **CHAPTER 6 TEST PATTERN GENERATION**.

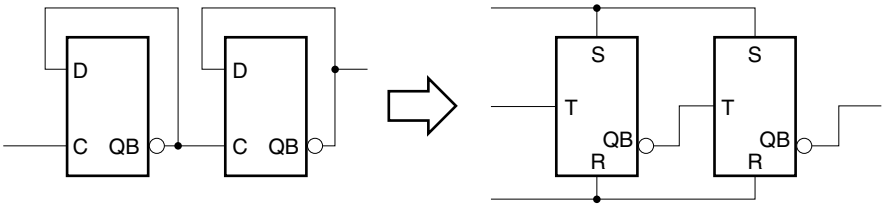
- Flip-flop initialization
- Division of counters
- Addition of test pins
- Division (modularization) of internal circuits by test pins

5.9.1 Flip-flop initialization

When the device is powered up, it is not known whether the output state of a block, such as a flip-flop or counter, is high level or low level. Consequently, initialization must be performed during the first few patterns when simulating.

In the design stage, the circuit should be configured so that an initialization pattern is not too long, and blocks with reset inputs should be used as much as possible so that the initial state of the internal circuit can be reset to a known state.

Figure 5-37. Initializing Flip-Flops

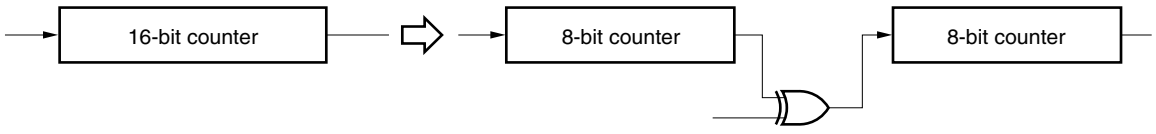


5.9.2 Division of counters

With multibit counters, the effective test method is to divide the counters to reduce the number of test patterns.

For example, the number of pulses necessary until the final stage of a 16-bit counter operates is 2^{16} pulses. By dividing the 16-bit counter into two 8-bit counters as shown in Figure 5-38, however, the number of pulses can be cut by 1/100 to 1/200.

Figure 5-38. Dividing Counters



5.9.3 Adding test pins and dividing circuits

As explained in **5.9.2 Division of counters**, there are cases where the number of test patterns increases even when the LSI test is simplified. This is done rather than setting up test pins in multibit counters and large-scale macros so that an operating mode can be externally operated.

(1) A test mode is specially set up when operation is divided into several modes. This is an effective technique for establishing the test-mode pins (test pins).

(2) With large-scale circuits, the several macros (modules) are divided. In this case, test pins are specially set up for partitioning the modules. This is an effective technique for testing LSIs in a partitioned condition.

5.10 Signal Racing and Spike Noise

5.10.1 Signal racing (contention)

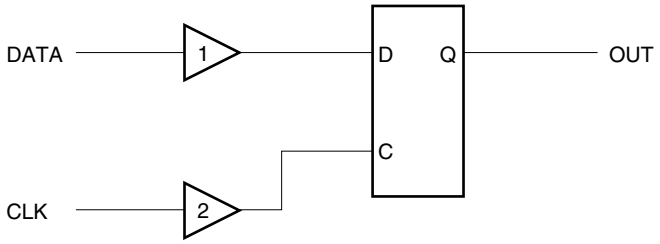
The condition where the timing changes when there are more than two input signals in a logic block is called racing.

If the test pattern shown in Figure 5-39 (b) is added to a circuit such as that in Figure 5-39 (a), a shift in flip-flop data and clock timing occurs due to the difference between the two delays in buffer 1, 2 and the wiring delay difference. The result of this is that the expected operation does not occur.

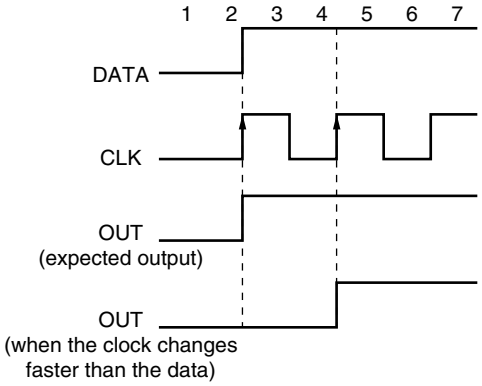
In the case of Figure 5-39 (a), data is first set in the flip-flop, making it necessary to consider a change in the clock. The test pattern for this is shown in Figure 5-39 (c).

Figure 5-39. Racing

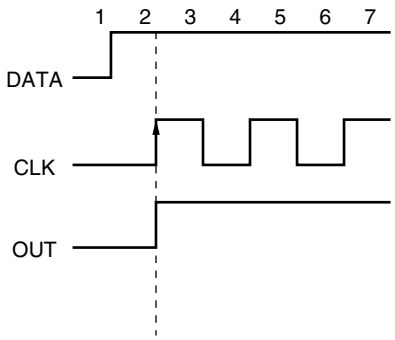
(a) Circuit with potential for racing



(b) Test patterns with potential for racing



(c) Test patterns that do not cause racing



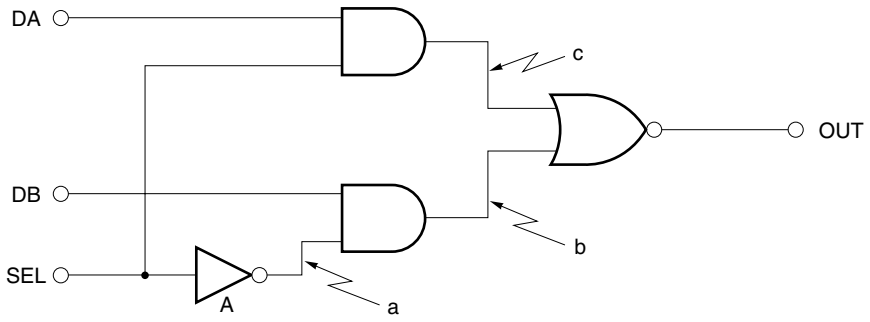
5.10.2 Spike noise

Spike noise is noise in a circuit that employs two or more gate inputs and is caused by a small input timing shift when the input signal timing changes. The time interval of this spike noise changes as a function of the size of the shift in timing. If the spike noise is input to the next-stage flip-flop block and the set/reset, the affected signal path related to the flip-flop's output signal can generate errors in operation.

Consequently, when gates with two or more inputs are used, it must be determined if an influence is exerted on the next-stage gates and the output signals by spikes generated by changes occurring when the multiple inputs change simultaneously. It must also be confirmed whether or not operating errors are occurring. If the spike noise cannot be observed in the following stage, it does not influence that stage, and the test pattern and circuit need not be modified.

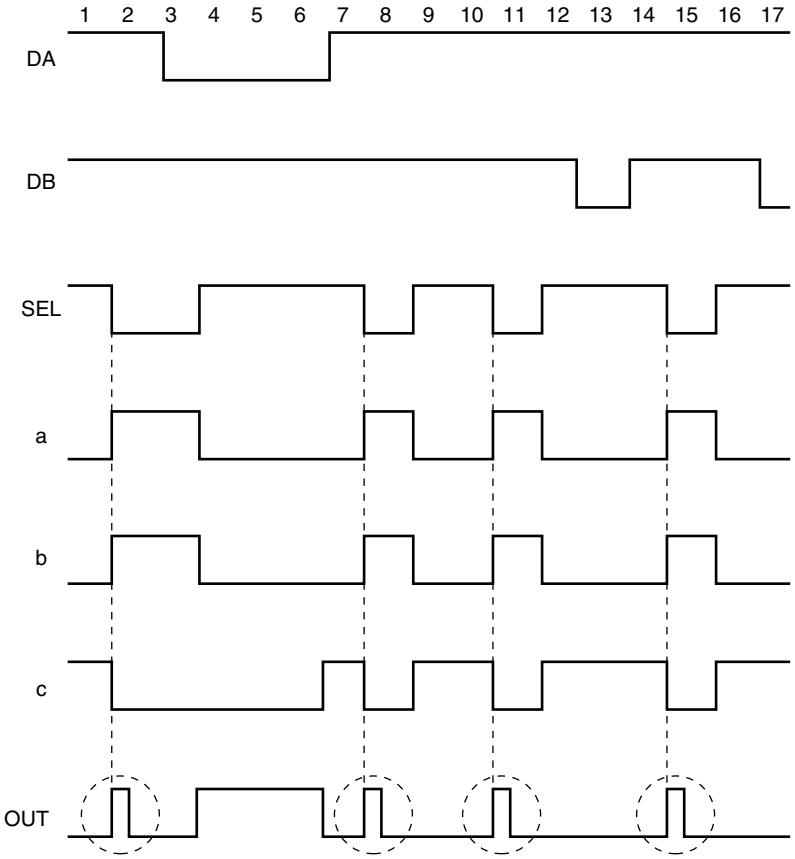
The following is an example of the generation of spike noise and measures that can be taken against it.

Figure 5-40. Data Selector Circuit



The AND-NOR data selector circuit shown in Figure 5-40 will generate the test pattern shown in Figure 5-41.

Figure 5-41. Test Pattern Example (Before Improvement)



In this case, when both the DA and DB input data signals are in a high-level state, spike noise is generated at the OUT (output signal) since the SEL (select signal) changes from H to L. The pattern in Figure 5-41 generates spikes at pattern locations 2, 8, 11, and 15.

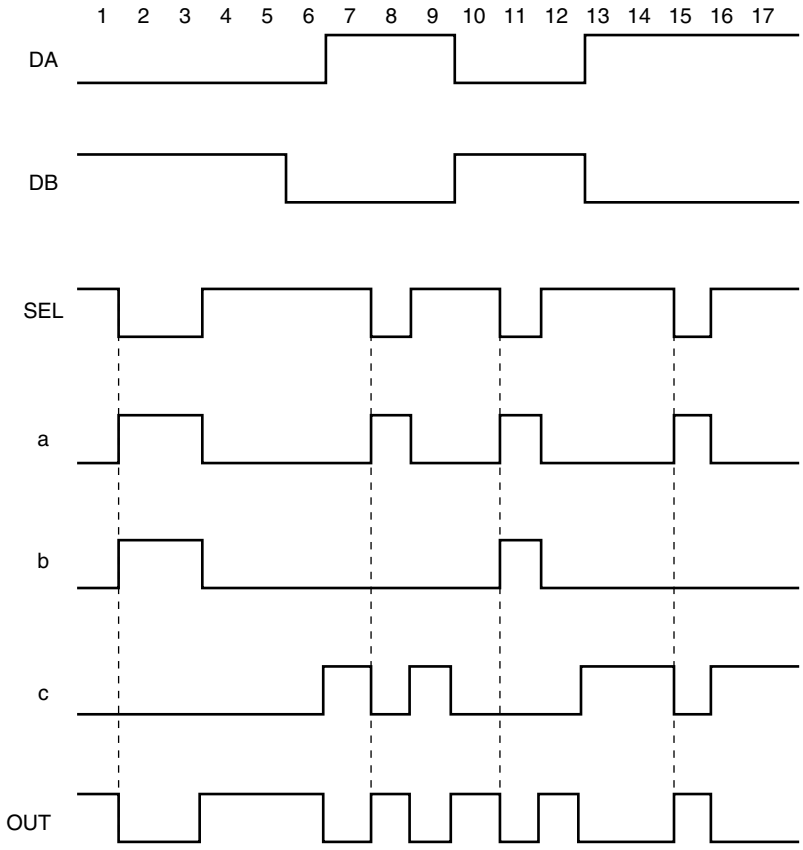
As is clear from the circuit diagram, when DA and DB are in the high-level state, the state of b and c are determined by the state of SEL. In addition, when SEL changes from H to L, b changes from L to H and c changes from H to L in the same pattern. Moreover, a changes when it goes through inverter A and the delay through A is greater than that of SEL. Because of this, b is delayed more than c. Consequently, the state of b and c are simultaneously L and L at 2, 8, 11, and 15 of the test pattern, and L-to-H-to-L spike noise is generated for OUT.

Consider the following two measures if this spike noise is input to the flip-flop clock or the set/reset.

<1> Design so that data is not changed, i.e. the output of flip-flops are not changed, due to spike noise at the timing where spike noise occurs.
<2> Modify the test pattern.

In the case of this example, when SEL changes from H to L, make at least one of DA and DB change to L. There is no spike noise at the OUT if the timing is designed as shown in Figure 5-42.

Figure 5-42. Test Pattern Example (After Improvement)

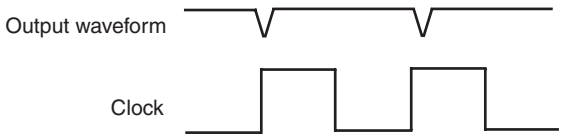


5.11 Output Waveform Noise

The DC characteristics of the low or high level of the output voltage are as described in **CHAPTER 3 PRODUCT SPECIFICATIONS**; however, noise may occur in the output waveform due to charge and discharge currents of the internal circuit operation.

To minimize the noise in the output waveform, externally add a smoothing bypass capacitor.

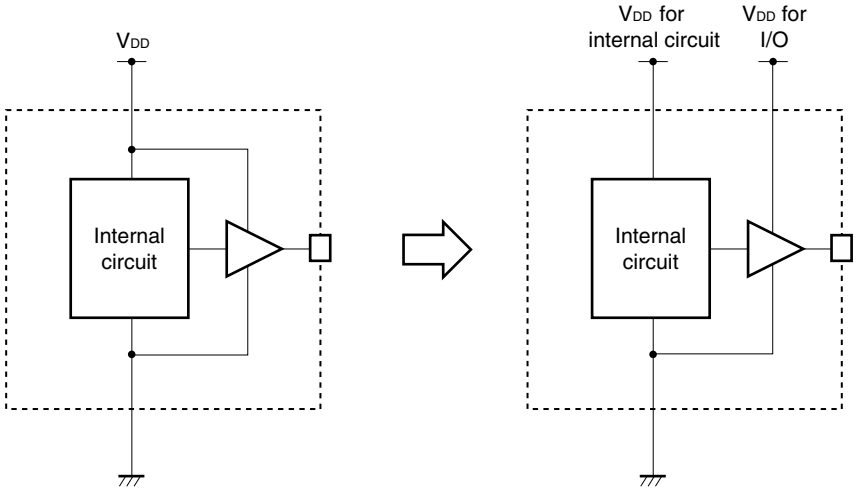
Figure 5-43. Output Waveform Noise



To completely suppress the noise in the output waveform, separate the power supply to V_{DD} for the internal circuit and V_{DD} for I/O.

The separation of the power supply is supported by CMOS-10HD 2-power supply products and EA-9HD 2-power supply products.

Figure 5-44. Power Supply Separation



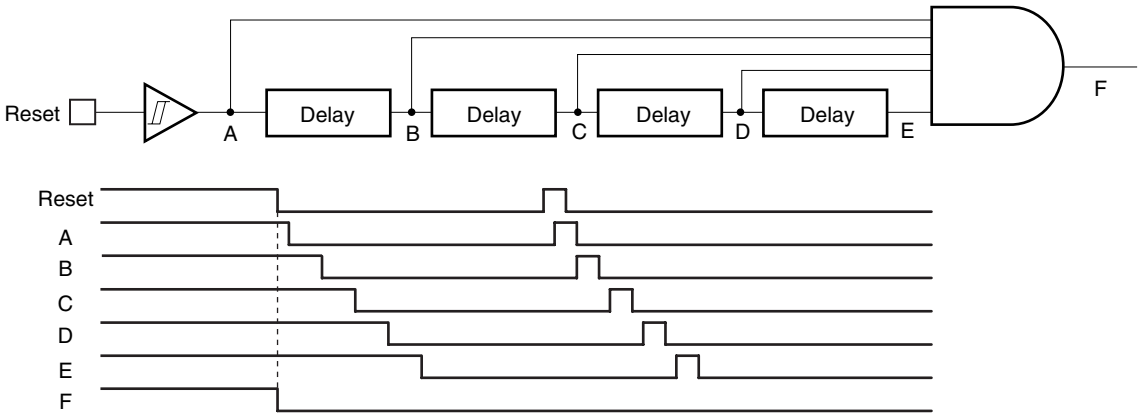
5.12 Reset Pin

Handle the reset pin as follows in order to prevent a reset operation from occurring when the input level changes momentarily due to noise.

(1) Use as a Schmitt input buffer.

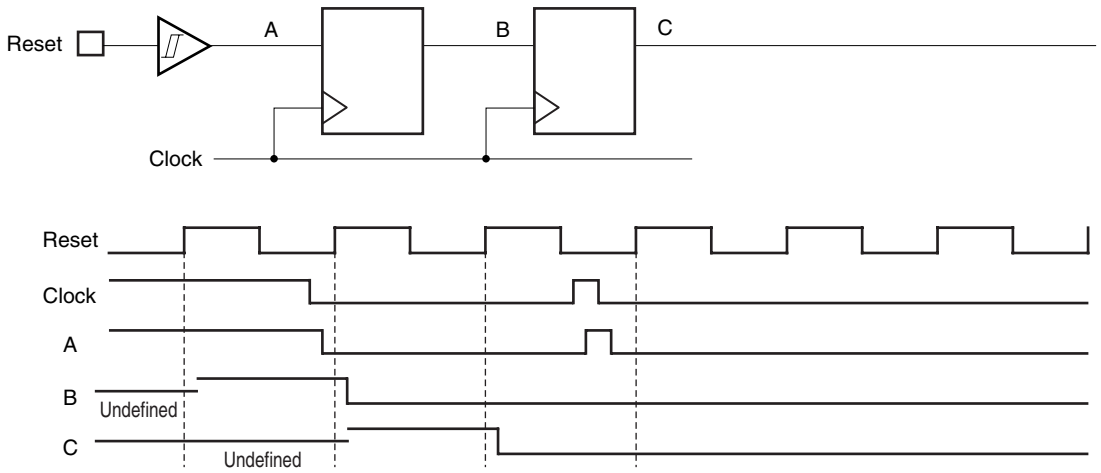
(2) Insert a filter circuit that eliminates momentary pulses.
Figures 5-45 and 5-46 show examples of countermeasure circuits used when a reset (active high) occurs.

Figure 5-45. Countermeasure Circuit Example 1



The countermeasure circuit in Figure 5-45 prevents a reset from being activated by a pulse, after a reset has been released.
The reset circuit is released, depending on the input reset.
This circuit is a differential circuit and requires caution regarding the layout. When using the circuit, contact NEC Electronics, because group placement and forcible placement may be required during layout.

Figure 5-46. Countermeasure Circuit Example 2



The countermeasure circuit in Figure 5-46 is configured of two F/F stages, in order to handle metastability that is caused by a conflict between a reset and the clock.

CHAPTER 6 TEST PATTERN GENERATION

When designing with gate arrays, the circuit's expected function and performance are verified through simulation on a computer. To execute the simulation, the user is requested to prepare a circuit diagram and test patterns.

These test patterns are also used for product inspection before shipment. During shipment inspection, the functions of the LSI are verified (test function) and the DC characteristics (such as power supply leakage current, input leakage current, and output current) are tested. Unless adequate consideration is given to the shipment inspection, therefore, the product is not thoroughly tested when shipped. Therefore, create test patterns with which fault detection and DC testing can be performed.

During simulation, the conditions under which the LSI is actually used by the user can be realized relatively easily. The LSI tester, which tests the actual LSI, however, cannot completely reproduce the conditions under which the user actually uses the LSI, in many cases. Therefore, create the test patterns in accordance with the capability of the LSI tester and by observing specified limits.

This chapter describes the points to be noted when creating test patterns.

6.1 Test Pattern Types

The types of test patterns available are shown in Table 6-1.

One DC test pattern is essential, but other test patterns may also be necessary depending on circuit or user requirements. When the LSI tester is used to perform DC measurement, the measurement is carried out using up to the first 32,000 patterns of the DC test pattern.

Table 6-1. Test Pattern Types

Pattern Name	Purpose	Pattern Creator
DC test pattern	DC measurement, logic verification	User
Function test pattern	Logic verification	User
High-speed function test pattern	Logic verification (real time)	User
Megamacro initialization pattern	Initialization	NEC Electronics (inserted by user)
Megamacro single-unit test setting pattern	Setting megamacro peripheral values	User
Megamacro test pattern	Logic verification (megamacro single unit)	NEC Electronics
Scan test pattern	Fault detection	User or NEC Electronics
RAM test pattern	Logic verification (RAM single unit)	NEC Electronics
Digital PLL initialization pattern	Initialization	User
Boundary scan test pattern	Logic verification (boundary scan circuit)	User

Although the pattern length per pattern is not restricted (except for the high-speed function test), the total pattern length is. For details, refer to **6.2.2 Limitations on test pattern length**.

6.2 Notes from Viewpoint of Product Test (LSI Tester)

6.2.1 I/O pin naming conventions

(1) Maximum number of characters for I/O pins

64 characters MAX.

(2) Characters allowed

Some characters must not be used when specifying a pin name. The characters that can be used are listed in the table below.

Table 6-2. Restrictions on Pin Names

Usable characters	Alphabetic uppercase letters Numeric characters “_” (underscore)
Unusable characters	“ / ” (slash) and all other special characters other than the underscore Alphabetic lowercase letters

6.2.2 Limitations on test pattern length

The length of a test pattern is limited by the size of the LSI tester’s memory.

The minimum and maximum lengths of test patterns (for DC test and for the function test) are listed in Table 6-3.

Table 6-3. Limitations on Number of Test Patterns

Number of Patterns / Package[Note 1]	Minimum Number of Test Patterns (Applicable to DC Test Patterns)	Maximum Number of Test Patterns[Note 2]
144 pins or less: with SCAN	150 patterns	128 K patterns
144 pins or less: without SCAN		256 K patterns
145 pins or more		512 K patterns

Note 1. The number of package pins includes the number of power supply pins (GND, V_{DD}, etc.).

Note 2. The maximum length of test pattern does not need to be considered for the RAM test pattern, scan test pattern created by NEC Electronics, and high-speed function test pattern.

Examine each length of test pattern for the user-created test pattern and megamacro boundary scan, taking the limited pattern length above into consideration.

6.2.3 Number of test patterns

There can be more than one test pattern. The maximum number of patterns is 20, including all interface test patterns such as those for DC test and function test. In this case, the RAM test pattern, scan test pattern created by NEC Electronics, and high-speed function test pattern do not need to be considered.

However, the number of test patterns should be minimized as far as possible in order to increase efficiency. Even if the test pattern is divided for the sake of convenience of design, in principle, submit one test pattern to NEC Electronics (the test patterns can be easily combined by using the wave editor of the pattern utility or OPENCAD).

To divide the test pattern, initialize each pattern (see **6.3.1 Initializing circuit**). If this is not possible, be sure to inform NEC Electronics of the sequence of the test patterns (in writing).

The test pattern must be divided in the following cases.

- If the time conditions (input delay and pulse width) and output judge time (strobe time) of the input signals differ
  For details, see **6.3 Notes on Creating Test Pattern for Function Test**.

6.3 Notes on Creating Test Pattern for Function Test

6.3.1 Initializing circuit

Whether the output state of blocks, such as flip-flops and counters, is at the high level or low level immediately after power application is unknown (see **5.9.1 Flip-flop initialization**). Consequently, the initial status of sequential circuits such as flip-flops and counters is “x” (undefined) during simulation. To verify operation of the circuit, it is necessary to change the internal function block state from an indeterminate state to a determinate state (circuit initialization).

When designing a circuit, prepare a pattern that can initialize the circuit at the beginning of the test pattern, and at the same time, consider use of a reset pin, so that the circuit can be easily initialized.

When preparing divided test patterns, in principle, initialization is necessary for each pattern (see **Figure 6-4 Test Pattern Example**).

6.3.2 Test cycle (test rate)

The test rate is referred to as the cycle of one test pattern.

Currently, the test cycle limitation at NEC Electronics for a general function test is as follows:

Test cycle: 200 ns

If a higher-speed test cycle than above is desired, perform the high-speed function test. For the high-speed function test pattern, refer to **6.6 High-Speed Function Test (Real-Time Test)**.

6.3.3 Output determination time (strobe time)

The output determination time (strobe time) refers to the time during which the output value of the product is referenced with the expected value on the test pattern. In the current normal function test pattern, this time is always the final time (199.99 ns) of the period, and anything outside of this becomes a high-speed function.

For details of the high-speed function test pattern, see **6.6 High-Speed Function Test (Real-Time Test)**.

6.3.4 Specification of timing phase

For the specification of timing phases currently supported, refer to Table 6-4 (including the basic timing).

The skew among the pins of the LSI tester (specified as ±5 ns) must be considered, and the time differential of each phase must be set to 10 ns or greater.

The basic timing phase indicates the NRZ signal when Δt_D = 0 ns. NRZ signals with an equal delay time (Δt_D) are considered as in-phase and counted as one phase no matter how many input pins there are with the same timing.

Likewise, RZ signals with an equal delay time (Δt_D) and pulse width (Δt_W) are also considered as in phase.

Positive clocks and negative clocks with an equal Δt_D and Δt_W are also counted as one phase. However, NRZ signals and RZ signals with an equal Δt_D are in-phase.

Table 6-4. Timing Phase Number

PKG	Timing Phase Number[Note]
All packages	6

Note Including basic timing phases.

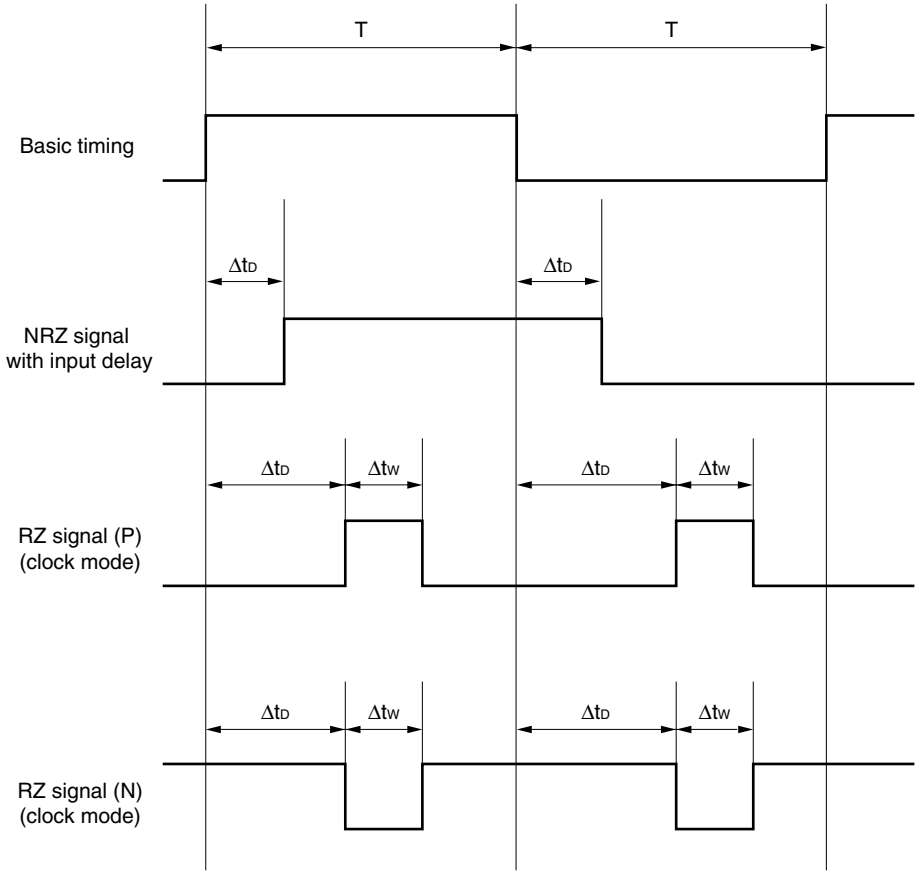
Table 6-5. Timing Constraints

Timing Limit / Signal Type	Input Delay (Δt_D)		Input Pulse Width (Δt_W)	
	MIN.	MAX.	MIN.	MAX.
Basic timing	0 ns		–	
NRZ signal	10 ns	T – 10 ns	–	
RZ signal (clock mode)	10 ns	T – Δt_W – 10 ns	145 pins or more: 10 ns 144 pins or less: 15 ns	T – Δt_D – 15 ns

Remark 1. NRZ (No Return to Zero) signal: Indicates there is only one change within one test pattern (1 test rate).

Remark 2. RZ (Return to Zero) signal: A signal with a change of 0 → 1 → 0 or 1 → 0 → 1 within one test pattern.

Figure 6-1. Timing Phase



Caution 1. At least 10 ns must remain between changes of each signal.

Caution 2. RZ signal input to bidirectional pins is prohibited.

Remark T: Test cycle (test rate)

The clock mode (RZ) signal of the input has two polarities, which determine how it is used.

Table 6-6. Clock Mode

Input Pattern	Definition	Operation	
		Positive Clock (P)	Negative Clock (N)
1 (H)	Clock generation	0 → 1 → 0 (positive clock generation)	1 → 0 → 1 (negative clock generation)
0 (L)	Clock stop	0 hold	1 hold

6.3.5 Skew

When two or more input signals are changed at the same time during simulation, no skew occurs between input signals. With an LSI tester that is used to check the quality of products, however, the input signals do not change at exactly the same time because of a skew of several ns that exists between input pins, even if it is specified that the signals change at the same time. Consequently, even if no problem is found during simulation, the product may not pass a quality test because of the skew between pins.

Therefore, take the following measures so that the product will operate normally even if there is an input skew when creating a test pattern.

(1) Do not change a flip-flop's data input and clock at the same time

→ Instead, alternate by one pattern.

(2) Use a clock signal (RZ signal) and an input delay signal (NRZ signal).

→ Stagger the input.

If it is assumed that the input skew is 10 ns and the setup time between data and clocks is 5 ns, then a 15 ns delay time is needed, as shown below.

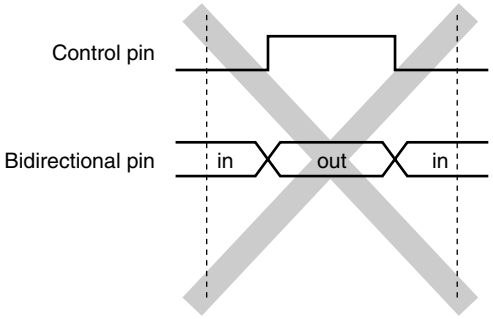
LSI tester input skew	+	Setup time	=	Input delay time specified to clock signal
10 ns	+	5 ns	=	15 ns

6.3.6 Notes on switching I/O mode of bidirectional pin

(1) Although the switching of the bidirectional pins' I/O mode is generally carried out at the basic timing, for the DC test pattern and function test pattern, it is possible to shift the I/O switch timing of a single set. This is known as the I/O modulation function (refer to **6.3.7 I/O modulation function** for details).

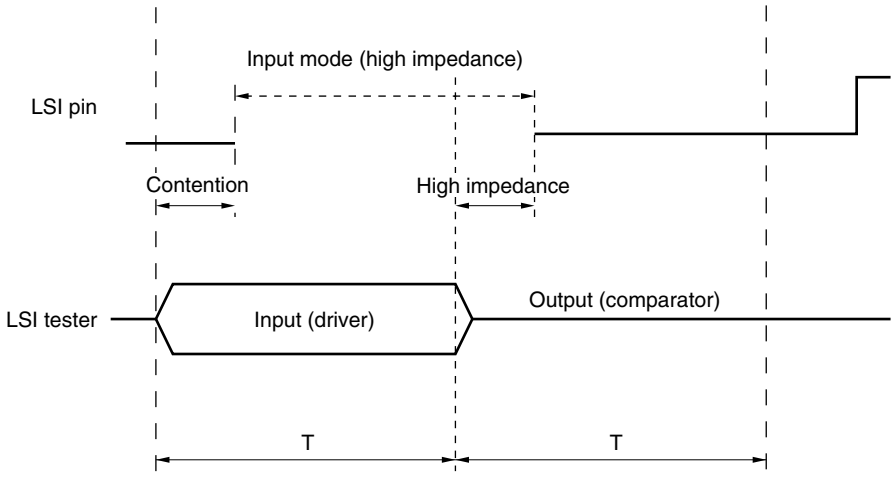
Note, however, that the bidirectional pin I/O mode cannot be switched using the RZ signal (because the mode will change twice within 1 rate: input → output → input. See **Figure 6-2**.)

Figure 6-2. Example of Incorrect Bidirectional Pin Switch Timing



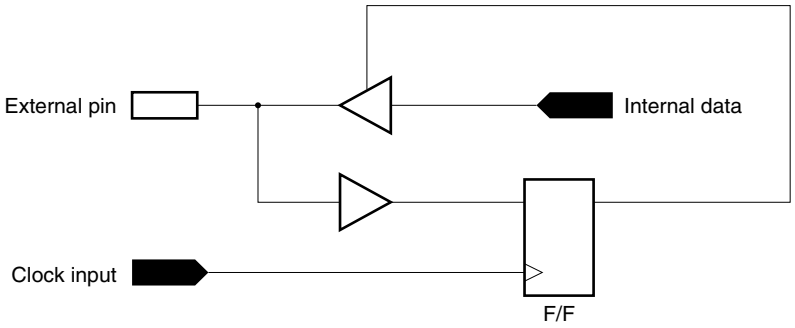
(2) In cases when an input delay has been added to the control pin in the bidirectional pin I/O mode, or when the I/O mode switch timing is different to the basic timing because there is a delay until the internal circuit is enabled, ensure that the input and output values match when switching the I/O mode. This processing prevents a current from flowing when the device's output signal conflicts with the LSI tester's driver (input), and is used to avoid power supply modulation or other such causes of malfunction. If it is not possible to match the input and output values, ensure that the conflict does not exceed 20 ns (see **6.3.8 I/O conflict**).
Note that it is prohibited to input the RZ signal (clock waveform) to a bidirectional pin.

Figure 6-3. Contention During Input/Output Switching



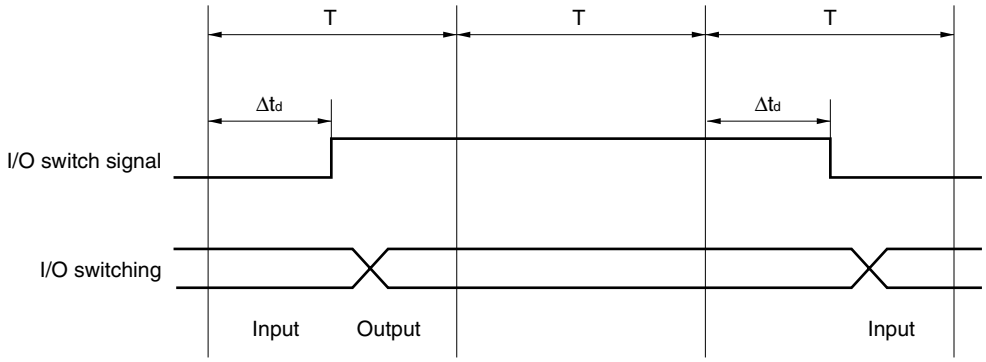
Remark T: Pattern period

(3) In cases when due to the circuit specifications of PCI bus circuits, etc. the I/O mode switch timing differs from the basic timing, and the bidirectional mode is switched after the pre-switching value is fetched inside the circuit, use the I/O modulation function (refer to **6.3.7 I/O modulation function** for details).



6.3.7 I/O modulation function

Although in the case of the DC test pattern and function test pattern it is possible to shift the I/O switch timing of a single set, the following restrictions apply.



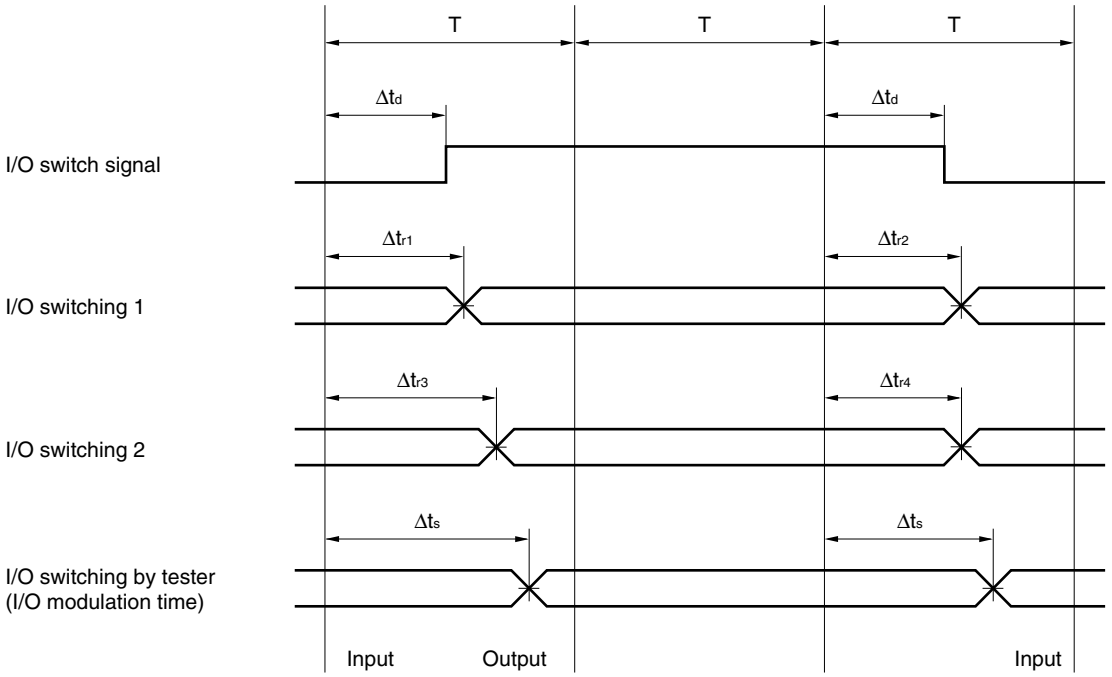
Remark T: Pattern period
Δt_d: Input delay of I/O switch signal

When shifting the I/O switch timing from the basic timing, the I/O switch time on the tester side is set as the I/O modulation.

The following expression must be satisfied, assuming Δt_{rmax} is the slowest time of all the pins and patterns among the bidirectional pin (simulation result) I/O switch times, and Δt_s is the I/O modulation time.

$$\Delta t_s \geq \Delta t_{rmax} + 5 \text{ ns}$$

The reason for this is that in cases when the bidirectional mode is switched after the pre-switching value is fetched inside circuits such as a PCI bus circuit, because it is necessary to hold the external (LSI tester) value until the pin's I/O mode has been switched, the circuit must be driven longer (I/O mode switching delayed longer) than in the simulation result: 5 ns of the skew between the LSI tester pins.



Remark T: Pattern period

Δt_d: Input delay of I/O switch signal

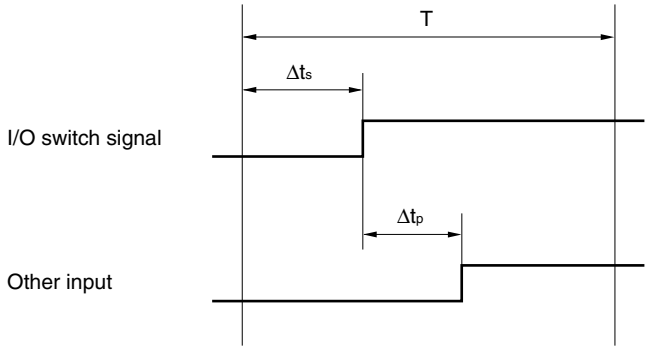
Δt_{r1} to Δt_{r4}: Bidirectional pins' I/O switch times

(Δt_{r3} in the above figure corresponds to Δt_{rmax} in the aforementioned equation.)

Δt_s: I/O modulation (I/O switching on the tester side) time

In addition to satisfying the above conditions, the following restrictions must be observed.

Item	I/O Modulation (Δt_s)		Interval Between I/O Modulation and Other Input Delay (Δt_p)
	MIN.	MAX.	MIN.
Restriction	10 ns	T – 10 ns	10 ns



When setting both the input delay (Δt_d) and I/O modulation (Δt_s) for the same pin, ensure that either of the following is satisfied: $\Delta t_s = \Delta t_d$, or $\Delta t_s + 10\ ns \leq \Delta t_d$.

Note that the I/O conflict time must be kept within 20 ns, even when using the I/O modulation function.

6.3.8 I/O conflict

If it is not possible to match the bidirectional pins' input and output values, the I/O conflict must not exceed 20 ns. The reference for judging I/O conflict is shown below.

Simulation Result	Expected Value	
	Input	Mode Undefined
Output 1	0, X	0, X
Output 0	1, X	1, X
Output X	0, 1, X	0, 1, X, Z

6.3.9 Testing multifunction I/O circuits

(1) Oscillators

Oscillators cannot be actually oscillated and tested with a simulator and LSI tester. Input a dummy signal to the input pin of the oscillator.

Use the inverted signal of the input signal as the expected value of the output of the oscillator.

The oscillator input signal is equivalent to the clock signal. Because a stable test cannot be performed due to conflict if this input signal and external data or set/reset input signals are changed at the same timing, be sure to stagger the timing.

Because the test pattern is not modeled in an oscillating state, the external timing of data or reset signals related to the clock in an oscillating state (oscillator input signals) is not tested.

(2) Open-drain output

The expected output value in the case of output disable must be high impedance (Z).

6.4 Notes on Creating DC Test Patterns

Restrictions for DC test patterns are basically same as those for function test patterns. The test pattern is not only used to test the functions but also used to test DC characteristics during shipment inspection. Therefore, the following points must be noted in creating a test pattern.

<1> If possible, prepare a dedicated test pattern set for the DC test pattern.
<2> The length of the DC test pattern should be more than 150 patterns. If the length of the pattern exceeds 32,000, perform the DC test between 1st and 32000th pattern.
<3> If possible, make input pins change at least two times (except for oscillation stop control pin).
<4> Output pins must output a high level and a low level at least once each.
<5> The output pin of a three-state output buffer must output a high-impedance state (off state).
<6> When a bidirectional buffer is used, make sure that the input state and output state are switched at least once.
<7> The test cycle must be sufficiently longer than the delay time (operating time) of the circuit. The basic cycle is 200 ns. Be sure to set the output determination time (strobe time) towards the end of the cycle (this is so the output is determined after the circuit has entered the stable state).
<8> If an RZ (Return to Zero) signal is input to an input pin, make sure that the RZ signal is not output as is. The output value of the output pin that outputs the RZ signal is always either one of two values at output determination time, and the other value cannot be tested.
<9> Bus fighting and bus floating for the internal bus is prohibited.
<10> Initialize the circuit until 50th pattern.
<11> The IDDq test is performed in the DC measurement pattern. The measurement pattern is selected automatically. If possible, operate the internal circuit to improve coverage.
<12> Be sure to set to oscillation mode when an oscillator block is mounted.
<13> In the test pattern in oscillation mode, input the same pattern as normal clock pattern for the input pin (XT1) and expected value of output pin (XT2) should be its inverse.

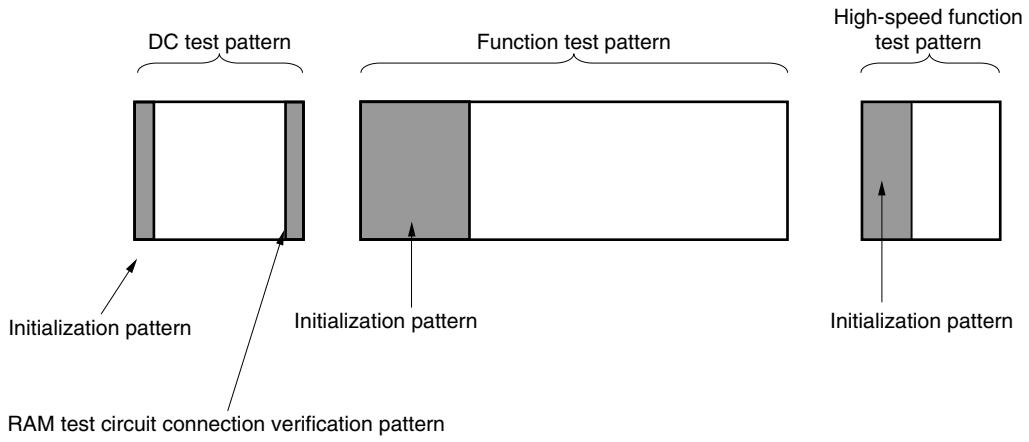
The RZ signal has changes of “0 → 1 → 0” and “1 → 0 → 1” in one test pattern (1 test rate). By contrast, the NRZ (No Return to Zero) signal has only one change in one test pattern (1 test rate).

6.5 Test Pattern for On-Chip RAM

NEC Electronics supplies a test pattern for RAM, and the user does not have to consider RAM tests. However, the following limitations are applied if NEC Electronics supplies the test pattern for RAM. (For details, see **7. 9 Memory**).

(1) Additional RAM pins (TIN, TEB, and TOUT) are needed in order to test the RAM.
(2) If there are multiple RAMs or connections between RAM and logic circuits, the connection to each RAM must be tested by the user test patterns.
(3) Be sure to set the TEB pin to user mode (high) for each of the user test patterns.

Figure 6-4. Test Pattern Example



6.6 High-Speed Function Test (Real-Time Test)

Checking the designed circuit through simulation at the actual operating frequency is a very effective technique for checking the actual operation of the LSI. In this way, problems concerning the timing of the circuit during actual operation that may have been overlooked by the designer can be found.

During the shipment inspection of the product, the actual operating conditions cannot be always simulated because the performance of the LSI tester may be limited. The high-speed function test, however, can simulate conditions very close to the actual operating conditions.

This section describes the following limits of the high-speed function test. Create a test pattern observing these limits.

6.6.1 Limitation of the test pattern length

The length per test pattern must consist of 32,000 patterns MAX.

6.6.2 Test cycle (test rate)

The test rate is referred to as the cycle of one test pattern.

Currently, the test cycle limitation at NEC Electronics for a general high-speed function test is as follows:

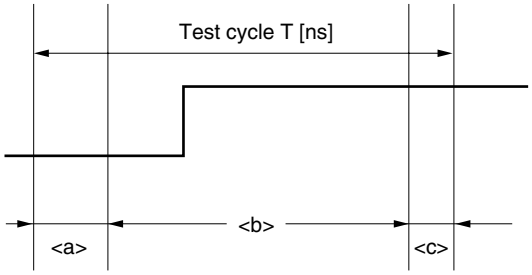
Test cycle: 50 ns MIN.

6.6.3 Output determination time (strobe time)

The output determination time (strobe time) indicates the time required to verify the output value of the product against the expected value on the test pattern. Currently, up to two strobe times can be assigned per test pattern. However, only one strobe time can be assigned per pin. If three or more strobe times or several strobe times per pin must be established, each one must have its own test pattern.

Setting strobe time within 15 ns the beginning of the basic timing or with 10 ns before the end of the timing is prohibited.

Figure 6-5. Strobe Time



<a> <b> <c>

15 ns ≤ strobe time ≤ T – 10 ns

Caution Open-drain, GTL+, and HSTL buffers are not real-time test targets.

6.6.4 Notes on high-speed function testing

To conduct the high-speed function test, execute MIN/MAX simulations under the following conditions. The results of both the simulations must match.

Confirm these simulations before and after placement and routing.

Note that I/O modulation cannot be used.

Ask NEC Electronics for the delay data (path delay file) after placement and routing.
At this time, the load capacitance data file (DIF FILE) for the output pins used for simulation is necessary.
Submit this file to NEC Electronics.
For the format of the DIF file, see **APPENDIX C ALBATROSS AND DIF FILE FORMATS**.

The purpose of these simulations is to detect the possibility of occurrence of problems when inspection is performed with an LSI tester. Therefore, conditions different from the actual operating conditions must sometimes be set.

Specify settings of the time condition for input signals, the output determination time (strobe time), and the test cycle (test rate) for each phase in “High-speed function test guidelines”.

<1> MAX. simulation conditions

Test cycle (T):	User-specified value
Load capacitance (C_L):	Bidirectional pin: 125 pF, MAX. value of load capacitance with LSI tester
	Output pin: 90 pF
Strobe time:	Set to specified value –5 ns with skew of strobe time assumed to be –5 ns

<2> MIN. simulation conditions

Test cycle (T):	User-specified value
Load capacitance (C_L):	50 pF, MIN. value of load capacitance with LSI tester
Strobe time:	Set to specified value +5 ns with skew of strobe time assumed to be +5 ns

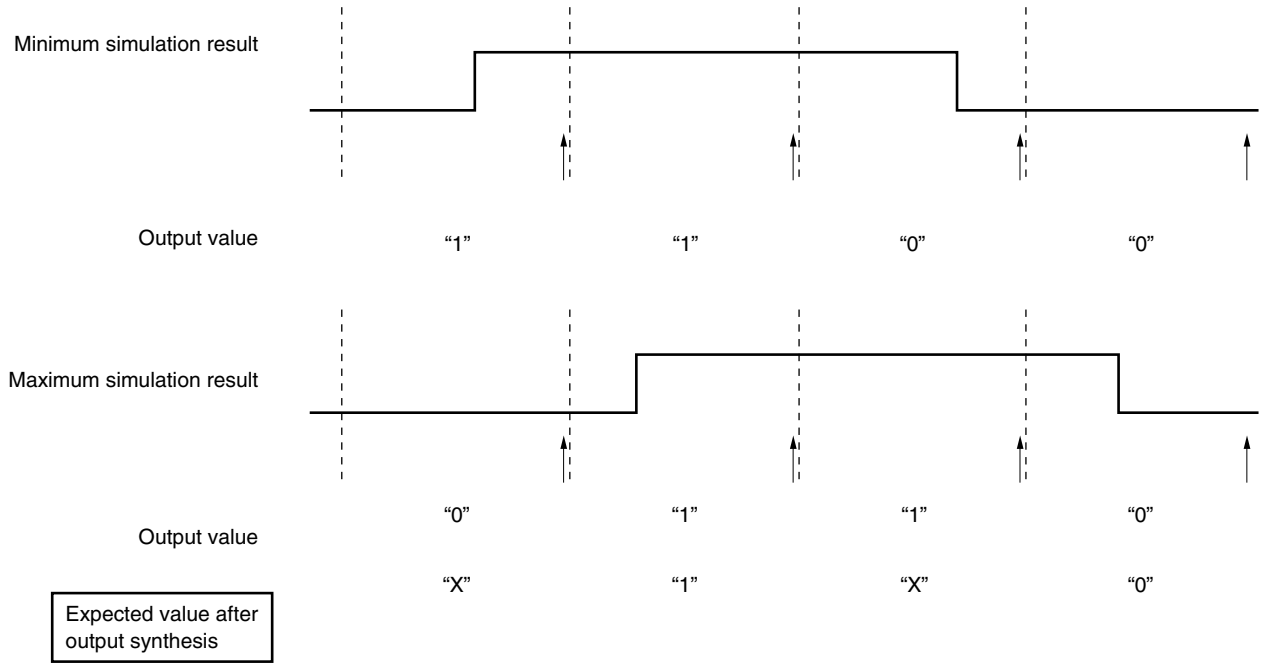
During real-time simulation, the simulation result may not converge in one pattern and the output may change at the next pattern, as shown in Figure 6-6.

If the simulation result is different between the MAX simulation and MIN simulation, take the following measures:

- Change the expected output value of the test pattern, which differs between the two test patterns, to “X” (Don’t care).

  Synthesize the test patterns (see **Figure 6-6**).
- Alternatively, include only the timing actually requiring inspection as the system, as the expected values.

Figure 6-6. Real-Time Simulation Results



6.7 Testability (Fault Coverage)

6.7.1 Consideration of testability (fault coverage)

Fault simulation is a way to verify the testability (fault coverage) when an ASIC is developed. In other words, it diagnoses the validity of a test pattern created to test the functions of logic circuits and detects the faults that are not detected by that test pattern.

During the ASIC manufacturing process, various faults may arise. These faults are broadly classified into dynamic faults and static faults.

Dynamic faults create long delay paths, spikes, and timing violations. Such faults are caused by the operating environment or design errors.

Static faults are represented by physical damage to the chip such as routing shorts and opens. In most of the cases, the production process is responsible for these faults. Logic simulation verifies the functions and timing of a created circuit. However, it does not verify the test efficiency of a test pattern for detecting static faults in the chip actually produced. Fault simulation defines static faults in the circuit and verifies whether faults have been accurately detected by the input test pattern from the output pins of the ASIC developed.

The purpose of fault simulation is to inspect how efficiently test patterns can detect a fault at the boundary of the function blocks of the created circuit. The test efficiency of these test patterns is called testability (fault coverage) and is expressed as a percentage to indicate how well the test patterns can detect the faults in the circuit.

$$\text{Testability (fault coverage)} = \frac{\text{Number of faults detectable by given test input pattern}}{\text{Total number of faults in circuit tested}} \times 100\ (\%)$$

If the testability (fault coverage) is low, the LSI may not be tested well and defective products may be shipped.

NEC Electronics recommends that the fault coverage, as far as possible, be made at least 90% in order to raise the quality of the product.

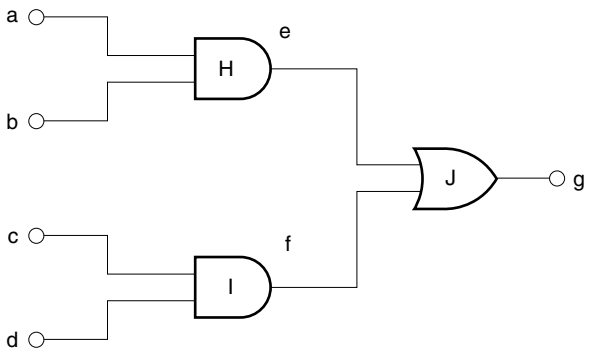
To improve testability (fault coverage), it is recommended to provide a test circuit at the circuit design stage and to employ the scan path test method.

6.7.2 Principle of fault simulation

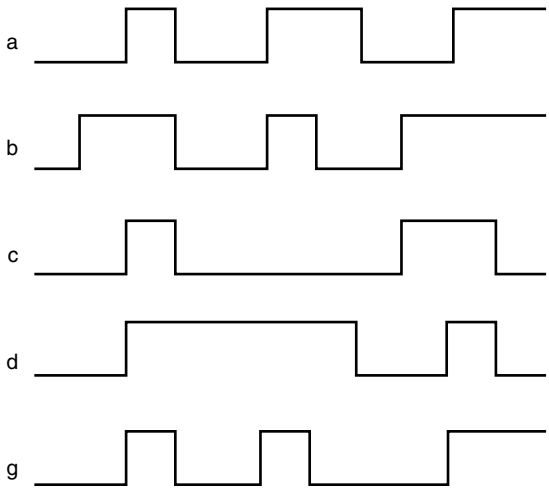
Fault simulation generally operates by the same algorithm as the logic simulation that tests the logical functions. In the execution of fault simulation, however, the faults can be set in the circuit. Figure 6-7 shows examples of fault simulation.

Figure 6-7. Concept of Fault Simulation (1/2)

(a) Circuit example

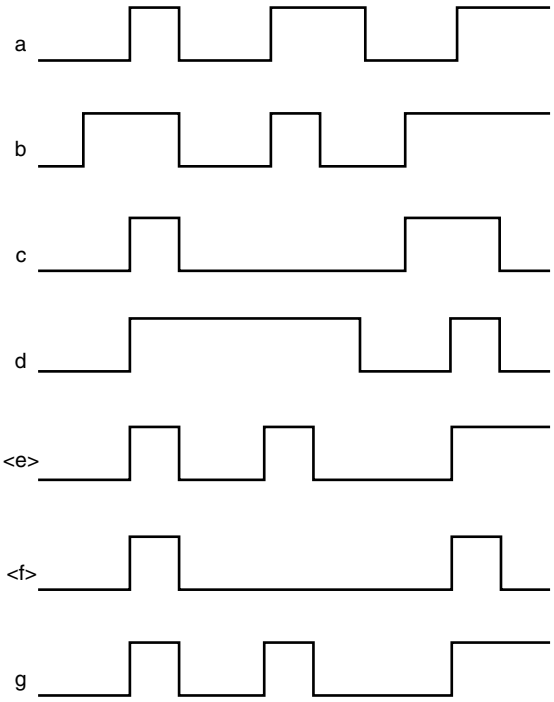


(b) Test patterns

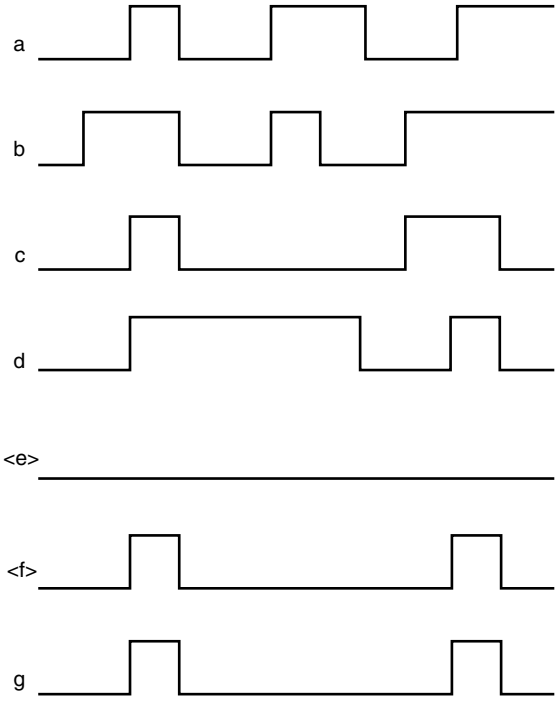


It is assumed that this circuit has a fault and that the output of the 2-input AND gate H is always at the low level. If an input signal the same as Figure 6-7 (c) is input in this case, it can be seen that the result of output “g” will be different (see **Figure 6-7 (c)** and **(d)**). Accordingly, this fault can be detected by these test patterns.

(c) Observation of point e and point f



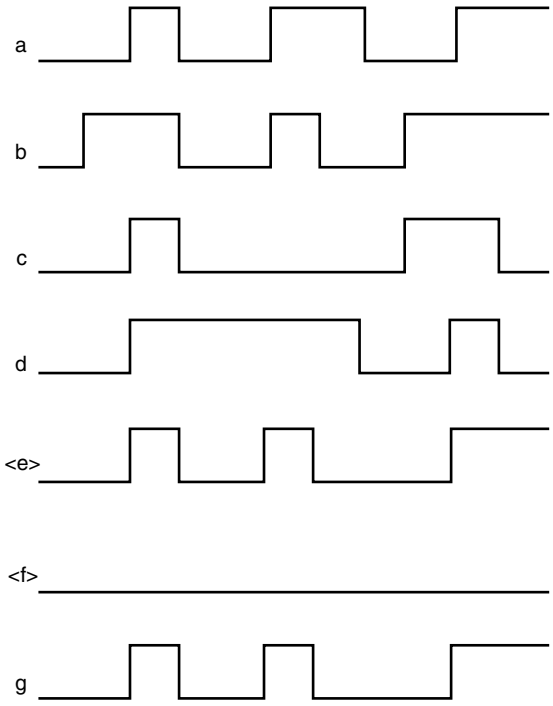
(d) Fault result of AND H



There may also be cases of a fault in which the output of the 2-input AND gate I is always at the low level. As shown in Figure 6-7 (e), this input signal (test pattern) becomes the same as the test pattern in Figure 6-7 (c), which shows that they are ineffective in detecting this fault.

Figure 6-7. Concept of Fault Simulation (2/2)

(e) Fault result of AND I



Fault simulation defines these types of faults one by one with respect to the internal circuit and checks whether the defined faults can be detected at the output pin by performing simulation.

The types of faults that can generally be defined by fault simulation are called single degenerate faults. The following two types of single degenerate faults are defined in circuits:

<1> Stuck-at-1: Fault where a given part is fixed at the high level (“1”)

<2> Stuck-at-0: Fault where a given part is fixed at the low level (“0”)

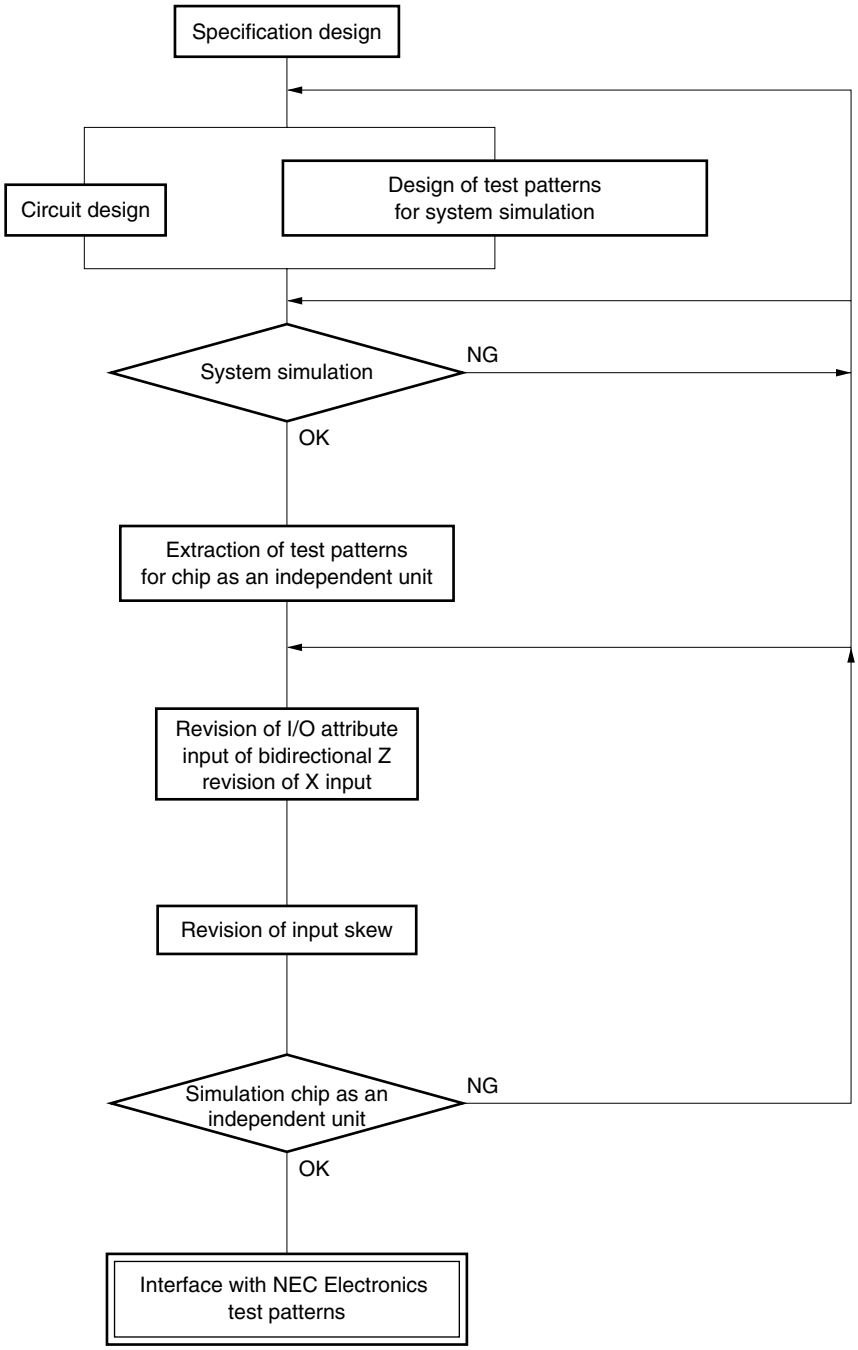
6.8 Consideration of System Simulation

System simulation is a method for checking the functions of a gate array under development by simulating the operations of the gate array in an environment close to the actual operating environment, such as on a board or in equipment.

After checking the functions of the gate array in equipment, the test pattern of the gate array alone is extracted by monitoring the signals at the input/output pins of the gate array.

This test pattern can be used as a test pattern for LSI testing. However, be sure to confirm that there is no problem (that the points to be noted in creating the test pattern are satisfied) by executing a simulation of only the gate array.

Figure 6-8. Creating Test Patterns by System Simulation



CHAPTER 7 MULTIFUNCTION BLOCKS

The CMOS-9HD Series offers the following multifunction blocks, in addition to the normal function blocks. This chapter explains the functions and usage of each multifunction block.

- LVTTL and 5 V tolerant blocks
- Buffer with on-chip pull-up/pull-down resistors
- Clock driver
- GTL+
- Digital PLL
- Memory block
- Compiled memory
- Megamacros

7.1 LVTTL and 5 V Tolerant Blocks

The CMOS-9HD Series offers the following interface blocks.
This section describes the features of each block. For the name of each block, consult NEC Electronics.

Input blocks

- LVTTL input block
- LVTTL input block (with fail-safe function)
- 5 V tolerant input block

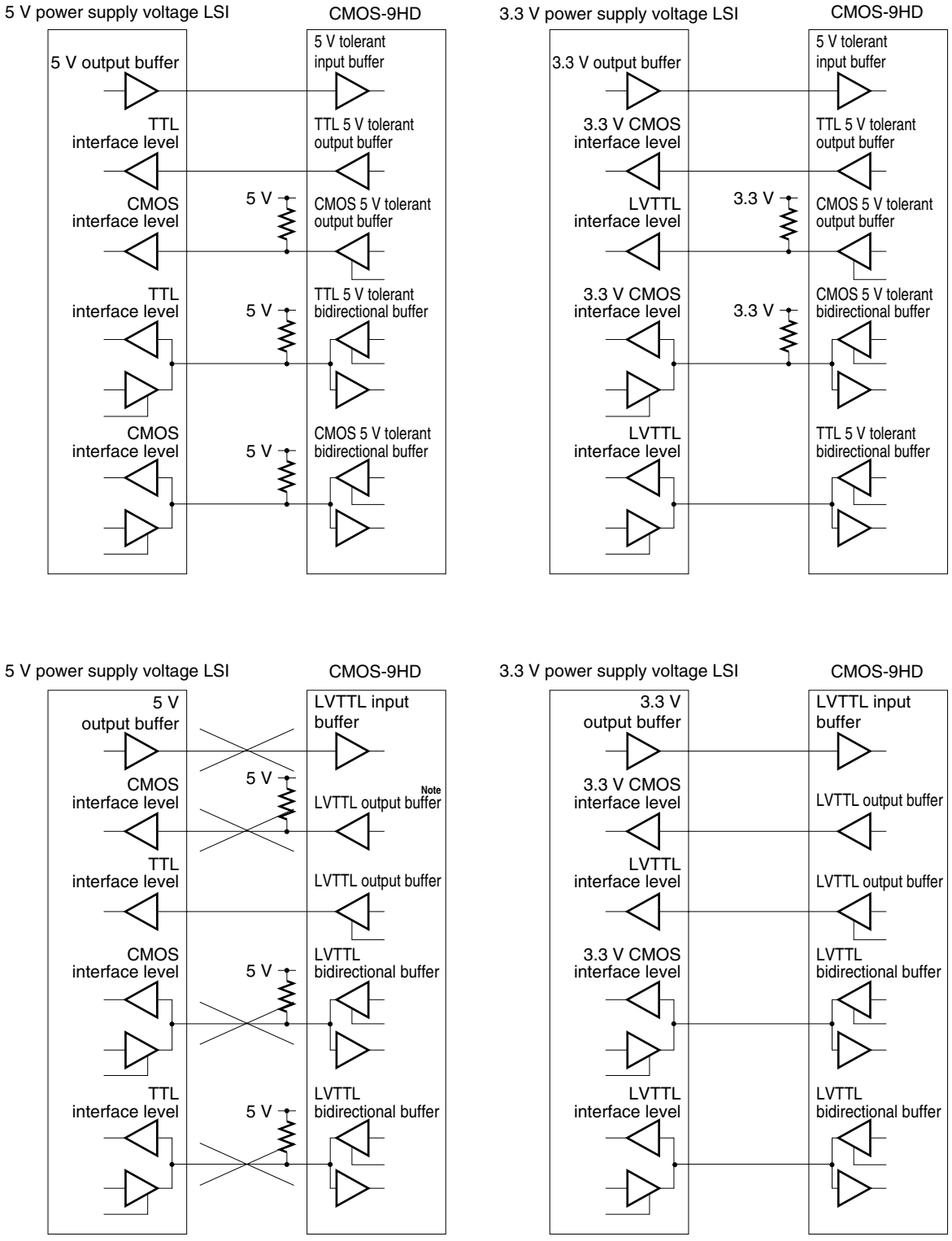
Output blocks

- LVTTL output block
- TTL 5 V tolerant output block
- CMOS 5 V tolerant output block

Each block is connected as shown in **Figure 7-1**.

<R> **Caution μPD66942 can support the LVTTL block only, excluding the block with fail-safe function.**

9Figure 7-1. Connections to 3.3 V and 5 V LSI Devices



Note Can be connected only when 5 V is not applied to LVTTL.

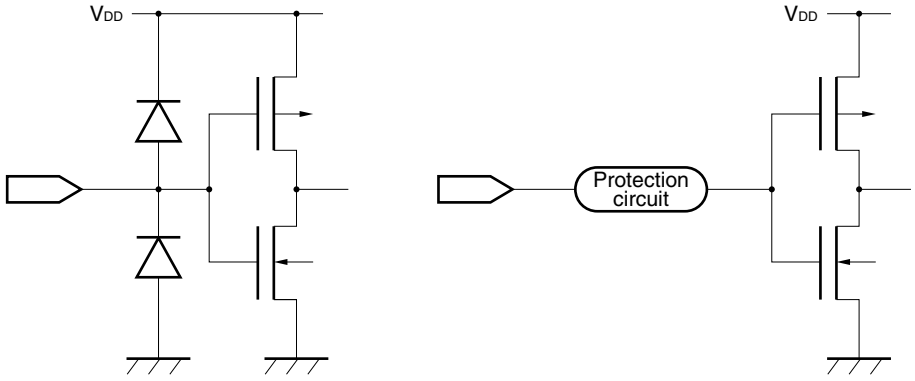
7.1.1 Input blocks

The LVTTL input block receives 3.3 V signals only; it cannot receive 5 V signals. A 5 V signal is received by a 5 V tolerant input block which can also receive 3.3 V signals because it is assumed that the supply voltage of the peripheral circuits of the gate array will be changed to 3.3 V in the future. Therefore, the input characteristics (V_{IL} and V_{IH}) comply with the LVTTL standard.

Because an input voltage higher than V_{DD} cannot be applied to a conventional gate array, no input voltage can be applied when the supply voltage of the gate array is turned off. A LVTTL input block with a fail-safe function can accept an input voltage even if the supply voltage to the gate array is off. If a high-level signal is input to the normal input buffer while the power supply to the gate array is off, a voltage is applied to the power line via protection diode (see **Figure 7-3 Equivalent Circuit Diagram for LVTTL Input Buffer with Fail-Safe Function**). The LVTTL input block with a fail-safe function prevents a voltage from being applied to the power line when the supply voltage to the gate array is off, even if a high-level signal is input. It can therefore be used for hot insertion and removal as long as the specified static voltage condition is satisfied.

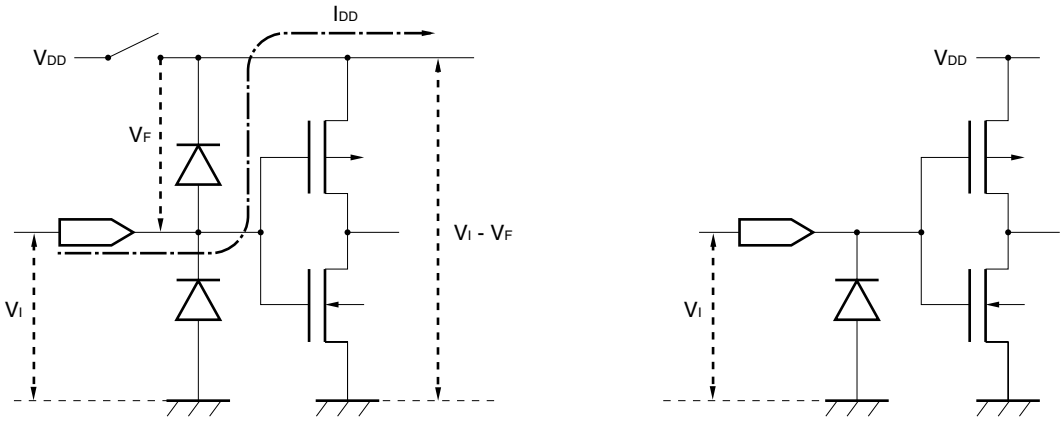
<R> **Caution μPD66942 can support LVTTL input buffer only, excluding the block with fail-safe function. LVTTL input buffer with fail-safe function and 5 V tolerant input buffer cannot be placed.**

Figure 7-2. Equivalent Circuit Diagrams for LVTTL Input and 5 V Tolerant Input Buffers



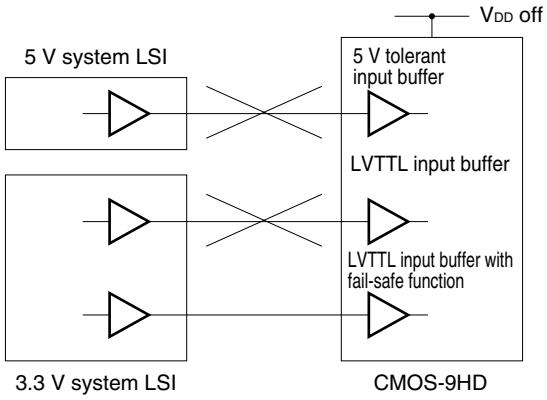
LVTTL input buffer　　5 V tolerant input buffer

Figure 7-3. Equivalent Circuit Diagram for LVTTL Input Buffer with Fail-Safe Function



Conventional input buffer　　LVTTL input buffer with fail-safe function

Figure 7-4. Connecting LVTTL Input Buffer with Fail-Safe Function



7.1.2 Output blocks

The CMOS-9HD Series offers the following two types of 5 V tolerant output blocks in addition to the LVTTL output block. These 5 V tolerant output blocks can be pulled up at a voltage higher than the previously prohibited supply voltage to the gate array (5 V).

<1> CMOS 5 V tolerant output buffer

This buffer is used when full swing at 5 V is necessary. Pull up the pins of this buffer at 5 V when the buffer is connected to a 5 V bus line. Even in this case, the influx current to the gate array is kept to a low level. Therefore, a DC high-level current does not flow, like an N-ch open-drain buffer. This output buffer must also be pulled up when a 3.3 V LSI is driven.

The difference between this output buffer and an open-drain buffer is that the LSI can be driven by this output buffer until the AC output reaches the constant voltage. Consequently, the delay time of the output buffer to the high level can be shortened.

<2> TTL 5 V tolerant output buffer

This buffer is used when the LSI at the next stage is of 5 V TTL logic. The output level is also compatible with a LVTTL output buffer. The TTL 5 V output buffer, however, has a 5 V protection circuit, considering that connection with a 5 V line is necessary. This block can also be pulled up at 5 V. If the supply voltage to the LSI which drives the gate array is changed from 5 V to 3.3 V in the future, only the external pull-up resistor has to be removed. However, the TTL 5 V tolerant output buffer allows a slight influx current to flow to the gate array when the buffer is pulled up at 5 V. Therefore, the output signal may not rise to 5 V depending on the pull-up resistance. Please Count in drop the voltage for $I_R \times R_{PU}$ (see **4.1.2 Output influx current (I_R)**).

With a three-state output buffer and bidirectional buffer (TTL 5 V tolerant output and CMOS 5 V tolerant output), the off-state current slightly increases due to the bias voltage of the 5 V protection circuit when the three-state circuit is in the off state.

<R> **Caution μPD66942 can place the LVTTL output buffer only. 5 V tolerant output buffers cannot be placed.**

Figure 7-5. Equivalent Circuit Diagrams for Output Buffer

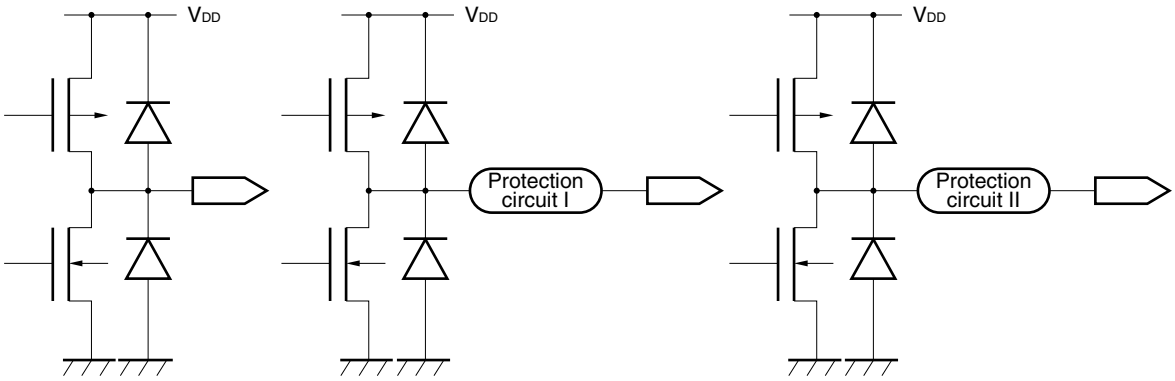
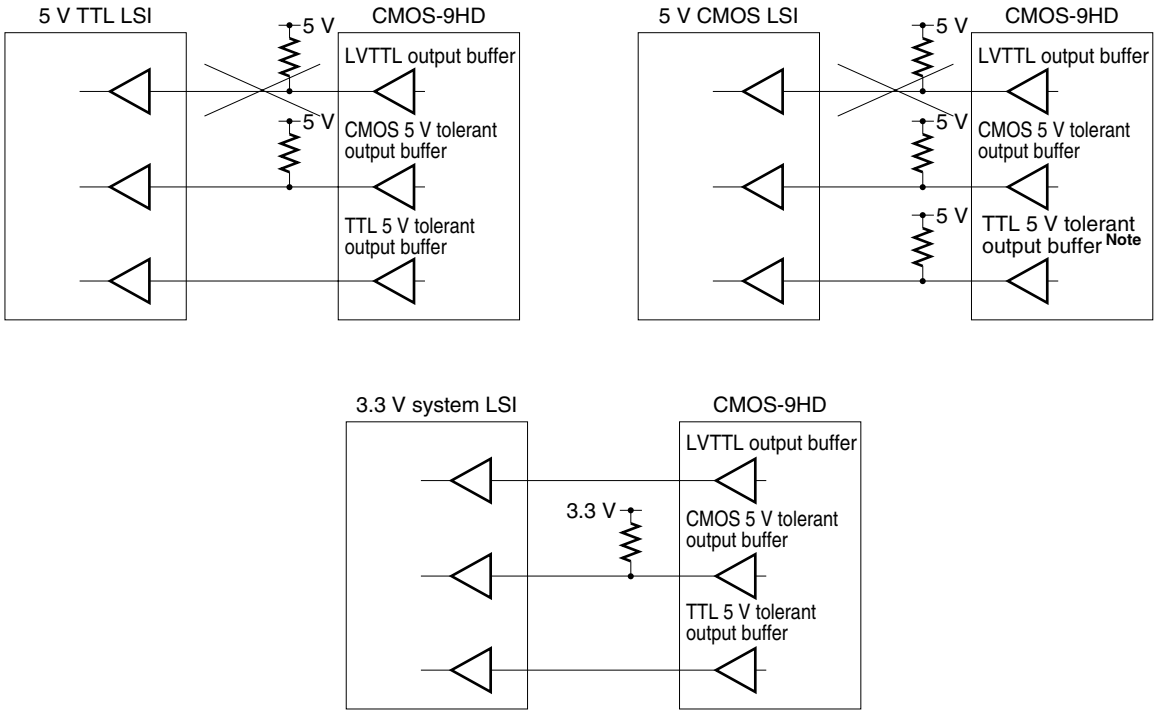


Figure 7-6. Connections for LVTTL Output and 5 V Tolerant Output Buffers



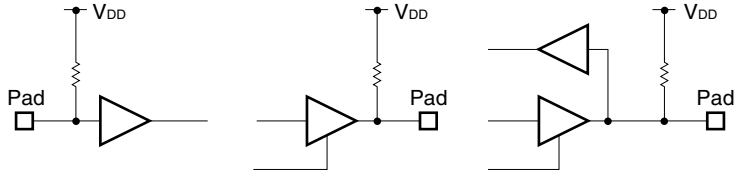
Note Refer to **7.1.2 <2> TTL 5 V tolerant output buffer** when use this buffer.

7.2 Input/Output/Bidirectional Buffers with On-Chip Pull-up/Pull-down Resistors

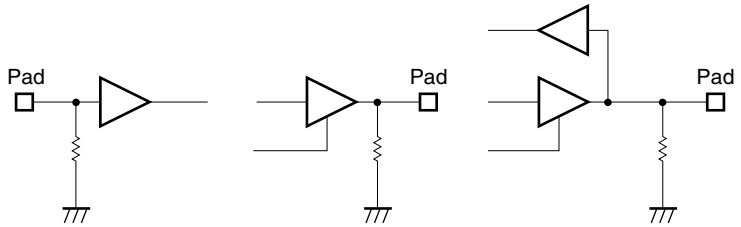
The CMOS-9HD Series has input buffers, Schmitt-input buffers, three-state output buffers, P-ch open-drain output buffers, N-ch open-drain output buffers, bidirectional buffers, Schmitt-input bidirectional buffers, and I/O blocks with on-chip pull-up/pull-down resistors. By using these, a more compact system can be created.

For the name of each block, see **CMOS-9HD Series, EA-9HD Series Block Library (A13052E)**.

Pull-up resistor



Pull-down resistor



During simulation, undefined (X) or high-impedance (Z) values cannot be input to the input pins of the input buffers and bidirectional buffers with on-chip pull-up/pull-down resistors.

The expected output value must be set to “Hi-Z” (high-impedance) or “don’t care” when the output pins of three-state output buffer and bidirectional buffers with on-chip pull-up/pull-down resistors are not active.

7.3 Clock Input Drivers

The clock signal input from an external source to the LSI must be supplied to the many on-chip flip-flops of the LSI, and the blocks used require the following features:

(1) High drive capability (fan-out)
(2) High-speed operation

Therefore, the CMOS-9HD Series offers the dedicated internal blocks listed in Table 7-1 to satisfy this requirement.

These clock input driver-dedicated blocks have the following features:

(1) Fan-out: 82 to 83 per output pin
(2) Low dependency of propagation delay time on fan-out

Because a clock input driver-dedicated block requires a lot of wiring, only one can be used in the LSI, regardless of the type of the block.

If the limits of Table 7-1 are to be exceeded, consult NEC Electronics.

Table 7-1. Clock Input Driver Dedicated Block

Block Name	Number of Allowable Fan-Outs	Number of Cells Used
FIB1	664	56
FDB1	664	56
FUB1	664	56
FWB1	664	56
FIH1	656	56
FDH1	656	56
FIG1	664	56
FDG1	664	56

7.4 Oscillator

7.4.1 Configuration of oscillator

Three types of oscillator blocks are available for configuring an oscillator: one using external feedback resistors, one with internal feedback resistors, and another with an oscillation stop function. Using any of these blocks, an oscillator can be configured simply by connecting a resonator, a capacitor, and limiting resistor to the external pins. However, only up to two oscillator-dedicated blocks can be used. When two blocks are used, one of them must be placed at the polarity opposite to the other to prevent mutual interference between the two, and each circuit must operate on a separate clock. Three or more oscillator blocks must not be used. If it is necessary to use more than one block, consult NEC Electronics.

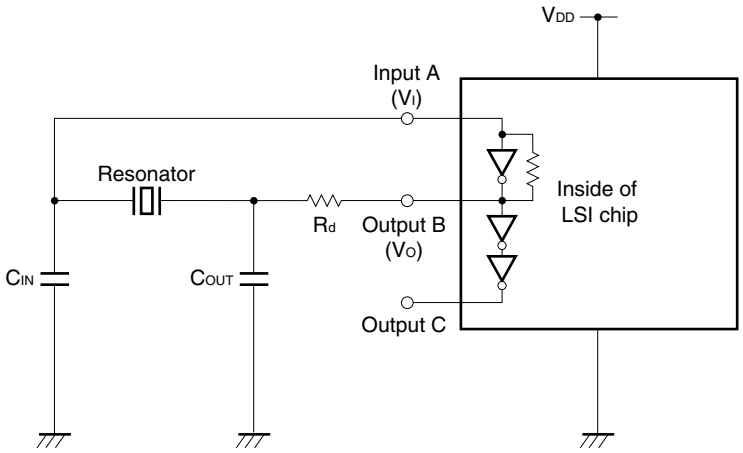
Table 7-2 shows the recommended oscillation frequency range of the oscillator and the combination of blocks configuring the oscillator.

For the configuration of an oscillator block whose placement is limited, see **CMOS Gate Array, Embedded Array Package Design Manual (A16400E)**. When using the oscillator block with stop function, connect the input buffer and oscillator block directly to control stopping of the oscillator block from an external source (see **7.4.2 Description of oscillator**). The stop control pin can be placed anywhere, but it should be placed as close to the oscillator block as possible.

Table 7-2. Recommended Oscillation Frequency Range and Configuration

Feedback Resistor		Stop Function	Configuration		Frequency	Placement Limit
			Input	Output		
External	1 MΩ	No	OSI1	OSO9	MHz band	No
Internal		No	OSI1	OSO1	MHz band	Yes
			OSI1	OSO3 (+OSF1) (formerly OSO0)		
		Yes	OSI2	OSO7		
			OSI2	OSO3 (+OSF3)		

Figure 7-7. Example of Oscillator Configuration



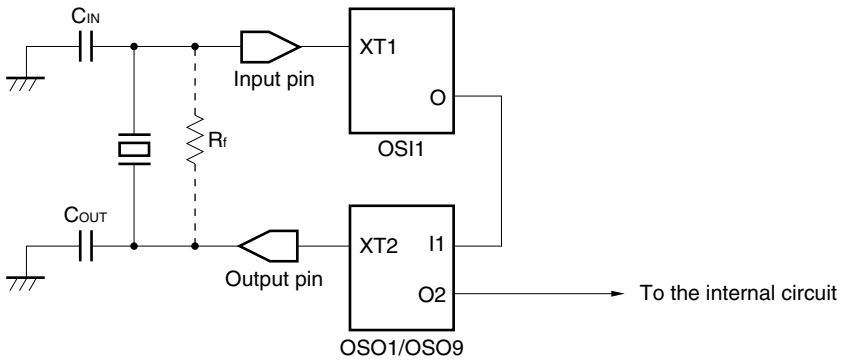
Remark To determine capacitors C_{IN} and C_{OUT}, limiting resistor R_d, and current consumption, evaluation is necessary with an evaluation sample (ES or CS).

7.4.2 Description of oscillator

Describe as follows when using an oscillator.

Figure 7-8. Oscillator Configuration (1/3)

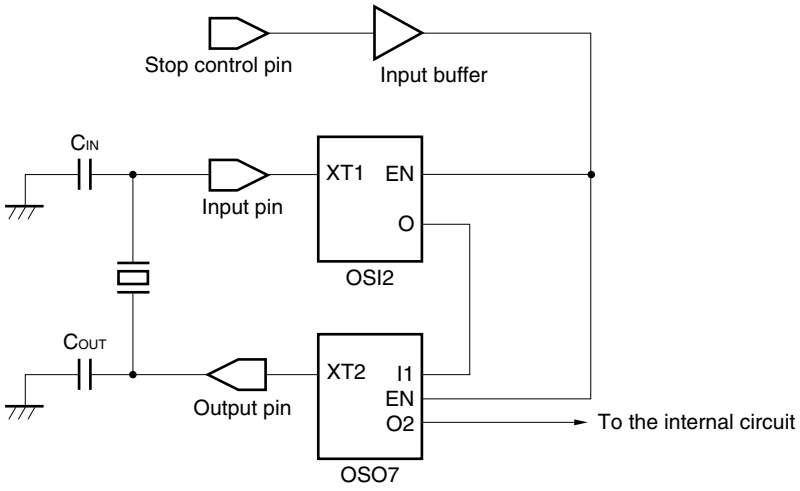
(a) OSI1 + OSO1 or OSI1 + OSO9



Remark When using OSO9, external feedback resistor R_f with a value of 1 MΩ or so is necessary.

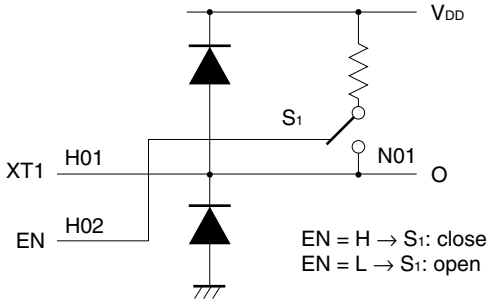
Figure 7-8. Oscillator Configuration (2/3)

(b) OSI2 + OSO7



Remark The O2 output when oscillation is stopped is L level.
The equivalent circuits of OSI2 and OSO7 are shown below.

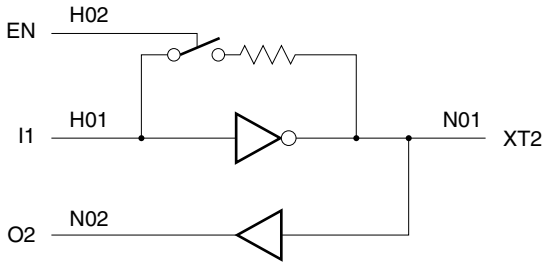
<1> OSI2 equivalent circuit



Truth table

XT1	EN	O	
0	0	0	
1	0	1	
1	1	1	
0	1	X	← Use prohibited

<2> OSO7 equivalent circuit



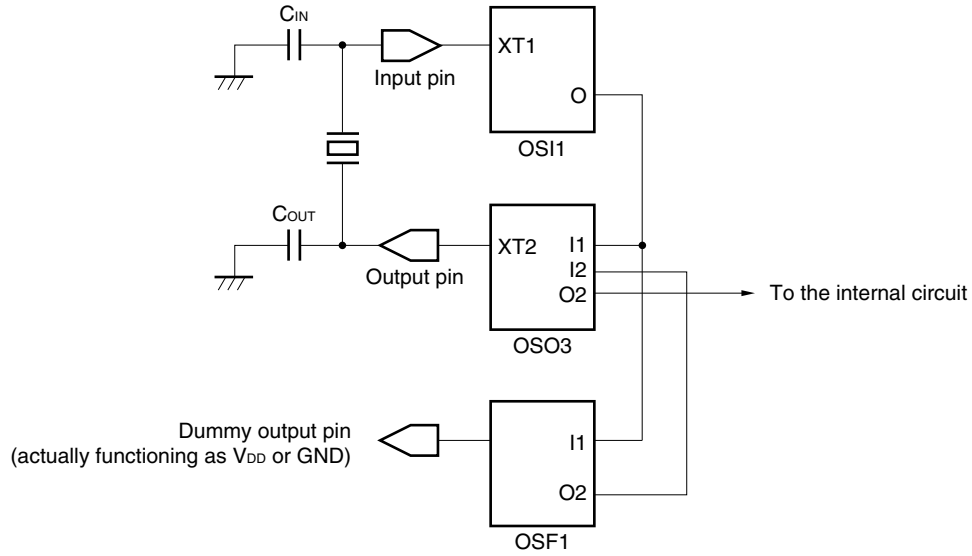
Truth table

I1	EN	XT2	O2	
0	0	1	1	
1	0	0	0	
1	1	0	0	
0	1	X	X	← Use prohibited

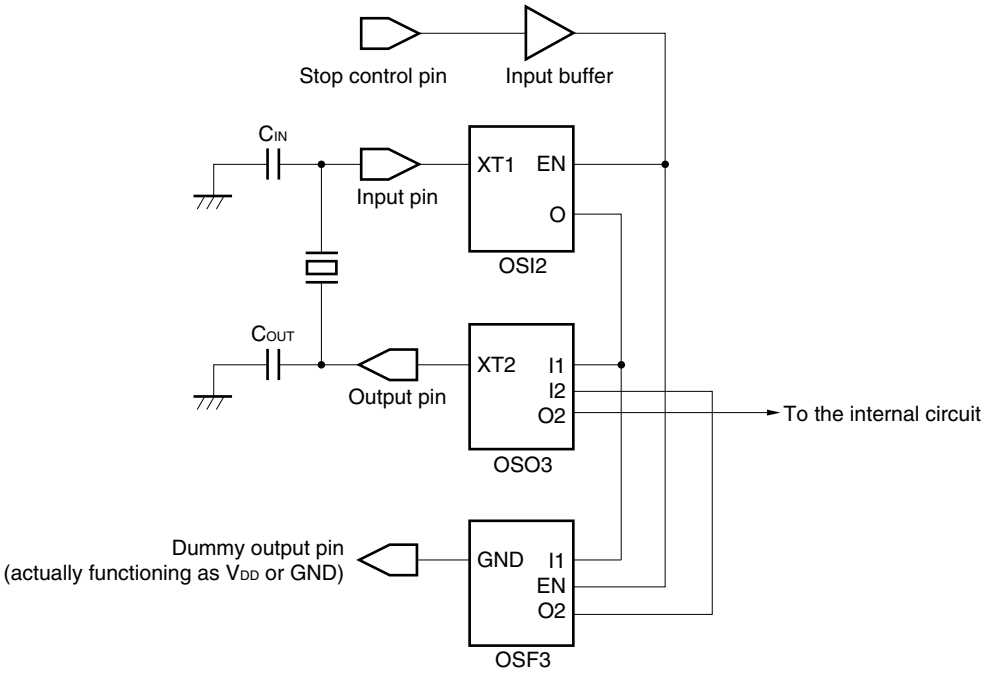
Caution If no resonator is connected, fix the input pin (XT1) to "H" level.

Figure 7-8. Oscillator Configuration (3/3)

(c) OSI1 + OSO3 + OSF1



(d) OSI2 + OSO3 + OSF3



Describe the test pattern of an oscillator as follows:

- Use the inverse of the pattern transmitted to the internal circuit as the input pattern of the input pin (XT1) of OSI1.
- Use the same pattern as that transmitted to the internal circuit as the output pattern of the output pin (XT2) of OSO1, OSO9, OSO7, and OSO3.
- Always input “0” to the stop control pin of OSO7 in the DC test pattern.
- The output pins of OSF1 and OSF3 are dummy pins. The actual function of this pin is V_{DD} or GND, depending on the package.

  However, all the output patterns should be zero (low level), regardless of whether the dummy pin is GND or V_{DD}.

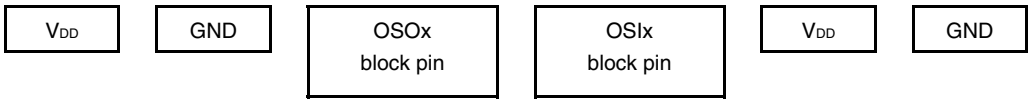
The pattern transmitted to the internal circuit and the pattern output to the output pin (XT2) of OSO1, OSO9, OSO7, and OSO3 is the inverted input pattern.

7.4.3 Notes on configuring oscillator

Because the CMOS-9HD gate array has an internal oscillator block, it can be used to configure an oscillator by connecting a resonator and constants outside the package. Although an oscillator can be easily configured, certain differences from logic circuits must be noted because an oscillator is an analog circuit that operates at a high frequency.

In order for the oscillator to operate stably, it is necessary to optimize the external constants (input capacitor, output capacitor, and limiting resistor). In addition, because the oscillator is an analog circuit, the following points must also be noted.

<1> Surround the oscillator pin (oscillator) with V_{DD} and GND as follows.



Remove the OSOx (oscillator) block pin from consideration for simultaneous switching. V_{DD} and GND around the oscillator pin can be considered for simultaneous switching.

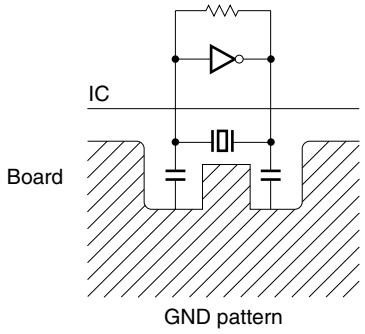
<2> Place the pins that may malfunction when noise is superimposed on them even momentarily (such as the clock and reset pins) as far as possible from the oscillator pin (oscillator).

<3> Since the output buffer is a source of noise, place it as far as possible from the oscillator pin (oscillator).

<4> The following points must be noted for the printed circuit board.

- Place the input and output pins, and the resonator of the oscillator as closely as possible, and keep the length of the wiring between them as short as possible.
- Also keep the length of the wiring between the ground of the capacitors and the GND of the gate array as short as possible. Use as thick a wiring line as possible.
- Keep the leads of the resonator and capacitors as short as possible. Secure the resonator and capacitors onto the printed circuit board to minimize the influence of mechanical vibration.
- As far as possible, enclose the external constants by GND patterns.

Figure 7-9. Example of GND Pattern on Board

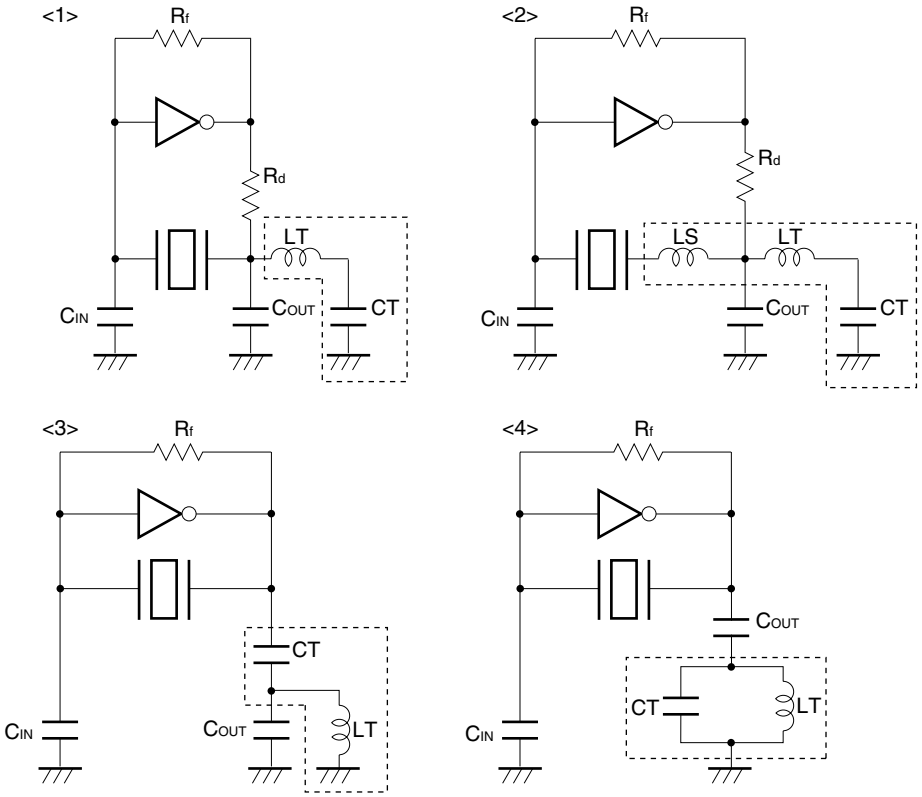


<5> To input the clock generated by the external oscillator from the input pins (OSI1, OSI2) of the oscillation block, connect it to the XIN (OSI1, OSI2) side and leave the XOUT (OSO1) side open. Since the oscillator is logically an inverter, a signal consisting of the inverted signal is input to the internal circuit.

The following points must be noted during evaluation to determine the external constants.

- It is recommended to attach an overtone circuit (LC). Figure 7-10 shows circuit examples.
- Evaluate the oscillator considering variations in the oscillation start time and voltage (etc.).
- Use the printed circuit board that is to be actually used (because the oscillation operation range may fluctuate due to the difference in the dielectric constant of the board).
- Check with the developed CMOS-9HD gate array (ES or CS) and the resonator to be actually used.

Figure 7-10. Example of Overtone Circuits



Remark The section within the broken lines is the overtone circuit.

7.4.4 Constants of external circuit

To generate a clock signal, evaluation of matching with the resonator is necessary. Table 7-3 shows an example of criteria for this evaluation. Determine the parameters to be measured through consultation with the resonator manufacturer.

Table 7-3. Example of Criteria

Item	Criteria
<1> Oscillation frequency	Frequency must be within accuracy of resonator.
<2> Oscillation start voltage (V_s)	2.0 V or less
<3> Oscillation hold voltage (V_h)	$V_h \leq V_s$
<4> Operation on power application	Check oscillation by repeatedly turning ON/OFF power.
<5> Current consumption	As low as possible.
<6> Peak value of oscillated waveform	2.2. V $\leq V_{IH}$, $V_{OH} \leq V_{DD}$ 0 V $\leq V_{IL}$, $V_{OL} \leq$ 0.5 V
<7> Duty factor	50% ±10%

Oscillation is evaluated with the ES or CS model. Because all the gate array, resonator, and external constants are subject to variations due to production conditions and operating conditions, take these variations into consideration during evaluation.

To evaluate parameters <4> through <7> above, fluctuations in power supply and temperature must be also taken into consideration. Measure these parameters under the following MIN., TYP., and MAX. conditions.

[Example] When fluctuations in power supply and temperature are taken into consideration:
T_A = –40 to +85°C
V_{DD} = 3.3 V ±10%
Measure these parameters under the following MIN., TYP., and MAX. conditions.

	MIN.	TYP.	MAX.
T_A (°C)	–40	25	+85
V_{DD} (V)	3.6	3.3	3.0

Remark The values in this table indicate the conditions of the MIN., TYP., and MAX. values of the propagation delay time (t_{PD}) of the gate array, and do not refer to the MIN., TYP., and MAX. values of the resonator.

7.4.5 Recommended resonator

Table 7-4 lists the external resonators that can be added to the OSO7 (OSO1) and OSO9 and their recommended external constants. This data has been evaluated by the resonator manufacturers.

Table 7-4. Resonator Evaluation (1/2)

(a) 3.3 ±0.3 V

Material	Manufacturer	Frequency (MHz)	Part Number		Capacitor	Recommended External Constant		
			Old	New		C_{IN} (pF)	C_{OUT} (pF)	R_d (Ω)
Ceramic	TDK Corp.	16.93	FCR16.93M2G	–	External	5	5	330
		33.86	FCR33.86M2G	–		10	10	–
		4.00	FCR4.0MC5	–	Internal	–	–	3,300
		8.00	FCR8.0MC5	–		–	–	1,500
		50.80	FCR50.8M2G	–		–	–	–
	Murata Mfg. Co., Ltd.	25.00	CSALS25M0X53-B0	–	External	10	10	0
		25.00	CSACW2500MX01[Note1]	CSACW25M0X51-R0[Note1]		10	10	0
		33.86	CSALS33M8X51-B0	–		7	7	0
		50.00	CSALS50M0X51-B0	–		3	3	0
		50.00	CSACW5000MX01[Note1]	CSACW50M0X51-R0[Note1]		3	3	0
		60.00	CSA60.00MXZ040	–		Open	3	0
		2.00	CSTLS2M00G56-B0	–	Internal	–	–	1,500
		2.00	CSTCC2.00MG0H6[Note1]	CSTCC2M00G56-R0[Note1]		–	–	1,500
		4.00	CSTS0400MG06	CSTLS4M00G56-B0		–	–	680
		4.00	CSTCR4M00G55-R0[Note1]	–		–	–	680
		8.00	CSTS0800MG06	CSTLS8M00G56-B0		–	–	220
		8.00	CSTCC8.00MG0H6[Note1]	CSTCC8M00G56-R0[Note1]		–	–	220
		16.00	CSTLS16M0X54-B0	–		–	–	0
		16.00	CSTCV16.00MXJ0C3[Note1]	CSTCV16M0X53J-R0[Note1]		–	–	0
		33.86	CSTCW3386MX01[Note1]	CSTCW33M8X51-R0[Note1]		–	–	0
		40.00	CSTLS40M0X51-B0	–		–	–	0
		40.00	CSTCW4000MX01[Note1]	CSTCW40M0X51-R0[Note1]		–	–	0
	Kyocera Corporation	4.00	PBRC4.00HR[Note1]	–	Internal	–	–	1,500
		8.00	PBRC8.00HR[Note1]	–		–	–	0
		16.00	SSR16.00BR-MN1[Note1]	–		–	–	0
		20.00	SSR20.00BR-H8S[Note1]	–		–	–	0
		33.86	SSR33.86 BR-ALP[Note2]	–		–	–	0
		48.00	SSR48.00 BR-AN05[Note3]	–		–	–	0

Note 1. Surface mount type

Note 2. Surface mount type. A 6.8 kΩ external feedback resistor is required for OSO7 (OSO1).

Note 3. Surface mount type. A 4.7 kΩ external feedback resistor is required for OSO7 (OSO1).

Remark Oscillation environment: V_{DD} = 3.3 ±0.3 V, T_A = –40 to +85°C
External feedback resistor of OSO9: 1 MΩ

Table 7-4. Resonator Evaluation (2/2)

(b) 3.0 ±0.3 V

Material	Manufacturer	Frequency (MHz)	Part Number		Capacitor	Recommended External Constant		
			Old	New		C_{IN} (pF)	C_{OUT} (pF)	R_d (Ω)
Ceramic	Murata Mfg. Co., Ltd.	2.00	CSTCC2.00MG0H6[Note]	CSTCC2M00G56-R0[Note]	Internal	–	–	1,500
		4.00	CSTCR4M00G55-R0[Note]	–		–	–	680
		4.00	CSTS0400MG06	CSTLS4M00G56-B0		–	–	680
		8.00	CSTCE8M00G55-R0[Note]	–		–	–	220
		8.00	CSTS0800MG06	CSTLS8M00G56-B0		–	–	220
		16.00	CSTCE16M0V53-R0[Note]	–		–	–	100
		25.00	CSTCG25M0V51-R0[Note]	–		–	–	100
		25.00	CSTCW2500MX01[Note]	CSTCW25M0X51-R0[Note]		–	–	0
		33.86	CSTCG33M8V53-R0[Note]	–		–	–	68
		33.86	CSTCW3386MX01[Note]	CSTCW33M8X51-R0[Note]		–	–	0
		40.00	CSACW4000MX01[Note]	CSACW40M0X51-R0[Note]	External	3	3	0
		50.00	CSACW5000MX01[Note]	CSACW50M0X51-R0[Note]		Open	Open	0

Note Surface mount type

Remark Oscillation environment: V_{DD} = 3.0 ±0.3 V, T_A = −40 to +85°C
External feedback resistor of OSO9: 1 MΩ

7.5 GTL+

Gunning transceiver logic (GTL+) is a new interface standard that implements high-speed signal transmission with a small amplitude signal. The GTL+ interface input consists of a CMOS differential circuit, similar to that of an ECL interface. However, the GTL+ interface output consists of an N-ch open-drain buffer with an enable pin attached. This enable pin controls the GTL+ output in the same manner as a conventional 3-state buffer. A small amplitude signal below 1.0 V is implemented by terminating the GTL+ output pin with a lower voltage than the power supply voltage.

When a GTL+ interface is used, it is necessary to optimally terminate the output to match the characteristic impedance of the wire and prevent reflection of the signal. In addition, because the amplitude is extremely small, fluctuation of the GND line must be minimized.

Caution When using this interface block, consult NEC Electronics in advance.

7.5.1 Electrical specifications

Table 7-5 shows the electrical specifications of GTL+.

Table 7-5. GTL+ Electrical Specifications

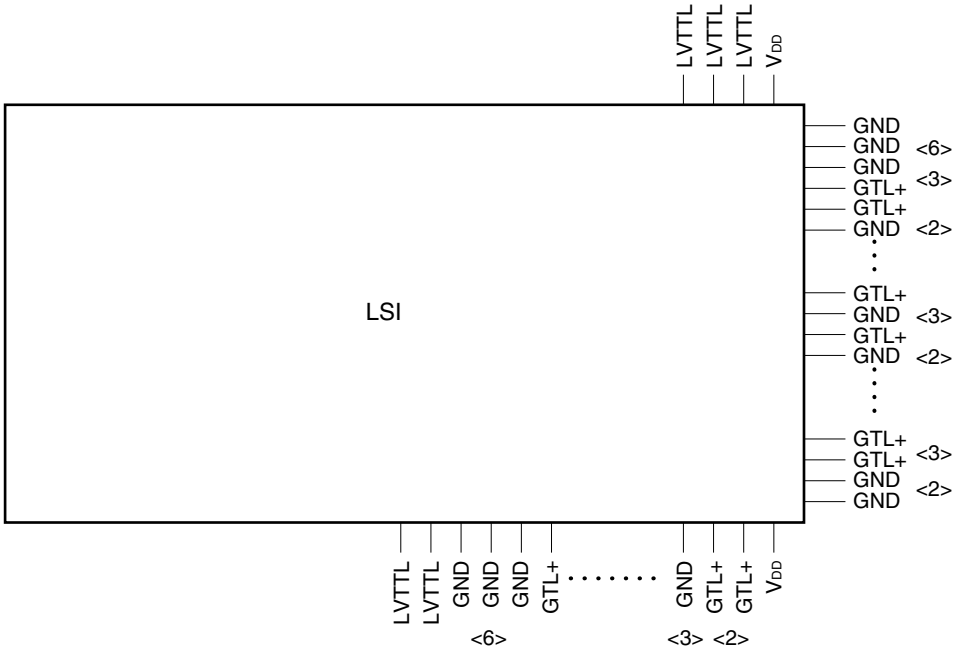
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Termination voltage	V_{TT}		1.35	1.5	1.65	V
Reference voltage	V_{REF}		(2/3) V_{TT} – 2%	1.0	(2/3) V_{TT} + 2%	V
High-level input voltage	V_{IH}		V_{REF} + 0.1			V
Low-level input voltage	V_{IL}				V_{REF} – 0.1	V
High-level output voltage	V_{OH}			1.5		V
Low-level output voltage	V_{OL}				0.55	V

7.5.2 GTL+ pin placement

The following pin placement guidelines must be observed when using the GTL+ interface blocks:

<1> Place a GTL+ buffer only at allowable pins.
<2> Add GND pins at the rate of one pin for every two GTL+ buffers (there are cases where the physical ratio is one GND pin for every GTL+ buffer, depending on the package and master).
<3> Place the added GND pins adjacent to a GTL+ buffer.
<4> Place the GTL+ buffers together between GND pins.
<5> Non-GTL+ buffers (even input buffers) must not be placed between the GND and V_{DD} pins between which GTL+ buffers are inserted.
<6> There should be 3 GND pins surrounding the entire set of GTL+ buffers.

Figure 7-11. Example of GTL+ Pin Placement



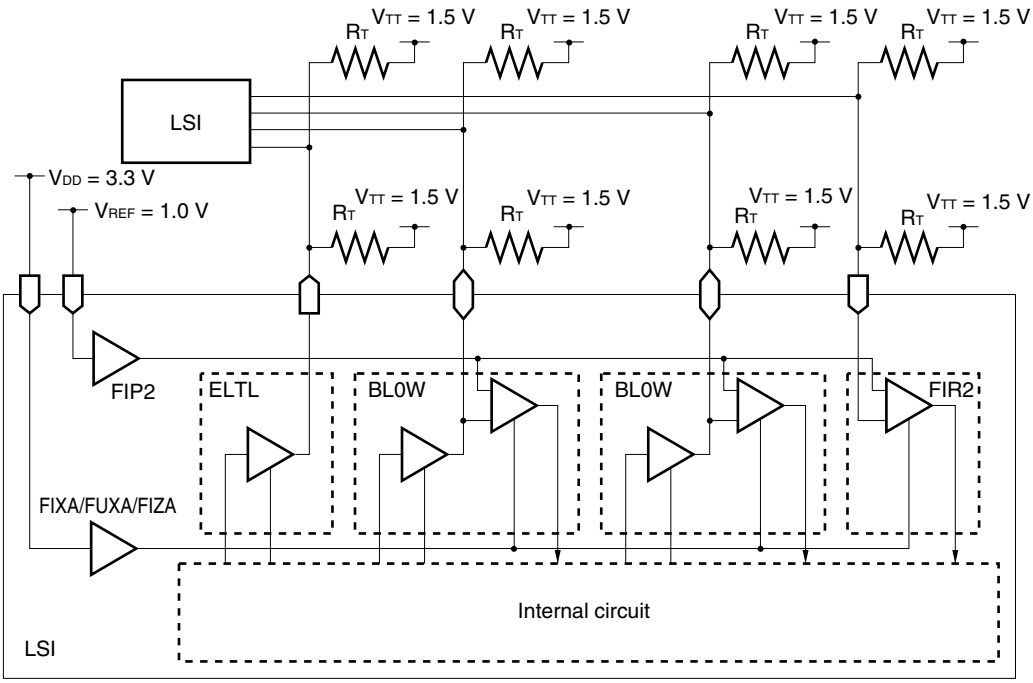
The simultaneous operation limits still apply even if there are multiple types of interfaces on the chip.

7.5.3 Connection rules

The GTL+ interface requires two extra pins. One for applying the reference voltage and another for the control enable. In addition, a terminating resistor optimized to prevent reflection of the signal is also required.

The pin that applies the reference voltage must be connected to the RFV pin of the GTL+ input buffer via an FIP2. The control pin of the GTL+ input buffer must also be connected to the IEN pin of the GTL+ input buffer via FIXA, FUXA, or FIZA.

Figure 7-12. Example of Using GTL+ Interface



7.5.4 Generating test pattern

To use the GTL+ interface, generate a test pattern according to the following rules:

<1> Apply a constant high level to the test pattern at the reference voltage input pin.

<2> Make sure that the test pattern at the input control pin is at low level in at least one of the patterns from pattern 51 to the end.

<3> If there are bidirectional pins, including an interface level other than that of GTL+, input a low-level signal to the input control pin when the input/output direction of the bidirectional buffer is determined.

7.6 Digital PLL

To implement a high-speed circuit that synchronizes two or more chips, the internal clock skew of each chip must be reduced and the phases of the clock signals of the chips must be synchronized as much as possible. However, the load of the clock line of one chip may differ from that of the other chip. It is therefore almost impossible to synchronize the phases of the clock signals with all the related F/F in the system by an ordinary method (see **Figure 7-13**). Therefore, NEC Electronics offers a digital PLL to improve the skew. A PLL (Phase Locked Loop) is used to minimize the phase difference between the clocks of the respective chips by synchronizing the clocks with a basic clock supplied from an external source (see **Figure 7-14**). In this case, the phase difference of the clocks between the respective F/F of each chip must be kept lower than CTS (Clock Tree Synthesis). For details, see **5.4 Clock Signal Design**. This method cannot improve the phase difference of the basic clock, but can relatively easily lower the skew between chips.

Figure 7-13. Clock Skew

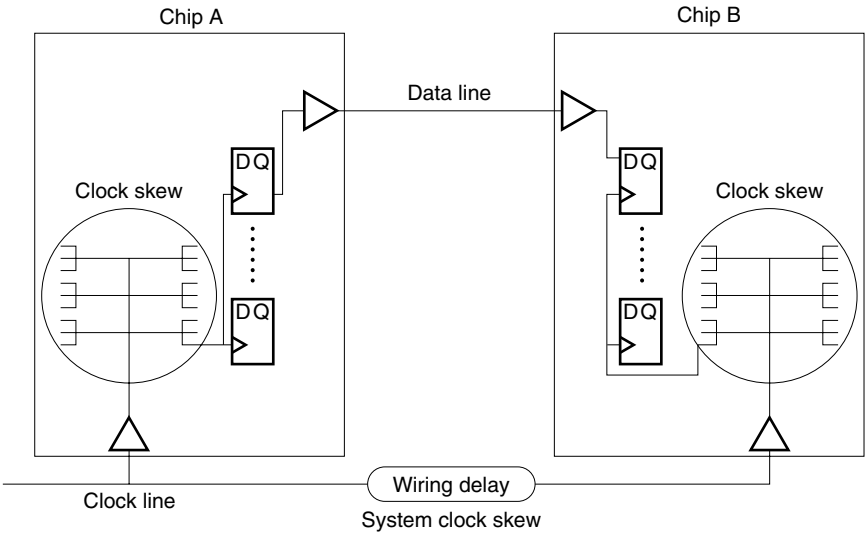
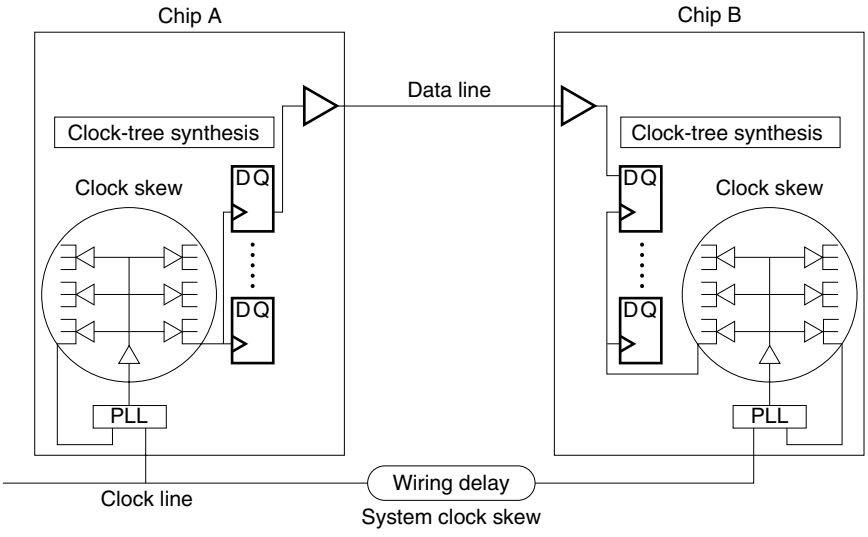


Figure 7-14. Clock Skew Countermeasures

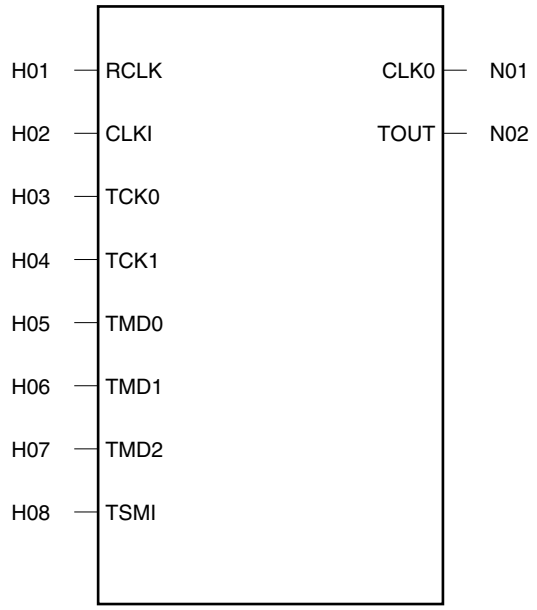


7.6.1 Digital PLL (F9E4)

(1) Function and operation mode

This section explains the functions and operation modes of the digital PLL (F9E4).

Block Name	Function	Number of cells
F9E4	Digital PLL (wide range: 33 to 80 MHz)	3770



F9E4

(a) Pin function list

Pin Name	Signal Name	Attribute	Function
H01	RCLK	IN	Reference clock signal
H02	CLKI	IN	Feedback clock signal
H03	TCK0	IN	Test clock signal (in NEC test mode)
H04	TCK1	IN	Test clock signal (in NEC test mode)
H05	TMD0	IN	Test mode select signal
H06	TMD1	IN	Test mode select signal
H07	TMD2	IN	Test mode select signal
H08	TSMI	IN	NEC test mode-dedicated input pin
N01	CLK0	OUT	Clock output signal
N02	TOUT	OUT	Lock signal and NEC test mode output signal

(b) Operation truth table

RCLK	CLKI	TCK0	TCK1	TMD0	TMD1	TMD2	TSMI	CLK0	TOUT	Mode
A	○	X	X	0	0	0	X	A	LOCK	PLL mode
A	X	X	X	1	0	0	X	0	0	Reset mode
A	X	X	X	0	1	0	X	A	0	Through path mode
A	X	X	X	0	0	1	X	0	0	Stop mode
A	X	○	○	1	1	0	○	0	TEST	NEC test mode
A	X	○	○	1	0	1	○	0	TEST	
A	X	○	○	1	1	1	○	0	TEST	

Remark A, ○: Indicates that the selected mode can be used.

(2) Electrical specifications

The electrical specifications of the digital PLL (F9E4) are shown in Tables 7-6 and 7-7.

Table 7-6. DC Characteristics of Digital PLL (F9E4)

Specification V_{DD} = 3.3 ±0.3 V, T_A = –40 to +85°C (T_J = –40 to +125°C)

Item	Symbol	MIN.	TYP.	MAX.	Units
RCLK high-level input voltage	V_{IH}	2.0		V_{DD}	V
RCLK low-level input voltage	V_{IL}	0		0.8	V

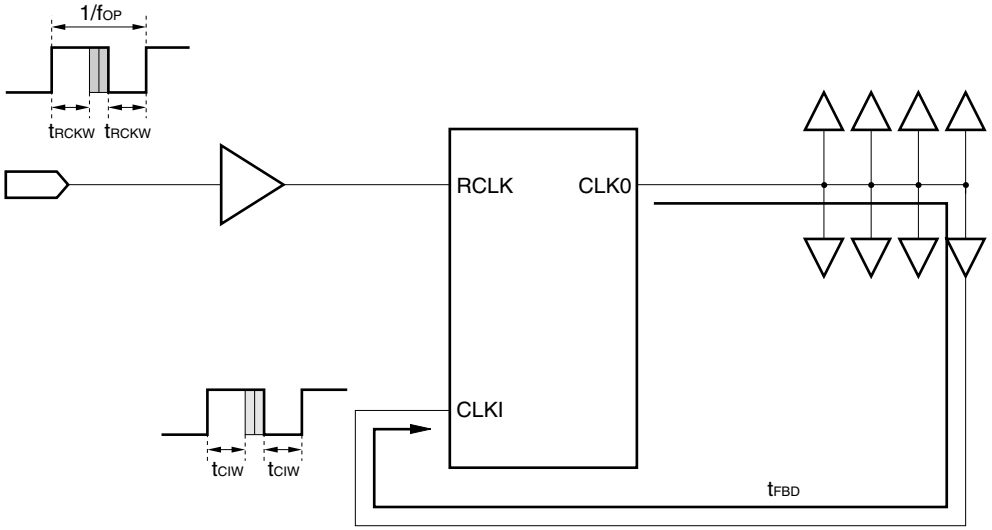
Table 7-7. AC Characteristics of Digital PLL (F9E4)

Specification V_{DD} = 3.3 ±0.3 V, T_A = –40 to +85°C (T_J = –40 to +125°C)

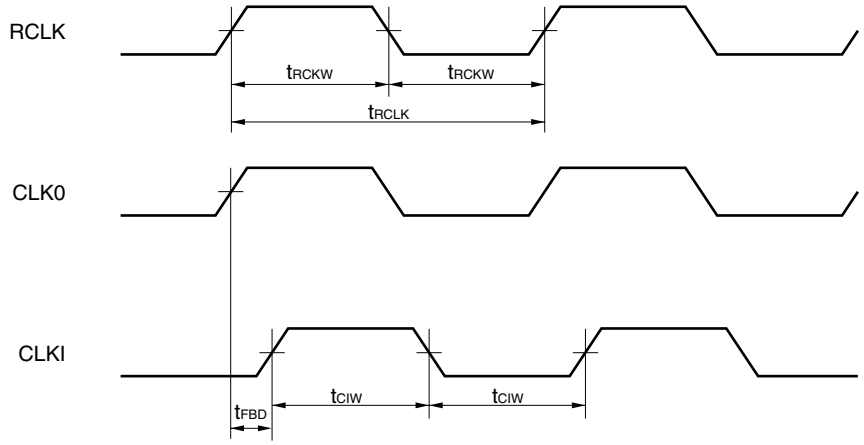
Item		Symbol	MIN.	TYP.	MAX.	Units
Operating frequency		f_{OP}	33		80	MHz
Reference clock (RCLK) cycle		t_{RCLK}	12.5		33.3	ns
Input minimum pulse width (H/L) (vs. RCLK)		t_{RCKW}	4.3			ns
Input minimum pulse width (H/L) (vs. CLKI)		t_{CIW}	3.3			ns
Clock tree delay		t_{FBD}	0		$2t_{RCLK}$ – 8.0	ns
Steady phase error		t_{OFF}			±0.1	ns
Jitter[Note]		t_{JITT}			±0.18	ns
Lead-in time		t_{LOCK}			1325	t_{RCLK}
Reset mode setup time		t_{RSTW}	5			ns
Through path mode delay	(LL)	t_{THR}	0.60	0.90	1.40	ns
	(HH)		0.40	0.70	1.10	
V_{DD} = 3.3 V ±5%	(LL)		0.60		1.30	ns
	(HH)		0.40		1.00	
Output stop time		t_{STOP}	0		4	t_{RCLK}

Note If an input signal includes jitter, the jitter of the digital PLL is the sum of the value shown in the above table and the jitter of the input signal.

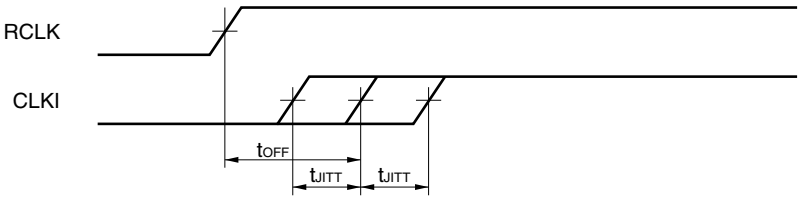
Figure 7-15. Digital PLL Timing (F9E4)



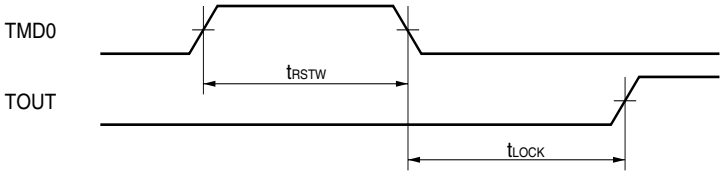
- **Input and output waveforms**



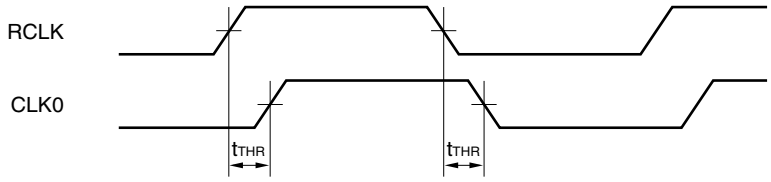
- **Jitter and steady phase error**



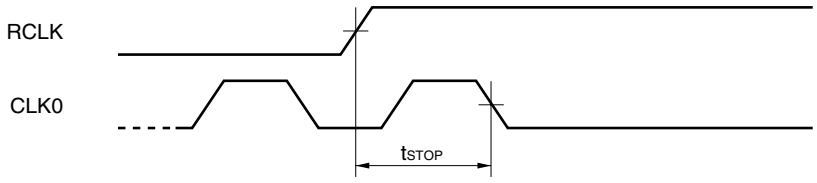
- **Lead-in time and reset mode**



- **Through path mode**



- **Stop mode**



(3) Connection rules

When using the digital PLL, seven input pins must be directly controlled from the external pins of the LSI. Moreover, one output pin must be directly output to an external pin. Therefore, the external input pins are connected via the input buffer of the digital PLL block, and the external output pin is also connected via the output buffer to the output pin of the digital PLL block.

Use the dedicated input buffer “FI0P (3.3 V I/F level)” or “FI0Q (5 V I/F level)” for the input pin of RCLK. Do not share its signal lines with the general signal lines.

Use Schmitt buffers (FIS1) as the input buffers of the TMD0, TMD1, and TMD2 pins to prevent malfunctioning due to noise. Input signals directly from external pins to these buffers, and do not share the signal lines of these buffers with general signal lines. Do not locate an input/output buffer with a high driving capability in the vicinity of these pins, and locate GND pins near these pins as far as possible to prevent malfunctioning due to noise.

Configure the circuits of the TCK0, TCK1, and TSMI input pins, and TOUT output pins so that these pins can be directly controlled or output by an external circuit in the NEC test mode shown in the table below. When these pins are shared with general signal lines, their wiring length tends to be long. Therefore, do not multiplex these pins with the pins that must operate at high speeds.

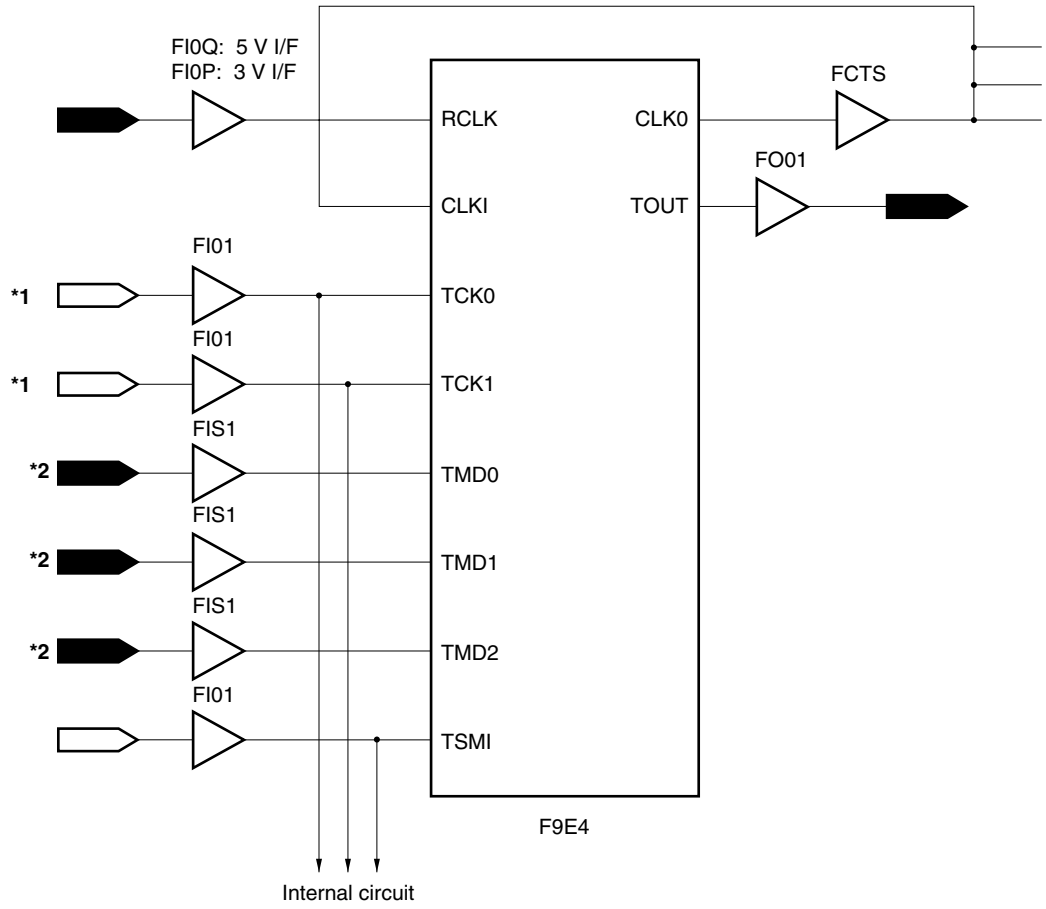
Figure 7-16 shows an example.

NEC test mode

TMD0	TMD1	TMD2
1	1	0
1	0	1
1	1	1

Figure 7-16. Digital PLL Connection Example (F9E4) (1/2)

(a) When digital PLL is used as single unit



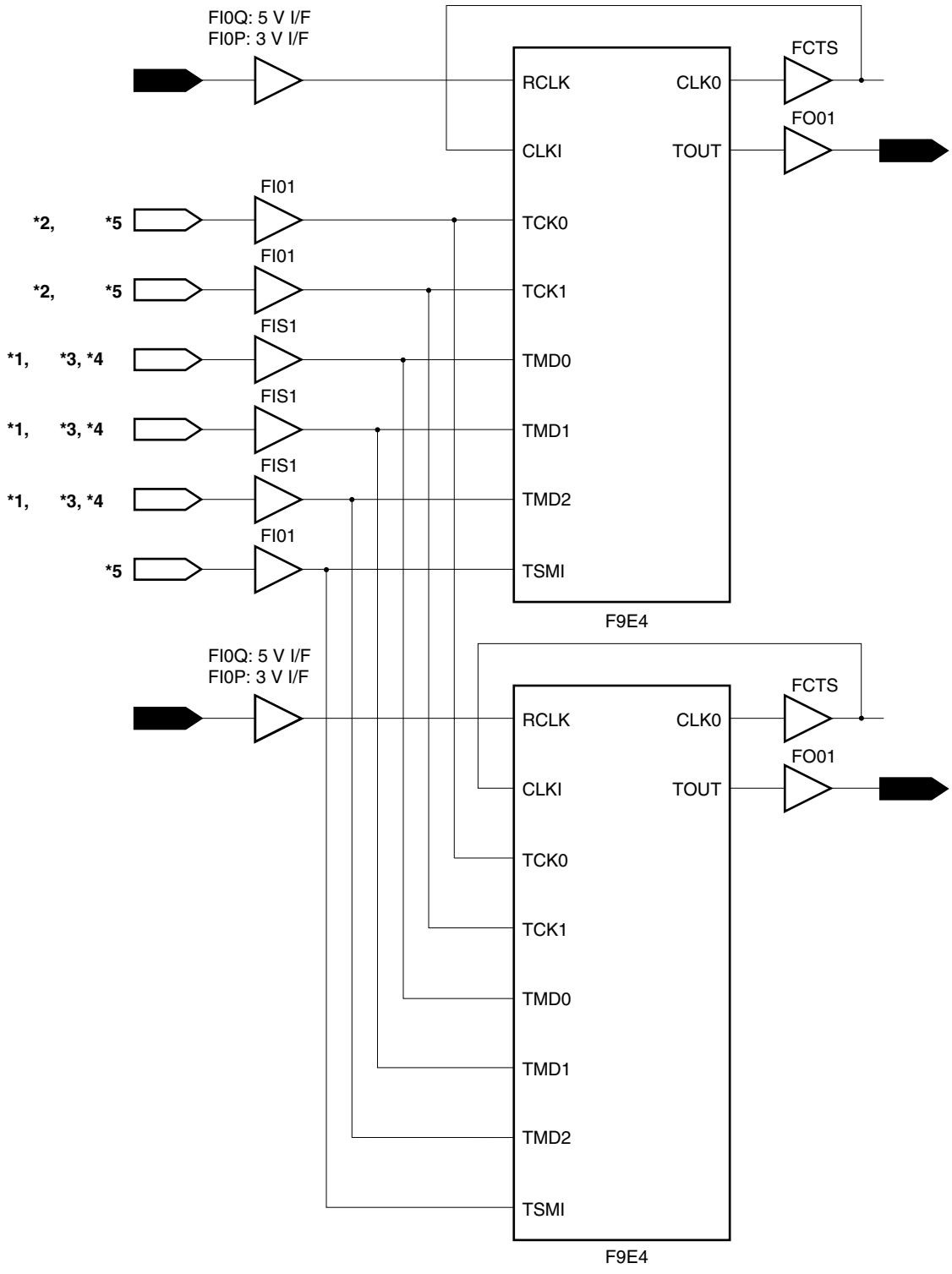
Caution 1. ▬▶: Pin that cannot be shared with other general function pins, except for TMD0, which is shared with power-on reset. In the same way, the pin connected to the TOUT pin cannot be shared.

Caution 2. Cannot multiplex with using bidirectional buffer, for the pin marked *1.

Caution 3. Use a Schmitt buffer for the pin marked *2.

Figure 7-16. Digital PLL Connection Example (F9E4) (2/2)

(b) When two digital PLLs are used separately



Caution 1. Use a Schmitt buffer for the pin marked *1.

Caution 2. The pin marked *2 cannot be shared with general pins using a bidirectional buffer.

Caution 3. The pin marked *3 cannot be shared with general pins, except for TMD0, which is shared with power-on reset.

Caution 4. The pin marked *4 can be shared with the same function pin only if several digital PLLs are used.

Caution 5. The pin marked *5 cannot be shared with pins using a GTL+ interface buffer, N-ch open-drain buffer, or CMOS 5 V tolerant output buffer.

Caution 6. ▬▶: Pin that cannot be shared with other pins.

(4) Digital PLL operation

Digital PLLs have a number of operation modes other than the PLL mode. This section explains the operation modes necessary for designing gate arrays with a PLL.

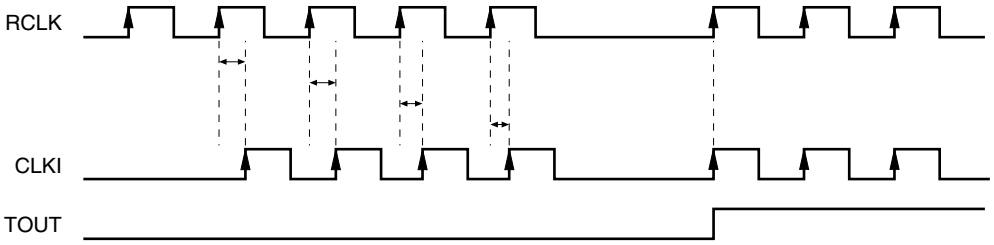
Be sure to reset the digital PLL (by executing the reset mode) before using the digital PLL (on power application). Execute reset when the voltage of the gate array has reached the switching voltage and the clock with the desired frequency has been input to the RCLK pin.

(a) PLL mode

This mode is set when both the TMD0 and TMD1 pins are low. In this mode, the digital PLL synchronizes the phases of an external reference clock with the phase of the internal clock of the LSI. The TOUT pin goes high when the clock signals are synchronized. Exercise care in using this pin because it may generate spike noise.

Moreover, when using the TOUT pin, be sure to contact NEC Electronics.

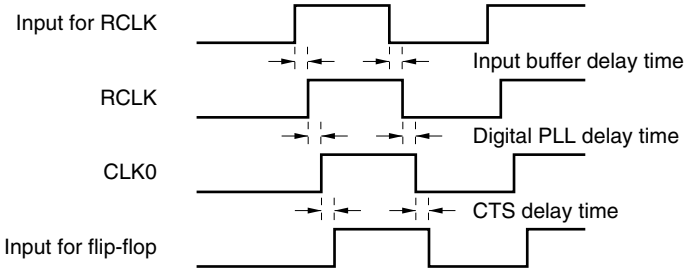
Figure 7-17. PLL Mode Timing



(b) Through path mode

This mode is set when the TMD0 pin is low and the TMD1 pin is high. Because simulation cannot be executed in the PLL mode which is the normal operation mode of the digital PLL, create a test pattern for simulation in this mode. Give thorough consideration to the delay of the clock line, including the delay of the digital PLL.

Figure 7-18. Through Path Mode Timing



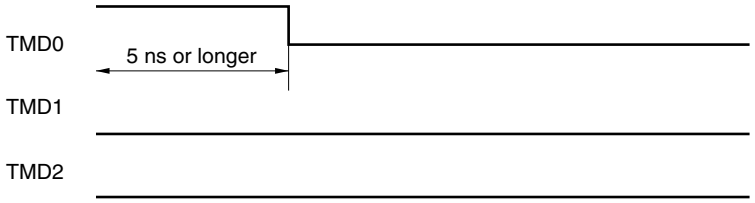
(c) Reset mode

This mode is for resetting the entire digital PLL.

After power application, execute the reset mode when the power supply of the gate array is at the voltage at which it is to be used and the frequency of RCLK has stabilized at the frequency at which it is to be used.

Although the timing of setting reset mode is not prescribed, take sufficient care not to input noise to the TMD0, TMD1, or TMD2 pins, and set the reset mode for at least 5 ns. Also, because the output clock will be unstable until the digital PLL locks after reset mode is released, reset the user circuit after the digital PLL has locked.

Figure 7-19. Reset Mode Timing



The reset mode is necessary in the following cases:

<1> After power application

<2> If the frequency of the reference clock (RCLK) constantly fluctuates.

Be sure to input stable clock (of constant frequency) to RCLK in the PLL mode.

If the frequency of the clock input to RCLK constantly fluctuates (i.e., if the following allowable frequency fluctuation range is exceeded), be sure to execute the reset mode.

Allowable frequency fluctuation: Frequency fluctuation = ±1 ns

<3> When the clock signal stop mode is executed and released

Example of using TMD0 related to reset mode

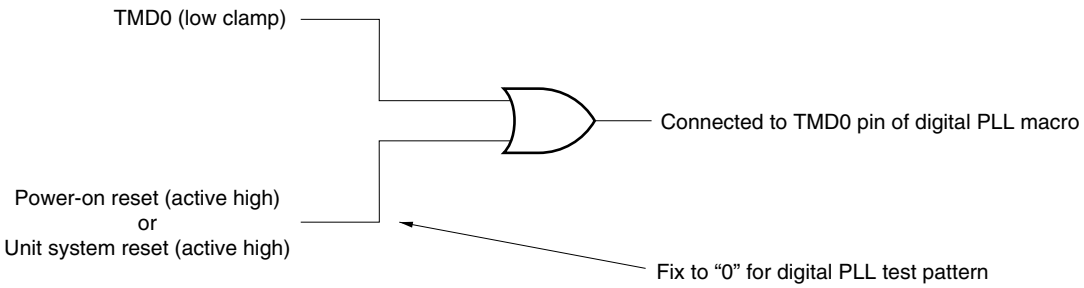
If the reset signal used when testing (simulating) the gate array is different from the signal for actual use (when the active level differs or when the logic of the reset signal is organized in the gate array), use the following circuit.

In this circuit configuration, clamp the TMD0 pin to the low level for actual use and fix the reset signal to "0" for testing.

At this time, make sure that noise is not superimposed on the TMD0 pin of the digital PLL.

Consult NEC Electronics when inserting a gate between the dedicated pin and PLL as shown in the following figure.

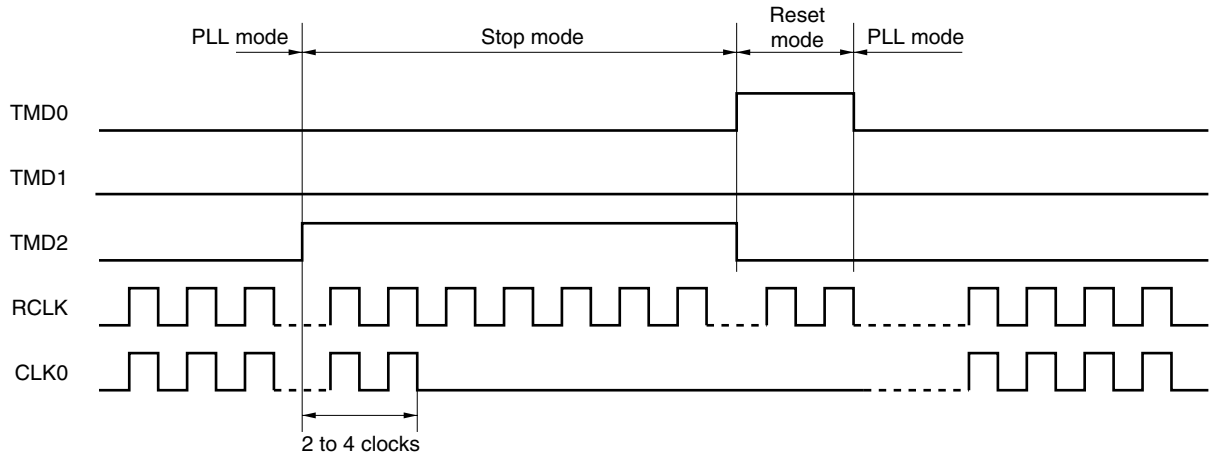
Figure 7-20. Example of Using TMD0



(d) Stop mode

This mode is set when the TMD0 and TMD1 pins are low and the TMD2 pin is high. In this mode, the internal clock signal of the gate array is stopped 2 to 4 clocks after TMD2 has gone high. When releasing the stop mode or when stopping the basic clock input to the RCLK pin, be sure to input the basic clock again and execute the reset mode.

Figure 7-21. Stop Mode Timing

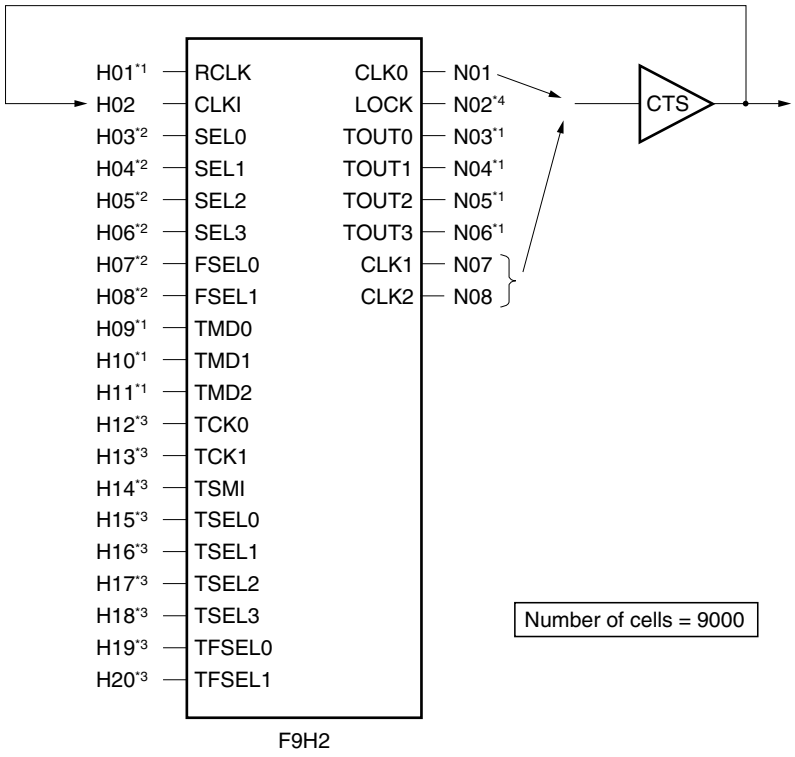


7.6.2 Digital PLL (F9H2)

(1) Function and operation mode

This section explains the functions and operation modes of the multiplication digital PLL (F9H2).

Figure 7-22. Digital PLL Connection Example (F9H2)



Caution 1. Pins marked *1 cannot be shared with other LSI pins (dedicated pins).

Caution 2. Pins marked *2 do not need to be connected with external pins.

Caution 3. Pins marked *3 can be shared with other LSI pins.

Caution 4. Pins marked *4 do not need to be connected with external pins.

Caution 5. Be sure to connect one of the CLK0 to CLK2 outputs to the CLKI input. (Never divide the outputs by a F/F or input a divided output to CLKI.) If multiple CLKn are used, the phases are not synchronized.

Caution 6. Clamp the SEL3, FSEL0, and FSEL1 pins to either the high level or low level by using F091.

(a) Pin function list

Pin Name	Signal Name	Attribute	Function
H01	RCLK	IN	Reference clock signal
H02	CLKI	IN	Feedback clock signal
H03	SEL0	IN	Multiplication factor setting signal
H04	SEL1	IN	
H05	SEL2	IN	
H06	SEL3	IN	
H07	FSEL0	IN	Frequency setting signal
H08	FSEL1	IN	
H09	TMD0	IN	Test mode select signal
H10	TMD1	IN	
H11	TMD2	IN	
H12	TCK0	IN	Test mode clock input signal
H13	TCK1	IN	
H14	TSMI	IN	Test mode switching signal
H15	TSEL0	IN	Test mode multiplication factor setting signal
H16	TSEL1	IN	
H17	TSEL2	IN	
H18	TSEL3	IN	
H19	TFSEL0	IN	Test mode setting signal
H20	TFSEL1	IN	
N01	CLK0	OUT	Multiplication clock output signal
N02	LOCK	OUT	Lock signal
N03	TOUT0	OUT	NEC test mode output signal
N04	TOUT1	OUT	
N05	TOUT2	OUT	
N06	TOUT3	OUT	
N07	CLK1	OUT	Multiplication clock output signal (2-division output)
N08	CLK2	OUT	Multiplication clock output signal (4-division output)

(b) Operation truth table

RCLK	TCKn	SELn	TSELn	TFSEL1	TFSEL0	TMD2	TMD1	TMD0	TSMI	CLKn	LOCK	TOUTn	Mode
A	X	○	X	X	X	0	0	0	X	A	LOCK[Note 1]	0	PLL mode[Note 2]
X	X	○	X	X	X	0	0	1	X	0	0	0	Reset mode
A	X	○	X	X	X	0	1	0	X	A	0	0	Through path mode[Note 3]
X	X	○	X	X	X	1	0	0	X	0	0	0	Stop mode
A	○	X	○	0	0	1	0	1	○	0	TEST	TEST	NEC test mode
A	○	X	○	0	1	1	0	1	○	0	TEST	TEST	
A	○	X	○	1	0	1	0	1	○	0	TEST	TEST	
A	○	X	○	1	1	1	0	1	○	0	TEST	TEST	
A	○	X	○	0	0	1	1	0	○	0	TEST	TEST	
A	○	X	○	0	1	1	1	0	○	0	TEST	TEST	
A	○	X	○	1	0	1	1	0	○	0	TEST	TEST	
A	○	X	○	1	1	1	1	0	○	0	TEST	TEST	
A	○	X	○	0	0	1	1	1	○	0	TEST	TEST	
A	○	X	○	0	1	1	1	1	○	0	TEST	TEST	
A	○	X	○	1	0	1	1	1	○	0	TEST	TEST	
A	○	X	○	1	1	1	1	1	○	0	TEST	TEST	

Note 1. This is 1 when the phase is locked (when the phase of RCLK and CLKI is synchronized).

Note 2. Multiplied A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

Note 3. A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

Remark A, ○: Indicates that the selected mode can be used.

(c) Multiplication factor settings

Set the multiplication factor by SELn (SELn, FSELn can also be clamped to F091).

Multiplication factor	FSELn[Note]	SEL3[Note]	SEL2	SEL1	SEL0	Usable Frequency Band (RCLK)
1	X	X	0	0	0	33 to 80 MHz
2	X	X	0	0	1	33 to 50 MHz, 66 to 100 MHz
3	X	X	0	1	0	33 MHz, 44.3 to 66.6 MHz
4	X	X	0	1	1	33 to 50 MHz

Note Fix FSELn and SEL3 to either 1 or 0 using F091.

Caution Can only be used within the above shown frequency band; other frequencies cannot be used.

(2) Electrical specifications

The electrical specifications of the digital PLL (F9H2) are shown in Table 7-8.

Table 7-8. AC Characteristics (F9H2)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
RCLK frequency[Note 1]	t_{RCKT}	33.0 33.0 33.0 33.0		80.0 100.0 66.6 50.0	MHz MHz MHz MHz	When × 1 is set When × 2 is set When × 3 is set When × 4 is set
Power supply allowable fluctuation width				V_{DD} ±0.3	V	Peak-to-peak
Input duty	t_{CIW}			50 ±5	%	
RCLK pulse width	t_{RCKW}	2.8			ns	
CLKI pulse width	t_{SIW}	2.0			ns	
Output jitter	t_{JITT}			600[Note 2]	ps	Fluctuation of the power supply caused by noise: 300 mV (peak-to-peak) or less
				Note 2, 3	ps	Fluctuation of the power supply caused by noise: 300 to 600 mV (peak-to-peak)
Output duty	t_{COW}	45		55	%	
Through path mode delay	t_{THR} t_{THL} t_{THR} t_{THL} t_{THR} t_{THL}	1.10 1.15 1.10 1.15 1.10 1.15		2.70 2.70 2.70 2.70 2.70 2.70	ns ns ns ns ns ns	CLK0 output CLK0 output CLK1 output CLK1 output CLK2 output CLK2 output
CTS delay restriction	t_{FBD}			20.42	ns	
Lead-in time	t_{LOCK}			2116	RCLK	
Steady phase error	t_{OFF}			±0.1	ns	No input jitter
Reset pulse width	t_{RSTW}	5			ns	
Output stop time	t_{STOP}	2		4	t_{COW}	
Power consumption[Note 4]	P_{PLL}		65		mW	V_{DD} = 3.3 V, T_A = 85 °C, RCLK = 50 MHz, CLK0 = 100 MHz

Note 1. The usable frequency range for each multiplication factor is as follows. Note that other frequencies cannot be used.

× 1: 33 to 80 MHz
× 2: 33 to 50 MHz, 66 to 100 MHz
× 3: 33 MHz, 44.3 to 66.6 MHz
× 4: 33 to 50 MHz

Note 2. The output jitter when the input jitter is 80 ps or less
If the input jitter exceeds 80 ps, add the input jitter to the output jitter value.

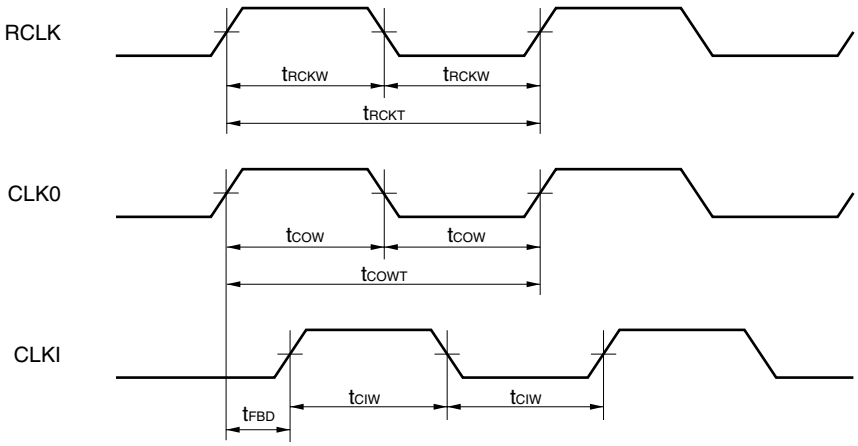
Note 3. Jitter [ps] = fluctuation of the power supply [mV] × 2 [ps/mV]

Note 4. The power consumption is calculated by using the following formula.

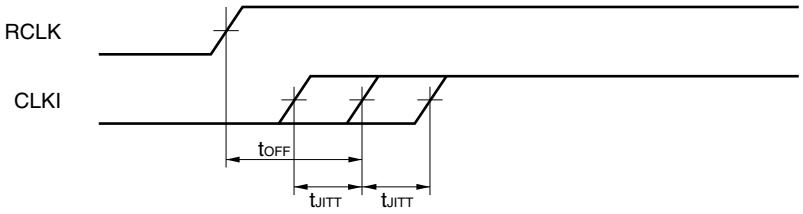
$$P_{PLL} = \{RCLK \times 900 \times 1.09 + (RCLK/8) \times 100 \times 1.09 + (RCLK/12) \times 80 \times 1.09 + CLK0 \times 130 \times 1.09\} / 1000 \text{ [mW]}$$

Remark RCLK: RCLK frequency [MHz], CLK0: Multiplication clock frequency [MHz],
1.09: Value when V_{DD} = 3.3 V, T_A = 85°C

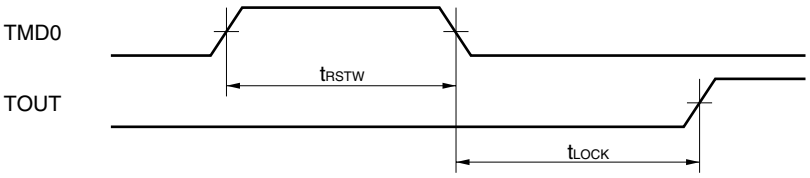
- **Input and output waveforms**



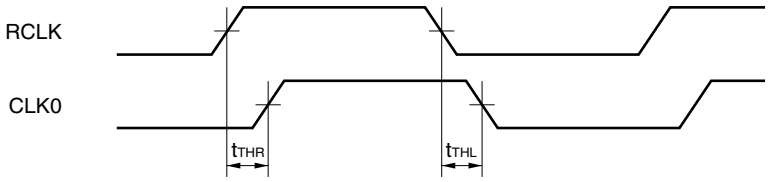
- **Jitter and steady phase error**



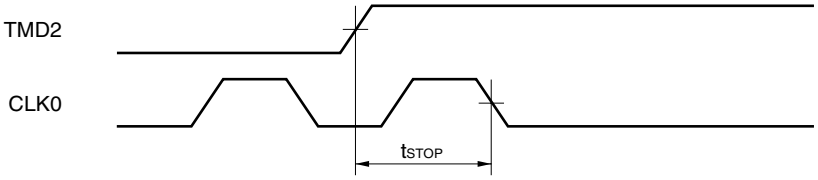
- **Lead-in time and reset mode**



- **Through path mode**



- **Output stop mode**

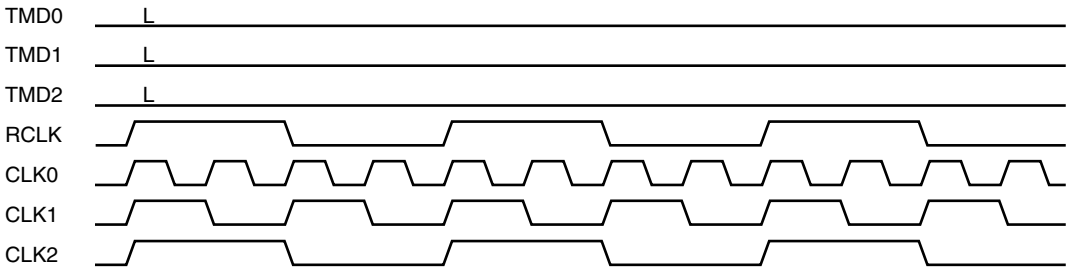


(3) Digital PLL operation mode

(a) PLL mode

In this mode, the phase of RCLK is synchronized with the phase of CLKn, and the clock set by the multiplication factor setting signal (SELn) is output.

[Waveform when x4 is set in PLL mode]



(b) Reset mode

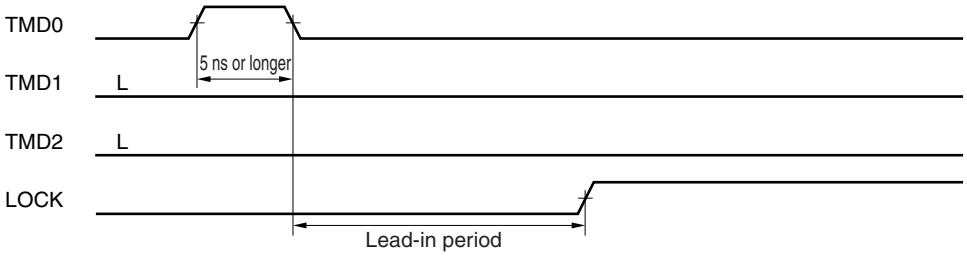
This mode is used to reset the entire digital PLL. Be sure to execute the reset mode after power application.

Although the timing of setting reset mode is not prescribed, set the reset mode for at least 5 ns.

Whether inputting RCLK or not during reset mode does not affect the operation.

The digital PLL locks within the lead-in period after reset mode is released.

[Waveform at reset mode]

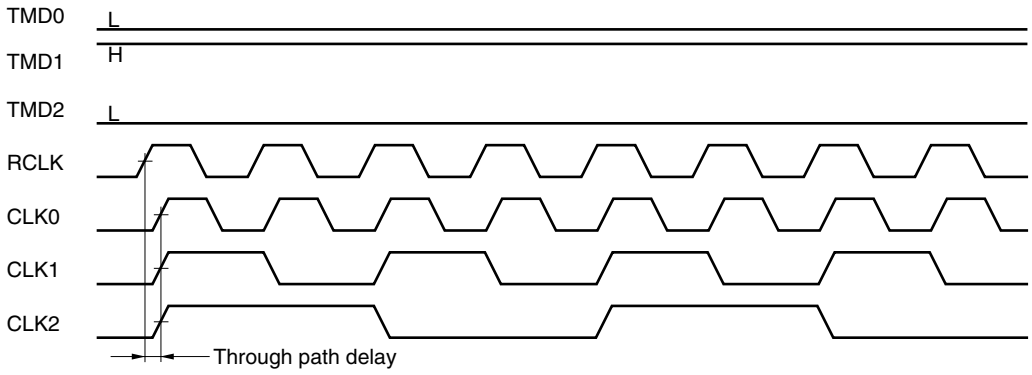


(c) Through path mode

This mode is used to test the user circuit that is placed in the stage following the digital PLL. CLK0 is output later than RCLK by the amount of through path delay (In through path mode, RCLK = CLK0 regardless the multiplication factor).

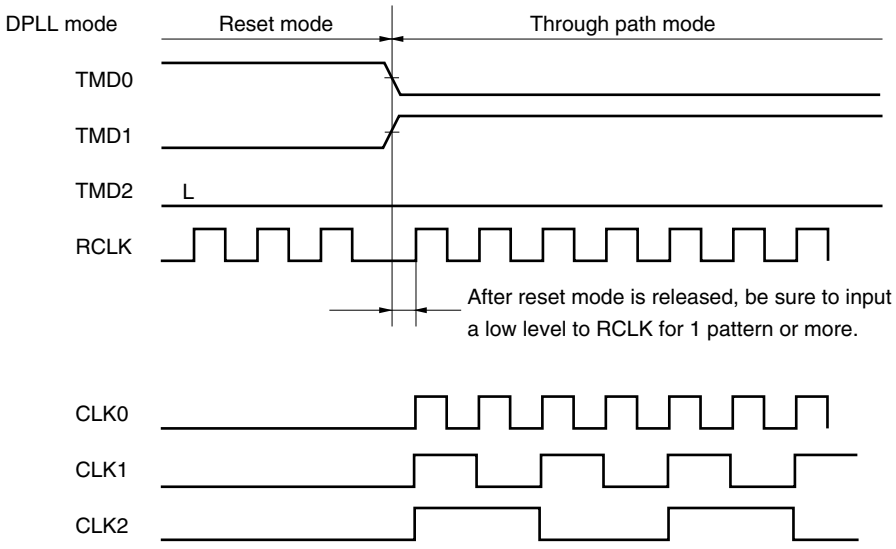
The delay time in the AC ratings does not include the delay value of the clock tree, etc.

[Waveform of through path output]



- **Caution when setting the F9H2 type to through path mode**

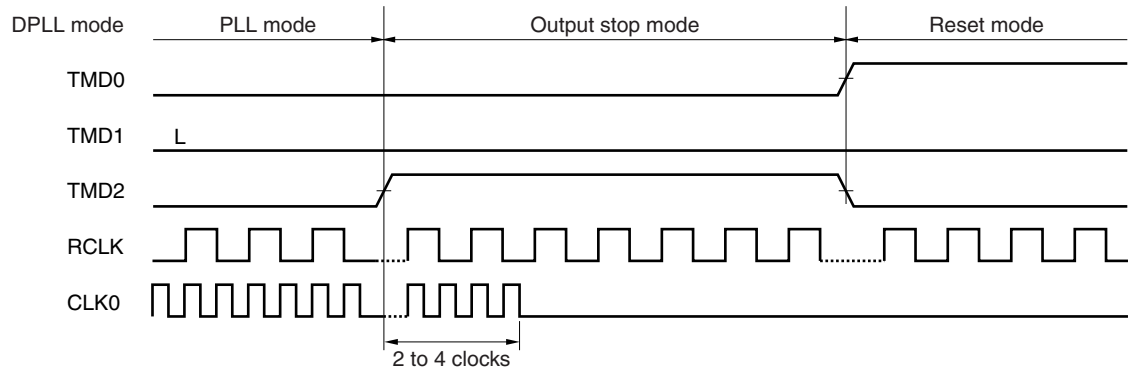
Always set through path mode from reset mode.



(d) Output stop mode

This mode is used to fix the CLK0 output to low. When 2 to 4 clocks have elapsed after the output stop mode is set, CLK0 is fixed to low level without generating a spike.

Although the timing of setting stop mode is not prescribed, be sure to execute the reset mode after the output stop mode is released.



(4) Connection rules

- The external input buffer FI0P or FI0Q must be used for RCLK input. Use FI0P for the 3 V interface and FI0Q for the 5 V interface.
- Allocate the digital PLL at the corner (any of the four corners is acceptable).
- Do not place RAM or ROM near the digital PLL.
- Place GNDs for both pins next to the pin at which RCLK is placed.
- Place additional GNDs to reduce external buffer noise and do not place a high driving buffer (e.g. GTL+) near the digital PLL.
- Be sure to connect a clock driver or CTS to the CLK0 to CLK02 outputs, and either of the outputs to the CLKI input of the digital PLL (F9H2) (unused CLKn outputs can be left open). However, when the output of CLKn is divided by a F/F, etc., do not connect the divided output to the CLKI input of the digital PLL (F9H2).
- Connect Schmitt buffers to directly input TMD0 to TMD2 from external pins.
  Make sure that no spike noise is input to the TMD0 to TMD2 pins.
- Because the digital PLL (F9H2) is tested as a standalone unit, design the connection so that pins other than CLKI, SEL0 to SEL2 and CLK0 to CLK2 can be input/output from an external pin (TCK0, TCK1, TSMI, TSEL0 to TSEL3, TFSEL0 and TFSEL1 can be shared with another external pin).
  RCLK, TCK0, and TCK1 cannot be shared by using a bidirectional buffer.
- Set the reset mode for at least 5 ns.
- After power application, release the reset mode when the power supply voltage, input clock pulse width, duty, and frequency are stabilized at 3.3 ±0.3 V, 2.8 ns or more, 50 ±5%, and ±1 ns of the frequency to be used, respectively.
- Be sure to execute the reset mode when the output stop mode is released.
- Perform a test in the through path mode before executing simulation.
- The waveform of the CLK1 output is equal to 1/2 the CLK0 output waveform.
- The waveform of the CLK2 output is equal to 1/4 the CLK0 output waveform.
- In PLL mode, the output clock is unstable until the digital PLL (F9H2) locks (TOUT changes from L to H). Consequently, operation cannot be guaranteed.
- After reset mode is released, be sure to input a ±1 ns cyclic variation with a 2.8 ns or longer pulse width at a duty of 50 ±5%. If an unstable clock exceeding this range is input to RCLK, the PLL is automatically shifted to reset mode, and the output clock may be unstable until the PLL locks.
- Be sure to execute the reset mode when the multiplication factor is changed.

- When reset mode is set or released, spike noise may be generated at the output clock.
- Supply the power supply voltage within the specifications (3.3 ±0.3 V) so that the fluctuation of the power supply caused by noise is 600 mV (peak-to-peak) or less.
  The correct operation of the digital PLL (F9H2) cannot be guaranteed if the fluctuation of the power supply caused by noise exceeds 600 mV.
- Supply the power supply voltage within the specifications (3.3 ±0.3 V) so that the fluctuation of the power supply caused by noise is 300 mV (peak-to-peak) or less.
  If the fluctuation of the power supply caused by noise is 300 to 600 mV, calculate the jitter using the following formula.
  Jitter [ps] = fluctuation of the power supply [mV] × 2 [ps/mV]
  The correct operation of the digital PLL (F9H2) cannot be guaranteed if the fluctuation of the power supply caused by noise is 600 mV or more.
- A special request is needed when a circuit (e.g. power-on-reset circuit) is placed between an input buffer and TMD0 to TMD2.
- Cautions on setting feedback clocks
  - Be sure to connect CTS to the CLK0 to CLK2 outputs, and that output to the CLKI input of the digital PLL (F9H2).
  - Do not divide outputs such as CLK0 by a F/F or input a divided output to CLKI.
  - Feed back a clock to the CLKI input that is an integral multiple of the reference clock.
  - Do not feed back a clock to the CLKI input that has a frequency lower than the reference clock[Note].

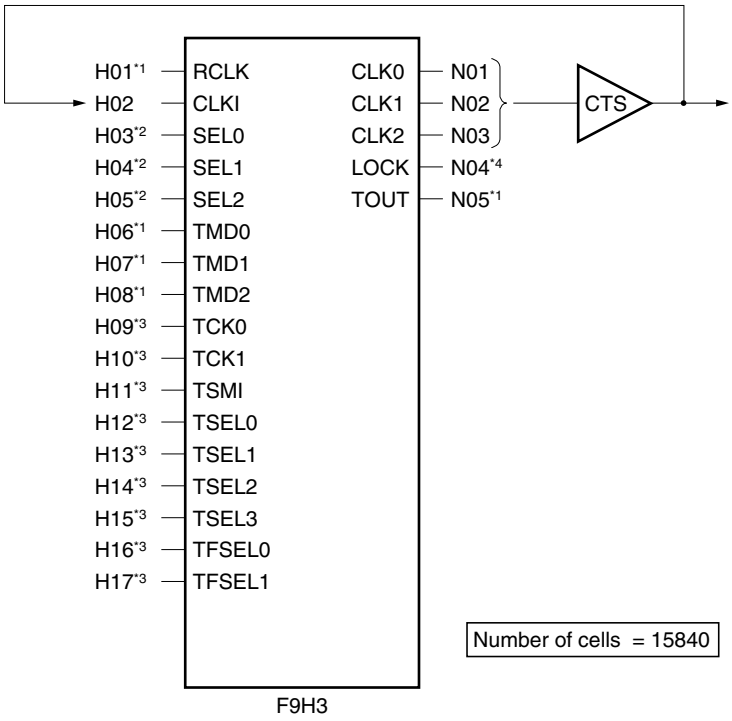
Note The feedback clock cannot be used in such a way that CLK1 is fed back in the ×3 multiplication mode, or CLK2 is fed back in the ×2 multiplication mode.

7.6.3 Digital PLL (F9H3)

(1) Function and operation mode

This section explains the functions and operation modes of the multiplication digital PLL (F9H3).

Figure 7-23. Digital PLL Connection Example (F9H3)



Caution 1. Pins marked *1 cannot be shared with other LSI pins (dedicated pins).

Caution 2. Pins marked *2 do not need to be connected with external pins.

Caution 3. Pins marked *3 can be shared with other LSI pins.

Caution 4. Pins marked *4 do not need to be connected with external pins.

Caution 5. Be sure to connect one of the CLK0 to CLK2 outputs to the CLKI input. (Never divide the outputs by a F/F or input a divided output to CLKI.) If multiple CLKn are used, the phases are not synchronized.

(a) Pin function list

Pin Name	Signal Name	Attribute	Function
H01	RCLK	IN	Reference clock signal
H02	CLKI	IN	Feedback clock signal
H03	SEL0	IN	Multiplication factor setting signal
H04	SEL1	IN	
H05	SEL2	IN	
H06	TMD0	IN	Test mode select signal
H07	TMD1	IN	
H08	TMD2	IN	
H09	TCK0	IN	Test mode clock input signal
H10	TCK1	IN	
H11	TSMI	IN	Test mode switching signal
H12	TSEL0	IN	Test mode multiplication factor setting signal
H13	TSEL1	IN	
H14	TSEL2	IN	
H15	TSEL3	IN	
H16	TFSEL0	IN	Test mode setting signal
H17	TFSEL1	IN	
N01	CLK0	OUT	Multiplication clock output signal
N02	CLK1	OUT	Multiplication clock output signal (2-division output)
N03	CLK2	OUT	Multiplication clock output signal (4-division output)
N04	LOCK	OUT	Lock signal
N05	TOUT	OUT	NEC test mode output signal

(b) Operation truth table

RCLK	TCKn	SELn	TSELn	TFSEL1	TFSEL0	TMD2	TMD1	TMD0	TSMI	CLKn	LOCK	TOUT	Mode
A	X	○	X	X	X	0	0	0	X	A	LOCK[Note 1]	0	PLL mode[Note 2]
X	X	○	X	X	X	0	X	1	X	0	0	0	Reset mode
A	X	○	X	X	X	0	1	0	X	A	0	0	Through path mode[Note 3]
X	X	○	X	X	X	1	0	0	X	0	0	0	Stop mode
A	○	X	○	0	0	1	0	1	○	0	X	TEST	NEC test mode
A	○	X	○	0	1	1	0	1	○	0	X	TEST	
A	○	X	○	1	0	1	0	1	○	0	X	TEST	
A	○	X	○	1	1	1	0	1	○	0	X	TEST	
A	○	X	○	0	0	1	1	0	○	0	X	TEST	
A	○	X	○	0	1	1	1	0	○	0	X	TEST	
A	○	X	○	1	0	1	1	0	○	0	X	TEST	
A	○	X	○	1	1	1	1	0	○	0	X	TEST	
A	○	X	○	0	0	1	1	1	○	0	X	TEST	
A	○	X	○	0	1	1	1	1	○	0	X	TEST	
A	○	X	○	1	0	1	1	1	○	0	X	TEST	
A	○	X	○	1	1	1	1	1	○	0	X	TEST	

Note 1. This is 1 when the phase is locked (when the phase of RCLK and CLKI is synchronized).

Note 2. Multiplied A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

Note 3. A is output to CLK0, 1/2 CLK0 is output to CLK1, and 1/4 CLK0 is output to CLK2.

Remark A, ○: Indicates that the selected mode can be used.

Reset mode setting

Set reset mode by setting TMD2 = 0, TMD1 = X, and TMD0 = 1 (X is either 0 or 1). To change the reset mode to PLL mode, set TMD (2:0) as follows.

Reset mode

TMD2	TMD1	TMD0
0	0	1

⇨

PLL mode

TMD2	TMD1	TMD0
0	0	0

To change the reset mode to through path mode, set TMD (2:0) as follows.

Reset mode

TMD2	TMD1	TMD0
0	1	1

⇨

Through path mode

TMD2	TMD1	TMD0
0	1	0

By setting as shown above, only one pin needs to be used to change the mode.

(c) Multiplication factor settings

Set the multiplication factor by SELn (SELn can also be clamped to F091).

Multiplication factor	SEL2	SEL1	SEL0	Usable Frequency Band (RCLK)
1	0	0	0	25 to 100 MHz
2	0	0	1	25 to 100 MHz
3	0	1	0	25 to 66.6 MHz
4	0	1	1	25 to 50 MHz
5	1	0	0	25 to 40 MHz
6	1	0	1	25 to 33.3 MHz
7	1	1	0	25 to 28.5 MHz
8	1	1	1	25 MHz

Caution Can only be used within the above shown frequency band; other frequencies cannot be used.

(2) Electrical specifications

The electrical specifications of the digital PLL (F9H3) are shown in Table 7-9.

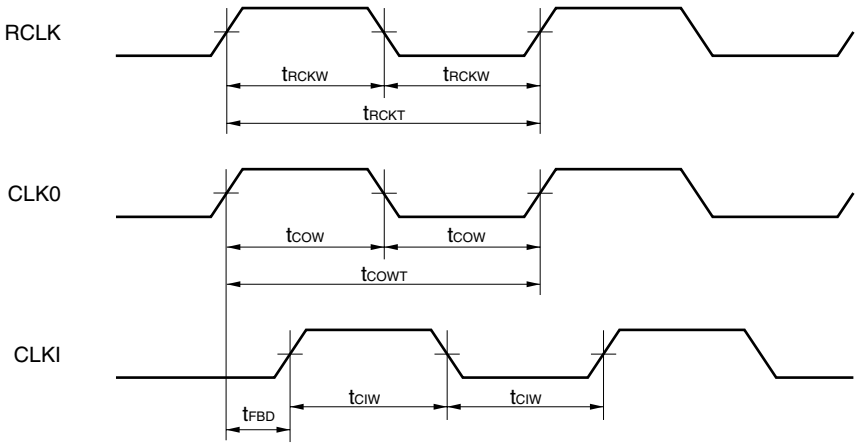
Table 7-9. AC Characteristics (F9H3)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
RCLK frequency	t_{RCKT}	25.0		100.0	MHz	When × 1 is set
		25.0		100.0	MHz	When × 2 is set
		25.0		66.6	MHz	When × 3 is set
		25.0		50.0	MHz	When × 4 is set
		25.0		40.0	MHz	When × 5 is set
		25.0		33.3	MHz	When × 6 is set
		25.0		28.5	MHz	When × 7 is set
		25.0		–	MHz	When × 8 is set
RCLK input allowable jitter	t_{RCKJ}			700	ps	
Power supply allowable fluctuation width				V_{DD} ±0.3	V	Peak-to-peak
Input duty	t_{CIW}			50 ±5	%	
RCLK pulse width	t_{RCKW}	2.8			ns	
CLKI pulse width	t_{SIW}	2.0			ns	
Output jitter	t_{JITT}			600[Note]	ps	Fluctuation of the power supply caused by noise: 200 mV (peak-to-peak) or less
Output duty	t_{COW}	45		55	%	
Through path mode delay	t_{THR}	0.886		1.958	ns	CLK0 output
	t_{THL}	0.893		1.979	ns	CLK0 output
	t_{THR}	0.845		1.853	ns	CLK1 output
	t_{THL}	0.845		1.909	ns	CLK1 output
	t_{THR}	0.845		1.853	ns	CLK2 output
	t_{THL}	0.845		1.909	ns	CLK2 output
CTS delay restriction	t_{FBD}			8.22	ns	
Lead-in time	t_{LOCK}			2116	RCLK	
Steady phase error	t_{OFF}			±0.1	ns	No input jitter
Reset pulse width	t_{RSTW}	5			ns	
Output stop time	t_{STOP}	2		4	t_{COW}	
Power consumption	P_{PLL}		50		mW	

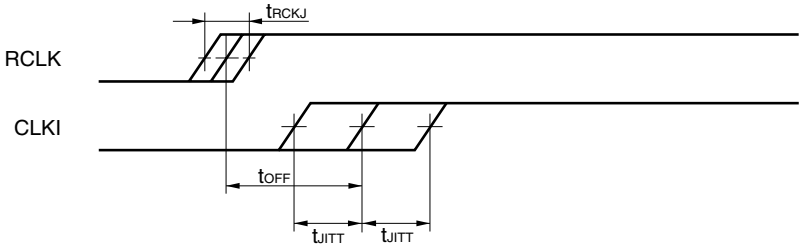
Note The output jitter when the input jitter is 80 ps or less

If the input jitter exceeds 80 ps, add the input jitter to the output jitter value.

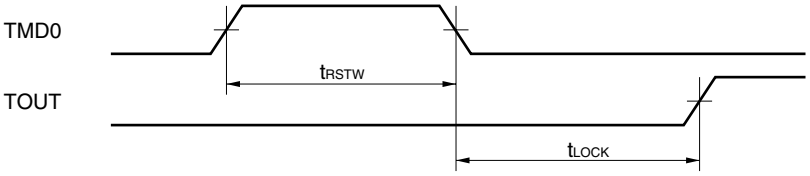
- **Input and output waveforms**



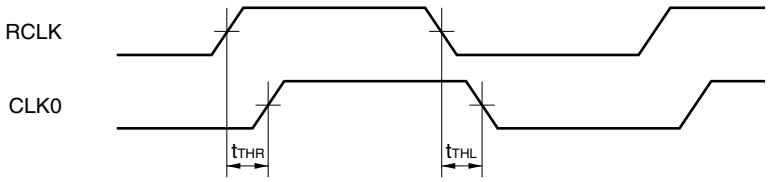
- **Jitter and steady phase error**



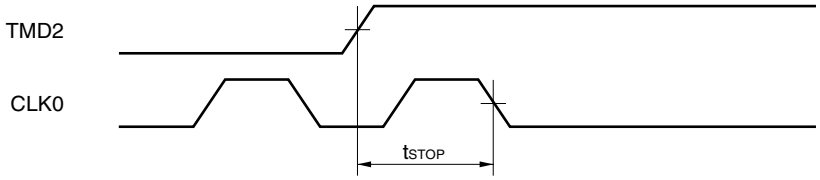
- **Lead-in time and reset mode**



- **Through path mode**



- **Output stop mode**

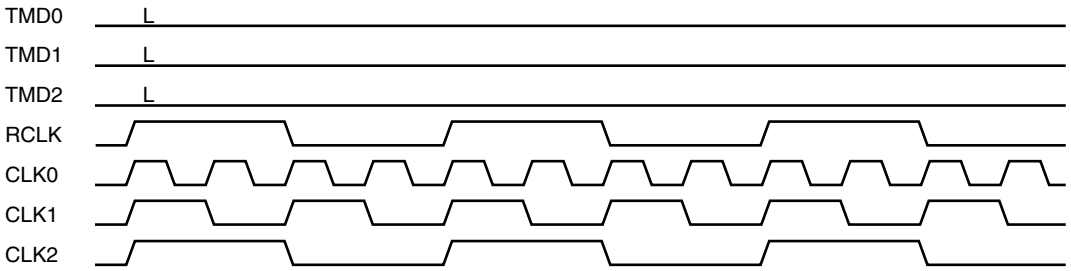


(3) Digital PLL operation

(a) PLL mode

In this mode, the phase of RCLK is synchronized with the phase of CLKn, and the clock set by the multiplication factor setting signal (SELn) is output.

[Waveform when x4 is set in PLL mode]



(b) Reset mode

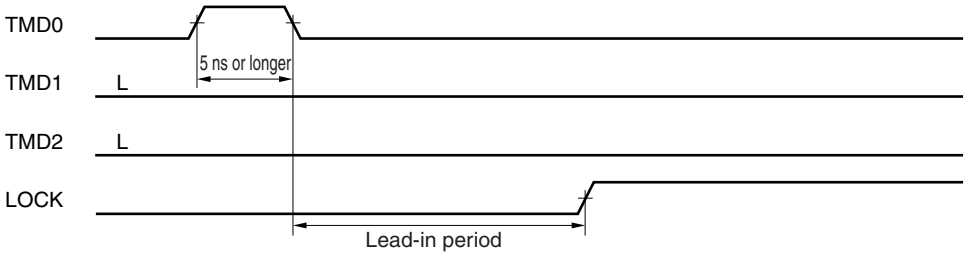
This mode is used to reset the entire digital PLL. Be sure to execute the reset mode after power application.

Although the timing of setting reset mode is not prescribed, set the reset mode for at least 5 ns.

Whether inputting RCLK or not during reset mode does not affect the operation.

The digital PLL locks within the lead-in period after reset mode is released.

[Waveform at reset mode]

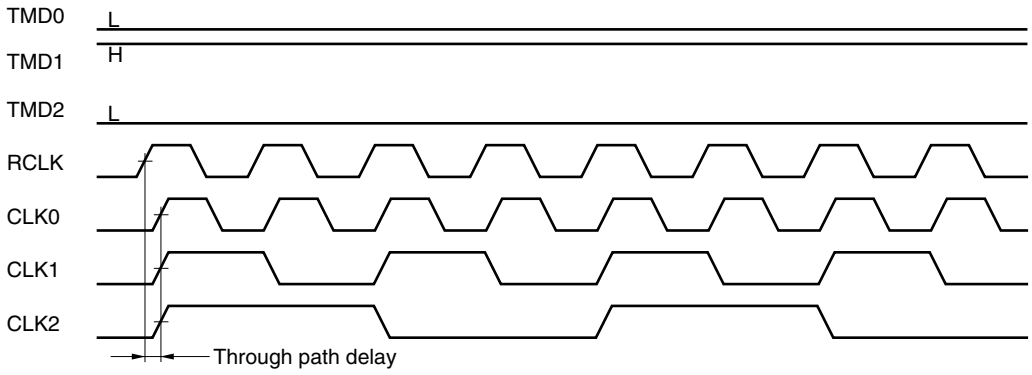


(c) Through path mode

This mode is used to test the user circuit that is placed in the stage following the digital PLL. CLK0 is output later than RCLK by the amount of through path delay (In through path mode, RCLK = CLK0 regardless the multiplication factor).

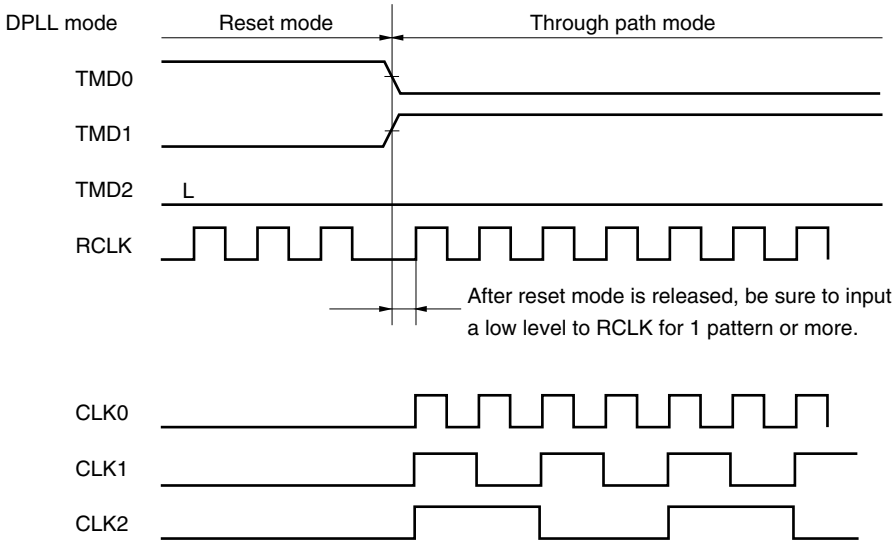
The delay time in the AC ratings does not include the delay value of the clock tree, etc.

[Waveform of through path output]



- **Caution when setting the F9H3 type to through path mode**

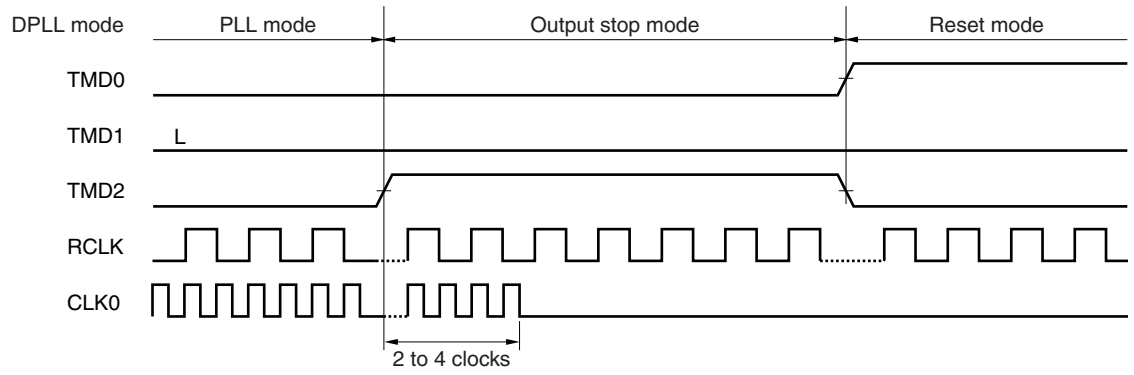
Always set through path mode from reset mode.



(d) Output stop mode

This mode is used to fix the CLK0 output to low. When 2 to 4 clocks have elapsed after the output stop mode is set, CLK0 is fixed to low level without generating a spike.

Although the timing of setting stop mode is not prescribed, be sure to execute the reset mode after the output stop mode is released.



(4) Connection rules

- Be sure to set through path mode and confirm the connection before executing simulation. Take care with the setting and connection of each pin since this is not simulation under the actual usage conditions.
- The external input buffer FI0P or FI0Q must be used for RCLK input. Use FI0P for the 3 V interface and FI0Q for the 5 V interface.
- Make sure that no spike noise is input to the RCLK, TMD0 to TMD2 input pins.
- Allocate the digital PLL at the corner (any of the four corners is acceptable).
- Do not place RAM or ROM near the digital PLL.
- Place GNDs for both pins next to the pin at which RCLK is placed.
- Place additional GNDs to reduce external buffer noise and do not place a high driving buffer (e.g. GTL+) near the digital PLL.
- Be sure to connect a clock driver or CTS to the CLK0 to CLK02 outputs, and either of the outputs to the CLKI input of the digital PLL (F9H3) (unused CLKn outputs can be left open). However, when the output of CLKn is divided by a F/F, etc., do not connect the divided output to the CLKI input of the digital PLL (F9H3).
- Feed back a clock that is an integral multiple of the reference clock to the CLKI input. Do not feed back a clock to the CLKI input that has a frequency lower than the reference clock.
- Connect Schmitt buffers to directly input TMD0 to TMD2 from external pins.
  Make sure that no spike noise is input to the TMD0 to TMD2 pins.
- Because the digital PLL (F9H3) is tested as a standalone unit, design the connection so that pins other than CLKI, SEL0 to SEL2 and CLK0 to CLK2 can be input/output from an external pin (TCK0, TCK1, TSEL0 to TSEL3, TFSEL0 and TFSEL1 can be shared with another external pin).
  RCLK, TCK0, and TCK1 cannot be shared by using a bidirectional buffer.
- The output clock cannot be guaranteed if any of the following conditions apply. Be sure to execute the reset mode.
  - After power application
  - Power supply is out of the rated range (3.3 ±0.3 V)
  - When mode is shifted between PLL mode, through path mode, and output STOP mode
  - When the multiplication factor setting (SELn) is changed
  - When the input AC ratings in **Table 7-9 AC Characteristics (F9H3)** are not satisfied
- Set the reset mode for at least 5 ns.

- After power application, release the reset mode when the power supply voltage, input clock pulse width, duty, and frequency are stabilized at 3.3 ±0.3 V, 2.8 ns or more, 50 ±5%, and ±0.5 ns of the frequency to be used, respectively.
- Be sure to execute the reset mode when the output stop mode is released.
- The waveform of the CLK1 output is equal to 1/2 the CLK0 output waveform.
- The waveform of the CLK2 output is equal to 1/4 the CLK0 output waveform.
- In PLL mode, the output clock is unstable until the digital PLL (F9H3) locks (TOUT changes from L to H). Consequently, operation cannot be guaranteed.
- Supply the power supply voltage within the specifications (3.3 ±0.3 V) so that the fluctuation of the power supply caused by noise is 200 mV (peak-to-peak) or less.
  Attach a bypass capacitor of 22 μF or more between V_{DD} and GND for the power supply block on a board on which an LSI is mounted.
- After reset mode is released, be sure to input a ±0.5 ns cyclic variation with a 2.8 ns or longer pulse width at a duty of 50 ±5%. If an unstable clock exceeding this range is input to RCLK, the PLL is automatically shifted to reset mode, and the output clock may be unstable until the PLL locks.
- When reset mode is set or released, spike noise may be generated at the output clock.
- A special request is needed when a circuit (e.g. power-on-reset circuit) is placed between an input buffer and TMD0 to TMD2.
- The output clock cannot be guaranteed if RCLK stops. Be sure to input RCLK continuously.
- Cautions on setting feedback clocks
  - Be sure to connect CTS to the CLK0 to CLK2 outputs, and that output to the CLKI input of the digital PLL (F9H3).
  - Do not divide outputs such as CLK0 by a F/F or input a divided output to CLKI.
  - Feed back a clock to the CLKI input that is an integral multiple of the reference clock.
  - Do not feed back a clock to the CLKI input that has a frequency lower than the reference clock[Note].

Note The feedback clock cannot be used in such a way that CLK1 is fed back in the ×3 multiplication mode, or CLK2 is fed back in the ×2 multiplication mode.

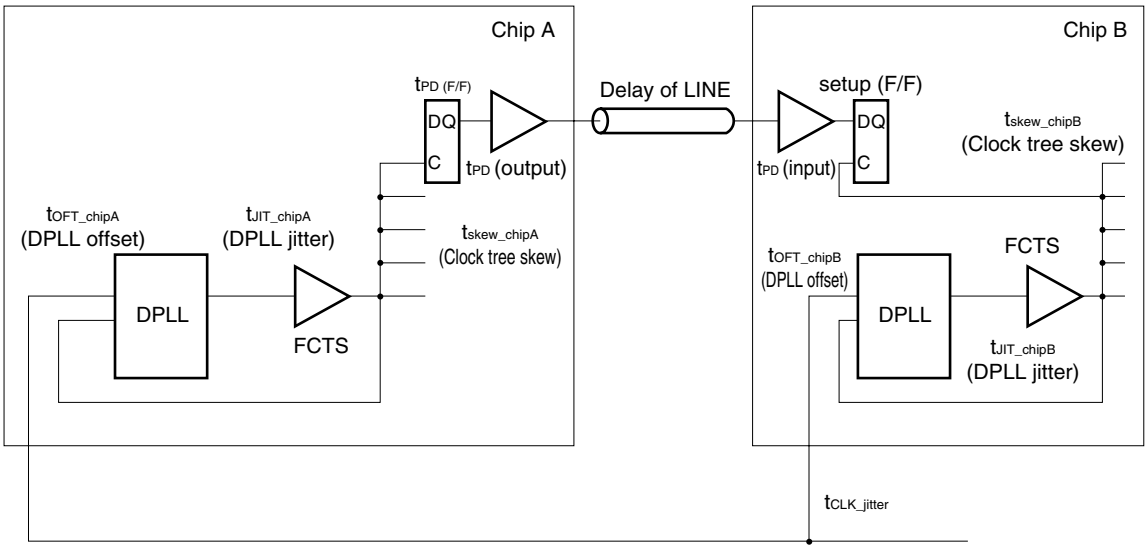
7.6.4 Signal transfer between devices

When signals are transmitted between devices with an on-board digital PLL, the maximum operating frequency is determined by taking the clock skew and jitter into consideration. This section explains the calculation of the maximum operating frequency. If shift registers are configured between devices, as shown in the circuit in Figure 7-24, the minimum period of the clock signal is expressed as follows:

Calculation equation:

$$T_{CLK} = t_{CLK\_jitter} + 0.5 \times t_{JIT\_chipA} + 0.5 \times t_{skew\_chipA} + t_{PD}\ (F/F) + t_{PD}\ (output) + \text{delay of LINE} + t_{PD}\ (input) + \text{setup (F/F)} + 0.5 \times t_{JIT\_chipB} + 0.5 \times t_{skew\_chipB} + t_{OFT\_chipA} + t_{OFT\_chipB}$$

Figure 7-24. Signal Transfer Between Devices



Remark DPLL: Digital PLL

7.6.5 Creating test pattern

The PLL operation cannot be reproduced by normal delay simulation. For shipment inspection of gate arrays with a digital PLL, therefore, the operations of the circuits other than the digital PLL are checked with the digital PLL bypassed, and the operation of the digital PLL is checked separately. The test pattern for the digital PLL is prepared by NEC Electronics. The user is requested to observe the connection rules of the digital PLL and notes on creating the test pattern.

Be sure to inform NEC Electronics of the names of the pins to which the digital PLL is to be connected. NEC Electronics supplies 4 K of test patterns for checking the digital PLL. Therefore, the maximum test pattern length the user can use is the difference between the maximum test pattern length and 4 K.

The RCLK pin must not be specified as a clock pin (for the clock pin, see **CHAPTER 6 TEST PATTERN GENERATION**).

(1) Normal simulation

The signals of the TMD0, TMD1, and TMD2 pins must be as follows. The user can use these signals only in the through path and reset modes.

Operation Mode	TMD0	TMD1	TMD2
Through path	0	1	0
Reset	1	0	0

(2) Digital PLL initial pattern[Note 1]

To check the operation of the digital PLL alone, use the digital PLL test pattern file available from NEC Electronics. However, when there are gates (logic) between the digital PLL test pins and the digital PLL main unit[Note 2], the patterns for checking direct access to the digital PLL test pins and main body and the test patterns (initialization patterns) for determining the expected output values of the blocks other than the digital PLL (such as flip-flops and I/O buffers) must be prepared by the user.

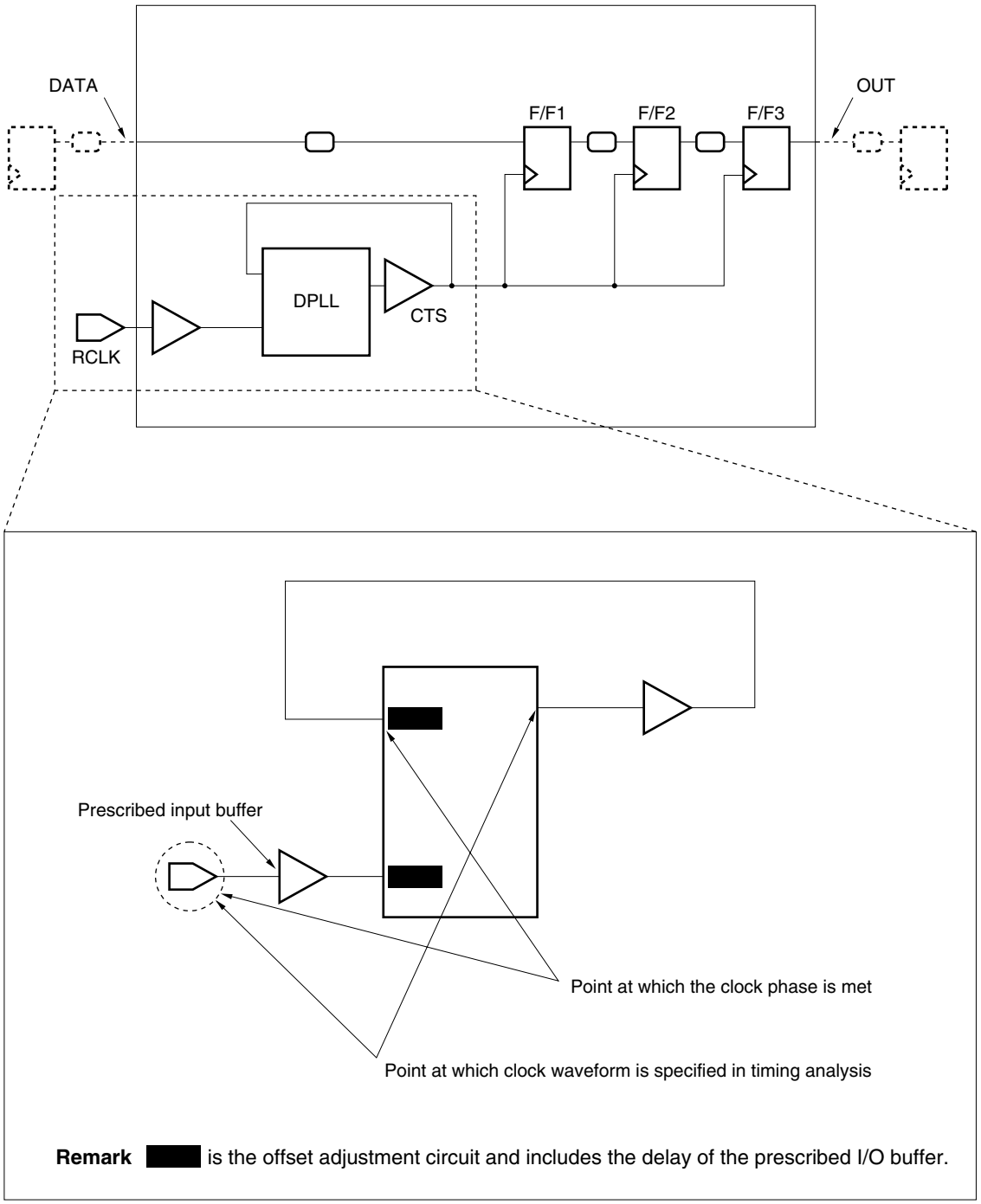
Note 1.
- Use only in the through path and reset modes.
- Ensure that only the final pattern of output buffers other than that of TOUT is “don’t care”.
- Depending on the test to be performed, RCLK is directly output to TOUT (the only monitor pin), so do not specify the RCLK pin for the clock.
- Do not describe timing relationships.

Note 2. In this case, please contact NEC Electronics.

7.6.6 Static timing analysis of circuits using digital PLL

The digital PLL STA model is currently only available for the through mode, so care is needed when verifying the timing between external inputs and flip-flops, flip-flops and flip-flops, and flip-flops and external outputs in lock mode. For details of the verification method, refer to **SYSTEM LSI DESIGN OPENCAD Static Timing Analyzer Tiara User's Manual (A16210E)**.

Figure 7-25. Example of Circuit Configuration When PLL Used



Remark ■ is the offset adjustment circuit and includes the delay of the prescribed I/O buffer.

Table 7-10. Delay Values of Digital PLL Offset Adjustment Circuit (F9E4)

Type	Maximum Delay Value
F9E4H	−580
F9E4G	−483
F9E4F	−390
F9E4E	−309
F9E4D	−233
F9E4C	−146
F9E4B	−58
F9E4A	26
F9E4I	110
F9E4J	198
F9E4K	285
F9E4L	361
F9E4M	442
F9E4N	535
F9E4O	632

Remark The unit is 1 ps/unit.

Table 7-11. Delay Values of Digital PLL Offset Adjustment Circuit (F9H2)

Type	Maximum Delay Value
F9H2O	−562
F9H2N	−466
F9H2M	−383
F9H2L	−305
F9H2K	−217
F9H2J	−125
F9H2I	−37
F9H2A	45
F9H2B	127
F9H2C	215
F9H2D	307
F9H2E	395
F9H2F	473
F9H2G	556
F9H2H	652

Remark The unit is 1 ps/unit.

Table 7-12. Delay Values of Digital PLL Offset Adjustment Circuit (F9H3)

Type	Maximum Delay Value
F9H3H	643
F9H3G	564
F9H3F	481
F9H3E	402
F9H3D	327
F9H3C	248
F9H3B	168
F9H3A	93
F9H3I	19
F9H3J	–61
F9H3K	–141
F9H3L	–215
F9H3M	–291
F9H3N	–377
F9H3O	–462

Remark The unit is 1 ps/unit.

7.7 PCI Local Bus Buffers

The PCI (Peripheral Component Interconnect) local bus is an integrated standard for local bus architecture that improves the speed of bus lines where bottlenecks would otherwise occur as signals are arbitrated between the PC and its peripheral components. Since this bus standard has signal transfers performed mainly by reflected waves, standards must be specified for a wide array of factors, including not only the bus protocol but also the bus driver's electrical specifications, the types of wire patterns and connectors used on the PC board, and even the shape of the PC board.

This section describes the CMOS-9HD Series type bus driver that complies with PCI LOCAL BUS SPECIFICATION REVISION 2.0/3 V.

Before creating PCI components for the CMOS-9HD Series, be sure to join the "PCI Special Interest Group" (PCISIG) since vendor ID and specific support will be needed.

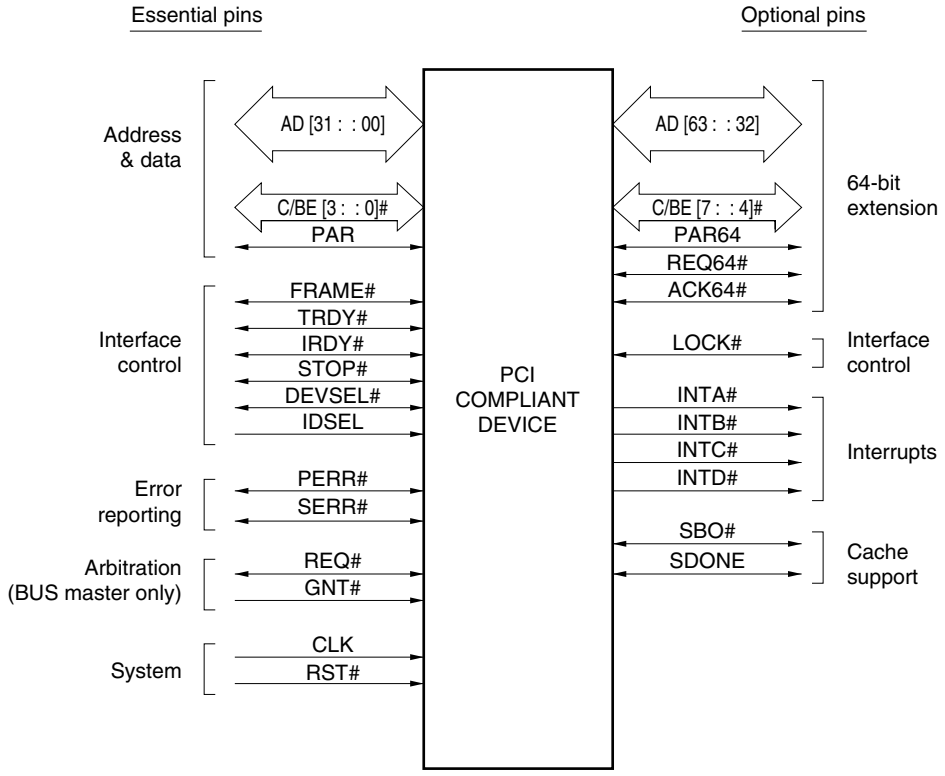
Specifications (standards) and other important documents can also be obtained from the PCISIG.

7.7.1 Signal specification of PCI local bus

The PCI interface requires that the target device have at least 47 pins that can be used as signal pins and that the bus master have at least 49 pins that can be used as signal pins in order to support implementation of an address/data line, interface control line, system signal line, and arbitration control line.

The pin list for the PCI local bus is shown below. For block list, refer to Table 7-13.

Figure 7-26. PCI Pin List



Remark The distance between each signal pin on the PCI local bus and the bus is specified. Therefore, it is recommended to place signal pins on one edge of the chip.

Table 7-13. PCI Blocks

(a) Blocks for 3.3 V PCI

3.3 V PCI Bus Driver	Full-Type	Half-Type
Input	BP3I	
Output	BP3O	FO01
Three-state	BP3T	B008
Bidirectional	BP3B	B003
Open-drain	EXT5	

(b) Blocks for 5 V PCI

5 V PCI Bus Driver	Full-Type
Input	BP5I
Output	BP5O
Three-state	BP5T
Bidirectional	BP5B

Remark Full type: Blocks used with pin-to-bus (1-to-multiple)
Half type: Blocks used with pin-to-pin (1-to-1)

Notes on using 5 V PCI

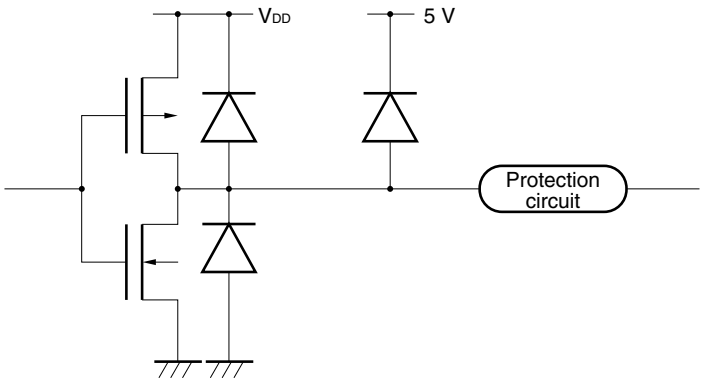
The 5 V PCI buffer has a clamping diode to protect the device from a reflection wave of 11 V (see **Figure 7-27 Equivalent Circuit Diagram of 5 V PCI Buffer**).
When using this buffer, therefore, a dedicated 5 V power supply pin for the clamping diode needs to be added.

The 5 V power supply is an additional power supply, and at least one must be located on the side of the chip on which the PCI buffer is located.
An additional 5 V power supply pin can be located anywhere on the side on which the PCI buffer is located.

- Even if there are several PCI buffers on a side, at least one additional 5 V power supply can be located on that side (more than one is also possible).
- When there is a PCI buffer located on every side, a total of at least four additional 5 V power supply pins can be located; one (or more) on each side.

Caution The addition of a power supply is not related to reinforcing the power supply to prevent simultaneous switching.

Figure 7-27. Equivalent Circuit Diagram of 5 V PCI Buffer



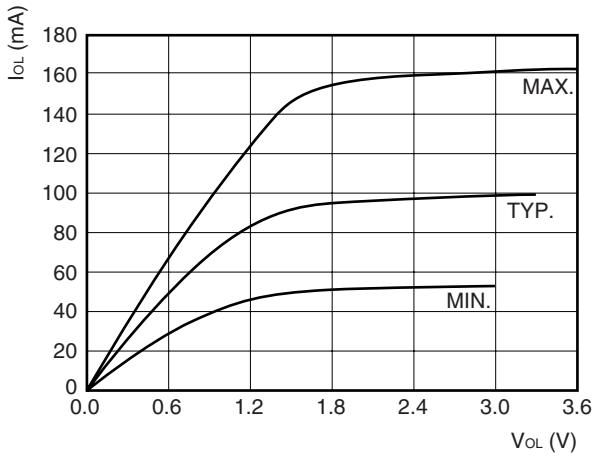
7.7.2 Output current of output buffer

The curve of I_O vs. V_O is shown in **Figure 7-28**.

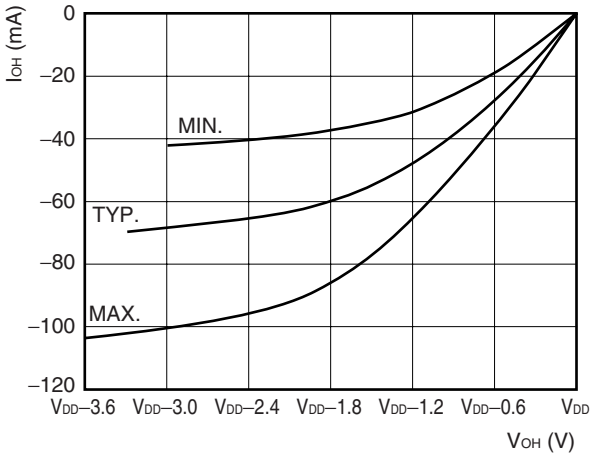
Figure 7-28. I_O vs. V_O (PCI Buffer)

(1) 3.3 V PCI buffer

(a) I_{OL} vs. V_{OL}

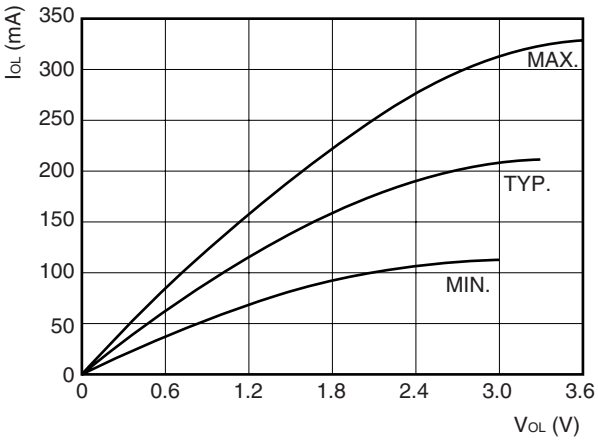


(b) I_{OH} vs. V_{OH}

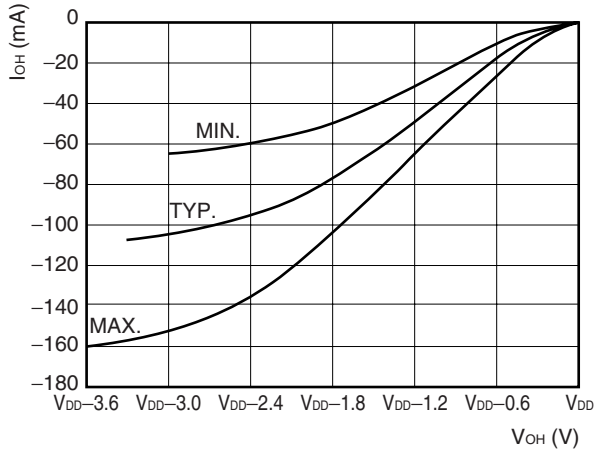


(2) 5 V PCI buffer

(a) I_{OL} vs. V_{OL}



(b) I_{OH} vs. V_{OH}



7.7.3 Electrical specifications

To use the PCI buffer, signal flow in the transmission path must be evaluated in advance. It requires some know-how to do this.

The DC characteristics and pin capacitance, etc. complies with PCI LOCAL BUS SPECIFICATION REVISION 2.0/3 V.

7.8 Memory

In the CMOS-9HD Series, the memory block can be included. This section explains the types of memory blocks and the points to be noted in using the memory blocks.

7.8.1 Memory blocks

The memory blocks shown in Table 7-14 are provided for the CMOS-9HD Series.

Multiple memory blocks can be mixed together.

Compiled RAM is also available.

Table 7-14. List of Memory Blocks

(a) High-density single-port RAM

	16	32	64	128	256	512	1024	2048	4096 [Word]
4	RB47	RB49	RB4B	RB4D	RB4F	RB4H	RB4M	RB4S	RB4U
8	RB87	RB89	RB8B	RB8D	RB8F	RB8H	RB8M	RB8S	
10			RBAB	RBAD	RBAF	RBAH	RBAM	RBAS	
16	RBC7	RBC9	RBCB	RBCD	RBCF	RBCH	RBCM		
20			RBEB	RBED	RBEF	RBEH	RBEM		
32	RBH7	RBH9	RBHB	RBHD	RBHF	RBHH			
40 [Bit]			RBKB	RBKD	RBKF	RBKH			

(b) High-density dual-port RAM

	16	32	64	128	256	512	1024	2048	4096 [Word]
4	R947	R949	R949	R94D	R94F	R94H	R94M	R94S	R94U
8	R987	R989	R989	R98D	R98F	R98H	R98M	R98S	
10			R9A9	R9AD	R9AF	R9AH	R9AM	R9AS	
16	R9C7	R9C9	R9C9	R9CD	R9CF	R9CH	R9CM		
20			R9E9	R9ED	R9EF	R9EH	R9EM		
32	R9H7	R9H9	R9H9	R9HD	R9HF	R9HH			
40 [Bit]			R9K9	R9KD	R9KF	R9KH			

(c) ROM

	128	256	512	1024	2048 [Word]
4	J14DK	J14FK	J14HK	J14MK	J14SK
8	J18DK	J18FK	J18HK	J18MK	J18SK
16	J1CDK	J1CFK	J1CHK	J1CMK	J1CSK
32 [Bit]		J1HFK	J1HHK	J1HMK	J1HSK

7.8.2 Compiled RAM

Compiled RAM differs from conventional RAM in that the user can select the bit size (however, the number of words is limited by the number of bits). Because compiled RAM is implemented completely by hard macro RAM, the access speed of the RAM can be determined accurately at the design stage. The compiled RAM block names are shown below.

Block name: High-speed synchronous dual-port = WKxxxxxx
High-speed asynchronous single-port = WJxxxxxx
High-speed asynchronous dual-port = WMxxxxxx

Figures 7-29, 7-31, and 7-33 show the number of cells used vs. the total number of bits. Figures 7-30, 7-32, and 7-34 show the access time vs. the total number of bits. These values are rough estimates.

Access to the addresses outside the existing range is possible, but the output is undefined.

Figure 7-29. Total Number of Bits vs. Number of Cells Used for High-Speed Synchronous Dual-port RAM

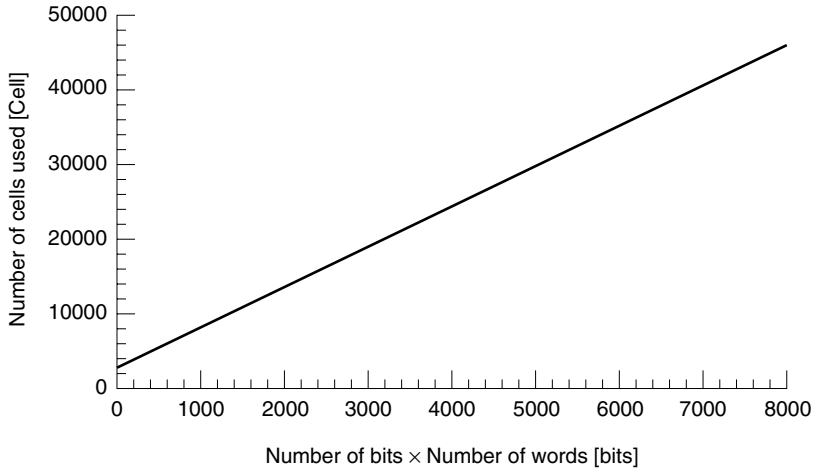
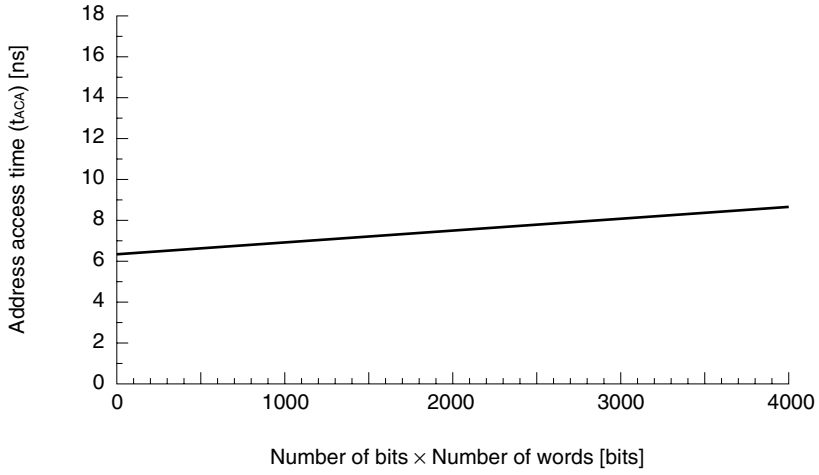


Figure 7-30. Total Number of Bits vs. Address Access Time for High-Speed Synchronous Dual-port RAM (t_{ACA})

(1) When memory ≤ 4 K



(2) When 4 K < memory ≤ 8 K

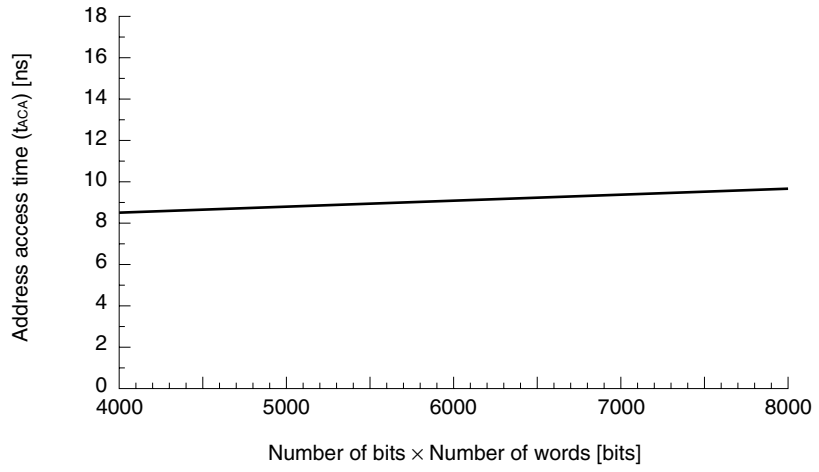


Figure 7-31. Total Number of Bits vs. Number of Cells Used for Asynchronous Single-port RAM

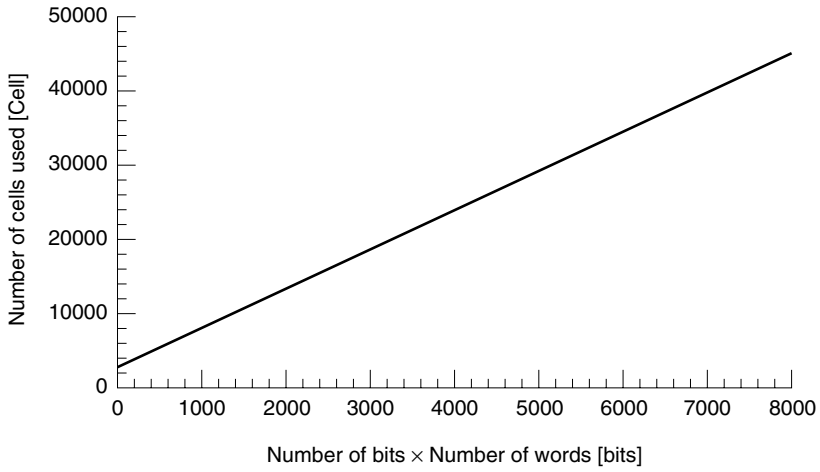
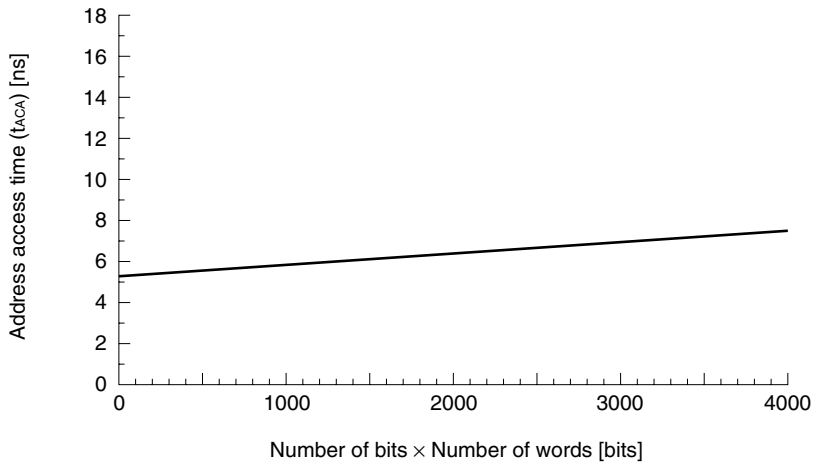


Figure 7-32. Total Number of Bits vs. Address Access Time for Asynchronous Single-port RAM (t_{ACA})

(1) When memory ≤ 4 K



(2) When 4 K < memory ≤ 8 K

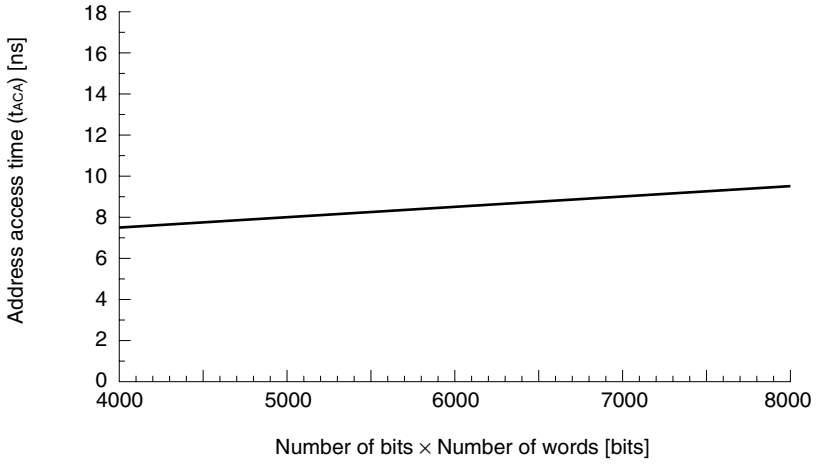


Figure 7-33. Total Number of Bits vs. Number of Cells Used for Asynchronous Dual-port RAM

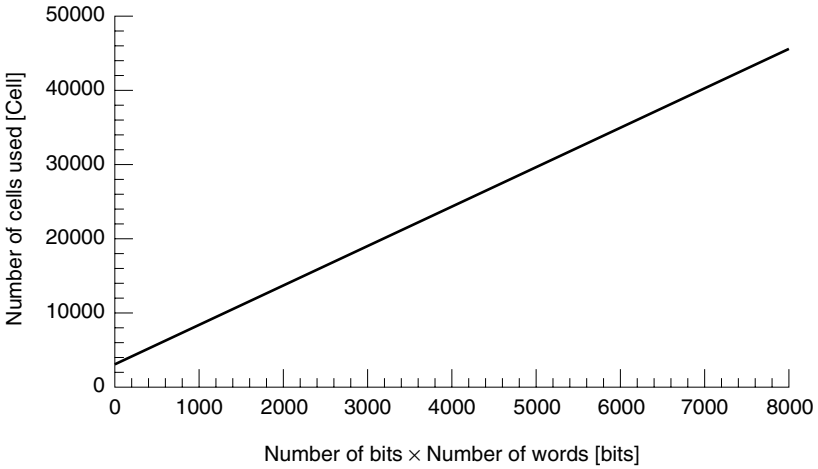
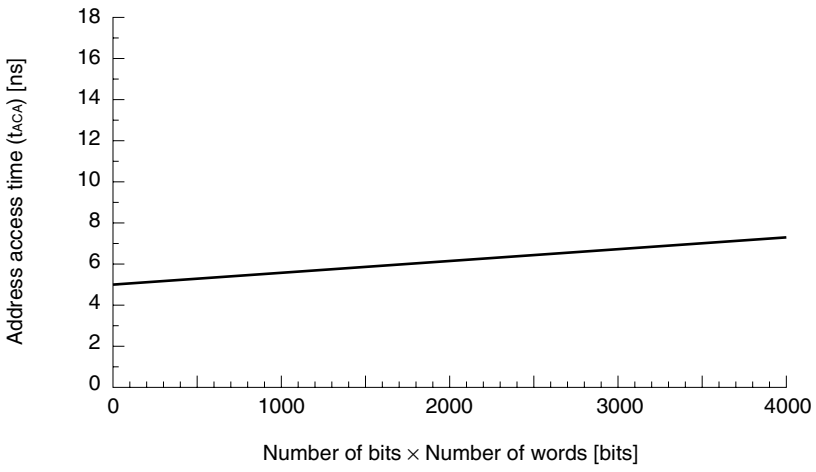
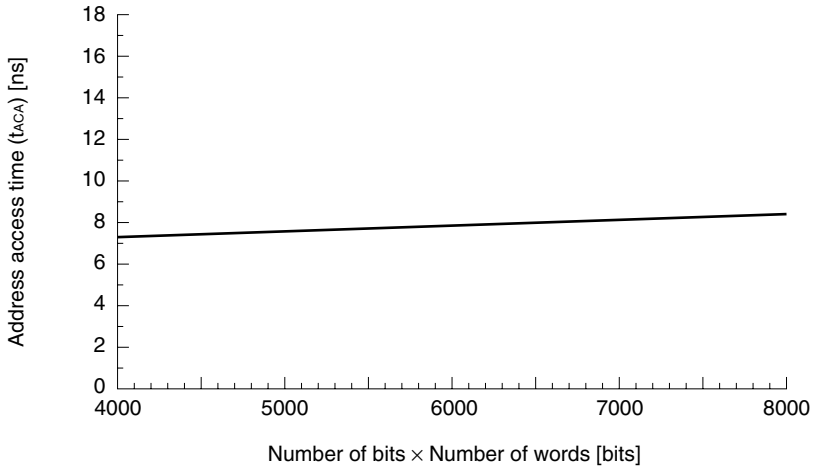


Figure 7-34. Total Number of Bits vs. Address Access Time for Asynchronous Dual-port RAM (t_{ACA})

(1) When memory ≤ 4 K



(2) When 4 K < memory ≤ 8 K



7.8.3 High-speed synchronous dual-port memory block of gate array compiled type

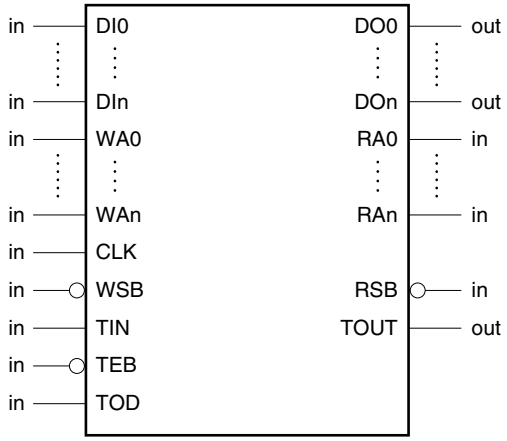
Caution This memory requires a library during layout. Please contact NEC Electronics if planning to use this memory.

(1) Compiled range

Number of words \ Number of bits	2 to 8	Up to 16	Up to 32	Up to 64	Up to 128
4 to 64	√	√	√	√	√
Up to 128	√	√	√	√	×
Up to 256	√	√	√	×	×
Up to 512	√	√	×	×	×
Up to 1024	√	×	×	×	×

Remark An odd number of bits is possible, providing the number is within the allowable range. Only realizable when the total number of words is an even number.

(2) Symbol diagram



(3) Pin function list

Symbol Name	Pin Attribute	Pin Function
DI (n:0)	Input	Data input
WA (n:0)	Input	Write address input
RA (n:0)	Input	Read address input
CLK	Input	Clock input
WSB	Input	Write select input
RSB	Input	Read select input
TIN	Input	Test clock input
TEB	Input	Test enable input
TOD	Input	DO pin disable input
DO (n:0)	Output	Data output
TOUT	Output	Test output

(4) Operation truth table

TOD	TEB[Note]	TIN	CLK	DIn	WAn	WSB	DMn	RAn	RSB	DOn	TOUT	Operation
0	1	X	↑	DIn	WAn	0	DIn (WAn)	X	1	0	X	Write
0	1	X	↑	DIn	WAn (≠RAn)	0	DIn (WAn)	RAn (≠WAn)	0	DMn (RAn)	X	Write, Read
0	1	X	↑	DIn	WAn (=RAn)	0	X	RAn (=WAn)	0	X	X	Prohibit
0	1	X	↑	X	X	1	Hold	RAn	0	DMn (RAn)	X	Read
0	1	X	X	X	X	1	Hold	X	1	0	X	Hold
0	1	X	↓, 0, 1	X	X	X	Hold	X	1	0	X	Hold
0	1	X	↓, 0, 1	X	X	X	Hold	X	0	Hold	X	Hold
0	0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode
1	X	X	X	X	X	X	X	X	X	0	X	Test Mode

Note TEB = 0 is test mode.

Remark DIn: Input data
DOn: Output data
DMn: Memory data
CLK: Clock
WSB: A-port select
WAn: A-port address (Write)
RSB: B-port select
RAn: B-port address (Read)
TEB: Test enable
TIN: Test input
TOUT: Test output
TOD: DO disable
X: Irrelevant

(5) Timing characteristics

(a) Read/write common timing characteristics

Symbol Name	Description	MIN. Side	MAX. Side	Remark
t_{CYC}	Clock cycle time	√	√	Common to read/write cycle
t_{CPL}	Low side clock minimum pulse width	√	√	Low side of CLK
t_{CPH}	High side clock minimum pulse width	√	√	High side of CLK

(b) Write cycle timing characteristics

Symbol Name	Description	MIN. Side	MAX. Side	Remark
t_{WAS}	Write address setup time	√	√	–
t_{WAH}	Write address hold time	√	√	–
t_{DS}	Data setup time	√	√	–
t_{DH}	Data hold time	√	√	–
t_{WSH}	Write select High side setup time	√	√	Timing specification making CLK invalid
t_{WHH}	Write select High side hold time	√	√	Timing specification making CLK invalid
t_{WSL}	Write select Low side setup time	√	√	Timing specification making CLK valid
t_{WHL}	Write select Low side hold time	√	√	Timing specification making CLK valid

(c) Read cycle timing characteristics

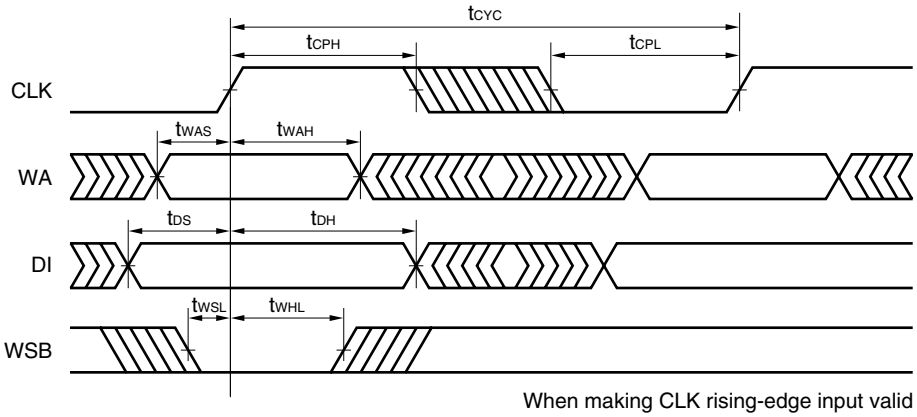
Symbol Name	Description	MIN. Side	MAX. Side	Remark
t_{ACA}	Address access time	√	√	t_{WSC} when RA = WA
t_{RAS}	Read address setup time	√	√	–
t_{RAH}	Read address hold time	√	√	–
t_{RSL}	Read select disable time	√	√	–
t_{RSC}	Read select access time	√	√	–

(6) Timing charts

In this high-speed synchronous dual-port RAM, since all write/read operations are performed by a single-phase clock (CLK), the write cycle time/read cycle time defined by the asynchronous RAM is provided as clock cycle time. Moreover, the clock pulse width (Low side, High side) is also defined for the basic clock (CLK) only.

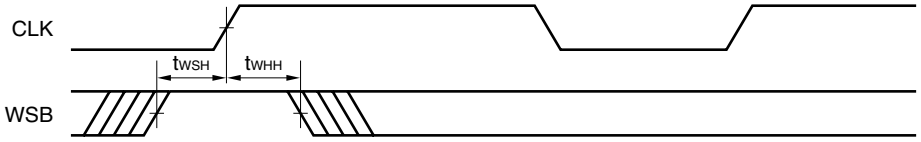
(a) Write cycle timing

<1> Write cycle timing



When making CLK rising-edge input valid

<2> Write cycle timing (invalid)

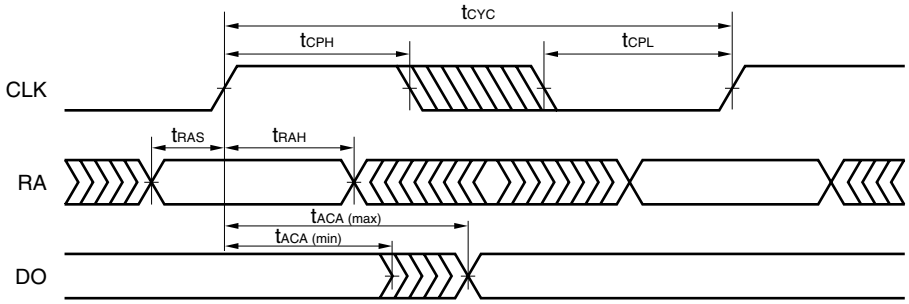


When making CLK rising-edge input invalid

Remark TEB = 1, TOD = 0

(b) Read cycle timing

<1> Read cycle timing (timing 1)



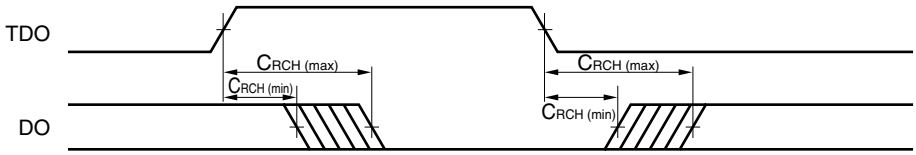
Remark TEB = 1, TOD = 0, RSB = 0

<2> Read cycle timing (timing 2)

Remark TEB = 1, TOD = 0, address signal must be set before low level of RSB signal

(c) Output disable timing

By making TOD = 1, the output pin DO is disabled and the data output pin DO is fixed to 0. Internal RAM follows the determined operations according to the control pins (RSB, WSB, and TEB).

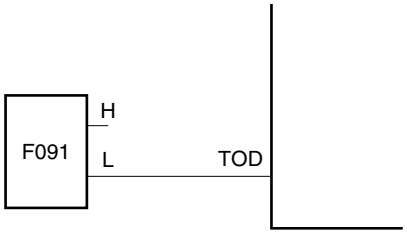


(7) Various specifications

If memory is created by OPENCAD, a data sheet will be created in the PostScript format (the file name is <RAM block name>.ps). For details of the various specifications (such as macro size, power consumption, AC characteristics), refer to the data sheets created by OPENCAD.

(8) TOD processing

Clamp TOD to L by using F091, etc.



7.8.4 High-speed asynchronous single-port/dual-port memory block of gate array compiled type

Caution This memory requires a library during layout. Please contact NEC Electronics if planning to use this memory.

(1) Compiled range

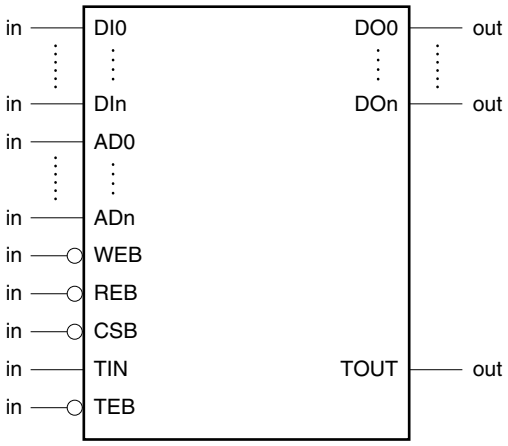
Compiled range of high-speed asynchronous single-port/dual-port RAM

Number of words \ Number of bits	2 to 8	Up to 16	Up to 32	Up to 64	Up to 128
4 to 32	√	√	√	√	√
Up to 128	√	√	√	√	×
Up to 256	√	√	√	×	×
Up to 512	√	√	×	×	×
Up to 1024	√	×	×	×	×

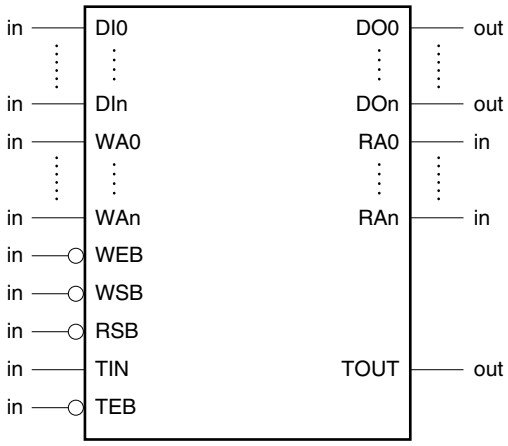
Remark An odd number of bits is possible, providing the number is within the allowable range. Only realizable when the total number of words is an even number.

(2) Symbol diagram

(a) Symbol diagram of single-port RAM



(b) Symbol diagram of dual-port RAM



(3) Pin function list

(a) Pin function table of single-port RAM

Symbol Name	Pin Attribute	Pin Function
DI (n:0)	Input	Data input
AD (n:0)	Input	Address input
WEB	Input	Write enable input
REB	Input	Read enable input
CSB	Input	Chip select input
TIN	Input	Test clock input
TEB	Input	Test enable input
DO (n:0)	Output	Data output
TOUT	Output	Test output

(b) Pin function table of dual-port RAM

Symbol Name	Pin Attribute	Pin Function
DI (n:0)	Input	Data input
WA (n:0)	Input	Write address input
RA (n:0)	Input	Read address input
WEB	Input	Write enable input
WSB	Input	Write select input
RSB	Input	Read select input
TIN	Input	Test clock input
TEB	Input	Test enable input
DO (n:0)	Output	Data output
TOUT	Output	Test output

(4) Operation truth table

(a) Truth table of single-port RAM

TEB[Note]	TIN	DIn	ADn	CSB	WEB	DMn	REB	DOn	TOUT	Operation
1	X	DIn	ADn	0	↓	DIn (ADn)	1	0	X	Write
1	X	DIn	ADn	0	↓	DIn (ADn)	0	DMn (ADn)	X	Write, Read
1	X	X	ADn	0	0	Hold	0	DMn (ADn)	X	Read
1	X	X	ADn	0	1	Hold	0	DMn (ADn)	X	Read
1	X	X	X	1	X	Hold	X	0	X	Hold
1	X	X	X	X	0	Hold	1	0	X	Hold
1	X	X	X	X	1	Hold	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	X	RESULT	Test Mode

Note TEB = 0 is test mode.

Remark DIn: Input data DOn: Output data DMn: Memory data
CSB: Chip select WEB: Write enable REB: Read enable
ADn: Address TEB: Test enable TIN: Test input
TOUT: Test output X: Irrelevant

(b) Truth table of dual-port RAM

TEB[Note]	TIN	DIn	WAn	WSB	WEB	DMn	RAn	RSB	DOn	TOUT	Operation
1	X	DIn	WAn	0	↓	DIn (WAn)	X	1	0	X	Write
1	X	DIn	WAn (≠RAn)	0	↓	DIn (WAn)	RAn (≠WAn)	0	DMn (RAn)	X	Write, Read
1	X	DIn	WAn (=RAn)	0	↓	DIn (WAn)	RAn (=WAn)	0	DIn (WAn)	X	Write, Read
1	X	X	X	1	X	Hold	RAn	0	DMn (RAn)	X	Read
1	X	X	X	X	0	Hold	RAn	0	DMn (RAn)	X	Read
1	X	X	X	X	1	Hold	RAn	0	DMn (RAn)	X	Read
1	X	X	X	1	X	Hold	X	1	0	X	Hold
1	X	X	X	X	0	Hold	X	1	0	X	Hold
1	X	X	X	X	1	Hold	X	1	0	X	Hold
0	CLOCK	X	X	X	X	X	X	X	X	RESULT	Test Mode

Note TEB = 0 is test mode.

Remark DIn: Input data DOn: Output data DMn: Memory data
WEB: Write enable WSB: Write select RSB: Read select
WAn: Write address RAn: Read address X: Irrelevant
TEB: Test enable TIN: Test input TOUT: Test output

(5) Timing characteristics

(a) Write cycle timing characteristics

Symbol Name	Description	MIN. Side	MAX. Side	Remark
t_{WC}	Write cycle time	√	√	–
t_{WPL}	Write enable pulse width (Low level)	√	√	–
t_{WPH}	Write enable pulse width (High level)	√	√	–
t_{AS}	Address setup time	√	√	–
t_{AH}	Address hold time	√	√	–
t_{DS}	Input data setup time	√	√	–
t_{DH}	Input data hold time	√	√	–
t_{CS}	Chip select setup time	√	√	For single-port
t_{CH}	Chip select hold time	√	√	For single-port
t_{WS}	Write select setup time	√	√	For dual-port
t_{WH}	Write select hold time	√	√	For dual-port
t_{WEC}	Write enable access time	√	√	–

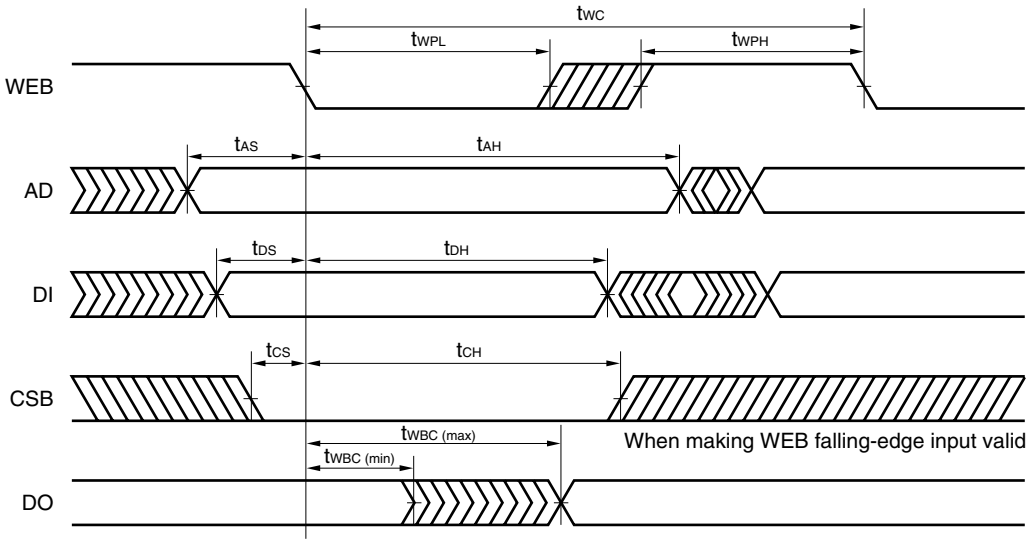
(b) Read cycle timing characteristics

Symbol Name	Description	MIN. Side	MAX. Side	Remark
t_{RCA}	Read cycle time	√	√	–
t_{ACA}	Address access time	√	√	–
t_{CSC}	Chip select access time	√	√	For single-port
t_{CSL}	Chip select disable time	√	√	For single-port
t_{REC}	Read enable (read select) access time	√	√	–
t_{REL}	Read enable (read select) disable time	√	√	–

(6) Timing charts

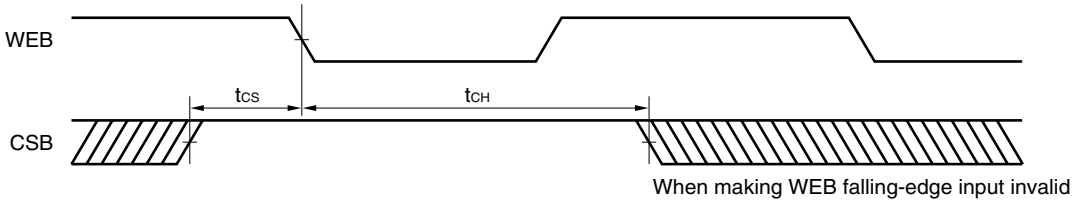
(a) single-port RAM timing

<1> Write cycle timing



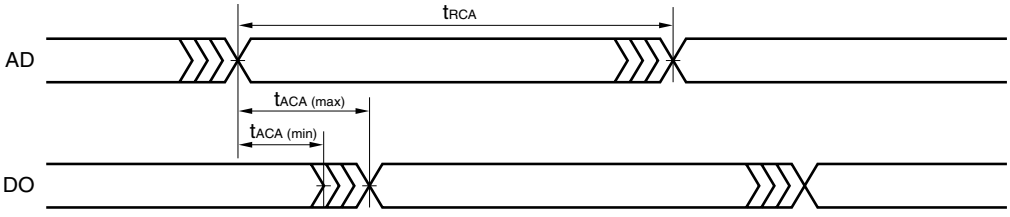
Remark TEB = 1

<2> Write cycle timing (invalid)



Remark TEB = 1

<3> Read cycle timing (timing 1)



Remark TEB = 1

<4> Read cycle timing (timing 2)

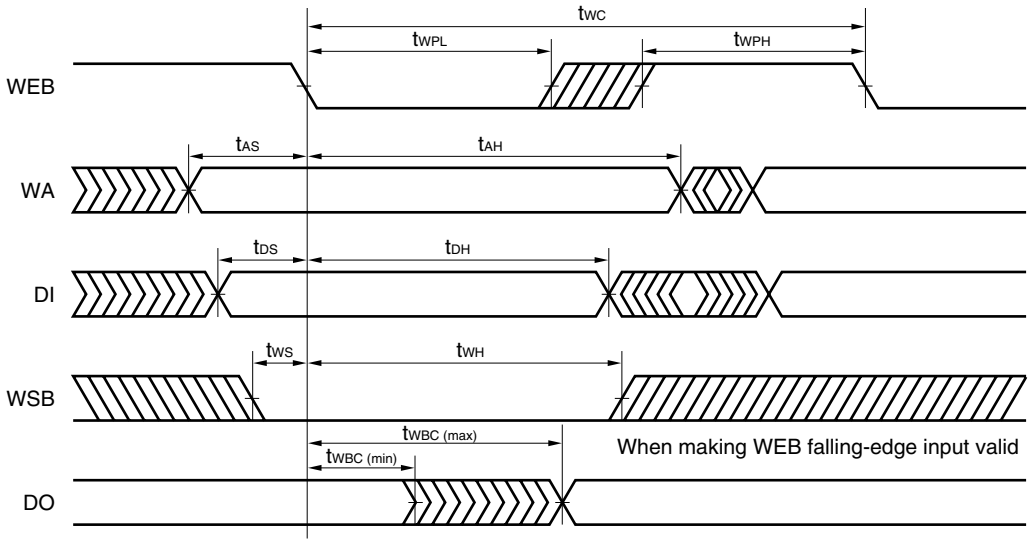
Remark TEB = 1, address signal must be set before low level of CSB signal

<5> Read cycle timing (timing 3)

Remark TEB = 1, address signal must be set before low level of REB signal

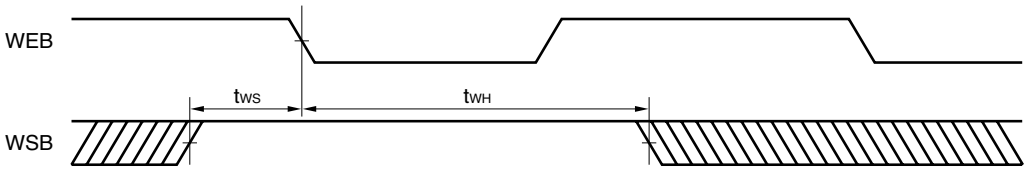
(b) dual-port RAM timing

<1> Write cycle timing



Remark TEB = 1

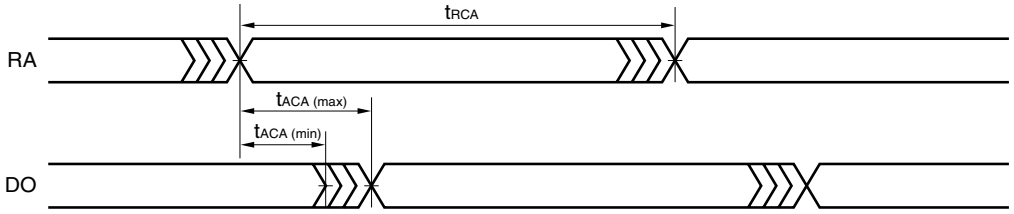
<2> Write cycle timing (invalid)



When making WEB falling-edge input invalid

Remark TEB = 1

<3> Read cycle timing (timing 1)



Remark TEB = 1

<4> Read cycle timing (timing 2)

Remark TEB = 1, address signal must be set before low level of RSB signal

(7) Various specifications

If memory is created by OPENCAD, a data sheet will be created in the PostScript format (the file name is <RAM block name>.ps). For details of the various specifications (such as macro size, power consumption, AC characteristics), refer to the data sheets created by OPENCAD.

7.8.5 RAM block

As shown in Figures 7-35 and 7-36, the high-density RAMs have a bit/word architecture based on basic macros (hard macros). The test circuit (BIST: Built-In Self Test) and built-in selector are configured by soft macros. This architecture eases restrictions on placement and routing, and reduces complexity when multiple RAMs are placed. The test circuit is also incorporated in the compiled RAM.

The memory test is included in the BIST soft macro. Only 3 pins are necessary for the test and there is no need to directly input to and output from all the pins.

If using RAM of NEC Electronics, be sure to use test circuit (BIST) of NEC Electronics standard.

Figure 7-35. Single-port RAM Circuit Configuration

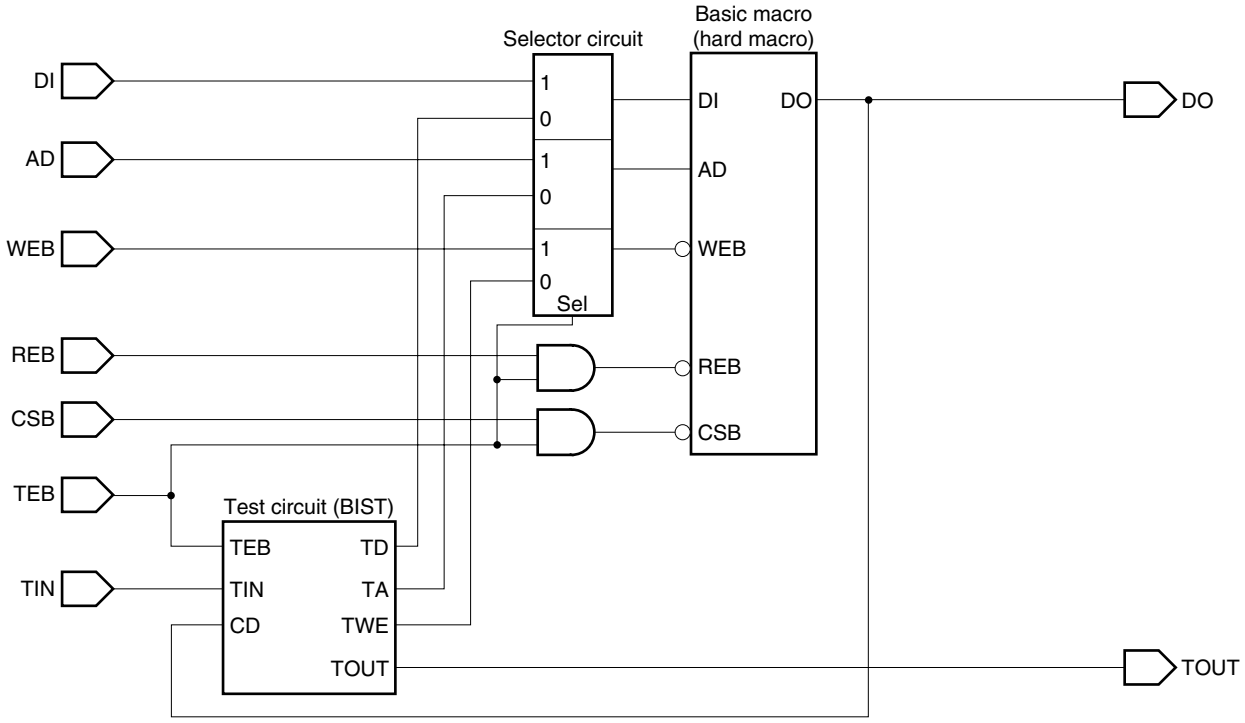
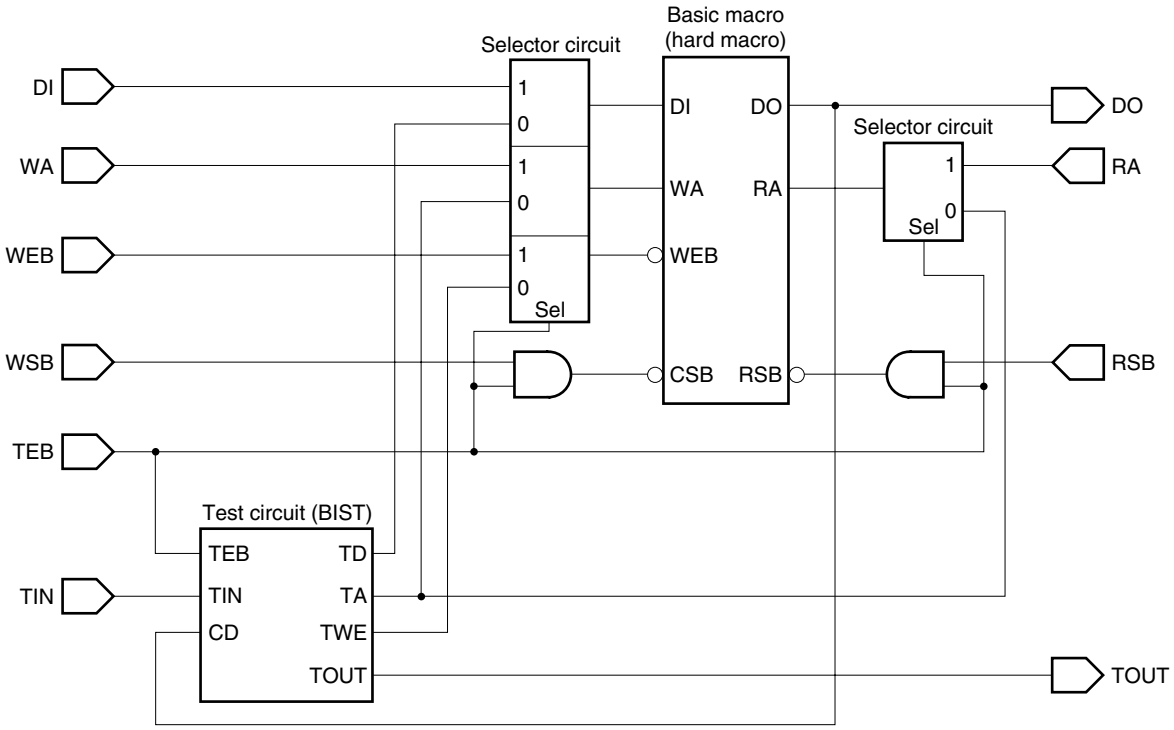


Figure 7-36. Dual-port RAM Circuit Configuration



7.9 Memory Block Description Format

Note the following cautions when describing a memory block as a circuit diagram or connection data.

7.9.1 Selection of memory block

In the CMOS-9HD Series, RAM blocks are configured as soft macros. Therefore, RAM blocks with any bit/word configuration can be freely placed by combining the basic memory cells. However, certain frequently used blocks have already been registered as a simulation model (see **CMOS-9HD Series, EA-9HD Series Memory Block Library (A13071E)**). Therefore, you should select and use blocks among these representative models whose size is closest to the desired bit/word size.

If there is no memory block in the desired size, such as when there are too many bits, consider connecting in parallel blocks having the same word size but different bit sizes.

Conversely, if there are too many words, use a decoder or other component to create a chip select signal as is done for ordinary memory circuits, then allocate the addresses.

When using memory in which the number of bits does not match the number of words, use soft macros instead, as described above. Contact NEC Electronics concerning the circuit configuration and test circuit (BIST) configuration.

7.9.2 Using memory block

As with other function blocks, there are rules concerning fan-in (F/I) and fan-out (F/O) (see **CMOS-9HD Series, EA-9HD Series Memory Block Library (A13071E)**). Make sure that the connections do not exceed fan-out limits, etc.

7.10 Memory Tests

7.10.1 RAM test

Using the BIST function to test RAM blocks in the CMOS-9HD Series eases the restrictions on the number of test patterns and makes it easier for users to perform memory checks.

As shown in Figure 7-37, the BIST function includes test signal generators that generate test addresses, test data, and test enable signals as well as a comparator that compares the output of the signal generators with the output of the expected value generator. User setup for performing RAM tests is done by simply connecting three pins: TIN, TEB, and TOUT, to external pins. When several RAM blocks have been mounted, the test inputs (TIN and TEB) can be shared with corresponding pins on other RAM blocks. The test output (TOUT) cannot be shared. It must be connected to a different external pin. Figure 7-38 shows a connection example.

When performing RAM tests, the basic idea is to send data directly from external input pins to the test inputs (TIN and TEB) and to retrieve the data from the test output (TOUT) via a direct connection to an external pin. If inverters or F/F are used instead of direct connections, the configuration must then include signal inversion, clocking, and the like, which makes it impossible to use the basic test pattern. The final state of any user-provided test pattern must be usable for RAM testing (i.e., the TIN, TOUT, and TEB pins must be able to handle RAM test signals sent directly from external pins).

NEC Electronics will provide the RAM test patterns.

Figure 7-37. Test Circuit (BIST) Block Diagram

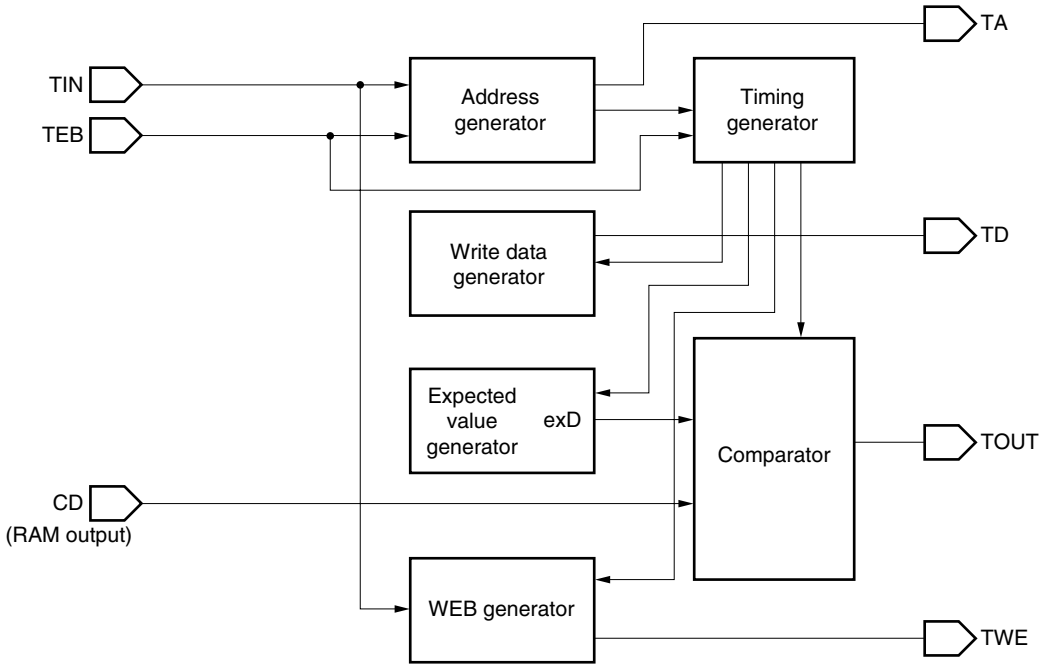


Figure 7-38. Example of RAM Test Circuits (1/2)

(a) Connection example for placing one RAM block

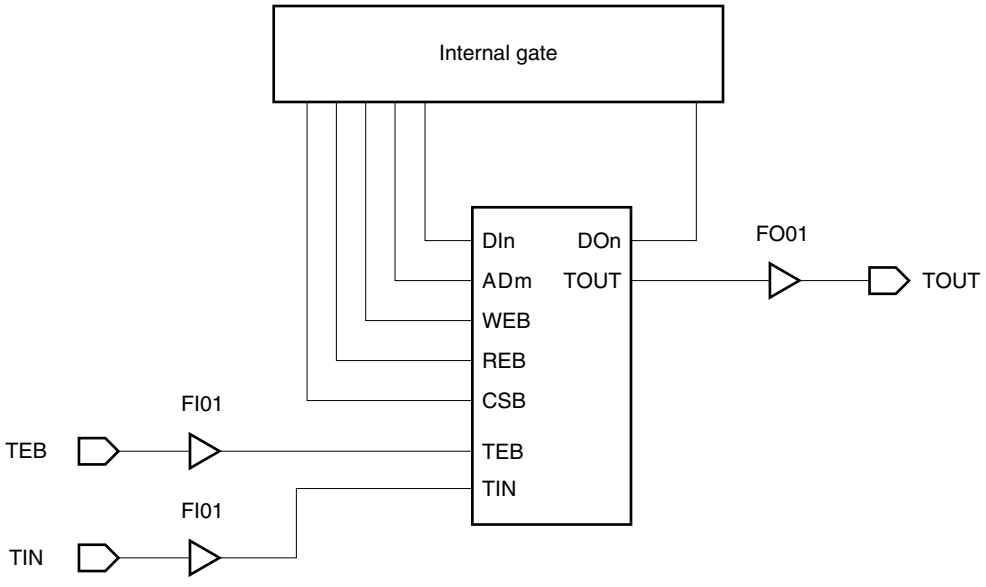
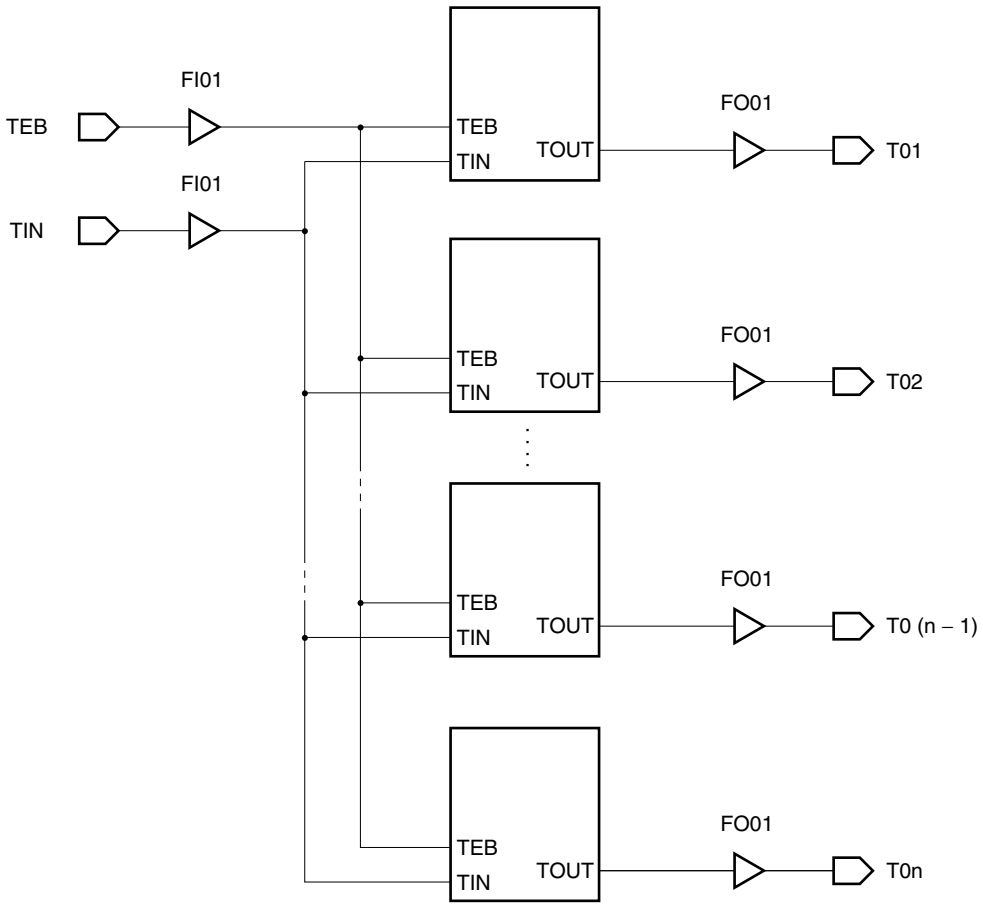


Figure 7-38. Example of RAM Test Circuits (2/2)

(b) Connection example for placing multiple RAM blocks



(1) Integrate the TEB input and TIN input as one pin and connect it to the respective RAM. Even when the RAM blocks have different capacities, each TEB input and TIN input is shared with the other TEB inputs and TIN inputs.

(2) Each TOUT pin outputs to a separate external pin.

7.10.2 Setup of test I/O pins (TIN, TEB, and TOUT)

(1) If there are unused pins

<R> If there is any unused pins other than power supply pins, use those pins for testing.

(2) If there are no unused pins

Certain pins that are already being used can be shared as test pins. Note the following when deciding which pins to set up as shared pins. Note that the TEB pin cannot be shared and another pin must be set up as a dedicated pin.

<1> Shared TIN pin: This pin can be shared with ordinary input pins or ordinary output pins. When sharing a TIN pin with an ordinary output pin, use the pin as a bidirectional pin for the TEB signal as the enable signal, use it as an output pin for normal usage, and as an input pin for testing. In addition, fix test pattern terminal to low level in this case. Figure 7-39 shows a connection example.

<2> Shared TOUT pin: This pin can also be shared with ordinary input pins or ordinary output pins. When sharing a TOUT pin with an ordinary input pin, use the pin as a bidirectional pin for the TEB signal as the enable signal, use it as an input pin for normal usage, and as an output pin for testing. When sharing this pin with an ordinary output pin, use an internal selector circuit for switching via the TEB signal. Figure 7-40 shows a connection example.

Caution This pin cannot be shared with pins using GTL+ interface buffer, N-ch open-drain buffer, or CMOS 5 V tolerant output buffer.

(3) Handling on board

Select one method from the following for handling the TEB and TIN pins.

<1> Handling of TEB pin[Note 1]:
- Use a pull-up buffer
- Pull it up externally
- Connect it to V_{DD} externally

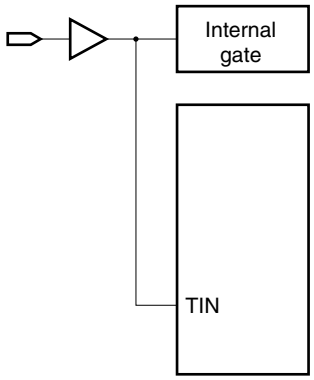
<2> Handling of TIN pin[Note 2]:
- Use a pull-up buffer
- Use a pull-down buffer
- Connect it to V_{DD} externally
- Connect it to GND externally

Note 1. Handle so that this pin is not set to the test mode.

Note 2. Handling is required when the TIN pin does not have an alternate function as a normal pin.

Figure 7-39. Making TIN Pin Alternate Function

(a) Alternate function as normal input pin



(b) Alternate function as normal output pin (bidirectional pin)

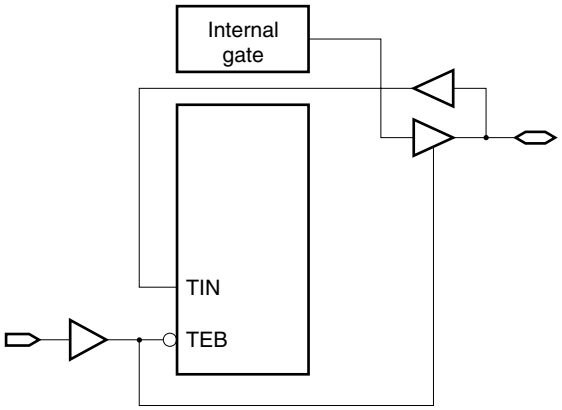
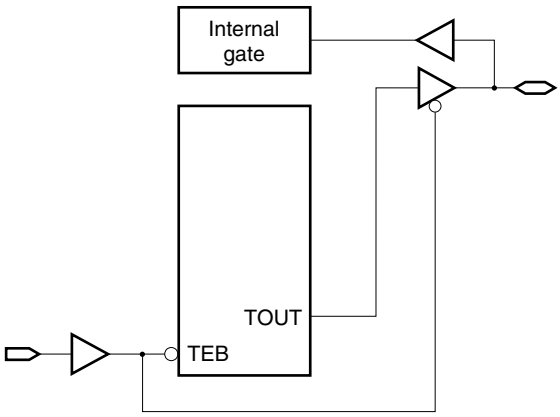
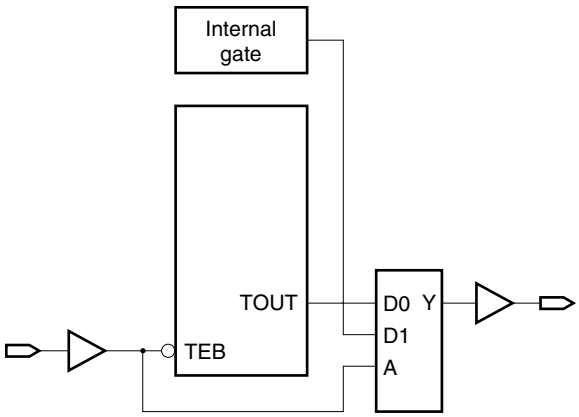


Figure 7-40. Making TOUT Pin Alternate Function

(a) Alternate function as normal input pin (bidirectional pin)



(b) Alternate function as normal output pin



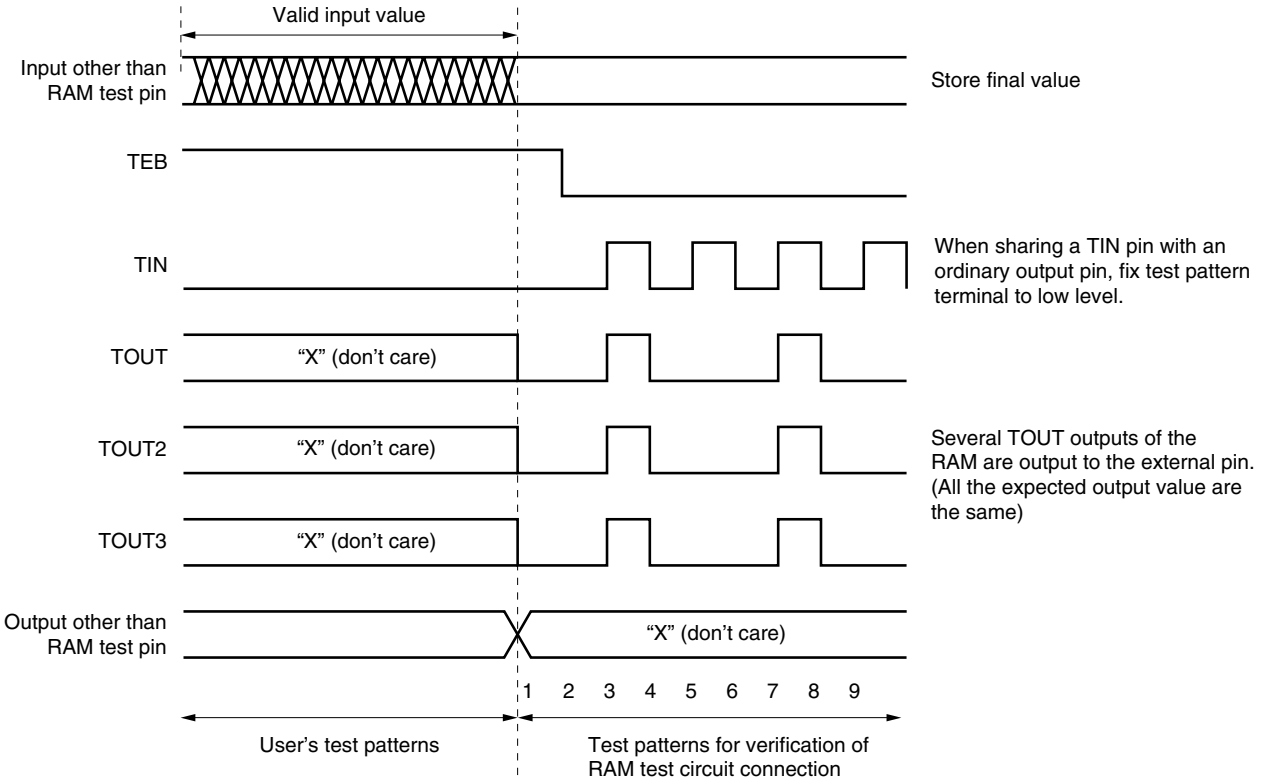
7.10.3 RAM test circuit connection check

To check whether or not the BIST circuit is properly connected, carry out checking by RAMCHK flow on OPENCAD generating and adding the connection confirmation patterns (nine patterns) as shown in Figure 7-41 to the end of the user-provided test pattern (Test pattern for DC check: if the DC pattern is independent, then it is this pattern) by using OPENCAD RAMCHK. Be sure to perform RAMCHK before submitting the test pattern to NEC Electronics. In addition, set the status in which input and output for the pin signals required to the BIST test (TEB, TIN, and TOUTx) can be executed at the end of the test pattern (Test pattern for DC check: if the DC pattern is independent, then it is this pattern.)

When sharing a TIN pin with an ordinary output pin, fix test pattern terminal to low level.

The RAM-BIST test pattern is provided by NEC Electronics and thus the user does not need to generate it.

Figure 7-41. Example of Test Patterns



(1) Input other than RAM test pin: Input 9 patterns in such a way that the final value of the user test pattern is preserved.

(2) TEB: First input a high level for 1 pattern and then input a low level for 8 patterns.

(3) TIN: First input a low level for 1 pattern and then input 8 patterns of repetitive 01 signals.

(4) TOUT: Set the expected output value to 001000100. When multiple RAM is placed, several TOUT outputs of the RAM must be output to the external pins (the RAM test is executed completely in parallel).

(5) Output other than RAM test pin: Set the expected output value to "X" (don't care).

Remark The connection check pattern of BIST is automatically generated by RAMCHK and thus it is not necessary to add it to the user's patterns in advance.

In addition, simultaneous checking can be carried out by connecting TIN and TEB in common in the gate array type RAM and cell-based IC type RAM.

7.10.4 ROM tests

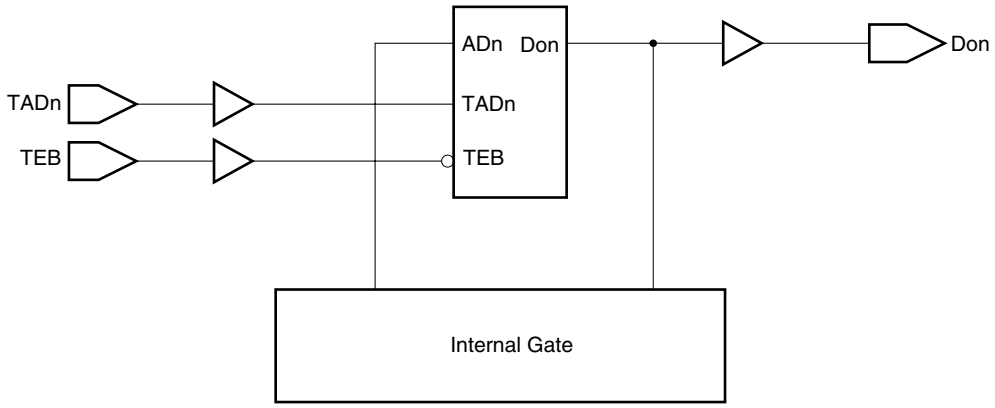
The ROM block has the test address. Turning on and off the test enable signal (TEB) switches between the real and test modes. If it is difficult to conduct ROM tests within the user-designed circuit, design a scheme that enables ROM tests to be conducted directly from external pins, as shown in Figure 7-42.

The user should prepare ROM test patterns.

ROM tests should read and check all memory contents with ROM codes. NEC Electronics does not check the ROM codes. The user should include this check in the test patterns.

See Section **7.11.5 ROM code format** for ROM code generation.

Figure 7-42. ROM Test Circuit Example



7.10.5 ROM code format

Either NINCF or extended Intel hex can be used as the interface data format for the ROM code.

All ROM code bits must be defined as either input or output pins. For example, if an area of 990 bytes are used in a 1K byte ROM, the user should specify also the remaining 34 bytes in the interface data file.

NINCF format :	NEC Electronics-defined format, handling data of undefined length
Extended Intel hex format :	World-standard ROM code, only applicable to byte data. Extended Intel hex format can handle 16-bit data.

(1) Incorporating the ROM code into a simulation system

Merely registering a ROM in a simulation library does not make it usable. The ROM code must be incorporated into the simulator before staring simulation.

The method for ROM code incorporation depends on the simulator. An example follows.

V.sim :	NINCF format only. The ROM code is incorporated at the beginning of simulation using the mr command.
Verilog :	The ROM code is converted from the extended Intel hex or NINCF format to the Verilog format. The Verilog format allows both hex and binary descriptions. In the ROM macro library, the ROM code is specified by $READMEMH (hex format) or $READMEMB (binary format).

(2) NINCF

The NINCF file is a text file with a fixed format shown in Figure 7-43.

Although ASCII codes can be entered using a text editor, have the NINCF file created automatically to avoid chances of error.

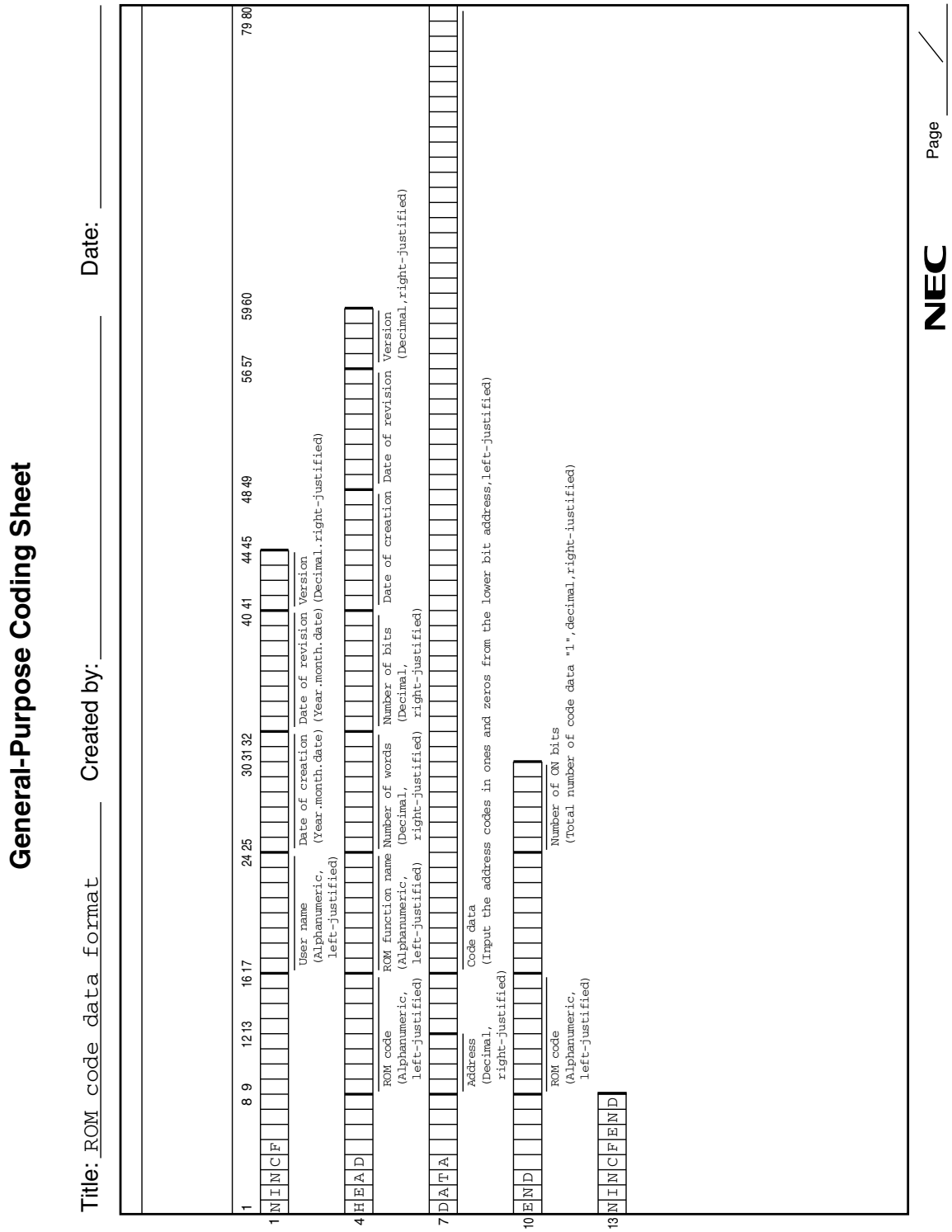
A utility program is available for automatic conversion from the extended Intel hex format.

(3) ROM code generation

Describe ROM code in the format shown in Figure 7-43 below.

Note that because this is a fixed-column format, the columns must not be shifted when describing.

Figure 7-43. Format of ROM Code Data

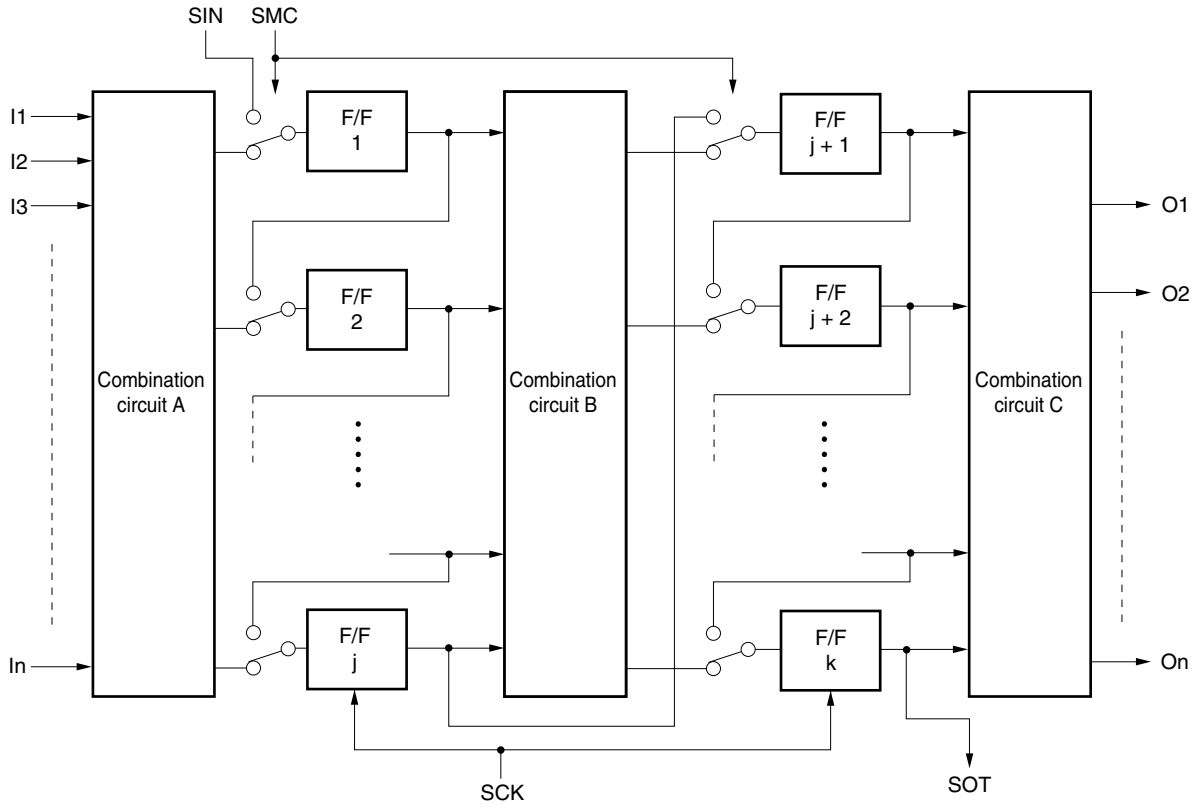


7.11 Scan Path Test

It is extremely difficult to create a test pattern that checks the operation of an LSI efficiently with a circuit that frequently uses flip-flops (F/F) and that has a deep logical depth. Scan path testing can change the connections of all the internal flip-flops of LSI-like shift registers. Therefore, the circuit can be tested efficiently by easily initializing all the flip-flops of a circuit with a deep logical depth and reading all the flip-flop states in a certain state.

For details, see **SYSTEM LSI DESIGN Design For Test User's Manual**.

Figure 7-44. Theory of Scan Path Test Method



Remark In: Input signal when testing a combination circuit, or normal input
On: Diagnostic output when testing a combination circuit, or normal output
SIN: Input signal when testing a sequential circuit
SMC: Mode switching signal
SCK: Test clock
SOT: Diagnostic output when testing a sequential circuit

7.12 Boundary Scan Test

In recent years, connections among LSIs on boards have become very complex due to the trend towards multi-layer boards, more pins per LSI chip, etc., which has had the effect of making LSI-related testing more complex.

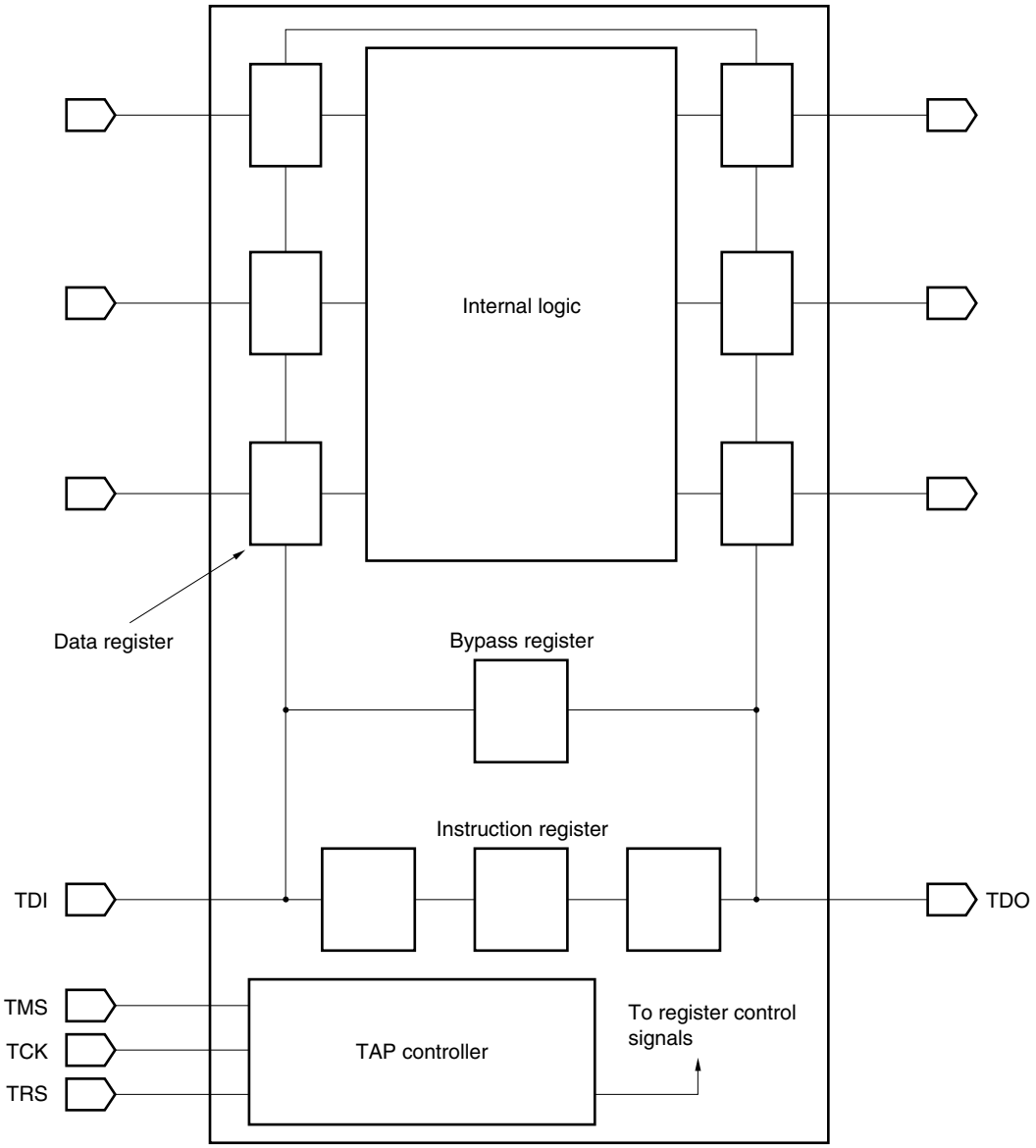
The boundary scan test method is an easy, highly reliable test method based on IEEE's 1149.1 standard.

This test makes it possible to check LSI connections, etc., by inputting and outputting test data with the dedicated register as if successively scanning the LSI input/output pins.

As can be seen in Figure 7-45, a boundary scan circuit includes dedicated buffers and data registers located between the LSI's internal logic and its external pins. These data registers can be used to measure values and control input and output at each pin. In other words, the data registers function in the same way as conventional test probes (the data registers are connected in serial).

For details, see **SYSTEM LSI DESIGN Design For Test User's Manual**.

Figure 7-45. Boundary Scan Circuit Diagram



APPENDIX A POWER CONSUMPTION

An accurate calculation of the power consumption of internal circuits requires a very large amount of information, such as capacitance, number of synchronously operating blocks, and operating frequency of each block. Consequently, the calculation becomes too complicated to be performed. On the basis of assumptions concerning such items as circuit operation and configuration, NEC Electronics provides reference values for power consumption. It must be noted that these values may be larger or smaller than the actual values, depending on factors such as the user's actual circuit and its configuration.

This chapter provides a power consumption calculation method that divides the power consumption of the internal circuit into combination circuits, latches, and flip-flops. This calculation should be used to review circuit power consumption. However, if the results are to be used to calculate the life-span of a battery, an extra margin should be provided.

Internal Cell Power Consumption

$$\Sigma P_{DCELL} = \Sigma P_{DGate} + \Sigma P_{DLatch} + \Sigma P_{DF/F} + \Sigma P_{DT}$$

(1) Combination circuits

$$P_{DGate} = 0.524 \times f \times Cell \ (\mu W)$$

where:

f: Operating frequency of data (MHz)

Cell[Note]: Number of cells that operate at f

Note "Cell" is not number of blocks.

(2) Latches

$$P_{DLatch} = \{P_{D(Gate = ON)} \times N + P_{D(Gate = OFF)} \times (1 - N)\} \times f \times Cell \quad (\mu W)$$

where:

f: Operating frequency of data (MHz)

Cell[Note]: Number of cells that operate at f

N: Percentage of "Gate = ON" = $\dfrac{T_{(Gate = ON)}}{T_{(Gate = ON)} + T_{(Gate = OFF)}}$

$P_{D(Gate = ON)}$: 0.516 (μW/Cell/MHz)

$P_{D(Gate = OFF)}$: 0.0385 (μW/Cell/MHz)

Note "Cell" is not number of blocks.

(3) D-F/F, JK-F/F, shift registers, and counters

$$P_{DF/F} = \frac{2 \times P_{D(OUTPUT)} + P_{D(CLK)} \times (N-2)}{N} \times f \times Cell \ (\mu W)$$

where:

f: Operating frequency of clock (MHz)

Cell[Note]: Number of cells that operate at f

N: $\frac{T_{(DATA)}}{T_{(CLK)}}$

$P_{D(OUTPUT)}$: 0.412 (μW/Cell/MHz)

$P_{D(CLK)}$: 0.121 (μW/Cell/MHz)

Note "Cell" is not number of blocks.

Remark $T_{(DATA)}$: Data cycle

$T_{(CLK)}$: Clock cycle

Example When the clock is twice as fast as one data cycle:

N = 1/0.5 = 2

(4) T-F/F

$P_{DT} = 0.367 \times f \times Cell$ (μW)

where:

f: Operating frequency of clock (MHz)

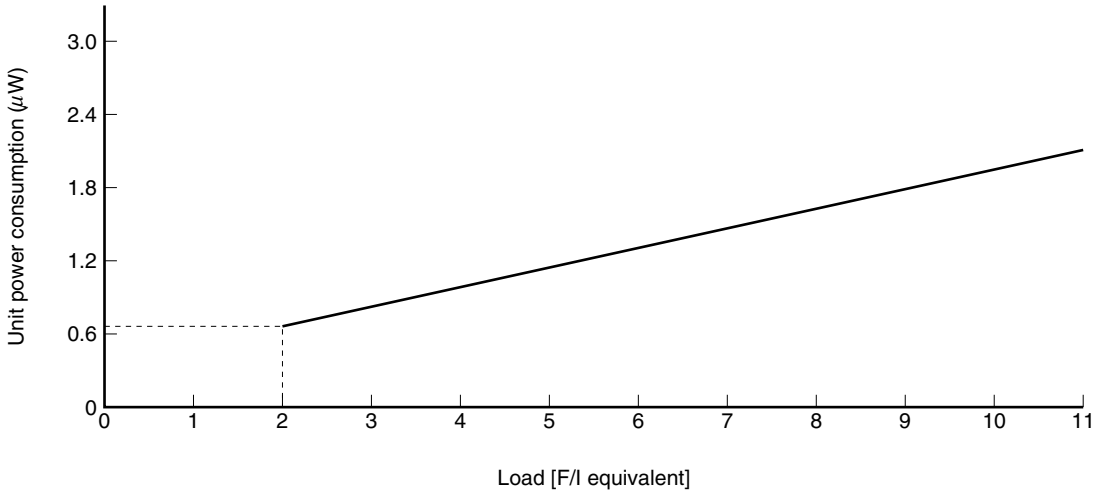
Cell[Note]: Number of cells that operate at f

Note "Cell" is not number of blocks.

(5) Load dependency of power consumption (preliminary)

Power consumption depends to a great extent on the load capacitance, as expressed by $P_D = CV^2f$.

Figure A-1. Load Dependency of Power Consumption



As shown in Figure A-1, the unit power consumption when F/O = 2 is an extremely small 0.66 μW/MHz. Because power consumption has a significant effect on reliability, a realistic value must be used.

The value of load = 4.98 (F/I equivalent) covers a distribution of about 70% of load values, based on statistical data accumulated at NEC Electronics, such as wiring length and pin pairs.

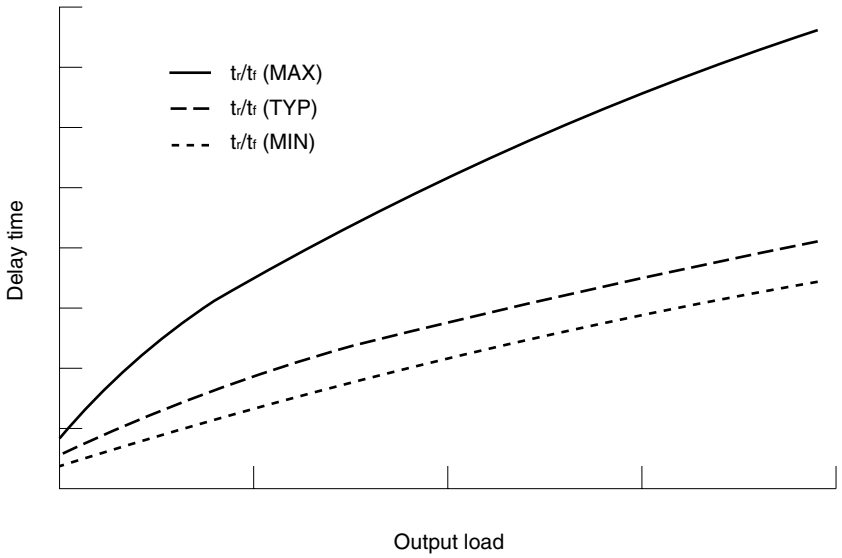
where:

F/O : 2 + ℓ : 2.98

APPENDIX B PROPAGATION DELAY TIME

The propagation delay time of each block varies significantly with the input signal waveform as shown in Figure B-1. With the CMOS-9HD Series, whose delay time is as short as several 100 ps at each block, the influence of the input waveform is not negligible.

Figure B-1. Delay Time Increase Due to Input Waveform
t_r/t_f (MIN) < t_r/t_f (TYP) < t_r/t_f (MAX)



Consequently, the simulator considers the input waveform of each block so that highly accurate delay simulation is executed. However, discrepancies in results due to the input waveform cannot be listed in the block library[Note]. For this reason, the accuracy of the propagation delay time calculations listed in the block library[Note] are valid only under certain limited conditions. The propagation delay times of critical paths, in which the load is likely to be light, are calculated accurately in the CMOS-9HD Series.

Figure B-1 shows only the tendency, so confirm actual values by simulation.

Note CMOS-9HD Series, EA-9HD Series Block Library (A13052E)

APPENDIX C ALBATROSS AND DIF FILE FORMATS

C.1 ALBATROSS File Format (Circuit Name.alb)

(1) File format

The ALBATROSS file format has the following characteristics:

- Free format
- Parameters must be delimited by blank space or a colon (:).
- Each statement must be terminated with a semicolon (;).
- Items within brackets ([ ]) can be repeated.
- Maximum of 80 columns per line (when the last character is not a semicolon, the line must continue on the next line)
- Identifiers, pin names, and units (NS; fixed) must be specified in uppercase letters
- Pin names consist of a maximum of 64 characters
- The description of the timing data (MODULATION + CLOCK) is based on the limitations shown for the **6.6 High-Speed Function Test (Real-Time Test)**.

(2) File configuration

The ALBATROSS file consists of the following seven parameters.

*ALBATROSS .....File header
*TIMING .....Header
PERIOD.....Pattern period
MODULATION .....Input skew
CLOCK.....Clock pin
*END_OF_TIMING.....End record
*END .....File end

(3) Details of file

The details of each parameter are as follows:

(a) File header

Syntax: *ALBATROSS circuit;
Function: Pattern header

1: circuit (character string) circuit name

(b) Header

Syntax: *TIMING
Function: Header

(c) Pattern period

Syntax: PERIOD period_t time_unit;
Function: Period value of pattern

1: period_t Pattern cycle
2: time_unit Cycle time

(d) Input skew

Syntax: MODULATION modulation_t time_unit: [pin];

Function: Value of skew added to input pin

1: modulation_t Value of input skew
2: time_unit Unit of value of skew
3: pin Pin name

(e) Clock

Syntax: CLOCK TYPE = type: [ch_time time_unit]: pin;

Function: Definition of clock pin and clock waveform

- TYPE = type
  P: Positive clock
  N: Negative clock
- ch_time Waveform time
- time_unit Unit of change time
- pin Pin name

(f) End

Syntax: *END_OF_TIMING;

Function: End

(g) File end

Syntax: *END

Function: File end

(4) Example

```
*ALBATROSS CF191
*TIMING;
PERIOD 200 NS;
MODULATION 20 NS: IN1 IN2 IN3;
CLOCK TYPE = P: 50NS 150NS: CLK;
*END_OF_TIMING;
*END
```

C.2 DIF File Format (Circuit Name.dif)

For details, see **SYSTEM LSI DESIGN OPENCAD OPC_VSHELL User's Manual (A16306E)**.

(1) File format

The DIF file format has the following characteristics:

- Free format
- The delimiter is a blank space.
- Maximum of 512 characters per line
- The first column of a comment line begins with [-].

(2) File configuration

The DIF file consists of the following three parameters:

DIF..... Header
/DESIGN..... Design block
/END..... End

(3) Details of file

The details of each parameter are as follows:

(a) Header

Syntax: DIF
Function: Header

(b) Design block

Syntax: /PIA
Function: Whole external pin (V_{DD}, GND, etc.)

(c) Condition block

Syntax: /PIN
Function: Whole design (value of pin capacitance added to output pin, etc.)

(d) End card

Syntax: /END
Function: End of the DIF file

(4) Example

```
*DIF opc_pinbe (1.11) 2002.12.12 (12:39:32)
/DESIGN 65945999
 TECHNOLOGY = CMOS9HD;
 CONDITION = cmos_3.3V;
 MASTER = 65945;
 PACKAGE = LQFP;
 PINS = 144;
 LAYER = 3L;
  /CONDITION 1
   /PIN
      ADO
           DIR = INPUT
      ;
      DATA1
           DIR = IO
      ;
      PC1
           DIR = OUTPUT
      ;
     /END PIN
  /END CONDITION
 /PIA
  /EPIN PAD
     ADO
            PAD =     77 # dut_ID 22 pin_type IN
            BLOCK = XINB;
     DATA1
            PAD =      24 # dut_ID 179 pin_type IO
            BLOCK = XWN2;
     PCR1
            PAD =    125 # dut_ID 68 pin_type OUT
            BLOCK = XB0D;
  /END EPIN

     /POWER PAD
              GND PAD = 13 191;
              VDD PAD = 14;
     /END POWER

/END PIA
/END DESIGN
*END
```

APPENDIX D DRAWING CIRCUIT DIAGRAMS AND TIMING CHARTS

D.1 Drawing Circuit Diagrams

Today, circuits are designed using an engineering workstation (EWS). The circuit diagram drawn by the user is converted to NEC format on the EWS or through the interface service offered by NEC Electronics.

When the user draws a circuit diagram, the following points should be kept in mind to ensure smooth interfacing with NEC Electronics.

D.1.1 Logic symbols

As a general rule, use the logic symbols that are in the block library[Note]. However, when there are differences between the EWS library and the block library[Note], follow the format of the EWS library.

Note CMOS-9HD Series, EA-9HD Series Block Library (A13052E)

D.1.2 Block names (function names)

Input buffers and other blocks have different designations, but may have logic symbols that are virtually the same. In particular, the various input/output buffer interface levels cannot be determined from simulation results. Because of this, the block name should be entered so that it is easily understood.

In addition, since block names are expressed in advance in EWS libraries, entries cannot be made by the EWS.

D.1.3 Pin names (I/O pin name of block)

Block I/O pins are named in the order “H01, H02,.../N01, N02,....” If a block has more than one I/O pin, the pin names must be used whenever possible.

Pin names are usually displayed in EWS libraries. If a pin name is displayed, it need not be entered. For more information on displaying pin names, follow the instructions in the interface manual for the EWS.

D.1.4 Gate names (specific name of each block)

Enter the respective characteristic gate names for block names entered in a circuit diagram. A gate name must have 255 or fewer letters. To avoid duplication of gate names and pin names, make the names unique.

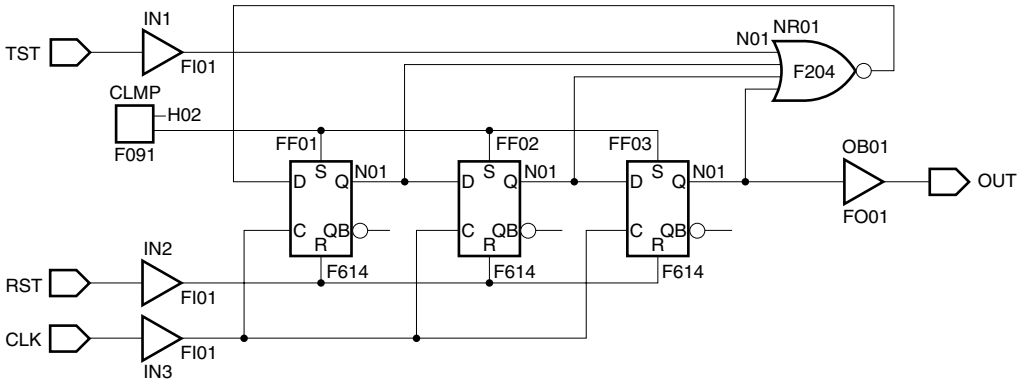
When an EWS is used, there are special cases where the naming rules are a function of the system being employed. See the EWS Interface Manual for details.

D.1.5 I/O pin names

A pin name of up to 64 alphanumeric characters must be assigned to each I/O pin of the LSI device. Each pin name must be unique and must not duplicate a gate name.

When an EWS is used, there are special cases where the naming rules are a function of the system being employed. See the EWS Interface Manual for details.

Figure D-1. Circuit Diagram Example



(1) Input pin names

The pin name of an input pin must consist of up to 64 alphanumeric characters.

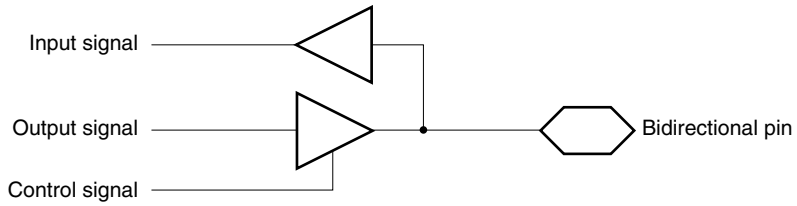
In addition, undefined and high impedance states cannot be input to an input pin because this causes the measurement conditions to change during testing with the LSI tester, making measurement impossible. Undefined and high impedance states also cannot be input to the input pins of input buffers and bidirectional buffers with on-chip pull-up/pull-down resistors.

If undefined or high impedance states are input as a test pattern, an error will result when simulation is executed.

(2) Bidirectional pin names

If the input and output of a bidirectional buffer are implemented from one pin, this must be named by using a bidirectional pin. The pin name must consist of up to 64 alphanumeric characters.

Figure D-2. Bidirectional Pin Names

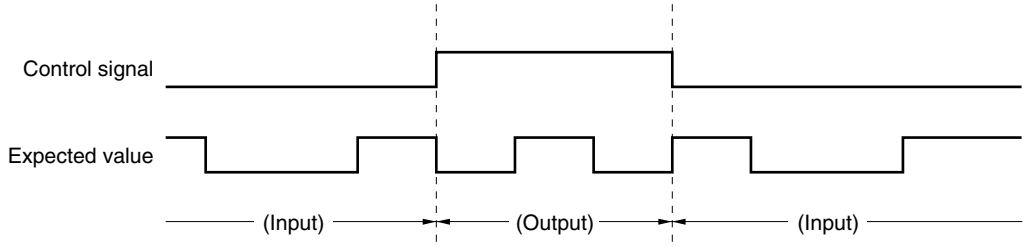


When a bidirectional pin test pattern is generated, care must be taken with regard to the following points:

<1> For switching from the output mode to the input mode, set the input and output signals to the same level.
<2> Do not set the control signal to the undefined state (if the state of the control signal becomes undefined, an undefined state is propagated to the input signal, generating an error in simulation).

During switching from the input mode to the output mode, an undefined state is propagated to the input signal due to the delay time of the control signal, generating an error in simulation. For such switching, it is important to configure the circuit so that an undefined state is not propagated to the input signal (see **6.3.6 Notes on switching I/O mode of bidirectional pin**).

Figure D-3. Bidirectional Pin Test Pattern Generation



(3) Three-state output pin notation

A three-state output pin must be named as shown in the examples in Figures D-4 and D-5. The pin name must consist of up to 64 alphanumeric characters.

Figure D-4. Three-State Output Pin Names

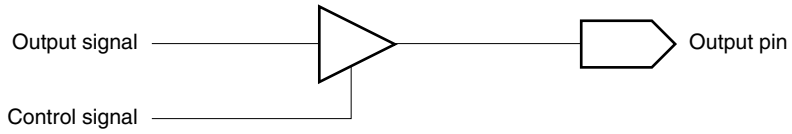
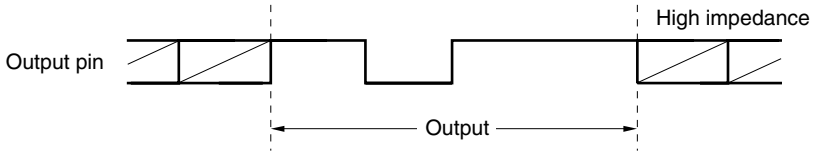


Figure D-5. Three-State Output Pin Test Pattern Generation



D.2 Handling Macros

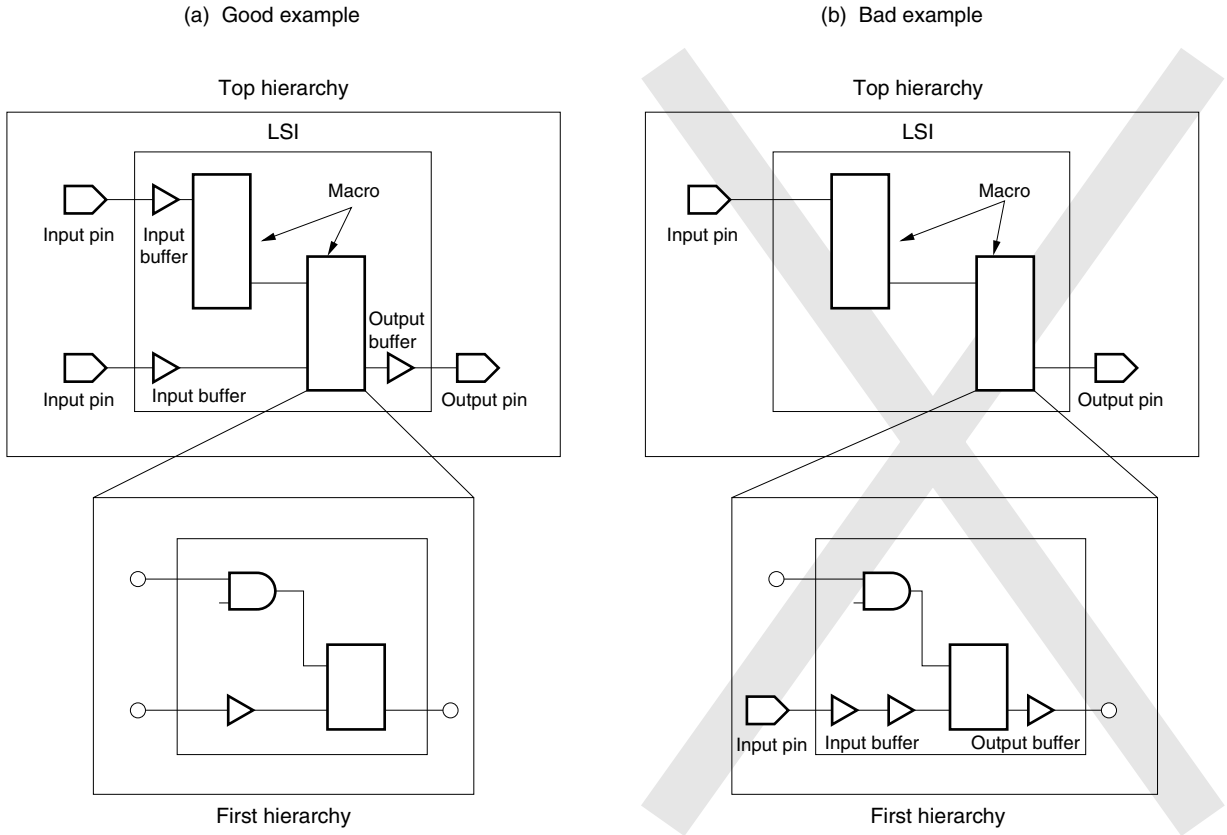
In logic design of a large scale circuit, in order to divide system internal block design and design man-hours, there are many cases where design is carried out using a hierarchical design method.

In the hierarchical design technique, functional units used in common are defined as macros (user macros). Each LSI chip is designed by connecting several macros to enable a specified function. In particular, a large-scale circuit is usually divided into several blocks, each of which is a hierarchical block and combined to configure the entire circuit.

In an EWS, etc., if a hierarchical design is done using a user macro, please use caution concerning the following points (see **Figure D-6**).

<1> Each Hierarchical block should perform a single logical operation.
<2> Design so that the total structure and the signal flow can be understood at the highest stage (the highest stage should be drawn on a single page).
<3> Whenever possible, design circuits that include a feedback loop so that the loop fits within the macro.
<4> Input pins and clamps (if needed) must be on the same page.
<5> Exercise care in the clock line flow. Ensure that delay differentials between pages do not exceed the allowable system clock skew.
<6> Each macro (bottom layer) must have a single function.
<7> A page should not contain signal lines only (pass-through only).
<8> External I/O buffers can be specified only at the top level. Avoid connecting I/O pins directly to an external device from a macro lower than that at the top level.
<9> A macro should not contain input, output, and bidirectional buffers.

Figure D-6. Handling Macros



D.3 Preparing Timing Charts

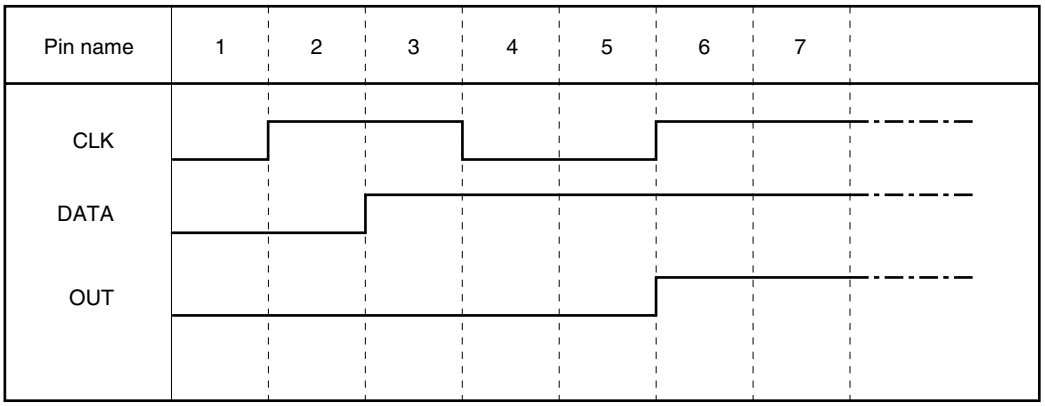
If the user provides NEC Electronics with a timing chart for generating the test patterns, or even if the user generates the test patterns, the timing charts must be drawn using the guidelines explained in this section.

(1) Entry method

The pin names of all input/output pins must be written in the vertical column. For each pattern, describe a “1” or “0” pattern for inputs and the expected values for outputs. Continuous sequential numbers, starting with 1, must be assigned to the test patterns.

Figure D-7 shows an example of filling out the timing chart.

Figure D-7. Timing Chart Entry

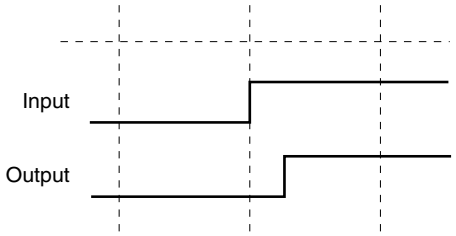


(2) Timing discrepancies

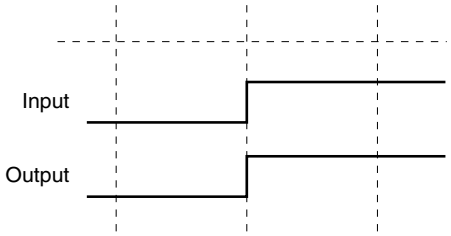
Because the output in actual circuits changes after the input pattern is applied, there is a timing delay between the input and output, as shown in Figure D-8 (a). However, the delay time between the input and output can be ignored when test patterns are generated, as shown in Figure D-8 (b). The patterns must be generated so that the entire circuit operates by the same timing.

Figure D-8. Timing Chart

(a) Actual circuit



(b) Timing chart entry (Test pattern entry)



Entry example

	Mode No.	Assigned Pin	Output Load (pF)	Pattern No.	Delay Time (ns)		Determination
					MIN.	MAX.	
1	1	IN1 → OUT2	15	131	13	50	○
2							
3							
4							
5							
6							

APPENDIX E LIST OF BLOCKS

E.1 Interface Block

E.1.1 3.3 V Interface

Function	Block	Description	Cells (I/O)
Input Buffer	FI01	-	7 (1)
	FID1	50 kΩ Pull-down	7 (1)
	FIU1	50 kΩ Pull-up	7 (1)
	FIW1	5 kΩ Pull-up	7 (1)
	FIS1	Schmitt	11 (1)
	FDS1	Schmitt 50 kΩ Pull-down	11 (1)
	FUS1	Schmitt 50 kΩ Pull-up	11 (1)
	FWS1	Schmitt 5 kΩ Pull-up	11 (1)
	FIB1	Clock Driver	56 (1)
	FDB1	Clock Driver 50 kΩ Pull-down	56 (1)
	FUB1	Clock Driver 50 kΩ Pull-up	56 (1)
	FWB1	Clock Driver 5 kΩ Pull-up	56 (1)
Input Buffer with Failsafe	FIA1	-	7 (1)
	FDA1	50 kΩ Pull-down	7 (1)
	FIE1	Schmitt	11 (1)
	FDE1	Schmitt 50 kΩ Pull-down	11 (1)
	FIH1	Clock Driver	56 (1)
	FDH1	Clock Driver 50 kΩ Pull-down	56 (1)
Input Buffer with EN (AND)	FN11	-	8 (1)
	FN21	50 kΩ Pull-down	8 (1)
Input Buffer with EN (OR)	FN13	-	8 (1)
	FN23	50 kΩ Pull-down	8 (1)
Output Buffer	FO09	3 mA	8 (1)
	FO04	6 mA	8 (1)
	FO01	9 mA	8 (1)
	FO02	12 mA	8 (1)
	FO03	18 mA	18 (1)
	FO06	24 mA	18 (1)
Low-noise Output Buffer	FE04	6 mA	10 (1)
	FE01	9 mA	10 (1)
	FE02	12 mA	10 (1)
	FE03	18 mA	10 (1)
	FE06	24 mA	10 (1)

Function	Block	Description	Cells (I/O)
3-State Buffer	B00T	3 mA	18 (1)
	B0DT	3 mA 50 kΩ Pull-down	18 (1)
	B0UT	3 mA 50 kΩ Pull-up	18 (1)
	B0WT	3 mA 5 kΩ Pull-up	18 (1)
	B00E	6 mA	18 (1)
	B0DE	6 mA 50 kΩ Pull-down	18 (1)
	B0UE	6 mA 50 kΩ Pull-up	18 (1)
	B0WE	6 mA 5 kΩ Pull-up	18 (1)
	B008	9 mA	18 (1)
	B0D8	9 mA 50 kΩ Pull-down	18 (1)
	B0U8	9 mA 50 kΩ Pull-up	18 (1)
	B0W8	9 mA 5 kΩ Pull-up	18 (1)
	B007	12 mA	18 (1)
	B0D7	12 mA 50 kΩ Pull-down	18 (1)
	B0U7	12 mA 50 kΩ Pull-up	18 (1)
	B0W7	12 mA 5 kΩ Pull-up	18 (1)
	B009	18 mA	20 (1)
	B0D9	18 mA 50 kΩ Pull-down	20 (1)
	B0U9	18 mA 50 kΩ Pull-up	20 (1)
	B0W9	18 mA 5 kΩ Pull-up	20 (1)
	B00H	24 mA	20 (1)
	B0DH	24 mA 50 kΩ Pull-down	20 (1)
	B0UH	24 mA 50 kΩ Pull-up	20 (1)
	B0WH	24 mA 5 kΩ Pull-up	20 (1)
Low-noise 3-State Buffer	BE0E	6 mA	11 (1)
	BEDE	6 mA 50 kΩ Pull-down	11 (1)
	BEUE	6 mA 50 kΩ Pull-up	11 (1)
	BEWE	6 mA 5 kΩ Pull-up	11 (1)
	BE08	9 mA	11 (1)
	BED8	9 mA 50 kΩ Pull-down	11 (1)
	BEU8	9 mA 50 kΩ Pull-up	11 (1)
	BEW8	9 mA 5 kΩ Pull-up	11 (1)
	BE07	12 mA	11 (1)
	BED7	12 mA 50 kΩ Pull-down	11 (1)
	BEU7	12 mA 50 kΩ Pull-up	11 (1)
	BEW7	12 mA 5 kΩ Pull-up	11 (1)
	BE09	18 mA	11 (1)
	BED9	18 mA 50 kΩ Pull-down	11 (1)
	BEU9	18 mA 50 kΩ Pull-up	11 (1)
	BEW9	18 mA 5 kΩ Pull-up	11 (1)
	BE0H	24 mA	11 (1)
	BEDH	24 mA 50 kΩ Pull-down	11 (1)
	BEUH	24 mA 50 kΩ Pull-up	11 (1)
	BEWH	24 mA 5 kΩ Pull-up	11 (1)

Function	Block	Description	Cells (I/O)
N-ch Open drain Buffer	EXTH	3 mA	8 (1)
	EXUH	3 mA 50 kΩ Pull-up	8 (1)
	EXWH	3 mA 5 kΩ Pull-up	8 (1)
	EXTJ	6 mA	8 (1)
	EXUJ	6 mA 50 kΩ Pull-up	8 (1)
	EXWJ	6 mA 5 kΩ Pull-up	8 (1)
	EXT1	9 mA	8 (1)
	EXT3	9 mA 50 kΩ Pull-up	8 (1)
	EXW3	9 mA 5 kΩ Pull-up	8 (1)
	EXT9	12 mA	8 (1)
	EXTB	12 mA 50 kΩ Pull-up	8 (1)
	EXWB	12 mA 5 kΩ Pull-up	8 (1)
	EXT5	18 mA	18 (1)
	EXT7	18 mA 50 kΩ Pull-up	18 (1)
	EXW7	18 mA 5 kΩ Pull-up	18 (1)
	EXTD	24 mA	18 (1)
	EXTF	24 mA 50 kΩ Pull-up	18 (1)
	EXWF	24 mA 5 kΩ Pull-up	18 (1)
Low-noise N-ch Open drain Buffer	EETJ	6 mA	5 (1)
	EEUJ	6 mA 50 kΩ Pull-up	5 (1)
	EEWJ	6 mA 5 kΩ Pull-up	5 (1)
	EET1	9 mA	5 (1)
	EET3	9 mA 50 kΩ Pull-up	5 (1)
	EEW3	9 mA 5 kΩ Pull-up	5 (1)
	EET9	12 mA	5 (1)
	EETB	12 mA 50 kΩ Pull-up	5 (1)
	EEWB	12 mA 5 kΩ Pull-up	5 (1)
	EET5	18 mA	5 (1)
	EET7	18 mA 50 kΩ Pull-up	5 (1)
	EEW7	18 mA 5 kΩ Pull-up	5 (1)
	EETD	24 mA	5 (1)
	EETF	24 mA 50 kΩ Pull-up	5 (1)
	EEWF	24 mA 5 kΩ Pull-up	5 (1)

Function	Block	Description	Cells (I/O)
I/O Buffer	B00U	3 mA	25 (1)
	B0DU	3 mA 50 kΩ Pull-down	25 (1)
	B0UU	3 mA 50 kΩ Pull-up	25 (1)
	B0WU	3 mA 5 kΩ Pull-up	25 (1)
	B00C	6 mA	25 (1)
	B0DC	6 mA 50 kΩ Pull-down	25 (1)
	B0UC	6 mA 50 kΩ Pull-up	25 (1)
	B0WC	6 mA 5 kΩ Pull-up	25 (1)
	B003	9 mA	25 (1)
	B0D3	9 mA 50 kΩ Pull-down	25 (1)
	B0U3	9 mA 50 kΩ Pull-up	25 (1)
	B0W3	9 mA 5 kΩ Pull-up	25 (1)
	B001	12 mA	25 (1)
	B0D1	12 mA 50 kΩ Pull-down	25 (1)
	B0U1	12 mA 50 kΩ Pull-up	25 (1)
	B0W1	12 mA 5 kΩ Pull-up	25 (1)
	B005	18 mA	27 (1)
	B0D5	18 mA 50 kΩ Pull-down	27 (1)
	B0U5	18 mA 50 kΩ Pull-up	27 (1)
	B0W5	18 mA 5 kΩ Pull-up	27 (1)
	B00F	24 mA	27 (1)
	B0DF	24 mA 50 kΩ Pull-down	27 (1)
	B0UF	24 mA 50 kΩ Pull-up	27 (1)
	B0WF	24 mA 5 kΩ Pull-up	27 (1)
Low-noise I/O Buffer	BE0C	6 mA	18 (1)
	BEDC	6 mA 50 kΩ Pull-down	18 (1)
	BEUC	6 mA 50 kΩ Pull-up	18 (1)
	BEWC	6 mA 5 kΩ Pull-up	18 (1)
	BE03	9 mA	18 (1)
	BED3	9 mA 50 kΩ Pull-down	18 (1)
	BEU3	9 mA 50 kΩ Pull-up	18 (1)
	BEW3	9 mA 5 kΩ Pull-up	18 (1)
	BE01	12 mA	18 (1)
	BED1	12 mA 50 kΩ Pull-down	18 (1)
	BEU1	12 mA 50 kΩ Pull-up	18 (1)
	BEW1	12 mA 5 kΩ Pull-up	18 (1)
	BE05	18 mA	18 (1)
	BED5	18 mA 50 kΩ Pull-down	18 (1)
	BEU5	18 mA 50 kΩ Pull-up	18 (1)
	BEW5	18 mA 5 kΩ Pull-up	18 (1)
	BE0F	24 mA	18 (1)
	BEDF	24 mA 50 kΩ Pull-down	18 (1)
	BEUF	24 mA 50 kΩ Pull-up	18 (1)
	BEWF	24 mA 5 kΩ Pull-up	18 (1)

Function	Block	Description	Cells (I/O)
Schmitt I/O Buffer	BSIU	3 mA	29 (1)
	BSDU	3 mA 50 kΩ Pull-down	29 (1)
	BSUU	3 mA 50 kΩ Pull-up	29 (1)
	BSWU	3 mA 5 kΩ Pull-up	29 (1)
	BSIC	6 mA	29 (1)
	BSDC	6 mA 50 kΩ Pull-down	29 (1)
	BSUC	6 mA 50 kΩ Pull-up	29 (1)
	BSWC	6 mA 5 kΩ Pull-up	29 (1)
	BSI3	9 mA	29 (1)
	BSD3	9 mA 50 kΩ Pull-down	29 (1)
	BSU3	9 mA 50 kΩ Pull-up	29 (1)
	BSW3	9 mA 5 kΩ Pull-up	29 (1)
	BSI1	12 mA	29 (1)
	BSD1	12 mA 50 kΩ Pull-down	29 (1)
	BSU1	12 mA 50 kΩ Pull-up	29 (1)
	BSW1	12 mA 5 kΩ Pull-up	29 (1)
	BSI5	18 mA	31 (1)
	BSD5	18 mA 50 kΩ Pull-down	31 (1)
	BSU5	18 mA 50 kΩ Pull-up	31 (1)
	BSW5	18 mA 5 kΩ Pull-up	31 (1)
	BSIF	24 mA	31 (1)
	BSDF	24 mA 50 kΩ Pull-down	31 (1)
	BSUF	24 mA 50 kΩ Pull-up	31 (1)
	BSWF	24 mA 5 kΩ Pull-up	31 (1)
Low-noise Schmitt I/O Buffer	BFIC	6 mA	22 (1)
	BFDC	6 mA 50 kΩ Pull-down	22 (1)
	BFUC	6 mA 50 kΩ Pull-up	22 (1)
	BFWC	6 mA 5 kΩ Pull-up	22 (1)
	BFI3	9 mA	22 (1)
	BFD3	9 mA 50 kΩ Pull-down	22 (1)
	BFU3	9 mA 50 kΩ Pull-up	22 (1)
	BFW3	9 mA 5 kΩ Pull-up	22 (1)
	BFI1	12 mA	22 (1)
	BFD1	12 mA 50 kΩ Pull-down	22 (1)
	BFU1	12 mA 50 kΩ Pull-up	22 (1)
	BFW1	12 mA 5 kΩ Pull-up	22 (1)
	BFI5	18 mA	22 (1)
	BFD5	18 mA 50 kΩ Pull-down	22 (1)
	BFU5	18 mA 50 kΩ Pull-up	22 (1)
	BFW5	18 mA 5 kΩ Pull-up	22 (1)
	BFIF	24 mA	22 (1)
	BFDF	24 mA 50 kΩ Pull-down	22 (1)
	BFUF	24 mA 50 kΩ Pull-up	22 (1)
	BFWF	24 mA 5 kΩ Pull-up	22 (1)

Function	Block	Description	Cells (I/O)
I/O Buffer with EN (AND)	BN2U	3 mA	26 (1)
	BN4U	3 mA 50 kΩ Pull-down	26 (1)
	BN2C	6 mA	26 (1)
	BN4C	6 mA 50 kΩ Pull-down	26 (1)
	BN23	9 mA	26 (1)
	BN43	9 mA 50 kΩ Pull-down	26 (1)
	BN21	12 mA	26 (1)
	BN41	12 mA 50 kΩ Pull-down	26 (1)
	BN25	18 mA	28 (1)
	BN45	18 mA 50 kΩ Pull-down	28 (1)
	BN2F	24 mA	28 (1)
	BN4F	24 mA 50 kΩ Pull-down	28 (1)
I/O Buffer with EN (OR)	BN3U	3 mA	26 (1)
	BN5U	3 mA 50 kΩ Pull-down	26 (1)
	BN3C	6 mA	26 (1)
	BN5C	6 mA 50 kΩ Pull-down	26 (1)
	BN33	9 mA	26 (1)
	BN53	9 mA 50 kΩ Pull-down	26 (1)
	BN31	12 mA	26 (1)
	BN51	12 mA 50 kΩ Pull-down	26 (1)
	BN35	18 mA	28 (1)
	BN55	18 mA 50 kΩ Pull-down	28 (1)
	BN3F	24 mA	28 (1)
	BN5F	24 mA 50 kΩ Pull-down	28 (1)

E.1.2 5 V Interface

Function		Block	Description	Cells (I/O)
Input Buffer		FIV1	-	7 (1)
		FDV1	50 kΩ Pull-down	7 (1)
		FIF1	Schmitt	11 (1)
		FDF1	Schmitt 50 kΩ Pull-down	11 (1)
		FIG1	Clock Driver	56 (1)
		FDG1	Clock Driver 50 kΩ Pull-down	56 (1)
Input Buffer with EN (AND)		FN1135	-	8 (1)
		FN2135	50 kΩ Pull-down	8 (1)
Input Buffer with EN (OR)		FN1335	-	8 (1)
		FN2335	50 kΩ Pull-down	8 (1)
CMOS Level	Output Buffer	FY09	3 mA	26 (1)
		FY04	6 mA	26 (1)
		FY01	9 mA	28 (1)
		FY02	12 mA	28 (1)
		FY03	18 mA	28 (1)
		FY06	24 mA	28 (1)

Function		Block	Description	Cells (I/O)
CMOS Level	Low-noise Output Buffer	FZ02	12 mA	28 (1)
		FZ03	18 mA	28 (1)
		FZ06	24 mA	28 (1)
	3-State Buffer	BD0T	3 mA	45 (1)
		BD0E	6 mA	45 (1)
		BD08	9 mA	47 (1)
		BD07	12 mA	47 (1)
		BD09	18 mA	47 (1)
		BD0H	24 mA	47 (1)
	Low-noise 3-State Buffer	BJ07	12 mA	40 (1)
		BJ09	18 mA	40 (1)
		BJ0H	24 mA	40 (1)
	I/O Buffer	BM0U	3 mA	52 (1)
		BM0C	6 mA	52 (1)
		BM03	9 mA	54 (1)
		BM01	12 mA	54 (1)
		BM05	18 mA	54 (1)
		BM0F	24 mA	54 (1)
	Low-noise I/O Buffer	BP01	12 mA	47 (1)
		BP05	18 mA	47 (1)
		BP0F	24 mA	47 (1)
	Schmitt I/O Buffer	BQIU	3 mA	56 (1)
		BQIC	6 mA	56 (1)
		BQI3	9 mA	58 (1)
		BQI1	12 mA	58 (1)
		BQI5	18 mA	58 (1)
		BQIF	24 mA	58 (1)
	Low-noise Schmitt I/O Buffer	BUI1	12 mA	51 (1)
		BUI5	18 mA	51 (1)
		BUIF	24 mA	51 (1)
	I/O Buffer with EN (AND)	BNXU35	3 mA	53 (1)
		BNXC35	6 mA	53 (1)
		BNX335	9 mA	55 (1)
		BNX135	12 mA	55 (1)
		BNX535	18 mA	55 (1)
		BNXF35	24 mA	55 (1)
	I/O Buffer with EN (OR)	BNMU35	3 mA	53 (1)
		BNMC35	6 mA	53 (1)
		BNM335	9 mA	55 (1)
		BNM135	12 mA	55 (1)
		BNM535	18 mA	55 (1)
		BNMF35	24 mA	55 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Output Buffer	FV0A	1 mA	8 (1)
		FV0B	2 mA	8 (1)
		FV09	3 mA	8 (1)
		FV04	6 mA	8 (1)
		FV01	9 mA	18 (1)
		FV02	12 mA	18 (1)
		FV03	18 mA	18 (1)
		FV06	24 mA	18 (1)
	Low-noise Output Buffer	FW02	12 mA	10 (1)
		FW03	18 mA	10 (1)
		FW06	24 mA	10 (1)
	3-State Buffer	BV0Q	1 mA	40 (1)
		BVDQ	1 mA 50 kΩ Pull-down	40 (1)
		BV0M	2 mA	40 (1)
		BVDM	2 mA 50 kΩ Pull-down	40 (1)
		BV0T	3 mA	40 (1)
		BVDT	3 mA 50 kΩ Pull-down	40 (1)
		BV0E	6 mA	40 (1)
		BVDE	6 mA 50 kΩ Pull-down	40 (1)
		BV08	9 mA	42 (1)
		BVD8	9 mA 50 kΩ Pull-down	42 (1)
		BV07	12 mA	42 (1)
		BVD7	12 mA 50 kΩ Pull-down	42 (1)
		BV09	18 mA	42 (1)
		BVD9	18 mA 50 kΩ Pull-down	42 (1)
		BV0H	24 mA	42 (1)
		BVDH	24 mA 50 kΩ Pull-down	42 (1)
	Low-noise 3-State Buffer	BY07	12 mA	28 (1)
		BYD7	12 mA 50 kΩ Pull-down	28 (1)
		BY09	18 mA	28 (1)
		BYD9	18 mA 50 kΩ Pull-down	28 (1)
		BY0H	24 mA	28 (1)
		BYDH	24 mA 50 kΩ Pull-down	28 (1)
	N-ch Open drain Buffer	EVTT	1 mA	8 (1)
		EVTK	2 mA	8 (1)
		EVTH	3 mA	8 (1)
		EVTJ	6 mA	8 (1)
		EVT1	9 mA	18 (1)
		EVT9	12 mA	18 (1)
		EVT5	18 mA	18 (1)
		EVTD	24 mA	18 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Low-noise N-ch Open drain Buffer	EYT9	12 mA	5 (1)
		EYT5	18 mA	5 (1)
		EYTD	24 mA	5 (1)
	I/O Buffer	BW0X	1 mA	47 (1)
		BWDX	1 mA 50 kΩ Pull-down	47 (1)
		BW0K	2 mA	47 (1)
		BWDK	2 mA 50 kΩ Pull-down	47 (1)
		BW0U	3 mA	47 (1)
		BWDU	3 mA 50 kΩ Pull-down	47 (1)
		BW0C	6 mA	47 (1)
		BWDC	6 mA 50 kΩ Pull-down	47 (1)
		BW03	9 mA	49 (1)
		BWD3	9 mA 50 kΩ Pull-down	49 (1)
		BW01	12 mA	49 (1)
		BWD1	12 mA 50 kΩ Pull-down	49 (1)
		BW05	18 mA	49 (1)
		BWD5	18 mA 50 kΩ Pull-down	49 (1)
		BW0F	24 mA	49 (1)
		BWDF	24 mA 50 kΩ Pull-down	49 (1)
	Low-noise I/O Buffer	BX01	12 mA	35 (1)
		BXD1	12 mA 50 kΩ Pull-down	35 (1)
		BX05	18 mA	35 (1)
		BXD5	18 mA 50 kΩ Pull-down	35 (1)
		BX0F	24 mA	35 (1)
		BXDF	24 mA 50 kΩ Pull-down	35 (1)
	Schmitt I/O Buffer	BKIX	1 mA	51 (1)
		BKDX	1 mA 50 kΩ Pull-down	51 (1)
		BKIK	2 mA	51 (1)
		BKDK	2 mA 50 kΩ Pull-down	51 (1)
		BKIU	3 mA	51 (1)
		BKDU	3 mA 50 kΩ Pull-down	51 (1)
		BKIC	6 mA	51 (1)
		BKDC	6 mA 50 kΩ Pull-down	51 (1)
		BKI3	9 mA	53 (1)
		BKD3	9 mA 50 kΩ Pull-down	53 (1)
		BKI1	12 mA	53 (1)
		BKD1	12 mA 50 kΩ Pull-down	53 (1)
		BKI5	18 mA	53 (1)
		BKD5	18 mA 50 kΩ Pull-down	53 (1)
		BKIF	24 mA	53 (1)
		BKDF	24 mA 50 kΩ Pull-down	53 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Low-noise Schmitt I/O Buffer	BZI1	12 mA	39 (1)
		BZD1	12 mA 50 kΩ Pull-down	39 (1)
		BZI5	18 mA	39 (1)
		BZD5	18 mA 50 kΩ Pull-down	39 (1)
		BZIF	24 mA	39 (1)
		BZDF	24 mA 50 kΩ Pull-down	39 (1)
	I/O Buffer with EN (AND)	BNXV35	3 mA	48 (1)
		BNYV35	3 mA 50 kΩ Pull-down	48 (1)
		BNXD35	6 mA	48 (1)
		BNYD35	6 mA 50 kΩ Pull-down	48 (1)
		BNX435	9 mA	50 (1)
		BNY435	9 mA 50 kΩ Pull-down	50 (1)
		BNX235	12 mA	50 (1)
		BNY235	12 mA 50 kΩ Pull-down	50 (1)
		BNX635	18 mA	50 (1)
		BNY635	18 mA 50 kΩ Pull-down	50 (1)
		BNXG35	24 mA	50 (1)
		BNYG35	24 mA 50 kΩ Pull-down	50 (1)
	I/O Buffer with EN (OR)	BNMV35	3 mA	48 (1)
		BNVV35	3 mA 50 kΩ Pull-down	48 (1)
		BNMD35	6 mA	48 (1)
		BNVD35	6 mA 50 kΩ Pull-down	48 (1)
		BNM435	9 mA	50 (1)
		BNV435	9 mA 50 kΩ Pull-down	50 (1)
		BNM235	12 mA	50 (1)
		BNV235	12 mA 50 kΩ Pull-down	50 (1)
		BNM635	18 mA	50 (1)
		BNV635	18 mA 50 kΩ Pull-down	50 (1)
		BNMG35	24 mA	50 (1)
		BNVG35	24 mA 50 kΩ Pull-down	50 (1)

E.1.3 Oscillator

Function	Block	Description	Cells (I/O)
Oscillator Input Buffer	OSI1	-	0 (1)
Oscillator Input Buffer for Enable	OSI2	-	0 (1)
Oscillator Output Buffer (Internal Feedback Resistor)	OSO1	-	0 (1)
Oscillator Output Buffer (for OSF Type)	OSO3	-	0 (1)
Oscillator Output Buffer (for Enable Type)	OSO7	-	0 (1)
Oscillator Output Buffer (External Feedback Resistor)	OSO9	-	0 (1)
Feedback Resistor for Oscillator	OSF1	-	0 (1)
Feedback Resistor for Oscillator For Enable	OSF3	-	0 (1)

E.1.4 PCI

Function	Block	Description	Cells (I/O)
3V PCI Input Buffer	BP3I	-	7 (1)
3V PCI Output Buffer	BP3O	-	18 (1)
3V PCI 3-State Buffer	BP3T	-	20 (1)
3V PCI I/O Buffer	BP3B	-	27 (1)
5V PCI Input Buffer	BP5I	-	7 (1)
5V PCI Output Buffer	BP5O	-	18 (1)
5V PCI 3-State Buffer	BP5T	-	42 (1)
5V PCI I/O Buffer	BP5B	-	49 (1)

E.1.5 High Speed Signal Transmission

Function	Block	Description	Cells (I/O)
3V GTL/GTL+/P-ECL Input Buffer for Enable Terminal	FIXA	-	56 (1)
	FUXA	50 kΩ Pull-up	56 (1)
5V GTL/GTL+/P-ECL Input Buffer for Enable Terminal	FIZA	-	56 (1)
GTL+ Input Buffer with EN	FIR2	-	19 (1)
GTL+ Input Buffer for Reference VOLTAGE	FIP2	-	0 (1)
GTL+ Output Buffer with ENB	ELTL	-	6 (1)
GTL+ I/O Buffer	BL0W	-	25 (1)

E.1.6 PLL

Function	Block	**Description**	Cells (I/O)
3V Input Buffer Reference Clock	FI0P	-	7 (1)
5V Input Buffer Reference Clock	FI0Q	-	7 (1)
DPLL (Phase locked loop)	F9E4	-	3770 (-)
DPLL (Phase locked loop-Clock multiply)	F9H3	-	15840 (-)
DPLL (Phase locked loop-Clock multiply)	F9H2	-	9000 (-)

E.2 Function Block

E.2.1 Level Generator

Function	Block	Description	Cells (I/O)
H,L Level Generator	F091	-	1 (-)

E.2.2 Inverter, Buffer, CTS Driver, Delay Gate

Function	Block	Description	Cells (I/O)
Inverter	L101	Single Out (Low Power)	1 (-)
	F101	Single Out	1 (-)
	F102	Single Out (X2 Drive)	2 (-)
	F143K	Single Out (X3 Drive)	3 (-)
	F144K	Single Out (X4 Drive)	4 (-)
	F145K	Single Out (X5 Drive)	5 (-)
	F146K	Single Out (X6 Drive)	6 (-)
	F148K	Single Out (X8 Drive)	12 (-)
	F148P	Single Out (X8 Drive)	8 (-)
	F148BR	Single Out (X8 Drive)	12 (-)
	F14AK	Single Out (X12 Drive)	21 (-)
Buffer	L111	Single Out (Low Power)	1 (-)
	F111	Single Out	2 (-)
	F112	Single Out (X2 Drive)	3 (-)
	F153K	Single Out (X3 Drive)	4 (-)
	F154K	Single Out (X4 Drive)	5 (-)
	F158K	Single Out (X8 Drive)	11 (-)
	F158BR	Single Out (X8 Drive)	11 (-)
	F15AK	Single Out (X12 Drive)	20 (-)
CTS Driver (Buffer Type)	FC52	Single type	100 (-)
	FC92	Single type (X2 Drive)	143 (-)
	FC53	Standard type	1905 (-)
	FC93	Standard type (X2 Drive)	1727 (-)
	FC54	Double type	36200 (-)
	FC94	Double type (X2 Drive)	20735 (-)
Delay Gate	F131	-	6 (-)
	F132	-	10 (-)
	F137	-	18 (-)
	F138	-	34 (-)

E.2.3 OR (NOR), AND (NAND)

Function	Block	Description	Cells (I/O)
2-Input NOR	L202	(Low Power)	1 (-)
	F202	-	2 (-)
	F222	(X2 Drive)	4 (-)
	F282	(X4 Drive)	6 (-)
	F2C2K	(X8 Drive)	12 (-)
	L202N1	1-Input Inverter (Low Power)	2 (-)
	F202N1	1-Input Inverter	3 (-)
	F222N1	1-Input Inverter (X2 Drive)	5 (-)
	F282N1	1-Input Inverter (X4 Drive)	7 (-)
3-Input NOR	F203	-	3 (-)
	F223	(X2 Drive)	6 (-)
	F2C3	(X4 Drive)	9 (-)
	F2C3NS	(X4 Drive)	12 (-)
	F203N1	1-Input Inverter	4 (-)
	F223N1	1-Input Inverter (X2 Drive)	7 (-)
	F2C3N1	1-Input Inverter (X4 Drive)	10 (-)
	F2C3N1S	1-Input Inverter (X4 Drive)	14 (-)
	F203N2	2-Input Inverter	4 (-)
	F223N2	2-Input Inverter (X2 Drive)	7 (-)
	F2C3N2	2-Input Inverter (X4 Drive)	9 (-)
	F2C3N2S	2-Input Inverter (X4 Drive)	12 (-)
4-Input NOR	L204	(Low Power)	4 (-)
	F204	-	4 (-)
	F224	(X2 Drive)	8 (-)
	L204N1	1-Input Inverter (Low Power)	4 (-)
	F204N1	1-Input Inverter	5 (-)
	F224N1	1-Input Inverter (X2 Drive)	9 (-)
	L204N2	2-Input Inverter (Low Power)	5 (-)
	F204N2	2-Input Inverter	5 (-)
	F224N2	2-Input Inverter (X2 Drive)	9 (-)
5-Input NOR	L205	(Low Power)	4 (-)
	F205	-	5 (-)
	F225	(X2 Drive)	6 (-)
	L205N1	1-Input Inverter (Low Power)	5 (-)
	F205N1	1-Input Inverter	6 (-)
	F225N1	1-Input Inverter (X2 Drive)	6 (-)
	L205N2	2-Input Inverter (Low Power)	5 (-)
	F205N2	2-Input Inverter	6 (-)
	F225N2	2-Input Inverter (X2 Drive)	7 (-)
	L205N3	3-Input Inverter (Low Power)	6 (-)
	F205N3	3-Input Inverter	7 (-)
	F225N3	3-Input Inverter (X2 Drive)	7 (-)

Function	Block	Description	Cells (I/O)
6-Input NOR	F206	-	5 (-)
	F226	(X2 Drive)	6 (-)
	L206N1	1-Input Inverter (Low Power)	5 (-)
	F206N1	1-Input Inverter	6 (-)
	F226N1	1-Input Inverter (X2 Drive)	7 (-)
	F206N2	2-Input Inverter	6 (-)
	F226N2	2-Input Inverter (X2 Drive)	7 (-)
	L206N3	3-Input Inverter (Low Power)	6 (-)
	F206N3	3-Input Inverter	7 (-)
	F226N3	3-Input Inverter (X2 Drive)	8 (-)
8-Input NOR	L208	(Low Power)	7 (-)
	F208	-	7 (-)
	F228	(X2 Drive)	8 (-)
	L208N1	1-Input Inverter (Low Power)	8 (-)
	F208N1	1-Input Inverter	8 (-)
	F228N1	1-Input Inverter (X2 Drive)	9 (-)
	L208N2	2-Input Inverter (Low Power)	8 (-)
	F208N2	2-Input Inverter	8 (-)
	F228N2	2-Input Inverter (X2 Drive)	9 (-)
	L208N3	3-Input Inverter (Low Power)	9 (-)
	F208N3	3-Input Inverter	9 (-)
	F228N3	3-Input Inverter (X2 Drive)	10 (-)
	L208N4	4-Input Inverter (Low Power)	9 (-)
	F208N4	4-Input Inverter	9 (-)
	F228N4	4-Input Inverter (X2 Drive)	10 (-)
2-Input OR	L212	(Low Power)	2 (-)
	F212	-	2 (-)
	F232	(X2 Drive)	3 (-)
	F252	(X4 Drive)	6 (-)
	F232NS	(X2 Drive)	4 (-)
	F2D2	(X4 Drive)	7 (-)
3-Input OR	L213	(Low Power)	2 (-)
	F213	-	3 (-)
	F233	(X2 Drive)	4 (-)
	F233NS	(X2 Drive)	5 (-)
	F2D3	(X4 Drive)	9 (-)
4-Input OR	L214	(Low Power)	3 (-)
	F214	-	3 (-)
	F234	(X2 Drive)	4 (-)
	L214N1	1-Input Inverter (Low Power)	3 (-)
	F214N1	1-Input Inverter	4 (-)
	F234N1	1-Input Inverter (X2 Drive)	5 (-)

Function	Block	Description	Cells (I/O)
5-Input OR	L215	(Low Power)	4 (-)
	F215	-	5 (-)
	F235	(X2 Drive)	7 (-)
	L215N1	1-Input Inverter (Low Power)	4 (-)
	F215N1	1-Input Inverter	5 (-)
	F235N1	1-Input Inverter (X2 Drive)	8 (-)
6-Input OR	L216	(Low Power)	4 (-)
	F216	-	5 (-)
	F236	(X2 Drive)	7 (-)
	L216N1	1-Input Inverter (Low Power)	5 (-)
	F216N1	1-Input Inverter	6 (-)
	F236N1	1-Input Inverter (X2 Drive)	8 (-)
	L216N2	2-Input Inverter (Low Power)	5 (-)
	F216N2	2-Input Inverter	6 (-)
	F236N2	2-Input Inverter (X2 Drive)	8 (-)
8-Input OR	L218	(Low Power)	6 (-)
	F218	-	8 (-)
	F238	(X2 Drive)	9 (-)
	L218N1	1-Input Inverter (Low Power)	7 (-)
	F218N1	1-Input Inverter	9 (-)
	F238N1	1-Input Inverter (X2 Drive)	10 (-)
	L218N2	2-Input Inverter (Low Power)	7 (-)
	F218N2	2-Input Inverter	9 (-)
	F238N2	2-Input Inverter (X2 Drive)	10 (-)
	L218N3	3-Input Inverter (Low Power)	8 (-)
	F218N3	3-Input Inverter	10 (-)
	F238N3	3-Input Inverter (X2 Drive)	11 (-)
2-Input NAND	L302	(Low Power)	1 (-)
	F302	-	2 (-)
	F322	(X2 Drive)	4 (-)
	F382	(X4 Drive)	6 (-)
	F3C2K	(X8 Drive)	12 (-)
	F382NS	(X4 Drive)	8 (-)
	L302N1	1-Input Inverter (Low Power)	2 (-)
	F302N1	1-Input Inverter	3 (-)
	F322N1	1-Input Inverter (X2 Drive)	5 (-)
	F382N1	1-Input Inverter (X4 Drive)	7 (-)
	F382N1S	1-Input Inverter (X4 Drive)	10 (-)

Function	Block	Description	Cells (I/O)
3-Input NAND	L303	(Low Power)	2 (-)
	F303	-	3 (-)
	F323	(X2 Drive)	6 (-)
	F3C3	(X4 Drive)	9 (-)
	F3C3NS	(X4 Drive)	12 (-)
	L303N1	1-Input Inverter (Low Power)	2 (-)
	F303N1	1-Input Inverter	4 (-)
	F323N1	1-Input Inverter (X2 Drive)	7 (-)
	F3C3N1	1-Input Inverter (X4 Drive)	10 (-)
	F3C3N1S	1-Input Inverter (X4 Drive)	14 (-)
	L303N2	2-Input Inverter (Low Power)	3 (-)
	F303N2	2-Input Inverter	4 (-)
	F323N2	2-Input Inverter (X2 Drive)	7 (-)
	F3C3N2	2-Input Inverter (X4 Drive)	10 (-)
	F3C3N2S	2-Input Inverter (X4 Drive)	16 (-)
4-Input NAND	L304	(Low Power)	2 (-)
	F304	-	4 (-)
	F324	(X2 Drive)	8 (-)
	F3C4	(X4 Drive)	10 (-)
	F3C4NS	(X4 Drive)	16 (-)
	L304N1	1-Input Inverter (Low Power)	3 (-)
	F304N1	1-Input Inverter	5 (-)
	F324N1	1-Input Inverter (X2 Drive)	9 (-)
	F3C4N1	1-Input Inverter (X4 Drive)	11 (-)
	F3C4N1S	1-Input Inverter (X4 Drive)	18 (-)
	L304N2	2-Input Inverter (Low Power)	3 (-)
	F304N2	2-Input Inverter	5 (-)
	F324N2	2-Input Inverter (X2 Drive)	9 (-)
	F3C4N2	2-Input Inverter (X4 Drive)	11 (-)
	F3C4N2S	2-Input Inverter (X4 Drive)	20 (-)
5-Input NAND	L305	(Low Power)	4 (-)
	F305	-	5 (-)
	F325	(X2 Drive)	6 (-)
	L305N1	1-Input Inverter (Low Power)	5 (-)
	F305N1	1-Input Inverter	6 (-)
	F325N1	1-Input Inverter (X2 Drive)	6 (-)
	L305N2	2-Input Inverter (Low Power)	5 (-)
	F305N2	2-Input Inverter	6 (-)
	F325N2	2-Input Inverter (X2 Drive)	7 (-)
	L305N3	3-Input Inverter (Low Power)	6 (-)
	F305N3	3-Input Inverter	7 (-)
	F325N3	3-Input Inverter (X2 Drive)	7 (-)

Function	Block	Description	Cells (I/O)
6-Input NAND	L306	(Low Power)	5 (-)
	F306	-	5 (-)
	F326	(X2 Drive)	6 (-)
	L306N1	1-Input Inverter (Low Power)	5 (-)
	F306N1	1-Input Inverter	6 (-)
	F326N1	1-Input Inverter (X2 Drive)	7 (-)
	L306N2	2-Input Inverter (Low Power)	6 (-)
	F306N2	2-Input Inverter	6 (-)
	F326N2	2-Input Inverter (X2 Drive)	7 (-)
	L306N3	3-Input Inverter (Low Power)	6 (-)
	F306N3	3-Input Inverter	7 (-)
	F326N3	3-Input Inverter (X2 Drive)	8 (-)
8-Input NAND	F308	-	6 (-)
	F328	(X2 Drive)	7 (-)
	L308N1	1-Input Inverter (Low Power)	6 (-)
	F308N1	1-Input Inverter	7 (-)
	F328N1	1-Input Inverter (X2 Drive)	8 (-)
	F308N2	2-Input Inverter	7 (-)
	F328N2	2-Input Inverter (X2 Drive)	8 (-)
	L308N3	3-Input Inverter (Low Power)	7 (-)
	F308N3	3-Input Inverter	8 (-)
	F328N3	3-Input Inverter (X2 Drive)	9 (-)
	F308N4	4-Input Inverter	8 (-)
	F328N4	4-Input Inverter (X2 Drive)	9 (-)
2-Input AND	L312	(Low Power)	2 (-)
	F312	-	2 (-)
	F332	(X2 Drive)	3 (-)
	F352	(X4 Drive)	6 (-)
	F3D2	(X8 Drive)	16 (-)
	F332NS	(X2 Drive)	4 (-)
	F352NS	(X4 Drive)	7 (-)
3-Input AND	L313	(Low Power)	2 (-)
	F313	-	3 (-)
	F333	(X2 Drive)	4 (-)
	F3D3	(X4 Drive)	9 (-)
	F333NS	(X2 Drive)	5 (-)
4-Input AND	L314	(Low Power)	3 (-)
	F314	-	3 (-)
	F334	(X2 Drive)	4 (-)
	F3D4	(X4 Drive)	10 (-)
	F334NS	(X2 Drive)	6 (-)
	L314N1	1-Input Inverter (Low Power)	3 (-)
	F314N1	1-Input Inverter	4 (-)
	F334N1	1-Input Inverter (X2 Drive)	5 (-)

Function	Block	Description	Cells (I/O)
5-Input AND	L315	(Low Power)	4 (-)
	F315	-	5 (-)
	F335	(X2 Drive)	7 (-)
	L315N1	1-Input Inverter (Low Power)	4 (-)
	F315N1	1-Input Inverter	5 (-)
	F335N1	1-Input Inverter (X2 Drive)	7 (-)
6-Input AND	L316	(Low Power)	4 (-)
	F316	-	5 (-)
	F336	(X2 Drive)	7 (-)
	L316N1	1-Input Inverter (Low Power)	5 (-)
	F316N1	1-Input Inverter	6 (-)
	F336N1	1-Input Inverter (X2 Drive)	8 (-)
	L316N2	2-Input Inverter (Low Power)	5 (-)
	F316N2	2-Input Inverter	6 (-)
	F336N2	2-Input Inverter (X2 Drive)	8 (-)
8-Input AND	L318	(Low Power)	5 (-)
	F318	-	6 (-)
	F338	(X2 Drive)	8 (-)
	L318N1	1-Input Inverter (Low Power)	6 (-)
	F318N1	1-Input Inverter	7 (-)
	F338N1	1-Input Inverter (X2 Drive)	9 (-)
	L318N2	2-Input Inverter (Low Power)	6 (-)
	F318N2	2-Input Inverter	7 (-)
	F338N2	2-Input Inverter (X2 Drive)	9 (-)
	L318N3	3-Input Inverter (Low Power)	7 (-)
	F318N3	3-Input Inverter	8 (-)
	F338N3	3-Input Inverter (X2 Drive)	10 (-)

E.2.4 AND-NOR

Function	Block	Description	Cells (I/O)
1-2-Input AND-NOR	L421	(Low Power)	2 (-)
	F421	-	3 (-)
	F421NP	(X2 Drive)	5 (-)
	F421T	(X4 Drive)	12 (-)
	L421NA	(Low Power)	2 (-)
	F421NA	-	4 (-)
	F421NAP	(X2 Drive)	5 (-)
	F421NAT	(X4 Drive)	14 (-)
	L421NB	(Low Power)	3 (-)
	F421NB	-	4 (-)
	F421NBP	(X2 Drive)	6 (-)
	F421NBT	(X4 Drive)	16 (-)
	L421NC	(Low Power)	3 (-)
	F421NC	-	5 (-)
	F421NCP	(X2 Drive)	6 (-)
	F421NCT	(X4 Drive)	9 (-)
	L421ND	(Low Power)	2 (-)
	F421ND	-	4 (-)
	F421NDP	(X2 Drive)	5 (-)
	F421NDT	(X4 Drive)	14 (-)
	L421NE	(Low Power)	3 (-)
	F421NE	-	4 (-)
	F421NEP	(X2 Drive)	6 (-)
	F421NET	(X4 Drive)	16 (-)

Function	Block	Description	Cells (I/O)
1-1-2-Input AND-NOR	F422	-	4 (-)
	F422NP	(X2 Drive)	5 (-)
	F422T	(X4 Drive)	16 (-)
	F422NA	-	5 (-)
	F422NAP	(X2 Drive)	6 (-)
	F422NAT	(X4 Drive)	18 (-)
	F422NB	-	5 (-)
	F422NBP	(X2 Drive)	6 (-)
	F422NBT	(X4 Drive)	16 (-)
	F422NC	-	6 (-)
	F422NCP	(X2 Drive)	7 (-)
	F422NCT	(X4 Drive)	18 (-)
	F422ND	-	6 (-)
	F422NDP	(X2 Drive)	7 (-)
	F422NDT	(X4 Drive)	10 (-)
	F422NE	-	5 (-)
	F422NEP	(X2 Drive)	6 (-)
	F422NET	(X4 Drive)	20 (-)
	F422NF	-	6 (-)
	F422NFP	(X2 Drive)	7 (-)
	F422NFT	(X4 Drive)	22 (-)
	F422NG	-	5 (-)
	F422NGP	(X2 Drive)	6 (-)
	F422NGT	(X4 Drive)	18 (-)
	F422NH	-	5 (-)
	F422NHP	(X2 Drive)	6 (-)
	F422NHT	(X4 Drive)	20 (-)

Function	Block	Description	Cells (I/O)
1-3-Input AND-NOR	L423	(Low Power)	2 (-)
	F423	-	4 (-)
	F423NP	(X2 Drive)	5 (-)
	F423T	(X4 Drive)	16 (-)
	L423NA	(Low Power)	3 (-)
	F423NA	-	5 (-)
	F423NAP	(X2 Drive)	6 (-)
	F423NAT	(X4 Drive)	18 (-)
	L423NB	(Low Power)	3 (-)
	F423NB	-	5 (-)
	F423NBP	(X2 Drive)	6 (-)
	F423NBT	(X4 Drive)	20 (-)
	L423NC	(Low Power)	4 (-)
	F423NC	-	6 (-)
	F423NCP	(X2 Drive)	7 (-)
	F423NCT	(X4 Drive)	22 (-)
	L423ND	(Low Power)	4 (-)
	F423ND	-	6 (-)
	F423NDP	(X2 Drive)	7 (-)
	F423NDT	(X4 Drive)	10 (-)
	L423NE	(Low Power)	3 (-)
	F423NE	-	5 (-)
	F423NEP	(X2 Drive)	6 (-)
	F423NET	(X4 Drive)	18 (-)
	L423NF	(Low Power)	3 (-)
	F423NF	-	5 (-)
	F423NFP	(X2 Drive)	6 (-)
	F423NFT	(X4 Drive)	20 (-)
	L423NG	(Low Power)	4 (-)
	F423NG	-	6 (-)
	F423NGP	(X2 Drive)	7 (-)
	F423NGT	(X4 Drive)	22 (-)

Function	Block	Description	Cells (I/O)
2-2-Input AND-NOR	L424	(Low Power)	2 (-)
	F424	-	4 (-)
	F424NP	(X2 Drive)	5 (-)
	F424T	(X4 Drive)	16 (-)
	L424NA	(Low Power)	3 (-)
	F424NA	-	5 (-)
	F424NAP	(X2 Drive)	6 (-)
	F424NAT	(X4 Drive)	18 (-)
	L424NB	(Low Power)	3 (-)
	F424NB	-	5 (-)
	F424NBP	(X2 Drive)	6 (-)
	F424NBT	(X4 Drive)	20 (-)
	L424NC	(Low Power)	4 (-)
	F424NC	-	6 (-)
	F424NCP	(X2 Drive)	7 (-)
	F424NCT	(X4 Drive)	10 (-)
	L424ND	(Low Power)	3 (-)
	F424ND	-	5 (-)
	F424NDP	(X2 Drive)	6 (-)
	F424NDT	(X4 Drive)	20 (-)
	L424NE	(Low Power)	4 (-)
	F424NE	-	6 (-)
	F424NEP	(X2 Drive)	7 (-)
	F424NET	(X4 Drive)	22 (-)
2-2-2-Input AND-NOR	L425	(Low Power)	5 (-)
	F425	-	6 (-)
	F425NP	(X2 Drive)	6 (-)
	F425T	(X4 Drive)	24 (-)
3-3-Input AND-NOR	L426	(Low Power)	5 (-)
	F426	-	6 (-)
	F426NP	(X2 Drive)	6 (-)
	F426T	(X4 Drive)	24 (-)
2-3-Input AND-NOR	L427	(Low Power)	4 (-)
	F427	-	5 (-)
	F427NP	(X2 Drive)	6 (-)
	F427T	(X4 Drive)	20 (-)
1-2-2-Input AND-NOR	F428	-	5 (-)
	F428NP	(X2 Drive)	6 (-)
	F428T	(X4 Drive)	20 (-)
2-2-2-2-Input AND-NOR	L429	(Low Power)	6 (-)
	F429	-	6 (-)
	F429NP	(X2 Drive)	7 (-)

Function	Block	Description	Cells (I/O)
1-4-Input AND-NOR	L440	(Low Power)	3 (-)
	F440	-	5 (-)
	F440NP	(X2 Drive)	6 (-)
1-5-Input AND-NOR	L441	(Low Power)	5 (-)
	F441	-	7 (-)
	F441NP	(X2 Drive)	8 (-)
4-4-Input AND-NOR	L442	(Low Power)	6 (-)
	F442	-	11 (-)
	F442NP	(X2 Drive)	12 (-)
4-4-4-Input AND-NOR	L444	(Low Power)	8 (-)
	F444	-	8 (-)
	F444NP	(X2 Drive)	9 (-)
2-4-Input AND-NOR	L445	(Low Power)	5 (-)
	F445	-	6 (-)
	F445NP	(X2 Drive)	6 (-)
1-1-1-2-Input AND-NOR	L446	(Low Power)	4 (-)
	F446	-	5 (-)
	F446NP	(X2 Drive)	6 (-)
1-1-1-3-Input AND-NOR	L447	(Low Power)	5 (-)
	F447	-	5 (-)
	F447NP	(X2 Drive)	6 (-)
1-1-2-2-Input AND-NOR	L448	(Low Power)	5 (-)
	F448	-	5 (-)
	F448NP	(X2 Drive)	6 (-)
3-3-3-3-Input AND-NOR	F449	-	8 (-)
	F449NP	(X2 Drive)	9 (-)
3-3-3-Input AND-NOR	L460	(Low Power)	6 (-)
	F460	-	7 (-)
	F460NP	(X2 Drive)	8 (-)
1-2-3-Input AND-NOR	L462	(Low Power)	5 (-)
	F462	-	6 (-)
	F462NP	(X2 Drive)	6 (-)
1-1-3-Input AND-NOR	L463	(Low Power)	4 (-)
	F463	-	5 (-)
	F463NP	(X2 Drive)	6 (-)
1-1-4-Input AND-NOR	L464	(Low Power)	5 (-)
	F464	-	5 (-)
	F464NP	(X2 Drive)	6 (-)
1-1-1-1-2-Input AND-NOR	F465	-	5 (-)
	F465NP	(X2 Drive)	6 (-)
4-4-4-4-Input AND-NOR	F466	-	10 (-)
	F466NP	(X2 Drive)	11 (-)

E.2.5 OR-NAND

Function	Block	Description	Cells (I/O)
1-4-Input OR-NAND	L430	(Low Power)	4 (-)
	F430	-	5 (-)
	F430NP	(X2 Drive)	7 (-)
1-2-Input OR-NAND	L431	(Low Power)	2 (-)
	F431	-	3 (-)
	F431NP	(X2 Drive)	5 (-)
	F431T	(X4 Drive)	12 (-)
	L431NA	(Low Power)	2 (-)
	F431NA	-	4 (-)
	F431NAP	(X2 Drive)	5 (-)
	F431NAT	(X4 Drive)	14 (-)
	L431NB	(Low Power)	3 (-)
	F431NB	-	4 (-)
	F431NBP	(X2 Drive)	6 (-)
	F431NBT	(X4 Drive)	16 (-)
	L431NC	(Low Power)	3 (-)
	F431NC	-	5 (-)
	F431NCP	(X2 Drive)	6 (-)
	F431NCT	(X4 Drive)	14 (-)
	L431ND	(Low Power)	2 (-)
	F431ND	-	4 (-)
	F431NDP	(X2 Drive)	5 (-)
	F431NDT	(X4 Drive)	14 (-)
	L431NE	(Low Power)	3 (-)
	F431NE	-	4 (-)
	F431NEP	(X2 Drive)	6 (-)
	F431NET	(X4 Drive)	12 (-)

Function	Block	Description	Cells (I/O)
1-1-2-Input OR-NAND	L432	(Low Power)	2 (-)
	F432	-	4 (-)
	F432NP	(X2 Drive)	5 (-)
	F432T	(X4 Drive)	16 (-)
	L432NA	(Low Power)	3 (-)
	F432NA	-	5 (-)
	F432NAP	(X2 Drive)	6 (-)
	F432NAT	(X4 Drive)	18 (-)
	L432NB	(Low Power)	3 (-)
	F432NB	-	5 (-)
	F432NBP	(X2 Drive)	6 (-)
	F432NBT	(X4 Drive)	20 (-)
	L432NC	(Low Power)	4 (-)
	F432NC	-	6 (-)
	F432NCP	(X2 Drive)	7 (-)
	F432NCT	(X4 Drive)	22 (-)
	L432ND	(Low Power)	4 (-)
	F432ND	-	6 (-)
	F432NDP	(X2 Drive)	7 (-)
	F432NDT	(X4 Drive)	20 (-)
	L432NE	(Low Power)	3 (-)
	F432NE	-	5 (-)
	F432NEP	(X2 Drive)	6 (-)
	F432NET	(X4 Drive)	20 (-)
	L432NF	(Low Power)	4 (-)
	F432NF	-	6 (-)
	F432NFP	(X2 Drive)	7 (-)
	F432NFT	(X4 Drive)	18 (-)
	L432NG	(Low Power)	3 (-)
	F432NG	-	5 (-)
	F432NGP	(X2 Drive)	6 (-)
	F432NGT	(X4 Drive)	18 (-)
	L432NH	(Low Power)	3 (-)
	F432NH	-	5 (-)
	F432NHP	(X2 Drive)	6 (-)
	F432NHT	(X4 Drive)	16 (-)

Function	Block	Description	Cells (I/O)
1-3-Input OR-NAND	F433	-	4 (-)
	F433NP	(X2 Drive)	5 (-)
	F433T	(X4 Drive)	16 (-)
	F433NA	-	5 (-)
	F433NAP	(X2 Drive)	6 (-)
	F433NAT	(X4 Drive)	18 (-)
	F433NB	-	5 (-)
	F433NBP	(X2 Drive)	6 (-)
	F433NBT	(X4 Drive)	20 (-)
	F433NC	-	6 (-)
	F433NCP	(X2 Drive)	7 (-)
	F433NCT	(X4 Drive)	18 (-)
	F433ND	-	6 (-)
	F433NDP	(X2 Drive)	7 (-)
	F433NDT	(X4 Drive)	16 (-)
	F433NE	-	5 (-)
	F433NEP	(X2 Drive)	6 (-)
	F433NET	(X4 Drive)	18 (-)
	F433NF	-	5 (-)
	F433NFP	(X2 Drive)	6 (-)
	F433NFT	(X4 Drive)	16 (-)
	F433NG	-	6 (-)
	F433NGP	(X2 Drive)	7 (-)
	F433NGT	(X4 Drive)	14 (-)

Function	Block	Description	Cells (I/O)
2-2-Input OR-NAND	L434	(Low Power)	2 (-)
	F434	-	4 (-)
	F434NP	(X2 Drive)	5 (-)
	F434T	(X4 Drive)	16 (-)
	L434NA	(Low Power)	3 (-)
	F434NA	-	5 (-)
	F434NAP	(X2 Drive)	6 (-)
	F434NAT	(X4 Drive)	18 (-)
	L434NB	(Low Power)	3 (-)
	F434NB	-	5 (-)
	F434NBP	(X2 Drive)	6 (-)
	F434NBT	(X4 Drive)	16 (-)
	L434NC	(Low Power)	4 (-)
	F434NC	-	6 (-)
	F434NCP	(X2 Drive)	7 (-)
	F434NCT	(X4 Drive)	16 (-)
	L434ND	(Low Power)	3 (-)
	F434ND	-	5 (-)
	F434NDP	(X2 Drive)	6 (-)
	F434NDT	(X4 Drive)	20 (-)
	L434NE	(Low Power)	4 (-)
	F434NE	-	6 (-)
	F434NEP	(X2 Drive)	7 (-)
	F434NET	(X4 Drive)	18 (-)
2-3-Input OR-NAND	L435	(Low Power)	4 (-)
	F435	-	8 (-)
	F435NP	(X2 Drive)	9 (-)
	F435T	(X4 Drive)	20 (-)
3-3-Input OR-NAND	L436	(Low Power)	5 (-)
	F436	-	9 (-)
	F436NP	(X2 Drive)	10 (-)
	F436T	(X4 Drive)	24 (-)
1-2-2-Input OR-NAND	F437	-	5 (-)
	F437NP	(X2 Drive)	6 (-)
	F437T	(X4 Drive)	20 (-)
2-2-2-Input OR-NAND	L438	(Low Power)	5 (-)
	F438	-	6 (-)
	F438NP	(X2 Drive)	6 (-)
1-5-Input OR-NAND	L439	(Low Power)	5 (-)
	F439	-	6 (-)
	F439NP	(X2 Drive)	8 (-)
2-4-Input OR-NAND	L450	(Low Power)	5 (-)
	F450	-	6 (-)
	F450NP	(X2 Drive)	8 (-)

Function	Block	Description	Cells (I/O)
4-4-Input OR-NAND	L451	(Low Power)	7 (-)
	F451	-	8 (-)
	F451NP	(X2 Drive)	10 (-)
1-1-3-Input OR-NAND	L452	(Low Power)	4 (-)
	F452	-	5 (-)
	F452NP	(X2 Drive)	6 (-)
1-1-4-Input OR-NAND	L453	(Low Power)	5 (-)
	F453	-	6 (-)
	F453NP	(X2 Drive)	9 (-)
2-2-2-2-Input OR-NAND	F454	-	13 (-)
	F454NP	(X2 Drive)	14 (-)
4-4-4-Input OR-NAND	F457	-	10 (-)
	F457NP	(X2 Drive)	11 (-)
1-1-1-2-Input OR-NAND	L458	(Low Power)	4 (-)
	F458	-	5 (-)
	F458NP	(X2 Drive)	5 (-)
1-1-1-3-Input OR-NAND	L459	(Low Power)	5 (-)
	F459	-	5 (-)
	F459NP	(X2 Drive)	6 (-)
1-1-1-1-2-Input OR-NAND	F490	-	5 (-)
	F490NP	(X2 Drive)	6 (-)
1-2-3-Input OR-NAND	L491	(Low Power)	5 (-)
	F491	-	5 (-)
	F491NP	(X2 Drive)	6 (-)
3-3-3-Input OR-NAND	L493	(Low Power)	6 (-)
	F493	-	7 (-)
	F493NP	(X2 Drive)	8 (-)
1-1-2-2-Input OR-NAND	L495	(Low Power)	5 (-)
	F495	-	6 (-)
	F495NP	(X2 Drive)	6 (-)
3-3-3-3-Input OR-NAND	F496	-	8 (-)
	F496NP	(X2 Drive)	9 (-)
4-4-4-4-Input OR-NAND	F498	-	14 (-)
	F498NP	(X2 Drive)	16 (-)

E.2.6 Exclusive OR, Exclusive NOR

Function	Block	Description	Cells (I/O)
2-Input Exclusive OR	L511	(Low Power)	3 (-)
	F511	-	4 (-)
	F511NP	(X2 Drive)	5 (-)
	F511NT	(X4 Drive)	11 (-)
3-Input Exclusive OR	L516	(Low Power)	6 (-)
	F516	-	9 (-)
	F516NP	(X2 Drive)	9 (-)
	F516NT	(X4 Drive)	14 (-)
2-Input Exclusive NOR	L512	(Low Power)	3 (-)
	F512	-	4 (-)
	F512NP	(X2 Drive)	5 (-)
	F512NT	(X4 Drive)	11 (-)
3-Input Exclusive NOR	L517	(Low Power)	6 (-)
	F517	-	8 (-)
	F517NT	(X4 Drive)	14 (-)

E.2.7 Adder, 3-State Buffer, Decoder, Multiplexer, Generator

Function	Block	Description	Cells (I/O)
1-Bit Full Adder	F521	-	9 (-)
	F521NP	(X2 Drive)	19 (-)
	F521NT	(X4 Drive)	26 (-)
4-Bit Full Adder	F523	-	34 (-)
1-Bit Carry Save Adder	F528	-	11 (-)
3-State Buffer	L531	with EN (Low Power)	4 (-)
	F531	with EN	5 (-)
	F533	with EN (X2 Drive)	7 (-)
	F53F	with EN (X4 Drive)	11 (-)
	F53H	with EN (X8 Drive)	24 (-)
	L532	with ENB (Low Power)	4 (-)
	F532	with ENB	5 (-)
	F534	with ENB (X2 Drive)	7 (-)
	F53G	with ENB (X4 Drive)	11 (-)
	F53K	with ENB (X8 Drive)	24 (-)
	F541	Inverter with EN	3 (-)
	F543	Inverter with EN (X2 Drive)	4 (-)
	F54F	Inverter with EN (X4 Drive)	6 (-)
	F54H	Inverter with EN (X8 Drive)	25 (-)
	F542	Inverter with ENB	3 (-)
	F544	Inverter with ENB (X2 Drive)	4 (-)
	F54G	Inverter with ENB (X4 Drive)	6 (-)
	F54K	Inverter with ENB (X8 Drive)	25 (-)

Function	Block	Description	Cells (I/O)
2 to 4 Decoder	L560	Positive Out (Low Power)	6 (-)
	F560	Positive Out	10 (-)
	F560NP	Positive Out (X2 Drive)	18 (-)
	L561	Negative Out (Low Power)	6 (-)
	F561	Negative Out	10 (-)
	F561NP	Negative Out (X2 Drive)	18 (-)
	L981	Negative Out with ENB (Low Power)	8 (-)
	F981	Negative Out with ENB	13 (-)
3 to 8 Decoder	L982	Negative Out with ENB (Low Power)	17 (-)
	F982	Negative Out with ENB	26 (-)
2 to 1 Multiplexer (Positive Out)	F565	-	4 (-)
	F56C	(X2 Drive)	7 (-)
	F565NT	(X4 Drive)	11 (-)
	L571	with ENB (Low Power)	4 (-)
	F571	with ENB	6 (-)
	F571NP	with ENB (X2 Drive)	8 (-)
2 to 1 Multiplexer (Negative Out)	F57B	-	5 (-)
	F57BNP	(X2 Drive)	6 (-)
4 to 1 Multiplexer (Positive Out)	F564	-	8 (-)
	F56B	(X2 Drive)	11 (-)
	F564NT	(X4 Drive)	16 (-)
	F570	with ENB	10 (-)
	F570NP	with ENB (X2 Drive)	12 (-)
	F56BNSP	High-speed (X2 Drive)	15 (-)
	F564NST	High-speed (X4 Drive)	21 (-)
4 to 1 Multiplexer (Negative Out)	F57A	-	10 (-)
	F57ANP	(X2 Drive)	10 (-)
8 to 1 Multiplexer (Positive Out)	F563	-	17 (-)
	F563NP	(X2 Drive)	20 (-)
	F563NT	(X4 Drive)	25 (-)
	F569	with ENB	19 (-)
	F569NP	with ENB (X2 Drive)	21 (-)
	F563NSP	High-speed (X2 Drive)	31 (-)
	F563NST	High-speed (X4 Drive)	41 (-)
8 to 1 Multiplexer (Negative Out)	F579	-	17 (-)
Quad 2 to 1 Multiplexer (Positive Out)	F552	-	13 (-)
Quad 2 to 1 Multiplexer (Negative Out)	F555	-	9 (-)
	L572	with ENB (Low Power)	10 (-)
	F572	with ENB	14 (-)
Quad 4 to 1 Multiplexer (Positive Out)	F551	-	27 (-)
Quad 4 to 1 Multiplexer (Negative Out)	F554	-	29 (-)
Quad 8 to 1 Multiplexer (Positive Out)	F550	-	64 (-)
Quad 8 to 1 Multiplexer (Negative Out)	F553	-	64 (-)

Function	Block	Description	Cells (I/O)
8-Bit Odd Parity Generator	F581	-	19 (-)
	F581NSP	(X2 Drive)	21 (-)
8-Bit Even Parity Generator	F582	-	19 (-)
	F582NSP	(X2 Drive)	21 (-)

E.2.8 RS-F/F, RS-latch

Function	Block	Description	Cells (I/O)
RS-Latch	F595	-	5 (-)
RS-F/F with R,S	F596	-	11 (-)

E.2.9 D-Latch

Function	Block	Description	Cells (I/O)
D-Latch	F601NL	(Low Power)	5 (-)
	F601	-	6 (-)
	F601NP	(X2 Drive)	8 (-)
	L601	Q Out (Low Power)	4 (-)
	F601NQL	Q Out (Low Power)	4 (-)
	F601NQ	Q Out	5 (-)
	F601NQP	Q Out (X2 Drive)	6 (-)
	F601NBL	QB Out (Low Power)	4 (-)
	F601NB	QB Out	5 (-)
	F601NBP	QB Out (X2 Drive)	6 (-)
D-Latch (High Speed)	F6R1	-	6 (-)
D-Latch with R	F602NL	(Low Power)	6 (-)
	F602	-	6 (-)
	F602NP	(X2 Drive)	9 (-)
	L602	Q Out (Low Power)	5 (-)
	F602NQL	Q Out (Low Power)	5 (-)
	F602NQ	Q Out	6 (-)
	F602NQP	Q Out (X2 Drive)	7 (-)
	F602NB	QB Out	6 (-)
	F602NBP	QB Out (X2 Drive)	7 (-)
D-Latch with R (High Speed)	F6R2	-	7 (-)
D-Latch with RB	F603NL	(Low Power)	5 (-)
	F603	-	7 (-)
	F603NP	(X2 Drive)	8 (-)
	L603	Q Out (Low Power)	4 (-)
	F603NQ	Q Out	5 (-)
	F603NQP	Q Out (X2 Drive)	6 (-)
	F603NBL	QB Out (Low Power)	5 (-)
	F603NB	QB Out	6 (-)
	F603NBP	QB Out (X2 Drive)	7 (-)

Function	Block	Description	Cells (I/O)
D-Latch with RB (High Speed)	F6R5	-	6 (-)
D-Latch with SB	F60KNL	(Low Power)	6 (-)
	F60K	-	7 (-)
	F60KNP	(X2 Drive)	9 (-)
	F60KNQL	Q Out (Low Power)	5 (-)
	F60KNQ	Q Out	6 (-)
	F60KNQP	Q Out (X2 Drive)	7 (-)
	F60KNB	QB Out	5 (-)
	F60KNBP	QB Out (X2 Drive)	6 (-)
D-Latch with RB,SB	F60JNL	(Low Power)	6 (-)
	F60J	-	7 (-)
	F60JNP	(X2 Drive)	9 (-)
	F60JNQ	Q Out	6 (-)
	F60JNQP	Q Out (X2 Drive)	7 (-)
	F60JNBL	QB Out (Low Power)	5 (-)
	F60JNB	QB Out	6 (-)
	F60JNBP	QB Out (X2 Drive)	7 (-)
D-Latch (GB)	F604NL	(Low Power)	5 (-)
	F604	-	6 (-)
	F604NP	(X2 Drive)	8 (-)
	L604	Q Out (Low Power)	4 (-)
	F604NQL	Q Out (Low Power)	4 (-)
	F604NQ	Q Out	5 (-)
	F604NQP	Q Out (X2 Drive)	6 (-)
	F604NBL	QB Out (Low Power)	4 (-)
	F604NB	QB Out	5 (-)
	F604NBP	QB Out (X2 Drive)	6 (-)
D-Latch (GB) (High Speed)	F6R8	-	6 (-)
D-Latch (GB) with RB	F605NL	(Low Power)	5 (-)
	F605	-	7 (-)
	F605NP	(X2 Drive)	8 (-)
	L605	Q Out (Low Power)	4 (-)
	F605NQ	Q Out	5 (-)
	F605NQP	Q Out (X2 Drive)	6 (-)
	F605NBL	QB Out (Low Power)	5 (-)
	F605NB	QB Out	6 (-)
	F605NBP	QB Out (X2 Drive)	7 (-)
D-Latch (GB) with RB (High Speed)	F6R9	-	6 (-)

E.2.10 D-F/F

Function	Block	Description	Cells (I/O)
D-F/F	F611	-	8 (-)
	F611NT	(X4 Drive)	14 (-)
	L611	Q Out (Low Power)	6 (-)
	F611NQT	Q Out (X4 Drive)	10 (-)
	F611NBT	QB Out (X4 Drive)	10 (-)
	F641NL	(Low Power)	7 (-)
	F641	-	8 (-)
	F641NP	(X2 Drive)	10 (-)
	F641NQL	Q Out (Low Power)	7 (-)
	F641NQ	Q Out	7 (-)
	F641NQP	Q Out (X2 Drive)	8 (-)
	F641NBL	QB Out (Low Power)	7 (-)
	F641NB	QB Out	7 (-)
	F641NBP	QB Out (X2 Drive)	8 (-)
D-F/F with R	F612NQT	Q Out (X4 Drive)	11 (-)
	F612NBT	QB Out (X4 Drive)	12 (-)
	F642NL	(Low Power)	8 (-)
	F642	-	9 (-)
	F642NP	(X2 Drive)	11 (-)
	F642NQL	Q Out (Low Power)	8 (-)
	F642NQ	Q Out	8 (-)
	F642NQP	Q Out (X2 Drive)	9 (-)
	F642NBL	QB Out (Low Power)	8 (-)
	F642NB	QB Out	8 (-)
	F642NBP	QB Out (X2 Drive)	9 (-)
D-F/F with S	F613NQT	Q Out (X4 Drive)	12 (-)
	F613NBT	QB Out (X4 Drive)	11 (-)
	F643NL	(Low Power)	8 (-)
	F643	-	9 (-)
	F643NP	(X2 Drive)	11 (-)
	F643NQL	Q Out (Low Power)	7 (-)
	F643NQ	Q Out	8 (-)
	F643NQP	Q Out (X2 Drive)	9 (-)
	F643NBL	QB Out (Low Power)	7 (-)
	F643NB	QB Out	8 (-)
	F643NBP	QB Out (X2 Drive)	9 (-)

Function	Block	Description	Cells (I/O)
D-F/F with R,S	F614	-	10 (-)
	L614	Q Out (Low Power)	8 (-)
	F614NQT	Q Out (X4 Drive)	13 (-)
	F614NBT	QB Out (X4 Drive)	13 (-)
	F644NL	(Low Power)	9 (-)
	F644	-	10 (-)
	F644NP	(X2 Drive)	12 (-)
	F644NQL	Q Out (Low Power)	9 (-)
	F644NQ	Q Out	9 (-)
	F644NQP	Q Out (X2 Drive)	10 (-)
	F644NBL	QB Out (Low Power)	9 (-)
	F644NB	QB Out	9 (-)
	F644NBP	QB Out (X2 Drive)	10 (-)
D-F/F with RB	F615NL	(Low Power)	8 (-)
	F615	-	9 (-)
	F615NP	(X2 Drive)	11 (-)
	F615NT	(X4 Drive)	16 (-)
	F615NQL	Q Out (Low Power)	8 (-)
	F615NQ	Q Out	8 (-)
	F615NQP	Q Out (X2 Drive)	9 (-)
	F615NQT	Q Out (X4 Drive)	12 (-)
	F615NBL	QB Out (Low Power)	8 (-)
	F615NB	QB Out	8 (-)
	F615NBP	QB Out (X2 Drive)	9 (-)
	F615NBT	QB Out (X4 Drive)	11 (-)
D-F/F with SB	F616NL	(Low Power)	8 (-)
	F616	-	9 (-)
	F616NP	(X2 Drive)	11 (-)
	F616NQL	Q Out (Low Power)	8 (-)
	F616NQ	Q Out	8 (-)
	F616NQP	Q Out (X2 Drive)	9 (-)
	F616NQT	Q Out (X4 Drive)	11 (-)
	F616NBL	QB Out (Low Power)	8 (-)
	F616NB	QB Out	8 (-)
	F616NBP	QB Out (X2 Drive)	9 (-)
	F616NBT	QB Out (X4 Drive)	12 (-)

Function	Block	Description	Cells (I/O)
D-F/F with RB,SB	F617	-	10 (-)
	L617	Q Out (Low Power)	8 (-)
	F617NQT	Q Out (X4 Drive)	13 (-)
	F617NBT	QB Out (X4 Drive)	13 (-)
	F647NL	(Low Power)	9 (-)
	F647	-	10 (-)
	F647NP	(X2 Drive)	12 (-)
	F647NQL	Q Out (Low Power)	9 (-)
	F647NQ	Q Out	9 (-)
	F647NQP	Q Out (X2 Drive)	10 (-)
	F647NBL	QB Out (Low Power)	9 (-)
	F647NB	QB Out	9 (-)
	F647NBP	QB Out (X2 Drive)	10 (-)
D-F/F (CB)	F631	-	8 (-)
	F631NT	(X4 Drive)	14 (-)
	L631	Q Out (Low Power)	6 (-)
	F631NQT	Q Out (X4 Drive)	10 (-)
	F631NBT	QB Out (X4 Drive)	10 (-)
	F661NL	(Low Power)	7 (-)
	F661	-	8 (-)
	F661NP	(X2 Drive)	10 (-)
	F661NQL	Q Out (Low Power)	7 (-)
	F661NQ	Q Out	7 (-)
	F661NQP	Q Out (X2 Drive)	8 (-)
	F661NBL	QB Out (Low Power)	7 (-)
	F661NB	QB Out	7 (-)
	F661NBP	QB Out (X2 Drive)	8 (-)
D-F/F (CB) with RB	F635NQT	Q Out (X4 Drive)	12 (-)
	F635NBT	QB Out (X4 Drive)	11 (-)
	F665NL	(Low Power)	8 (-)
	F665	-	9 (-)
	F665NP	(X2 Drive)	11 (-)
	F665NQL	Q Out (Low Power)	7 (-)
	F665NQ	Q Out	8 (-)
	F665NQP	Q Out (X2 Drive)	9 (-)
	F665NBL	QB Out (Low Power)	7 (-)
	F665NB	QB Out	8 (-)
	F665NBP	QB Out (X2 Drive)	9 (-)

Function	Block	Description	Cells (I/O)
D-F/F (CB) with SB	F636NQT	Q Out (X4 Drive)	11 (-)
	F636NBT	QB Out (X4 Drive)	12 (-)
	F666NL	(Low Power)	8 (-)
	F666	-	9 (-)
	F666NP	(X2 Drive)	11 (-)
	F666NQL	Q Out (Low Power)	7 (-)
	F666NQ	Q Out	8 (-)
	F666NQP	Q Out (X2 Drive)	9 (-)
	F666NBL	QB Out (Low Power)	7 (-)
	F666NB	QB Out	8 (-)
	F666NBP	QB Out (X2 Drive)	9 (-)
D-F/F (CB) with RB,SB	F637	-	10 (-)
	L637	Q Out (Low Power)	8 (-)
	F637NQT	Q Out (X4 Drive)	13 (-)
	F637NBT	QB Out (X4 Drive)	13 (-)
	F667NL	(Low Power)	9 (-)
	F667	-	10 (-)
	F667NP	(X2 Drive)	12 (-)
	F667NQL	Q Out (Low Power)	9 (-)
	F667NQ	Q Out	9 (-)
	F667NQP	Q Out (X2 Drive)	10 (-)
	F667NBL	QB Out (Low Power)	9 (-)
	F667NB	QB Out	9 (-)
	F667NBP	QB Out (X2 Drive)	10 (-)
D-F/F with 2 to 1 Selector	F611ST	(X4 Drive)	17 (-)
	F611SQT	Q Out (X4 Drive)	13 (-)
	F611SBT	QB Out (X4 Drive)	13 (-)
	F641SL	(Low Power)	9 (-)
	F641S	-	10 (-)
	F641SP	(X2 Drive)	12 (-)
	F641SQ	Q Out	9 (-)
	F641SQP	Q Out (X2 Drive)	10 (-)
	F641SB	QB Out	9 (-)
	F641SBP	QB Out (X2 Drive)	10 (-)
D-F/F with R,2 to 1 Selector	F612SQT	Q Out (X4 Drive)	14 (-)
	F612SBT	QB Out (X4 Drive)	14 (-)
	F642SL	(Low Power)	10 (-)
	F642S	-	11 (-)
	F642SP	(X2 Drive)	13 (-)
	F642SQ	Q Out	10 (-)
	F642SQP	Q Out (X2 Drive)	11 (-)
	F642SB	QB Out	10 (-)
	F642SBP	QB Out (X2 Drive)	11 (-)

Function	Block	Description	Cells (I/O)
D-F/F with S,2 to 1 Selector	F613SQT	Q Out (X4 Drive)	14 (-)
	F613SBT	QB Out (X4 Drive)	14 (-)
	F643SL	(Low Power)	10 (-)
	F643S	-	11 (-)
	F643SP	(X2 Drive)	13 (-)
	F643SQ	Q Out	10 (-)
	F643SQP	Q Out (X2 Drive)	11 (-)
	F643SB	QB Out	10 (-)
	F643SBP	QB Out (X2 Drive)	11 (-)
D-F/F with R,S,2 to 1 Selector	F614SQT	Q Out (X4 Drive)	15 (-)
	F614SBT	QB Out (X4 Drive)	15 (-)
	F644SL	(Low Power)	11 (-)
	F644S	-	12 (-)
	F644SP	(X2 Drive)	14 (-)
	F644SQ	Q Out	11 (-)
	F644SQP	Q Out (X2 Drive)	12 (-)
	F644SB	QB Out	11 (-)
	F644SBP	QB Out (X2 Drive)	12 (-)
D-F/F with RB,2 to 1 Selector	F615SL	(Low Power)	10 (-)
	F615S	-	11 (-)
	F615SP	(X2 Drive)	13 (-)
	F615ST	(X4 Drive)	18 (-)
	F615SQ	Q Out	10 (-)
	F615SQP	Q Out (X2 Drive)	11 (-)
	F615SQT	Q Out (X4 Drive)	14 (-)
	F615SB	QB Out	10 (-)
	F615SBP	QB Out (X2 Drive)	11 (-)
	F615SBT	QB Out (X4 Drive)	14 (-)
D-F/F with SB,2 to 1 Selector	F616SL	(Low Power)	10 (-)
	F616S	-	11 (-)
	F616SP	(X2 Drive)	13 (-)
	F616SQ	Q Out	10 (-)
	F616SQP	Q Out (X2 Drive)	11 (-)
	F616SQT	Q Out (X4 Drive)	14 (-)
	F616SB	QB Out	10 (-)
	F616SBP	QB Out (X2 Drive)	11 (-)
	F616SBT	QB Out (X4 Drive)	14 (-)

Function	Block	Description	Cells (I/O)
D-F/F with RB,SB,2 to 1 Selector	F617SQT	Q Out (X4 Drive)	15 (-)
	F617SBT	QB Out (X4 Drive)	15 (-)
	F647SL	(Low Power)	11 (-)
	F647S	-	12 (-)
	F647SP	(X2 Drive)	14 (-)
	F647SQ	Q Out	11 (-)
	F647SQP	Q Out (X2 Drive)	12 (-)
	F647SB	QB Out	11 (-)
	F647SBP	QB Out (X2 Drive)	12 (-)
D-F/F (CB) with 2 to 1 Selector	F631ST	(X4 Drive)	17 (-)
	F631SQT	Q Out (X4 Drive)	13 (-)
	F631SBT	QB Out (X4 Drive)	13 (-)
	F661SL	(Low Power)	9 (-)
	F661S	-	10 (-)
	F661SP	(X2 Drive)	12 (-)
	F661SQ	Q Out	9 (-)
	F661SQP	Q Out (X2 Drive)	10 (-)
	F661SB	QB Out	9 (-)
	F661SBP	QB Out (X2 Drive)	10 (-)
D-F/F (CB) with RB,2 to 1 Selector	F635ST	(X4 Drive)	18 (-)
	F635SQT	Q Out (X4 Drive)	14 (-)
	F635SBT	QB Out (X4 Drive)	14 (-)
	F665SL	(Low Power)	10 (-)
	F665S	-	11 (-)
	F665SP	(X2 Drive)	13 (-)
	F665SQ	Q Out	10 (-)
	F665SQP	Q Out (X2 Drive)	11 (-)
	F665SB	QB Out	10 (-)
	F665SBP	QB Out (X2 Drive)	11 (-)
D-F/F (CB) with SB,2 to 1 Selector	F636ST	(X4 Drive)	18 (-)
	F636SBT	QB Out (X4 Drive)	14 (-)
	F666SL	(Low Power)	10 (-)
	F666S	-	11 (-)
	F666SP	(X2 Drive)	13 (-)
	F666SQ	Q Out	10 (-)
	F666SQP	Q Out (X2 Drive)	11 (-)
	F666SB	QB Out	10 (-)
	F666SBP	QB Out (X2 Drive)	11 (-)

Function	Block	Description	Cells (I/O)
D-F/F (CB) with RB,SB,2 to 1 Selector	F637SQT	Q Out (X4 Drive)	15 (-)
	F637SBT	QB Out (X4 Drive)	15 (-)
	F667SL	(Low Power)	11 (-)
	F667S	-	12 (-)
	F667SP	(X2 Drive)	14 (-)
	F667SQ	Q Out	11 (-)
	F667SQP	Q Out (X2 Drive)	12 (-)
	F667SB	QB Out	11 (-)
	F667SBP	QB Out (X2 Drive)	12 (-)
D-F/F with Hold	F641HL	(Low Power)	9 (-)
	F641H	-	10 (-)
	F641HP	(X2 Drive)	12 (-)
	F641HQ	Q Out	9 (-)
	F641HQP	Q Out (X2 Drive)	10 (-)
	F641HB	QB Out	9 (-)
	F641HBP	QB Out (X2 Drive)	10 (-)
D-F/F with RB,Hold	F615HL	(Low Power)	10 (-)
	F615H	-	11 (-)
	F615HP	(X2 Drive)	13 (-)
	F615HQ	Q Out	10 (-)
	F615HQP	Q Out (X2 Drive)	11 (-)
	F615HB	QB Out	10 (-)
	F615HBP	QB Out (X2 Drive)	11 (-)
D-F/F with SB,Hold	F616HL	(Low Power)	10 (-)
	F616H	-	11 (-)
	F616HP	(X2 Drive)	13 (-)
	F616HQ	Q Out	10 (-)
	F616HQP	Q Out (X2 Drive)	11 (-)
	F616HB	QB Out	10 (-)
	F616HBP	QB Out (X2 Drive)	11 (-)
D-F/F with RB,SB,Hold	F647HL	(Low Power)	11 (-)
	F647H	-	12 (-)
	F647HP	(X2 Drive)	14 (-)
	F647HQ	Q Out	11 (-)
	F647HQP	Q Out (X2 Drive)	12 (-)
	F647HB	QB Out	11 (-)
	F647HBP	QB Out (X2 Drive)	12 (-)
D-F/F (CB) with 2 to 1 Selector (2 CTRL),RB	F673	-	11 (-)
D-F/F (CB) with Hold,2 to 1 Selector (2 CTRL),RB	F674	-	12 (-)

E.2.11 T-F/F, JK-F/F

Function	Block	Description	Cells (I/O)
T-F/F with R,S	F744NL	(Low Power)	8 (-)
	F744	-	9 (-)
	F714	-	9 (-)
	F744NP	(X2 Drive)	11 (-)
	L714	Q Out (Low Power)	8 (-)
	F744NQ	Q Out	8 (-)
	F744NQP	Q Out (X2 Drive)	9 (-)
T-F/F with RB	F745NL	(Low Power)	7 (-)
	F745	-	8 (-)
	F745NP	(X2 Drive)	10 (-)
	F745NQ	Q Out	7 (-)
	F745NQP	Q Out (X2 Drive)	8 (-)
T-F/F with RB,SB	F747NL	(Low Power)	8 (-)
	F747	-	9 (-)
	F717	-	9 (-)
	F747NP	(X2 Drive)	11 (-)
	L717	Q Out (Low Power)	8 (-)
	F747NQ	Q Out	8 (-)
	F747NQP	Q Out (X2 Drive)	9 (-)
T-F/F with Data-Hold R,S	F791	-	12 (-)
T-F/F (TB) with RB	F765NL	(Low Power)	7 (-)
	F765	-	8 (-)
	F765NP	(X2 Drive)	10 (-)
	F765NQ	Q Out	7 (-)
	F765NQP	Q Out (X2 Drive)	8 (-)
T-F/F (TB) with RB,SB	F767NL	(Low Power)	8 (-)
	F767	-	9 (-)
	F737	-	9 (-)
	F767NP	(X2 Drive)	11 (-)
	L737	Q Out (Low Power)	8 (-)
	F767NQ	Q Out	8 (-)
	F767NQP	Q Out (X2 Drive)	9 (-)
JK-F/F	F771NL	(Low Power)	9 (-)
	F771	-	10 (-)
	F771NP	(X2 Drive)	12 (-)
	F771NQL	Q Out (Low Power)	9 (-)
	F771NQ	Q Out	9 (-)
	F771NQP	Q Out (X2 Drive)	10 (-)
	F771NBL	QB Out (Low Power)	9 (-)
	F771NB	QB Out	9 (-)
	F771NBP	QB Out (X2 Drive)	10 (-)

Function	Block	Description	Cells (I/O)
JK-F/F (High Speed)	F7D1	-	10 (-)
JK-F/F with R,S	F774NL	(Low Power)	11 (-)
	F774	-	12 (-)
	F774NP	(X2 Drive)	14 (-)
	F774NQL	Q Out (Low Power)	11 (-)
	F774NQ	Q Out	11 (-)
	F774NQP	Q Out (X2 Drive)	12 (-)
	F774NBL	QB Out (Low Power)	11 (-)
	F774NB	QB Out	11 (-)
	F774NBP	QB Out (X2 Drive)	12 (-)
JK-F/F with RB	F775NL	(Low Power)	10 (-)
	F775	-	11 (-)
	F775NP	(X2 Drive)	13 (-)
	F775NQL	Q Out (Low Power)	10 (-)
	F775NQ	Q Out	10 (-)
	F775NQP	Q Out (X2 Drive)	11 (-)
	F775NBL	QB Out (Low Power)	10 (-)
	F775NB	QB Out	10 (-)
	F775NBP	QB Out (X2 Drive)	11 (-)
JK-F/F with SB	F776NL	(Low Power)	11 (-)
	F776	-	12 (-)
	F776NP	(X2 Drive)	14 (-)
	F776NQL	Q Out (Low Power)	11 (-)
	F776NQ	Q Out	11 (-)
	F776NQP	Q Out (X2 Drive)	12 (-)
	F776NBL	QB Out (Low Power)	11 (-)
	F776NB	QB Out	11 (-)
	F776NBP	QB Out (X2 Drive)	12 (-)
JK-F/F with RB,SB	F777NL	(Low Power)	11 (-)
	F777	-	12 (-)
	F777NP	(X2 Drive)	14 (-)
	F777NQL	Q Out (Low Power)	11 (-)
	F777NQ	Q Out	11 (-)
	F777NQP	Q Out (X2 Drive)	12 (-)
	F777NBL	QB Out (Low Power)	11 (-)
	F777NB	QB Out	11 (-)
	F777NBP	QB Out (X2 Drive)	12 (-)

Function	Block	Description	Cells (I/O)
JK-F/F (CB)	F781NL	(Low Power)	9 (-)
	F781	-	10 (-)
	F781NP	(X2 Drive)	12 (-)
	F781NQL	Q Out (Low Power)	9 (-)
	F781NQ	Q Out	9 (-)
	F781NQP	Q Out (X2 Drive)	10 (-)
	F781NBL	QB Out (Low Power)	9 (-)
	F781NB	QB Out	9 (-)
	F781NBP	QB Out (X2 Drive)	10 (-)
JK-F/F (CB) (High Speed)	F7E1	-	10 (-)
JK-F/F (CB) with RB,SB	F787NL	(Low Power)	11 (-)
	F787	-	12 (-)
	F787NP	(X2 Drive)	14 (-)
	F787NQL	Q Out (Low Power)	11 (-)
	F787NQ	Q Out	11 (-)
	F787NQP	Q Out (X2 Drive)	12 (-)
	F787NBL	QB Out (Low Power)	11 (-)
	F787NB	QB Out	11 (-)
	F787NBP	QB Out (X2 Drive)	12 (-)

E.2.12 Other Block

Function	Block	Description	Cells (I/O)
4-Bit D-Latch	F901	-	20 (-)
	L901	Q Out (Low Power)	12 (-)
4-Bit D-Latch (High Speed)	F971	-	20 (-)
8-Bit D-Latch	F902	-	38 (-)
	L902	Q Out (Low Power)	22 (-)
8-Bit D-Latch (High Speed)	F972	-	38 (-)
4-Bit D-F/F	L924	Q Out (Low Power)	20 (-)
4-Bit Shift Register	L914	Q Out (Low Power)	20 (-)
4-Bit Magnitude Comparator	F985	-	32 (-)

E.3 Scan Path Block

E.3.1 Standard Type

Function	Block	Description	Cells (I/O)
D-F/F with R,S,2 to 1 Selector	S000	-	12 (-)
D-F/F with 2 to 1 Selector	S001	(Low Power)	9 (-)
	S002	-	10 (-)
D-F/F with RB,2 to 1 Selector	S004	-	11 (-)
D-F/F with SB,2 to 1 Selector	S005	-	11 (-)
D-F/F with R,S,Hold,2 to 1 Selector	S050	-	14 (-)
D-F/F with Hold,2 to 1 Selector	S052	-	12 (-)
JK-F/F with R,S,D-F/F Function	S100	-	14 (-)
JK-F/F with D-F/F Function	S102	-	12 (-)
JK-F/F with R,S,Hold,D-F/F Function	S150	-	17 (-)
JK-F/F with Hold,D-F/F Function	S152	-	15 (-)
D-Latch with R,D-F/F Function	S201	-	12 (-)
D-Latch with D-F/F Function	S202	-	11 (-)
D-Latch with D-F/F Function (High Speed)	S204	-	11 (-)
D-Latch with R,Special Function,R	S301	-	8 (-)
D-Latch with Special Function	S302	-	7 (-)
D-Latch with Special Function (High Speed)	S303	-	7 (-)
2 to 1 Data Selector	S999	-	4 (-)

E.3.2 LSSD Scan

Function	Block	Description	Cells (I/O)
Clocked LSSD D-Latch	SD601	-	10 (-)
	SD601NP	(X2 Drive)	13 (-)
Clocked LSSD D-Latch with R	SD602	-	11 (-)
	SD602NP	(X2 Drive)	14 (-)
Clocked LSSD D-Latch with RB	SD603	-	11 (-)
	SD603NP	(X2 Drive)	14 (-)
Clocked LSSD D-Latch (GB)	SD604	-	10 (-)
	SD604NP	(X2 Drive)	13 (-)
Clocked LSSD D-Latch (GB) with RB	SD605	-	11 (-)
	SD605NP	(X2 Drive)	14 (-)
Clocked LSSD D-F/F	SD611	-	12 (-)
	SD641	(X2 Drive)	15 (-)
	SD611T	(X4 Drive)	19 (-)
Clocked LSSD D-F/F with R,S	SD614	-	14 (-)
	SD644	(X2 Drive)	17 (-)
Clocked LSSD D-F/F with RB	SD615	-	13 (-)
	SD645	(X2 Drive)	16 (-)

Function	Block	Description	Cells (I/O)
Clocked LSSD D-F/F with SB	SD616	-	13 (-)
	SD646	(X2 Drive)	16 (-)
Clocked LSSD D-F/F with RB,SB	SD617	-	14 (-)
	SD647	(X2 Drive)	17 (-)
Clocked LSSD D-F/F (CB)	SD631	-	12 (-)
	SD661	(X2 Drive)	15 (-)
Clocked LSSD D-F/F (CB) with RB,SB	SD637	-	14 (-)
	SD667	(X2 Drive)	17 (-)

E.3.3 NEC Scan

Function	Block	Description	Cells (I/O)
D-Latch	SE601	-	12 (-)
	SE601NP	(X2 Drive)	15 (-)
	SE601NQ	Q Out	11 (-)
	SE601NQP	Q Out (X2 Drive)	13 (-)
	SE601NB	QB Out	11 (-)
	SE601NBP	QB Out (X2 Drive)	13 (-)
D-Latch with R	SE602	-	13 (-)
	SE602NP	(X2 Drive)	16 (-)
	SE602NQ	Q Out	12 (-)
	SE602NQP	Q Out (X2 Drive)	14 (-)
	SE602NB	QB Out	12 (-)
	SE602NBP	QB Out (X2 Drive)	14 (-)
D-Latch with RB	SE603	-	13 (-)
	SE603NP	(X2 Drive)	16 (-)
	SE603NQ	Q Out	12 (-)
	SE603NQP	Q Out (X2 Drive)	14 (-)
	SE603NB	QB Out	12 (-)
	SE603NBP	QB Out (X2 Drive)	14 (-)
D-Latch (GB)	SE604	-	12 (-)
	SE604NP	(X2 Drive)	15 (-)
	SE604NQ	Q Out	11 (-)
	SE604NQP	Q Out (X2 Drive)	13 (-)
	SE604NB	QB Out	11 (-)
	SE604NBP	QB Out (X2 Drive)	13 (-)
D-Latch (GB) with RB	SE605	-	13 (-)
	SE605NP	(X2 Drive)	16 (-)
	SE605NQ	Q Out	12 (-)
	SE605NQP	Q Out (X2 Drive)	14 (-)
	SE605NB	QB Out	12 (-)
	SE605NBP	QB Out (X2 Drive)	14 (-)

Function	Block	Description	Cells (I/O)
D-F/F	SE611	-	11 (-)
	SE611NT	(X4 Drive)	18 (-)
	SE611NQT	Q Out (X4 Drive)	14 (-)
	SE611NBT	QB Out (X4 Drive)	14 (-)
	SE641	-	11 (-)
	SE641NP	(X2 Drive)	14 (-)
	SE641NQ	Q Out	10 (-)
	SE641NQP	Q Out (X2 Drive)	12 (-)
	SE641NB	QB Out	10 (-)
	SE641NBP	QB Out (X2 Drive)	12 (-)
D-F/F with R,S	SE614	-	13 (-)
	SE614NQT	Q Out (X4 Drive)	16 (-)
	SE614NBT	QB Out (X4 Drive)	16 (-)
	SE644	-	13 (-)
	SE644NP	(X2 Drive)	16 (-)
	SE644NQ	Q Out	12 (-)
	SE644NQP	Q Out (X2 Drive)	14 (-)
	SE644NB	QB Out	12 (-)
	SE644NBP	QB Out (X2 Drive)	14 (-)
D-F/F with RB	SE615	-	12 (-)
	SE615NQ	Q Out	11 (-)
	SE615NQT	Q Out (X4 Drive)	15 (-)
	SE615NB	QB Out	11 (-)
	SE615NBT	QB Out (X4 Drive)	15 (-)
	SE645NP	(X2 Drive)	15 (-)
	SE645NQP	Q Out (X2 Drive)	13 (-)
	SE645NBP	QB Out (X2 Drive)	13 (-)
D-F/F with SB	SE616	-	12 (-)
	SE616NQ	Q Out	11 (-)
	SE616NQT	Q Out (X4 Drive)	15 (-)
	SE616NB	QB Out	11 (-)
	SE616NBT	QB Out (X4 Drive)	15 (-)
	SE646NP	(X2 Drive)	15 (-)
	SE646NQP	Q Out (X2 Drive)	13 (-)
	SE646NBP	QB Out (X2 Drive)	13 (-)
D-F/F with RB,SB	SE617	-	13 (-)
	SE617NQT	Q Out (X4 Drive)	16 (-)
	SE617NBT	QB Out (X4 Drive)	16 (-)
	SE647	-	13 (-)
	SE647NP	(X2 Drive)	16 (-)
	SE647NQ	Q Out	12 (-)
	SE647NQP	Q Out (X2 Drive)	14 (-)
	SE647NB	QB Out	12 (-)
	SE647NBP	QB Out (X2 Drive)	14 (-)

Function	Block	Description	Cells (I/O)
D-F/F (CB)	SE631	-	11 (-)
	SE631NT	(X4 Drive)	18 (-)
	SE631NQT	Q Out (X4 Drive)	14 (-)
	SE631NBT	QB Out (X4 Drive)	14 (-)
	SE661	-	11 (-)
	SE661NP	(X2 Drive)	14 (-)
	SE661NQ	Q Out	10 (-)
	SE661NQP	Q Out (X2 Drive)	12 (-)
	SE661NB	QB Out	10 (-)
	SE661NBP	QB Out (X2 Drive)	12 (-)
D-F/F (CB) with RB,SB	SE637	-	13 (-)
	SE637NQT	Q Out (X4 Drive)	16 (-)
	SE637NBT	QB Out (X4 Drive)	16 (-)
	SE667	-	13 (-)
	SE667NP	(X2 Drive)	16 (-)
	SE667NQ	Q Out	12 (-)
	SE667NQP	Q Out (X2 Drive)	14 (-)
	SE667NB	QB Out	12 (-)
	SE667NBP	QB Out (X2 Drive)	14 (-)

E.3.4 Scan Controller

Function	Block	Description	Cells (I/O)
Clock Distributor	SCD1	-	8 (-)
Clock Distributor with Test (Positive Clock)	SCDC	-	2 (-)
Clock Distributor with Test (Negative Clock)	SCDD	-	2 (-)
I/F Control (AMC) with EN	SFEH	-	3 (-)
I/F Control (AMC) with ENB	SFEL	-	2 (-)
I/F Control (SMC) with EN	SOEH	-	4 (-)
	SOEH2	(X2 Drive)	7 (-)
I/F Control (SMC) with ENB	SOEL	-	3 (-)
	SOEL2	(X2 Drive)	6 (-)
Mega Macro Skip	SMS1	-	4 (-)
Set/Reset Control	SRH1	-	2 (-)
Set-B/Reset-B Control	SRL1	-	2 (-)
Loop Cut	SRPD	-	12 (-)
Clock Generator	SCKG	-	16 (-)
Common Input	SCI1	-	2 (-)
Common Output	SCO1	-	5 (-)
GND	SGND	-	2 (-)

E.4 Boundary Scan Block (Interface)

E.4.1 3.3 V Interface

Function	Block	Description	Cells (I/O)
Input Buffer	FI01BI	-	7 (1)
	FID1BI	50 kΩ Pull-down	7 (1)
	FIU1BI	50 kΩ Pull-up	7 (1)
	FIW1BI	5 kΩ Pull-up	7 (1)
	FIS1BI	Schmitt	11 (1)
	FDS1BI	Schmitt 50 kΩ Pull-down	11 (1)
	FUS1BI	Schmitt 50 kΩ Pull-up	11 (1)
	FWS1BI	Schmitt 5 kΩ Pull-up	11 (1)
	FIB1BI	Clock Driver	56 (1)
	FDB1BI	Clock Driver 50 kΩ Pull-down	56 (1)
	FUB1BI	Clock Driver 50 kΩ Pull-up	56 (1)
	FWB1BI	Clock Driver 5 kΩ Pull-up	56 (1)
Input Buffer with Failsafe	FIA1BI	-	7 (1)
	FDA1BI	50 kΩ Pull-down	7 (1)
	FIE1BI	Schmitt	11 (1)
	FDE1BI	Schmitt 50 kΩ Pull-down	11 (1)
	FIH1BI	Clock Driver	56 (1)
	FDH1BI	Clock Driver 50 kΩ Pull-down	56 (1)
Output Buffer	FO09B2	3 mA	13 (1)
	FO04B2	6 mA	13 (1)
	FO01B2	9 mA	13 (1)
	FO02B2	12 mA	13 (1)
	FO03B2	18 mA	25 (1)
	FO06B2	24 mA	25 (1)
Low-noise Output Buffer	FE04B2	6 mA	15 (1)
	FE01B2	9 mA	15 (1)
	FE02B2	12 mA	15 (1)
	FE03B2	18 mA	15 (1)
	FE06B2	24 mA	15 (1)

Function	Block	Description	Cells (I/O)
3-State Buffer	B00TB3	3 mA	29 (1)
	B0DTB3	3 mA 50 kΩ Pull-down	29 (1)
	B0UTB3	3 mA 50 kΩ Pull-up	29 (1)
	B0WTB3	3 mA 5 kΩ Pull-up	29 (1)
	B00EB3	6 mA	29 (1)
	B0DEB3	6 mA 50 kΩ Pull-down	29 (1)
	B0UEB3	6 mA 50 kΩ Pull-up	29 (1)
	B0WEB3	6 mA 5 kΩ Pull-up	29 (1)
	B008B3	9 mA	29 (1)
	B0D8B3	9 mA 50 kΩ Pull-down	29 (1)
	B0U8B3	9 mA 50 kΩ Pull-up	29 (1)
	B0W8B3	9 mA 5 kΩ Pull-up	29 (1)
	B007B3	12 mA	29 (1)
	B0D7B3	12 mA 50 kΩ Pull-down	29 (1)
	B0U7B3	12 mA 50 kΩ Pull-up	29 (1)
	B0W7B3	12 mA 5 kΩ Pull-up	29 (1)
	B009B3	18 mA	32 (1)
	B0D9B3	18 mA 50 kΩ Pull-down	32 (1)
	B0U9B3	18 mA 50 kΩ Pull-up	32 (1)
	B0W9B3	18 mA 5 kΩ Pull-up	32 (1)
	B00HB3	24 mA	32 (1)
	B0DHB3	24 mA 50 kΩ Pull-down	32 (1)
	B0UHB3	24 mA 50 kΩ Pull-up	32 (1)
	B0WHB3	24 mA 5 kΩ Pull-up	32 (1)
Low-noise 3-State Buffer	BE0EB3	6 mA	22 (1)
	BEDEB3	6 mA 50 kΩ Pull-down	22 (1)
	BEUEB3	6 mA 50 kΩ Pull-up	22 (1)
	BEWEB3	6 mA 5 kΩ Pull-up	22 (1)
	BE08B3	9 mA	22 (1)
	BED8B3	9 mA 50 kΩ Pull-down	22 (1)
	BEU8B3	9 mA 50 kΩ Pull-up	22 (1)
	BEW8B3	9 mA 5 kΩ Pull-up	22 (1)
	BE07B3	12 mA	22 (1)
	BED7B3	12 mA 50 kΩ Pull-down	22 (1)
	BEU7B3	12 mA 50 kΩ Pull-up	22 (1)
	BEW7B3	12 mA 5 kΩ Pull-up	22 (1)
	BE09B3	18 mA	22 (1)
	BED9B3	18 mA 50 kΩ Pull-down	22 (1)
	BEU9B3	18 mA 50 kΩ Pull-up	22 (1)
	BEW9B3	18 mA 5 kΩ Pull-up	22 (1)
	BE0HB3	24 mA	22 (1)
	BEDHB3	24 mA 50 kΩ Pull-down	22 (1)
	BEUHB3	24 mA 50 kΩ Pull-up	22 (1)
	BEWHB3	24 mA 5 kΩ Pull-up	22 (1)

Function	Block	Description	Cells (I/O)
I/O Buffer	B00UBB	3 mA	38 (1)
	B0DUBB	3 mA 50 kΩ Pull-down	38 (1)
	B0UUBB	3 mA 50 kΩ Pull-up	38 (1)
	B0WUBB	3 mA 5 kΩ Pull-up	38 (1)
	B00CBB	6 mA	38 (1)
	B0DCBB	6 mA 50 kΩ Pull-down	38 (1)
	B0UCBB	6 mA 50 kΩ Pull-up	38 (1)
	B0WCBB	6 mA 5 kΩ Pull-up	38 (1)
	B003BB	9 mA	38 (1)
	B0D3BB	9 mA 50 kΩ Pull-down	38 (1)
	B0U3BB	9 mA 50 kΩ Pull-up	38 (1)
	B0W3BB	9 mA 5 kΩ Pull-up	38 (1)
	B001BB	12 mA	38 (1)
	B0D1BB	12 mA 50 kΩ Pull-down	38 (1)
	B0U1BB	12 mA 50 kΩ Pull-up	38 (1)
	B0W1BB	12 mA 5 kΩ Pull-up	38 (1)
	B005BB	18 mA	41 (1)
	B0D5BB	18 mA 50 kΩ Pull-down	41 (1)
	B0U5BB	18 mA 50 kΩ Pull-up	41 (1)
	B0W5BB	18 mA 5 kΩ Pull-up	41 (1)
	B00FBB	24 mA	41 (1)
	B0DFBB	24 mA 50 kΩ Pull-down	41 (1)
	B0UFBB	24 mA 50 kΩ Pull-up	41 (1)
	B0WFBB	24 mA 5 kΩ Pull-up	41 (1)
Low-noise I/O Buffer	BE0CBB	6 mA	31 (1)
	BEDCBB	6 mA 50 kΩ Pull-down	31 (1)
	BEUCBB	6 mA 50 kΩ Pull-up	31 (1)
	BEWCBB	6 mA 5 kΩ Pull-up	31 (1)
	BE03BB	9 mA	31 (1)
	BED3BB	9 mA 50 kΩ Pull-down	31 (1)
	BEU3BB	9 mA 50 kΩ Pull-up	31 (1)
	BEW3BB	9 mA 5 kΩ Pull-up	31 (1)
	BE01BB	12 mA	31 (1)
	BED1BB	12 mA 50 kΩ Pull-down	31 (1)
	BEU1BB	12 mA 50 kΩ Pull-up	31 (1)
	BEW1BB	12 mA 5 kΩ Pull-up	31 (1)
	BE05BB	18 mA	31 (1)
	BED5BB	18 mA 50 kΩ Pull-down	31 (1)
	BEU5BB	18 mA 50 kΩ Pull-up	31 (1)
	BEW5BB	18 mA 5 kΩ Pull-up	31 (1)
	BE0FBB	24 mA	31 (1)
	BEDFBB	24 mA 50 kΩ Pull-down	31 (1)
	BEUFBB	24 mA 50 kΩ Pull-up	31 (1)
	BEWFBB	24 mA 5 kΩ Pull-up	31 (1)

Function	Block	Description	Cells (I/O)
Schmitt I/O Buffer	BSIUBB	3 mA	42 (1)
	BSDUBB	3 mA 50 kΩ Pull-down	42 (1)
	BSUUBB	3 mA 50 kΩ Pull-up	42 (1)
	BSWUBB	3 mA 5 kΩ Pull-up	42 (1)
	BSICBB	6 mA	42 (1)
	BSDCBB	6 mA 50 kΩ Pull-down	42 (1)
	BSUCBB	6 mA 50 kΩ Pull-up	42 (1)
	BSWCBB	6 mA 5 kΩ Pull-up	42 (1)
	BSI3BB	9 mA	42 (1)
	BSD3BB	9 mA 50 kΩ Pull-down	42 (1)
	BSU3BB	9 mA 50 kΩ Pull-up	42 (1)
	BSW3BB	9 mA 5 kΩ Pull-up	42 (1)
	BSI1BB	12 mA	42 (1)
	BSD1BB	12 mA 50 kΩ Pull-down	42 (1)
	BSU1BB	12 mA 50 kΩ Pull-up	42 (1)
	BSW1BB	12 mA 5 kΩ Pull-up	42 (1)
	BSI5BB	18 mA	45 (1)
	BSD5BB	18 mA 50 kΩ Pull-down	45 (1)
	BSU5BB	18 mA 50 kΩ Pull-up	45 (1)
	BSW5BB	18 mA 5 kΩ Pull-up	45 (1)
	BSIFBB	24 mA	45 (1)
	BSDFBB	24 mA 50 kΩ Pull-down	45 (1)
	BSUFBB	24 mA 50 kΩ Pull-up	45 (1)
	BSWFBB	24 mA 5 kΩ Pull-up	45 (1)
Low-noise Schmitt I/O Buffer	BFICBB	6 mA	35 (1)
	BFDCBB	6 mA 50 kΩ Pull-down	35 (1)
	BFUCBB	6 mA 50 kΩ Pull-up	35 (1)
	BFWCBB	6 mA 5 kΩ Pull-up	35 (1)
	BFI3BB	9 mA	35 (1)
	BFD3BB	9 mA 50 kΩ Pull-down	35 (1)
	BFU3BB	9 mA 50 kΩ Pull-up	35 (1)
	BFW3BB	9 mA 5 kΩ Pull-up	35 (1)
	BFI1BB	12 mA	35 (1)
	BFD1BB	12 mA 50 kΩ Pull-down	35 (1)
	BFU1BB	12 mA 50 kΩ Pull-up	35 (1)
	BFW1BB	12 mA 5 kΩ Pull-up	35 (1)
	BFI5BB	18 mA	35 (1)
	BFD5BB	18 mA 50 kΩ Pull-down	35 (1)
	BFU5BB	18 mA 50 kΩ Pull-up	35 (1)
	BFW5BB	18 mA 5 kΩ Pull-up	35 (1)
	BFIFBB	24 mA	35 (1)
	BFDFBB	24 mA 50 kΩ Pull-down	35 (1)
	BFUFBB	24 mA 50 kΩ Pull-up	35 (1)
	BFWFBB	24 mA 5 kΩ Pull-up	35 (1)

Function	Block	Description	Cells (I/O)
N-ch Open drain Buffer	EXTHB2	3 mA	13 (1)
	EXUHB2	3 mA 50 kΩ Pull-up	13 (1)
	EXWHB2	3 mA 5 kΩ Pull-up	13 (1)
	EXTJB2	6 mA	13 (1)
	EXUJB2	6 mA 50 kΩ Pull-up	13 (1)
	EXWJB2	6 mA 5 kΩ Pull-up	13 (1)
	EXT1B2	9 mA	13 (1)
	EXT3B2	9 mA 50 kΩ Pull-up	13 (1)
	EXW3B2	9 mA 5 kΩ Pull-up	13 (1)
	EXT9B2	12 mA	13 (1)
	EXTBB2	12 mA 50 kΩ Pull-up	13 (1)
	EXWBB2	12 mA 5 kΩ Pull-up	13 (1)
	EXT5B2	18 mA	25 (1)
	EXT7B2	18 mA 50 kΩ Pull-up	25 (1)
	EXW7B2	18 mA 5 kΩ Pull-up	25 (1)
	EXTDB2	24 mA	25 (1)
	EXTFB2	24 mA 50 kΩ Pull-up	25 (1)
	EXWFB2	24 mA 5 kΩ Pull-up	25 (1)
Low-noise N-ch Open drain Buffer	EETJB2	6 mA	10 (1)
	EEUJB2	6 mA 50 kΩ Pull-up	10 (1)
	EEWJB2	6 mA 5 kΩ Pull-up	10 (1)
	EET1B2	9 mA	10 (1)
	EET3B2	9 mA 50 kΩ Pull-up	10 (1)
	EEW3B2	9 mA 5 kΩ Pull-up	10 (1)
	EET9B2	12 mA	10 (1)
	EETBB2	12 mA 50 kΩ Pull-up	10 (1)
	EEWBB2	12 mA 5 kΩ Pull-up	10 (1)
	EET5B2	18 mA	10 (1)
	EET7B2	18 mA 50 kΩ Pull-up	10 (1)
	EEW7B2	18 mA 5 kΩ Pull-up	10 (1)
	EETDB2	24 mA	10 (1)
	EETFB2	24 mA 50 kΩ Pull-up	10 (1)
	EEWFB2	24 mA 5 kΩ Pull-up	10 (1)

E.4.2 5 V Interface

Function	Block	Description	Cells (I/O)
Input Buffer	FIV1BI	-	7 (1)
	FDV1BI	50 kΩ Pull-down	7 (1)
	FIF1BI	-	11 (1)
	FDF1BI	50 kΩ Pull-down	11 (1)
	FIG1BI	-	56 (1)
	FDG1BI	50 kΩ Pull-down	56 (1)

Function		Block	Description	Cells (I/O)
CMOS Level	Output Buffer	FY09B2	3 mA	31 (1)
		FY04B2	6 mA	31 (1)
		FY01B2	9 mA	34 (1)
		FY02B2	12 mA	34 (1)
		FY03B2	18 mA	34 (1)
		FY06B2	24 mA	34 (1)
	Low-noise Output Buffer	FZ02B2	12 mA	33 (1)
		FZ03B2	18 mA	33 (1)
		FZ06B2	24 mA	33 (1)
	3-State Buffer	BD0TB3	3 mA	57 (1)
		BD0EB3	6 mA	57 (1)
		BD08B3	9 mA	60 (1)
		BD07B3	12 mA	60 (1)
		BD09B3	18 mA	60 (1)
		BD0HB3	24 mA	60 (1)
	Low-noise 3-State Buffer	BJ07B3	12 mA	51 (1)
		BJ09B3	18 mA	51 (1)
		BJ0HB3	24 mA	51 (1)
	I/O Buffer	BM0UBB	3 mA	66 (1)
		BM0CBB	6 mA	66 (1)
		BM03BB	9 mA	69 (1)
		BM01BB	12 mA	69 (1)
		BM05BB	18 mA	69 (1)
		BM0FBB	24 mA	69 (1)
	Low-noise I/O Buffer	BP01BB	12 mA	60 (1)
		BP05BB	18 mA	60 (1)
		BP0FBB	24 mA	60 (1)
	Schmitt I/O Buffer	BQIUBB	3 mA	70 (1)
		BQICBB	6 mA	70 (1)
		BQI3BB	9 mA	73 (1)
		BQI1BB	12 mA	73 (1)
		BQI5BB	18 mA	73 (1)
		BQIFBB	24 mA	73 (1)
	Low-noise Schmitt I/O Buffer	BUI1BB	12 mA	64 (1)
		BUI5BB	18 mA	64 (1)
		BUIFBB	24 mA	64 (1)
TTL Level	Output Buffer	FV0AB2	1 mA	13 (1)
		FV0BB2	2 mA	13 (1)
		FV09B2	3 mA	13 (1)
		FV04B2	6 mA	13 (1)
		FV01B2	9 mA	25 (1)
		FV02B2	12 mA	25 (1)
		FV03B2	18 mA	25 (1)
		FV06B2	24 mA	25 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Low-noise Output Buffer	FW02B2	12 mA	15 (1)
		FW03B2	18 mA	15 (1)
		FW06B2	24 mA	15 (1)
	3-State Buffer	BV0QB3	1 mA	52 (1)
		BVDQB3	1 mA 50 kΩ Pull-down	52 (1)
		BV0MB3	2 mA	52 (1)
		BVDMB3	2 mA 50 kΩ Pull-down	52 (1)
		BV0TB3	3 mA	52 (1)
		BVDTB3	3 mA 50 kΩ Pull-down	52 (1)
		BV0EB3	6 mA	52 (1)
		BVDEB3	6 mA 50 kΩ Pull-down	52 (1)
		BV08B3	9 mA	54 (1)
		BVD8B3	9 mA 50 kΩ Pull-down	54 (1)
		BV07B3	12 mA	54 (1)
		BVD7B3	12 mA 50 kΩ Pull-down	54 (1)
		BV09B3	18 mA	54 (1)
		BVD9B3	18 mA 50 kΩ Pull-down	54 (1)
		BV0HB3	24 mA	54 (1)
		BVDHB3	24 mA 50 kΩ Pull-down	54 (1)
	Low-noise 3-State Buffer	BY07B3	12 mA	39 (1)
		BYD7B3	12 mA 50 kΩ Pull-down	39 (1)
		BY09B3	18 mA	39 (1)
		BYD9B3	18 mA 50 kΩ Pull-down	39 (1)
		BY0HB3	24 mA	39 (1)
		BYDHB3	24 mA 50 kΩ Pull-down	39 (1)
	I/O Buffer	BW0XBB	1 mA	61 (1)
		BWDXBB	1 mA 50 kΩ Pull-down	61 (1)
		BW0KBB	2 mA	61 (1)
		BWDKBB	2 mA 50 kΩ Pull-down	61 (1)
		BW0UBB	3 mA	61 (1)
		BWDUBB	3 mA 50 kΩ Pull-down	61 (1)
		BW0CBB	6 mA	61 (1)
		BWDCBB	6 mA 50 kΩ Pull-down	61 (1)
		BW03BB	9 mA	63 (1)
		BWD3BB	9 mA 50 kΩ Pull-down	63 (1)
		BW01BB	12 mA	63 (1)
		BWD1BB	12 mA 50 kΩ Pull-down	63 (1)
		BW05BB	18 mA	63 (1)
		BWD5BB	18 mA 50 kΩ Pull-down	63 (1)
		BW0FBB	24 mA	63 (1)
		BWDFBB	24 mA 50 kΩ Pull-down	63 (1)

Function		Block	Description	Cells (I/O)
TTL Level	Low-noise I/O Buffer	BX01BB	12 mA	48 (1)
		BXD1BB	12 mA 50 kΩ Pull-down	48 (1)
		BX05BB	18 mA	48 (1)
		BXD5BB	18 mA 50 kΩ Pull-down	48 (1)
		BX0FBB	24 mA	48 (1)
		BXDFBB	24 mA 50 kΩ Pull-down	48 (1)
	Schmitt I/O Buffer	BKIXBB	1 mA	65 (1)
		BKDXBB	1 mA 50 kΩ Pull-down	65 (1)
		BKIKBB	2 mA	65 (1)
		BKDKBB	2 mA 50 kΩ Pull-down	65 (1)
		BKIUBB	3 mA	65 (1)
		BKDUBB	3 mA 50 kΩ Pull-down	65 (1)
		BKICBB	6 mA	65 (1)
		BKDCBB	6 mA 50 kΩ Pull-down	65 (1)
		BKI3BB	9 mA	67 (1)
		BKD3BB	9 mA 50 kΩ Pull-down	67 (1)
		BKI1BB	12 mA	67 (1)
		BKD1BB	12 mA 50 kΩ Pull-down	67 (1)
		BKI5BB	18 mA	67 (1)
		BKD5BB	18 mA 50 kΩ Pull-down	67 (1)
		BKIFBB	24 mA	67 (1)
		BKDFBB	24 mA 50 kΩ Pull-down	67 (1)
	Low-noise Schmitt I/O Buffer	BZI1BB	12 mA	52 (1)
		BZD1BB	12 mA 50 kΩ Pull-down	52 (1)
		BZI5BB	18 mA	52 (1)
		BZD5BB	18 mA 50 kΩ Pull-down	52 (1)
		BZIFBB	24 mA	52 (1)
		BZDFBB	24 mA 50 kΩ Pull-down	52 (1)
	N-ch Open drain Buffer	EVTTB2	1 mA	13 (1)
		EVTKB2	2 mA	13 (1)
		EVTHB2	3 mA	13 (1)
		EVTJB2	6 mA	13 (1)
		EVT1B2	9 mA	25 (1)
		EVT9B2	12 mA	25 (1)
		EVT5B2	18 mA	25 (1)
		EVTDB2	24 mA	25 (1)
	Low-noise N-ch Open drain Buffer	EYT9B2	12 mA	10 (1)
		EYT5B2	18 mA	10 (1)
		EYTDB2	24 mA	10 (1)

E.4.3 PCI

Function	Block	Description	Cells (I/O)
3V PCI Input Buffer	BP3IBI	-	7 (1)
3V PCI Output Buffer	BP3OB2	-	25 (1)
3V PCI 3-State Buffer	BP3TB3	-	32 (1)
3V PCI I/O Buffer	BP3BBB	-	41 (1)
5V PCI Input Buffer	BP5IBI	-	7 (1)
5V PCI Output Buffer	BP5OB2	-	25 (1)
5V PCI 3-State Buffer	BP5TB3	-	54 (1)
5V PCI I/O Buffer	BP5BBB	-	63 (1)

E.5 Boundary Scan Block (Function)

E.5.1 TAP Macro

Function	Block	Description	Cells (I/O)
TAP MACRO	SBC4	-	- (-)
TAP Macro with NEC Scan	SBCL	-	- (-)

E.5.2 Level Generator

Function	Block	Description	Cells (I/O)
Level Generator(CLANP)	SBZ1	-	0 (-)

E.5.3 D-Latch

Function	Block	Description	Cells (I/O)
D-Latch with SB Q Out (Low Power) for Boundary Scan Block	L606	-	5 (-)

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