PFESiP EP-1 Evaluation Board Lite

TITLE		*Midas lab*
Title: PFESiP EP-1 Evaluation Board Lite		
Size: A3	Document Number: S813BA01	Rev: 1.0
Date: Monday, July 28, 2008	Sheet 1 of 16	

Date	Revision	Page	Description of Changes
2008.02.15	0.0		First Edition
2008.03.13	0.0	7	1Kohm is mounted on R31. R33 is unmounted.
2008.03.21	0.0	10	0ohm is mounted on R79. R78 is unmounted.
2008.04.12	0.1	8	1. U10 TL7705ACD is changed to TL7702ACD. Additionally, the following corrections. U10:7 --x-- +5V (The pattern is cut.) U10:7 -- 5.6K -- +5V U10:7 -- 10K -- GND 2. Remodeling of RST- of CP2102. U9:2 --x-- U7:11 (The pattern is cut.)
		16	3. CA1 100uF is changed to 470uF.
2008.04.21	1.0	7,8,10,12,16	The parts number of LED was changed.
		14	CN11(JTAG) is unmounted.
2008.04.24	1.0	7,8,10,12	The value of resister for LED was changed.
2008.05.13	1.0	10	The value of resister(R81,R82) for LED was changed.

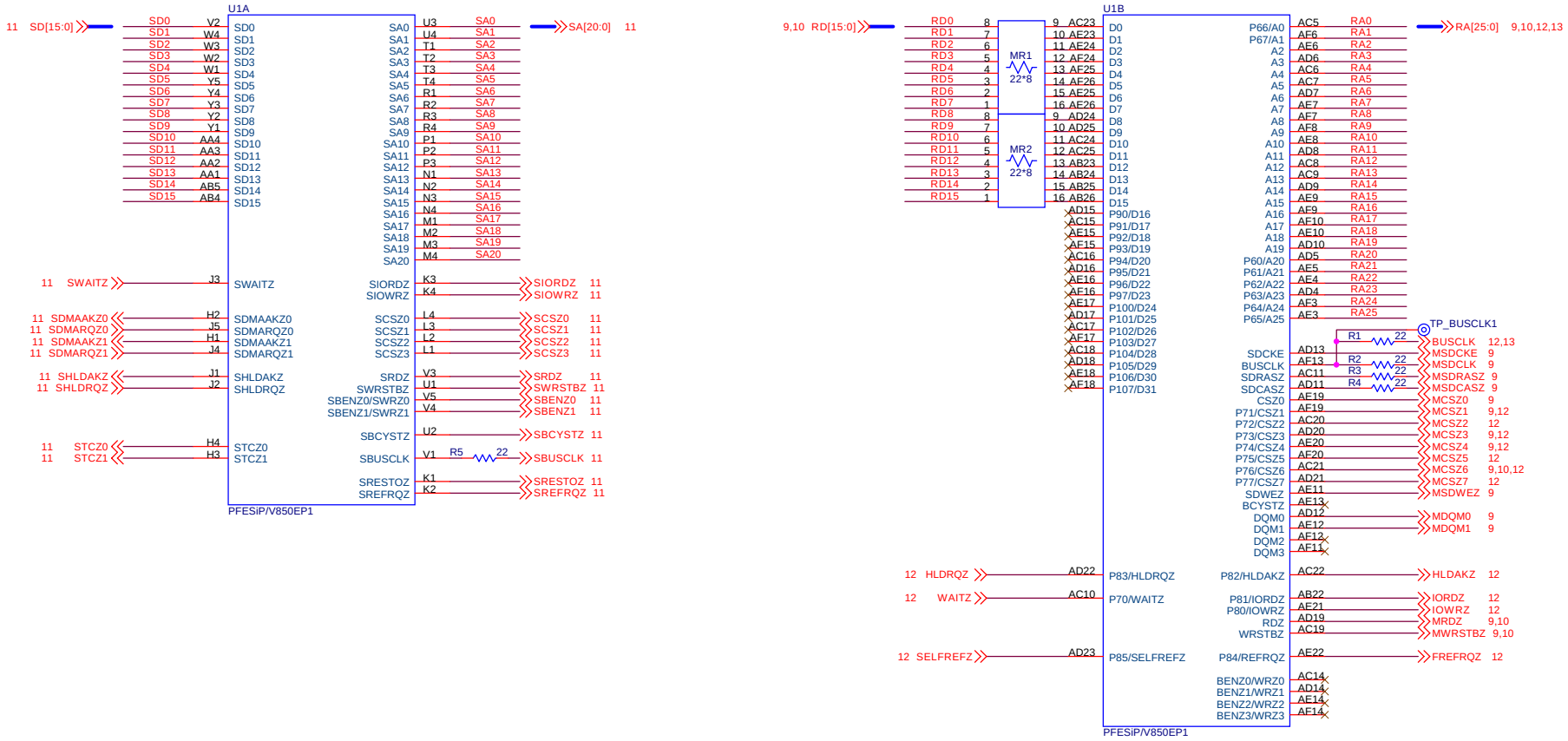
REVISION LEVEL HISTORY

Midas lab

Title: PFESiP EP-1 Evaluation Board Lite

Size: A3 | Document Number: S813BA01 | Rev: 1.0

Date: Monday, July 28, 2008 | Sheet 2 of 16



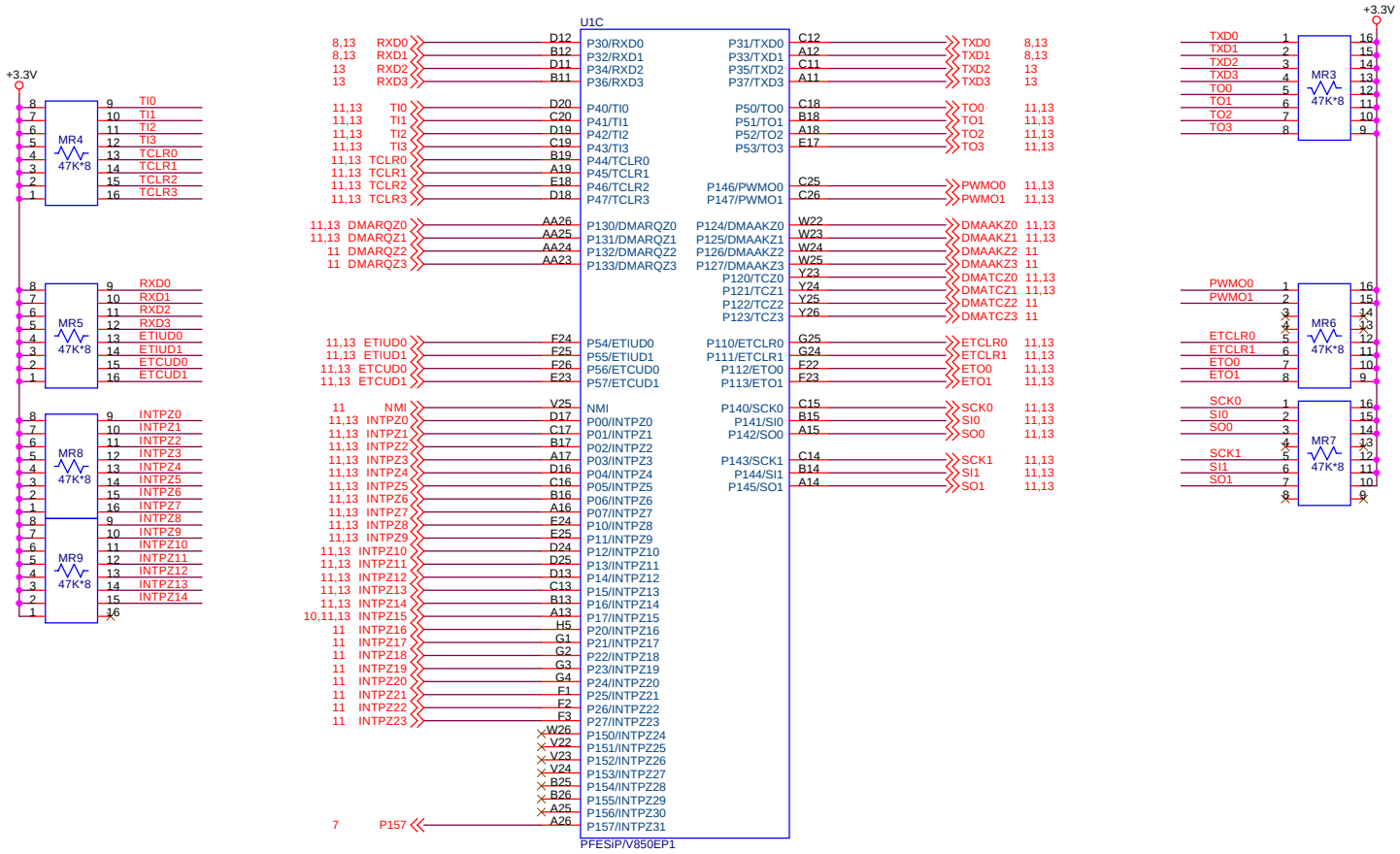
CPU(SBUS, MEMC)

Midas lab

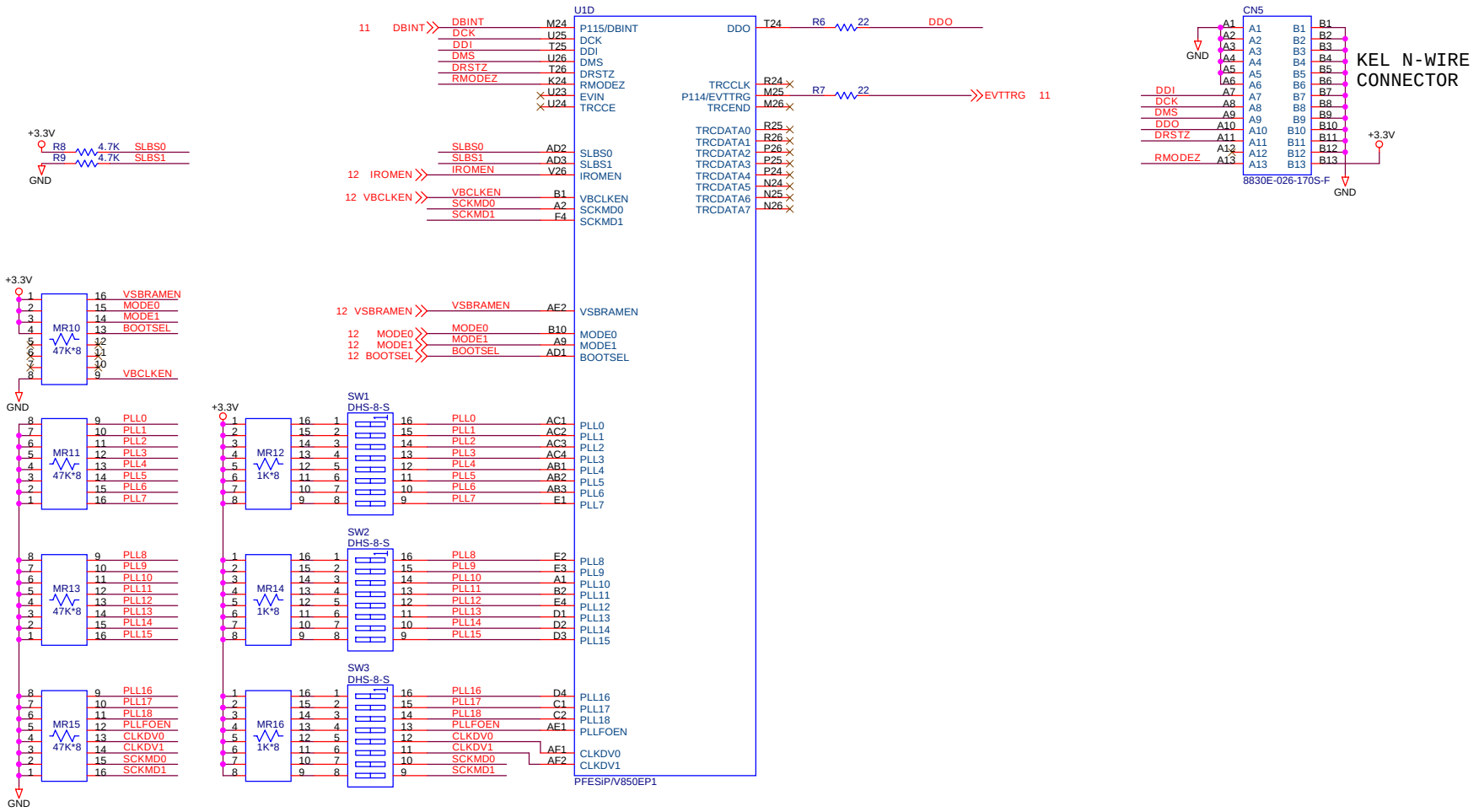
Title: PFESiP EP-1 Evaluation Board Lite

Size	Document Number	Rev
A3	S813BA01	1.0

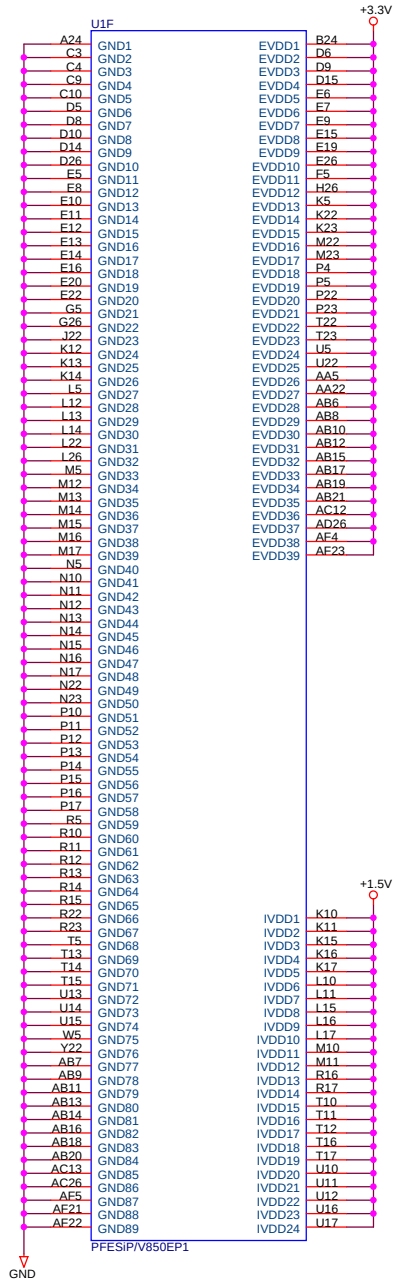
Date: Monday, July 28, 2008 Sheet 3 of 16



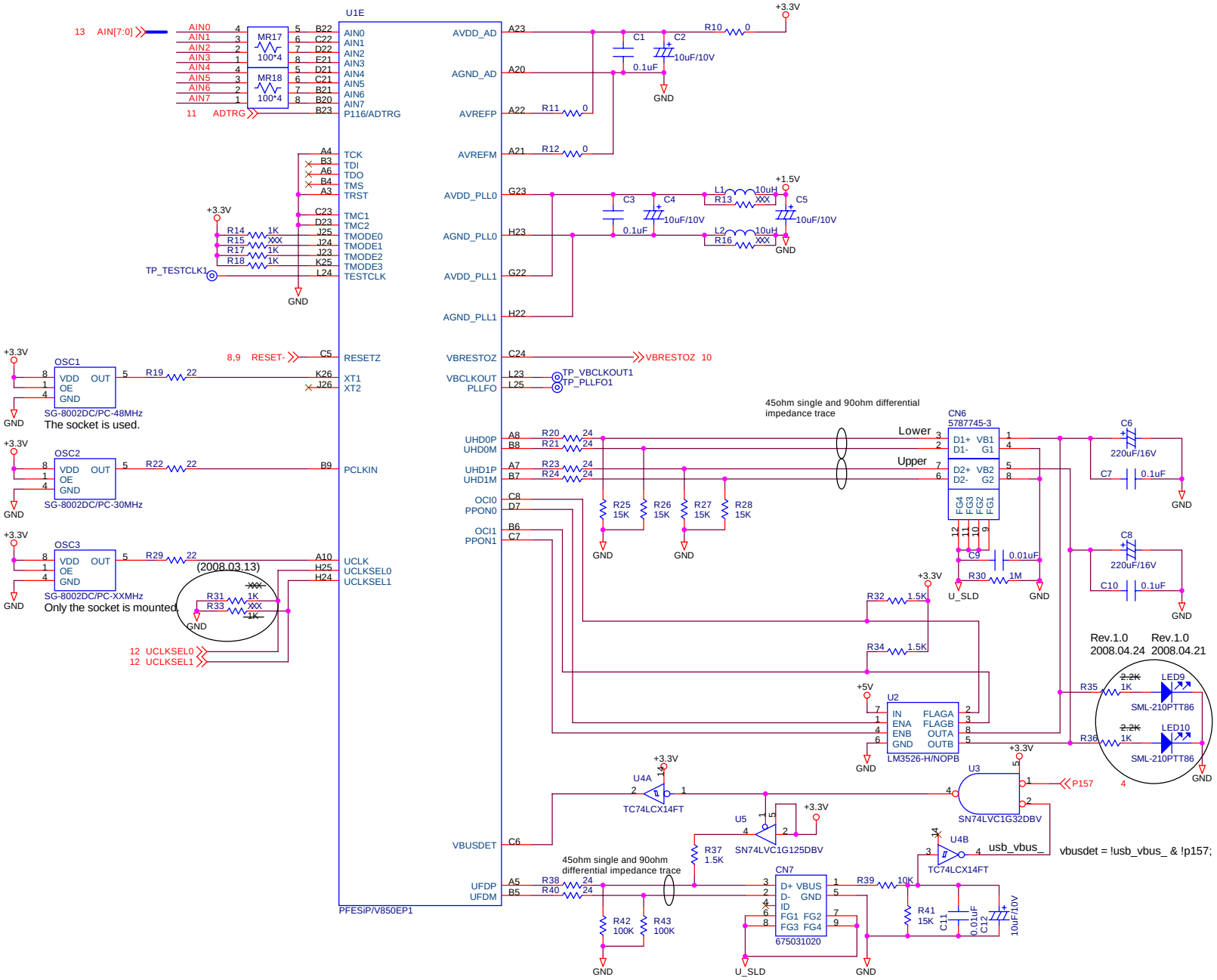
CPU(PORT)		**Midas lab**
Title	PFESiP EP-1 Evaluation Board Lite	
Size: A3	Document Number: S813BA01	Rev: 1.0
Date: Monday, July 28, 2008	Sheet 4 of 16	



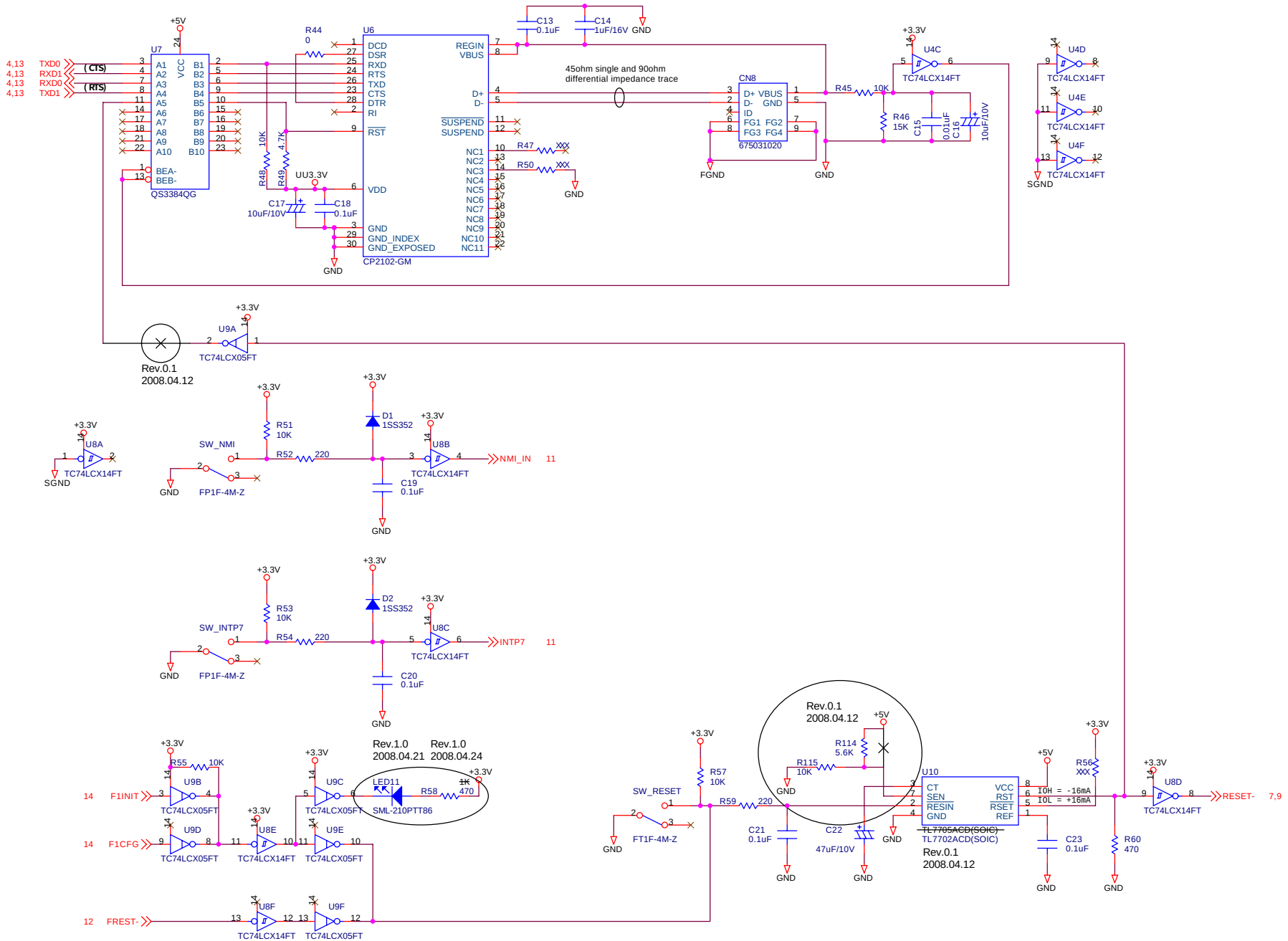
CPU(ModeSW, N-Wire)		Midas lab
Title	PFESiP EP-1 Evaluation Board Lite	
Size A3	Document Number S813BA01	Rev 1.0
Date: Monday, July 28, 2008	Sheet 5 of 16	



CPU(PS)		**Midas lab**
Title	PFESiP EP-1 Evaluation Board Lite	
Size A3	Document Number S813BA01	Rev 1.0
Date: Monday, July 28, 2008	Sheet 6 of 16	

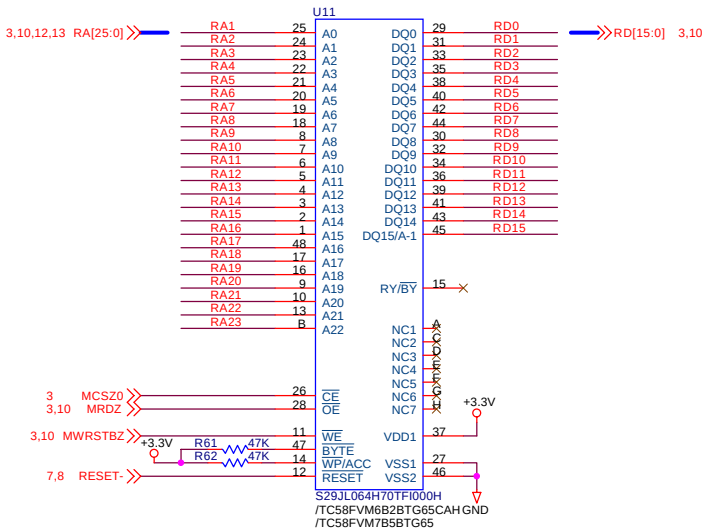


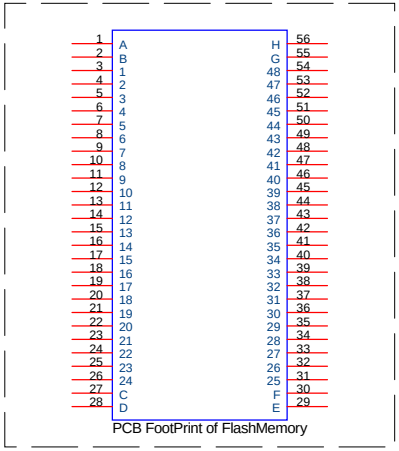
CPU(A/D,USB2.0)			**Midas lab**
Title	PFESiP EP-1 Evaluation Board Lite		
Size A3	Document Number S813BA01		Rev 1.0
Date: Monday, July 28, 2008	Sheet 7	of 16	



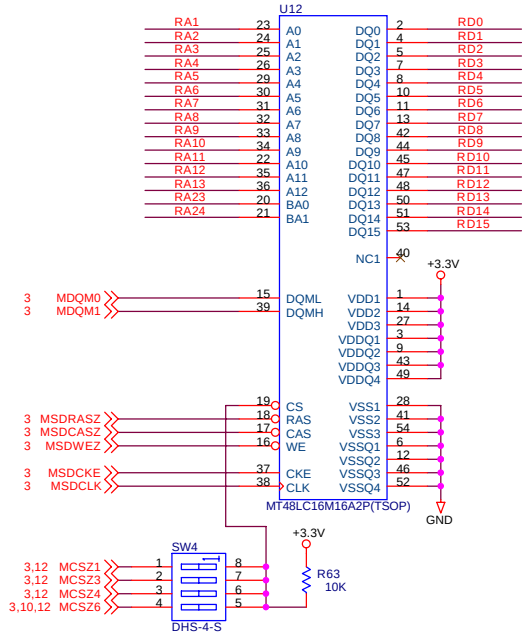
DSUB9,PushSW,PON_RES		Midas lab
Title	PFESiP EP-1 Evaluation Board Lite	
Size A3	Document Number S813BA01	Rev 1.0
Date: Monday, July 28, 2008	Sheet 8 of 16	

[FlashMemory]

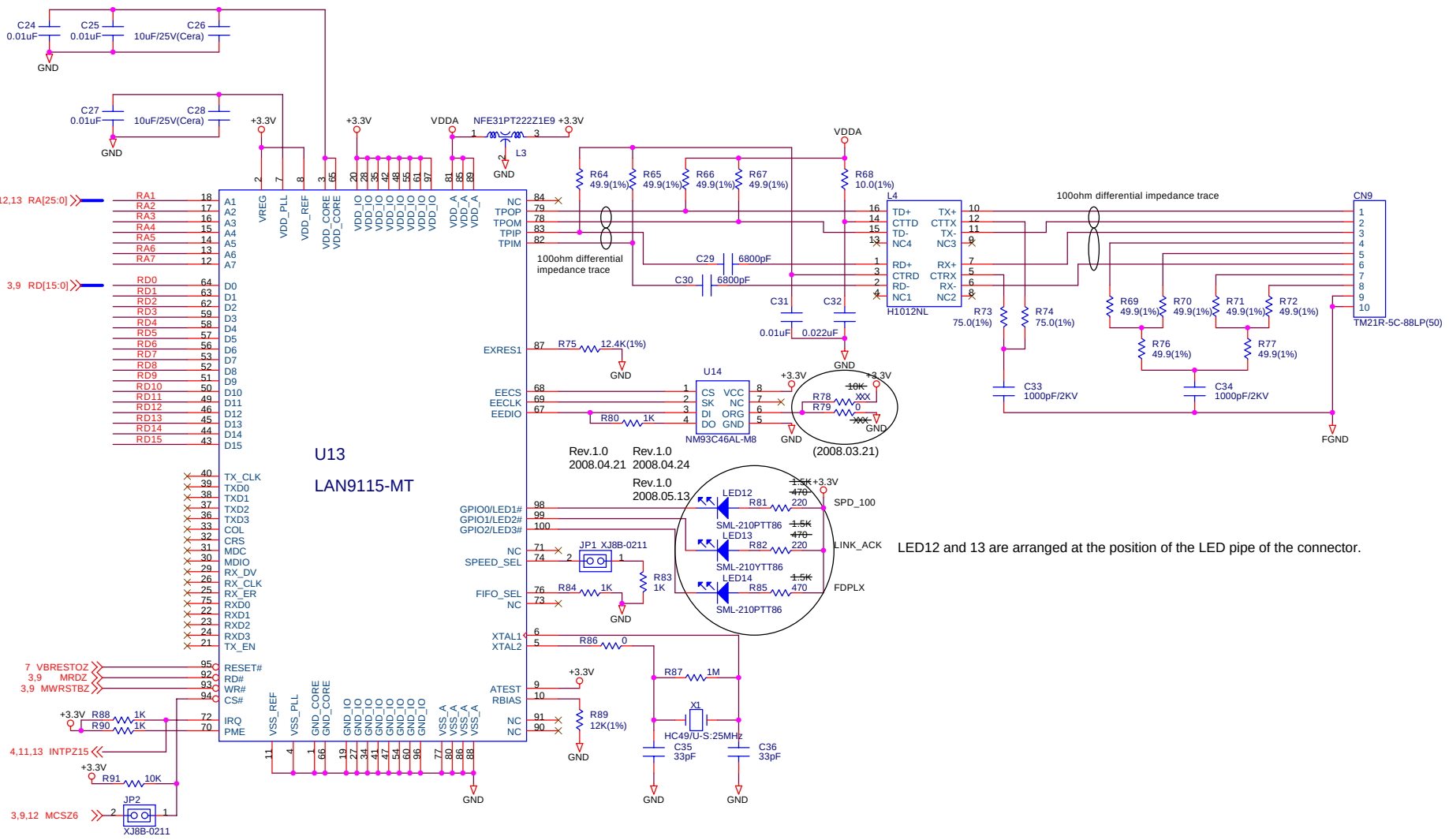




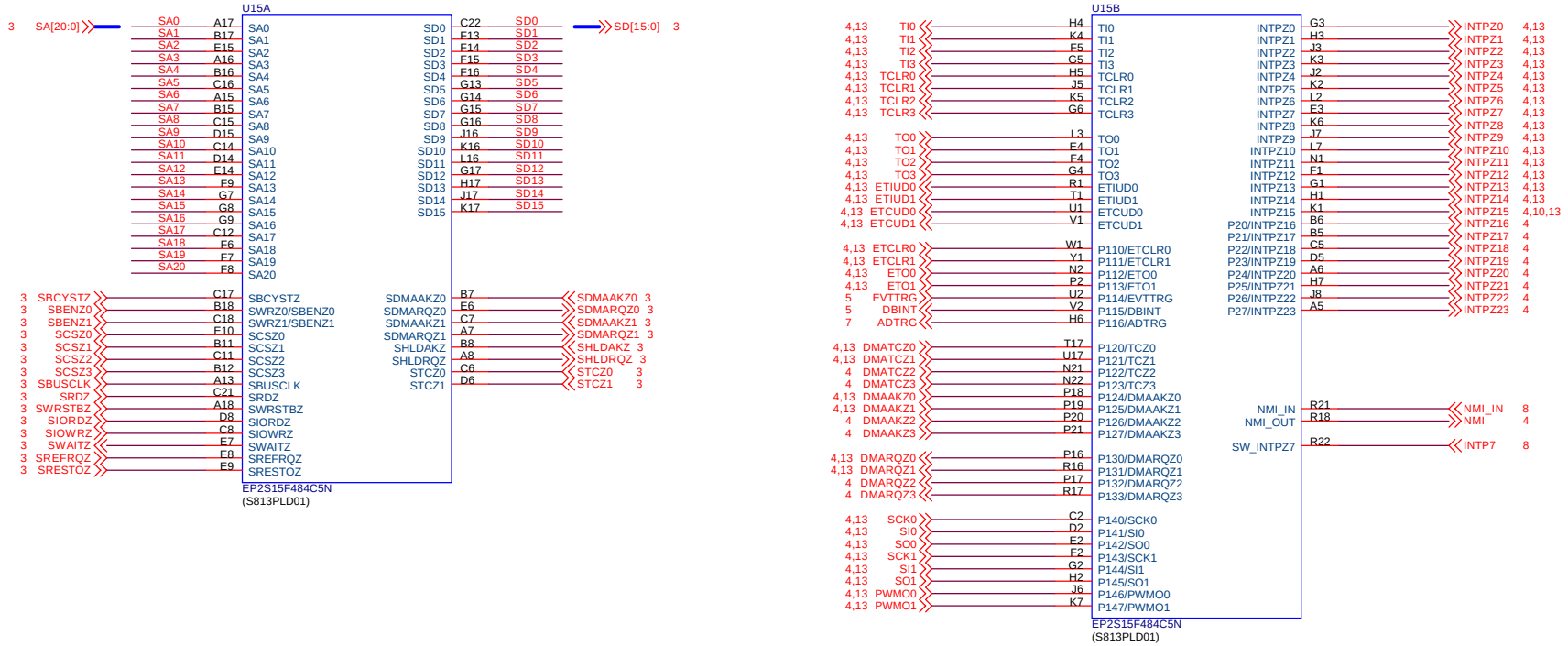
[SDRAM]



FROM,SDRAM16		**Midas lab**
Title	PFESiP EP-1 Evaluation Board Lite	
Size A3	Document Number S813BA01	Rev 1.0
Date: Monday, July 28, 2008	Sheet 9 of 16	



LAN		Midas lab
Title	PFESiP EP-1 Evaluation Board Lite	
Size A3	Document Number S813BA01	Rev 1.0
Date: Monday, July 28, 2008	Sheet 10 of 16	



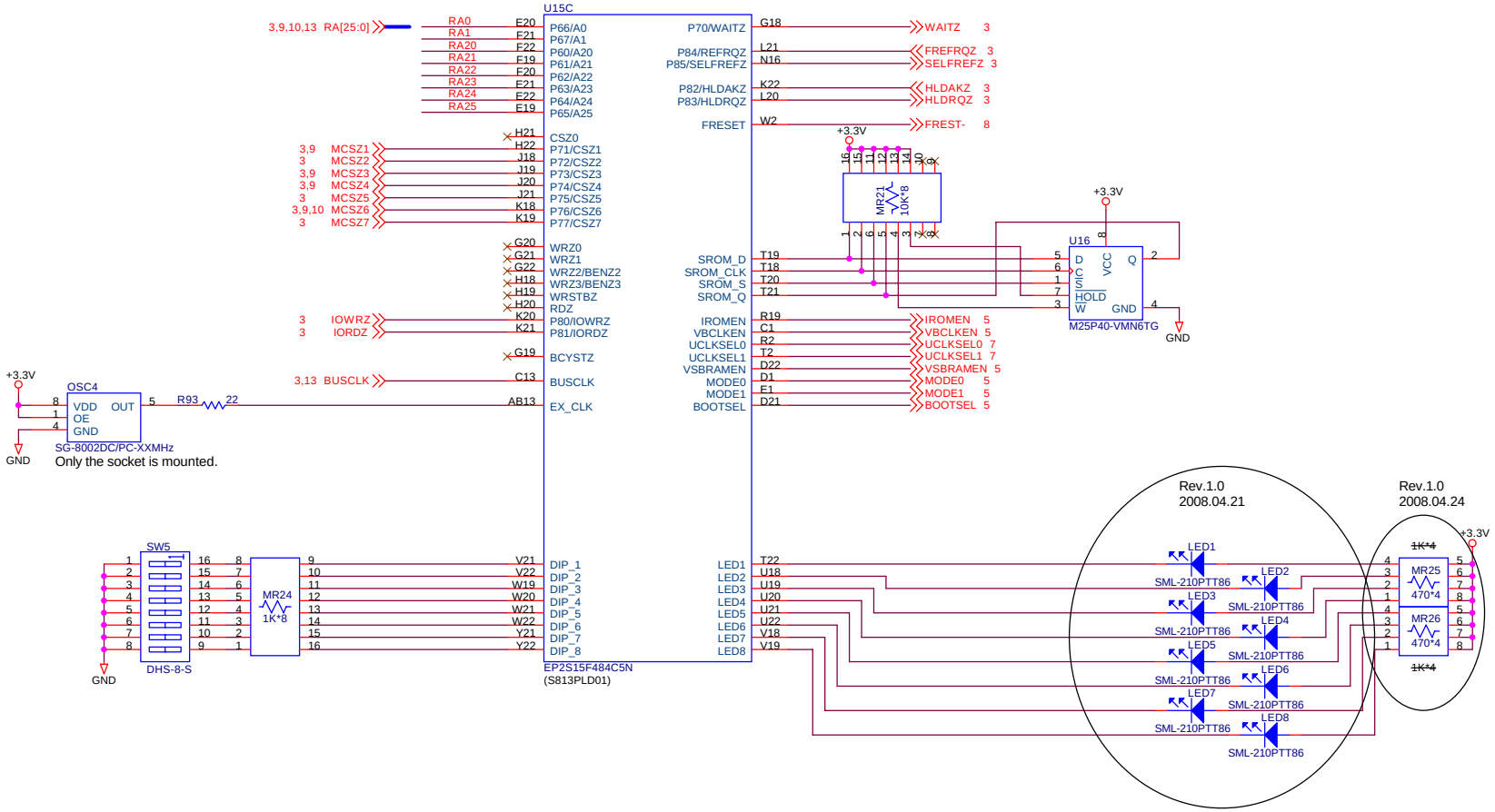
FPGA1(SBUS,PORT)

Midas lab

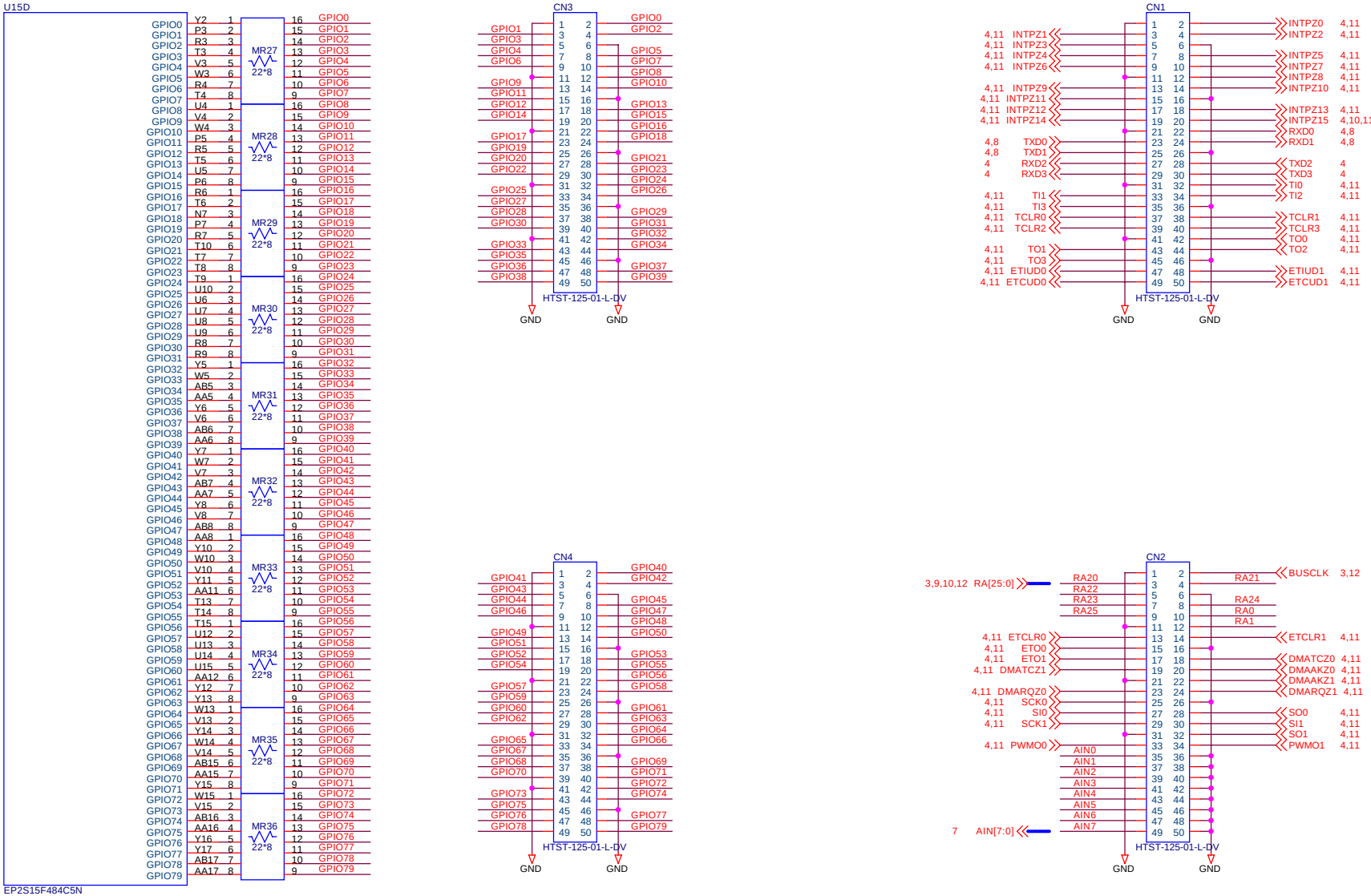
Title: PFESiP EP-1 Evaluation Board Lite

Size	Document Number	Rev
A3	S813BA01	1.0

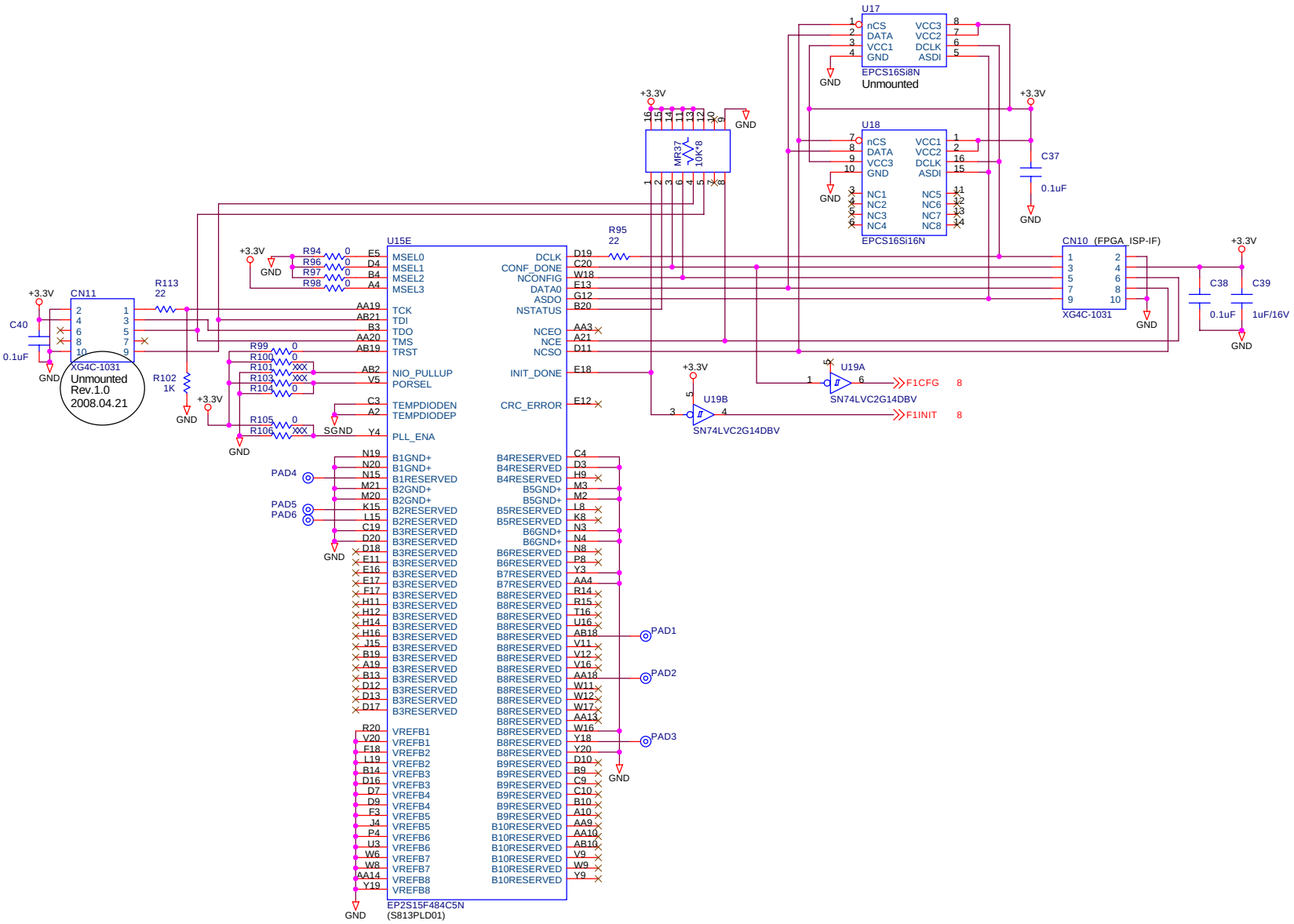
Date: Monday, July 28, 2008 Sheet 11 of 16



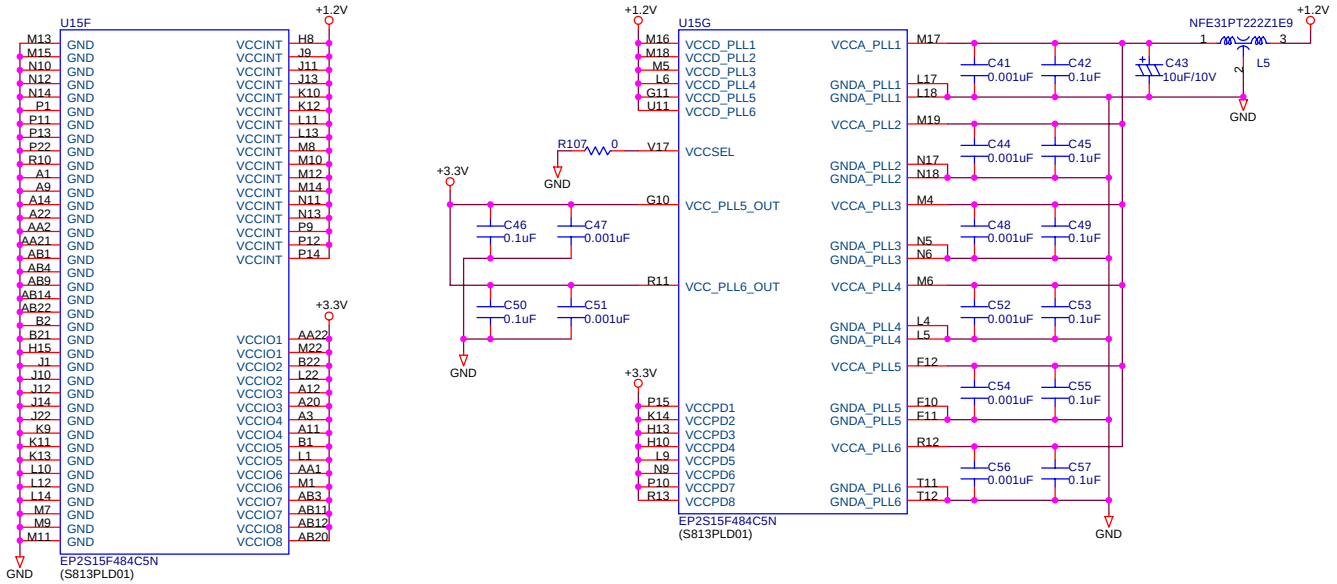
FPGA1(MEM I/F, MISC)		Midas lab
Title: PFESiP EP-1 Evaluation Board Lite		
Size: A3	Document Number: S813BA01	Rev: 1.0
Date: Monday, July 28, 2008	Sheet 12 of 16	



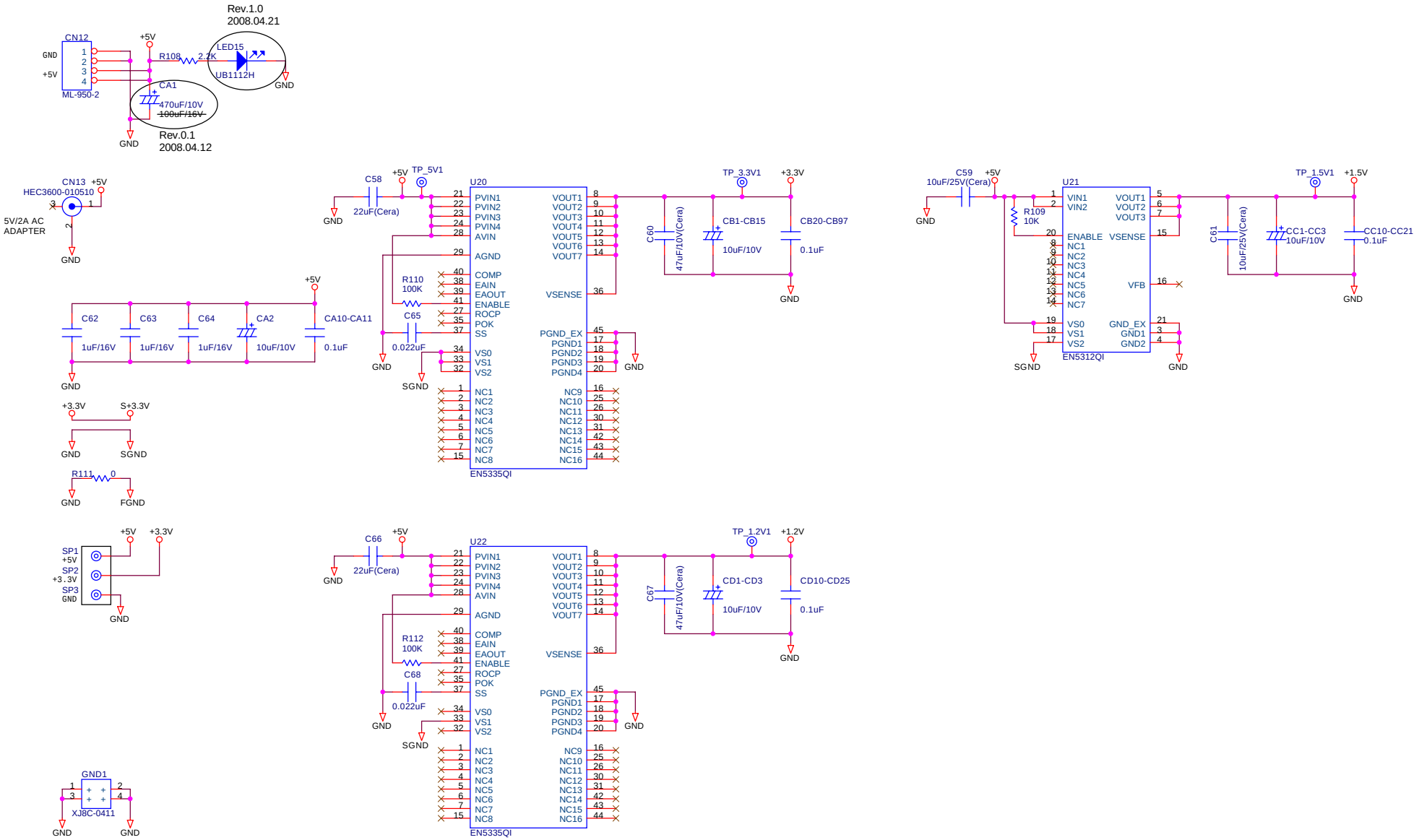
FPGA1(GPIO), CON50			**Midas lab**
Title: PFESiP EP-1 Evaluation Board Lite			
Size: A3	Document Number: S813BA01		Rev: 1.0
Date: Monday, July 28, 2008	Sheet 13 of 16		



FPGA1(Configuration)			**Midas lab**
Title	PFESiP EP-1 Evaluation Board Lite		
Size A3	Document Number S813BA01		Rev 1.0
Date: Monday, July 28, 2008	Sheet 14 of 16		



FPGA1(PS)		**Midas lab**
Title	PFESiP EP-1 Evaluation Board Lite	
Size A3	Document Number S813BA01	Rev 1.0
Date: Monday, July 28, 2008	Sheet 15 of 16	



PS		Midas lab
Title	PFESiP EP-1 Evaluation Board Lite	
Size A3	Document Number S813BA01	Rev 1.0
Date: Monday, July 28, 2008	Sheet 16 of 16	