To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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# PFESiP® EP-1
# Configurable motor control engine

## Overview

NEC Electronics' PFESiP EP-1 Series[Note] is an SiP-type customizable microcontroller that adopts the V850 architecture which has a high real-time response, which is suitable for motor controls of industrial equipment such as servos and inverters. And PFESiP EP-1 is provided with a USB 2.0 device/host controller, a customizable gate block of up to 240 K gates, and low EMI noise. By these functions, development costs and the development period can be reduced to as low as a tenth a full-customizable microcontroller or SoC.

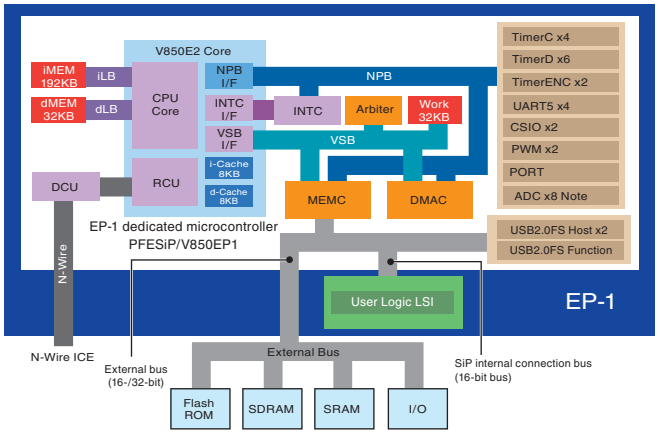
Number of components and board area can also be reduced from multi-components use such as stand-alone microcontroller with separate logic ICs. It further makes the motherboard design easier and achieves higher electrical reliability in connection between microcontroller and logic ICs.(e.g. reduction of SSO noise and EMS)

**Note** PFESiP : Platform for Embedded System in a Package
EP-1 : Embedded Processor -1

## Features

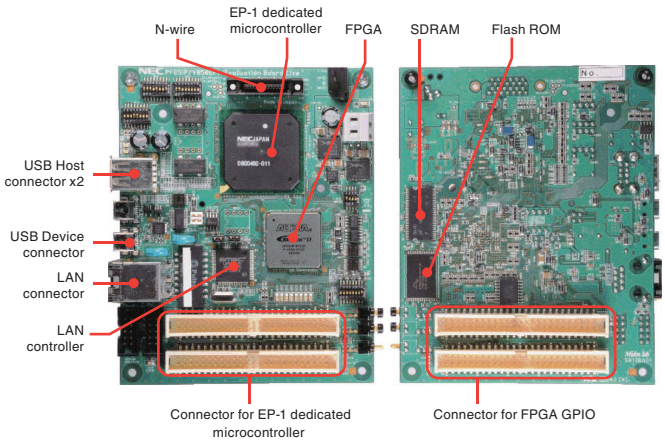
- V850E2 CPU core max. 200MHz operation
- Customizable logic block of 240 K gates
- Three types of masters are provided according to the logic capacity (80K/160K/240K gates).
- With USB2.0FS port mounted (Host x 2, device x 1)
- Selectable external-bus (16-/32-bit)
- With 192 KB instruction RAM mounted
- Low-thermal resistance PBGA package (1.0/0.8 mm pitch)
- USB sample program available

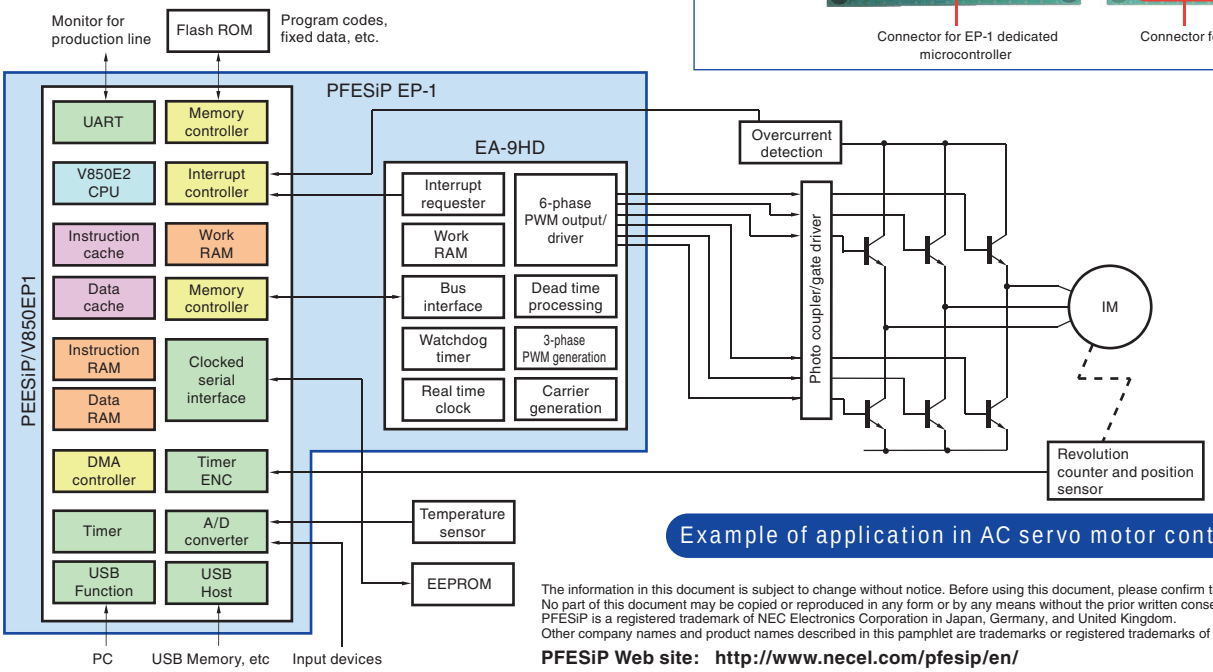
## EP-1 block diagram




**Note** The ADC function can be used only when a 32-bit external bus is used.

## EP-1 Evaluation Board Lite




Example of application in AC servo motor control engine



**PFESiP Web site: http://www.necel.com/pfesip/en/**

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