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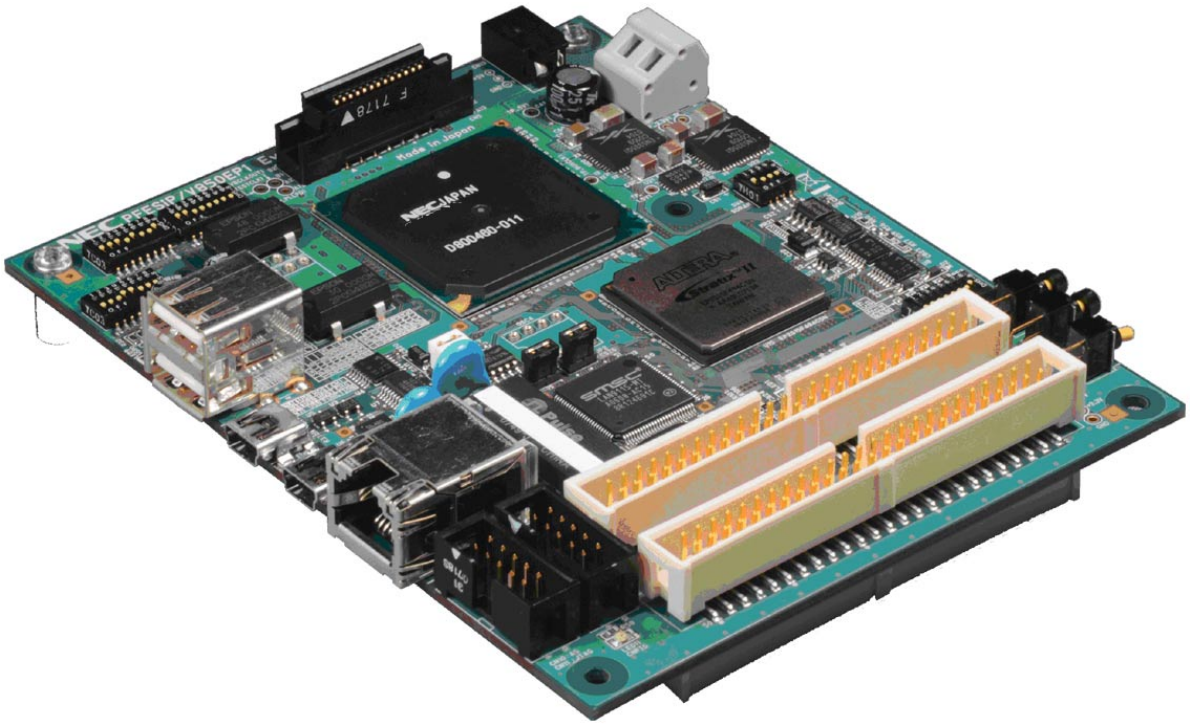
RENESAS

User's Manual

PFESiP® EP-1
Evaluation Board Lite

Technical Information

Document No. A19354EJ1V1UM00 (1st edition)
Date published September 2008 NS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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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PREFACE

Readers This manual is intended for users who understand the functions of the microcontroller function chip with an on-chip V850E2 CPU core (PFESiP/V850EP1) and wish to evaluate developing PFESiP EP-1 Series products using the chip.

Purpose This manual is intended to help users, who wish to evaluate introducing PFESiP EP-1 Series products using the PFESiP/V850EP1, understand how to use the development evaluation board.

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, microcontrollers, SRAM, page ROM, and SDRAM.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representation:	xxxZ (Z after pin or signal name)	
Note:	Footnote for item marked with Note in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numeric representation:	Binary ... xxxx or xxxxB	
	Decimal ... xxxx	
	Hexadecimal ... xxxxH	
Prefix indicating power of 2 (address space, memory capacity):	K (kilo):	$2^{10} = 1,024$
	M (mega):	$2^{20} = 1,024^2$
	G (giga):	$2^{30} = 1,024^3$
Data type:	Word … 32 bits	
	Half-word … 16 bits	
	Byte … 8 bits	

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Furthermore, some related documents may be intended for individual customers, because the documents are prepared in the development/planning stage of each core.

Documents Related to PFESiP EP-1 Series

Document Name	Document No.
V850E2 Architecture User's Manual	U17135E
PFESiP EP-1 Series Design Manual	A19068E
PFESiP/V850EP1 Product Data User's Manual	A19069E
PFESiP/V850EP1 Hardware (CPU Function) User's Manual	A19070E
PFESiP/V850EP1 Hardware (USB Function) User's Manual	A19071E
PFESiP/V850EP1 USB Function Sample Software Application Note	A19349E

Documents Related to PFESiP EP-1 Evaluation Board

Document Name	Document No.
PFESiP EP-1 Evaluation Board Technical Information User's Manual	A19350E
PFESiP EP-1 Evaluation Board Lite Technical Information User's Manual	This manual

Documents Related to development tools (User's Manual)

Document Name			Document No.
RX850 Pro (Real-Time OS)	Ver.3.21	Basics	U18165E
	Ver.3.20	Installation	U17421E
	Ver.3.21	Technical	U18164E
	Ver.3.20	Task Debugger	U17422E
PM+ Ver. 6.30 Project Manager			U18416E
QB-V850MINI On-Chip Debug Emulator			U17638E
ID850QB Ver. 3.20 Integrated Debugger	Operation		U17964E
RX850V4 Ver. 4.22 Real-Time OS	Functionalities		U16643E
	Task Debugger		U16811E
AZ850V4 Ver. 4.10 System Performance Analyzer			U17093J

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CHAPTER 1 INTRODUCTION

The PFESiP EP-1 Evaluation Board Lite is a development evaluation board for assisting the development of PFESiP EP-1 Series products and can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and for user logic development and verification using the on-board FPGA.

The PFESiP/V850EP1 has an on-chip high-performance 32-bit RISC-type CPU core (V850E2 core).

The basic functions of PFESiP EP-1 Series products based on the PFESiP/V850EP1 can be evaluated using this board.

The PFESiP EP-1 Evaluation Board Lite is a development evaluation board whose price has been reduced by reducing the functions of the PFESiP EP-1 Evaluation Board and that has been developed for users wishing to evaluate introducing the PFESiP EP-1 Series products.

The Stratix® II EP2S15F484C5 made by Altera is used as the on-board FPGA and the Quartus® II Web Edition can be used.

Use the PFESiP EP-1 Evaluation Board when adding an external board requiring numerous signals, or when requiring a large-capacity logic cell or on-board RAM, because the size of the on-board FPGA is smaller in contrast to the PFESiP EP-1 Evaluation Board.

1.1 Overview of PFESiP EP-1 Evaluation Board Lite

The PFESiP EP-1 Evaluation Board Lite is a development evaluation board for assisting the development of PFESiP EP-1 Series products.

It can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and as a PFESiP EP-1 prototyping environment by using the functions of the embedded array (EA-9HD), which is provided with the user logic paired with the PFESiP/V850EP1, for user logic development and verification by the on-board FPGA within the PFESiP EP-1 Series SiP. A more systematic evaluation can be performed by connecting the PFESiP EP-1 Evaluation Board Lite to the user board using expansion connectors. Furthermore, a flash ROM and an SDRAM are provided as on-board memories.

Note that the load capacitance of the PFESiP EP-1 Evaluation Board Lite is not always equivalent, in contrast to the environment of actual SiP products, because the signals originally connected within the SiP are connected to the FPGA on-board.

Remark See the **PFESiP/V850EP1 User's Manual** for the functions and specifications of the PFESiP/V850EP1.

1.1.1 Features

(1) On-board memory

A flash ROM and SDRAM which can be directly accessed via the external bus interface (MEMC I/F) of the PFESiP/V850EP1 is mounted on-board and a general memory system is provided.
A memory system with a 32-bit width cannot be used.

On-Board Memory Type	Capacity	Connection Bit Width
Flash ROM	8 MB	16 bits
SDRAM	32 MB	16 bits

(2) On-board FPGA (Altera™ Stratix II)

An FPGA, Stratix II EP2S15F484C5 made by Altera is mounted on-board. The Quartus II Web Edition design software can be downloaded from the Altera Web site free of charge.
The SiP internal connection bus interface of the PFESiP/V850EP1 and almost all signals of the NPB macro I/O pins are connected to this FPGA. The functions of an embedded array to be used in combination with the PFESiP/V850EP1 are performed by this on-board FPGA. In addition, arbitrary signals can be connected via the on-board FPGA, because most expansion connector signals are connected via the FPGA.
External bus interface (MEMC I/F) signals are not connected to the FPGA.
An LED (red) is connected to the DONE signal that indicates that configuring the FPGA has been completed. The LED indicates that the configuration has been started when it is lit and indicates that the configuration has ended when it is turned off.

Mounted FPGA	Size of Reference Circuit Equivalent to CB-IC	Logic Element	Total Number of Bytes of RAM	Number of I/Os
EP2S15F484C5	152 K gates	15,600	52 Kb	342 Note

Note 342 I/Os can be used with the EP2S15F484C5, but only 271 I/Os are used with the PFESiP EP-1 Evaluation Board Lite.

Caution The PFESiP EP-1 Evaluation Board Lite does not support BTO selection of the FPGA. The FPGA cannot be changed to a higher-grade pin-compatible FPGA.

(3) Expansion connectors

General-purpose 50-pin connectors are equipped.

Connector	No. of Valid Signals	Purpose
General-purpose 50-pin connectors	CN1 (40)	For on-chip peripheral function I/Os of the PFESiP/V850EP1
	CN2 (27)	8 are used as A/D converter inputs. (16 pins, including the GND pins used in combination with the above pins are used.)
	CN3 (40)	For on-board FPGA I/Os (GPIO)
	CN4 (40)	

(4) USB 2.0 FS and UART interface (supported by USB-to-serial signal conversion)

The following general-purpose interfaces are provided by the internal functions of the PFESiP/V850EP1.

Interface Type	Connector	Remark
USB 2.0 FS/LS Host × 2	USB B type (CN6)	2-port host connector × 1
USB 2.0 FS Function × 1	USB mini B type (CN7)	
USB 2.0 support (12 Mbps) ↔ On-chip UART5 of PFESiP/V850EP1	USB mini B type (CN8)	On-chip UART5 of PFESiP/V850EP1 is converted to USB 2.0, using bridge IC CP2102.

(5) On-board power supply circuit

AC adapters (5 V, 2 A, positive center pin, EIJ-2 standard DC jack) are supported.

The AC adapter dedicated to the PFESiP EP-1 Evaluation Board cannot be used.

The required 3.3 V, 1.5 V, and 1.2 V power supplies are supplied by the on-board power supply circuit.

(6) Operating mode setting

The various operating modes of the PFESiP/V850EP1 can be set using the output from the FPGA. (A default FPGA data template is attached.)

The multiplication and modulation rates of the on-chip SSCG-PLL of the PFESiP/V850EP1 can be set using the dip switches. (Changing the multiplication or modulation rate during operation is not supported.)

(7) On-chip debug function

The on-chip debug function performed by the N-Wire interface is supported by the on-chip DCU (debug control unit) of the PFESiP/V850EP1.

This evaluation board does not support the trace function.

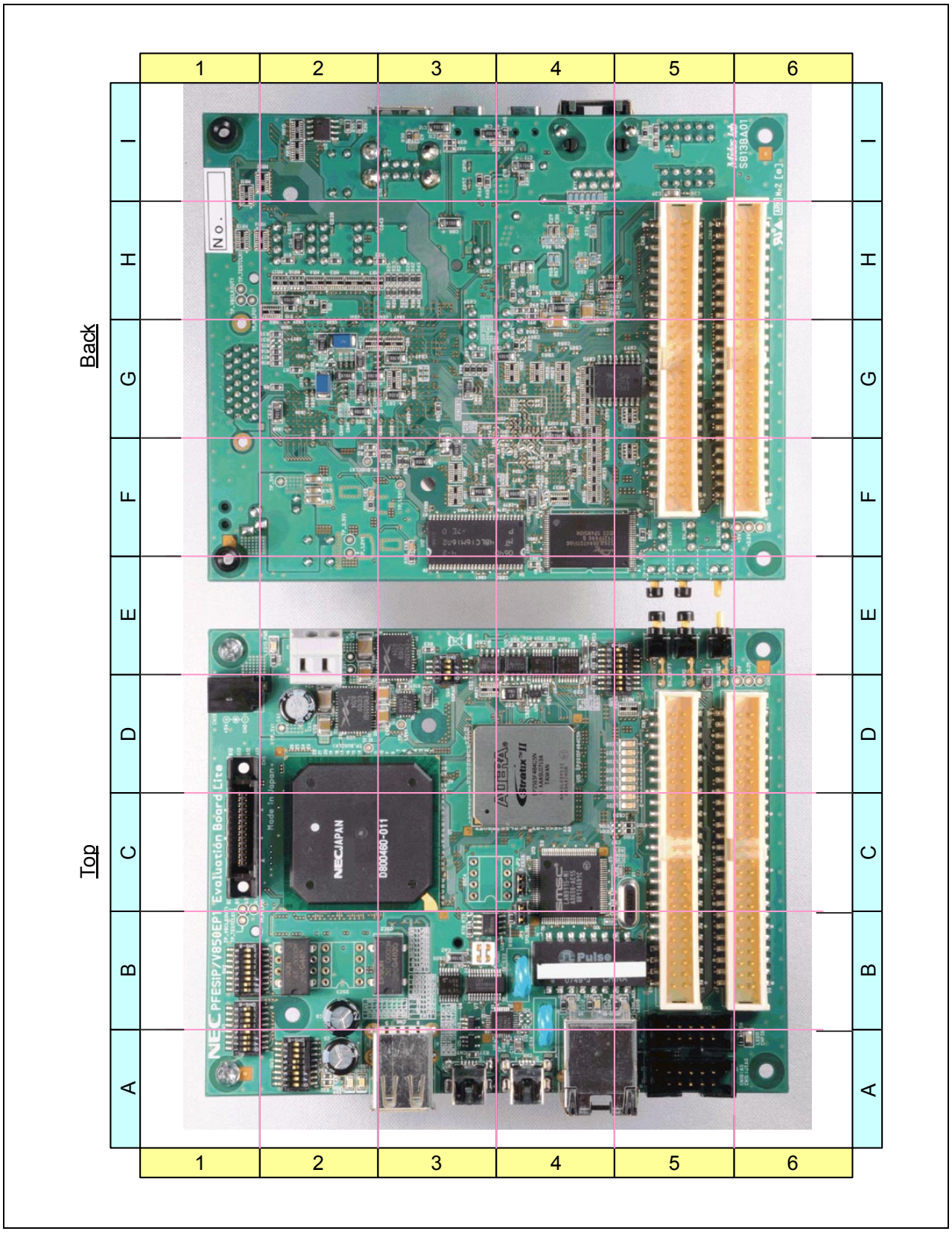
The MINICUBE made by NEC Electronics is the recommended in-circuit emulator.

1.1.2 Appearance of PFESiP EP-1 Evaluation Board Lite

The appearance of the PFESiP EP-1 Evaluation Board Lite is shown below.

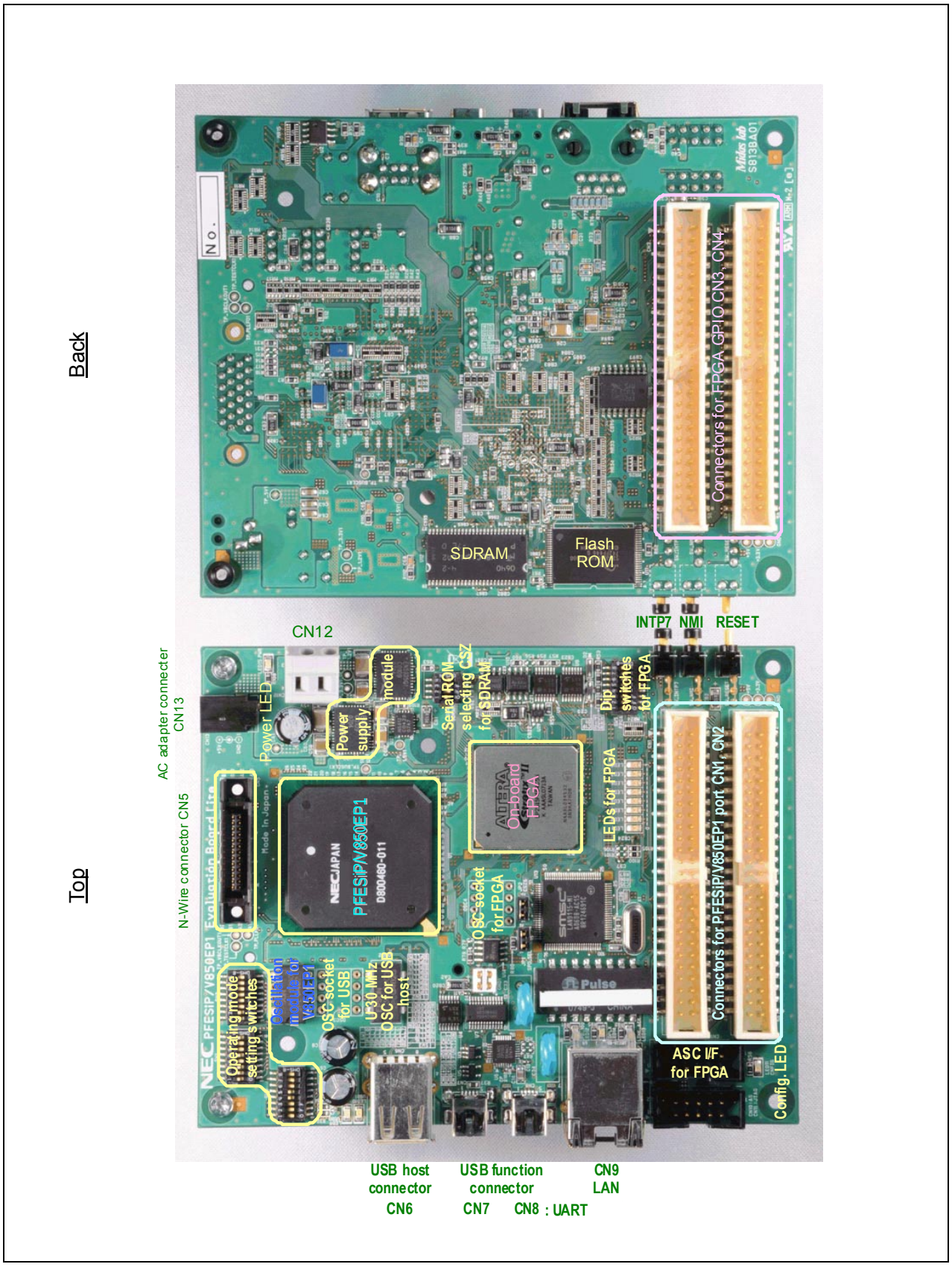
Remark Positions specified on-board in the following pages indicate coordinates on the following figure.

Figure 1-1. PFESiP EP-1 Evaluation Board Lite (Appearance)



1.1.3 PFESiP EP-1 Evaluation Board Lite (function of each part)

Figure 1-2. PFESiP EP-1 Evaluation Board Lite (Function of Each Part)



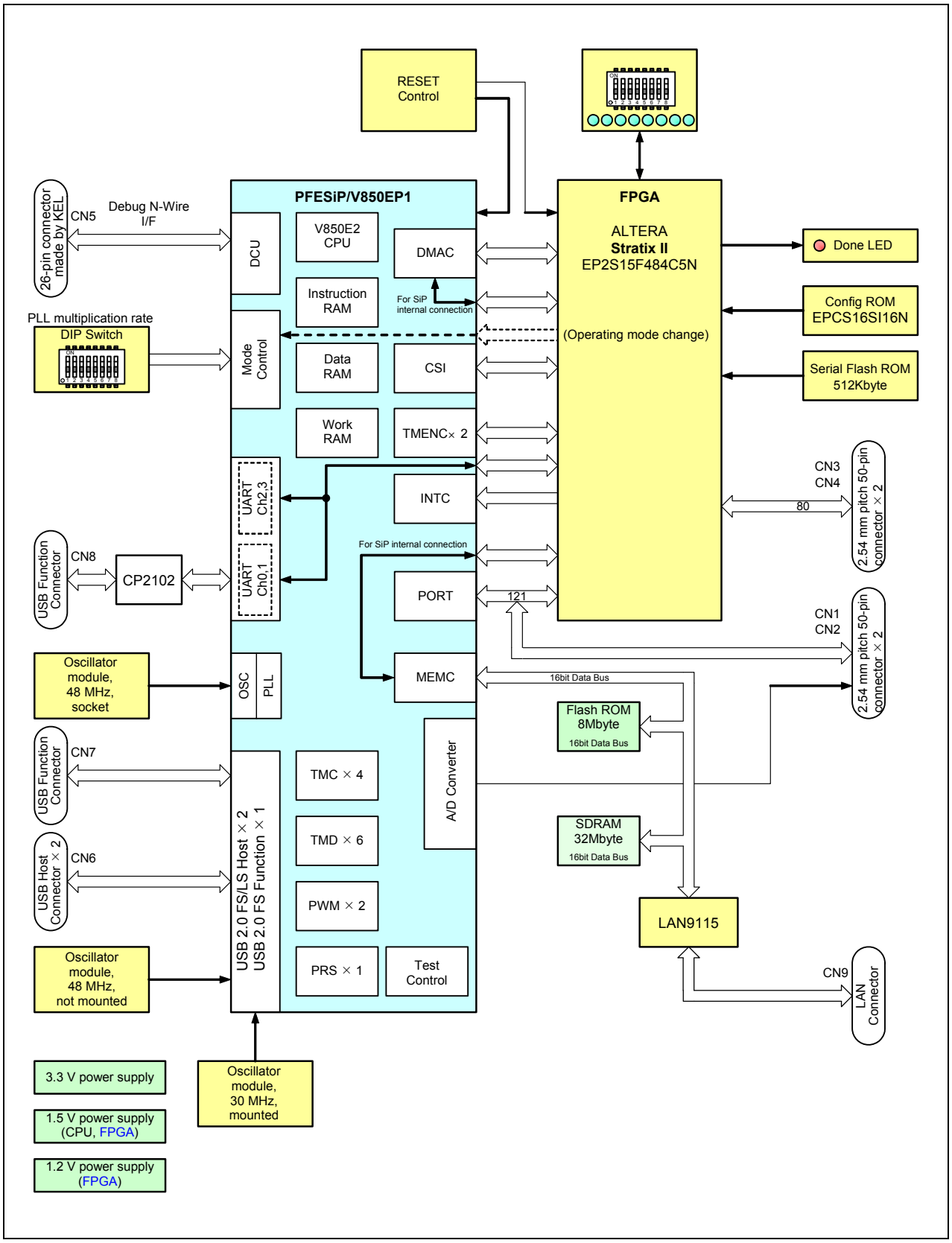
1.1.4 Specifications of PFESiP EP-1 Evaluation Board Lite

Table 1-1. Specifications of PFESiP EP-1 Evaluation Board Lite

Item	Specifications
Maximum operating frequency	
CPU operating frequency	200 MHz
Internal VSB bus frequency	100 MHz
External memory bus	66.7 MHz (C_L = 30 pF)
External memory wait setting	Condition: VBCLK = BUSCLK = 66.7 MHz PFESiP/V850EP1 output delay = 11.0 ns, maximum Wiring delay = 5 ns (to and fro) PFESiP/V850EP1 input delay = 3.8 ns, maximum
Flash ROM Spansion (S29JL064H70TFI000H)	Address setting wait = 0, idle state = 2, data wait = 5 Access time = 70 ns
SDRA MMT48LC16M16A2TG-7E	LTC = 0, C_L = 2, idle state = 0 ACTIVE Command to R/W Command = 1
On-board memory and FPGA	
Flash ROM	8 MB (fixed to CSZ0)
SDRAM	32 MB (selected from CSZ1, CSZ3, CSZ4, or CSZ6 by SW4)
FPGA	Altera Stratix II EP2S15F484C5N (Any CSZ selected within FPGA)
PFESiP/V850EP1 on-chip memory	
On-chip instruction RAM (ROM-less setting possible)	iLB_RAM: 192 KB
On-chip data RAM	dLB_RAM: 32 KB
On-chip work RAM (disable setting possible)	VSB_RAM: 32 KB
FPGA connection memory	
Serial flash ROM	512 KB (4 Mb)
Connector	
Expansion connectors	
General-purpose 50-pin connectors (CN1, CN2, CN3, CN4)	General-purpose 2.54 mm pitch (50 pins × 4)
N-Wire (CN5) tracing impossible	Default MINICUBE connector (26-pin connector made by KEL), RTE-NEC for RTE-2000-TP (Midas lab) supported
USB function connector (PFESiP/V850EP1 on-chip UART connection)	UART ↔ USB conversion performed using CP2102-GM
Active serial configuration interface for FPGA (CN10)	10 pins dedicated to ByteBlaster™ II/USB Blaster™ download cable, JTAG not mounted
PFESiP/V850EP1 on-chip USB 2.0 FS function	USB2.0 FS/LS Host × 2, USB2.0 FS Function
Operating conditions	
PFESiP/V850EP1 input frequency	Standard 48 MHz (mounted in socket)
Power supply	Supplied from CN13 by dedicated AC adapter (UL110-0520 made by UNIFIVE), 5 V supplied from power supply terminal (CN12)

1.1.5 Summarized block diagram of PFESiP EP-1 Evaluation Board Lite

Figure 1-3. Overall Block Diagram



1.1.6 Detailed block diagram of PFESiP EP-1 Evaluation Board Lite

Figure 1-4. Detailed Block Diagram of PFESiP EP-1 Evaluation Board Lite (1/2)

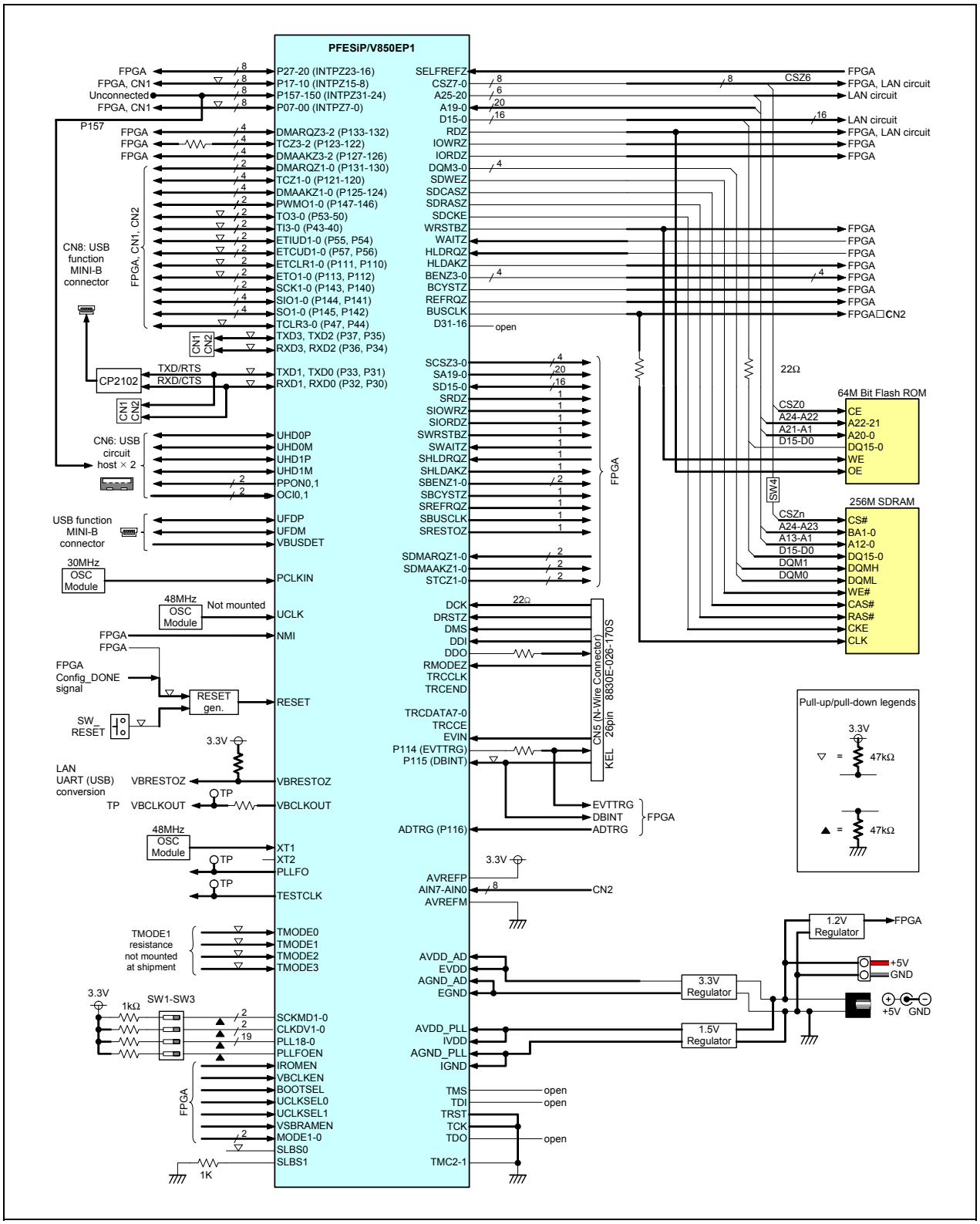
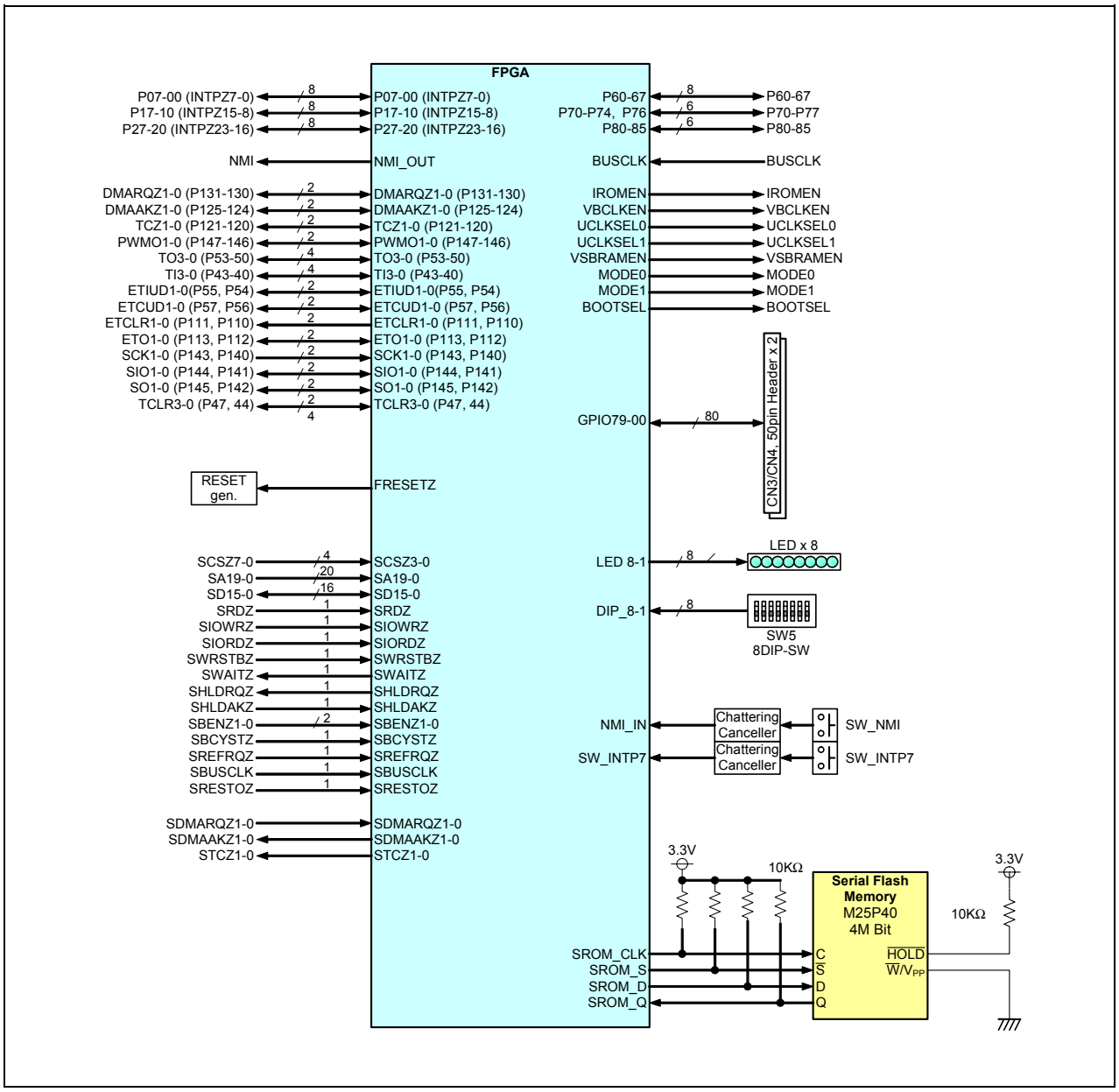


Figure 1-4. Detailed Block Diagram of PFESiP EP-1 Evaluation Board Lite (2/2)



1.1.7 Caution regarding maximum operating frequency of PFESiP/V850EP1

The maximum operating frequency of the PFESiP/V850EP1 differs depending on the operating conditions. CPCLK is an integer multiple of VBCLK and BUSCLK, and VBCLK is equal to or is an integer multiple of BUSCLK. Conditions half or less of those of CPCLK are applied to VBCLK. Consequently, the combinations of settings are restricted as follows.

Table 1-2. Maximum Operating Frequency of PFESiP/V850EP1 According to Operating Conditions

SDRAM, Low-Speed Mask ROM	Prioritized Clocks	Clocks		
		CPCLK	VBCLK	BUSCLK
None	CPCLK, VBCLK	200 MHz[Note]	100 MHz	100 MHz
Present	CPCLK, VBCLK	200 MHz	100 MHz	50 MHz[Note]
	BUSCLK	200 MHz	66.6 MHz	66.6 MHz[Note]

Note Clock that is the reference for determining the frequency.

Caution The design-guaranteed value of the maximum operating frequency cannot always be achieved, depending on the load of the FPGA.

1.2 Overview of PFESiP/V850EP1

The PFESiP/V850EP1 is a microcontroller function chip developed for the PFESiP EP-1 Series and uses a V850E2 CPU core.

The PFESiP/V850EP1 uses a high-speed process in which the CPU core operates at 200 MHz (maximum) and the internal bus at 100 MHz (maximum). This CPU core has an on-chip instruction cache and data cache. Furthermore, it has a DMA controller, an interrupt controller, general-purpose ports, a timer, a serial interface, an A/D converter, a memory controller, a host controller supporting USB 2.0 FS (full-speed) and LS (low-speed), a function controller supporting USB 2.0 FS (full-speed) as on-chip peripheral functions, and internal functions as a single-chip microcontroller.

A ROM/page ROM/SRAM or SDRAM can be connected as an external memory. Furthermore, the PFESiP/V850EP1 has an on-chip instruction RAM and data RAM, and can perform high-speed processing by executing an external program by transferring it to the instruction RAM.

In software application evaluation, debugging by the N-Wire in-circuit emulator and downloading of programs can be performed using the on-chip debug control unit (DCU).

1.2.1 Functions of PFESiP/V850EP1

(1/2)

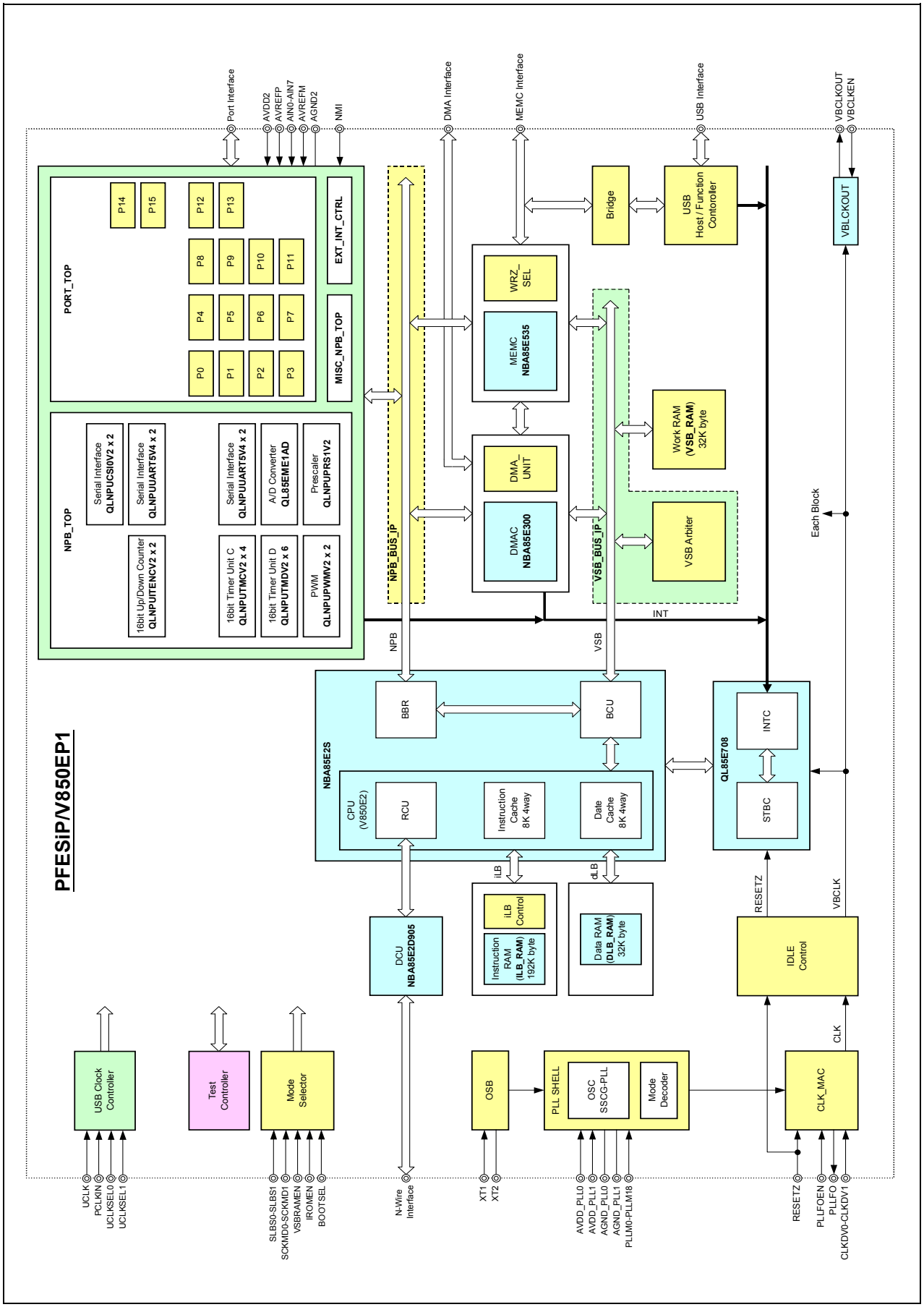
Item \ Product Name		PFESiP/V850EP1
CPU core		V850E2 CPU core
Minimum instruction execution time		5.0 ns (during 200 MHz operation)
General-purpose registers		32 bits × 32
Instruction set		V850E2 instruction set
Instruction cache		8 KB 4-way set associative instruction cache
Data cache		8 KB 4-way set associative data cache
Instruction RAM (iLB_RAM)	Can independently access each other	192 KB RAM structure (128-bit fetch bus)
Data RAM (dLB_RAM)		32 KB (CPCLK × 1-clock access)
Work RAM (VSB_RAM)		32 KB (VBCLK × 2-clock access)
DMA controller		4-channel DMA controller
Memory space, memory access function		• External 66.7 MHz interface • 512 MB linear address space • Memory area division function • Programmable chip select function: 8 • Programmable wait function • Idle state insertion function • Page ROM/ROM/SRAM/SDRAM interface • SDRAM support area: CSZ1, CSZ3, CSZ4, and CSZ6 areas
Interrupts/exceptions		• Non-maskable interrupt (NMI): 1 • Maskable interrupts User interrupts: 32 (external interrupts) Internal interrupts: 56 (NPB macro: 45, DMA: 4, USB: 7) • Priority level specifiable in 8 levels • Software exceptions: 32 sources • Exception trap: 1 source • Valid-edge select function • Variable digital noise filter function
SiP-dedicated interface functions		• SRAM interface Address space: 2 MB 4 dedicated chip select signals selected from CSZ1 to CSZ7 using registers 16-bit data bus Bus hold function supported • DMA interface Interface with 2 channels selected from 4 channels using registers • External interrupt function 8 interrupt signals assigned to SiP internal connections first
Standby function		IDLE/HALT mode (IDLE mode can be released by external interrupt and reset)

(2/2)

Item \ Product Name	PFESiP/V850EP1	
On-chip peripheral functions (NPB bus connection)		
I/O ports	CMOS I/Os: 121	
Timers	16-bit timer/event counter × 4 channels Interval timer × 6 channels Up/down counter/timer for 16-bit 2-phase encoder input × 2 channels	
PWM unit	8-/9-/10-/12-bit resolution PWM output × 2 channels	
Serial interfaces	Asynchronous serial interface × 4 channels Clocked serial interface × 2 channels	
USB host controller	USB 2.0 FS (full-speed), LS (low-speed) supported Internal 2-channel root-hub function 2-channel downstream port	Both host controller and function controller are placed at CSZ5. USB host controller uses external SDRAM.
USB function controller	1 channel supporting USB 2.0 FS (full-speed) Number of end points: 4 (control, bulk-in, bulk-out, interrupt)	
A/D converter	Internal 8-channel 10-bit 500 kHz A/D converter (NPB bus connection)	
On-chip debug functions	Incorporated in debug controller (DCU) • Run/break function, trace function, event function	
Clock line	External clock input multiplied by PLL and clock supplied (SSCG function provided) CPU: 200 MHz maximum, bus clock: 100 MHz maximum (CPCLK: VBCLK = 1/2, 1/3, 1/4) SDRAM interface: 66.7 MHz maximum (VBCLK: BUSCLK = 1/1, 1/2) Clock source and PLL setting switch pin provided (not switchable during operation)	
Power supply	For pin power supply: EV_{DD} = 3.3 ±0.3 V For internal power supply: IV_{DD} = 1.5 ±0.15 V	
Series	CB-12M type	

Remark The PFESiP EP-1 Evaluation Board Lite does not support the trace function.

1.2.2 Internal block diagram of PFESiP/V850EP1



1.2.3 PFESiP/V850EP1 pins usable on this board

(1/7)

Usable PFESiP/V850EP1 Pins				Connected to 50-Pin Connector		Connected to FPGA	On-Board Peripheral-Circuit Connection and Pin Processing
Port	Function Pin 1	Function Pin 2	SiP Internal Connection	CN1	CN2	FPGA Pin Name	
P00	INTPZ0	CCC00	–	2	–	INTPZ0/CCC00	50 kΩ Pull-up
P01	INTPZ1	CCC01	–	3	–	INTPZ1/CCC01	50 kΩ Pull-up
P02	INTPZ2	CCC10	–	4	–	INTPZ2/CCC10	50 kΩ Pull-up
P03	INTPZ3	CCC11	–	5	–	INTPZ3/CCC11	50 kΩ Pull-up
P04	INTPZ4	CCC20	–	7	–	INTPZ4/CCC20	50 kΩ Pull-up
P05	INTPZ5	CCC21	–	8	–	INTPZ5/CCC21	50 kΩ Pull-up
P06	INTPZ6	CCC30	–	9	–	INTPZ6/CCC30	50 kΩ Pull-up
P07	INTPZ7	CCC31	–	10	–	INTPZ7/CCC31	50 kΩ Pull-up
P10	INTPZ8	CC00	–	12	–	INTPZ8/CC00	50 kΩ Pull-up
P11	INTPZ9	CC01	–	13	–	INTPZ9/CC01	50 kΩ Pull-up
P12	INTPZ10	CC10	–	14	–	INTPZ10/CC10	50 kΩ Pull-up
P13	INTPZ11	CC11	–	15	–	INTPZ11/CC11	50 kΩ Pull-up
P14	INTPZ12	–	–	17	–	INTPZ12	50 kΩ Pull-up
P15	INTPZ13	–	–	18	–	INTPZ13	50 kΩ Pull-up
P16	INTPZ14	–	–	19	–	INTPZ14	50 kΩ Pull-up
P17	INTPZ15	–	–	20	–	INTPZ15	LAN circuit, 1 kΩ pull-up
P20	INTPZ16	–	√	–	–	P20/INTPZ16	
P21	INTPZ17	–	√	–	–	P21/INTPZ17	
P22	INTPZ18	–	√	–	–	P22/INTPZ18	
P23	INTPZ19	–	√	–	–	P23/INTPZ19	
P24	INTPZ20	–	√	–	–	P24/INTPZ20	
P25	INTPZ21	–	√	–	–	P25/INTPZ21	
P26	INTPZ22	–	√	–	–	P26/INTPZ22	
P27	INTPZ23	–	√	–	–	P27/INTPZ23	
P30	RXD0	–	–	22	–	–	USB conversion circuit, 50 kΩ pull-up
P31	TXD0	–	–	23	–	–	USB conversion circuit, 50 kΩ pull-up
P32	RXD1	–	–	24	–	–	50 kΩ pull-up, USB circuit
P33	TXD1	–	–	25	–	–	50 kΩ pull-up, USB circuit
P34	RXD2	–	–	27	–	–	50 kΩ Pull-up
P35	TXD2	–	–	28	–	–	50 kΩ Pull-up
P36	RXD3	–	–	29	–	–	50 kΩ Pull-up
P37	TXD3	–	–	30	–	–	50 kΩ Pull-up
P40	TI0	–	–	32	–	TI0	50 kΩ Pull-up
P41	TI1	–	–	33	–	TI1	50 kΩ Pull-up
P42	TI2	–	–	34	–	TI2	50 kΩ Pull-up
P43	TI3	–	–	35	–	TI3	50 kΩ Pull-up
P44	TCLR0	–	–	37	–	TCLR0	50 kΩ Pull-up
P45	TCLR1	–	-	38	-	TCLR1	50 kΩ Pull-up
P46	TCLR2	–	-	39	-	TCLR2	50 kΩ Pull-up
P47	TCLR3	–	-	40	-	TCLR3	50 kΩ Pull-up

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Usable PFESiP/V850EP1 Pins				Connected to 50-Pin Connector		Connected to FPGA	On-Board Peripheral-Circuit Connection and Pin Processing
Port	Function Pin 1	Function Pin 2	SiP Internal Connection	CN1	CN2	FPGA Pin Name	
P50	TO0	–	–	42	–	TO0	50 kΩ Pull-up
P51	TO1	–	–	43	–	TO1	50 kΩ Pull-up
P52	TO2	–	–	44	–	TO2	50 kΩ Pull-up
P53	TO3	–	–	45	–	TO3	50 kΩ Pull-up
P54	ETIUD0	–	–	47	–	ETIUD0	50 kΩ Pull-up
P55	ETIUD1	–	–	48	–	ETIUD1	50 kΩ Pull-up
P56	ETCUD0	–	–	49	–	ETCUD0	50 kΩ Pull-up
P57	ETCUD1	–	–	50	–	ETCUD1	50 kΩ Pull-up
P60	A20	–	–	–	3	P60/A20	Flash ROM
P61	A21	–	–	–	4	P61/A21	Flash ROM
P62	A22	–	–	–	5	P62/A22	Flash ROM
P63	A23	–	–	–	7	P63/A23	SDRAM, flash ROM
P64	A24	–	–	–	8	P64/A24	SDRAM
P65	A25	–	–	–	9	P65/A25	
P66	A0	–	–	–	10	P66/A0	
P67	A1	–	–	–	12	P67/A1	LAN circuit, SDRAM, flash ROM
–	A2	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A3	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A4	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A5	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A6	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A7	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A8	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A9	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A10	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A11	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A12	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A13	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	A14	–	–	–	–	–	LAN circuit, flash ROM
–	A15	–	–	–	–	–	LAN circuit, flash ROM
–	A16	–	–	–	–	–	Flash ROM
–	A17	–	–	–	–	–	Flash ROM
–	A18	–	–	–	–	–	Flash ROM
–	A19	–	–	–	–	–	Flash ROM
P70	WAITZ	–	–	–	–	P70/WAITZ	
–	CSZ0	–	–	–	–	–	Flash ROM
P71	CSZ1	–	–	–	–	P71/CSZ1	SW4 (SDRAM)
P72	CSZ2	–	–	–	–	P72/CSZ2	
P73	CSZ3	–	–	–	–	P73/CSZ3	SW4 (SDRAM)
P74	CSZ4	–	–	–	–	P74/CSZ4	SW4 (SDRAM)
P76	CSZ6	–	–	–	–	P76/CSZ6	LAN circuit (can be opened with JP2), SW4 (SDRAM)

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Usable PFESiP/V850EP1 Pins				Connected to 50-Pin Connector		Connected to FPGA	On-Board Peripheral-Circuit Connection and Pin Processing
Port	Function Pin 1	Function Pin 2	SiP Internal Connection	CN1	CN2	FPGA Pin Name	
–	RDZ	–	–	–	–	–	LAN circuit, flash ROM
–	WRZ0	BENZ0	–	–	–	–	LAN circuit
–	WRZ1	BENZ1	–	–	–	–	LAN circuit
–	WRSTBZ	–	–	–	–	–	Flash ROM
–	BCYSTZ	–	–	–	–	–	
–	BUSCLK	–	–	–	2	BUSCLK	Test pin, SDRAM
–	DQM0	–	–	–	–	–	SDRAM
–	DQM1	–	–	–	–	–	SDRAM
–	SDWEZ	–	–	–	–	–	SDRAM
–	SDCASZ	–	–	–	–	–	SDRAM
–	SDRASZ	–	–	–	–	–	SDRAM
–	SDCKE	–	–	–	–	–	SDRAM
P80	IOWRZ	–	–	–	–	P80/IOWRZ	
P81	IORDZ	–	–	–	–	P81/IORDZ	
P82	HLDAKZ	–	–	–	–	P82/HLDAKZ	
P83	HLDRQZ	–	–	–	–	P83/HLDRQZ	
P84	REFRQZ	–	–	–	–	P84/REFRQZ	
P85	SELFREFZ	–	–	–	–	P85/SELFREFZ	
–	D0	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D1	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D2	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D3	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D4	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D5	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D6	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D7	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D8	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D9	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D10	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D11	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D12	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D13	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D14	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	D15	–	–	–	–	–	LAN circuit, SDRAM, flash ROM
–	DDI	–	–	–	–	–	N-Wire (CN5)
–	DCK	–	–	–	–	–	N-Wire (CN5)
–	DMS	–	–	–	–	–	N-Wire (CN5)
–	DDO	–	–	–	–	–	N-Wire (CN5)
–	DRSTZ	–	–	–	–	–	N-Wire (CN5)
–	RMODEZ	–	–	–	–	–	N-Wire (CN5)
–	RESETZ	–	–	–	–	–	Input from reset circuit

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Usable PFESiP/V850EP1 Pins				Connected to 50-Pin Connector		Connected to FPGA	On-Board Peripheral-Circuit Connection and Pin Processing
Port	Function Pin 1	Function Pin 2	SiP Internal Connection	CN1	CN2	FPGA Pin Name	
–	XT1	–	–	–	–	–	Mounted in socket
–	VBCLKOUT	–	–	–	–	–	Test pin
–	PLLFO	–	–	–	–	–	Test pin
–	AVDD_PLL0	–	–	–	–	–	Filter division: 1.5 V
–	AVDD_PLL1	–	–	–	–	–	Filter division: 1.5 V
–	AGND_PLL0	–	–	–	–	–	Filter division: GND
–	AGND_PLL1	–	–	–	–	–	Filter division: GND
–	EVDD	–	–	–	–	–	3.3 V
–	IVDD	–	–	–	–	–	1.5 V
–	EGND	–	–	–	–	–	GND
–	IGND	–	–	–	–	–	GND
P110	ETCLR0	–	–	–	13	P110/ETCLR0	50 kΩ Pull-up
P111	ETCLR1	–	–	–	14	P111/ETCLR1	50 kΩ Pull-up
P112	ETO0	–	–	–	15	P112/ETO0	50 kΩ Pull-up
P113	ETO1	–	–	–	17	P113/ETO1	50 kΩ Pull-up
P120	TCZ0	–	–	–	18	P120/TCZ0	
P121	TCZ1	–	–	–	19	P121/TCZ1	
P124	DMAAKZ0	–	–	–	20	P124/DMAAKZ0	
P125	DMAAKZ1	–	–	–	21	P125/DMAAKZ1	
P130	DMARQZ0	–	–	–	23	P130/DMARQZ0	
P131	DMARQZ1	–	–	–	24	P131/DMARQZ1	
P140	SCK0	–	–	–	25	P140/SCK0	
P141	SI0	–	–	–	27	P141/SI0	
P142	SO0	–	–	–	28	P142/SO0	
P143	SCK1	–	–	–	29	P143/SCK1	
P144	SI1	–	–	–	30	P144/SI1	
P145	SO1	–	–	–	32	P145/SO1	
P146	PWMO0	–	–	–	33	P146/PWMO0	
P147	PWMO1	–	–	–	34	P147/PWMO1	
–	NMI	–	–	–	–	NMI_OUT	
–	SDMARQZ0	–	√	–	–	SDMARQZ0	
–	SDMARQZ1	–	√	–	–	SDMARQZ1	
–	SDMAAKZ0	–	√	–	–	SDMAAKZ0	
–	SDMAAKZ1	–	√	–	–	SDMAAKZ1	
–	STCZ0	–	√	–	–	STCZ0	
–	STCZ1	–	√	–	–	STCZ1	
–	SCSZ0	–	√	–	–	SCSZ0	
–	SCSZ1	–	√	–	–	SCSZ1	
–	SCSZ2	–	√	–	–	SCSZ2	
–	SCSZ3	–	√	–	–	SCSZ3	
–	SA0	–	√	–	–	SA0	
–	SA1	–	√	–	–	SA1	

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Usable PFESiP/V850EP1 Pins				Connected to 50-Pin Connector		Connected to FPGA	On-Board Peripheral-Circuit Connection and Pin Processing
Port	Function Pin 1	Function Pin 2	SiP Internal Connection	CN1	CN2	FPGA Pin Name	
–	SA2	–	√	–	–	SA2	
–	SA3	–	√	–	–	SA3	
–	SA4	–	√	–	–	SA4	
–	SA5	–	√	–	–	SA5	
–	SA6	–	√	–	–	SA6	
–	SA7	–	√	–	–	SA7	
–	SA8	–	√	–	–	SA8	
–	SA9	–	√	–	–	SA9	
–	SA10	–	√	–	–	SA10	
–	SA11	–	√	–	–	SA11	
–	SA12	–	√	–	–	SA12	
–	SA13	–	√	–	–	SA13	
–	SA14	–	√	–	–	SA14	
–	SA15	–	√	–	–	SA15	
–	SA16	–	√	–	–	SA16	
–	SA17	–	√	–	–	SA17	
–	SA18	–	√	–	–	SA18	
–	SA19	–	√	–	–	SA19	
–	SA20	–	√	–	–	SA20	
–	SD0	–	√	–	–	SD0	
–	SD1	–	√	–	–	SD1	
–	SD2	–	√	–	–	SD2	
–	SD3	–	√	–	–	SD3	
–	SD4	–	√	–	–	SD4	
–	SD5	–	√	–	–	SD5	
–	SD6	–	√	–	–	SD6	
–	SD7	–	√	–	–	SD7	
–	SD8	–	√	–	–	SD8	
–	SD9	–	√	–	–	SD9	
–	SD10	–	√	–	–	SD10	
–	SD11	–	√	–	–	SD11	
–	SD12	–	√	–	–	SD12	
–	SD13	–	√	–	–	SD13	
–	SD14	–	√	–	–	SD14	
–	SD15	–	√	–	–	SD15	
–	SRDZ	–	√	–	–	SRDZ	
–	SWRZ0	SBENZ0	√	–	–	SWRZ0/SBENZ0	
–	SWRZ1	SBENZ1	√	–	–	SWRZ1/SBENZ1	
–	SIOWRZ	–	√	–	–	SIOWRZ	
–	SIORDZ	–	√	–	–	SIORDZ	
–	SWRSTBZ	–	√	–	–	SWRSTBZ	

(6/7)

Usable PFESiP/V850EP1 Pins				Connected to 50-Pin Connector		Connected to FPGA	On-Board Peripheral-Circuit Connection and Pin Processing
Port	Function Pin 1	Function Pin 2	SiP Internal Connection	CN1	CN2	FPGA Pin Name	
–	SWAITZ	–	√	–	–	SWAITZ	
–	SHLDRQZ	–	√	–	–	SHLDRQZ	
–	SHLDAKZ	–	√	–	–	SHLDAKZ	
–	SBCYSTZ	–	√	–	–	SBCYSTZ	
–	SBUSCLK	–	√	–	–	SBUSCLK	
–	SREFRQZ	–	√	–	–	SREFRQZ	
–	SRESTOZ	–	√	–	–	SRESTOZ	
–	UCLK	–	–	–	–	–	Socket only (no parts mounted)
–	UHD0P	–	–	–	–	–	USB circuit
–	UHD0M	–	–	–	–	–	USB circuit
–	UHD1P	–	–	–	–	–	USB circuit
–	UHD1M	–	–	–	–	–	USB circuit
–	PPON0	–	–	–	–	–	USB circuit
–	PPON1	–	–	–	–	–	USB circuit
–	OCI0	–	–	–	–	–	USB circuit
–	OCI1	–	–	–	–	–	USB circuit
–	UFDP	–	–	–	–	–	USB circuit
–	UFDM	–	–	–	–	–	USB circuit
–	VBUSDET	–	–	–	–	–	USB circuit
–	PCLKIN	–	–	–	–	–	Fixed to 30 MHz
–	UCLKSEL0	–	–	–	–	UCLKSEL0	1 kΩ pull-down mounted (XT1 selection)
–	UCLKSEL1	–	–	–	–	UCLKSEL1	Resistance not mounted (PCLKIN selection)
–	AIN0	–	×Note	–	35	–	
–	AIN1	–	×Note	–	37	–	
–	AIN2	–	×Note	–	39	–	
–	AIN3	–	×Note	–	41	–	
–	AIN4	–	×Note	–	43	–	
–	AIN5	–	×Note	–	45	–	
–	AIN6	–	×Note	–	47	–	
–	AIN7	–	×Note	–	49	–	
–	TMODE0	–	–	–	–	–	1 kΩ Pull-up
–	TMODE1	–	–	–	–	–	1 kΩ pull-up (pattern only)
–	TMODE2	–	–	–	–	–	1 kΩ Pull-up
–	TMODE3	–	–	–	–	–	1 kΩ Pull-up
–	TESTCLK	–	–	–	–	–	Test pin
–	TMC1	–	–	–	–	–	GND
–	TMC2	–	–	–	–	–	GND
–	TMS	–	–	–	–	–	OPEN
–	TDI	–	–	–	–	–	OPEN
–	TRST	–	–	–	–	–	GND

Note The standard package does not support analog input of the A/D converter.

(7/7)

Usable PFESiP/V850EP1 Pins				Connected to 50-Pin Connector		Connected to FPGA	On-Board Peripheral-Circuit Connection and Pin Processing	
Port	Function Pin 1	Function Pin 2	SiP Internal Connection	CN1	CN2	FPGA Pin Name		
–	TCK	–	–	–	–	–	GND	
–	TDO	–	–	–	–	–	OPEN	
–	IROMEN	–	–	–	–	IROMEN		
–	SLBS0	–	√	–	–	–	Fixed to 16-bit bus	4.7 kΩ Pull-up
–	SLBS1	–	√	–	–	–		4.7 kΩ Pull-down
–	VBCLKEN	–	√	–	–	VBCLKEN	50 kΩ Pull-down	
–	SCKMD0	–	√	–	–	–	Mode setting (SW3)	
–	SCKMD1	–	√	–	–	–	Mode setting (SW3)	
–	VSBRAMEN	–	√	–	–	VSBRAMEN	50 kΩ Pull-up	
–	CLKDV0	–	√	–	–	–	Mode setting (SW3)	
–	CLKDV1	–	√	–	–	–	Mode setting (SW3)	
–	BOOTSEL	–	√	–	–	BOOTSEL	50 kΩ Pull-up	
–	MODE0	–	√	–	–	MODE0	50 kΩ Pull-up	
–	MODE1	–	√	–	–	MODE1	50 kΩ Pull-up	
–	PLL0	–	√	–	–	–	Mode setting (SW1)	
–	PLL1	–	√	–	–	–	Mode setting (SW1)	
–	PLL2	–	√	–	–	–	Mode setting (SW1)	
–	PLL3	–	√	–	–	–	Mode setting (SW1)	
–	PLL4	–	√	–	–	–	Mode setting (SW1)	
–	PLL5	–	√	–	–	–	Mode setting (SW1)	
–	PLL6	–	√	–	–	–	Mode setting (SW1)	
–	PLL7	–	√	–	–	–	Mode setting (SW1)	
–	PLL8	–	√	–	–	–	Mode setting (SW2)	
–	PLL9	–	√	–	–	–	Mode setting (SW2)	
–	PLL10	–	√	–	–	–	Mode setting (SW2)	
–	PLL11	–	√	–	–	–	Mode setting (SW2)	
–	PLL12	–	√	–	–	–	Mode setting (SW2)	
–	PLL13	–	√	–	–	–	Mode setting (SW2)	
–	PLL14	–	√	–	–	–	Mode setting (SW2)	
–	PLL15	–	√	–	–	–	Mode setting (SW2)	
–	PLL16	–	√	–	–	–	Mode setting (SW3)	
–	PLL17	–	√	–	–	–	Mode setting (SW3)	
–	PLL18	–	√	–	–	–	Mode setting (SW3)	
–	PLLFOEN	–	–	–	–	–	Mode setting (SW3)	

CHAPTER 2 HARDWARE INSTALLATION

2.1 Preface

2.1.1 Operating mode setting

To use the PFESiP EP-1 Evaluation Board Lite for various purposes, it requires dip switch settings for the PFESiP/V850EP1. The operating mode setting pins that are usually not required to be changed can be changed from the FPGA.

(1) Item to be set using dip switches

Dip switches are provided to set the clock operating mode of the PFESiP/V850EP1.
Set the clock operating mode according to CHAPTER 3 SWITCH SETTINGS before connecting the power supply.

(2) Items to be set from FPGA

The settings of the operating mode setting pins that are usually not required to be changed in normal use can be changed from the FPGA as required. The settings listed in Table 2-1 are those when the pins are set to high impedance without defining them from the FPGA.

Table 2-1. Operating Mode Setting Pins Set from FPGA

Pin Name	State When Floating	
	Setting Value	Setting
UCLKSEL0	0	XT1 select
UCLKSEL1	1	PCLKIN select
IROMEN	0	Invalid
VBCLKEN	0	Output disabled
VSBRAMEN	1	VSBRAM enabled
BOOTSEL	1	External MEMC
MODE0	1	USB function enabled
MODE1	1	USB host enabled

2.1.2 Mounting oscillation module

(1) OSC1 (for PFESiP/V850EP1)

Position	Figure 1-1 (Appearance) B-2

A 3.3 V, 48 MHz oscillation module is provided as the standard oscillation module.
The oscillation module can be changed to other oscillation modules operating at 3.3 V due to the IC socket structure.
The maximum input frequency is 50 MHz.

(2) OSC3 (for UCLK)

Position	Figure 1-1 (Appearance) B-2

No standard oscillation module is provided.
OSC1 is selected by the default setting.
An oscillation module operating at 3.3 V can be mounted on the socket due to the IC socket structure.

(3) OSC4 (for FPGA)

Position	Figure 1-1 (Appearance) C-3

OSC4 can be used as the clock for the on-board large-capacity FPGA.
It is connected to EX_CLK of the FPGA.
An oscillation module operating at 3.3 V can be mounted on the socket due to the IC socket structure.

Caution PCLKIN (30 MHz) to be used with the USB is each provided as OSC2. It does not use a socket.

2.2 Connecting Power Supply

The PFESiP EP-1 Evaluation Board Lite can use the AC adapter or power supply terminal.

Normally, it uses only a single +5.0 V power supply. Correctly connect a power supply according to the operating environment.

2.2.1 AC adapter (CN13)

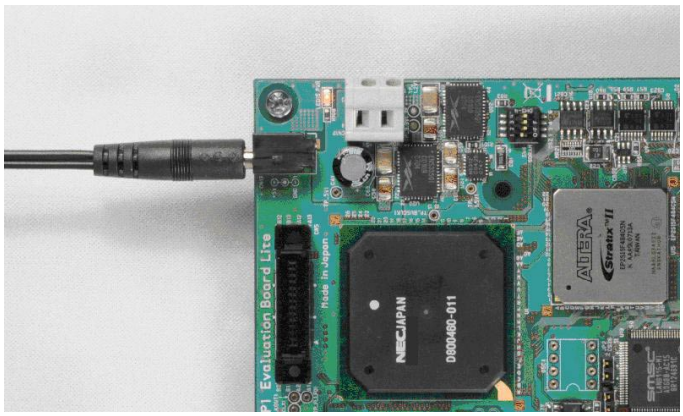
Position **Figure 1-1 (Appearance) D-1**

Connect the +5.0 V power supply jack of the AC adapter included as a standard attachment to connector CN13.

The AC adapter specifications are 5 V and a 2 A positive center pin, and the DC jack complies with the EIJ-2 standard.

The AC adapter dedicated to the PFESiP EP-1 Evaluation Board cannot be used.

The 3.3 V, 1.5 V, and 1.2 V power supplies required on-board are generated by the on-board power supply module.



Cautions 1. This cannot be used together with CN12.

2. Set the on-board operating mode setting switches before connecting the power supply.

2.2.2 5.0 V power supply terminal (CN12)

Position **Figure 1-1 (Appearance) E-2**

The 5.0 V power supply terminal is connected using +5.0 V from the external power supply via a wire. Insert a small slotted screwdriver into the hole, to the center of the substrate, and insert the wire from the outer side of the substrate. The wire will be fixed when the slotted screwdriver is removed.

The 3.3 V, 1.5 V, and 1.2 V power supplies required on-board are generated by the on-board power supply module.

Cautions 1. This cannot be used together with CN13.

2. Set the on-board operating mode setting switches before connecting the power supply.

CHAPTER 3 SWITCH SETTINGS

3.1 Operating Mode Setting Dip Switches

Positions **Figure 1-1 (Appearance) A-1, B-1, A-2**

SW1 and SW2 are dip switches used to set the operating mode.

SW1 and SW2 are used to set the oh-chip CPU core and memory controller operating modes of the PFESiP/V850EP1.

With each operating mode setting signal, if it is set from the FPGA, the pin will be set to high level with high-level output and to low level with low-level output.

A pin to be set using a switch is set to low level when the switch is turned off and to high level when the switch is turned on.

Table 3-1. Operating Mode Settings

DIPSW FPGA	Mode Setting Signal	When Turned off (0)	When Turned on (1)
Fixed	SLBS0	Bus width setting during startup is fixed to 16 bits on-board. SLBS <1:0> = 01:16 bits	
Fixed	SLBS1		
SW1	PLL7-0	M = 24, n = 100, p = 1 is the default setting. (CPCLK200MHz, VBCLK100MHz, BUSCLK50MHz)	
SW2	PLL15-8		
SW3[3:1]	PLL18-16		
SW3-4	PLLFOEN	PLLFO pin outputs low level	PLLFO pin outputs PLLFO
SW3-5	CLKDV0	Setting of VBCLK division ratio to CPCLK CLKDV[1:0] = 00: Setting prohibited, 01:CPCLK/2, 10:CPCLK/3, 11:CPCLK/4	
SW3-6	CLKDV1		
SW3-7	SCKMD0	Setting of BUSCLK division ratio to VBCLK	
		VBCLK/1	VBCLK/2
SW3-8	SCKMD1	Normal state	Setting prohibited
FPGA	IROMEN	Normal state	
FPGA	VBCLKEN	VBCLKOUT output disabled (low-level output)	VBCLKOUT output enabled
FPGA	UCLKSEL0	XT1 or XT2 selected as USB clock	UCLK selected as USB clock
FPGA	UCLKSEL1	XT1 or XT2 selected as USB bridge clock	PCLKIN selected as USB bridge clock
FPGA	VSBRAMEN	Work RAM (VSB_RAM) disabled	Work RAM (VSB_RAM) enabled
FPGA	MODE0	USB function disabled	USB function enabled
FPGA	MODE1	USB host function disabled	USB host function enabled
FPGA	BOOTSEL	Booted from SCSZ0 (SiP interior)	Booted from CSZ0 (external bus)

Remark Setting the operating mode from the FPGA is usually not required.

3.1.1 Setting operating mode using dip switches (SW3-4 to SW3-8)

(1) PLLFOEN (PLLFO output enable)… SW3-4

The FO output of the internal PLL can be output from the PLLFO pin. The FO output is also not stopped in IDLE mode.

FO is output to PLLFO only if high level is input to PLLFOEN. If low level is input, the device ID is output.

This output control is an enable control structure. Whiskers may occur when the pin settings are switched during an operation.

SW3-4	PLLFOEN	PLLFO Output Control
OFF	0	Low-level output
ON	1	Enables output

(2) CLKDV0, CLKDV1 (VBCLK divide control)… SW3-5, SW3-6

These are the inputs that set the VBCLK division ratio to CPCLK.

The mode in which CPCLK = VBCLK is not supported.

Do not set both SW3-5 and SW3-6 to be off at the same time.

SW3-6	SW3-5	CLKDV1	CLKDV0	VBCLK Selection
OFF	OFF	0	0	Setting prohibited
OFF	ON	0	1	CPCLK/2
ON	OFF	1	0	CPCLK/3
ON	ON	1	1	CPCLK/4

(3) SCKMD0, SCKMD1 (BUSCLK divide control) … SW3-7, SW3-8

These set the division ratio of the external bus clock (BUSCLK) to the internal system clock (VBCLK).

The maximum operating frequency of VBCLK is 100 MHz. On the other hand, the maximum operating frequency of the external bus interface is 66.7 MHz, so when using VBCLK at its maximum operating frequency, VBCLK/2 is recommended for BUSCLK.

SW3-8	SW3-7	SCKMD1	SCKMD0	BUSCLK Selection
OFF	OFF	0	0	VBCLK/1
OFF	ON	0	1	VBCLK/2
ON	OFF	1	0	Setting prohibited
ON	ON	1	1	

3.1.2 SSCG-PLL operating mode setting dip switches

Functions are assigned to the SSCG-PLL setting pins as follows.

DPSW	Pin Name	PFESiP/V850EP1 Internal Signal	Function
SW1-1	PLL0	PLLM0	M counter input 0
SW1-2	PLL1	PLLM1	M counter input 1
SW1-3	PLL2	PLLM2	M counter input 2
SW1-4	PLL3	PLLM3	M counter input 3
SW1-5	PLL4	PLLM4	M counter input 4
SW1-6	PLL5	PLLM5	M counter input 5
SW1-7	PLL6	PLLM6	M counter input 6
SW1-8	PLL7	PLLN0	M counter input 0
SW2-1	PLL8	PLLN1	N counter input 1
SW2-2	PLL9	PLLN2	N counter input 2
SW2-3	PLL10	PLLP0	P counter input 0
SW2-4	PLL11	PLLP1	P counter input 1
SW2-5	PLL12	SSMDL0	SSCG setting input
SW2-6	PLL13	SSMDL1	SSCG setting input
SW2-7	PLL14	SSADJ0	SSCG setting input
SW2-8	PLL15	SSADJ1	SSCG setting input
SW3-1	PLL16	SSADJ2	SSCG setting input
SW3-2	PLL17	PLLS0	SSCG setting input
SW3-3	PLL18	PLLS1	SSCG setting input

<table>
<tr><th>Pin Name</th><th>Internal Signal</th><th>Function</th></tr>
<tr><td>PLL0 to PLL6
PLL7 to PLL9
PLL10 to PLL11</td><td>PLLM0 to PLLM6
PLLN0 to PLLN2
PLLP0 to PLLP1</td><td>Input setting internal PLL multiplication rate
m = Setting values of PLLM0 to PLLM6 (0 to 127) + 1: 2 to 128
n = Setting values of PLLN0 to PLLN2 (0 to 7) + 92 + 1: 93 to 100
p = Setting value of $2^{PLLP0 - PLLP1}$: 1, 2, 4
Multiplication rate = n/m/p
<table>
<tr><th>Item</th><th>Symbol</th><th>Expression</th><th>MIN.</th><th>MAX</th><th>Unit</th></tr>
<tr><td>Input frequency</td><td>fstd</td><td>–</td><td>2.0</td><td>50.0</td><td>MHz</td></tr>
<tr><td>PFD input frequency</td><td>fpfd</td><td>fpfd = fstd/m</td><td>1.0</td><td>2.1</td><td>MHz</td></tr>
<tr><td>VCO output frequency</td><td>fvco</td><td>fvco = fstd×n/m</td><td>100</td><td>200</td><td>MHz</td></tr>
<tr><td>Output frequency</td><td>fout</td><td>Fout = fstd×n/m/p</td><td>25</td><td>200</td><td>MHz</td></tr>
<tr><td>Input duty</td><td>Iduty</td><td>–</td><td>30</td><td>70</td><td>%</td></tr>
<tr><td>Multiplication rate</td><td>MULT</td><td>MULT = n/m/p</td><td>0.182</td><td>50</td><td>-</td></tr>
</table>
PLL will be set to through mode both when PLLM0 to PLLM6 are all low level and PLLP0 and PLLP1 are all high level.</td></tr>
<tr><td>PLL12 to PLL13</td><td>SSMDL0 to SSMDL1</td><td>Inputs setting SSCG modulation range
<table>
<tr><th>SSMDL1</th><th>SSMDL0</th><th>Modulation cycle [kHz]</th></tr>
<tr><td>0</td><td>0</td><td>15.00-26.25</td></tr>
<tr><td>0</td><td>1</td><td>25.00-36.75</td></tr>
<tr><td>1</td><td>0</td><td>35.00-48.30</td></tr>
<tr><td>1</td><td>1</td><td>45.00-68.25</td></tr>
</table></td></tr>
<tr><td>PLL14 to PLL16</td><td>SSADJ0 to SSADJ2</td><td>Inputs setting SSCG frequency diffusion mode and that range
<table>
<tr><th>SSADJ2</th><th>SSADJ1</th><th>SSADJ0</th><th>Frequency modulation rate</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>About –0.5%</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>About –1.0%</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>About –2.0%</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>About –3.0%</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>About –4.0%</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>About –5.0%</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>No modulation</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No modulation</td></tr>
</table></td></tr>
<tr><td>PLL17 to PLL18</td><td>PLLS0 to PLLS1</td><td>S selector inputs of SSCG
<table>
<tr><th>PLLS1</th><th>PLLS0</th><th>PFD input frequency [MHz]</th></tr>
<tr><td>0</td><td>0</td><td>1.00 ≤fpfd<1.20</td></tr>
<tr><td>0</td><td>1</td><td>1.20≤fpfd<1.45</td></tr>
<tr><td>1</td><td>0</td><td>1.45≤fpfd<1.70</td></tr>
<tr><td>1</td><td>1</td><td>1.70≤fpfd≤2.10</td></tr>
</table></td></tr>
</table>

3.1.3 Setting operating mode from FPGA

Setting the operating mode from the FPGA is not required in general use.

The settings of the operating mode setting pins that are usually not required to be changed can be changed from the FPGA as required.

(1) VBCLKEN (VBCLK output enable)… FPGA

The internal system clock (VBCLK) can be output from the VBCLKOUT pin. VBCLK will be output to VBCLKOUT only if high level is input to VBCLKEN.

This output control is an enable control structure. Whiskers may occur when the pin settings are switched during an operation.

FPGA	VBCLKEN	System Clock Output Control
OFF	0	Disables output (low-level output)
ON	1	Enables output

(2) UCLKSEL0 (USB clock select)… FPGA

This selects the 48 MHz USB clock inputs (HCLK48M, FCLK48M) to be input to UCLK.

It selects the USB clock from UCLK, XT1, and XT2.

An on-board oscillation module (OSC3) is not provided.

FPGA	UCLKSEL0	USB Clock (HCLK48M, FCLK48M) Selection
0	0	Inputs XT1 or XT2
1	1	Inputs UCLK (inputs 48 MHz of OSC3)

(3) UCLKSEL1 (USB clock select)… FPGA

This selects the USB clock input (PCLK) to be input to PCLKIN.

The input frequency is from 25 MHz to 33 MHz.

It selects the internal USB bus bridge clock from PCLKIN, XT1, and XT2.

30 MHz is input from the on-board oscillation module (OSC2) to PCLKIN.

FPGA	UCLKSEL1	Internal USB Bus Bridge Clock (PCLK) Selection
0	0	Inputs XT1 or XT2
1	1	Inputs PCLKIN (inputs 30 MHz of OSC2)

(4) VSBRAMEN (VSB RAM enable)… FPGA

The PFESiP/V850EP1 has an on-chip 32 KB work RAM (VSB_RAM) on the VSB bus.
This work RAM (VSB_RAM) uses the VMCSZ2 (VDCSZ2) area. Connect VSBRAMEN to low level when connecting the VDCSZ2 (VDCSZ2) area to the external memory.

Table 3-2. On-Chip Work RAM (VSB_RAM) Setting

FPGA	VSBRAMEN	On-Chip Work RAM (VSB_RAM) Operation	VDCSZ2 (CSZ2) Area
0	0	On-chip work RAM (VSB_RAM) is disabled.	External memory
1	1	On-chip work RAM (VSB_RAM) is enabled.	On-chip work RAM (VSB_RAM)

Cautions 1. When using the work RAM (VSB_RAM), be sure to set the ME2 bit of bus cycle type configuration register 0 (BCT0) to 0 in order to prevent a conflict with the CSZ2 area (external memory) of the memory controller.

2. The CSZ2 pin becomes inactive when the work RAM is accessed.

(5) MODE0, MODE1 (USB operation mode)… FPGA

These select the operating mode of the PFESiP/V850EP1.

FPGA	FPGA	MODE1	MODE0	Operating Mode
0	0	0	0	USB function disabled
0	1	0	1	Only USB function enabled
1	0	1	0	Only USB host enabled
1	1	1	1	USB host/function enabled

(6) BOOTSEL (boot select)… FPGA

This selects the boot area from the SiP internal/external memory.
If the SiP interior is selected, the SiP chip select signal select register (SCSS) will be initialized to 0008H and booting will be performed from address 0000 0000H of the memory connected to the SCSZ0 pin.

FPGA	BOOTSEL	Boot Area Selection	Initial SCSS Register Value
0	0	Memory connected to SCSZ0 in SiP	0008H
1	1	Memory connected to CSZ0 of external bus interface	0000H

Caution The SCSZ0 signal for SiP internal connection is connected to the on-board FPGA similarly as other SiP internal connection buses. To emulate a system that has a boot ROM in the SiP, integrate the boot ROM to the on-board FPGA and connect it to the SiP internal bus.

3.2 Chip Select Signal Setting Dip Switches

Position	Figure 1-1 (Appearance) E-3

SW4 is the dip switch that sets the chip select signal of the on-board SDRAM.

Switch and Mark	Target Resource
SW4 (SDRAM)	SDRAM

The CSZn signal of the PFESiP/V850EP1 can be arbitrarily selected for the SDRAM.
The chip select signal set to be on will be enabled (n = 1, 3, 4, 6).

Caution Only a single type of a chip select signal can be used for a single resource. Consequently, do not switch multiple switches in a single dip to be on.

SRAM		
DPSW	When Switched on	When Switched off
SW4-1	Selects CSZ1	Deselects CSZ1
SW4-2	Selects CSZ3	Deselects CSZ3
SW4-3	Selects CSZ4	Deselects CSZ4
SW4-4	Selects CSZ6	Deselects CSZ6

3.3 Jumper Settings

The PFESiP EP-1 Evaluation Board Lite has two jumpers.
Set them appropriately according to the purpose of use.

JPn Position	Purpose	Setting	
JP1 B-4	LAN circuit speed selection	short	10 Mbps
		open	100 Mbps
JP2 C-4	Assigning CS to LAN circuit	short	Uses CSZ6 with a LAN (CSZ6 is fixed).
		open	Does not use a LAN.

3.3.1 JP1, JP2 (for setting LAN circuit)

Positions **Figure 1-1 (Appearance) B-4, C-4**

These set the operating state of a circuit using LAN9115 on-board.

(1) JP1 (SPEED_SEL)

JP1	LAN Controller Speed Selection	Automatic Negotiation
Short	Selects 10 Mbps.	Disabled
Open	Selects 100 Mbps.	Enabled

(2) JP2 (CS)

JP2	LAN Circuit CS Assignment
Short	Uses CSZ6 with LAN (other than CSZ6 cannot be used).
Open	Does not use LAN and releases CSZ6 for other purposes.

CHAPTER 4 EXTERNAL MEMORY ACCESS SETTING EXAMPLE

Settings such as chip select settings and settings of the number of waits are required to access the memories mounted on-board. These settings are performed in the initial program initialization process. With CA850, for example, the settings are set mainly in the startup routine.

Remark This chapter explains the register settings unique to the PFESiP EP-1 Evaluation Board Lite. See the references at the beginning of this manual for the settings of general registers.

4.1 On-Board Memory Specifications

Positions **Figure 1-1 (Appearance) F-3, F-4**

The PFESiP EP-1 Evaluation Board Lite has an on-board flash ROM and SDRAM that are used for general purposes. The PFESiP/V850EP1 has an on-chip instruction RAM (for fetching programs), data RAM (for data), and work RAM (for work).

4.1.1 External memory

Table 4-1. External Memories

	Flash ROM	SDRAM16
Product name	S29JL064H70TFI000H	MT48LC16M16A2TG-7E
Access time	70 ns@100 pF	C_L = 2/3, 5.4 ns
Capacity	8 MB	32 MB (32 MB × 1)
Bus size	16 bits	16 bits (16 bits × 1)
Chip select area	Fixed to CSZ0	Any one from CSZ1, CSZ3, CSZ4, and CSZ6

Remark The following setting examples are explained based on the following settings.

Flash ROM: CSZ0 area
VSB_RAM: CSZ2 area
SDRAM: CSZ3 area
USB: CSZ5 area
LAN: CSZ6 area

(1) Flash ROM

(a) Fixed values

Item	Corresponding Register	Setting Value	Remark
Chip area select	CSC0	Sub-areas 00 to 02	Connected to CSZ0 (instructions can be fetched) Flash ROM area is restricted because work RAM (VSB_RAM) is used.
Bus cycle type	BCT0	SRAM, I/O	S29JL064H70TFI000H does not support page mode.
Address setting wait	ASC	0	
Local bus size	LBS	16 bits	Maximum bus size of the PFESiP EP-1 Evaluation Board Lite is 16 bits.

(b) Operating frequency dependence

Item	Corresponding Register	BUSCLK			Remark
		75 MHz	50 MHz	25 MHz	
Data wait	DWC0	5	3	1	BUSCLK cycle × (Tw+1.5) –11.0–3.8–5 > 25 (@100 pF) BUSCLK cycle × (Tw+2) –11.0–3.8–5 > 70 (@100 pF)
Idle state	BCC	2	1	0	t_{DF} = 25 ns (max.) 11.0 + 25 + 2.5 – 1.5 – BUSCLK cycle

Remarks 1. For the data wait and on-page data wait, “BUSCLK cycle × (Number of waits + 1.5) – RDZ delay time (max.) – Data input setting (min.) – Substrate delay (to and fro)” must be longer than the ROM access time from the read strobe, and “BUSCLK cycle × (Number of waits + 2) – Address or chip select delay time (max.) – Data input setting (min.) – Substrate delay (to and fro)” must be longer than the ROM access time from an address or chip select signal.

2. A time exceeding “RDZ delay time (max.) + ROM data floating (max.) + Substrate delay (one-way) – Data output delay (min.) – BUSCLK cycle (of T0 cycle)” must be secured for the idle state.

3. The on-board flash ROM peripheral circuit is not equipped with a circuit applying high voltage. Consequently, only the following operating modes are supported.

Mode	CE#	OE#	WE#	RESET#	WP#/ACC	DQ0-DQ15
Read	L	L	H	H	Any	DOUT
Standby	H	Any	Any	H	Any	Hi-Z
Output disable	Any	H	H	Any	Any	Hi-Z
Write	L	H	⌐⌊⌐	H	Any	DIN
Hardware reset/standby	Any	Any	Any	L	Any	Hi-Z
Boot block protection	Any	Any	Any	Any	L	Any

4. The on-board flash ROM of the PFESiP EP-1 Evaluation Board Lite is fixed to word mode.

4.1.2 Internal memory

	Instruction RAM (iLB RAM)	Data RAM (dLB RAM)	Work RAM (VSB RAM)
Capacity	192 KB	32 KB	32 KB
Connection bus	iLB	dLB	VSB
Bus size	128 bits	32 bits	32 bits
Access clock	CPCLK × 1 clock	CPCLK × 1 clock	VBCLK × 2 clocks

(1) On-chip work RAM (VSB_RAM)

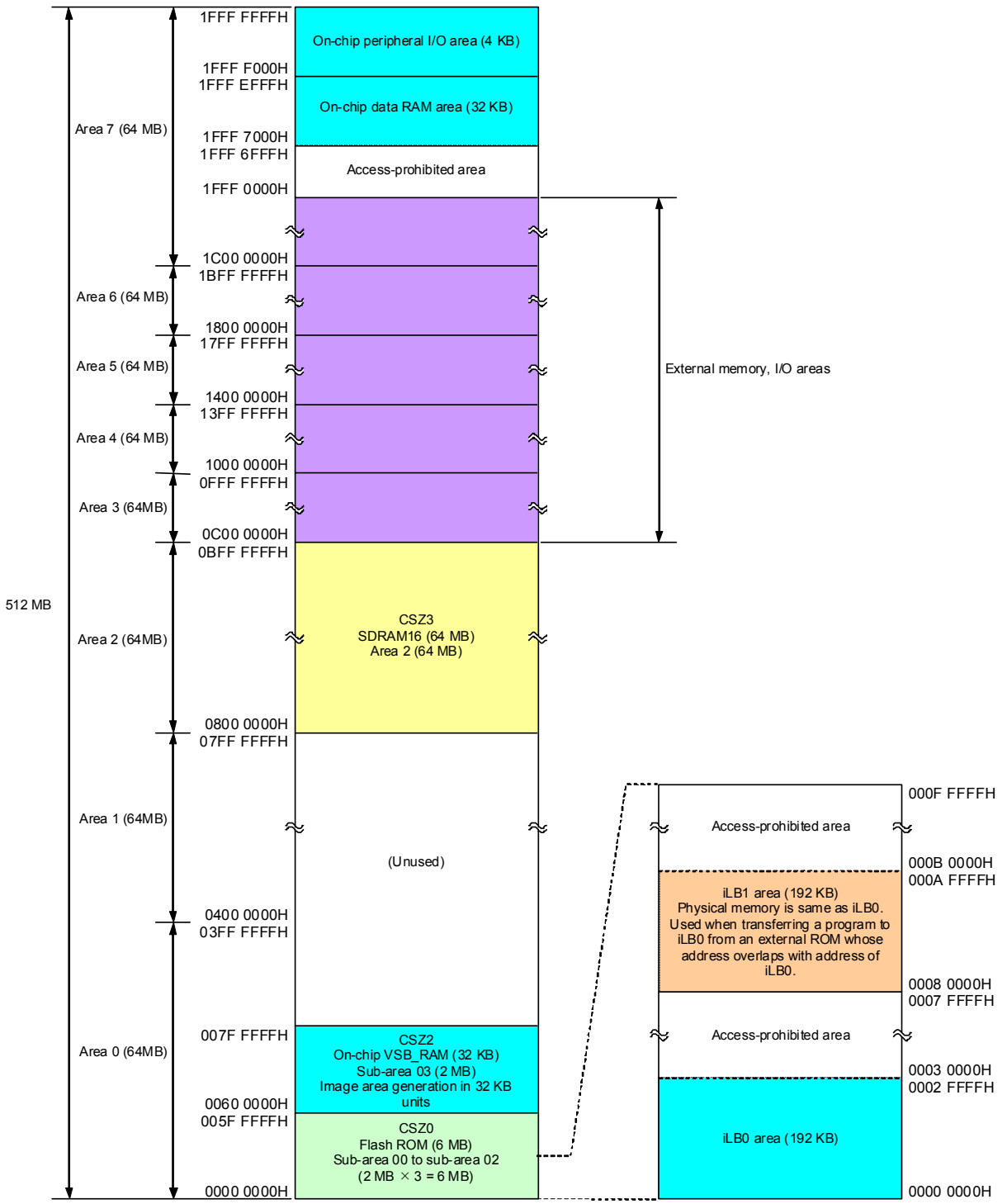
Item	Corresponding Register	Setting Value	Remark
Chip area select	CSC0	Sub-area 03	Connected to CSZ2 (instructions can be fetched)
Bus cycle type	BCT0	Operation disabled	Operation of CSZ2 area of memory controller disabled

Remark The VSB_RAM is always accessed in two VBCLK clocks.

(2) NPB strobe wait control register (VSWC)

Internal Bus Operating Frequency (VBCLK)	VSWC Setting Value
VBCLK ≤ 10.00MHz	0001 H
10.00 MHz < VBCLK ≤ 50.00 MHz	0041 H
50.00 MHz < VBCLK ≤ 66.00 MHz	0041 H
66.00 MHz < VBCLK ≤ 80.00 MHz	0042 H
80.00 MHz < VBCLK ≤100.00 MHz	0042 H

4.1.3 Memory map



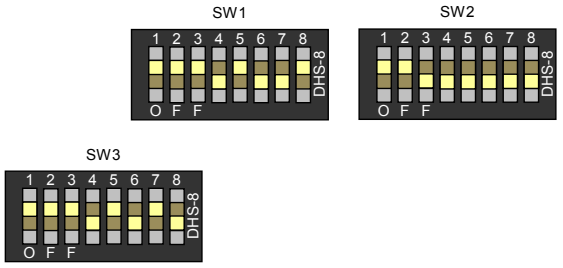
Remark Up to 8 MB can be used as the flash ROM, but the flash ROM area is restricted to 6 MB, because the on-chip work RAM (VSB_RAM) is used in this example.

4.2 Setting External Memory Access Operation

To start the PFESiP/V850EP1, the mode registers related to the following bus interfaces must be set. The following setting examples are those under the following conditions.

Item	Setting
XT1 input frequency	48 MHz
CPU pipeline clock (CPCLK)	200 MHz
Internal system clock (VBCLK)	100 MHz
Bus clock (BUSCLK)	50 MHz

Table 4-2. Mode Setting Using Dip Switches

Item	Setting Contents	Setting
PLL operating mode	SW1-1 to SW1-7: M value = 23 (m value = 24) SW1-8 to SW2-2: N value = 7 (n value = 100) SW2-3 and SW2-4: P value = 0 (p value = 1) Multiplication rate = n/m/p = × 4.1666 48 MHz × 4.1666 = 200 MHz	
	SW2-5 and SW2-6: Modulation cycle 15 kHz SW2-7 to SW3-1: No modulation SW3-2 and SW3-3: S selector = 2.0 MHz SW3-4: PLLFO is low-level output SW3-5 and SW3-6: VBCLK = CPCLK/2 SW3-7 and SW3-8: BUSCLK = VBCLK/2	

(1) Register setting values

Table 4-3. Register Setting Values

Address	Register Name	Register Symbol	Setting Example
1FFF F060H	Chip area select control register 0	CSC0	4807H
1FFF F062H	Chip area select control register 1	CSC1	0820H
1FFF F06EH	NPB strobe wait control register	VSWC	0042H
1FFF F44CH	Port 6 mode control register	PMC6	BFH
1FFF F44EH	Port 7 mode control register	PMC7	49H
1FFF F450H	Port 8 mode control register	PMC8	Initial value used
1FFF F452H	Port 9 mode control register	PMC9	Initial value used
1FFF F454H	Port 10 mode control register	PMC10	Initial value used
1FFF F480H	Bus cycle type configuration register 0	BCT0	B008H
1FFF F482H	Bus cycle type configuration register 1	BCT1	0880H
1FFF F484H	Data wait control register 0	DWC0	0003H
1FFF F486H	Data wait control register 1	DWC1	0700H
1FFF F488H	Bus cycle control register	BCC	0001H
1FFF F48AH	Address setting wait control register	ASC	0000H
1FFF F48CH	Bus cycle control register	BCP	Initial value used
1FFF F48EH	Local bus sizing control register	LBS	1861H
1FFF F494H	DMA flyby transfer wait control register	FWC	Initial value used
1FFF F496H	DMA flyby transfer idle control register	FIC	Initial value used
1FFF F498H	Bus mode control register	BMC	Initial value used
1FFF F49AH	Page ROM configuration register	PRC	Initial value used
1FFF F4A4H	SDRAM configuration register 1	SCR1	Initial value used
1FFF F4A6H	SDRAM refresh control register 1	RFS1	Initial value used
1FFF F4ACH	SDRAM configuration register 3	SCR3	2099H
1FFF F4AEH	SDRAM refresh control register 3	RFS3	800BH
1FFF F4B0H	SDRAM configuration register 4	SCR4	Initial value used
1FFF F4B2H	SDRAM refresh control register 4	RFS4	Initial value used
1FFF F4B8H	SDRAM configuration register 6	SCR6	Initial value used
1FFF F4BAH	SDRAM refresh control register 6	RFS6	Initial value used
1FFF F8B0H	Write enable switch register	WREN	Initial value used

(2) Port 6 mode control register (PMC6)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC6	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	1FFFF44CH	83H	R/W
Setting value	1	0	1	1	1	1	1	1		BFH	
Alternative function	A1	A0	A25	A24	A23	A22	A21	A20			
Function selection	A1	P66	A25	A24	A23	A22	A21	A20			

(3) Port 7 mode control register (PMC7)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC7	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	1FFFF44EH	01H	R/W
Setting value	0	1	0	0	1	0	0	1		49H	
Alternative function	CSZ7	CSZ6	CSZ5	CSZ4	CSZ3	CSZ2	CSZ1	WAITZ			
Function selection	P77	CSZ6	P75	P74	CSZ3	P72	P71	WAITZ			

(4) Chip area select control register 0 (CSC0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
CSC0	CS 33	CS 32	CS 31	CS 30	CS 23	CS 22	CS 21	CS 20	CS 13	CS 12	CS 11	CS 10	CS 03	CS 02	CS 01	CS 00	1FFFF060H	C231H	R/W
Setting value	0	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1		4807H	
CSZn signal	CSZ3				CSZ2				CSZ1				CSZ0						
Selected area	Area 2				Sub-area 03				Unused				Sub-areas 00 to 02						
Target	SDRAM				VSB_RAM				Unused				Flash ROM						

(5) Chip area select control register 1 (CSC1)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
CSC1	CS 43	CS 42	CS 41	CS 40	CS 53	CS 52	CS 51	CS 50	CS 63	CS 62	CS 61	CS 60	CS 73	CS 72	CS 71	CS 70	1FFFF062H	C231H	R/W
Setting value	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0		0820H	
CSZn signal	CSZ4				CSZ5				CSZ6				CSZ7						
Selected area	Unused				Sub-area 70				Area 6				Unused						
Target	Unused				USB				LAN				Unused						

(6) Bus cycle type configuration register 0 (BCT0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
BCT0	ME3	0	BT 31	BT 30	ME2	0	0	BT 20	ME1	0	BT 11	BT 10	ME0	0	0	BT 00	1FFFF480H	8888H	R/W
Setting value	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0		B008H	
CSZn signal	CSZ3				CSZ2				CSZ1				CSZ0						
Operation	SDRAM				Unused				Unused				SRAM,I/O						
Target	SDRAM				VSB_RAM				Unused				Flash ROM						

(7) Bus cycle type configuration register 1 (BCT1)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
BCT1	ME7	0	0	BT 70	ME6	0	BT 61	BT 60	ME5	0	0	BT 50	ME4	0	BT 41	BT 40	1FFFF482H	8888H	R/W
Setting value	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0		0880H	
CSZn signal	CSZ7				CSZ6				CSZ5				CSZ4						
Operation	Unused				SRAM,I/O				SRAM,I/O				Unused						
Target	Unused				LAN				USB				Unused						

(8) NPB strobe wait control register (VSWC)

Only internal NPB is used.

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
VSWC	0	0	0	0	0	0	0	0	SUW L1	SUW L2	0	0	VSW L3	VSW L2	VSW L1	VSW L0	1FFFF06EH	00CFH	R/W
VSWC	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0		0042H	
Operation	Data setup = 1 VBCLK →												VPSTB=3VBCLK						

(9) Data wait control register 0 (DWC0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
DWC0	0	DW 32	DW 31	DW 30	0	DW 22	DW 21	DW 20	0	DW 12	DW 11	DW 10	0	DW 02	DW 01	DW 00	1FFFF484H	7777H	R/W
Setting value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1		0003H	
CSZn signal	CSZ3				CSZ2				CSZ1				CSZ0						
Operation	-				-				0 wait				3 waits						
Target	SDRAM				VSB_RAM				Unused				Flash ROM						

(10) Data wait control register 1 (DWC1)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
DWC1	0	DW 72	DW 71	DW 70	0	DW 62	DW 61	DW 60	0	DW 52	DW 51	DW 50	0	DW 42	DW 41	DW 40	1FFFF486H	7777H	R/W
Setting value	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0		0700H	
CSZn signal	CSZ7				CSZ6				CSZ5				CSZ4						
Operation	0 wait				7 waits				0 wait				0 wait						
Target	Unused				LAN				USB				Unused						

(11) Bus cycle control register (BCC)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
BCC	BC 71	BC 70	BC 61	BC 60	BC 51	BC 50	BC 41	BC 40	BC 31	BC 30	BC 21	BC 20	BC 11	BC 10	BC 01	BC 00	1FFFF488H	FFFFH	R/W
Setting value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		0001H	
Target CS	CSZ7		CSZ6		CSZ5		CSZ4		CSZ3		CSZ2		CSZ1		CSZ0				
Operation	0		0		0		0		0		-		0		1				
Target	Unused		LAN		USB		Unused		SDRAM		VSB_RAM		Unused		Flash ROM				

(12) Address setting wait control register (ASC)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
ASC	AC 71	AC 70	AC 61	AC 60	AC 51	AC 50	AC 41	AC 40	AC 31	AC 30	AC 21	AC 20	AC 11	AC 10	AC 01	AC 00	1FFFF48AH	FFFFH	R/W
Setting value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0000H	
Target CS	CSZ7		CSZ6		CSZ5		CSZ4		CSZ3		CSZ2		CSZ1		CSZ0				
Operation	0		0		0		0		-		-		0		0				
Target	Unused		LAN		USB		Unused		SDRAM		VSB_RAM		Unused		Flash ROM				

(13) Local bus sizing control register (LBS)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
LBS	LB 71	LB 70	LB 61	LB 60	LB 51	LB 50	LB 41	LB 40	LB 31	LB 30	LB 21	LB 20	LB 11	LB 10	LB 01	LB 00	1FFFF48EH	5555H/Note1	R/W
Setting value	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1		1861H	
Target CS	CSZ7		CSZ6		CSZ5		CSZ4		CSZ3		CSZ2		CSZ1		CSZ0				
Operation	8 bits		16 bits		32 bits		8 bits		16 bits		**Note2**		8 bits		16 bits				
Target	Unused		LAN		USB		Unused		SDRAM		VSB_RAM		Unused		Flash ROM				

Notes 1. With the PFESiP EP-1 Evaluation Board Lite, the levels of SLBS0 and SLBS1 of the PFESiP/V850EP1 are fixed on-board, and SLBS0 and SLBS1 are started at a 16-bit bus width. The initial value of LBS at this time is 5555H. Furthermore, the external bus cannot be used at a 32-bit bus width.

2. The VSB_RAM is connected at a 32-bit width, regardless of the LBS register setting.

(14) SDRAM configuration register 3 (SCR3)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
SCR3	LTC	LTM2	LTM1	LTM0	0	0	0	WCF	BCW1	BCW0	SSO1	SSO0	RAW1	RAW0	SAW1	SAW0	1FFFF4ACH	30C0H	R/W
Setting value	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0	1		2099H	
Operation	Normal	CL = 2			-			-	2 waits		16 bits		RAW=13		SAW=9				

(15) SDRAM refresh control register 3 (RFS3)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
RFS3	REN	0	0	0	0	0	RCC1	RCC0	0	0	RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	1FFFF4AEH	0000H	R/W
Setting value	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0		800CH	
Operation	Enabled	-					Cfac=32		-		RIN=12								

4.2.1 PFESiP/V850EP1 start procedure

The PFESiP/V850EP1 starts fetching instruction after a reset is released when it has completed waiting for oscillation stabilization and the on-chip PLL to be locked.

Initialize the PFESiP/V850EP1 according to the following sequence.

(1) When not using on-chip instruction RAM (always fetching instructions with external memory)

Fetching instructions is started from address 0000 0000H in the external memory after a reset is released. First, use an execution program to set the following registers that affect the external bus access performance. Fetching instructions from address 0000 0000H is also started by inputting a reset while the power is turned on.

- NPB strobe wait control register (VSWC)
  On-chip peripheral I/O (NPB) access wait setting
- Data wait control registers 0, 1 (DWC0, DWC1)
  External bus data wait setting
- Address setting wait control register (ASC)
  External bus address setup wait setting
- Bus cycle control register (BCC)
  External bus idle state setting

Set registers such as chip area select control registers 0 and 1 (CSC0, CSC1), bus cycle type configuration registers 0 and 1 (BCT0, BCT1), the local bus sizing control register (LBS), and the page ROM configuration register (PRC) as required.

	Manipulation Procedure
<1>	Starting booting from external memory after releasing system reset
<2>	Normal program start

(2) Disabling on-chip instruction RAM → Enabling on-chip instruction RAM: (Changing during program execution)

Fetching instructions from address 0000 0000H in the external memory is started after a reset is released.

First, use the execution program to check/set the following registers that affect the external bus access performance.

The instruction RAM (iLB_RAM) cannot be accessed from the CPU (NBA85E2S) because the instruction RAM (iLB_RAM) is disabled, but the DMAC (NBA85E300) connected to the CPU (NBA85E2S) can specify the instruction RAM (iLB_RAM) as the DMA transfer destination setting in the external DMA addressing control register DMXADCn (n = 0 to 3). If the instruction RAM (iLB_RAM) is specified as the transfer destination, DMA transfer can be performed for the instruction RAM (iLB_RAM).

The program is started from the external memory when starting the CPU (NBA85E2S) and the contents of the external memory are transferred to the instruction RAM (iLB_RAM) using this function. After the transfer is completed, fetching instructions from the instruction RAM (iLB_RAM) is started by enabling the instruction RAM (iLB_RAM) using the iLB RAM control register and jumping to address 0000 0000H.

The V850E2 architecture enables program execution from the data RAM (dLB_RAM) area. Executing the program to perform DMA transfer from the external memory to the instruction RAM (iLB_RAM) and re-setting the on-chip instruction RAM (iLB_RAM) using the iLB RAM control register (ILBEN) is executed using the data RAM (dLB_RAM).

The stages before and after downloading to the instruction RAM (iLB_RAM) can be identified by checking the iLB RAM control register setting when fetching instructions from address 0000 0000H.

- iLB RAM control register (ILBEN)
  Instruction RAM (iLB_RAM) area (iLB0 area) check
- NPB strobe wait control register (VSWC)
  On-chip peripheral I/O (NPB) access wait setting
- Data wait control registers 0, 1 (DWC0, DWC1)
  External bus data wait setting
- Address setting wait control register (ASC)
  External bus address setup wait setting
- Bus cycle control register (BCC)
  External bus idle state setting

Set registers such as chip area select control registers 0 and 1 (CSC0, CSC1), bus cycle type configuration registers 0 and 1 (BCT0, BCT1), the local bus sizing control register (LBS), and the page ROM configuration register (PRC) as required.

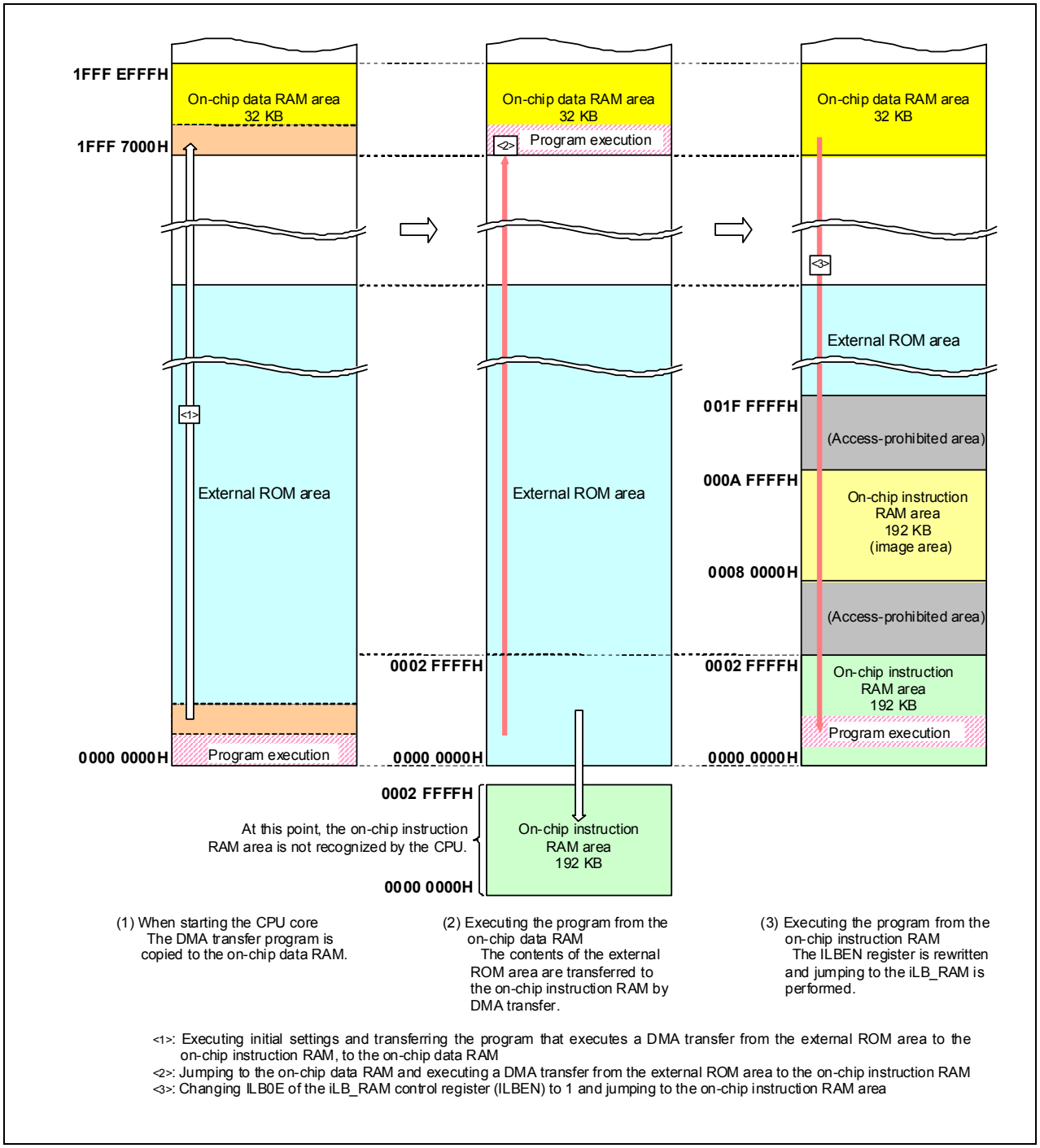
	Manipulation Procedure
<1>	Starting booting from external ROM after releasing system reset
<2>	Identifying iLB0E of iLB RAM control register (ILBEN) (iLB0E = 0)
<3>	Transferring program transferring external ROM contents to instruction RAM (iLB_RAM) to data RAM (dLB_RAM) area
<4>	Jumping to data RAM (dLB_RAM) transfer program
<5>	Transferring the contents of addresses 0000 0000H to 0002 FFFFH in external memory to addresses 0000 0000H to 0002 FFFFH in instruction RAM (iLB_RAM) area by DMA transfer
<6>	Setting iLB0E of iLB RAM control register (ILBEN) to 1 (verifying ILBEN register after writing)
<7>	Starting booting from on-chip instruction RAM (iLB_RAM) after jumping to address 0
<8>	Identifying iLB0E of iLB RAM control register (ILBEN) (iLB0E = 1)
<9>	Normal program start

Caution Set SDRAM configuration registers 1, 3, 4, and 6 (SCR1, SCR3, SCR4, and SCR6) after process <3>.

Remark Maskable interrupt requests generated while interrupts are disabled (DI state) are suspended. The maskable interrupt requests will be acknowledged immediately after the interrupt enable state (EI state) is set, if the interrupt requests are not cleared (the xxIFn bit of the interrupt control register (xxICn) is not cleared (0)) and the xxMKn bit of the interrupt control register is not set (1). Only one interrupt request, however, will be suspended for a single interrupt source, and only one interrupt request will be acknowledged even if two or more of the same interrupt request are generated.

An example in which the program is executed by copying the contents of the external ROM to the instruction RAM (iLB_RAM) is shown below.

Figure 4-1. Transfer from External ROM to Instruction RAM (iLB_RAM)



<1>: Executing initial settings and transferring the program that executes a DMA transfer from the external ROM area to the on-chip instruction RAM, to the on-chip data RAM
<2>: Jumping to the on-chip data RAM and executing a DMA transfer from the external ROM area to the on-chip instruction RAM
<3>: Changing ILB0E of the iLB_RAM control register (ILBEN) to 1 and jumping to the on-chip instruction RAM area

CHAPTER 5 USING EXPANSION CONNECTORS

The PFESiP EP-1 Evaluation Board Lite has two types of expansion connectors.

Some general-purpose ports of the PFESiP/V850EP1 can be used for CN1 and CN2, and general-purpose signals (GPIOn) from the FPGA for CN3 and CN4.

Connector Shape	No. of Pins	Connector No.	No. of Signals	
				Subtotal
General-purpose 50-pin connectors	50×2 = 100	CN1	For PFESiP/V850EP1 I/Os	40
		CN2	For PFESiP/V850EP1 I/Os	27
			For PFESiP/V850EP1 analog inputs	8
General-purpose 50-pin connectors	50×2 = 100	CN3	FPGA general purposes 40	40
		CN4	FPGA general purposes 40	40

Numerous GPIOs of the on-board FPGA are connected to the expansion connectors.

Any signal can therefore be connected to the connectors by the on-board FPGA. Note, however, that the operating speed drops depending on the length of the signal lines.

5.1 Connectors (CN3, CN4)

Two 50-pin headers to which signals from the FPGA can be easily input or output are provided.

General-purpose flat cables with a 2.54 mm pitch by two rows can be used.

The connectors can be used as the pins for checking the circuit integrated to the FPGA. Power must be separately supplied to an external circuit, because only GND is connected as a power supply.

Table 5-1. Simplified Connector (General-Purpose 50-Pin) Pin Layout

CN3 pin layout

No.	Signal Name	Signal Name	No.
1	GND	GPIO00	2
3	GPIO01	GPIO02	4
5	GPIO03	GND	6
7	GPIO04	GPIO05	8
9	GPIO06	GPIO07	10
11	GND	GPIO08	12
13	GPIO09	GPIO10	14
15	GPIO11	GND	16
17	GPIO12	GPIO13	18
19	GPIO14	GPIO15	20
21	GND	GPIO16	22
23	GPIO17	GPIO18	24
25	GPIO19	GND	26
27	GPIO20	GPIO21	28
29	GPIO22	GPIO23	30
31	GND	GPIO24	32
33	GPIO25	GPIO26	34
35	GPIO27	GND	36
37	GPIO28	GPIO29	38
39	GPIO30	GPIO31	40
41	GND	GPIO32	42
43	GPIO33	GPIO34	44
45	GPIO35	GND	46
47	GPIO36	GPIO37	48
49	GPIO38	GPIO39	50

CN4 pin layout

No.	Signal Name	Signal Name	No.
1	GND	GPIO40	2
3	GPIO41	GPIO42	4
5	GPIO43	GND	6
7	GPIO44	GPIO45	8
9	GPIO46	GPIO47	10
11	GND	GPIO48	12
13	GPIO49	GPIO50	14
15	GPIO51	GND	16
17	GPIO52	GPIO53	18
19	GPIO54	GPIO55	20
21	GND	GPIO56	22
23	GPIO57	GPIO58	24
25	GPIO59	GND	26
27	GPIO60	GPIO61	28
29	GPIO62	GPIO63	30
31	GND	GPIO64	32
33	GPIO65	GPIO66	34
35	GPIO67	GND	36
37	GPIO68	GPIO69	38
39	GPIO70	GPIO71	40
41	GND	GPIO72	42
43	GPIO73	GPIO74	44
45	GPIO75	GND	46
47	GPIO76	GPIO77	48
49	GPIO78	GPIO79	50

5.2 PFESiP/V850EP1 Port Output Connectors (CN1, CN2)

Two 50-pin headers for the port output of the PFESiP/V850EP1 are provided.
General-purpose flat cables with a 2.54 mm pitch by two rows can be used.

Table 5-2. PFESiP/V850EP1 Ports Connected to CN1 and CN2

Port Name	Shared Pin
P00-P07	INTPZ0-INTPZ7
P10-P17	INTPZ8-INTPZ15
P30	RXD0
P31	TXD0
P32	RXD1
P33	TXD1
P34	RXD2
P35	TXD2
P36	RXD3
P37	TXD3
P40-P43	TI0-TI3
P44-P47	TCLR0-TCLR3
P50-P53	TO0-TO3
P54, P55	ETIUD0, ETIUD1
P56, P57	ETCUD0, ETCUD1

Port Name	Shared Pin
	BUSCLK
P60-P67	A20-A25, A0-A1
P110, P111	ETCLR0, ETCLR1
P112, P113	ETO0, ETO1
P120-P121	TCZ0-TCZ1
P124-P125	DMAAKZ0-DMAAKZ1
P130-P131	DMARQZ0-DMARQZ1
P140	SCK0
P141	SI0
P142	SO0
P143	SCK1
P144	SI1
P145	SO1
P146-P147	PWMO0-PWMO1
	AIN0-AIN7

Table 5-3. Simplified Connector (General-Purpose 50-Pin) Pin Layout

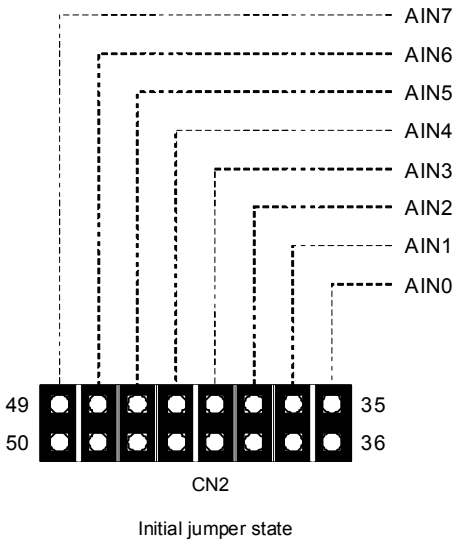
CN1 pin layout

No.	Signal Name	Signal Name	No.
1	GND	P00/INTPZ0/CCC00	2
3	P01/INTPZ1/CCC01	P02/INTPZ2/CCC10	4
5	P03/INTPZ3/CCC11	GND	6
7	P04/INTPZ4/CCC20	P05/INTPZ5/CCC21	8
9	P06/INTPZ6/CCC30	P07/INTPZ7/CCC31	10
11	GND	P10/INTPZ8/CC00	12
13	P11/INTPZ9/CC01	P12/INTPZ10/CC10	14
15	P13/INTPZ11/CC11	GND	16
17	P14/INTPZ12	P15/INTPZ13	18
19	P16/INTPZ14	P17/INTPZ15	20
21	GND	P30/RXD0	22
23	P31/TXD0	P32/RXD1	24
25	P33/TXD1	GND	26
27	P34/RXD2	P35/TXD2	28
29	P36/RXD3	P37/TXD3	30
31	GND	P40/TI0	32
33	P41/TI1	P42/TI2	34
35	P43/TI3	GND	36
37	P44/TCLR0	P45/TCLR1	38
39	P46/TCLR2	P47/TCLR3	40
41	GND	P50/TO0	42
43	P50/TO0	P52/TO2	44
45	P53/TO3	GND	46
47	P54/ETIUD0	P55/ETIUD1	48
49	P56/ETCUD0	P57/ETCUD1	50

CN2 pin layout

No.	Signal Name	Signal Name	No.
1	GND	BUSCLK	2
3	P60/A20	P61/A21	4
5	P62/A22	GND	6
7	P63/A23	P64/A24	8
9	P65/A25	P66/A0	10
11	GND	P67/A1	12
13	P110/ETCLR0	P111/ETCLR1	14
15	P112/ETO0	GND	16
17	P113/ETO1	P120/TCZ0	18
19	P121/TCZ1	P124/DMAAKZ0	20
21	GND	P125/DMAAKZ1	22
23	P130/DMARQZ0	P131/DMARQZ1	24
25	P140/SCK0	GND	26
27	P141/SI0	P142/SO0	28
29	P143/SCK1	P144/SI1	30
31	GND	P145/SO1	32
33	P146/PWMO0	P147/PWMO1	34
35	ANI0	GND	36
37	ANI1	GND	38
39	ANI2	GND	40
41	ANI3	GND	42
43	ANI4	GND	44
45	ANI5	GND	46
47	ANI6	GND	48
49	ANI7	GND	50

Table 5-4. Analog Pin Jumper Post Setting



Initial jumper state

(1) CN2, pins 35 to 50 (ANI0 to ANI7)

ANI0 to ANI7 of the A/D converter of the PFESiP/V850EP1 are connected to pins 35 to 50 of CN2 such that each signal is paired with GND.

To externally input analog signals, connect the signals to this terminal using twisted pair lines by which each signal is paired with GND.

CHAPTER 6 EMULATION CONNECTOR

6.1 N-Wire Interface

Position | **Figure 1-1 (Appearance) C-1**

The PFESiP/V850EP1 incorporates an on-chip debug function (debug control unit: DCU).

The 26-pin connector, 8830E-026-170S (straight) made by KEL is provided as a connector to connect this DCU to the in-circuit emulator supporting N-Wire.

The DCU trace function incorporated in the PFESiP/V850EP1 cannot be used.

The MINICUBE (QB-V850MINI) made by NEC Electronics is the standard in-circuit emulator.

The RTE-2000-TP and RTE-2000H-TP made by Midas lab can also be used. CBL-J40 is the connection cable for using the RTE-2000-TP made by Midas lab. CBL-KEL26 is the connection cable for using the RTE-2000H-TP.

Remarks 1. Documents related to the QB-V850MINI can be downloaded from the following URL.
http://www.necel.com/cgi-bin/nesdis/o003.cgi?article=QB-V850MINI

2. The QB-V850MINI includes the ID850QB as the debugger.

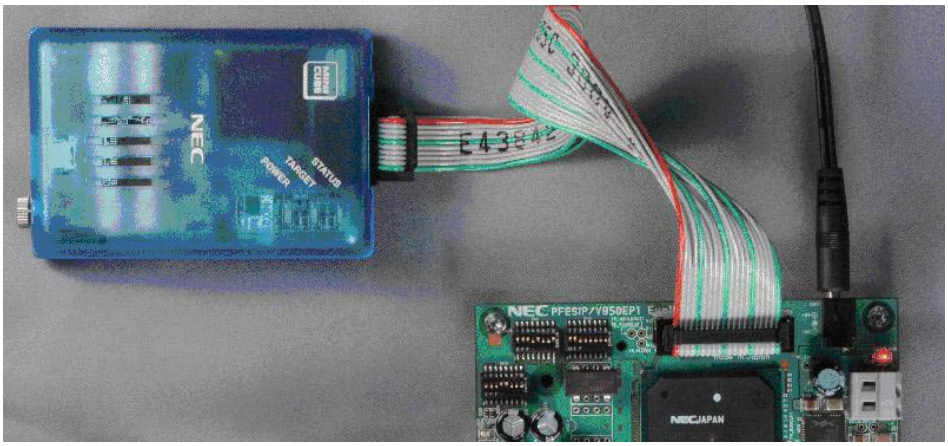
3. Contact an agency of Midas lab, Inc. for how to use the RTE-2000-TP and RTE-2000H-TP.

Table 6-1. N-Wire Connector (CN5)

Purpose	Pin No.	Signal Name
Connection to GND	A1	TRCCLK
Connection to GND	A2	TRCDATA0
Connection to GND	A3	TRCDATA1
Connection to GND	A4	TRCDATA2
Connection to GND	A5	TRCDATA3
Connection to GND	A6	TRCEND
DDI	A7	DDI
DCK	A8	DCK
DMS	A9	DMS
DDO	A10	DDO
DRSTZ	A11	DRSTZ
OPEN	A12	Reserve
RMODEZ	A13	Reserve

Signal Name	Pin No.	Purpose
GND	B1	Connection to GND
GND	B2	Connection to GND
GND	B3	Connection to GND
GND	B4	Connection to GND
GND	B5	Connection to GND
GND	B6	Connection to GND
GND	B7	Connection to GND
GND	B8	Connection to GND
GND	B9	Connection to GND
GND	B10	Connection to GND
Reserve	B11	Connection to GND
Reserve	B12	Connection to GND
VCCIO	B13	Connection to 3.3 V

Figure 6-1. Connection with MINICUBE (QB-V850MINI)



CHAPTER 7 ON-BOARD FPGA

Position	Figure 1-1 (Appearance) D-4

The PFESiP EP-1 Evaluation Board Lite is a development evaluation board for assisting the development of PFESiP EP-1 Series products.

It can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and as a PFESiP EP-1 prototyping environment by using the functions of the embedded array (EA-9HD), which is provided with the user logic paired with the PFESiP/V850EP1, for user logic development and verification by the on-board FPGA within the PFESiP EP-1 Series SiP. Specifically, the SiP internal connection buses connected in the SiP are all connected to the on-board FPGA.

Numerous GPIOs of the on-board FPGA are connected to the expansion connectors and any signal can be connected to the connectors by the on-board FPGA.

The FPGA is a product in the Stratix II Family made by Altera. The EP2S15F484C5 is provided as the standard FPGA.

The FPGA is configured using a configuration device (EPCS16) and programming can be performed from a personal computer by connecting ByteBlaster II or the USB Blaster Download Cable to the Active Serial Programming I/F connector (CN10).

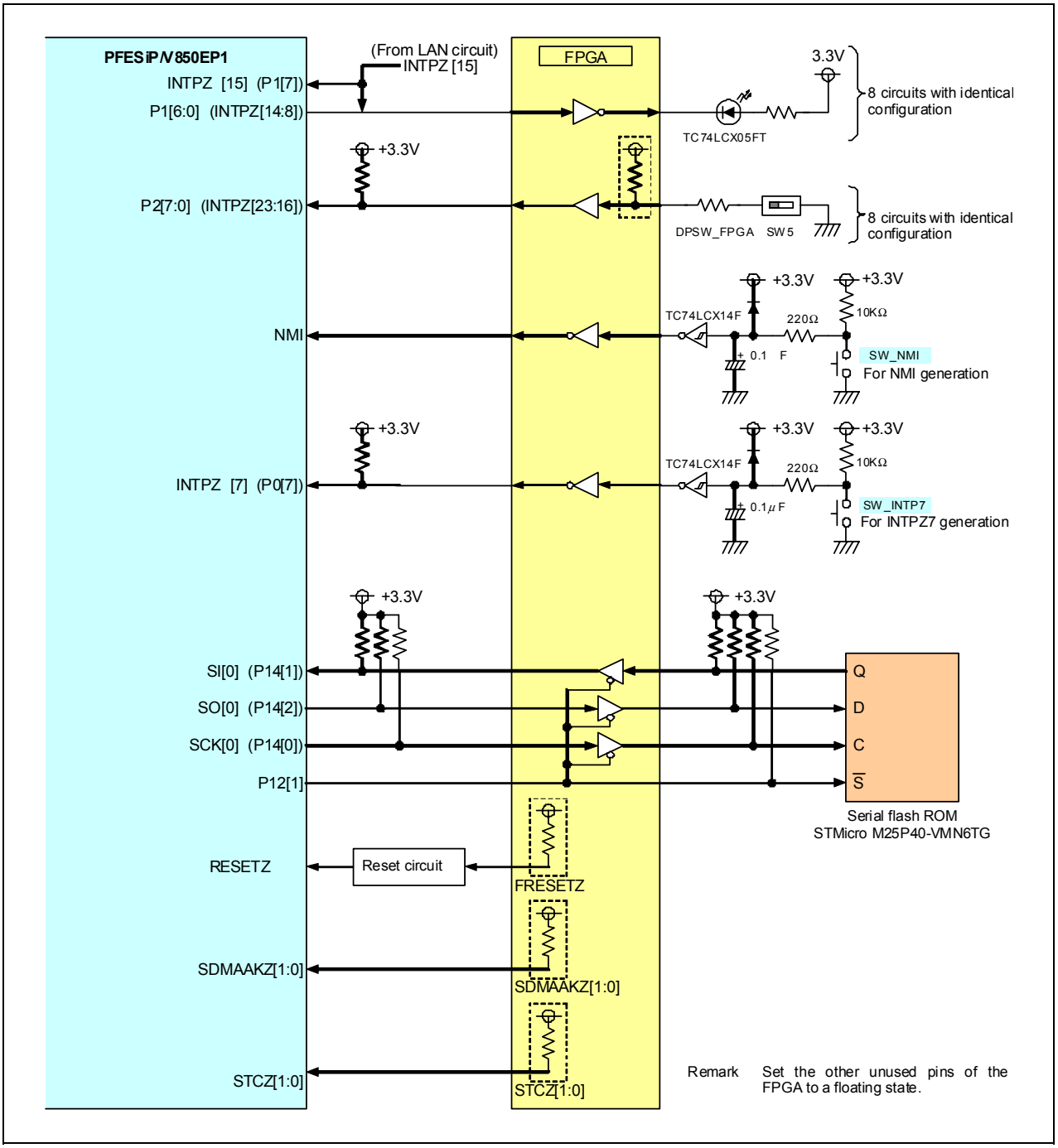
7.1 Default FPGA Programming

The FPGA is intended to be used for application evaluation of the PFESiP/V850EP1 and a user ASIC (embedded array (EA-9HD)), but only the minimum of functions are programmed when it is shipped.

P20 to P27, P10 to P17, NMI, and INTPZ7 are connected as follows. This enables the lighting of the LEDs and level input from a dip switch (FPGA_DPSW: SW5) by the PFESiP/V850EP1 via the FPGA.

The on-board serial ROM is connected to channel 0 of the on-chip clocked serial interface of the PFESiP/V850EP1.

Figure 7-1. Default FPGA Programming



7.1.1 VerilogHDL source of default PFESiP/V850EP1 data

V850EP1_Lite_Default.v file (1/2)

```
//-----------------------------------------------------
//
//  Library Name :  V850EP1_Lite_Default
//  Unit    Name :  V850EP1_Lite_Default_top
//
//-----------------------------------------------------

module V850EP1_Lite_Default_top(
     NMI_IN,
     SROM_Q,
     DIP_,
     P12,
     P2,
     SCK,
     SO,
     SW_INTP,
     NMI_OUT,
     SROM_D,
     SROM_CLK,
     SROM__S,
     INTPZ,
     LED,
     P1,
     SI
);

inputNMI_IN;
wire NMI_IN;
inputSROM_Q;
wire SROM_Q;
input[8:1] DIP_;
wire [8:1] DIP_;
input[1:1] P12;
wire [1:1] P12;
input[7:0] P1;
wire [7:0] P1;
input[0:0] SCK;
wire [0:0] SCK;
input[0:0] SO;
wire [0:0] SO;
input[7:7] SW_INTP;
wire [7:7] SW_INTP;
output NMI_OUT;
wire NMI_OUT;
output SROM_D;
wire SROM_D;
output SROM_CLK;
wire SROM_CLK;
output SROM__S;
wire SROM__S;
output [7:7] INTPZ;
wire [7:7] INTPZ;
output [8:1] LED;
wire [8:1] LED;
output [7:0] P2;
wire [7:0] P2;
output [0:0] SI;
wire [0:0] SI;
```

V850EP1_Lite_Default.v file (2/2)

```
    assign LED[8:1] = ~ (P1[7:0]);

    assign P2[7:0] = DIP_[8:1];

    assign NMI_OUT = ~ (NMI_IN);

    assign INTPZ[7] = ~ (SW_INTP[7]);

    assign SROM_CLK = (P12[1] == 1'b0) ? SCK[0] : 1'bz;

    assign SROM__S = P12[1];

    assign SROM_D = (P12[1] == 1'b0) ? SO[0] : 1'bz;

    assign SI[0] = (P12[1] == 1'b0) ? SROM_Q : 1'bz;


endmodule
```

7.2 Default FPGA Data

A setting file corresponding to the Quartus II software made by Altera is provided for the default programming of the on-board FPGA.

7.2.1 FPGA data generation environment

The Stratix II Family EP2S15F484C5 made by Altera is mounted as the FPGA and the EPCS16, which is an active serial device, is mounted as the configuration device.

The following tool of the following version is required for generating the FPGA data.

Quartus II	Web Edition 7.2 or later

When generating the FPGA data, set the following options in the Device and Pin Options dialog box when generating a project.

Target Device	EP2S15F484C5
Configuration Device	EPCS16
General	Enable INIT_DONE output
Unused Pins	As input tri-stated

7.2.2 File explanation

The TOP directory is V850EP1_Lite_Default.

Only the main files are explained in Table 7-1.

Table 7-1. Explanation of Files Directly under TOP Directory

File Name	Purpose
V850EP1_Lite_Default.qpf	Quartus II project file
V850EP1_Lite_Default.v	VerilogHDL source of default data
V850EP1_Lite_Default.qsf	File storing pin layout information, device information, and information of each option setting
V850EP1_Lite_Default.pof	File to be written to the FPGA download ROM

Remark The above files are recommended to be backed up, taking into consideration that they may not operate due to faults in a newly created circuit.

7.3 Push Switches for FPGA

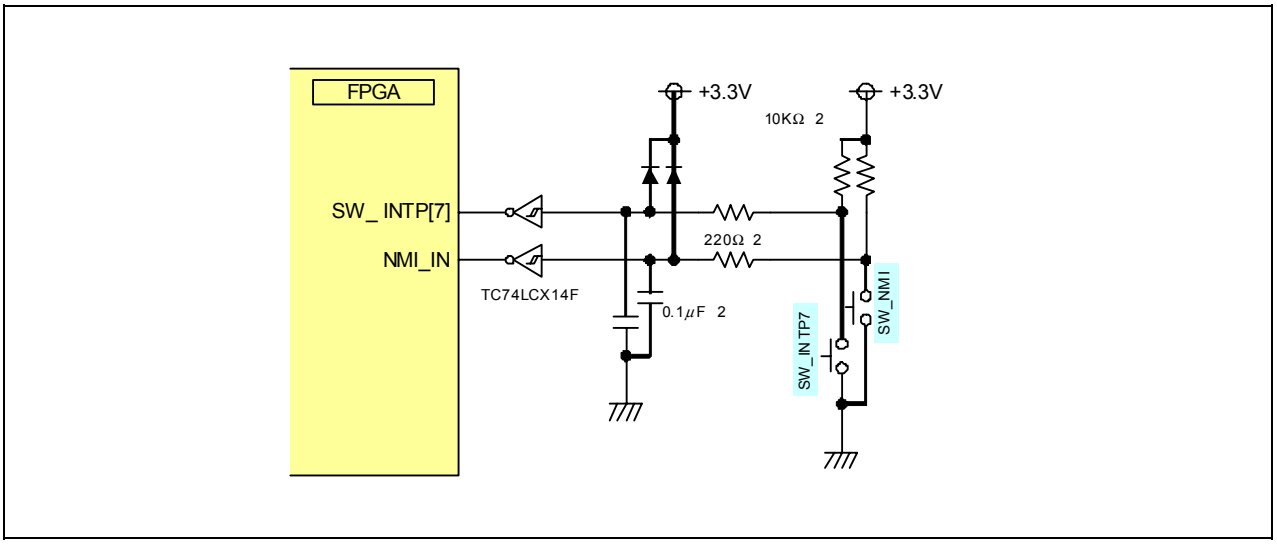
Positions	Figure 1-1 (Appearance) E-5, E-6

The FPGA is connected to two push switches provided with a chattering prevention circuit.

The switches are connected to NMI and INTP7 in the default FPGA circuit.

All interrupt request flags are cleared in the initialization program, because if the internal initialization is earlier than the rise of the chattering prevention circuit power supply when the power is turned on, the interrupt request flag will be set during booting.

Figure 7-2. Push Switches for FPGA



7.4 DIP Switches for FPGA

Positions	Figure 1-1 (Appearance) E-5 to D-5

The FPGA is connected to DIP switches. The states of the DIP switches can be sampled by any signal thanks to the internal connections of the FPGA. The pins to which the DIP switches are connected are externally pulled up and low level is input when the DIP switches are turned on. The DIP switch signals are dumped via 1 kΩ resistors to prevent a large current from flowing when high level is output while the DIP switches are turned on.

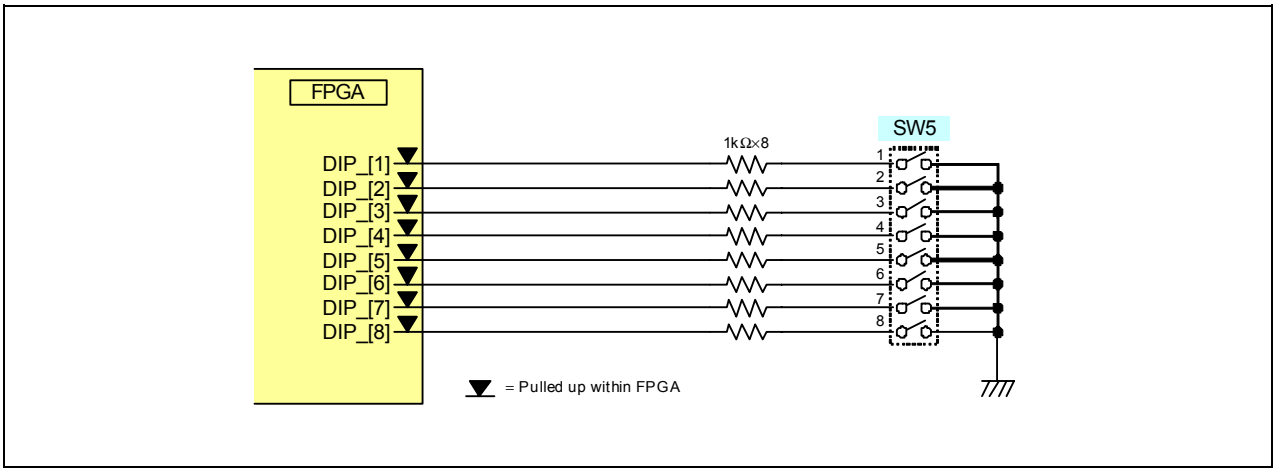
The DIP switches are connected to port 1 (P10 to P17) of the PFESiP/V850EP1 in the default FPGA circuit.

If P10 to P17 are set to control mode using the PMC1 register, they function as external interrupt signals INTPZ8 to INTPZ15. A chattering absorption circuit, however, is not provided.

Table 7-2. SW5 Operation with Default Program

SW5	P1 (P10 to P17/INTPZ8 to INTPZ15)
OFF	FFH
ON	00H

Figure 7-3. DIP Switches for FPGA



Caution Be sure to never set port 1 (P1) to output mode with the default FPGA program.

7.5 LEDs for FPGA

Positions	Figure 1-1 (Appearance) D-5 to C-5

The FPGA is connected to LEDs. The LEDs (green) can be lit by any signal thanks to the internal connections of the FPGA. The LEDs are lit when the LED connection pin output of the FPGA is “0”.

The LEDs are not lit while the FPGA is performing initialization, because the LED connection pins are pulled up.

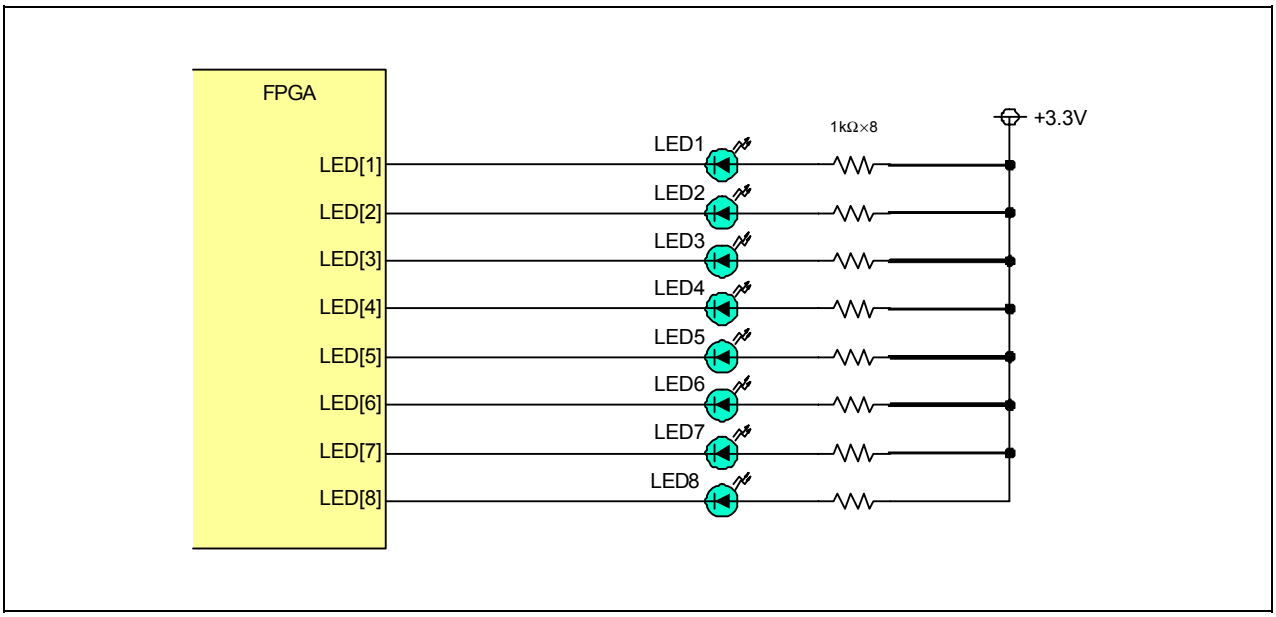
When the FPGA is in the default programming state, the LEDs are inversely connected to port 2 (P20 to P27) of the PFESiP/V850EP1 and all LEDs are lit when the FPGA completes the initialization.

To use these LEDs, set P20 to P27 as output ports using the PM2 register.

Table 7-3. LED Operation with Default Program

SW5	P1 (P10 to P17/INTPZ8 to INTPZ15)
OFF	FFH
ON	00H

Figure 7-4. LED Circuit for FPGA

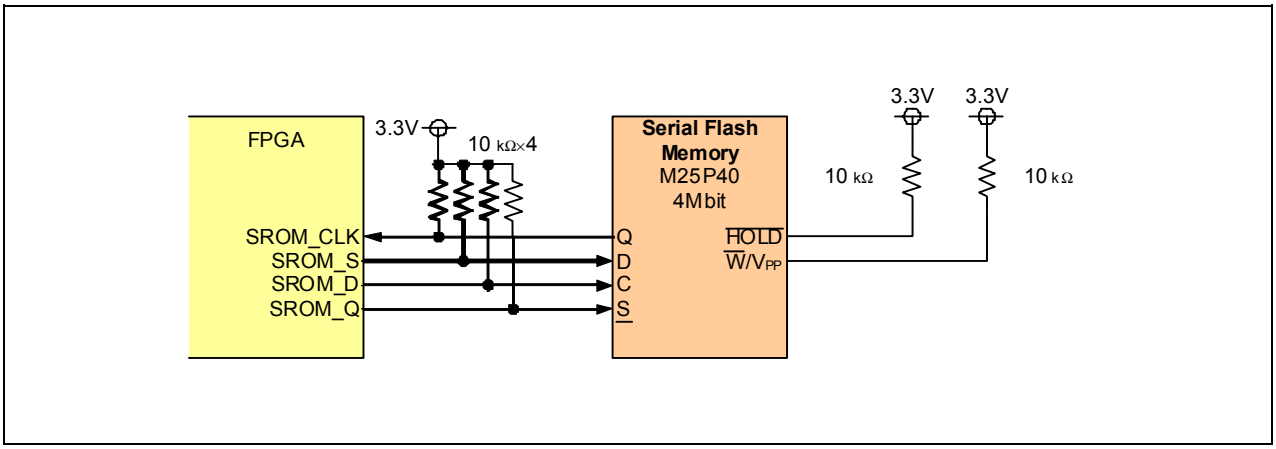


7.6 Serial ROM for FPGA

Position | **Figure 1-1 (Appearance) E-4**

A 4 Mb serial ROM (M25P40) made by STMicroelectronics is connected to the FPGA for various applications using the serial ROM.

Figure 7-5. Serial ROM Connections



Remark Contact STMicroelectronics for how to use the M25P40.

7.7 Connection of FPGA and Expansion Connectors

The general-purpose signals (GPIOn: n = 0 to 79) for external expansion from the FPGA are connected to expansion connectors (general-purpose 50-pin connectors) CN3 and CN4.

See **7.8 FPGA Pin Connections** for details.

7.8 FPGA Pin Connections

The shaded signals ▭ are those used as global clocks.

(1/5)

FPGA Pin Name 1	FPGA Pin Name 2	FPGA Pin Name 3	FPGA BANK	FPGA Pin No.	FPGA Internal Processing	V850EP1 Pin Name 1	V850EP1 Pin Name 2	V850EP1 Pin Name 3	50-Pin Connector (for Port)	50-Pin Connector (for GPIO)	Other
P0[0]	INTPZ[0]	CCC0[0]	B5	G3		P0[0]	INTPZ[0]	CCC0[0]	CN1-2		50K Pull-up
P0[1]	INTPZ[1]	CCC0[1]	B5	H3		P0[1]	INTPZ[1]	CCC0[1]	CN1-3		50K Pull-up
P0[2]	INTPZ[2]	CCC1[0]	B5	J3		P0[2]	INTPZ[2]	CCC1[0]	CN1-4		50K Pull-up
P0[3]	INTPZ[3]	CCC1[1]	B5	K3		P0[3]	INTPZ[3]	CCC1[1]	CN1-5		50K Pull-up
P0[4]	INTPZ[4]	CCC2[0]	B5	J2		P0[4]	INTPZ[4]	CCC2[0]	CN1-7		50K Pull-up
P0[5]	INTPZ[5]	CCC2[1]	B5	K2		P0[5]	INTPZ[5]	CCC2[1]	CN1-8		50K Pull-up
P0[6]	INTPZ[6]	CCC3[0]	B5	L2		P0[6]	INTPZ[6]	CCC3[0]	CN1-9		50K Pull-up
P0[7]	INTPZ[7]	CCC3[1]	B5	E3		P0[7]	INTPZ[7]	CCC3[1]	CN1-10		50K Pull-up
P1[0]	INTPZ[8]	CC0[0]	B5	K6		P1[0]	INTPZ[8]	CC0[0]	CN1-12		50K Pull-up
P1[1]	INTPZ[9]	CC0[1]	B5	J7		P1[1]	INTPZ[9]	CC0[1]	CN1-13		50K Pull-up
P1[2]	INTPZ[10]	CC1[0]	B5	L7		P1[2]	INTPZ[10]	CC1[0]	CN1-14		50K Pull-up
P1[3]	INTPZ[11]	CC1[1]	B6	N1		P1[3]	INTPZ[11]	CC1[1]	CN1-15		50K Pull-up
P1[4]	INTPZ[12]		B5	F1		P1[4]	INTPZ[12]		CN1-17		50K Pull-up
P1[5]	INTPZ[13]		B5	G1		P1[5]	INTPZ[13]		CN1-18		50K Pull-up
P1[6]	INTPZ[14]		B5	H1		P1[6]	INTPZ[14]		CN1-19		50K Pull-up
P1[7]	INTPZ[15]		B5	K1		P1[7]	INTPZ[15]		CN1-20		LAN circuit, 1K pull-up
P2[0]	INTPZ[16]		B4	B6		P2[0]	INTPZ[16]				
P2[1]	INTPZ[17]		B4	B5		P2[1]	INTPZ[17]				
P2[2]	INTPZ[18]		B4	C5		P2[2]	INTPZ[18]				
P2[3]	INTPZ[19]		B4	D5		P2[3]	INTPZ[19]				
P2[4]	INTPZ[20]		B4	A6		P2[4]	INTPZ[20]				
P2[5]	INTPZ[21]		B4	H7		P2[5]	INTPZ[21]				
P2[6]	INTPZ[22]		B5	J8		P2[6]	INTPZ[22]				
P2[7]	INTPZ[23]		B4	A5		P2[7]	INTPZ[23]				
P4[0]	TI[0]		B5	H4		P4[0]	TI[0]		CN1-32		50K Pull-up
P4[1]	TI[1]		B5	K4		P4[1]	TI[1]		CN1-33		50K Pull-up
P4[2]	TI[2]		B5	F5		P4[2]	TI[2]		CN1-34		50K Pull-up
P4[3]	TI[3]		B5	G5		P4[3]	TI[3]		CN1-35		50K Pull-up
P4[4]	TCLR[0]		B5	H5		P4[4]	TCLR[0]		CN1-37		50K Pull-up
P4[5]	TCLR[1]		B5	J5		P4[5]	TCLR[1]		CN1-38		50K Pull-up
P4[6]	TCLR[2]		B5	K5		P4[6]	TCLR[2]		CN1-39		50K Pull-up
P4[7]	TCLR[3]		B5	G6		P4[7]	TCLR[3]		CN1-40		50K Pull-up
P5[0]	TO[0]		B5	L3		P5[0]	TO[0]		CN1-42		50K Pull-up
P5[1]	TO[1]		B5	E4		P5[1]	TO[1]		CN1-43		50K Pull-up
P5[2]	TO[2]		B5	F4		P5[2]	TO[2]		CN1-44		50K Pull-up
P5[3]	TO[3]		B5	G4		P5[3]	TO[3]		CN1-45		50K Pull-up
P5[4]	ETIUD[0]		B6	R1		P5[4]	ETIUD[0]		CN1-47		50K Pull-up
P5[5]	ETIUD[1]		B6	T1		P5[5]	ETIUD[1]		CN1-48		50K Pull-up
P5[6]	ETCUD[0]		B6	U1		P5[6]	ETCUD[0]		CN1-49		50K Pull-up
P5[7]	ETCUD[1]		B6	V1		P5[7]	ETCUD[1]		CN1-50		50K Pull-up
P6[0]	A[20]		B2	F22		P6[0]	A[20]		CN2-3		FROM
P6[1]	A[21]		B2	F19		P6[1]	A[21]		CN2-4		FROM
P6[2]	A[22]		B2	F20		P6[2]	A[22]		CN2-5		FROM
P6[3]	A[23]		B2	E21		P6[3]	A[23]		CN2-7		SDRAM,FROM
P6[4]	A[24]		B2	E22		P6[4]	A[24]		CN2-8		SDRAM
P6[5]	A[25]		B2	E19		P6[5]	A[25]		CN2-9		
P6[6]	A[0]		B2	E20		P6[6]	A[0]		CN2-10		
P6[7]	A[1]		B2	F21		P6[7]	A[1]		CN2-12		LAN circuit, SDRAM, FROM

(2/5)

FPGA Pin Name 1	FPGA Pin Name 2	FPGA Pin Name 3	FPGA BANK	FPGA Pin No.	FPGA Internal Processing	V850EP1 Pin Name 1	V850EP1 Pin Name 2	V850EP1 Pin Name 3	50-Pin Connector (for Port)	50-Pin Connector (for GPIO)	Other
P7[0]	WAITZ		B2	G18		P7[0]	WAITZ				
P7[1]	CSZ[1]		B2	H22		P7[1]	CSZ[1]				SW4-1
P7[2]	CSZ[2]		B2	J18		P7[2]	CSZ[2]				
P7[3]	CSZ[3]		B2	J19		P7[3]	CSZ[3]				SW4-2
P7[4]	CSZ[4]		B2	J20		P7[4]	CSZ[4]				SW4-3
P7[6]	CSZ[6]		B2	K18		P7[6]	CSZ[6]				LAN circuit, SW44
BUSCLK			B3	C13			BUSCLK		CN2-2		Test pin, SDRAM
P8[0]	IOWRZ		B2	K20		P8[0]	IOWRZ				
P8[1]	IORDZ		B2	K21		P8[1]	IORDZ				
P8[2]	HLDAKZ		B2	K22		P8[2]	HLDAKZ				
P8[3]	HLDRQZ		B2	L20		P8[3]	HLDRQZ				
P8[4]	REFRQZ		B2	L21		P8[4]	REFRQZ				
P8[5]	SELFREFZ		B1	N16		P8[5]	SELFREFZ				
P11[0]	ETCLR[0]		B6	W1		P11[0]	ETCLR[0]		CN2-13		50K Pull-up
P11[1]	ETCLR[1]		B6	Y1		P11[1]	ETCLR[1]		CN2-14		50K Pull-up
P11[2]	ETO[0]		B6	N2		P11[2]	ETO[0]		CN2-15		50K Pull-up
P11[3]	ETO[1]		B6	P2		P11[3]	ETO[1]		CN2-17		50K Pull-up
P12[0]	TCZ[0]		B1	T17		P12[0]	TCZ[0]		CN2-18		
P12[1]	TCZ[1]		B1	U17		P12[1]	TCZ[1]		CN2-19		
P12[4]	DMAAKZ[0]		B1	P18		P12[4]	DMAAKZ[0]		CN2-20		
P12[5]	DMAAKZ[1]		B1	P19		P12[5]	DMAAKZ[1]		CN2-21		
P13[0]	DMARQZ[0]		B1	P16		P13[0]	DMARQZ[0]		CN2-23		
P13[1]	DMARQZ[1]		B1	R16		P13[1]	DMARQZ[1]		CN2-24		
P14[0]	SCK[0]		B5	C2		P14[0]	SCK[0]		CN2-25		
P14[1]	SI[0]		B5	D2		P14[1]	SI[0]		CN2-27		
P14[2]	SO[0]		B5	E2		P14[2]	SO[0]		CN2-28		
P14[3]	SCK[1]		B5	F2		P14[3]	SCK[1]		CN2-29		
P14[4]	SI[1]		B5	G2		P14[4]	SI[1]		CN2-30		
P14[5]	SO[1]		B5	H2		P14[5]	SO[1]		CN2-32		
P14[6]	PWMO[0]		B5	J6		P14[6]	PWMO[0]		CN2-33		
P14[7]	PWMO[1]		B5	K7		P14[7]	PWMO[1]		CN2-34		
NMI_OUT			B1	R18			NMI				
SDMARQZ[0]			B4	E6			SDMARQZ[0]				
SDMARQZ[1]			B4	A7			SDMARQZ[1]				
SDMAAKZ[0]			B4	B7	Pull-up		SDMAAKZ[0]				
SDMAAKZ[1]			B4	C7	Pull-up		SDMAAKZ[1]				
STCZ[0]			B4	C6	Pull-up		STCZ[0]				
STCZ[1]			B4	D6	Pull-up		STCZ[1]				
SCSZ[0]			B4	E10			SCSZ[0]				
SCSZ[1]			B4	B11			SCSZ[1]				
SCSZ[2]			B4	C11			SCSZ[2]				
SCSZ[3]			B4	B12			SCSZ[3]				
SA[0]			B3	A17			SA[0]				
SA[1]			B3	B17			SA[1]				
SA[2]			B3	E15			SA[2]				
SA[3]			B3	A16			SA[3]				
SA[4]			B3	B16			SA[4]				
SA[5]			B3	C16			SA[5]				
SA[6]			B3	A15			SA[6]				
SA[7]			B3	B15			SA[7]				
SA[8]			B3	C15			SA[8]				

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FPGA Pin Name 1	FPGA Pin Name 2	FPGA Pin Name 3	FPGA BANK	FPGA Pin No.	FPGA Internal Processing	V850EP1 Pin Name 1	V850EP1 Pin Name 2	V850EP1 Pin Name 3	50-Pin Connector (for Port)	50-Pin Connector (for GPIO)	Other
SA[9]			B3	D15			SA[9]				
SA[10]			B3	C14			SA[10]				
SA[11]			B3	D14			SA[11]				
SA[12]			B3	E14			SA[12]				
SA[13]			B4	F9			SA[13]				
SA[14]			B4	G7			SA[14]				
SA[15]			B4	G8			SA[15]				
SA[16]			B4	G9			SA[16]				
SA[17]			B4	C12			SA[17]				
SA[18]			B4	F6			SA[18]				
SA[19]			B4	F7			SA[19]				
SA[20]			B4	F8			SA[20]				
SD[0]			B2	C22			SD[0]				
SD[1]			B3	F13			SD[1]				
SD[2]			B3	F14			SD[2]				
SD[3]			B3	F15			SD[3]				
SD[4]			B3	F16			SD[4]				
SD[5]			B3	G13			SD[5]				
SD[6]			B3	G14			SD[6]				
SD[7]			B3	G15			SD[7]				
SD[8]			B3	G16			SD[8]				
SD[9]			B2	J16			SD[9]				
SD[10]			B2	K16			SD[10]				
SD[11]			B2	L16			SD[11]				
SD[12]			B2	G17			SD[12]				
SD[13]			B2	H17			SD[13]				
SD[14]			B2	J17			SD[14]				
SD[15]			B2	K17			SD[15]				
SRDZ			B2	C21			SRDZ				
SWRZ[0]	SBENZ[0]		B3	B18			SWRZ[0]	SBENZ[0]			
SWRZ[1]	SBENZ[1]		B3	C18			SWRZ[1]	SBENZ[1]			
SIOWRZ			B4	C8			SIOWRZ				
SIORDZ			B4	D8			SIORDZ				
SWRSTBZ			B3	A18			SWRSTBZ				
SWAITZ			B4	E7			SWAITZ				
SHLDRQZ			B4	A8			SHLDRQZ				
SHLDAKZ			B4	B8			SHLDAKZ				
SBCYSTZ			B3	C17			SBCYSTZ				
SBUSCLK			B3	A13			SBUSCLK				
SREFRQZ			B4	E8			SREFRQZ				
SRESTOZ			B4	E9			SRESTOZ				
UCLKSEL[0]			B6	R2			UCLKSEL[0]				
UCLKSEL[1]			B6	T2			UCLKSEL[1]				1K Pull-down
IROMEN			B1	R19			IROMEN				
VBCLKEN			B5	C1			VBCLKEN				50K Pull-down
VSBRAMEN			B2	D22			VSBRAMEN				50K Pull-up
BOOTSEL			B2	D21			BOOTSEL				50K Pull-up
MODE[0]			B5	D1			MODE[0]				50K Pull-up
MODE[1]			B5	E1			MODE[1]				50K Pull-up
FRESETZ			B6	W2							To reset circuit
NMI_IN			B1	R21							SW_NMI circuit
SW_INTP[7]			B1	R22							SW_INTP7 circuit

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FPGA Pin Name 1	FPGA Pin Name 2	FPGA Pin Name 3	FPGA BANK	FPGA Pin No.	FPGA Internal Processing	V850EP1 Pin Name 1	V850EP1 Pin Name 2	V850EP1 Pin Name 3	50-Pin Connector (for Port)	50-Pin Connector (for GPIO)	Other
SROM_CLK			B1	T18							SROM, 10K Pull-up
SROM_D			B1	T19							SROM, 10K Pull-up
SROM__S			B1	T20							SROM, 10K Pull-up
SROM_Q			B1	T21							SROM, 10K Pull-up
LED[1]			B1	T22							LED1
LED[2]			B1	U18							LED2
LED[3]			B1	U19							LED3
LED[4]			B1	U20							LED4
LED[5]			B1	U21							LED5
LED[6]			B1	U22							LED6
LED[7]			B1	V18							LED7
LED[8]			B1	V19							LED8
DIP_[1]			B1	V21	Pull-up						SW5-1
DIP_[2]			B1	V22	Pull-up						SW5-2
DIP_[3]			B1	W19	Pull-up						SW5-3
DIP_[4]			B1	W20	Pull-up						SW5-4
DIP_[5]			B1	W21	Pull-up						SW5-5
DIP_[6]			B1	W22	Pull-up						SW5-6
DIP_[7]			B1	Y21	Pull-up						SW5-7
DIP_[8]			B1	Y22	Pull-up						SW5-8
EX_CLK			B8	AB13							OSC4 (not mounted)
GPIO[0]			B6	Y2						CN3-2	
GPIO[1]			B6	P3						CN3-3	
GPIO[2]			B6	R3						CN3-4	
GPIO[3]			B6	T3						CN3-5	
GPIO[4]			B6	V3						CN3-7	
GPIO[5]			B6	W3						CN3-8	
GPIO[6]			B6	R4						CN3-9	
GPIO[7]			B6	T4						CN3-10	
GPIO[8]			B6	U4						CN3-12	
GPIO[9]			B6	V4						CN3-13	
GPIO[10]			B6	W4						CN3-14	
GPIO[11]			B6	P5						CN3-15	
GPIO[12]			B6	R5						CN3-17	
GPIO[13]			B6	T5						CN3-18	
GPIO[14]			B6	U5						CN3-19	
GPIO[15]			B6	P6						CN3-20	
GPIO[16]			B6	R6						CN3-22	
GPIO[17]			B6	T6						CN3-23	
GPIO[18]			B6	N7						CN3-24	
GPIO[19]			B6	P7						CN3-25	
GPIO[20]			B6	R7						CN3-27	
GPIO[21]			B7	T10						CN3-28	
GPIO[22]			B7	T7						CN3-29	
GPIO[23]			B7	T8						CN3-30	
GPIO[24]			B7	T9						CN3-32	
GPIO[25]			B7	U10						CN3-33	
GPIO[26]			B7	U6						CN3-34	
GPIO[27]			B7	U7						CN3-35	

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FPGA Pin Name 1	FPGA Pin Name 2	FPGA Pin Name 3	FPGA BANK	FPGA Pin No.	FPGA Internal Processing	V850EP1 Pin Name 1	V850EP1 Pin Name 2	V850EP1 Pin Name 3	50-Pin Connector (for Port)	50-Pin Connector (for GPIO)	Other
GPIO[28]			B7	U8						CN3-37	
GPIO[29]			B7	U9						CN3-38	
GPIO[30]			B6	R8						CN3-39	
GPIO[31]			B7	R9						CN3-40	
GPIO[32]			B7	Y5						CN3-42	
GPIO[33]			B7	W5						CN3-43	
GPIO[34]			B7	AB5						CN3-44	
GPIO[35]			B7	AA5						CN3-45	
GPIO[36]			B7	Y6						CN3-47	
GPIO[37]			B7	V6						CN3-48	
GPIO[38]			B7	AB6						CN3-49	
GPIO[39]			B7	AA6						CN3-50	
GPIO[40]			B7	Y7						CN4-2	
GPIO[41]			B7	W7						CN4-3	
GPIO[42]			B7	V7						CN4-4	
GPIO[43]			B7	AB7						CN4-5	
GPIO[44]			B7	AA7						CN4-7	
GPIO[45]			B7	Y8						CN4-8	
GPIO[46]			B7	V8						CN4-9	
GPIO[47]			B7	AB8						CN4-10	
GPIO[48]			B7	AA8						CN4-12	
GPIO[49]			B7	Y10						CN4-13	
GPIO[50]			B7	W10						CN4-14	
GPIO[51]			B7	V10						CN4-15	
GPIO[52]			B7	Y11						CN4-17	
GPIO[53]			B7	AA11						CN4-18	
GPIO[54]			B8	T13						CN4-19	
GPIO[55]			B8	T14						CN4-20	
GPIO[56]			B8	T15						CN4-22	
GPIO[57]			B8	U12						CN4-23	
GPIO[58]			B8	U13						CN4-24	
GPIO[59]			B8	U14						CN4-25	
GPIO[60]			B8	U15						CN4-27	
GPIO[61]			B8	AA12						CN4-28	
GPIO[62]			B8	Y12						CN4-29	
GPIO[63]			B8	Y13						CN4-30	
GPIO[64]			B8	W13						CN4-32	
GPIO[65]			B8	V13						CN4-33	
GPIO[66]			B8	Y14						CN4-34	
GPIO[67]			B8	W14						CN4-35	
GPIO[68]			B8	V14						CN4-37	
GPIO[69]			B8	AB15						CN4-38	
GPIO[70]			B8	AA15						CN4-39	
GPIO[71]			B8	Y15						CN4-40	
GPIO[72]			B8	W15						CN4-42	
GPIO[73]			B8	V15						CN4-43	
GPIO[74]			B8	AB16						CN4-44	
GPIO[75]			B8	AA16						CN4-45	
GPIO[76]			B8	Y16						CN4-47	
GPIO[77]			B8	Y17						CN4-48	
GPIO[78]			B8	AB17						CN4-49	
GPIO[79]			B8	AA17						CN4-50	

CHAPTER 8 OTHER FUNCTIONS

8.1 Various LEDs

8.1.1 USB host port LEDs (LED9, LED10)

Position **Figure 1-1 (Appearance) A-2**

These LEDs indicate that the power of the two USB host ports is turned on. They glow red when the power is turned on.

USB Host Port	LED No.	Coordinates	Connector Stage
Port 0	LED9 (USB0) (red)	A-2	Lower stage
Port 1	LED10 (USB1) (red)	A-3	Upper stage

8.1.2 LED for FPGA DONE (LED11)

Position **Figure 1-1 (Appearance) A-6**

LED11 State	Configuration State
Lit (red)	During configuration
Turned off	Configuration completed

This LED indicates the configuration state of the FPGA.
It glows red during the configuration and is turned off when the configuration is completed.

8.1.3 Power supply LED (LED15)

Position **Figure 1-1 (Appearance) E-2**

Normally, the PFESiP EP-1 evaluation board is operated by supplying a single +5 V power supply.
LED15 glows blue when a +5 V is supplied.

LED15 State	Power Supply State
Lit (blue)	On
Turned off	Off

8.2 On-Chip Serial Interface (USB Conversion Circuit)

Position | **Figure 1-1 (Appearance) A-4**

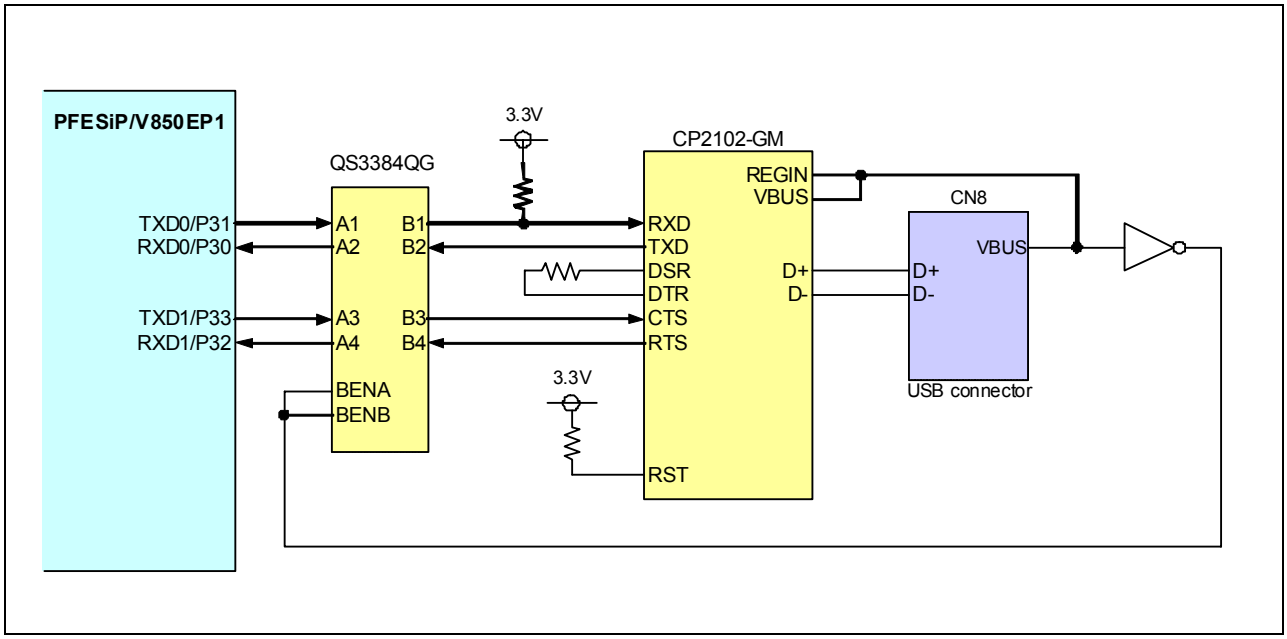
Only one channel of the on-chip asynchronous serial interface (UART) of the PFESiP/V850EP1 is converted to the USB mini B connector (CN8) using the UART and USB bridge IC (CP2102) made by Silicon Laboratories and mounted on-board.

The CP2102 driver is supplied by Silicon Laboratories (device manufacturer) free of license.

The latest drivers supporting various OSs can be downloaded from the following Silicon Laboratories Web site.

https://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx

Figure 8-1. USB Mini B Connector UART Conversion

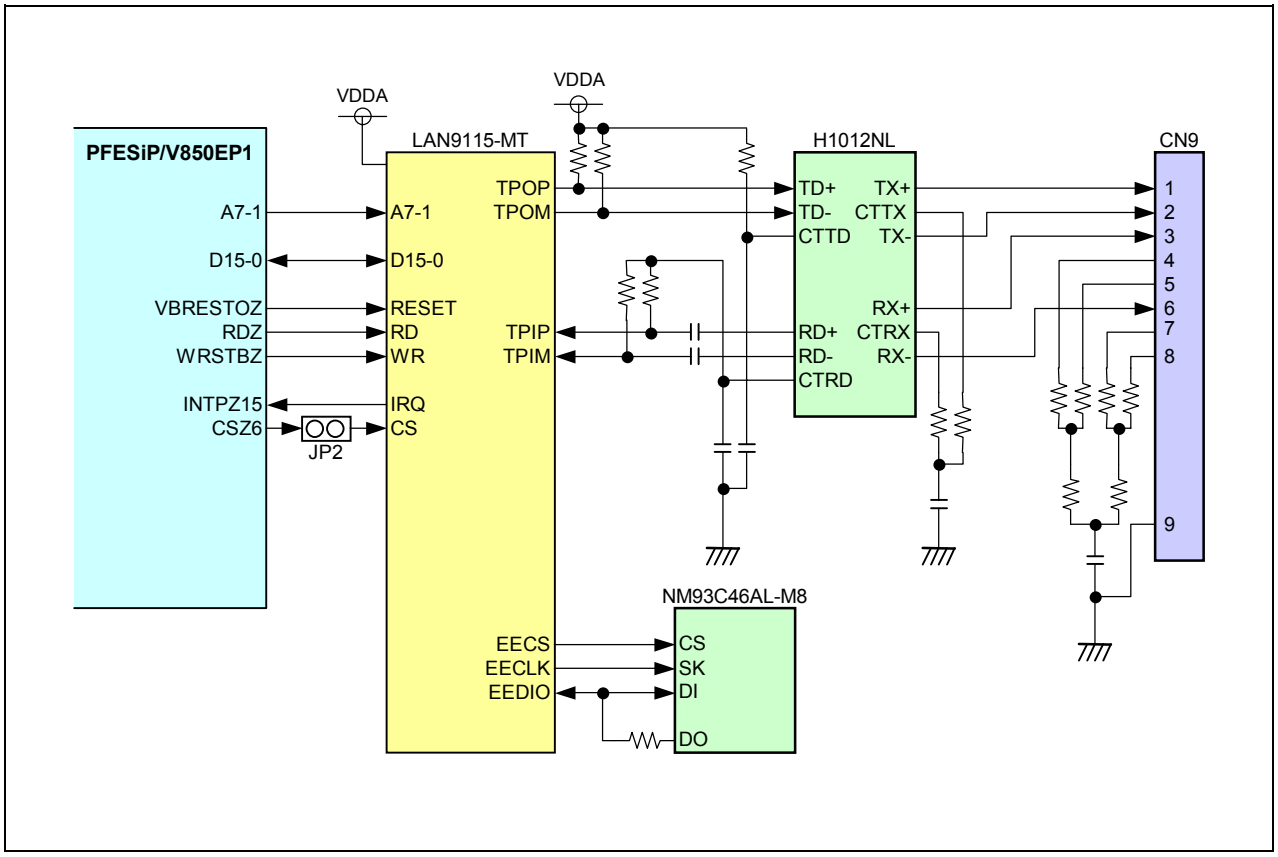


8.3 External LAN Interface (LAN9115)

Positions **Figure 1-1 (Appearance) A-4 to A-5**

A LAN interface is provided by connecting a LAN9115 chip made by SMSC to the on-chip memory controller bus of the PFESiP/V850EP1.

Figure 8-2. LAN Interface Circuit



8.4 USB Function

The PFESiP/V850EP1 has an on-chip USB function controller and a USB host controller, both conforming to the Universal Serial Bus Specification.

- USB function controller:
  Supports 12 Mbps (full-speed) transfer
  Provided with 1-ch upstream ports
  Incorporates the following end points for transfer

End Point Name	FIFO Size (Bytes)	Transfer Type	Remark
EP0	64	Control Read/Write	
EP1	64×2	Bulk In	Double-buffer configuration
EP2	64×2	Bulk Out	Double-buffer configuration
EP7	8	Interrupt	

Bulk-in/-out data can be transferred by DMA transfer (2-clock transfer).

- USB host controller:
  Supports 12 Mbps (full-speed) and 1.5 Mbps (low-speed) transfer
  Supports OHCI (open host controller interface) 1.0a
  (The control for transitioning the disabled state of the USB port to the enabled state is restricted.)
  Incorporates a 2-ch root hub function and is provided with two downstream ports
  Uses an 8 KB on-chip SRAM and external SDRAM as shared memories

8.4.1 Peripheral circuit of USB function controller

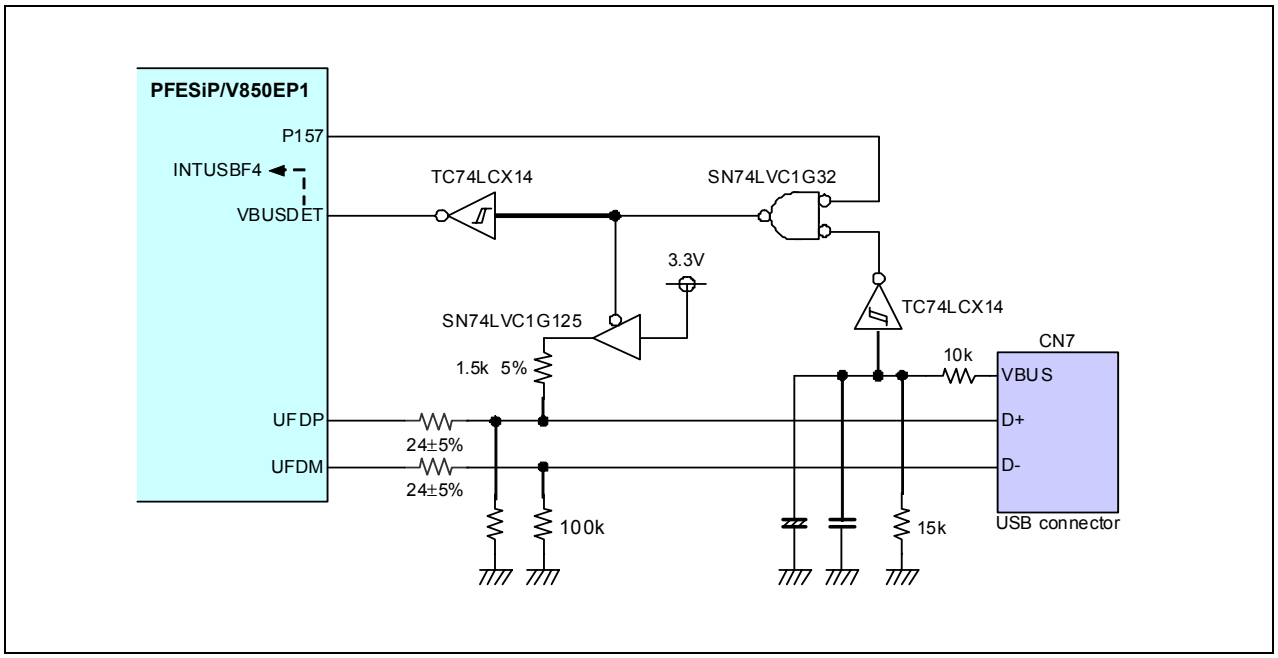
Position **Figure 1-1 (Appearance) A-3**

Resistors of 24 Ω ±5% are connected in series in the vicinity of the D+/D– pins (UFDP, UFDM) of the USB function controller of the PFESiP/V850EP1. The D+ pin (UFDP) is pulled up to 3.3 V at 1.5 kΩ ±5%, because the USB function controller of the PFESiP/V850EP1 supports full-speed (FS) transfer.

VBUS detection is performed using the VBUSDET pin. VBUS detection using the VBUSDET pin can be performed only when low level is output from P157. Pulling up the D+ pin (UFDP) is valid when high level is input to the VBUSDET pin.

The D+/ D– pins are pulled down at 100 kΩ to prevent a floating state of the pins when they are initialized or unused.

Figure 8-3. Peripheral Circuit of USB Function Controller



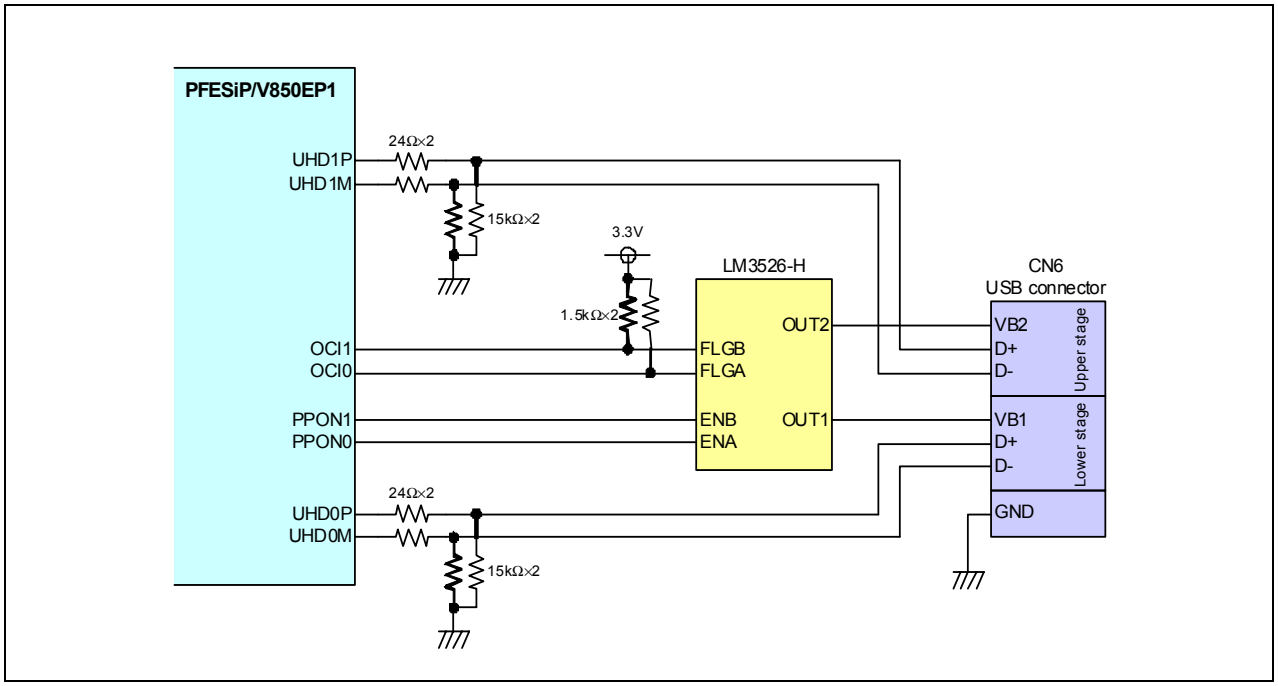
8.4.2 Peripheral circuit of USB host controller

Position **Figure 1-1 (Appearance) A-3**

Resistors of 24 Ω ±5% are connected in series in the vicinity of the D+/ D− pins (UHD0P, UHD0M, UHD1P, UHD1M) of the USB host controller of the PFESiP/V850EP1. The pins are pulled down to GND at 15 kΩ ±5%.

The dual-port USB power switch with overcurrent protection (LM3526) is used as the power switch of the host controller.

Figure 8-4. Peripheral Circuit of USB Host Controller



8.4.3 USB host port LEDs (LED9, LED10)

Position **Figure 1-1 (Appearance) A-2**

These LEDs indicate that the power of the two USB host ports is turned on. They glow red when the power is turned on.

USB Host Port	LED No.	Coordinates	Connector Stage
Port 0	LED9 (USB0) (red)	A-2	Lower stage
Port 1	LED10 (USB1) (red)	A-3	Upper stage

Caution If the LEDs are lit and turned off immediately when the power of the USB host ports is turned on, a reset may be effected for the system. This is because a device with a load capacitance of at least the assumed amount is connected to the USB host ports and the AC adapter cannot supply enough power, in which case using the AC adapter should be stopped and stable power should be supplied by an external power supply by using the CN12 terminal. The assumed load is about that when connecting a USB hub with a power supply to each port.

8.5 Manipulation Switches

8.5.1 Reset switch

Position	Figure 1-1 (Appearance) E-6

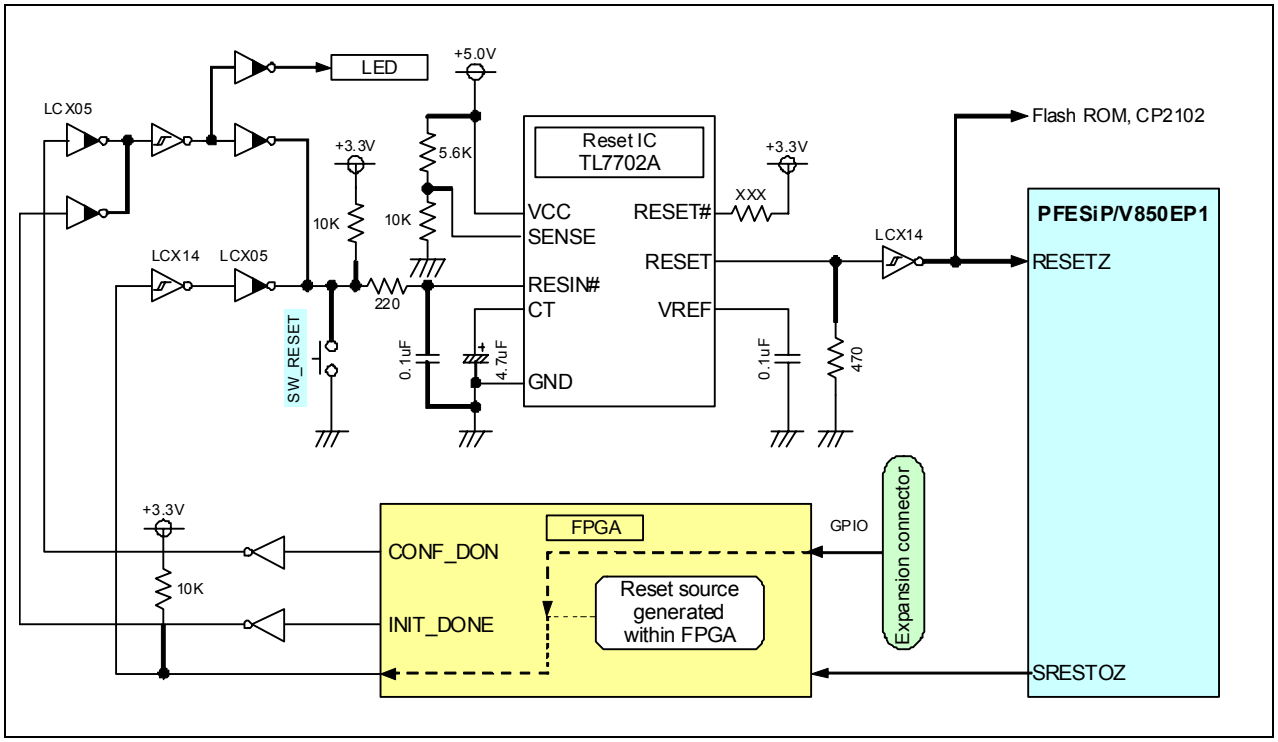
SW_RESET (RESETZ) is provided for reset purposes of the PFESiP/V850EP1.

SW_RESET is provided as a momentary-type toggle switch. The oscillation stabilization wait function, PLL lock wait function, and the reset functions required for clearing the pipeline are incorporated in the PFESiP/V850EP1. The PFESiP/V850EP1 starts waiting for oscillation stabilization when the reset input is released. The PFESiP/V850EP1 enters the reset state also when the FPGA is being configured.

This reset signal is also supplied to the flash ROM and CPLD3 that manages the flash ROM bank.

RESETZ can be manipulated via the FPGA in addition to manipulation with a switch. Manipulation via the FPGA must be performed with the all the switches turned off.

Figure 8-5. Power-on-Reset Switch



8.5.2 Interrupt switches

Position	Figure 1-1 (Appearance) E-5

NMI (SW_NMI) and INTPZ7 (SW_INTP7) are on-board push switches with a built-in chattering prevention circuit.
These switches operate when the on-board large-capacity FPGA is in the default programming state.
When the switches are not pressed, high level is output to the PFESiP/V850EP1.
When the switches are pressed, low level is output to the PFESiP/V850EP1.

SW_NMI, SW_INTP7	PFESiP/V850EP1 Input
Normal	High-level input
Pressed	Low-level input

Make sure that all interrupt request flags are cleared in the initialization program, because an interrupt request flag will be set during booting if the internal initialization of when the power is turned on is earlier than the rise of the chattering prevention circuit power supply.

Caution To use NMI and INTPZ7 when rewriting the contents of the on-board FPGA, add the processing of NMI and INTPZ7 to the FPGA data.

APPENDIX A DIFFERENCES FROM PFESiP EP-1 Evaluation Board

(1/2)

Item	PFESiP EP-1 Evaluation Board	PFESiP EP-1 Evaluation Board Lite
On-board memory		
Flash ROM	16 MB, Toshiba TC58FVM7B5BTG65 Any CSZ selectable using SW14, boot switching, write protection selectable using SW_FWP, BUSY pin controllable	8 MB, Spansion S29JL064H70TFI000H CSZ0 connection fixed, no boot switching, write enabling fixed, BUSY pin not controllable
SRAM	4 MB/2 MB (bus width dependent) NEC Electronics μPD4416016G5-A15 Any CSZ selectable using SW7	None
32-bit width connection SDRAM	64 MB, MICRON MT48LC16M16A2TG-7E Any CSZ selectable using SW6	None
16-bit width connection SDRAM	32 MB, MICRON MT48LC16M16A2TG-7E Any CSZ selectable using SW9	32 MB, MICRON MT48LC16M16A2TG-7E Any CSZ selectable using SW4
On-board FPGA related items		
On-board FPGA	Xilinx® Virtex®-4 XC4VLX40FF1148-11 (standard) LX60, LX80, LX100, and LX160 selectable by BTO	Altera Stratix II EP2S15F484C5 No BTO selection
Logic cell	41,472	15,600
On-board RAM	216 KB	52 KB
Usable GPIO	287 pins	80 pins
Design tool	ISE® Foundation	Development using Quartus II Web Edition possible
FPGA connection serial flash ROM	64 Mb STMicroelectronics M25P64	4 Mb STMicroelectronics M25P40
FPGA programming connector	For platform cable USB: CN5	Active Serial Configuration Interface dedicated to ByteBlaster II/USB Blaster Download Cable: CN10, JTAG (CN11) not mounted
Connectors		
Expansion connectors		
For system expansion	AMP MICTOR 2-767004-5 receptacle 152 pins×3: CN6, CN7, CN9	None
For stack	AMP MICTOR 5767017-4 plug 152 pins×2: CN13, CN14	None
For V850EP1 port	General-purpose 50 pins×2: CN11, CN12 (80 signals)	General-purpose 50 pins×2: CN1, CN2 (80 signals including analog inputs)
For FPGA GPIO	General-purpose 50 pins×2: CN8, CN10 (80 signals)	General-purpose 50 pins×2: CN3, CN4 (80 signals)
Analog input (AIN)	Jumper inputs (JP9, JP10, JP11) On-board variable resistor connected to AIN6	General-purpose 50-pin CN2 (35 to 50) used
N-Wire (debug I/F)	RTE-NEC/MICTOR38-2K for Midas lab RTE-2000-TP: CN1 8 trace signals supported Separate Mictor adapter required when connecting MINICUBE	KEL 26-pin connector supporting MINICUBE: CN5 Tracing cannot be performed RTE-NEC for Midas lab RTE-2000-TP supported
ROM cable connector	CN4	None
SDRAM bus tracer	CN20	None

(2/2)

Item	PFESiP EP-1 Evaluation Board	PFESiP EP-1 Evaluation Board Lite
USB, LAN, and UART functions		
PFESiP/V850EP1 on-chip USB 2.0 FS function	USB2.0 FS/LS Host×2:JUSB_A1 USB 2.0 FS function (standard B): JUSB_B1	USB2.0 FS/LS Host×2:CN6 USB 2.0 FS function (mini B): CN7
USB clock	48 MHz UCLK externally mounted	Only socket (XT1 selected by default)
LAN interface	None	SMSC LAN9115 on-board LAN controller can be used: CN9 Connected to PFESiP/V850EP1 via external bus interface (can be connected to CSZ6 and disconnected by JP2) INTPZ15 assigned as dedicated interrupt
PFESiP/V850EP1 on-chip UART connector	JSIO1, JSIO2 D-sub 9-pin cross cable×2	Conversion between UART and USB using CP2102-GM USB mini B connector: CN8
Operating mode setting		
CPU operating mode setting	Dip switches (SW1, SW2)	Pin level setting in standard state (Can be changed from FPGA as required)
PLL operating mode setting	Dip switches (SW3, SW4, SW5)	Dip switches (SW1, SW2, SW3)
Clock setting	Dip switch (SW5)	Dip switch (SW3)
Operating conditions, etc.		
Power supply (AC adapter input)	Supplied from CN21 or CN23 by dedicated AC adapter (One can be used for external distribution) Connector for external stabilization power supply DC power supply jack×2 (For AC adapter connection and external distribution)	Supplied from CN13 by dedicated AC adapter (No external distribution function)
Power supply (stabilization power supply input)	CN16 (5V) CN17 (3.3V) CN18 (1.5V)	CN12 (5 V) only Separate supply of 3.3 V and 1.5 V not possible
Specified AC adapter	UIA324-05 made by UNIFIVE, 5 V, 4 A, 240 V supported	UL110-0520 made by UNIFIVE, 5 V, 2 A, up to 120 V
Voltages used	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V	3.3 V, 1.5 V, 1.2 V
Current measurement function	Currents of 3.3 V and 1.5 V measurable with current measurement jumpers JP45 and JP46	None

[MEMO]

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