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RENESAS

User's Manual

PFESiP® EP-1 Evaluation Board

Technical Information

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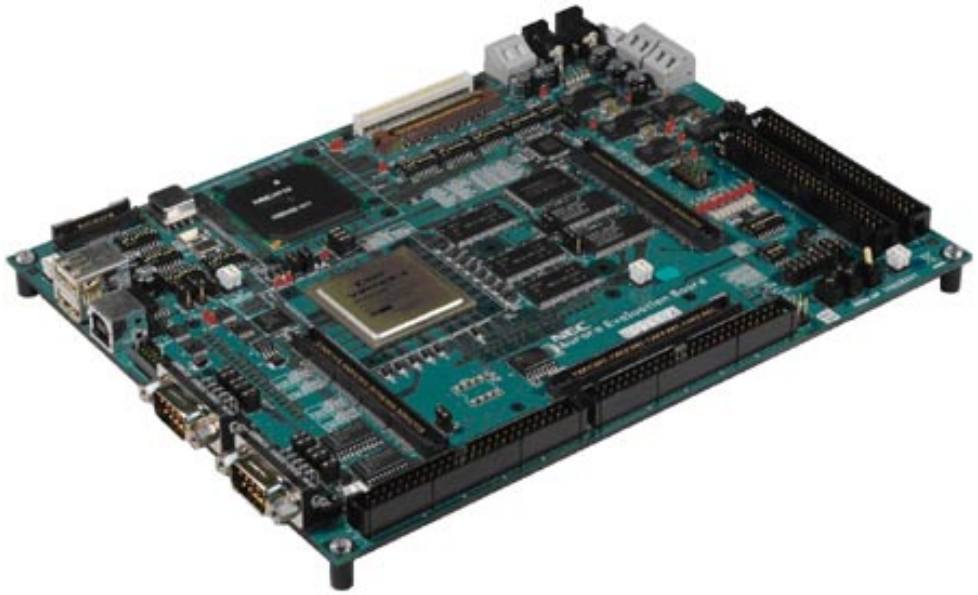
Date published September 2008 NS



NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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PREFACE

Readers This manual is intended for users who understand the functions of the microcontroller function chip with an on-chip V850E2 CPU core (PFESiP/V850EP1) and wish to evaluate developing PFESiP EP-1 Series products using the chip.

Purpose This manual is intended to help users, who wish to evaluate prototyping of PFESiP EP-1 Series products using the PFESiP/V850EP1, understand how to use the development evaluation board.
Using the PFESiP EP-1 Evaluation Board Lite is recommended for users evaluating the introduction of PFESiP EP-1 Series products.

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, microcontrollers, SRAM, page ROM, and SDRAM.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxxZ (Z after pin or signal name)
Note:	Footnote for item marked with Note in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Prefix indicating power of 2	
(address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data type:	Word … 32 bits
	Half-word … 16 bits
	Byte … 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Furthermore, some related documents may be intended for individual customers, because the documents are prepared in the development/planning stage of each core.

Documents Related to PFESiP EP-1 Series

Document Name	Document No.
V850E2 Architecture User's Manual	U17135E
PFESiP EP-1 Series Design Manual	A19068E
PFESiP/V850EP1 Product Data User's Manual	A19069E
PFESiP/V850EP1 Hardware (CPU Function) User's Manual	A19070E
PFESiP/V850EP1 Hardware (USB Function) User's Manual	A19071E
PFESiP/V850EP1 USB Function Sample Sofware Application Note	A19349E

Documents Related to PFESiP EP-1 Evaluation Board

Document Name	Document No.
PFESiP EP-1 Evaluation Board Technical Information User's Manual	This manual
PFESiP EP-1 Evaluation Board Lite Technical Information User's Manual	A19354E

Documents Related to development tools (User's Manual)

Document Name			Document No.
RX850 Pro (Real-time OS)	Ver.3.21	Basics	U18165E
	Ver.3.20	Installation	U17421E
	Ver.3.21	Technical	U18164E
	Ver.3.20	Task Debugger	U17422E
PM+ Ver.6.30 Project Manager			U18416E
QB-V850MINI On-chip Debug Emulator			U17638E
ID850QB Ver.3.20 Integrated Debugger		Operation	U17964E
RX850V4 Ver.4.22 Real-Time OS		Fanctionalities	U16643E
		Task Debugger	U16811E
AZ850V4 Ver.4.10 System Performance Analyzer			U17093J

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CHAPTER 1 INTRODUCTION

The PFESiP EP-1 Evaluation Board is a development evaluation board for assisting the development of PFESiP EP-1 Series products and can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and for user logic development and verification using the on-board FPGA.

The PFESiP/V850EP1 has an on-chip high-performance 32-bit RISC-type CPU core (V850E2 core).

The basic functions of PFESiP EP-1 Series products based on the PFESiP/V850EP1 can be evaluated using this board.

As the on-board FPGA, the Virtex®-4 Family LX Series made by Xilinx is employed and the XC4VLX40 is mounted as standard. The FPGA size can be changed.

For users wishing to evaluate introducing PFESiP EP-1 Series products, the PFESiP EP-1 Evaluation Board Lite, which is a minor version of the PFESiP EP-1 Evaluation Board with less functions, is provided. With the PFESiP EP-1 Evaluation Board Lite, the Stratix® II EP2S15F484C5 (mounting size: about 150 K gates, FPGA not changeable) made by Altera is employed as the on-bard FPGA and the Quartus® II Web Edition can be used. Select a board that is suitable for the purpose of use.

1.1 Overview of PFESiP EP-1 Evaluation Board

The PFESiP EP-1 Evaluation Board is a development evaluation board for assisting the development of PFESiP EP-1 Series products.

It can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and as a PFESiP EP-1 prototyping environment by using the functions of the embedded array (EA-9HD), which is provided with the user logic paired with the PFESiP/V850EP1, for user logic development and verification by the on-board FPGA within the PFESiP EP-1 Series SiP. A more systematic evaluation can be performed by connecting the PFESiP EP-1 Evaluation Board to the user board via an expansion connector. Furthermore, a flash ROM and an SDRAM are provided as on-board memories.

Note that the load capacitance of the PFESiP EP-1 Evaluation Board is not always equivalent, in contrast to the environment of actual SiP products, because the signals originally connected within the SiP are connected to the FPGA on-board.

Remarks 1. The PFESiP EP-1 Evaluation Board is provided with expansion connectors compatible with the MICROSSP Evaluation Board. A stack board developed for the MICROSSP Evaluation Board can also be used for the PFESiP EP-1 Evaluation Board by programming the on-board FPGA.
The MICROSSP® (MICRO Silicon Solution Platform) is a development platform facilitating the development of complex system LSIs with an on-chip CPU core (SoC) and is provided with an evaluation board. A stack board for system expansion, with which the PFESiP EP-1 Evaluation Board is also compatible for use, is also provided. Contact NEC Electronics for details.
(http://www.necel.com/cbic/ja/microssp/board.html)

2. See the **PFESiP/V850EP1 User's Manual** for the functions and specifications of the PFESiP/V850EP1.

1.2 PFESiP EP-1 Evaluation Board Ordering Information

Variations with different FPGA types mounted and provided or not provided with sockets and plugs for stacking can be selected for the PFESiP EP-1 Evaluation Board according to the application. A representative selection of the PFESiP EP-1 Evaluation Board is described below.

1.2.1 FPGA selection

The PFESiP EP-1 Evaluation Board employs the Virtex-4 Family LX Series made by Xilinx as the on-board FPGA. The FF1148 package is employed and an FPGA can be selected from FPGAs with a different capacitance and speed grade, but with a common footprint pattern. The number of I/Os that can be used is the same for any FPGA selected.

The XC4VLX40 is selected as the FPGA mounted as standard. When mounting an FPGA other than the XC4VLX40, conditions regarding the quantity may be added.

1.2.2 Ordering restriction, etc.

(1) Delivery date, etc.

The PFESiP EP-1 Evaluation Board is manufactured on order.
The delivery date is reported to the customer by summing up the approximate time required for procuring the components, manufacturing, evaluation, and packing.

(2) Dedicated AC adapter

An AC adapter dedicated to the PFESiP EP-1 Evaluation Board is optionally provided.
Power can be supplied by using a lead wire from an external stabilization power supply. When wishing to use the dedicated AC adapter, request it optionally.

1.2.3 PFESiP EP-1 Evaluation Board options

The following options can be selected.

Table 1-1. PFESiP EP-1 Evaluation Board Options

Item	Selectable Specifications					
PFESiP/V850EP1 mounting method	☐ Directly mounted (standard)					
	☐ Mounted on socket					
FPGA size	Mounted FPGA	Size of reference circuit, equivalent to CB-IC	Logic cells	Distributed RAM	Block RAM	Number of I/Os
	☐ XC4VLX40	350 K gates	41,472	288 Kb	1,728 Kb	640
	☐ XC4VLX60	500 K gates	59,904	416 Kb	2,880 Kb	
	☐ XC4VLX80	650 K gates	80,640	560 Kb	3.600 Kb	
	☐ XC4VLX100	900 K gates	110,592	768 Kb	4,320 Kb	
	☐ XC4VLX160	1,250 K gates	152,064	1056 Kb	5,184 Kb	
FPGA speed grade	☐ –10 (low speed) ☐ –11 (medium speed: standard specification) ☐ –12 (high speed)					
FPGA mounting method	☐ Directly mounted (standard)					
	☐ Mounted on socket					
MICTOR connector	☐ None		Two 50-pin general-purpose connectors are mounted. In this case, the FPGA connection test is not performed.			
	☐ AMP MICTOR receptacle		AMP MICTOR receptacle is mounted.			
	☐ AMP MICTOR plug		AMP MICTOR plug is mounted (used for stacking the PFESiP EP-1 Evaluation Boards).			
Dedicated AC adapter	☐ None	–				
	☐ Included	Dedicated AC adapter common to MICROSSP Evaluation Board and PFESiP EP-1 Evaluation Board.				

Table 1-2. Standard Specifications of PFESiP EP-1 Evaluation Board

Item	Standard Specifications					
PFESiP/V850EP1 mounting method	■ Directly mounted					
FPGA size	Mounted FPGA	Size of reference circuit, equivalent to CB-IC	Logic cells	Distributed RAM	Block RAM	Number of I/Os
	■ XC4VLX40	350 K gates	41,472	288 Kb	1,728 Kb	640
FPGA speed grade	■ –11 (medium speed)					
FPGA mounting method	■ Directly mounted					
MICTOR connector	■ AMP MICTOR receptacle		AMP MICTOR receptacle is mounted.			
Dedicated AC adapter	■ None	–				

1.2.4 Features

(1) On-board memory

A flash ROM, SRAMs, and SDRAMs which can be directly accessed via the external bus interface (MEMC I/F) of the PFESiP/V850EP1 is mounted on-board and a general memory system is provided.

On-Board Memory Type	Capacity	Connection Bit Width
Flash ROM	16 MB Note	16 bits
SRAM	4 MB/2 MB	32/16 bits (16 bits × 2/16 bits × 1)
SDRAM32	64 MB	32 bits (16 bits × 2)
SDRAM16	32 MB	16 bits (16 bits × 1)

Note A function for dividing the 16 MB ROM into banks can also be used.
The start bank can be selected by using the on-board dip switches.

(2) On-board FPGA

The Xilinx XC4LX40FF1148-10 is mounted in the standard specifications.
The external bus interface (MEMC I/F) of the PFESiP/V850EP1, SiP internal connection bus interface, and almost all signals of the NPB macro I/O pins are connected to the FPGA. The functions of an embedded array to be used in combination with the PFESiP/V850EP1 are performed by this on-board FPGA. In addition, arbitrary signals can be connected via the on-board FPGA, because most system expansion connector signals are connected via the FPGA.
The FPGA can be changed to the FPGAs shown in the following table, which have a common pin layout.
An LED (red) is connected to the DONE signal that indicates that configuring the FPGA has been completed. The LED indicates that the configuration has been started when it is lit and indicates that the configuration has ended when it is turned off.

Mounted FPGA	Size of Reference Circuit Equivalent to CB-IC	Logic Cells	Distributed RAM	Block RAM	Number of I/Os
XC4VLX40	350 K gates	41,472	288 Kb	1,728 Kb	640 Note
XC4VLX60	500 K gates	59,904	416 Kb	2,880 Kb	
XC4VLX80	650 K gates	80,640	560 Kb	3.600 Kb	
XC4VLX100	900 K gates	110,592	768 Kb	4,320 Kb	
XC4VLX160	1,250 K gates	152,064	1056 Kb	5,184 Kb	

Note The XC4VLX80 or higher can use 768 I/Os. With the PFESiP EP-1 Evaluation Board, however, the maximum number of I/Os that can be used is 640 for all devices.

(3) Expansion connectors

Three types of connectors can be equipped, each for a different purpose.
The AMP MICTOR plug is not mounted as standard.

Connector	No. of Valid signals	Purpose	
AMP MICTOR receptacle (152 pins)	CN6 (112) CN7 (110) CN9 (112)	For board stack	For external bus interface (MEMC I/F), on-board FPGA I/Os (UDL pin)
AMP MICTOR plug (152 pins)	CN13 (110) CN14 (112)	For board stack	For on-board FPGA I/Os
General-purpose 50-pin connector	CN8 (40) CN10 (40)	For on-board FPGA I/Os (for low-speed interface)	
	CN11 (39) CN12 (40)	For on-chip peripheral function I/Os of the PFESiP/V850EP1	

Note the stack height when using the AMP MICTOR receptacle or a general-purpose 50-pin connector together with other connectors.

(4) USB 2.0 FS and UART interface

The following general-purpose interfaces are provided by the internal functions of the PFESiP/V850EP1.

Interface Type	Connector	Remark
USB 2.0 FS/LS Host × 2	USB A type (JUSB_A1)	2-port host connector × 1
USB 2.0 FS Function × 1	USB B type (JUSB_B1)	
UART (On-chip UART5 of PFESiP/V850EP1)	DSUB 9 pin (JSIO1, JSIO2)	JSIO1 is selected by JP from UART5_0 and UART5_2. JSIO2 is selected by JP from UART5_1 and UART5_3.

(5) On-board power supply circuit

Both an AC adapter (5 V) and a stabilization power supply are supported (cannot be used together).
The required +3.3 V, +2.5 V, +1.8 V, and +1.5 V power supplies are supplied by the on-board power supply circuit.
The +3.3 V and +1.5 V power supplies of the PFESiP/V850EP1 can be directly supplied from an external stabilization power supply.

(6) Operating mode setting

The various operating modes of the PFESiP/V850EP1 can be set by using the on-board dip switches.
The multiplication and modulation rates of the on-chip SSCG-PLL of the PFESiP/V850EP1 can be set using the dip switches. (Changing the multiplication or modulation rate during operation is not supported.)

(7) On-chip debug function

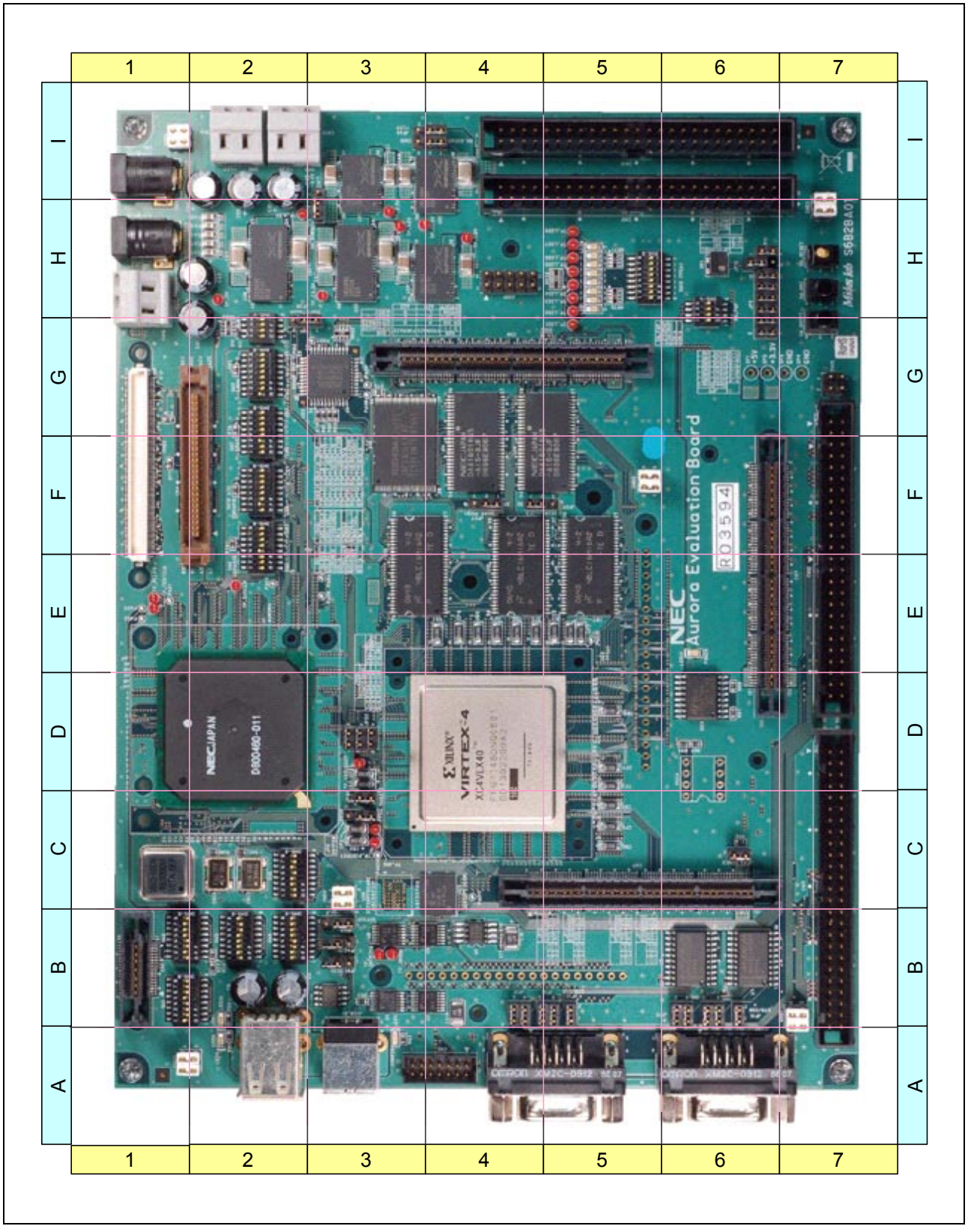
The on-chip debug function performed by the N-Wire interface is supported by the on-chip DCU (debug control unit) of the PFESiP/V850EP1. Eight trace signals are supported.

1.2.5 External view of PFESiP EP-1 Evaluation Board

The external view of the PFESiP EP-1 Evaluation Board is shown below.

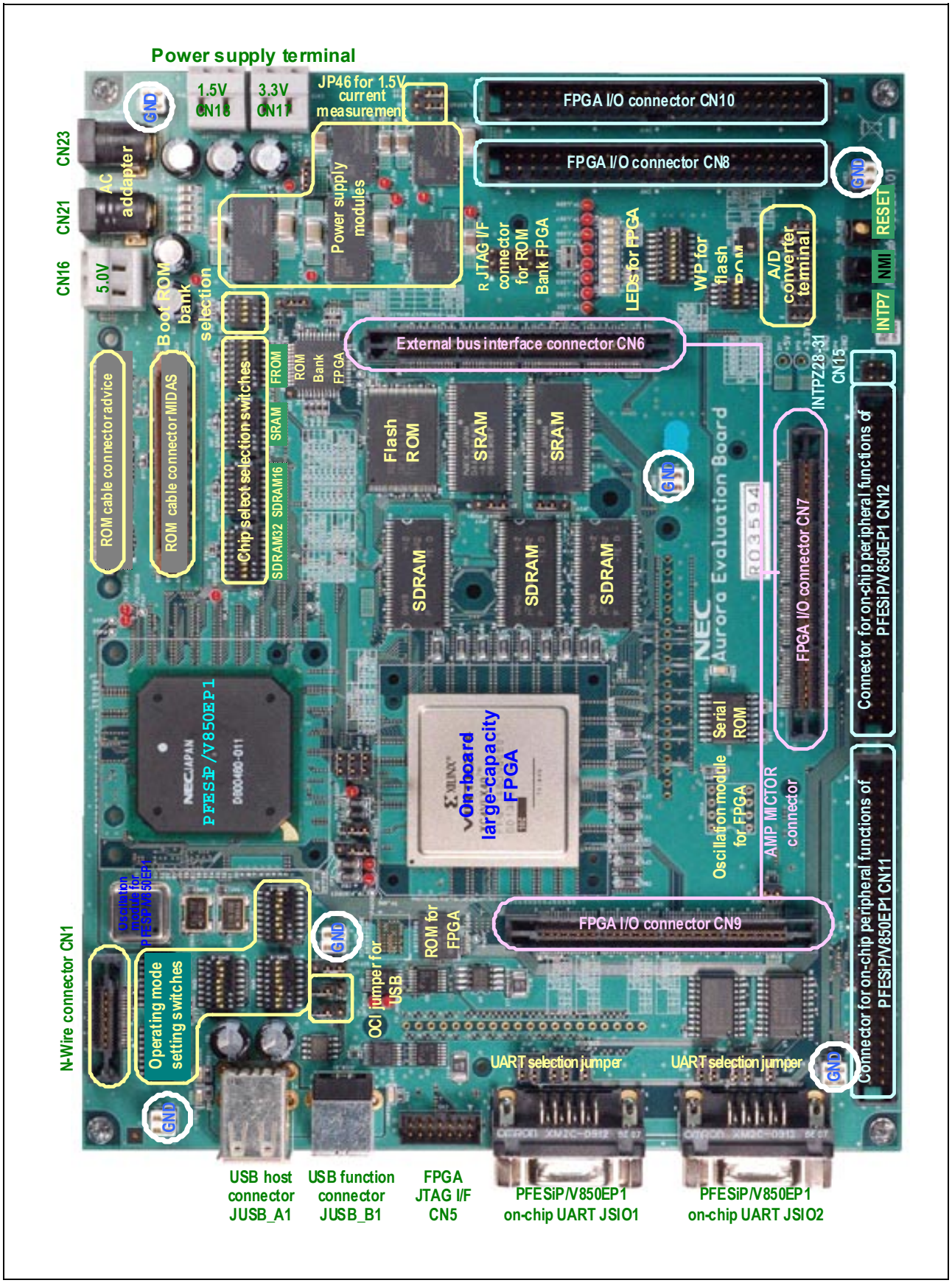
Remark Positions specified on-board in the following pages reference coordinates on the following figure.

Figure 1-1. PFESiP EP-1 Evaluation Board (Appearance)



1.2.6 Function of each part

Figure 1-2. Function of Each Part

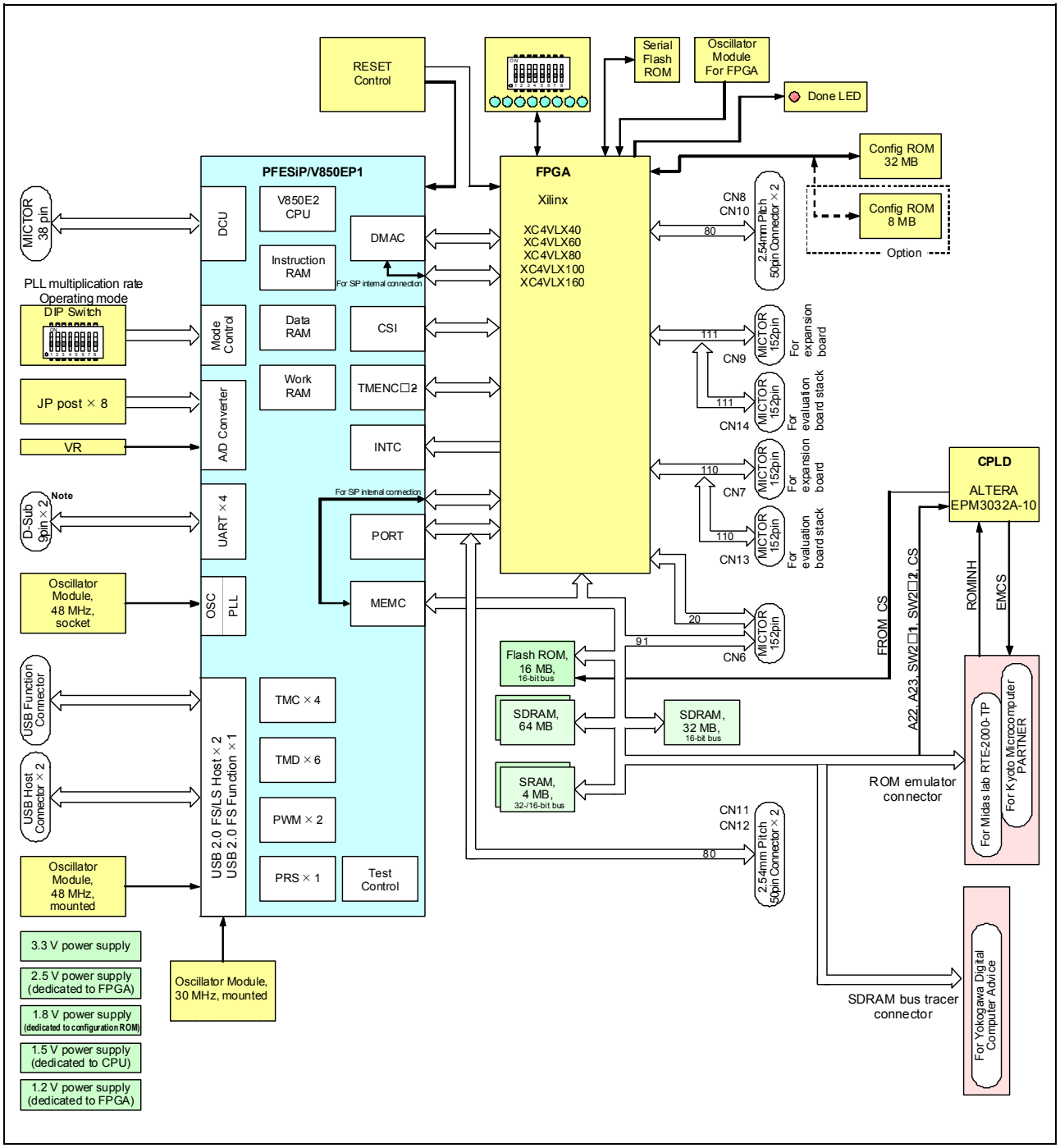


1.2.7 Specifications of PFESiP EP-1 Evaluation Board

Table 1-3. Specifications of PFESiP EP-1 Evaluation Board

Item		Specifications
Maximum operating frequency		
CPU operating frequency		200 MHz
Internal VSB bus frequency		100 MHz
External memory bus		66.7 MHz (C_L = 30 pF)
External memory wait setting		Condition: VBCLK = BUSCLK = 66.7 MHz PFESiP/V850EP1 output delay = 11.0 ns, maximum Wiring delay = 5 ns (to and fro) PFESiP/V850EP1 input delay = 3.8 ns, maximum
Flash ROM TC58FVM7B5BTG65		Address setting wait = 0, idle state = 2, data wait = 4
SRAM μPD4416016G5-A15		Address setting wait = 0, idle state = 1, data wait = 0 or 1
SDRAM (SDRAM32, SDRAM16) MT48LC16M16A2TG-7E		LTC = 0, C_L = 2, idle state = 0, ACTIVE Command to R/W Command = 1
On-board memory and FPGA		
Flash ROM	Any CSZ selected with SW14	16 MB (up to 8 MB can be used simultaneously when connected to CSZ0)
SRAM	Any CSZ selected with SW7	4 M/2 MB (when 32 bits/16 bits)
SDRAM32	Any CSZ selected with SW6	64 MB
SDRAM16	Any CSZ selected with SW9	32 MB
FPGA	Any CSZ selected within FPGA	XC4VLX40FF1148-10 (selected by BTO)
PFESiP/V850EP1 on-chip memory		
On-chip instruction RAM		iLB_RAM: 192 KB
On-chip data RAM		dLB_RAM: 32 KB
On-chip work RAM (disable setting possible)		VSB_RAM: 32 KB
FPGA connection memory		
Flash Serial ROM (for booting)		8 MB (64 Mb)
Connectors		
Expansion connectors		
For expansion board (CN6, 7, 9)		AMP MICTOR 2-767004-5 receptacle (152 pins × 3)
For evaluation board stack (CN13, 14)		AMP MICTOR 5767017-4 plug (152 pins × 2)
General-purpose 50-pin connectors (CN8, 10, 11, 12)		General-purpose 2.54 mm pitch (50 pins × 4)
N-Wire (CN1), 8 traces only		RTE-NEC/MICTOR38-2K for Midas lab RTE-2000-TP
ROM cable connector(CN4)		CBL-STD16-2K for Midas lab RTE-2000-TP
SDRAM bus tracer connector (CN20)		Supports Yokogawa Digital Computer advicePLUS
RS-232C (built into PFESiP/V850EP1 (JSIO1, JSIO2))		D-Sub 9-pin cross cable × 2
FPGA JTAG (CN5)		2.54 mm pitch, 14 pins
PFESiP/V850EP1 on-chip USB 2.0 FS function		USB2.0 FS/LS Host × 2, USB2.0 FS Function
PFESiP/V850EP1 P154-157 output connector (CN15)		2.54 mm pitch general-purpose connector (4 pins)
Operating conditions		
PFESiP/V850EP1 input frequency		Standard 48 MHz
Power supply		+5.0 V supplied from AC adapter (CN21, CN23) or power supply terminal (CN16). EV_{DD} and IV_{DD} of PFESiP/V850EP1 can be directly supplied from external power supply.

1.2.8 Summarized block diagram of PFESiP EP-1 Evaluation Board



Note Channels 0 and 2 are switched by using JP12 and JP14. Channels 1 and 3 are switched by using JP15 and JP17.

1.2.9 Detailed block diagram of PFESiP EP-1 Evaluation Board

Figure 1-3. Detailed Block Diagram of PFESiP EP-1 Evaluation Board (1/2)

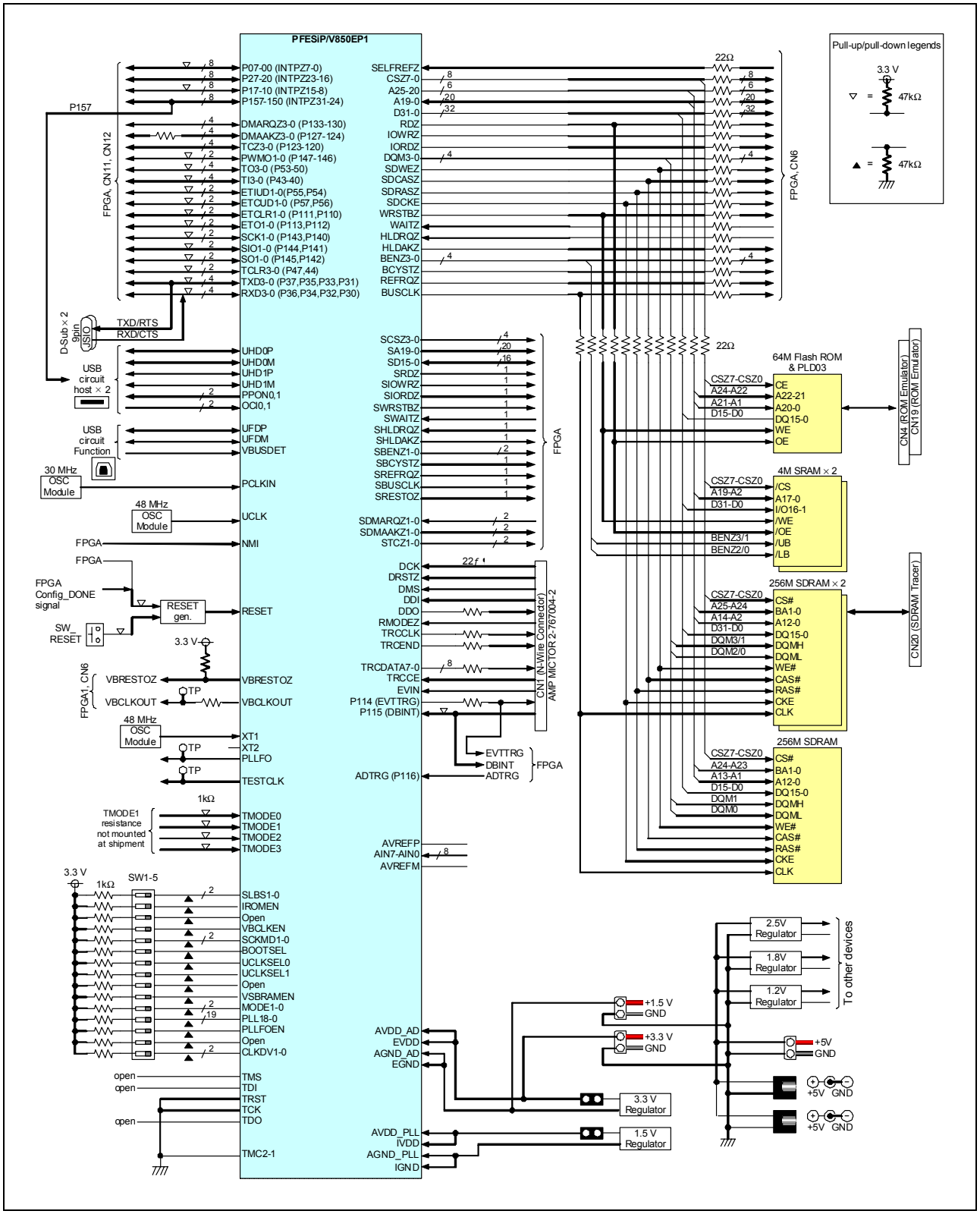
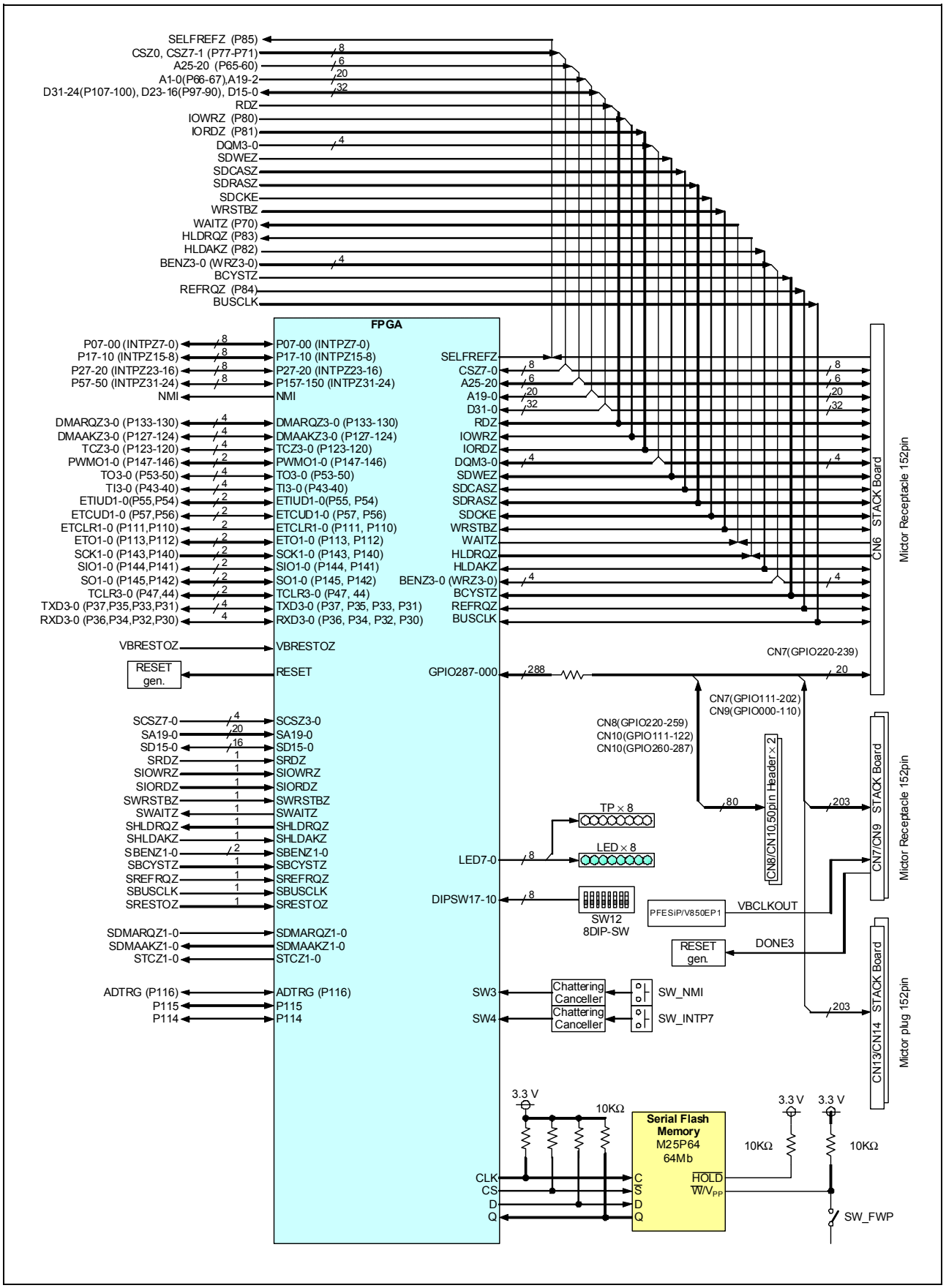


Figure 1-3. Detailed Block Diagram of PFESiP EP-1 Evaluation Board (2/2)



1.2.10 Caution regarding maximum operating frequency of PFESiP/V850EP1

The maximum operating frequency of the PFESiP/V850EP1 differs depending on the operating conditions. CPCLK is an integer multiple of VBCLK and BUSCLK, and VBCLK is equal to or is an integer multiple of BUSCLK. Conditions half or less of those of CPCLK are applied to VBCLK. Consequently, the combinations of settings are restricted as follows.

Table 1-4. Maximum Operating Frequency of PFESiP/V850EP1 According to Operating Conditions

SDRAM, Low-Speed Mask ROM	Prioritized Clocks	Clocks		
		CPCLK	VBCLK	BUSCLK
None	CPCLK, VBCLK	200 MHz Note	100 MHz	100 MHz
Present	CPCLK, VBCLK	200 MHz	100 MHz	50 MHz Note
	BUSCLK	200 MHz	66.6 MHz	66.6 MHz Note

Note Clock that is the reference for determining the frequency.

Caution The design-guaranteed value of the maximum operating frequency cannot always be achieved, depending on the load of the FPGA.

1.3 Overview of PFESiP/V850EP1

The PFESiP/V850EP1 is a microcontroller function chip developed for the PFESiP EP-1 Series and uses a V850E2 CPU core.

The PFESiP/V850EP1 uses a high-speed process in which the CPU core operates at 200 MHz (maximum) and the internal bus at 100 MHz (maximum). This CPU core has an on-chip instruction cache and data cache. Furthermore, it has a DMA controller, an interrupt controller, general-purpose ports, a timer, a serial interface, an A/D converter, a memory controller, a host controller supporting USB 2.0 FS (full-speed) and LS (low-speed), a function controller supporting USB 2.0 FS (full-speed) as on-chip peripheral functions, and internal functions as a single-chip microcontroller.

A ROM/page ROM/SRAM or SDRAM can be connected as an external memory. Furthermore, the PFESiP/V850EP1 has an on-chip instruction RAM and data RAM, and can perform high-speed processing by executing an external program by transferring it to the instruction RAM.

In software application evaluation, debugging by the N-Wire in-circuit emulator and downloading of programs can be performed using the on-chip debug control unit (DCU).

1.3.1 Functions of PFESiP/V850EP1

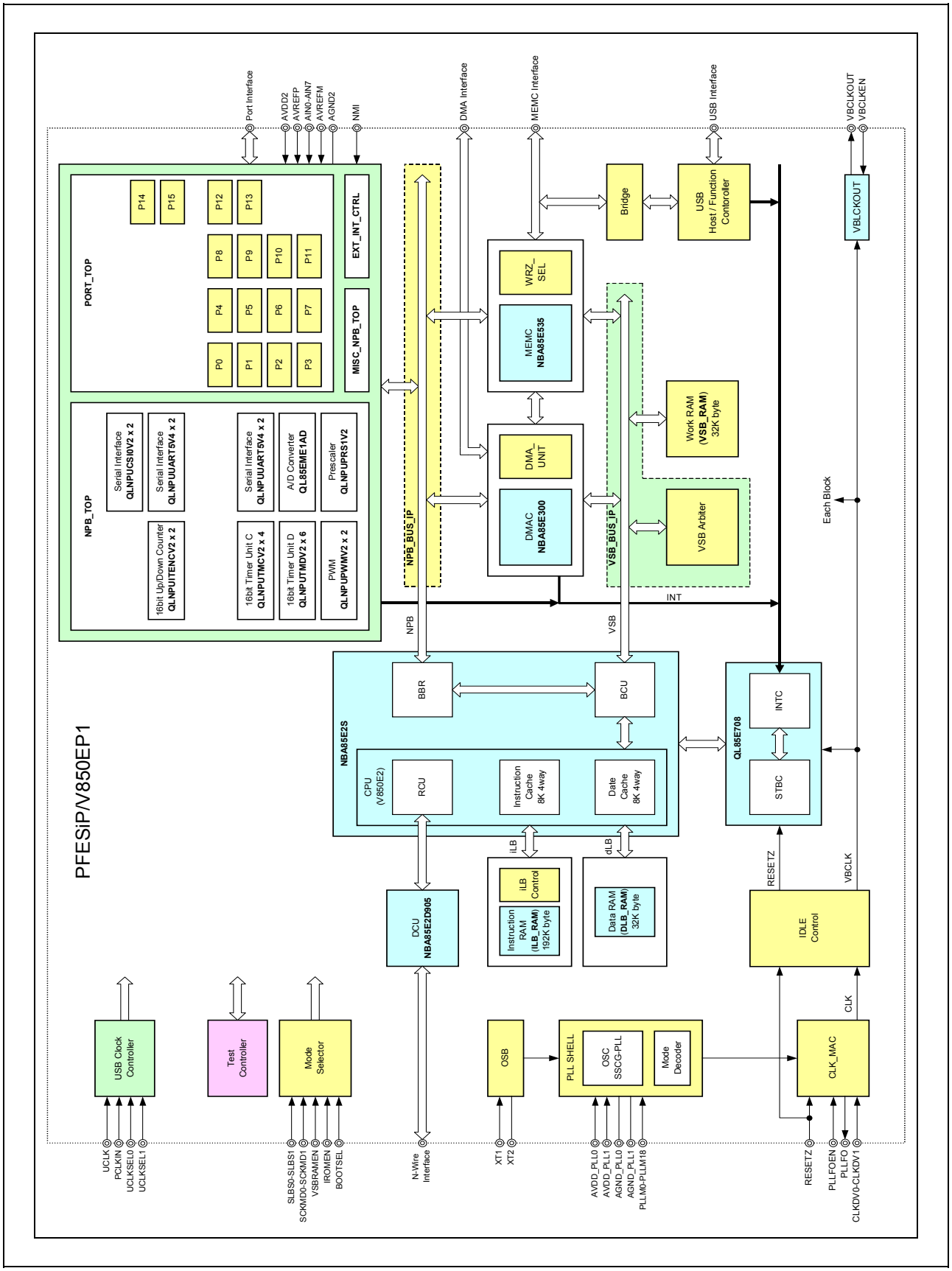
(1/2)

Item \ Product Name		PFESiP/V850EP1
CPU core		V850E2 CPU core
Minimum instruction execution time		5.00 ns (during 200 MHz operation)
General-purpose registers		32 bits × 32
Instruction set		V850E2 instruction set
Instruction cache		8 KB 4-way set associative instruction cache
Data cache		8 KB 4-way set associative data cache
Instruction RAM (iLB_RAM)	Can independently access each other	192 KB RAM structure (128-bit fetch bus)
Data RAM (dLB_RAM)		32 KB (CPCLK × 1-clock access)
Work RAM (VSB_RAM)		32 KB (VBCLK × 2-clock access)
DMA controller		4-channel DMA controller
Memory space, memory access function		• External 66.7 MHz interface • 512 MB linear address space • Memory area division function • Programmable chip select function: 8 • Programmable wait function • Idle state insertion function • Page ROM/ROM/SRAM/SDRAM interface • SDRAM support area: CSZ1, CSZ3, CSZ4, and CSZ6 areas
Interrupts/exceptions		• Non-maskable interrupt (NMI): 1 • Maskable interrupts User interrupts: 32 (external interrupts) Internal interrupts: 56 (NPB macro: 45, DMA: 4, USB: 7) • Priority level specifiable in 8 levels • Software exceptions: 32 sources • Exception trap: 1 source • Valid-edge select function • Variable digital noise filter function
SiP-dedicated interface functions		• SRAM interface Address space: 2 MB 4 dedicated chip select signals selected from CSZ1 to CSZ7 using registers 16-bit data bus Bus hold function supported • DMA interface Interface with 2 channels selected from 4 channels using registers • External interrupt function 8 interrupt signals assigned to SiP internal connections first
Standby function		IDLE/HALT mode (IDLE mode can be released by external interrupt and reset)

(2/2)

Item \ Product Name	PFESiP/V850EP1	
On-chip peripheral functions (NPB bus connection)		
I/O ports	CMOS I/Os: 121	
Timers	16-bit timer/event counter × 4 channels Interval timer × 6 channels Up/down counter/timer for 16-bit 2-phase encoder input × 2 channels	
PWM unit	8-/9-/10-/12-bit resolution PWM output × 2 channels	
Serial interfaces	Asynchronous serial interface × 4 channels Clocked serial interface × 2 channels	
USB host controller	USB 2.0 FS (full-speed), LS (low-speed) supported Internal 2-channel root-hub function 2-channel downstream port	Both host controller and function controller are placed at CSZ5. USB host controller uses external SDRAM.
USB function controller	1 channel supporting USB 2.0 FS (full-speed) Number of end points: 4 (control, bulk-in, bulk-out, interrupt)	
A/D converter	Internal 8-channel 10-bit 500 kHz A/D converter (NPB bus connection)	
On-chip debug functions	Incorporated in debug controller (DCU) • Run/break function, trace function, event function	
Clock line	External clock input multiplied by PLL and clock supplied (SSCG function provided) CPU: 200 MHz maximum, bus clock: 100 MHz maximum (CPCLK: VBCLK = 1/2, 1/3, 1/4) SDRAM interface: 66.7 MHz maximum (VBCLK: BUSCLK = 1/1, 1/2) Clock source and PLL setting switch pin provided (not switchable during operation)	
Power supply	For pin power supply: EV_{DD} = 3.3 ±0.3 V For internal power supply: IV_{DD} = 1.5 ±0.15 V	
Series	CB-12M type	

1.3.2 Internal block diagram of PFESiP/V850EP1



CHAPTER 2 HARDWARE INSTALLATION

2.1 Preface

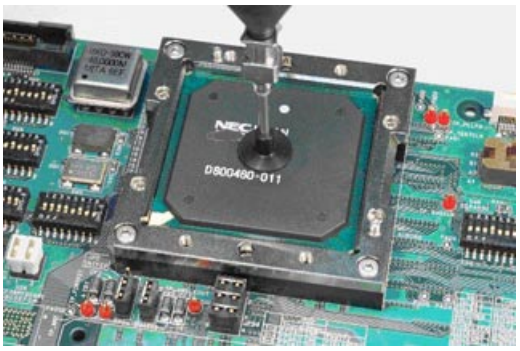
2.1.1 Mounting PFESiP/V850EP1

Position	Figure 1-1 (Appearance) D-3

Remark Two types of PFESiP EP-1 Evaluation Boards, one mounted with the PFESiP/V850EP1 and another mounted with a socket are available.
The type mounted with a socket is explained in this section. Mounting is not required with the type mounted with a chip, so proceed to **2.1.2 Operating mode setting**.

The PFESiP/V850EP1, which is normally built into an SiP as a chip, is provided specially for the PFESiP EP-1 Evaluation Board. The PFESiP/V850EP1 is a 484-pin plastic BGA package. Note that it is not falsely inserted into the socket, because the ball layout is symmetrical for both the X and Y axes. Using a vacuum pick is recommended for handling the device.

The 484-pin plastic BGA package has an INDEX mark in one of its four corners. Insert the PFESiP/V850EP1 into the socket by matching the INDEX mark and the position where the socket is chamfered.



2.1.2 Operating mode setting

To use the PFESiP EP-1 Evaluation Board for various purposes, toggle switches, dip switches, and jumpers are provided to set each operating mode.

Set the operating mode according to **CHAPTER 3 SWITCH SETTINGS** before connecting the power supply.

2.1.3 Mounting oscillation module

(1) OSC1 (for PFESiP/V850EP1)

Position **Figure 1-1 (Appearance) C-1**

A 3.3 V, 48 MHz oscillation module is provided as the standard oscillation module.
The oscillation module can be changed to other oscillation modules operating at 3.3 V due to the IC socket structure.
The maximum input frequency is 50 MHz.

(2) OSC4 (for FPGA)

Position **Figure 1-1 (Appearance) D-6**

OSC4 is the clock for the on-board large-capacity FPGA.
It is connected to CLK2P of the FPGA.
Other oscillation modules operating at 3.3 V can be used due to the IC socket structure.

Caution PCLKIN (30 MHz) and UCLK (48 MHz) to be used with the USB are provided as OSC2 and OSC3, respectively. They do not use a socket.

2.2 Connecting Power Supply

The PFESiP EP-1 Evaluation Board can use the AC adapter or power supply terminal.

Normally, it uses only a single +5.0 V power supply. Correctly connect a power supply according to the operating environment.

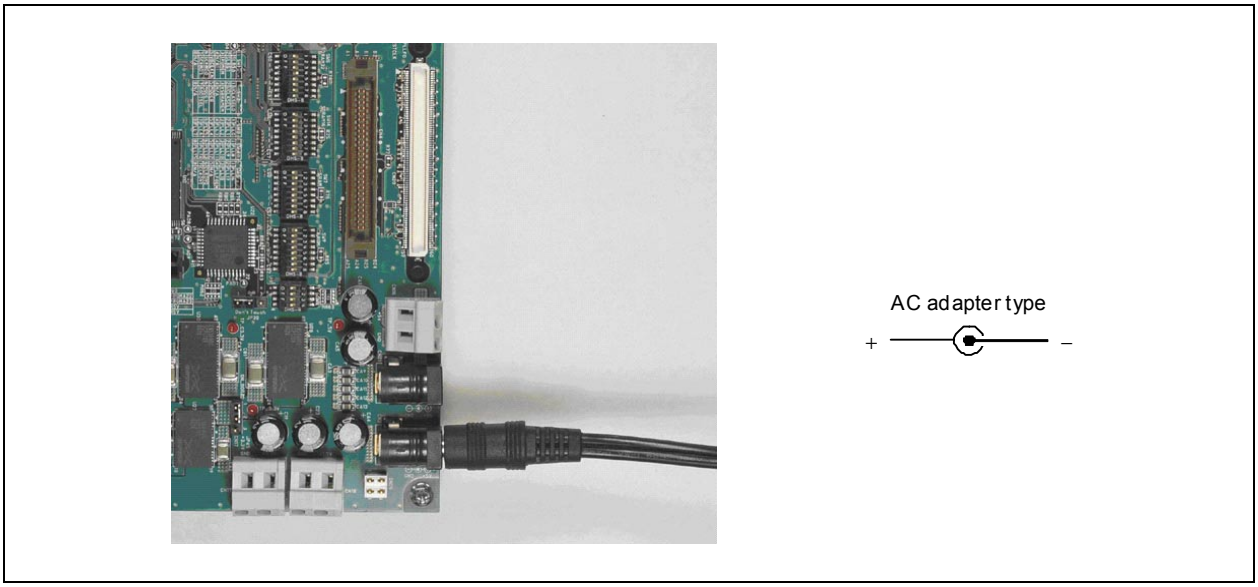
2.2.1 AC adapter (CN21, CN23)

Position **Figure 1-1 (Appearance) I-1**

Connect the +5.0 V power supply jack of an AC adapter such as the RTE-PS04 to connector CN21 or CN23.

The unused connector can be used to supply power to another board.

The +3.3 V, +2.5V, +1.8 V, +1.5 V, and +1.2 V power supplies required on-board are generated by the on-board power supply module.



Cautions 1. This cannot be used together with CN16.

2. Set the on-board operating mode setting switches before connecting the power supply.

2.2.2 5.0 V power supply terminal (CN16)

Position **Figure 1-1 (Appearance) H-1**

The 5.0 V power supply terminal is connected using +5.0 V from the external power supply via a wire. Insert a small slotted screwdriver into the hole, to the center of the substrate, and insert the wire from the outer side of the substrate. The wire will be fixed when the slotted screwdriver is removed.

The +3.3 V, +2.5 V, +1.8 V, +1.5 V, and +1.2 V power supplies required on-board are generated by the on-board power supply module.

Cautions 1. This cannot be used together with CN21 or CN23.

2. Set the on-board operating mode setting switches before connecting the power supply.

2.2.3 3.3 V and 1.5 V power supply terminal

Position **Figure 1-1 (Appearance) I-2**

The +3.3 V power supply of the PFESiP/V850EP1 I/O buffer and the internal +1.5 V power supply of the PFESiP/V850EP1 can be separately supplied from an external power supply. At this time, supply also a +5.0 V power supply.

The currents of the +3.3 V and +1.5 V power supplies of the PFESiP/V850EP1 can also be measured by connecting the currents, because power is supplied from a separate power supply.

The +3.3 V and +1.5 V power supply terminals are connected using +3.3 V and +1.5 V from an external power supply via a wire. Insert a small slotted screwdriver into the hole, to the center of the substrate, and insert the wire from the outer side of the substrate. The wire will be fixed when the slotted screwdriver is removed.

Cautions 1. Set the on-board operating mode setting switches before connecting the power supply.

2. Be sure to connect the +5.0 V power supply for supplying power to devices other than the PFESiP/V850EP1.

CHAPTER 3 SWITCH SETTINGS

3.1 Operating Mode Setting Dip Switches

Positions **Figure 1-1 (Appearance) B-1, B-2**

Some among SW1, SW2, and SW5 are dip switches used to set the operating mode.

Some among SW1, SW2, and SW5 are used to set the on-chip CPU core and memory controller operating modes of the PFESiP/V850EP1.

Each operating mode setting signal, except UCLKSEL0 and UCLKSEL1, is set to low level when the switches are turned off and to high level when the switches are turned on.

UCLKSEL0 and UCLKSEL1 are set to high level when the switches are turned off and to low level when the switches are turned on.

Table 3-1. Operating Mode Settings

DPSW	Mode Setting Signal	When Turned off (0)	When Turned on (1)
SW1-1	SLBS0	Bus width setting during startup	
SW1-2	SLBS1	SLBS <1:0> = 00: 32 bits, 01: 16 bits, 1X: 8 bits	
SW1-3	IROMEN	Normal state	Setting prohibited
SW1-4	N/A		
SW1-5	VBCLKEN	VBCLKOUT output disabled (low-level output)	VBCLKOUT output enabled
SW1-6	SCKMD0	Setting of BUSCLK division ratio to VBCLK	
		VBCLK/1	VBCLK/2
SW1-7	SCKMD1	Normal state	Setting prohibited
SW1-8	N/A		
SW2-1	UCLKSEL0	UCLK selected as USB clock	XT1 or XT2 selected as USB clock
SW2-2	UCLKSEL1	PCLKIN selected as USB bridge clock	XT1 or XT2 selected as USB bridge clock
SW2-3	VSBRAMEN	Work RAM (VSB_RAM) disabled	Work RAM (VSB_RAM) enabled
SW2-4	N/A		
SW2-5	MODE0	USB function disabled	USB function enabled
SW2-6	MODE1	USB host function disabled	USB host function enabled
SW2-7	BOOTSEL	Booted from SCSZ0 (SiP interior)	Booted from CSZ0 (external bus)
SW2-8	N/A		
SW5-4	PLLFOEN	PLLFO pin outputs low level	PLLFO pin outputs PLLFO
SW5-5	N/A		
SW5-6	CLKDV0	Setting of VBCLK division ratio to CPCLK	
SW5-7	CLKDV1	CLKDV [1:0] = 00: Setting prohibited, 01: CPCLK/2, 10: CPCLK/3, 11: CPCLK/4	
SW5-8	N/A		

3.1.1 Operating mode settings

(1) SLBS0, SLBS1 (local Bus Size)…SW1-1, SW1-2

These select the external bus size when starting the PFESiP/V850EP1.
To start the PFESiP/V850EP1 from an external flash ROM with the PFESiP EP-1 Evaluation Board, set SLBS1 = 0 (OFF) and SLBS0 = 1 (ON) and select a 16-bit width. After starting the PFESiP/V850EP1, set the bus width for each chip select signal by using the local bus sizing control register (LBS).
The operation of ports 6, 9, and 10 are as follows according to the settings of SLBS0 and SLBS1.

SW1-2	SW1-1	SLBS1	SLBS0	External Bus Size During Startup	P66 Pin Operation	P67 Pin Operation	PMC6	Operation of P90 to P97 and P100 to 107 Pins	PMC9	PMC10
OFF	OFF	0	0	32 bits	Input port	Input port	03H	D16 to D31	FFH	FFH
OFF	ON	0	1	16 bits		A1	83H	Input port	00H	00H
ON	OFF	1	0	8 bits	A0		C3H			
ON	ON	1	1							

(2) VBCLKEN (VBCLK output enable)…SW1-5

The internal system clock (VBCLK) can be output from the VBCLKOUT pin.
VBCLK will be output to VBCLKOUT only if high level is input to VBCLKEN.
This output control is an enable control structure. Whiskers may occur when the pin settings are switched during an operation.
If the switch is turned off, a low level will be output to the VBCLKOUT pin.

SW1-5	VBCLKEN	System Clock Output Control
OFF	0	Disables output (low-level output)
ON	1	Enables output

(3) SCKMD0, SCKMD1 (BUSCLK divide control)…SW1-6, SW1-7

These set the division ratio of the external bus clock (BUSCLK) to the internal system clock (VBCLK).
The maximum operating frequency of VBCLK is 100 MHz. On the other hand, the maximum operating frequency of the external bus interface is 66.7 MHz, so when using VBCLK at its maximum operating frequency, VBCLK/2 is recommended for BUSCLK.

SW1-7	SW1-6	SCKMD1	SCKMD0	BUSCLK Selection
OFF	OFF	0	0	VBCLK/1
OFF	ON	0	1	VBCLK/2
ON	OFF	1	0	Setting prohibited
ON	ON	1	1	

(4) UCLKSEL0 (USB clock select)…SW2-1

This selects the 48 MHz USB clock inputs (HCLK48M, FCLK48M) to be input to UCLK.
It selects the USB clock from UCLK, XT1, and XT2.
48 MHz is input from the on-board oscillation module (OSC3) to UCLK.

SW2-1	UCLKSEL0	USB Clock (HCLK48M, FCLK48M) Selection
OFF	1	Inputs UCLK (inputs 48 MHz of OSC3)
ON	0	Inputs XT1 or XT2

(5) UCLKSEL1 (USB clock select)…SW2-2

This selects the USB clock input (PCLK) to be input to PCLKIN.
The input frequency is from 25 MHz to 33 MHz.
It selects the internal USB bus bridge clock from PCLKIN, XT1, and XT2.
30 MHz is input from the on-board oscillation module (OSC2) to PCLKIN.

SW2-2	UCLKSEL1	Internal USB Bus Bridge Clock (PCLK) Selection
OFF	1	Inputs PCLKIN (inputs 30 MHz of OSC2)
ON	0	Inputs XT1 or XT2

(6) VSBRAMEN (VSB RAM Enable)…SW2-3

The PFESiP/V850EP1 has an on-chip 32 KB work RAM (VSB_RAM) on the VSB bus.
This work RAM (VSB_RAM) uses the VMCSZ2 (VDCSZ2) area. Connect VSBRAMEN to low level when connecting the VDCSZ2 (VDCSZ2) area to the external memory.

Table 3-2. On-Chip Work RAM (VSB_RAM) Setting

SW2-3	VSBRAMEN	On-Chip Work RAM (VSB_RAM) Operation	VDCSZ2 (CSZ2) Area
OFF	0	On-chip work RAM (VSB_RAM) is disabled.	External memory
ON	1	On-chip work RAM (VSB_RAM) is enabled.	On-chip work RAM (VSB_RAM)

Cautions 1. When using the work RAM (VSB_RAM), be sure to set the ME2 bit of bus cycle type configuration register 0 (BCT0) to 0 in order to prevent a conflict with the CSZ2 area (external memory) of the memory controller.

2. The CSZ2 pin becomes inactive when the work RAM is accessed.

(7) MODE0, MODE1 (USB Operation Mode)…SW2-5, SW2-6

These select the operating mode of the PFESiP/V850EP1.

SW2-6	SW2-5	MODE1	MODE0	Operating Mode
OFF	OFF	0	0	USB function disabled
OFF	ON	0	1	Only USB function enabled
ON	OFF	1	0	Only USB host enabled
ON	ON	1	1	USB host/function enabled

(8) BOOTSEL (Boot Select)…SW2-7

This selects the boot area from the SiP internal/external memory.
If the SiP interior is selected, the SiP chip select signal select register (SCSS) will be initialized to 0008H and booting will be performed from address 0000 0000H of the memory connected to the SCSZ0 pin.

SW2-7	BOOTSEL	Boot Area Selection	Initial SCSS Register Value
OFF	0	Memory connected to SCSZ0 in SiP	0008H
ON	1	Memory connected to CSZ0 of external bus interface	0000H

Caution The SCSZ0 signal for SiP internal connection is connected to the on-board FPGA similarly as other SiP internal connection buses. To emulate a system that has a boot ROM in the SiP, integrate the boot ROM to the on-board FPGA and connect it to the SiP internal bus.

(9) PLLFOEN (PLL FO Output Enable)…SW5-4

The FO output of the internal PLL can be output from the PLLFO pin. The FO output is also not stopped in IDLE mode.
FO is output to PLLFO only if high level is input to PLLFOEN. If low level is input, the device ID is output.
This output control is an enable control structure. Whiskers may occur when the pin settings are switched during an operation.

SW5-4	PLLFOEN	PLLFO Output Control
OFF	0	Low-level output
ON	1	Enables output

(10) CLKDV0, CLKDV1 (VBCLK Divide Control)…SW5-6, SW5-7

These are the inputs that set the VBCLK division ratio to CPCLK.
The mode in which CPCLK = VBCLK is not supported.
Do not set both SW5-6 and SW5-7 to be off at the same time.

SW5-7	SW5-6	CLKDV1	CLKDV0	VBCLK Selection
OFF	OFF	0	0	Setting prohibited
OFF	ON	0	1	CPCLK/2
ON	OFF	1	0	CPCLK/3
ON	ON	1	1	CPCLK/4

3.1.2 SSCG-PLL operating mode setting dip switches

Functions are assigned to the SSCG-PLL setting pins as follows.

DPSW	Pin Name	PFESiP/V850EP1 Internal Signal	Function
SW3-1	PLL0	PLLM0	M counter input 0
SW3-2	PLL1	PLLM1	M counter input 1
SW3-3	PLL2	PLLM2	M counter input 2
SW3-4	PLL3	PLLM3	M counter input 3
SW3-5	PLL4	PLLM4	M counter input 4
SW3-6	PLL5	PLLM5	M counter input 5
SW3-7	PLL6	PLLM6	M counter input 6
SW3-8	PLL7	PLLN0	M counter input 0
SW4-1	PLL8	PLLN1	N counter input 1
SW4-2	PLL9	PLLN2	N counter input 2
SW4-3	PLL10	PLLP0	P counter input 0
SW4-4	PLL11	PLLP1	P counter input 1
SW4-5	PLL12	SSMDL0	SSCG setting input
SW4-6	PLL13	SSMDL1	SSCG setting input
SW4-7	PLL14	SSADJ0	SSCG setting input
SW4-8	PLL15	SSADJ1	SSCG setting input
SW5-1	PLL16	SSADJ2	SSCG setting input
SW5-2	PLL17	PLLS0	SSCG setting input
SW5-3	PLL18	PLLS1	SSCG setting input

<table>
<tr><th>Pin Name</th><th>Internal Signal</th><th>Function</th></tr>
<tr><td>PLL0 to PLL6
PLL7 to PLL9
PLL10 to PLL11</td><td>PLLM0 to PLLM6
PLLN0 to PLLN2
PLLP0 to PLLP1</td><td>Input setting internal PLL multiplication rate
m = Setting values of PLLM0 to PLLM6 (0 to 127) + 1: 2 to 128
n = Setting values of PLLN0 to PLLN2 (0 to 7) + 92 + 1: 93 to 100
p = Setting value of $2^{PLLP0 - PLLP1}$: 1, 2, 4
Multiplication rate = n/m/p
<table>
<tr><th>Item</th><th>Symbol</th><th>Expression</th><th>MIN.</th><th>MAX</th><th>Unit</th></tr>
<tr><td>Input frequency</td><td>fstd</td><td>–</td><td>2.0</td><td>50.0</td><td>MHz</td></tr>
<tr><td>PFD input frequency</td><td>fpfd</td><td>fpfd = fstd/m</td><td>1.0</td><td>2.1</td><td>MHz</td></tr>
<tr><td>VCO output frequency</td><td>fvco</td><td>fvco = fstd×n/m</td><td>100</td><td>200</td><td>MHz</td></tr>
<tr><td>Output frequency</td><td>fout</td><td>Fout = fstd×n/m/p</td><td>25</td><td>200</td><td>MHz</td></tr>
<tr><td>Input duty</td><td>lduty</td><td>–</td><td>30</td><td>70</td><td>%</td></tr>
<tr><td>Multiplication rate</td><td>MULT</td><td>MULT = n/m/p</td><td>0.182</td><td>50</td><td>–</td></tr>
</table>
PLL will be set to through mode both when PLLM0 to PLLM6 are all low level and PLLP0 and PLLP1 are all high level.</td></tr>
<tr><td>PLL12 to PLL13</td><td>SSMDL0 to SSMDL1</td><td>Inputs setting SSCG modulation range
<table>
<tr><th>SSMDL1</th><th>SSMDL0</th><th>Modulation cycle [kHz]</th></tr>
<tr><td>0</td><td>0</td><td>15.00-26.25</td></tr>
<tr><td>0</td><td>1</td><td>25.00-36.75</td></tr>
<tr><td>1</td><td>0</td><td>35.00-48.30</td></tr>
<tr><td>1</td><td>1</td><td>45.00-68.25</td></tr>
</table></td></tr>
<tr><td>PLL14 to PLL16</td><td>SSADJ0 to SSADJ2</td><td>Inputs setting SSCG frequency diffusion mode and that range
<table>
<tr><th>SSADJ2</th><th>SSADJ1</th><th>SSADJ0</th><th>Frequency modulation rate</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>About –0.5%</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>About –1.0%</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>About –2.0%</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>About –3.0%</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>About –4.0%</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>About –5.0%</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>No modulation</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No modulation</td></tr>
</table></td></tr>
<tr><td>PLL17 to PLL18</td><td>PLLS0 to PLLS1</td><td>Selector inputs of SSCG
<table>
<tr><th>PLLS1</th><th>PLLS0</th><th>PFD input frequency [MHz]</th></tr>
<tr><td>0</td><td>0</td><td>1.00≤fpfd<1.20</td></tr>
<tr><td>0</td><td>1</td><td>1.20≤fpfd<1.45</td></tr>
<tr><td>1</td><td>0</td><td>1.45≤fpfd<1.70</td></tr>
<tr><td>1</td><td>1</td><td>1.70≤ pfd≤2.10</td></tr>
</table></td></tr>
</table>

3.2 Chip Select Signal Setting Dip Switches

Positions **Figure 1-1 (Appearance) F-2, G-2**

SW6, SW7, SW9, and SW14 are the dip switches that set the chip select signal of the on-board flash ROM, SRAM, SDRAM32, and SDRAM16.

Switch and Mark	Target Resource
SW6 (SDRAM32)	SDRAM32
SW7 (SRAM)	SRAM
SW9 (FROM)	Flash ROM
SW14 (SDRAM16)	SDRAM16

The CSZn signal of the PFESiP/V850EP1 can be arbitrarily selected for each target resource.
The chip select signal set to be on will be enabled (n = 0 to 7).

Remarks 1. Only a single type of a chip select signal can be used for a single resource. Consequently, do not switch multiple switches in a single dip to be on.

2. A single chip select signal cannot be assigned to multiple resources. Consequently, do not switch on a switch with the same number among SW6, SW7, SW9, and SW14.

SRAM		
DPSW	When Switched on	When Switched off
SW7-1	Selects CSZ0	Deselects CSZ0
SW7-2	Selects CSZ1	Deselects CSZ1
SW7-3	Selects CSZ2	Deselects CSZ2
SW7-4	Selects CSZ3	Deselects CSZ3
SW7-5	Selects CSZ4	Deselects CSZ4
SW7-6	Selects CSZ5	Deselects CSZ5
SW7-7	Selects CSZ6	Deselects CSZ6
SW7-8	Selects CSZ7	Deselects CSZ7

Flash ROM		
DPSW	When Switched on	When Switched off
SW9-1	Selects CSZ0	Deselects CSZ0
SW9-2	Selects CSZ1	Deselects CSZ1
SW9-3	Selects CSZ2	Deselects CSZ2
SW9-4	Selects CSZ3	Deselects CSZ3
SW9-5	Selects CSZ4	Deselects CSZ4
SW9-6	Selects CSZ5	Deselects CSZ5
SW9-7	Selects CSZ6	Deselects CSZ6
SW9-8	Selects CSZ7	Deselects CSZ7

SDRAM32		
DPSW	When Switched on	When Switched off
SW6-1	Selects CSZ0	Deselects CSZ0
SW6-2	Selects CSZ1	Deselects CSZ1
SW6-3	Selects CSZ2	Deselects CSZ2
SW6-4	Selects CSZ3	Deselects CSZ3
SW6-5	Selects CSZ4	Deselects CSZ4
SW6-6	Selects CSZ5	Deselects CSZ5
SW6-7	Selects CSZ6	Deselects CSZ6
SW6-8	Selects CSZ7	Deselects CSZ7

SDRAM16		
DPSW	When Switched on	When Switched off
SW14-1	Selects CSZ0	Deselects CSZ0
SW14-2	Selects CSZ1	Deselects CSZ1
SW14-3	Selects CSZ2	Deselects CSZ2
SW14-4	Selects CSZ3	Deselects CSZ3
SW14-5	Selects CSZ4	Deselects CSZ4
SW14-6	Selects CSZ5	Deselects CSZ5
SW14-7	Selects CSZ6	Deselects CSZ6
SW14-8	Selects CSZ7	Deselects CSZ7

3.3 Boot ROM Bank Selection Dip Switches

Position **Figure 1-1 (Appearance) G-2**

The on-board flash ROM is 16 MB. The flash ROMs are normally connected to CSZ0 because they are generally used for booting. At this time, the upper limit of CSZ0 is 8 MB. If the flash ROM is set to other than CSZ0 by using SW8, a 16 MB area can be used.

SW8 is a dip switch for selecting the banks that are configured by dividing the two bits of the higher address of the flash ROM. A different program can be stored in each bank and any bank can be selected to be started by selecting the banks as follows.

Note that only SW8-1 and SW8-2 are used for SW8 and SW8-3 and SW8-4 are provided for future expansion.

SW8-2	SW8-1	Bank Selection
OFF	OFF	Selects all banks (up to 16 MB). Equivalent to 0000 0000H to 00FF FFFFH of the flash ROM
OFF	ON	Selects bank 1 (up to 4 MB). Equivalent to 0040 0000H to 007F FFFFH of the flash ROM
ON	OFF	Selects bank 2 (up to 4 MB). Equivalent to 0080 0000H to 00BF FFFFH of the flash ROM
ON	ON	Selects bank 3 (up to 4 MB). Equivalent to 00C0 0000H to 00FF FFFFH of the flash ROM

3.4 SW_FWP (Flash ROM Boot block write protect)

Position | **Figure 1-1 (Appearance) H-6**

This sets boot block protection for each on-board flash ROM.
If the switch is turned off, the boot block will not be protected.

SW_FWP-1	FROMWP	Flash ROM Boot Block Protection
OFF	1	Normal mode (does not protect boot block).
ON	0	Protects boot block.

SW_FWP-2	SROMWP	FPGA Serial Flash ROM Boot Block Protection
OFF	1	Normal mode (does not protect boot block).
ON	0	Protects boot block.

Remarks 1. The on-board flash ROM peripheral circuit is not equipped with a circuit applying high voltage. Consequently, only the following operating modes are supported.

Mode	CE#	OE#	WE#	RESET#	WP#/ACC	DQ0-DQ15
Read	L	L	H	H	Any	DOUT
Standby	H	Any	Any	H	Any	Hi-Z
Output disable	Any	H	H	Any	Any	Hi-Z
Write	L	H	⌐⌐	H	Any	DIN
Hardware reset/standby	Any	Any	Any	L	Any	Hi-Z
Boot block protection	Any	Any	Any	Any	L	Any

2. The on-board flash ROM of the PFESiP EP-1 Evaluation Board is fixed to word mode.

3.5 Jumper Settings

The PFESiP EP-1 Evaluation Board has numerous jumpers. Set them appropriately according to the purpose of use.

(1/2)

JPn Position	Purpose	Setting		Remark
JP2 C-3	INTPZ8 source switching	1-2	FPGA (INTP from FPGA)	
		2-3	FROM (INTP from flash boot ROM)	
		open	Setting prohibited	
JP9 H-6, G-6	GND connection of AIN0 to AIN5 of A/D converter	short	GND (connects to GND).	Shorts when analog input is not used.
		open	Connects externally by using twisted pair line combining GND.	
JP10 H-6	Connection of AIN6 of A/D converter	1-2	VR1 (connects on-board volume).	
		2-3	GND (connects to GND).	
		open	Connects externally by using twisted pair line combining GND.	
JP11 H-6	GND connection of AIN7 of A/D converter	short	GND (connects to GND).	Shorts when analog input is not used.
		open	Connects externally by using twisted pair line combining GND.	
JP12 B-4	Connection of TXD0 and TXD2 of UART	1-2, 3-4	Selects UART0 (connects TXD0 to TXD and TXD2 to RTS).	
		1-3, 2-4	Selects UART2 (connects TXD0 to RTS and TXD2 to TXD).	
JP13 B-5	Connection of DTR/DSR of JSIO1 connector	short	Connects DTR and DSR.	Shorts when connecting with common PC.
		open	Does not connect DTR and DSR.	
JP14 B-5	Connection of RXD0 and RXD2 of UART	1-2, 3-4	Selects UART0 (connects RXD0 to RXD and RXD2 to CTS).	
		1-3, 2-4	Selects UART2 (connects RXD0 to CTS and RXD2 to RXD).	
JP15 B-4	Connection of TXD1 and TXD3 of UART	1-2, 3-4	Selects UART1 (connects TXD1 to TXD and TXD3 to RTS).	
		1-3, 2-4	Selects UART3 (connects TXD1 to RTS and TXD3 to TXD).	
JP16 B-6	Connection of DTR/DSR of JSIO2 connector	short	Connects DTR and DSR.	Shorts when connecting with common PC.
		open	Does not connect DTR and DSR.	
JP17 B-6	Connection of RXD1 and RXD3 of UART	1-2, 3-4	Selects UART1 (connects RXD1 to RXD and RXD3 to CTS).	
		1-3, 2-4	Selects UART3 (connects RXD1 to CTS and RXD3 to RXD).	
JP20 (1-2)	Selection of WAITZ signal connection	short	Connects WAITZ signal from FPGA and CN6.	
		open	Connects only WAITZ signal from CN6.	
(3-4)	Selection of SELFREFZ signal connection	short	Connects SELFREFZ signal from FPGA and CN6.	
		open	Connects only SELFREFZ signal from CN6.	
(5-6) D-3	Selection of HLDRQZ signal connection	short	Connects HLDRQZ signal from FPGA and CN6.	
		open	Connects only HLDRQZ signal from CN6.	
JP27 F-4	On-board SRAM bus size switching (Addr.)	1-2	32 (32-bit bus)	Must be same setting as JP29.
		2-3	16 (16-bit bus)	
		open	Setting prohibited	
JP29 F-4, 5	On-board SRAM bus size switching (CS)	1-2	32 (32-bit bus)	Must be same setting as JP27.
		2-3	16 (16-bit bus)	
		open	Setting prohibited	
JP40 C-3	SWAITZ connection	short	Connects SWAITZ to FPGA.	
		open	Fixes SWAITZ to inactive level.	
JP41 B-3	OCI0 connection	short	Inputs low level to OCI0 (overcurrent state).	
		open	Normal state	

(2/2)

JPn Position	Purpose	Setting		Remark
JP42 B-3	OCI1 connection	short	Inputs low level to OCI1 (overcurrent state).	
		open	Normal state	
JP43 C-6	Selection of FPGA DONE signal pull-up	short	Pulls up with this board.	Shorts when using the PFESiP EP-1 Evaluation Board as a single unit.
		open	Does not pull up with this board.	
JP44 B-3	FPGA ROM2 use	1-2	When only one FPGA configuration ROM is mounted (supported with XC4VLX40 to XC4VLX100)	
		2-3	When two FPGA configuration ROMs are mounted (supported with XC4VLX40 to XC4VLX160)	
		open	Setting prohibited	
JP45 H-3	3.3 V power supply selection	1-2	Supplies power from on-board power supply.	
		2-3	Supplies power from CN17.	
		Other	Setting prohibited	
JP46 I-4	1.5 V power supply selection	1-3, 2-4	Supplies power from on-board power supply.	
		3-5, 4-6	Supplies power from CN18.	
		Other	Setting prohibited	

Do not change the following jumper from its normal state for testing or debugging.

JPn Position	Purpose	Setting		Remark
JP38 G-2	PLD03 test	1-2	Normal use	
		2-3	Setting prohibited (for testing)	
		open	Setting prohibited	

3.5.1 JP27, JP29 (on-board SRAM bus configuration)

Positions **Figure 1-1 (Appearance) F-4, F-5**

These select the on-board SRAM bus size. The settings of JP27 and JP29 must be the same.

(1) JP27 (SRAM_MODE1)

JP27	On-Board SRAM Bus Size Switching (Addr)
1-2 (32)	32-bit bus. Connects A21 signal to A19 pin of lower on-board SRAM.
2-3 (16)	16-bit bus. Connects A1 signal to A19 pin of lower on-board SRAM.
Open	This setting is prohibited because A19 pin of lower on-board SRAM enters high-impedance state.

(2) JP29 (SRAM_MODE2)

JP29	On-Board SRAM Bus Size Switching (CS)
1-2 (32)	32-bit bus. Connects CS signal to CE pin of higher on-board SRAM.
2-3 (16)	16-bit bus. Fixes CE pin of higher on-board SRAM to “H”.
Open	This setting is prohibited because CE pin of higher on-board SRAM enters high-impedance state.

3.5.2 JP2 (INTPZ8 interrupt signal)

Position **Figure 1-1 (Appearance) C-3**

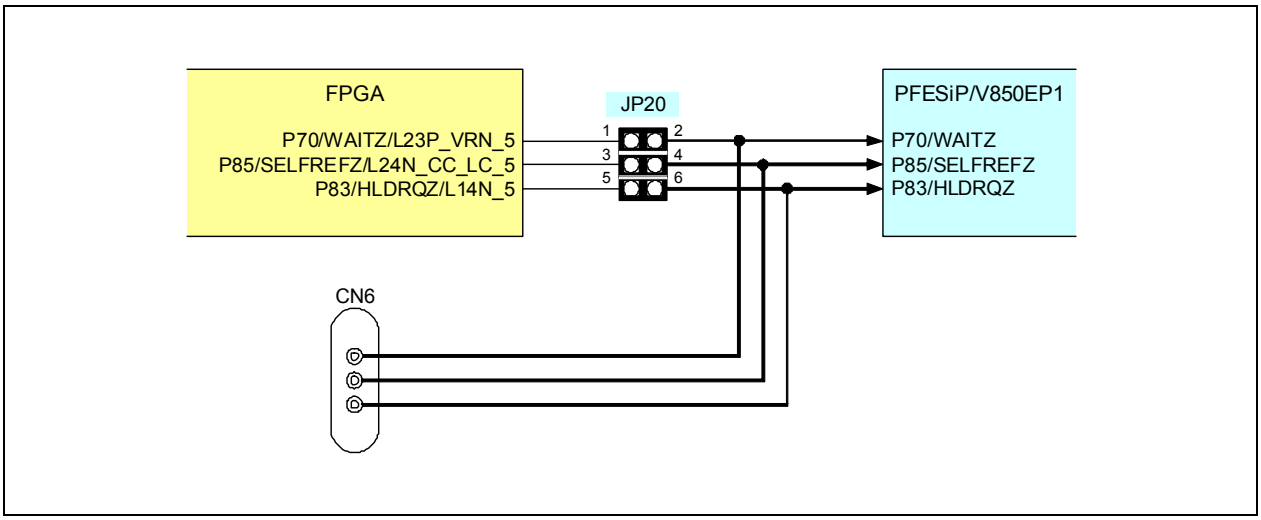
This selects the INTPZ8 (P10) signal to be input to the PFESiP/V850EP1.

JP2	INTPZ8 (P10) Source Switching
1-2 (FPGA)	Connects P10 of on-board FPGA to INTPZ8 (P10) pin.
2-3 (FROM)	Connects RY/BY signal of flash ROM to INTPZ8 (P10) pin. Select this if RY/BY signal is required when writing to flash ROM.
Open	This setting is prohibited because INTPZ8 (P10) pin enters high-impedance state.

3.5.3 JP20 (WAITZ, SELFREFZ, HLDRQZ jumpers)

Position **Figure 1-1 (Appearance) D-3**

This separately selects the connection of the WAITZ, SELFREFZ, and HLDRQZ signals.



Caution Do not perform settings other than the following.

JP20 1-2	WAITZ Signal Connection Selection
Short	Connects WAITZ signal to WAITZ signal from P70 or CN6 of FPGA by wired OR..
Open	Connects WAITZ signal to WAITZ signal from CN6.

JP20 3-4	SELFREFZ Signal Connection Selection
Short	Connects SELFREFZ signal to SELFREFZ signal from P85 or CN6 of FPGA by wired OR.
Open	Connects SELFREFZ signal to SELFREFZ signal from CN6.

JP20 5-6	HLDRQZ Signal Connection Selection
Short	Connects HLDRQZ signal to HLDRQZ signal from P83 or CN6 of FPGA by wired OR..
Open	Connects HLDRQZ signal to HLDRQZ signal from CN6.

3.5.4 JP40 (SWAITZ jumper)

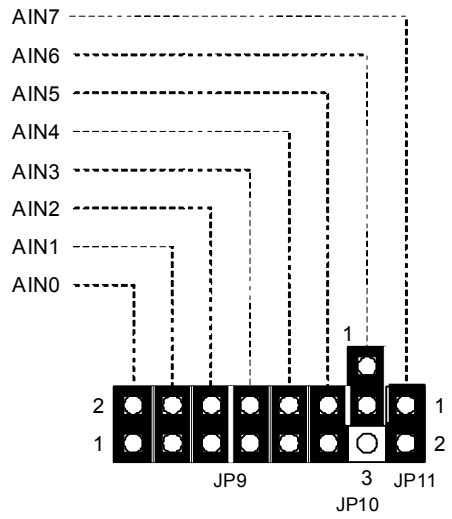
Position **Figure 1-1 (Appearance) C-3**

This selects the connection of the SWAITZ signal.

JP40	SWAITZ Signal Connection Selection
Short	Connects SWAITZ signal to SWAITZ/L28P_6 of FPGA.
Open	Fixes SWAITZ signal to inactive level (high level).

3.5.5 JP9-JP11 (analog inputs selection)

Positions | **Figure 1-1 (Appearance) H-6, G-6**



Initial jumper state

(1) JP9 (AIN0-AIN5), JP11 (AIN7)

AIN0 to AIN5 of the A/D converter of the PFESiP/V850EP1 are connected to terminals where GND and the signals are paired at JP9. AIN7 is connected to a terminal where GND and the signal are paired at JP11. Normally, the signals and GND are shorted by the jumpers.

To externally input analog signals, connect the signals to these terminals using twisted pair lines by which each signal is paired with GND.

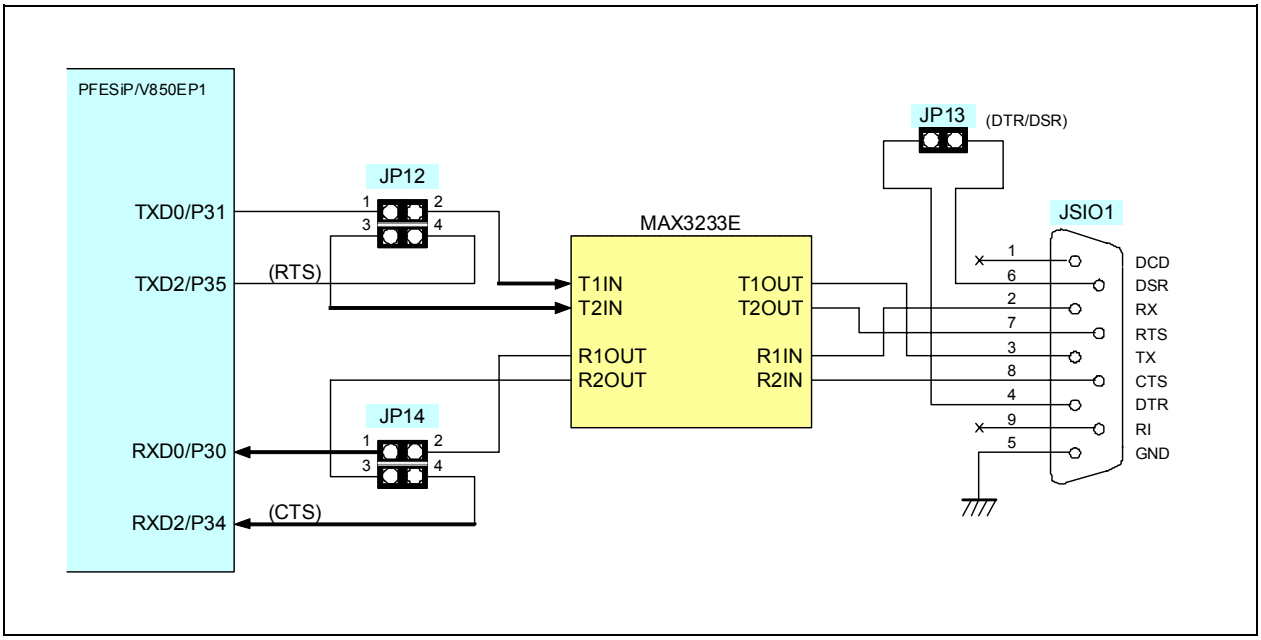
(2) JP10 (AIN6)

AIN6 of the A/D converter is connected to a volume that divides the voltage of the 3.3 V power supply.

JP10	AIN6 Connection Destination Switching
1-2	Connects the on-board volume (VR1).
2-3	Uses as external analog input, with 2: analog input and 3: GND.
Open	This setting is prohibited because AIN6 is undefined when left open.

3.5.6 JP12 to JP14 (serial interface JSIO1 connection)

Position | **Figure 1-1 (Appearance) B-4, B-5**



(1) JP12 (TXD)

This switches between the TXD and RTS functions of the TXD0 and TXD2 pins.

JP12	Switching Between TXD and RTS Functions of TXD0 and TXD2 Pins
1-2, 3-4	TXD0 functions as TXD and TXD2 as RTS.
1-3, 2-4	TXD0 functions as RTS and TXD2 as TXD.
Open	TXD0 and TXD2 are unused. TXD0 and TXD2 are externally pulled up.

(2) JP13 (DTR/DSR)

This connects DTR and DSR.
To connect DTR and DSR to a common PC, DTR and DSR are shorted for use.

JP13	DTR and DSR Pin Settings
Short	Shorts connection between DTR and DSR (general use method).
Open	Leaves connection between DTR and DSR open.

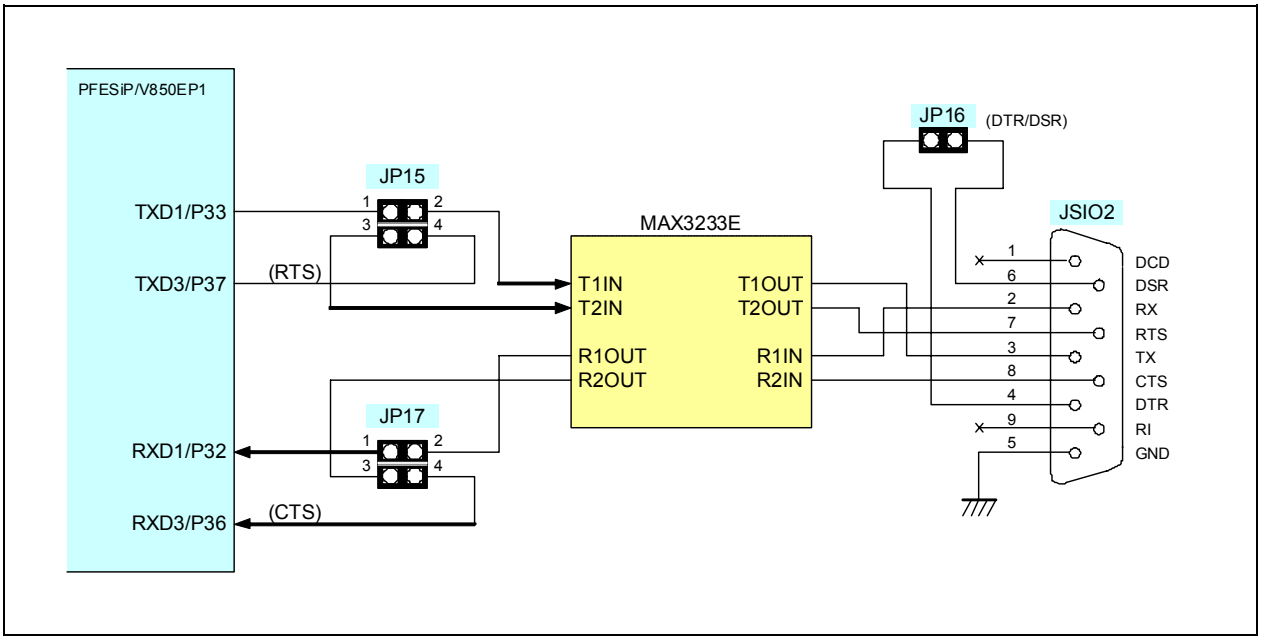
(3) JP14 (RXD)

This switches between the RXD and CTS functions of the RXD0 and RXD2 pins.

JP14	Switching Between RXD and CTS Functions of RXD0 and RXD2 Pins
1-2, 3-4	RXD0 functions as RXD and RXD2 as CTS.
1-3, 2-4	RXD0 functions as CTS and RXD2 as RXD.
Open	RXD0 and RXD2 are unused. RXD0 and RXD2 are externally pulled up.

3.5.7 JP15 to JP17 (serial interface JSIO2 connection)

Position | **Figure 1-1 (Appearance) B-6**



(1) JP15 (TXD)

This switches between the TXD and RTS functions of the TXD1 and TXD3 pins.

JP12	Switching Between TXD and RTS Functions of TXD1 and TXD3 Pins
1-2, 3-4	TXD1 functions as TXD and TXD3 as RTS.
1-3, 2-4	TXD1 functions as RTS and TXD3 as TXD.
Open	TXD1 and TXD3 are unused. TXD1 and TXD3 are externally pulled up.

(2) JP16 (DTR / DSR)

This connects DTR and DSR.
To connect DTR and DSR to a common PC, DTR and DSR are shorted for use.

JP13	DTR and DSR Pin Settings
Short	Shorts connection between DTR and DSR (general use method).
Open	Leaves connection between DTR and DSR open.

(3) JP17 (RXD)

This switches between the RXD and CTS functions of the RXD1 and RXD3 pins.

JP14	Switching Between RXD and CTS Functions of RXD1 and RXD3 Pins
1-2, 3-4	RXD1 functions as RXD and RXD3 as CTS.
1-3, 2-4	RXD1 functions as CTS and RXD3 as RXD.
Open	RXD1 and RXD3 are unused. RXD1 and RXD3 are externally pulled up.

3.5.8 JP41, JP42 (USB interface OCI0, OCI1 jumpers)

Position **Figure 1-1 (Appearance) B-3**

Leave JP41 and JP42 open for normal use.

JP41	USB Host Interface OCI0 Pin Selection
Short	Inputs low level to OCI0 (overcurrent state).
Open	Normal state (connects to high-side switch).

JP42	USB Host Interface OCI1 Pin Selection
Short	Inputs low level to OCI1 (overcurrent state).
Open	Normal state (connects to high-side switch).

3.5.9 JP43 (FPGA DONE signal pull-up setting jumper)

Position **Figure 1-1 (Appearance) C-6**

Short JP43 when using the PFESiP EP-1 Evaluation Board by itself.

The PFESiP EP-1 Evaluation Board can be stacked with another board. At this time, system reset is released by asserting all DONE signals of the FPGA. To combine the PFESiP EP-1 Evaluation Board with another board, the pull-up processing of the PFESiP EP-1 Evaluation Board may have to be canceled, because these DONE signals are connected by wired OR.

JP43	Pulls-up Process
Short	Pulls up with this board.
Open	Does not pull up with this board.

3.5.10 JP44 (FPGA configuration ROM selection jumper)

Position **Figure 1-1 (Appearance) B-6**

When only one configuration ROM for the on-board FPGA is used (JP44 1-2), Virtex-4 XC4VLX40 to XC4VLX100 can be used as the FPGA.

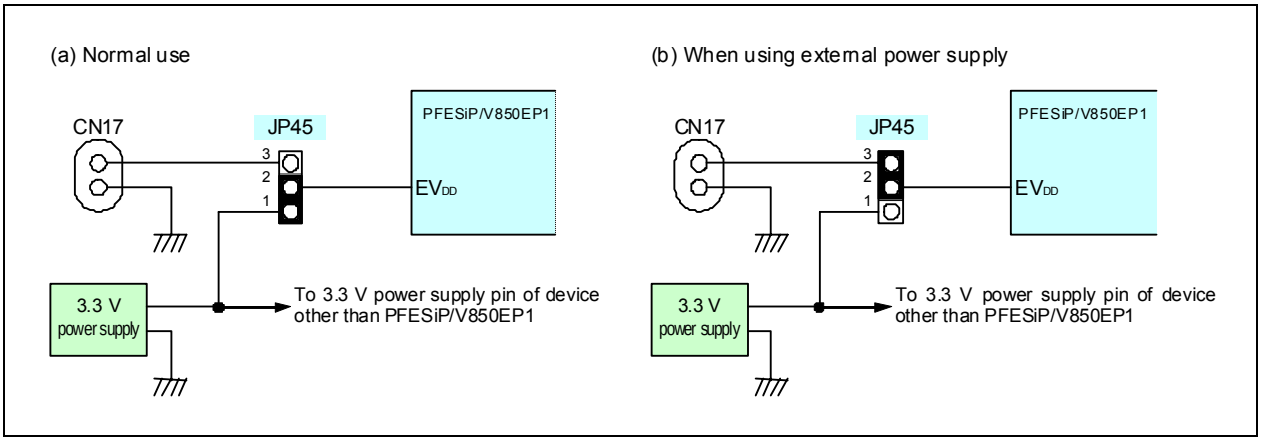
Any FPGA up to XC4VLX160 can be mounted on the PFESiP EP-1 Evaluation Board. In this case, XCF08PFSG48C will be additionally mounted as a configuration ROM and 2-3 of JP44 will be shorted.

JP44	FPGA ROM2 Use Selection
1-2	When only one FPGA configuration ROM is mounted (supported with XC4VLX40 to XC4VLX100)
2-3	When two FPGA configuration ROMs are mounted (supported with XC4VLX40 to XC4VLX160)
Open	Setting prohibited

3.5.11 JP45 (PFESiP/V850EP1 EV_{DD}: +3.3 V power supply jumper)

Position **Figure 1-1 (Appearance) H-3**

With the PFESiP EP-1 Evaluation Board, an on-board power supply or an external power supply can be selected as the +3.3 V power supply used by the PFESiP/V850EP1. Use an external power supply and connect an ammeter when measuring the current.



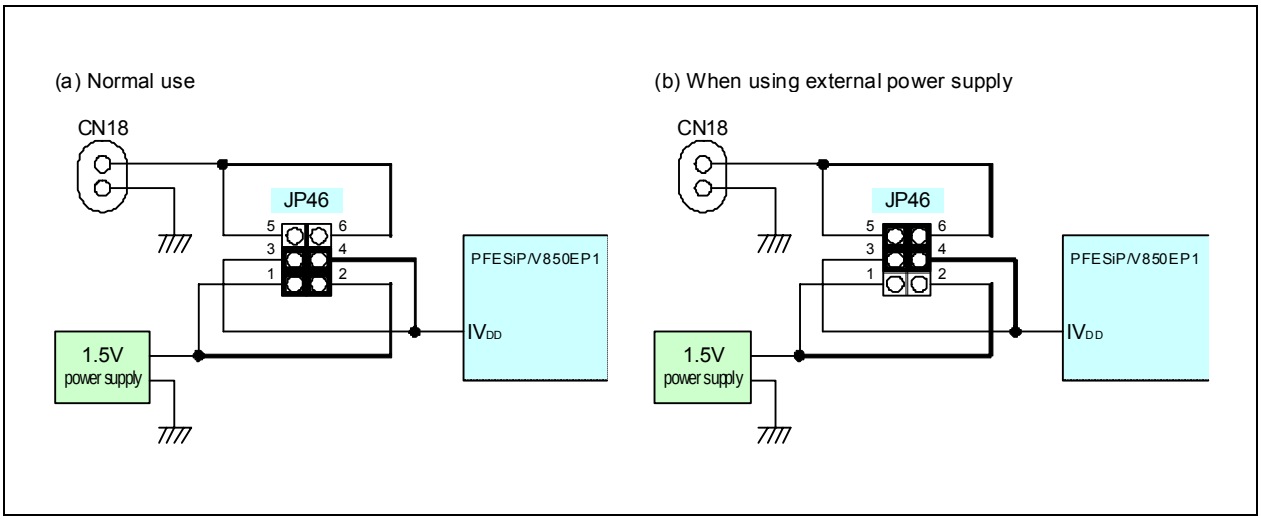
Caution The +3.3 V power supply of other than the PFESiP/V850EP1 is generated from a +5.0 V power supply. Connect the +5.0 V power supply even when externally supplying EV_{DD}: +3.3 V of the PFESiP/V850EP1 by using CN17.

JP45	PFESiP/V850EP1 EV_{DD} (3.3 V) Power Supply Selection
1-2	Supplies power from on-board power supply.
2-3	Supplies power from CN17.
Open	Setting prohibited

3.5.12 JP46 (PFESiP/V850EP1 IV_{DD}: +1.5 V power supply jumper)

Position **Figure 1-1 (Appearance) I-4**

With the PFESiP EP-1 Evaluation Board, the +1.5 V power supply can be used only as an internal power supply. An on-board power supply or an external power supply can be selected as the +1.5 V power supply. Use an external power supply and connect an ammeter when measuring the current. Two jumpers are used to secure the current capacity.



JP46	PFESiP/V850EP1 IV_{DD} (1.5 V) Power Supply Selection
1-3, 2-4	Supplies power from on-board power supply.
3-5, 4-6	Supplies power from CN18.
Open	Setting prohibited

CHAPTER 4 EXTERNAL MEMORY ACCESS SETTING EXAMPLE

Settings such as chip select settings and settings of the number of waits are required to access the memories mounted on-board. These settings are performed in the initial program initialization process. With CA850, for example, the settings are set mainly in the startup routine.

Remark This chapter explains the register settings unique to the PFESiP EP-1 Evaluation Board. See the related documents for the settings of general registers.

4.1 On-Board Memory Specifications

Positions **Figure 1-1 (Appearance) E-3, F-2, F-3**

The PFESiP EP-1 Evaluation Board has an on-board flash ROM, SRAM and SDRAM that are used for general purposes. The PFESiP/V850EP1 has an on-chip instruction RAM (for fetching programs), data RAM (for data), and work RAM (for work).

4.1.1 External memory

Table 4-1. External Memories

	Flash ROM	SRAM	SDRAM32	SDRAM16
Product name	TC58FVM7B5BTG65	μPD4416016G5-A15	MT48LC16M16A2TG-7E	MT48LC16M16A2TG-7E
Access time	65 ns@100 pF	15 ns@30 pF	C_L = 2/3, 5.4 ns	C_L = 2/3, 5.4 ns
Capacity	16 MB	4 MB (2 MB×2)	64 MB (32 MB×2)	32 MB (32 MB×1)
Bus size	16 bits	32 bits (16 bits×2)	32 bits (16 bits×2)	16 bits (16 bits×1)
Chip select area	Any one from CSZ0 to CSZ7. CSZ0 as standard.	Any one from CSZ0 to CSZ7.	Any one from SZ1, CSZ3, CSZ4, and CSZ6	Any one from CSZ1, CSZ3, CSZ4, and CSZ6

Remark The following setting examples are explained based on the following settings.

Flash ROM: CSZ0 area
SRAM: CSZ1 area
SDRAM32: CSZ3 area
VSB_RAM: CSZ2 area

4.1.2 Internal memory

	Instruction RAM (iLB RAM)	Data RAM (dLB RAM)	Work RAM (VSB RAM)
Capacity	192 KB	32 KB	32 KB
Connection bus	iLB	dLB	VSB
Bus size	128 bits	32 bits	32 bits
Access clock	CPCLK × 1 clock	CPCLK × 1 clock	VBCLK × 2 clocks

The work RAM is enabled when SW2-3 (VSBRAMEN) is turned on.

4.2 Setting External Memory Access Operation

To start the PFESiP/V850EP1, the mode registers related to the following bus interfaces must be set.

Address	Register Name	Register Symbol
1FFF F060H	Chip area select control register 0	CSC0
1FFF F062H	Chip area select control register 1	CSC1
1FFF F066H	Bus size configuration register	BSC
1FFF F06AH	Cache area specification register	BHC
1FFF F06EH	NPB strobe wait control register	VSWC
1FFF F44CH	Port 6 mode control register	PMC6
1FFF F44EH	Port 7 mode control register	PMC7
1FFF F450H	Port 8 mode control register	PMC8
1FFF F452H	Port 9 mode control register	PMC9
1FFF F454H	Port 10 mode control register	PMC10
1FFF F480H	Bus cycle type configuration register 0	BCT0
1FFF F482H	Bus cycle type configuration register 1	BCT1
1FFF F484H	Data wait control register 0	DWC0
1FFF F486H	Data wait control register 1	DWC1
1FFF F488H	Bus cycle control register	BCC
1FFF F48AH	Address setting wait control register	ASC
1FFF F48CH	Bus cycle control register	BCP
1FFF F48EH	Local bus sizing control register	LBS
1FFF F494H	DMA flyby transfer wait control register	FWC
1FFF F496H	DMA flyby transfer idle control register	FIC
1FFF F498H	Bus mode control register	BMC
1FFF F49AH	Page ROM configuration register	PRC
1FFF F4A4H	SDRAM configuration register 1	SCR1
1FFF F4A6H	SDRAM refresh control register 1	RFS1
1FFF F4ACH	SDRAM configuration register 3	SCR3
1FFF F4AEH	SDRAM refresh control register 3	RFS3
1FFF F4B0H	SDRAM configuration register 4	SCR4
1FFF F4B2H	SDRAM refresh control register 4	RFS4
1FFF F4B8H	SDRAM configuration register 6	SCR6
1FFF F4BAH	SDRAM refresh control register 6	RFS6
1FFF F8B0H	Write enable switch register	WREN

(1) Flash ROM

(a) Fixed values

Item	Corresponding Register	Setting Value	Remark
Chip area select	CSC0	Sub-areas 00 to 02	Connected to CSZ0 (instructions can be fetched) Flash ROM area is restricted because work RAM (VSB_RAM) is used.
VSB bus size	BSC	32 bits	Connection of memory controller and CPU core is fixed to 32 bits.
Bus cycle type	BCT0	Page ROM	TC58FVM7B5BTG65 supports page mode.
Address setting wait	ASC	0	
Page ROM setting	PRC	16 bits × 8	TC58FVM7B5BTG65 supports page mode.
Local bus size	LBS	16 bits	Initial value is set to 16 bits because PFESiP/V850EP1 is started from external ROM when reset is released. Started with SLBS1 (SW1-2) = 0 (OFF) and SLBS0 (SW1-1) = 1 (ON)

(b) Operating frequency dependence

Item	Corresponding Register	BUSCLK			Remark
		66.7MHz	48MHz	24MHz	
Data wait	DWC0	4	3	1	BUSCLK cycle × (Tw + 1.5) − 11.0 − 3.8 − 5 >25 (@100pF) BUSCLK cycle × (Tw + 2) − 11.0 − 3.8 − 5 >70 (@100pF)
On-page data wait	PRC	2	1	0	BUSCLK cycle × (Tw + 1.5) − 11.0 − 3.8 >30 (@100pF)
Idle state	BCC	2	1	0	t_{DF} = 25ns (MAX.) 11.0 + 25 + 2.5 − 1.5 − BUSLCK cycle

Remarks 1. For the data wait and on-page data wait, “BUSCLK cycle × (Number of waits + 1.5) − RDZ delay time (max.) − Data input setting (min.) − Substrate delay (to and fro)” must be longer than the ROM access time from the read strobe, and “BUSCLK cycle × (Number of waits + 2) − Address or chip select delay time (max.) − Data input setting (min.) − Substrate delay (to and fro)” must be longer than the ROM access time from an address or chip select signal.

2. A time exceeding “RDZ delay time (max.) + ROM data floating (max.) + Substrate delay (one-way) − Data output delay (min.) − BUSCLK cycle (of T0 cycle)” must be secured for the idle state.

(2) SRAM

(a) Fixed values

Item	Corresponding Register	Setting Value	Remark
Chip area select	CSC0	Area 1	Connected to CSZ1 (instructions can be fetched)
VSB bus size	BSC	32 bits	Connection of memory controller and CPU core is fixed to 32 bits.
Bus cycle type	BCT0	SRAM/I/O	
Address setting wait	ASC	0	
Local bus size	LBS	32 bits	Initial value is set to 16 bits because PFESiP/V850EP1 is started from ROM when reset is released.

(b) Operating frequency dependence

Item	Corresponding Register	BUSCLK			Remark
		66.7 MHz	48 MHz	24 MHz	
Data wait	DWC0	1	0	0	BUSCLK cycle × (Tw + 1.5) – 11.0 – 3.8 – 5 > 5 (@30pF) BUSCLK cycle × (Tw + 2) – 11.0 – 3.8 – 5 > 10 (@30pF)
Idle state	BCC	1	0	0	t_{COD}, t_{ODO} = 7ns (MAX.) 11.0 + 7 + 2.5 – 1.5 – BUSLCK cycle

Remarks 1. For the data wait, the read cycle condition must be stringent, “BUSCLK cycle × (Number of waits + 1.5) – RDZ delay time (max.) – Data input setting (min.) – Substrate delay (to and fro)” must be longer than the RAM access time from the read strobe, and “BUSCLK cycle × (Number of waits + 2) – Address or chip select delay time (max.) – Data input setting (min.) – Substrate delay (to and fro)” must be longer than the RAM access time from an address or chip select signal.

2. A time exceeding “RDZ delay time (max.) + ROM data floating (max.) + Substrate delay (one-way) – Data output delay (min.) – BUSCLK cycle (of T0 cycle)” must be secured for the idle state.

(3) SDRAM32

(a) Fixed values

Item	Corresponding Register	Setting Value	Remark
Chip area select	CSC0	Area 1	Connected to CSZ3 (instructions can be fetched)
VSB bus size	BSC	32 bits	Connection of memory controller and CPU core is fixed to 32 bits.
Bus cycle type	BCT0	SDRAM	
Local bus size	LBS	32 bits	Initial value is set to 16 bits because PFESiP/V850EP1 is started from ROM when reset is released.
On-page address shift width	SCR3	2 bits	32-bit width
Row address width	SCR3	13 bits	A25, A24: Bank address
Bank Active → R/W Cmd.	SCR3	2 clocks	t_{RCD} = 1.5 clocks or more
Address multiplexing	SCR3	9 bits	A14 to A2: Row address (13 bits), column address (9 bits)

(b) Operating frequency dependence

Item	Corresponding Register	BUSCLK			Remark
		66.7 MHz	48 MHz	24 MHz	
CAS latency	SCR3	2	2	2	$t_{AC(3)}$ = 5.4 ns (MAX.), $t_{AC(2)}$ = 5.4 ns (MAX.)
Refresh interval	RFS3	Cfac=32: 16 Cfac=128: 4 Cfac=256: 2	Cfac=32: 11 Cfac=128: 2 Cfac=256: 1	Cfac=32: 5 Cfac=128: 1	t_{REF} = 64 ms (MAX.) (8,192 rows)
Idle state	BCC	0	0	0	t_{HZ} = 5.4 ns (MAX.) 5.4 + 2.5 – 1.5 – BUSLCK cycle

Remark A time exceeding “SDRAM data floating (max.) + Substrate delay (one-way) – Data output delay (min.) – BUSCLK cycle (of T0 cycle)” must be secured for the idle state.

(4) On-chip work RAM (VSB_RAM)

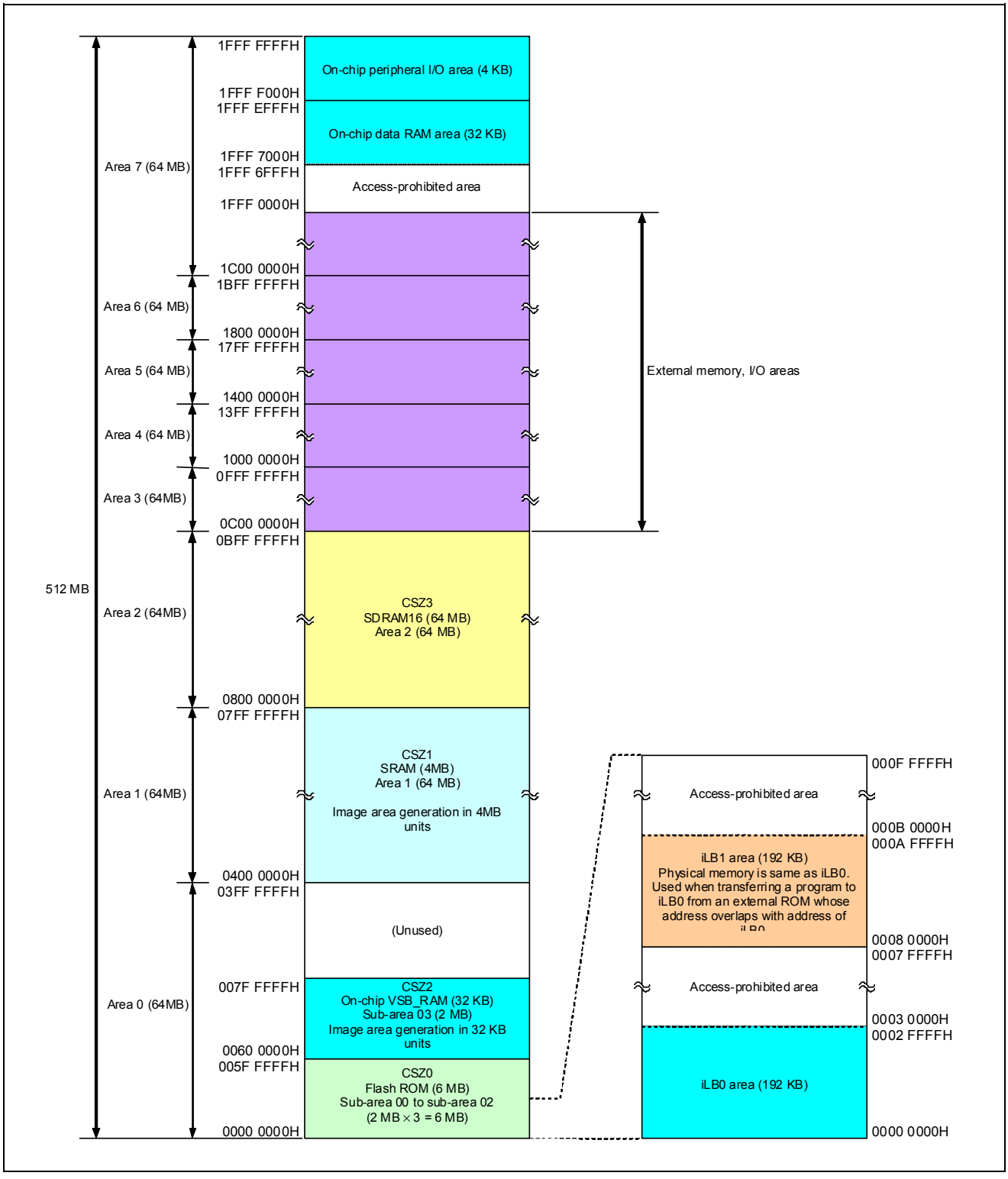
Item	Corresponding Register	Setting Value	Remark
Chip select area	CSC0	Sub-area 03	Connected to CSZ2 (instructions can be fetched)
VSB bus size	BSC	32 bits	Connection of memory controller and CPU core is fixed to 32 bits.
Bus cycle type	BCT0	Operation disabled	Operation of CSZ2 area of memory controller disabled

Remark VSB_RAM is always accessed in two VBCLK clocks.

(5) NPB strobe wait control register (VSWC)

Item	VBCLK		
	66.7 MHz	48 MHz	24 MHz
VSWC Setting Value	0042H	0041H	0001H

(6) Memory map

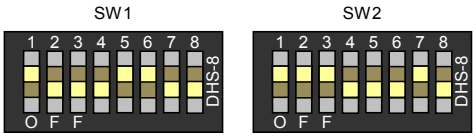
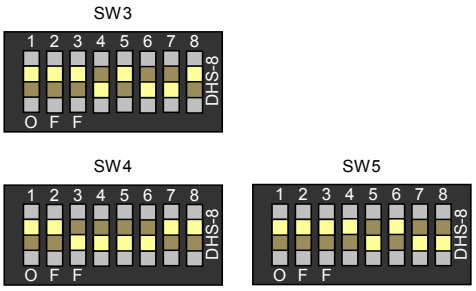
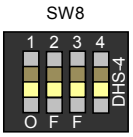


Remark Up to 8 MB can be used as the flash ROM, but the flash ROM area is restricted to 6 MB, because the on-chip work RAM (VSB_RAM) is used in this example.

(7) Register setting examples

The following setting examples are those under the following conditions.

Item	Setting
XT1 input frequency	48 MHz
CPU pipeline clock (CPCLK)	200 MHz
Internal system clock (VBCLK)	100 Hz
Bus clock (BUSCLK)	50 MHz

Item	Setting Contents	Setting
Operating mode setting	SW1-1 and SW1-2: Start 16-bit bus width. SW1-3: Must be 0. SW1-4: Unused (Don't Care) SW1-5: Disables VBCLKOUT output. SW1-6: BUSCLK = VBCLK/2 SW1-7: Must be 0. SW2-1: Selects UCLK as USB clock. SW2-2: Selects PCLKIN for USB bridge. SW2-3: Enables work RAM (VSB_RAM). SW2-4: Unused (Don't Care) SW2-5 and SW2-6: OFF SW2-7: Boots from CSZ0 (external bus)	
PLL operating mode	SW3-1 to SW3-7: M value = 23 (m value = 24) SW3-8 to SW4-2: N value = 7 (n value = 100) SW4-3 and SW4-4: P value = 0 (p value = 1) Multiplication rate = n/m/p = × 4.1666 48 MHz × 4.1666 = 200 MHz SW4-5 and SW4-6: Modulation cycle 15 kHz SW4-7 to SW5-1: No modulation SW5-2 to SW5-3: S selector = 2.0MHz SW5-4: PLLFO is low-level output SW5-6 and SW 5-7: VBCLK = CPCLK/2	
For boot ROM bank selection	SW8-1 and SW8-2: Select all banks.	

(8) Port 6 mode control register (PMC6)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC6	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	1FFFF44CH	83H	R/W
Setting value	1	1	1	1	1	1	1	1		FFH	
Alternative function	A1	A0	A25	A24	A23	A22	A21	A20			
Function selection	A1	A0	A25	A24	A23	A22	A21	A20			

(9) Port7 mode control register (PMC7)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC7	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	1FFFF44EH	01H	R/W
Setting value	0	0	0	0	1	0	1	1		0BH	
Alternative function	CSZ7	CSZ6	CSZ5	CSZ4	CSZ3	CSZ2	CSZ1	WAITZ			
Function selection	P77	P76	P75	P74	CSZ3	P72	CSZ1	WAITZ			

(10) Port9 mode control register (PMC9)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC9	PMC97	PMC96	PMC95	PMC94	PMC93	PMC92	PMC91	PMC90	1FFFF452H	00H	R/W
Setting value	1	1	1	1	1	1	1	1		FFH	
Alternative function	D23	D22	D21	D20	D19	D18	D17	D16			
Function selection	D23	D22	D21	D20	D19	D18	D17	D16			

(11) Port 10 mode control register (PMC10)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC10	PMC107	PMC106	PMC105	PMC104	PMC103	PMC102	PMC101	PMC100	1FFFF454H	00H	R/W
Setting value	1	1	1	1	1	1	1	1		FFH	
Alternative function	D31	D30	D29	D28	D27	D26	D25	D24			
Function selection	D31	D30	D29	D28	D27	D26	D25	D24			

(12) Chip area select control register 0 (CSC0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
CSC0	CS 33	CS 32	CS 31	CS 30	CS 23	CS 22	CS 21	CS 20	CS 13	CS 12	CS 11	CS 10	CS 03	CS 02	CS 01	CS 00	1FFFF060H	C231H	R/W
Setting value	0	1	0	0	1	0	0	0	0	0	1	0	0	1	1	1		4827H	
CSZn signal	CSZ3				CSZ2				CSZ1				CSZ0						
Selected area	Area 2				Sub-area 03				Area 1				Sub-areas 00 to 02						
Target	SDRAM				VSB_RAM				SRAM				Flash ROM						

(13) Bus size configuration register (BSC)

Caution Do not change the BSC register value from its initial value (AAAAH) for general use.

(14) Bus cycle type configuration register (BCT0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
BCT0	ME3	0	BT31	BT30	ME2	0	0	BT20	ME1	0	BT11	BT10	ME0	0	0	BT00	1FFFF480H	8888H	R/W
Setting value	1	0	1	1	0	0	0	0	1	0	0	0	1	0	0	1		B089H	
CSZn signal	CSZ3				CSZ2				CSZ1				CSZ0						
Operation	SDRAM				Unused				SRAM, I/O				Page ROM						
Target	SDRAM				VSB_RAM				SRAM				Flash ROM						

(15) NPB strobe wait control register (VSWC)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
VSWC	0	0	0	0	0	0	0	0	SUWL1	SUWL2	0	0	VSWL3	VSWL2	VSWL1	VSWL0	1FFFF06EH	00CFH	R/W
Setting value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0		0042H	
Operation	Data setup = 1VBCLK⟶													VPSTB = 3VBCLK					

(16) Data wait control register 0 (DWC0)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
DWC0	0	DW32	DW31	DW30	0	DW22	DW21	DW20	0	DW12	DW11	DW10	0	DW02	DW01	DW00	1FFFF484H	7777H	R/W
Setting value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1		0003H	
CSZn signal	CSZ3				CSZ2				CSZ1				CSZ0						
Operation	–				–				0 wait				3 wait						
Target	SDRAM				VSB_RAM				SRAM				Flash ROM						

(17) Bus cycle control register (BCC)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
BCC	BC71	BC70	BC61	BC60	BC51	BC50	BC41	BC40	BC31	BC30	BC21	BC20	BC11	BC10	BC01	BC00	1FFFF488H	FFFFH	R/W
Setting value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		0001H	
Target CS	CSZ7		CSZ6		CSZ5		CSZ4		CSZ3		CSZ2		CSZ1		CSZ0				
Operation	0		0		0		0		0		–		0		1				
Target	Unused		Unused		Unused		Unused		SDRAM		VSB_RAM		SRAM		Flash ROM				

(18) Address setting wait control register (ASC)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
ASC	AC71	AC70	AC61	AC60	AC51	AC50	AC41	AC40	AC31	AC30	AC21	AC20	AC11	AC10	AC01	AC00	1FFFF48AH	FFFFH	R/W
Setting value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0000H	
Target CS	CSZ7		CSZ6		CSZ5		CSZ4		CSZ3		CSZ2		CSZ1		CSZ0				
Operation	0		0		0		0		–		–		0		0				
Target	Unused		Unused		Unused		Unused		SDRAM		VSB_RAM		SRAM		Flash ROM				

(19) Local bus sizing control register (LBS)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
LBS	LB 71	LB 70	LB 61	LB 60	LB 51	LB 50	LB 41	LB 40	LB 31	LB 30	LB 21	LB 20	LB 11	LB 10	LB 01	LB 00	1FFFF48EH	0000H[Note]/ 5555H/ AAAAH	R/W
Setting value	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1		00A9H	
Target CS	CSZ7		CSZ6		CSZ5		CSZ4		CSZ3		CSZ2		CSZ1		CSZ0				
Operation	–		–		–		–		32 bits		–		32 bits		16 bits				
Target	Unused		Unused		Unused		Unused		SDRAM		VSB_RAM		SRAM		Flash ROM				

Note This value is determined by the SLBS0 (SW1-2) and SLBS1 (SW1-1) pins. The PFESiP/V850EP1 should be started with a 16-bit width when starting it from an external ROM. The initial value of LBS at this time is 5555H.

(20) Page ROM configuration register (PRC)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
PRC	0	PRW2	PRW1	PRW0	0	0	0	0	0	0	0	0	MA6	MA5	MA4	MA3	1FFFF49AH	7000H	R/W
Setting value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1		1001H	
Operation	–				1 wait				–				1 Page=16 bits × 8						

(21) SDRAM configuration register 3 (SCR3)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
SCR3	LTC	LTM2	LTM1	LTM0	0	0	0	WCF	BCW1	BCW0	SSO1	SSO0	RAW1	RAW0	SAW1	SAW0	1FFFF4ACH	30C0H	R/W
Setting value	0	0	1	0	0	0	0	0	1	0	1	0	1	0	0	1		20A9H	
Operation	Normal		CL = 2		–		–		2 wait		32 bits		RAW=13		SAW=9				

(22) SDRAM refresh control register 3 (RFS3)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	After reset	R/W
RFS3	REN	0	0	0	0	0	RCC1	RCC0	0	0	RIN5	RIN4	RIN3	RIN2	RIN1	RIN0	1FFFF4AEH	0000H	R/W
Setting value	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0		800CH	
Operation	Enabled			–			Cfac=32			–			RIN=12						

(23) Write enable switch register (WREN)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
WREN	0	0	0	0	0	0	0	SWREN	1FFFF8B0H	01H	R/W
Setting value	0	0	0	0	0	0	0	1		01H	
Alternative function	BENZ0-BENZ3 / WRZ0-WRZ3										
Function selection	BENZ0-BENZ3										

(24) Register setting values

Table 4-2. Register Setting Values

address	Register Name	Register Symbol	Setting Example
1FFF F060H	Chip area select control register 0	CSC0	4827H
1FFF F062H	Chip area select control register 1	CSC1	Not set
1FFF F066H	Bus size configuration register	BSC	Initial value used
1FFF F06AH	Cache area specification register	BHC	Not set
1FFF F06EH	NPB strobe wait control register	VSWC	0042H
1FFF F44CH	Port 6 mode control register	PMC6	FFH
1FFF F44EH	Port 7 mode control register	PMC7	0BH
1FFF F450H	Port 8 mode control register	PMC8	Not set
1FFF F452H	Port 9 mode control register	PMC9	FFH
1FFF F454H	Port 10 mode control register	PMC10	FFH
1FFF F480H	Bus cycle type configuration register 0	BCT0	B089H
1FFF F482H	Bus cycle type configuration register 1	BCT1	Not set
1FFF F484H	Data wait control register 0	DWC0	0003H
1FFF F486H	Data wait control register 1	DWC1	Not set
1FFF F488H	Bus cycle control register	BCC	0001H
1FFF F48AH	Address setting wait control register	ASC	0000H
1FFF F48CH	Bus cycle control register	BCP	Not set
1FFF F48EH	Local bus sizing control register	LBS	00A9H
1FFF F494H	DMA flyby transfer wait control register	FWC	Not set
1FFF F496H	DMA flyby transfer idle control register	FIC	Not set
1FFF F498H	Bus mode control register	BMC	Not set
1FFF F49AH	Page ROM configuration register	PRC	1001H
1FFF F4A4H	SDRAM configuration register 1	SCR1	Not set
1FFF F4A6H	SDRAM refresh control register 1	RFS1	Not set □
1FFF F4ACH	SDRAM configuration register 3	SCR3	20A9H
1FFF F4AEH	SDRAM refresh control register 3	RFS3	800CH
1FFF F4B0H	SDRAM configuration register 4	SCR4	Not set
1FFF F4B2H	SDRAM refresh control register 4	RFS4	Not set
1FFF F4B8H	SDRAM configuration register 6	SCR6	Not set
1FFF F4BAH	SDRAM refresh control register 6	RFS6	Not set
1FFF F8B0H	Write enable switch register	WREN	Initial value used

4.2.1 PFESiP/V850EP1 start procedure

The PFESiP/V850EP1 starts fetching instruction after a reset is released when it has completed waiting for oscillation stabilization and the on-chip PLL to be locked.

Initialize the PFESiP/V850EP1 according to the following sequence.

(1) When not using on-chip instruction RAM (always fetching instructions with external memory)

Fetching instructions is started from address 0000 0000H in the external memory after a reset is released. First, use an execution program to set the following registers that affect the external bus access performance.

Fetching instructions from address 0000 0000H is also started by inputting a reset while the power is turned on.

- NPB strobe wait control register (VSWC)
  On-chip peripheral I/O (NPB) access wait setting
- Data wait control registers 0, 1 (DWC0, DWC1)
  External bus data wait setting
- Address setting wait control register (ASC)
  External bus address setup wait setting
- Bus cycle control register (BCC)
  External bus idle state setting

Set registers such as chip area select control registers 0 and 1 (CSC0, CSC1), bus cycle type configuration registers 0 and 1 (BCT0, BCT1), the local bus sizing control register (LBS), and the page ROM configuration register (PRC) as required.

	Manipulation Procedure
<1>	Starting booting from external memory after releasing system reset
<2>	Normal program start

(2) Disabling on-chip instruction RAM → Enabling on-chip instruction RAM: (Changing during program execution)

Fetching instructions from address 0000 0000H in the external memory is started after a reset is released.
First, use the execution program to check/set the following registers that affect the external bus access performance.
The instruction RAM (iLB_RAM) cannot be accessed from the CPU (NBA85E2S) because the instruction RAM (iLB_RAM) is disabled, but the DMAC (NBA85E300) connected to the CPU (NBA85E2S) can specify the instruction RAM (iLB_RAM) as the DMA transfer destination setting in the external DMA addressing control register DMXADCn (n = 0 to 3). If the instruction RAM (iLB_RAM) is specified as the transfer destination, DMA transfer can be performed for the instruction RAM (iLB_RAM).
The program is started from the external memory when starting the CPU (NBA85E2S) and the contents of the external memory are transferred to the instruction RAM (iLB_RAM) using this function. After the transfer is completed, fetching instructions from the instruction RAM (iLB_RAM) is started by enabling the instruction RAM (iLB_RAM) using the iLB RAM control register and jumping to address 0000 0000H.
The V850E2 architecture enables program execution from the data RAM (dLB_RAM) area. Executing the program to perform DMA transfer from the external memory to the instruction RAM (iLB_RAM) and re-setting the on-chip instruction RAM (iLB_RAM) using the iLB RAM control register (ILBEN) is executed using the data RAM (dLB_RAM).
The stages before and after downloading to the instruction RAM (iLB_RAM) can be identified by checking the iLB RAM control register setting when fetching instructions from address 0000 0000H.

- iLB RAM control register (ILBEN)
  Instruction RAM (iLB_RAM) area (iLB0 area) check
- NPB strobe wait control register (VSWC)
  On-chip peripheral I/O (NPB) access wait setting
- Data wait control registers 0, 1 (DWC0, DWC1)
  External bus data wait setting
- Address setting wait control register (ASC)
  External bus address setup wait setting
- Bus cycle control register (BCC)
  External bus idle state setting

Set registers such as chip area select control registers 0 and 1 (CSC0, CSC1), bus cycle type configuration registers 0 and 1 (BCT0, BCT1), the local bus sizing control register (LBS), and the page ROM configuration register (PRC) as required.

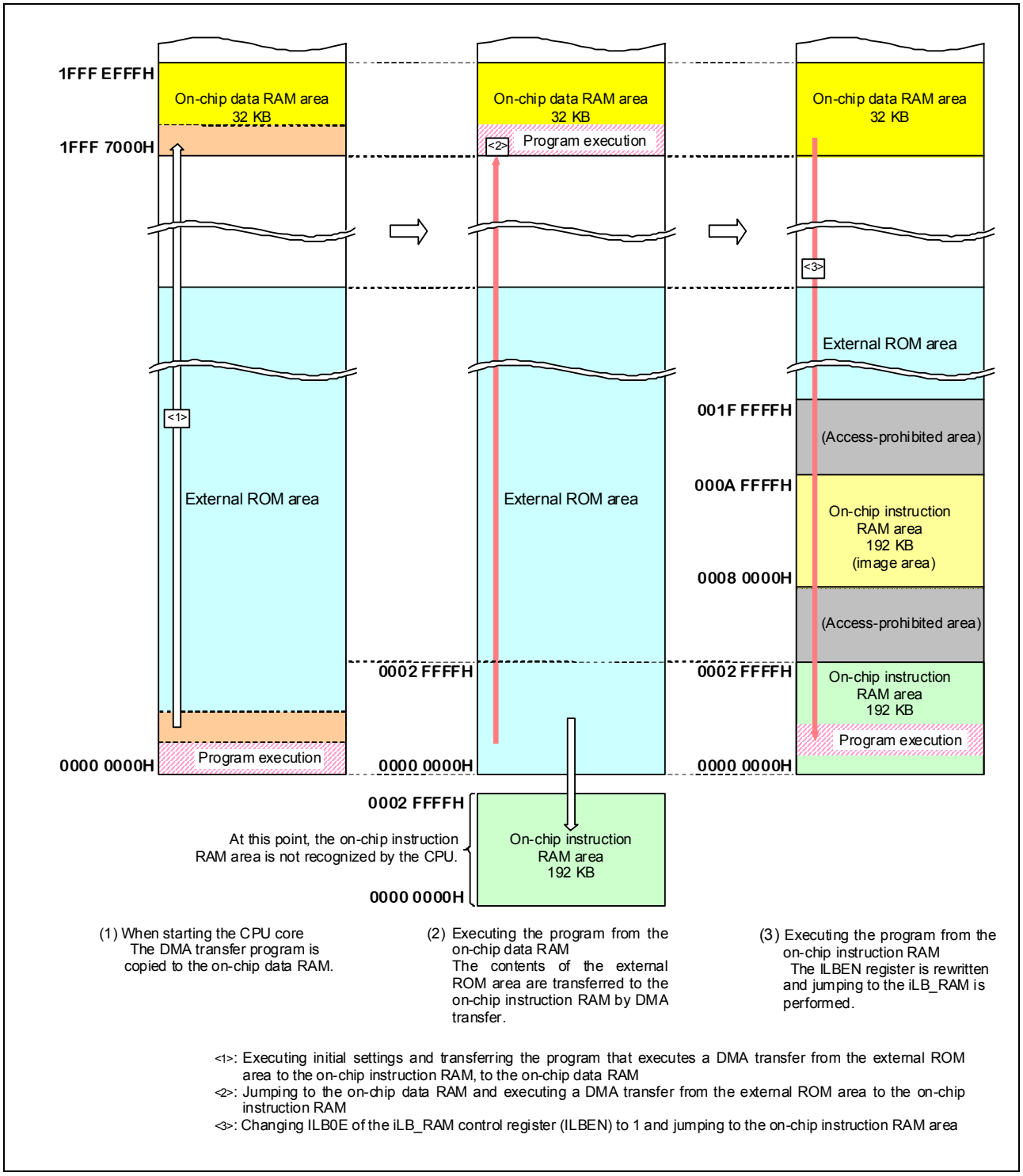
	Manipulation Procedure
<1>	Starting booting from external ROM after releasing system reset
<2>	Identifying iLB0E of iLB RAM control register (ILBEN) (iLB0E = 0)
<3>	Transferring program transferring external ROM contents to instruction RAM (iLB_RAM) to data RAM (dLB_RAM) area
<4>	Jumping to data RAM (dLB_RAM) transfer program
<5>	Transferring the contents of addresses 0000 0000H to 0002 FFFFH in external memory to addresses 0000 0000H to 0002 FFFFH in instruction RAM (iLB_RAM) area by DMA transfer
<6>	Setting iLB0E of iLB RAM control register (ILBEN) to 1 (verifying ILBEN register after writing)
<7>	Starting booting from on-chip instruction RAM (iLB_RAM) after jumping to address 0
<8>	Identifying iLB0E of iLB RAM control register (ILBEN) (iLB0E = 1)
<9>	Normal program start

Caution Set SDRAM configuration registers 1, 3, 4, and 6 (SCR1, SCR3, SCR4, and SCR6) after process <3>.

Remark Maskable interrupt requests generated while interrupts are disabled (DI state) are suspended. The maskable interrupt requests will be acknowledged immediately after the interrupt enable state (EI state) is set, if the interrupt requests are not cleared (the xxIFn bit of the interrupt control register (xxICn) is not cleared (0)) and the xxMKn bit of the interrupt control register is not set (1). Only one interrupt request, however, will be suspended for a single interrupt source, and only one interrupt request will be acknowledged even if two or more of the same interrupt request are generated.

An example in which the program is executed by copying the contents of the external ROM to the instruction RAM (iLB_RAM) is shown below.

Figure 4-1. Transfer from External ROM to Instruction RAM (iLB_RAM)



CHAPTER 5 USING EXPANSION CONNECTORS

The PFESiP EP-1 Evaluation Board has three types of expansion connectors.

Among these connectors, CN6, CN7, and CN9 are compatible with MICROSSP Evaluation Board #1/MICROSSP Evaluation Board #3. A connector (MICTOR plug) for stacking multiple units of this board is also available.

Connector Shape[Note]	No. of Pins	Connector No.	No. of Signals	Subtotal
AMP MICTOR receptacle	152×3 = 456	CN6	91 dedicated to MEMC I/F	112
			1 dedicated to FPGA clock	
			20 for FPGA general purposes All shared with CN8	
		CN7	109 for FPGA general purposes Among which 12 are shared with CN10	110
			1 VBCLKOUT	
		CN9	111 for FPGA general purposes	112
			1 DONE signal[Note]	
General-purpose 50-pin connector	50×2 = 100	CN8	40 for FPGA general purposes Among which 20 are shared with CN6	40
		CN10	40 for FPGA general purposes Among which 12 are shared with CN7	40
General-purpose 50-pin connector	50×2 = 100	CN11	For PFESiP/V850EP1 I/Os	40
		CN12	For PFESiP/V850EP1 I/Os	40
AMP MICTOR plug	152×2 = 304	CN13	Same signals as CN7 are placed. No VBCLKOUT output, no power supply.	109
		CN14	Same signals as CN9 are placed. No power supply.	112

Note Only some of the above connectors may be mounted for mass-products.

Caution The FPGA DONE signal output from an expansion board must be output as an open-drain signal. It is connected with the FPGA DONE signal of this board and the DONE signal of the evaluation board stacked under this board by wired OR.

Numerous GPIOs of the on-board FPGA are connected to the expansion connectors. Any signal can therefore be connected to the connectors by the on-board FPGA. Note, however, that the operating speed drops depending on the length of the signal lines. Note the stack height when using a general-purpose 50-pin connector together with another connector. Also, note the signals shared between the connectors.

Remark The PFESiP EP-1 Evaluation Board is provided with expansion connectors compatible with conventional MICROSSP Evaluation Board #1. A stack board developed for MICROSSP Evaluation Board #1 can also be used for the PFESiP EP-1 Evaluation Board by programming the on-board FPGA.

5.1 AMP MICTOR Connector (CN6, CN7, CN9, CN13, CN14)

The external bus interface of the PFESiP/V850EP1 and FPGA general-purpose signals are connected to these connectors.

By developing a stack board using these connectors, external memory devices can be added and an interface circuit for connecting to the user system can be built.

CN6, CN7, CN9, CN13, and CN14 are connected to the following signals.

Connector No.	Connected Signal	Count
CN6 (152 pins)	External memory interface signal	90
	Bus reset output (VBRESTOZ) signal	1
	FPGA external clock input signal	1
	FPGA general-purpose signal	20
	GND	28
	+5.0 V power supply	6
	+3.3 V power supply	6
CN7, CN13 (152 pins)	FPGA general-purpose signal	109
	GND	28
	VBCLKOUT (not connected to CN13 and left open)	1
	+5.0 V power supply	7
	+3.3 V power supply	7
CN9, CN14 (152 pins)	FPGA general-purpose signal	111
	GND	28
	DONE3 (FPGA DONE signal from stack board or evaluation board stacked underneath. Connected by open-drain signal from each board. Connected to reset generator. Provided with JP for turning pull-up to on/off)	1
	+5.0 V power supply	6
	+3.3 V power supply	6

Some FPGA signals assigned to the AMP MICTOR connectors are shared with simplified connectors (CN8, CN10). Exercise caution when using both connectors at the same time.

5.1.1 Supported plugs

When stacking another board on the PFESiP EP-1 Evaluation Board, consider the following supported plugs.

Two units of the MICTOR 2-767004-5 (152-pin receptacle) made by AMP are used as the connectors.

For a plug supporting the MICTOR 2-767004-5 (152-pin receptacle) made by AMP, select a plug by referring to the following table to select the stack height..

Product Name	Total Height from Board Surface
1-767005-1	About 12.5 mm
5767042-4	About 18.75
5767017-4	About 22.86 mm

Remark Contact Tyco Electronics AMP K.K. for details.

5.1.2 Receptacles used when stacking boards

When stacking the PFESiP EP-1 Evaluation Board on another board that complies with the same connector standard, consider the following receptacles.

The following considers the interference by a mounted state of the PFESiP/V850EP1 or an on-board FPGA when two PFESiP EP-1 Evaluation Boards are stacked. Consider also other projections when actually stacking boards.

Product No.	Tallied Length	Mounted State of PFESiP/V850EP1		Mounted State of FPGA	
		Socket Mounted	Device Mounted	Socket Mounted	Device Mounted
5767017-4	About 22.86 mm	Stackable	Stackable	Stackable	Stackable
5767042-4	About 18.75 mm	Stackable	Stackable	Not stackable	Stackable
1-5767005-1	About 12.57 mm	Not stackable	Stackable	Not stackable	Stackable

5.1.3 Signal assignment of connectors

(1) CN6 … External memory interface+ FPGA general purposes

Table 5-1. CN6 (MICTOR) Pin Layout

No.	Signal Name	Signal Name	No.
1	GND	RDZ	2
3	WRSTBZ	BENZ0_WRZ0	4
5	BENZ1_WRZ1	GND	6
7	BENZ2_WRZ2	BENZ3_WRZ3	8
9	A25_P65	A24_P64	10
11	GND	A23_P63	12
13	A22_P62	A21_P61	14
15	A20_P60	GND	16
17	A19	A18	18
19	A17	A16	20
21	GND	A15	22
23	A14	A13	24
25	A12	GND	26
27	A11	A10	28
29	A9	A8	30
31	GND	A7	32
33	A6	A5	34
35	A4	GND	36
37	A3	A2	38
39	A1_P67	A0_P66	40
41	GND	D0	42
43	D1	D2	44
45	D3	GND	46
47	D4	D5	48
49	D6	D7	50
51	GND	D8	52
53	D9	D10	54
55	D11	GND	56
57	D12	D13	58
59	D14	D15	60
61	GND	D16_P90	62
63	D17_P91	D18_P92	64
65	D19_P93	GND	66
67	D20_P94	D21_P95	68
69	D22_P96	D23_P97	70
71	GND	D24_P100	72
73	D25_P101	D26_P102	74
75	D27_P103	GND	76

Continued to the table on the right

Continued from table on the left

77	D28_P104	D29_P105	78
79	D30_P106	D31_P107	80
81	GND	BCYSTZ	82
83	CSZ0	CSZ1_P71	84
85	CSZ2_P72	GND	86
87	CSZ3_P73	CSZ4_P74	88
89	CSZ5_P75	CSZ6_P76	90
91	GND	CSZ7_P77	92
93	SDCKE	SDRASZ	94
95	SDCASZ	GND	96
97	REFRQZ	Pull Up 10k□	98
99	WAITZ	DQM0	100
101	GND	DQM1	102
103	DQM2	DQM3	104
105	SELFREFZ	GND	106
107	SDWEZ	BUSCLK	108
109	IOWRZ	IORDZ	110
111	GND	HLDAKZ	112
113	HLDRQZ	VBRESETOZ	114
115	CN_CLK	GND	116
117	GPIO220	GPIO221	118
119	GPIO222	GPIO223	120
121	GND	GPIO224	122
123	GPIO225	GPIO226	124
125	GPIO227	GND	126
127	GPIO228	GPIO229	128
129	GPIO230	GPIO231	130
131	GND	GPIO232	132
133	GPIO233	GPIO234	134
135	GPIO235	GND	136
137	GPIO236	GPIO237	138
139	GPIO238	GPIO239	140
141	+3.3 V	+5 V	142
143	+3.3 V	+5 V	144
145	+3.3 V	+5 V	146
147	+3.3 V	+5 V	148
149	+3.3 V	+5 V	150
151	+3.3 V	+5 V	152

(2) CN7 … FPGA general purposes

Table 5-2. CN7, CN13 (MICTOR) Pin Layout

No.	Signal Name	Signal Name	No.
1	GND	GPIO111	2
3	GPIO112	GPIO113	4
5	GPIO114	GND	6
7	GPIO115	GPIO116	8
9	GPIO117	GPIO118	10
11	GND	GPIO119	12
13	GPIO120	GPIO121	14
15	GPIO122	GND	16
17	GPIO123	GPIO124	18
19	GPIO125	GPIO126	20
21	GND	GPIO127	22
23	GPIO128	GPIO129	24
25	GPIO130	GND	26
27	GPIO131	GPIO132	28
29	GPIO133	GPIO134	30
31	GND	GPIO135	32
33	GPIO136	GPIO137	34
35	GPIO138	GND	36
37	GPIO139	GPIO140	38
39	GPIO141	GPIO142	40
41	GND	GPIO143	42
43	GPIO144	GPIO145	44
45	GPIO146	GND	46
47	GPIO147	GPIO148	48
49	GPIO149	GPIO150	50
51	GND	GPIO151	52
53	GPIO152	GPIO153	54
55	GPIO154	GND	56
57	GPIO155	GPIO156	58
59	GPIO157	GPIO158	60
61	GND	GPIO159	62
63	GPIO160	GPIO161	64
65	GPIO162	GND	66
67	GPIO163	GPIO164	68
69	GPIO165	GPIO166	70
71	GND	GPIO167	72
73	GPIO168	GPIO169	74
75	GPIO170	GND	76

Continued to the table on the right

Continued from table on the left

77	GPIO171	GPIO172	78
79	GPIO173	GPIO174	80
81	GND	GPIO175	82
83	GPIO176	GPIO177	84
85	GPIO178	GND	86
87	GPIO179	GPIO180	88
89	GPIO181	GPIO182	90
91	GND	GPIO183	92
93	GPIO184	GPIO185	94
95	GPIO186	GND	96
97	GPIO187	GPIO188	98
99	GPIO189	GPIO190	100
101	GND	GPIO191	102
103	GPIO192	GPIO193	104
105	GPIO194	GND	106
107	GPIO195	GPIO196	108
109	GPIO197	GPIO198	110
111	GND	GPIO199	112
113	GPIO200	GPIO201	114
115	GPIO202	GND	116
117	GPIO203	GPIO204	118
119	GPIO205	GPIO206	120
121	GND	GPIO207	122
123	GPIO208	GPIO209	124
125	GPIO210	GND	126
127	GPIO211	GPIO212	128
129	GPIO213	GPIO214	130
131	GND	GPIO215	132
133	GPIO216	GPIO217	134
135	GPIO218	GND	136
137	GPIO219	STBUSCLK Note	138
139	+3.3 V Note	+5 V Note	140
141	+3.3 V Note	+5 V Note	142
143	+3.3 V Note	+5 V Note	144
145	+3.3 V Note	+5 V Note	146
147	+3.3 V Note	+5 V Note	148
149	+3.3 V Note	+5 V Note	150
151	+3.3 V Note	+5 V Note	152

Note CN7 is connected to STBUSCLK of the PFESiP/V850EP1 and CN13 to the FPGA with the signal STCK_STBUSCLK. The +3.3 V and +5 V power supplies of pins 139 to 152 are not supplied to CN13 and are left open.

(3) CN9 … FPGA general purposes

Table 5-3. CN9, CN14 (MICTOR) Pin Layout

No.	Signal Name	Signal Name	No.
1	GND	GPIO0	2
3	GPIO1	GPIO2	4
5	GPIO3	GND	6
7	GPIO4	GPIO5	8
9	GPIO6	GPIO7	10
11	GND	GPIO8	12
13	GPIO9	GPIO10	14
15	GPIO11	GND	16
17	GPIO12	GPIO13	18
19	GPIO14	GPIO15	20
21	GND	GPIO16	22
23	GPIO17	GPIO18	24
25	GPIO19	GND	26
27	GPIO20	GPIO21	28
29	GPIO22	GPIO23	30
31	GND	GPIO24	32
33	GPIO25	GPIO26	34
35	GPIO27	GND	36
37	GPIO28	GPIO29	38
39	GPIO30	GPIO31	40
41	GND	GPIO32	42
43	GPIO33	GPIO34	44
45	GPIO35	GND	46
47	GPIO36	GPIO37	48
49	GPIO38	GPIO39	50
51	GND	GPIO40	52
53	GPIO41	GPIO42	54
55	GPIO43	GND	56
57	GPIO44	GPIO45	58
59	GPIO46	GPIO47	60
61	GND	GPIO48	62
63	GPIO49	GPIO50	64
65	GPIO51	GND	66
67	GPIO52	GPIO53	68
69	GPIO54	GPIO55	70
71	GND	GPIO56	72
73	GPIO57	GPIO58	74
75	GPIO59	GND	76

Continued to the table on the right

Continued from table on the left

77	GPIO60	GPIO61	78
79	GPIO62	GPIO63	80
81	GND	GPIO64	82
83	GPIO65	GPIO66	84
85	GPIO67	GND	86
87	GPIO68	GPIO69	88
89	GPIO70	GPIO71	90
91	GND	GPIO72	92
93	GPIO73	GPIO74	94
95	GPIO75	GND	96
97	GPIO76	GPIO77	98
99	GPIO78	GPIO79	100
101	GND	GPIO80	102
103	GPIO81	GPIO82	104
105	GPIO83	GND	106
107	GPIO84	GPIO85	108
109	GPIO86	GPIO87	110
111	GND	GPIO88	112
113	GPIO89	GPIO90	114
115	GPIO91	GND	116
117	GPIO92	GPIO93	118
119	GPIO94	GPIO95	120
121	GND	GPIO96	122
123	GPIO97	GPIO98	124
125	GPIO99	GND	126
127	GPIO100	GPIO101	128
129	GPIO102	GPIO103	130
131	GND	GPIO104	132
133	GPIO105	GPIO106	134
135	GPIO107	GND	136
137	GPIO108	GPIO109	138
139	GPIO110	DONE3 Note	140
141	+3.3 V Note	+5 V Note	142
143	+3.3 V Note	+5 V Note	144
145	+3.3 V Note	+5 V Note	146
147	+3.3 V Note	+5 V Note	148
149	+3.3 V Note	+5 V Note	150
151	+3.3 V Note	+5 V Note	152

Note The FPGA DONE output from each board is connected to this signal as an open-drain output. The +3.3 V and +5 V power supplies of pins 139 to 152 are not supplied to CN13 and are left open.

5.2 Simplified Connectors (CN8, CN10)

Two 50-pin headers to which signals from the FPGA can be easily input or output are provided.

General-purpose flat cables with a 2.54 mm pitch by two rows can be used.

The connectors can be used as the pins for checking the circuit integrated to the FPGA.

Use the connectors for low-speed function evaluation, because they are not suitable for high-speed transfer when compared to AMP MICTOR connectors. Power must be separately supplied to an external circuit, because only GND is connected as a power supply.

Table 5-4. Simplified Connector (General-Purpose 50-Pin) Pin Layout

CN8 pin layout

No.	Signal Name	Signal Name	No.
1	GND	GPIO220	2
3	GPIO221	GPIO222	4
5	GPIO223	GND	6
7	GPIO224	GPIO225	8
9	GPIO226	GPIO227	10
11	GND	GPIO228	12
13	GPIO229	GPIO230	14
15	GPIO231	GND	16
17	GPIO232	GPIO233	18
19	GPIO234	GPIO235	20
21	GND	GPIO236	22
23	GPIO237	GPIO238	24
25	GPIO239	GND	26
27	GPIO240	GPIO241	28
29	GPIO242	GPIO243	30
31	GND	GPIO244	32
33	GPIO245	GPIO246	34
35	GPIO247	GND	36
37	GPIO248	GPIO249	38
39	GPIO250	GPIO251	40
41	GND	GPIO252	42
43	GPIO253	GPIO254	44
45	GPIO255	GND	46
47	GPIO256	GPIO257	48
49	GPIO258	GPIO259	50

CN10 pin layout

No.	Signal Name	Signal Name	No.
1	GND	GPIO260	2
3	GPIO261	GPIO262	4
5	GPIO263	GND	6
7	GPIO264	GPIO265	8
9	GPIO266	GPIO267	10
11	GND	GPIO268	12
13	GPIO269	GPIO270	14
15	GPIO271	GND	16
17	GPIO272	GPIO273	18
19	GPIO274	GPIO275	20
21	GND	GPIO276	22
23	GPIO277	GPIO278	24
25	GPIO279	GND	26
27	GPIO280	GPIO281	28
29	GPIO282	GPIO283	30
31	GND	GPIO284	32
33	GPIO285	GPIO286	34
35	GPIO287	GND	36
37	GPIO111	GPIO112	38
39	GPIO113	GPIO114	40
41	GND	GPIO115	42
43	GPIO116	GPIO117	44
45	GPIO118	GND	46
47	GPIO119	GPIO120	48
49	GPIO121	GPIO122	50

5.3 PFESiP/V850EP1 Port Output Connectors (CN11, CN12)

Two 50-pin headers for the port output of the PFESiP/V850EP1 are provided.
General-purpose flat cables with a 2.54 mm pitch by two rows can be used.
The output ports are those output to CN6 (memory controller pin) and those other than P154 to P157.
P154 to P157 are connected to the CN15 pin header.

Table 5-5. PFESiP/V850EP1 Ports Connected to CN11 and CN12

Port Name	Shared Pin
P00-P07	INTPZ0-INTPZ7
P10-P17	INTPZ8-INTPZ15
P20-P27	INTPZ16-INTPZ23
P30	RXD0
P31	TXD0
P32	RXD1
P33	TXD1
P34	RXD2
P35	TXD2
P36	RXD3
P37	TXD3
P40-P43	TI0-TI3
P44-P47	TCLR0-TCLR3
P50-P53	TO0-TO3
P54, P55	ETIUD0, ETIUD1
P56, P57	ETCUD0, ETCUD1

Port Name	Shared Pin
P110, P111	ETCLR0, ETCLR1
P112, P113	ETO0, ETO1
P114	EVTTRG
P115	DBINT
P116	ADTRG
P120-P123	TCZ0-TCZ3
P124-P127	DMAAKZ0-DMAAKZ3
P130-P133	DMARQZ0-DMARQZ3
P140	SCK0
P141	SI0
P142	SO0
P143	SCK1
P144	SI1
P145	SO1
P146-P147	PWMO0-PWMO1
P150-P153	INTPZ24-INTPZ27

Table 5-6. Simplified Connector (General-Purpose 50-Pin) Pin Layout

CN11 pin layout

No.	Signal Name	Signal Name	No.
1	GND	P130	2
3	P131	P132	4
5	P133	GND	6
7	P120	P121	8
9	P122	P123	10
11	GND	P124	12
13	P125	P126	14
15	P127	GND	16
17	P150	P151	18
19	P152	P153	20
21	GND	P110	22
23	P111	P112	24
25	P113	GND	26
27	P114	P115	28
29	P116	P10	30
31	GND	P11	32
33	P12	P13	34
35	P14	GND	36
37	P15	P16	38
39	P17	P40	40
41	GND	P41	42
43	P42	P43	44
45	P44	GND	46
47	P45	P46	48
49	P47	P47	50

CN12 pin layout

No.	Signal Name	Signal Name	No.
1	GND	P50	2
3	P51	P52	4
5	P53	GND	6
7	P54	P55	8
9	P56	P57	10
11	GND	P00	12
13	P01	P02	14
15	P03	GND	16
17	P04	P05	18
19	P06	P07	20
21	GND	P140	22
23	P141	P142	24
25	P143	GND	26
27	P144	P145	28
29	P146	P147	30
31	GND	P30	32
33	P31	P32	34
35	P33	GND	36
37	P34	P35	38
39	P36	P37	40
41	GND	P20	42
43	P21	P22	44
45	P23	GND	46
47	P24	P25	48
49	P26	P27	50

5.4 PFESiP/V850EP1 P154 to P157 Header (CN15)

P154 to P157, which cannot be handled with CN11 and CN12, are connected to CN15.

Table 5-7. Pin Headers (CN15) Pin Layout

CN15 Pin Layout

No.	Signal Name	Signal Name	No.
1	P154	P155	2
3	P156	P157	4

CHAPTER 6 EMULATION CONNECTOR

6.1 N-Wire Interface

Position	Figure 1-1 (Appearance) B-1

The PFESiP/V850EP1 incorporates an on-chip debug function (debug control unit: DCU).

A MICTOR connector (2-5767004-2) made by AMP is provided as a connector to connect this DCU to the in-circuit emulator supporting N-Wire.

The DCU trace function incorporated in the PFESiP/V850EP1 can perform 8-bit tracing when fully used.

The RTE-NEC/MICTOR38-2K is the connection cable for using the RTE-2000-TP made by Midas lab as the in-circuit emulator. The PB-JTAG-N-A36 is the connection cable for using the RTE-2000H-TP.

The advicePLUS YN601 made by Yokogawa Digital Computer and the PARTNER-Jet made by Kyoto Microcomputer can also be used as the in-circuit emulator.[Note 1]

The affordable MINICUBE (QB-V850MINI) made by NEC Electronics can also be used when not using the trace function.[Note 2]

Note 1. With the PARTNER-Jet, the number of traces is four.

2. The NEC N-Wire probe (model number: JETMIPSNWC) and N-Wire to MICTOR (model number: CMIPN-MI) of Kyoto Microcomputer Co., Ltd. are required for connecting the PARTNER-Jet and PFESiP EP-1 Evaluation Board.

3. The Mictor Adaptor (B-137A: straight product) of Sumitomo Heavy Industries Mechatronics, Ltd. is required for connecting the QB-V850MINI and PFESiP EP-1 Evaluation Board. A B-137 (right angle product) cannot be used.
Purchase the Mictor Adaptor from the IE-V850E1-CD-NW option FAX ordering table at the following URL..
http://www.shi-mechatronics.jp/products/zax/index.html

Remarks 1. Contact an agency of Midas lab, Inc. for how to use the RTE-2000-TP

2. Contact Yokogawa Digital Computer Corporation for how to use the advicePLUS.

3. Contact Kyoto Microcomputer Co., Ltd. for how to use the PARTNER-Jet

4. The PARTNER-Jet includes the PARTNER as the debugger.

5. Documents related to the QB-V850MINI can be downloaded from the following URL.
http://www.necel.com/cgi-bin/nesdis/o003.cgi?article=QB-V850MINI

6. The QB-V850MINI includes the ID-850QB as the debugger.

Table 6-1. N-Wire connector (CN1)

Purpose	Pin No.	Signal Name
GND	1	GND
PFESiP/V850EP1 (DCK)	3	DCK
PFESiP/V850EP1 (DMS)	5	DMS
PFESiP/V850EP1 (DDI)	7	DDI
PFESiP/V850EP1 (DDO)	9	DDO
OPEN	11	Reserved 1
OPEN	13	Reserved 2
OPEN	15	Reserved 3
PFESiP/V850EP1 (TRCCLK)	17	TRCCLK
PFESiP/V850EP1 (TRCEND)	19	TRCEND
PFESiP/V850EP1 (TRCDATA0)	21	TRCDATA0
PFESiP/V850EP1 (TRCDATA1)	23	TRCDATA1
PFESiP/V850EP1 (TRCDATA2)	25	TRCDATA2
PFESiP/V850EP1 (TRCDATA3)	27	TRCDATA3
PFESiP/V850EP1 (TRCDATA4)	29	TRCDATA4
PFESiP/V850EP1 (TRCDATA5)	31	TRCDATA5
PFESiP/V850EP1 (TRCDATA6)	33	TRCDATA6
PFESiP/V850EP1 (TRCDATA7)	35	TRCDATA7
GND	37	GND

Signal Name	Pin No.	Purpose
GND	2	GND
V_{DD}	4	3.3 V
DRSTZ	6	PFESiP/V850EP1 (DRST)
PORT0_OUT	8	PFESiP/V850EP1 (P115)
PORT1_OUT	10	PFESiP/V850EP1 (RMODEZ)
PORT2_OUT	12	PFESiP/V850EP1 (EVIN)
PORT0_IN	14	PFESiP/V850EP1 (P114)
PORT1_IN	16	OPEN
PORT2_IN	18	OPEN
TRCCE	20	PFESiP/V850EP1 (TRCCE)
TRCDATA8	22	Connection to GND
TRCDATA9	24	Connection to GND
TRCDATA10	26	Connection to GND
TRCDATA11	28	Connection to GND
TRCDATA12	30	Connection to GND
TRCDATA13	32	Connection to GND
TRCDATA14	34	Connection to GND
TRCDATA15	36	Connection to GND
GND	38	GND

Figure 6-1. Connection with RTE-2000-TP (RTE-NEC/MICTOR38-2K)

Figure 6-2. Connection with RTE-2000H-TP (PB-JTAG-N-A36)

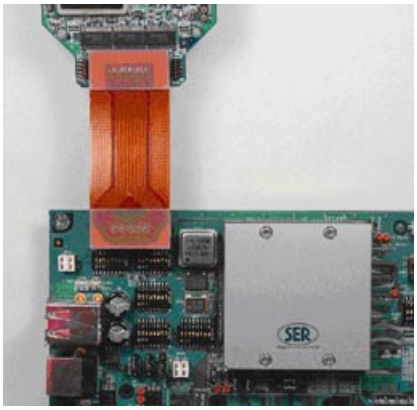
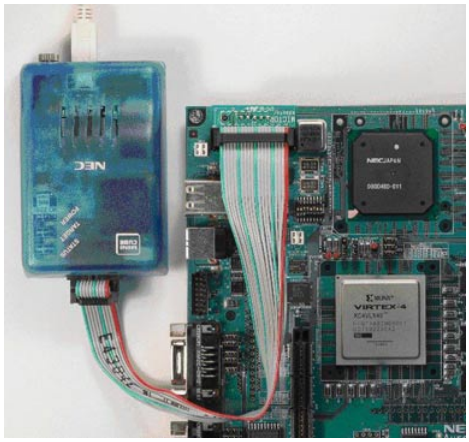


Figure 6-3. Connection with MINI CUBE (QB-V850MINI + B-137A)



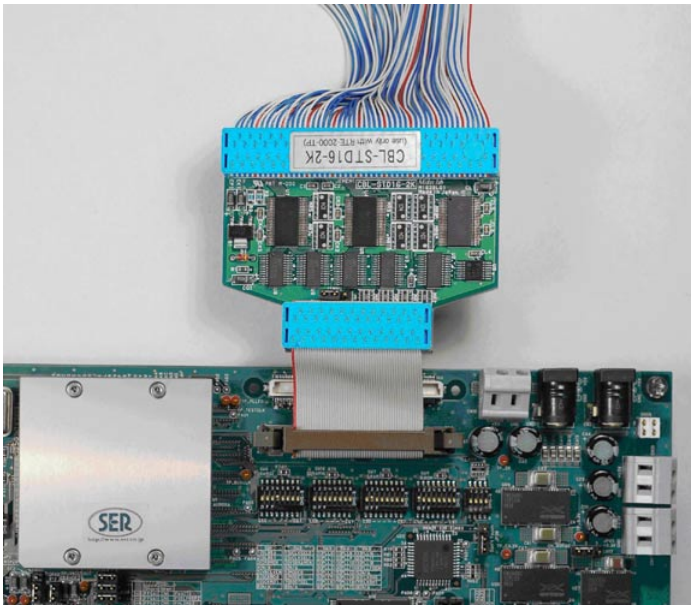
6.2 ROM Cable Connector (for Midas)

Position	Figure 1-1 (Appearance) F-2

The PFESiP EP-1 Evaluation Board has an on-board ROM cable connector for the RTE-2000-TP made by Midas lab. The CBL-STD16-2K made by Midas lab is used as the ROM cable connector.

When the power of the RTE-2000-TP and PFESiP EP-1 Evaluation Board is turned on while the ROM cable connector is connected, the on-board flash ROM will be disabled and the ROM cable connector will be given precedence.

Figure 6-4. Connection with RTE-2000-TP (ROM Cable Connector)



Caution When using the on-board flash ROM, including when writing to the flash ROM, do not connect the ROM cable connector.
The ROM cable connector and the on-board flash ROM are placed in the same space and are exclusively used. When the PFESiP EP-1 Evaluation Board is started with the ROM cable connector connected, the on-board flash ROM function cannot be used.

Remark Contact an agency of Midas lab, Inc. for how to use the ROM cable connector and RTE-2000-TP.

6.3 SDRAM Bus Tracer Connector (for advice)

Position	Figure 1-1 (Appearance) F-1

The PFESiP EP-1 Evaluation Board is provided with the SDRAM bus tracer connector of the advicePLUS YN601 made by Yokogawa Digital Computer.

Figure 6-5. Connection with advicePLUS YN601 (SDRAM Bus Tracer)

Remark Contact Yokogawa Digital Computer Corporation for how to use the SDRAM bus tracer.

CHAPTER 7 ON-BOARD LARGE-CAPACITY FPGA

Position	Figure 1-1 (Appearance) D-4

The PFESiP EP-1 Evaluation Board is a PFESiP development assistance board based on the PFESiP/V850EP1.

The functions of the embedded array (EA-9HD) paired with the PFESiP/V850EP1 in the SiP are replaced with an on-board FPGA. Specifically, the SiP internal connection buses connected in the SiP are all connected to the on-board FPGA.

Numerous GPIOs of the on-board FPGA are connected to the expansion connectors and any signal can be connected to the connectors by the on-board FPGA.

The FPGA is a product in the Virtex-4 Family LX Series made by Xilinx. The XC4VLX40FF1148-11 is mounted as the standard FPGA.

The FPGA is configured using a flash ROM (XCF32PFSG48C) and programming can be performed from a personal computer by connecting the Platform Cable USB to the JTAG connector. The FPGA can also be directly configured from JTAG without using the XCF32PFSG48C.

Remark The XCF08PFSG48C of configuration ROM2 is an optional product used only when using the XC4VLX160 as the FPGA. In this case, the PFESiP EP-1 Evaluation Board is shipped with 2-3 of JP44 shorted.

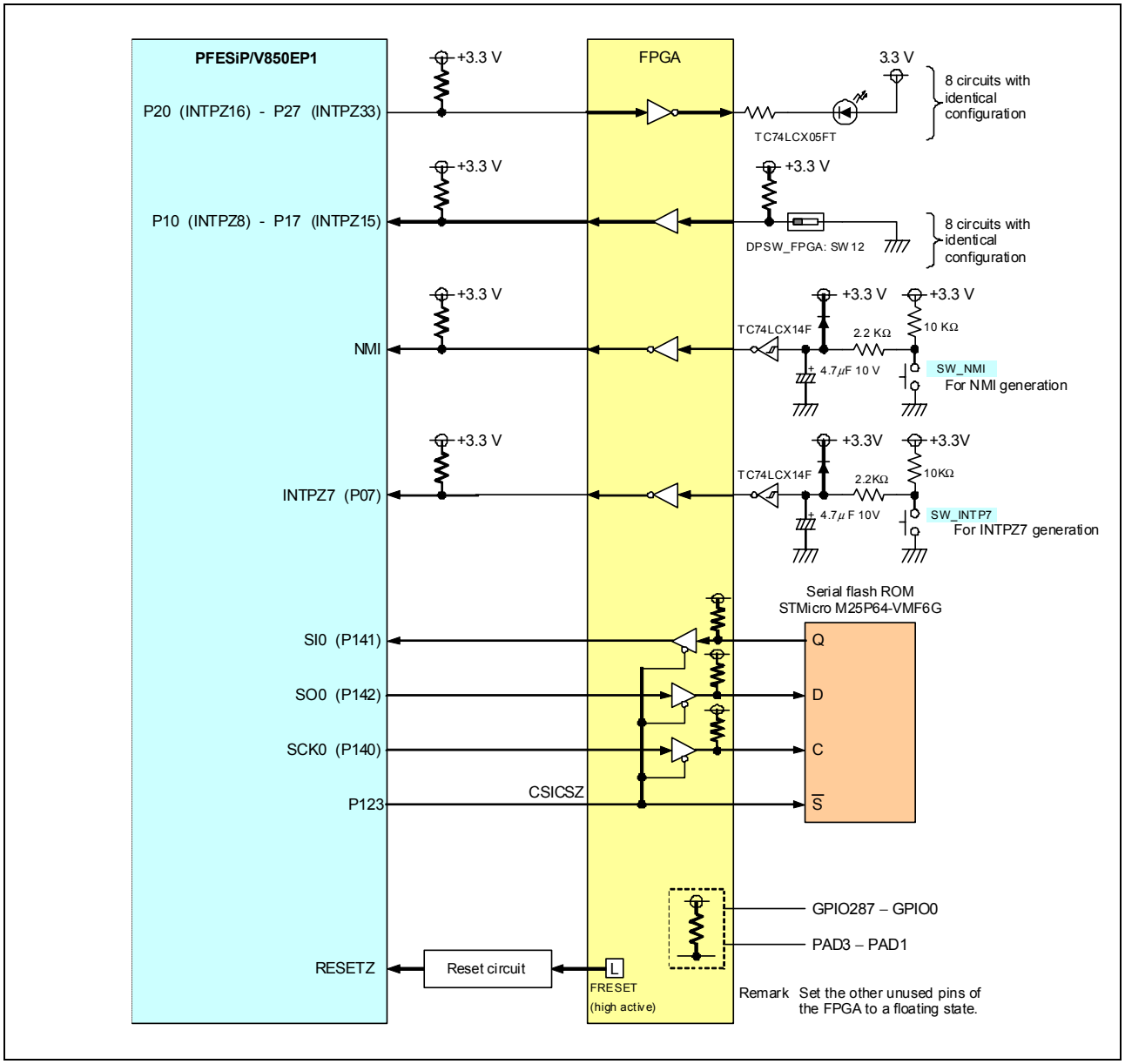
7.1 Default FPGA Programming

The FPGA is intended to be used for application evaluation of the PFESiP/V850EP1 and a user ASIC (embedded array (EA-9HD)), but only the minimum of functions are programmed when it is shipped.

P20 to P27, P10 to P17, NMI, and INTPZ7 are connected as follows. This enables the lighting of the LEDs and level input from a dip switch (FPGA_DPSW: SW12) by the PFESiP/V850EP1 via the FPGA.

The on-board serial ROM is connected to channel 0 of the on-chip clocked serial interface of the PFESiP/V850EP1.

Figure 7-1. Default FPGA Programming



7.1.1 VerilogHDL source of default PFESiP/V850EP1 data

Default PFESiP/V850EP1Default1.v file (1/2)

```
//-----------------------------------------------------
//
//  Library Name :  AuroraDefault
//  Unit    Name :  AuroraDefault
//  Unit    Type :  Block Diagram
//
//-----------------------------------------------------


module AuroraDefault (NMI_IN, P2, P1, SROM_D, LED, INTPZ, SROM_Q, SROM_CLK,
                      SROM_S, GPIO, DIPSW, SW_INTP7, NMI_OUT, FRESET, PAD, CSICSZ, SCK, SO, SI
                      );

  inout SROM_D;
  wire SROM_D;
  inout SROM_Q;
  wire SROM_Q;
  inout SROM_CLK;
  wire SROM_CLK;
  inout SROM_S;
  wire SROM_S;
  input CSICSZ;
  wire CSICSZ;
  input [0:0] SCK;
  wire [0:0] SCK;
  input [0:0] SO;
  wire [0:0] SO;
  output [0:0] SI;
  wire [0:0] SI;

  inout [287:0] GPIO;
  wire [287:0] GPIO;
  inout [3:1] PAD;
  wire [3:1] PAD;

  output [8:1] LED;
  wire [8:1] LED;
  input [7:0] P2;
  wire [7:0] P2;
  output [7:0] P1;
  wire [7:0] P1;
  input [8:0] DIPSW;
  wire [8:0] DIPSW;
  output NMI_OUT;
  wire NMI_OUT;
  input NMI_IN;
  wire NMI_IN;
  output [7:7] INTPZ;
  wire [7:7] INTPZ;
  input SW_INTP7;
  wire SW_INTP7;
  output FRESET;
  wire FRESET;
  wire CSZ;
```

Default PFESiP/V850EP1Default1.v file (2/2)

```
assign LED[8:1] = ~ (P2[7:0]);

  assign P1[7:0] = DIPSW[8:1];

  assign NMI_OUT = ~ (NMI_IN);

  assign INTPZ[7] = ~ (SW_INTP7);

  assign FRESET = 1'b1;

  assign SROM_CLK = (CSICSZ == 1'b0) ? SCK[0] : 1'bz;

  assign SROM_S = CSICSZ;

  assign SROM_D = (CSICSZ == 1'b0) ? SO[0] : 1'bz;

  assign SI[0] = (CSICSZ == 1'b0) ? SROM_Q : 1'bz;

  assign CSZ = 1'b0;


endmodule
```

7.2 Default FPGA Data

A setting file corresponding to the ISE software made by Xilinx is provided for the default programming of the on-board FPGA.

7.2.1 FPGA data generation environment

The Virtex-4 Family LX Series made by Xilinx is employed as the FPGA and the XC4VLX40FF1148-11 is mounted as standard.

The version of the placement and routing tool is shown below.

Placement and routing tool	ISE8.1

Caution Be sure to use the placement and routing tool of the version stated above.

7.2.2 File explanation

The TOP directory is PFESiP/V850EP1Default1.

Only the main files are explained in Table 7-1.

Table 7-1. Explanation of Files Directly under TOP Directory

File Name	Related Tool	Purpose
AuroraDefault1.ise	ISE	ISE project file
AuroraDefault1.v	Editor, etc.	VerilogHDL source of default data
AuroraDefault1.ucf	ISE	File storing pin layout information, device information, and information of each option setting
AuroraDefault1.bit Note	ISE	File that can be directly downloaded to the FPGA
AuroraDefault1.mcs Note	ISE	File to be written to the FPGA download ROM

Note The above bit file is recommended to be backed up, taking into consideration that ICE may not start in a newly created circuit.

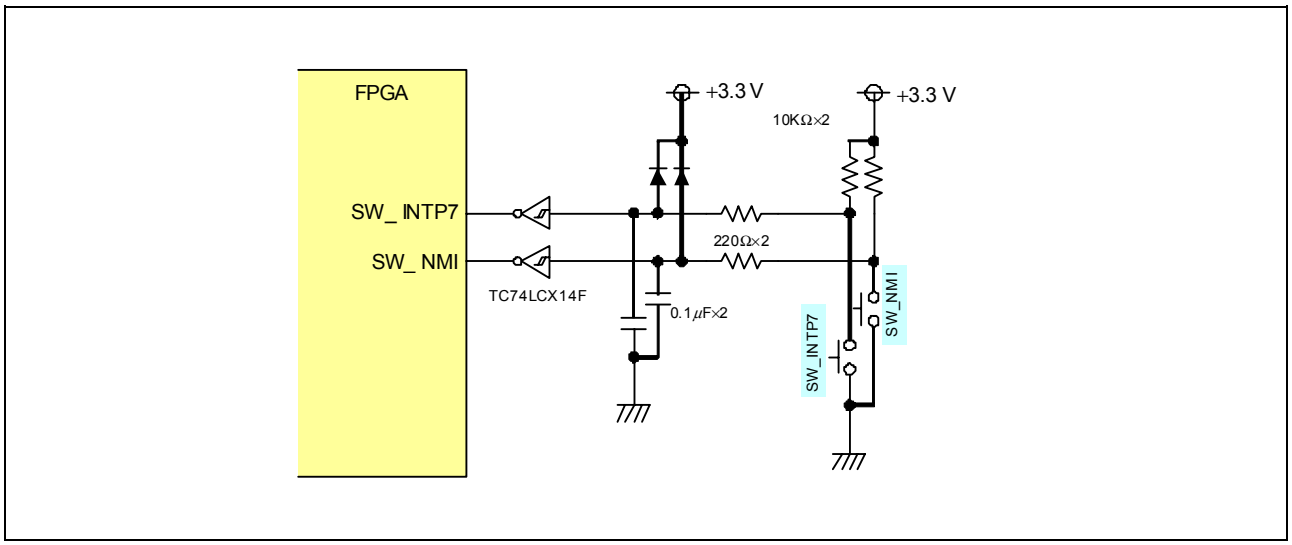
7.3 Push Switches for FPGA

Position	Figure 1-1 (Appearance) H-7

The FPGA is connected to two push switches provided with a chattering prevention circuit.

The switches are connected to NMI and INTP7 in the default FPGA circuit. All interrupt request flags are cleared in the initialization program, because if the internal initialization is earlier than the rise of the chattering prevention circuit power supply when the power is turned on, the interrupt request flag will be set during booting.

Figure 7-2. Push Switches for FPGA



7.4 DIP Switches for FPGA

Position	Figure 1-1 (Appearance) H-5

The FPGA is connected to DIP switches. The states of the DIP switches can be sampled by any signal thanks to the internal connections of the FPGA. The pins to which the DIP switches are connected are externally pulled up and low level is input when the DIP switches are turned on. The DIP switch signals are dumped via 1 kΩ resistors to prevent a large current from flowing when high level is output while the DIP switches are turned on.

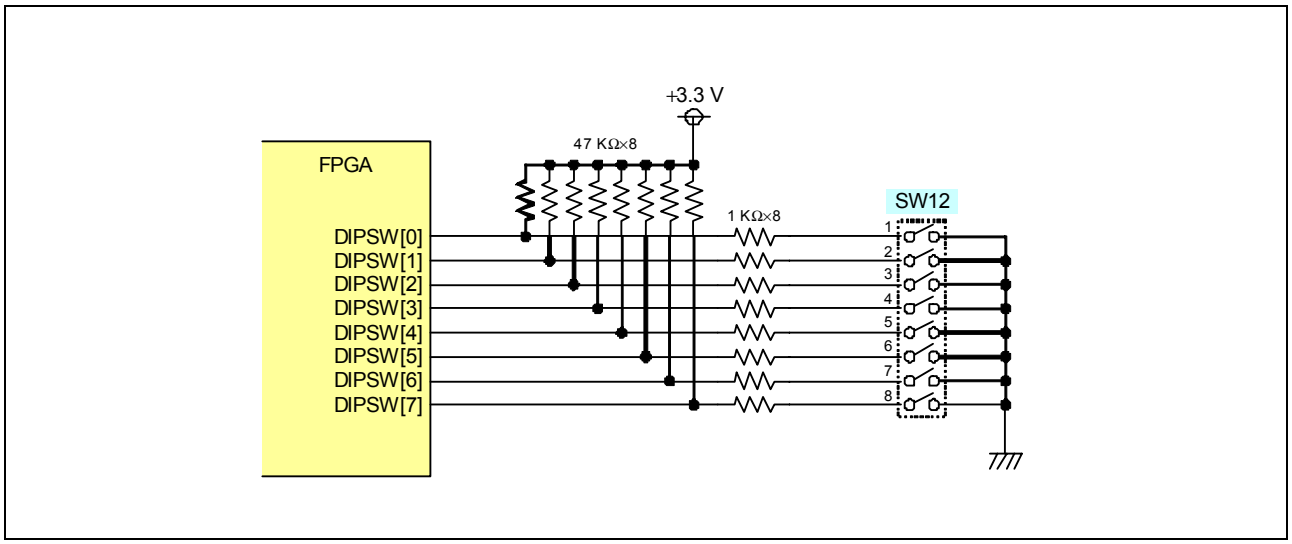
The DIP switches are connected to port 15 (P150-P157) of the PFESiP/V850EP1 in the default FPGA circuit.

If P150 to P157 are set to control mode using the PMC15 register, they function as external interrupt signals INTPZ24 to INTPZ31. A chattering absorption circuit, however, is not provided.

Table 7-2. SW12 Operation with Default Program

SW12	P15 (P150-P157 / INTPZ24-INTPZ31)
OFF	FFH
ON	00H

Figure 7-3. DIP Switches for FPGA



Caution Be sure to never set port 15 (P15) to output mode with the default FPGA program.

7.5 LEDs for FPGA

Positions | **Figure 1-1 (Appearance) E-3 to F-3**

The FPGA is connected to LEDs. The LEDs (green) can be lit by any signal thanks to the internal connections of the FPGA. The LEDs are lit when the LED connection pin output of the FPGA is “0”.

The LEDs are not lit while the FPGA is performing initialization, because the LED connection pins are pulled up.

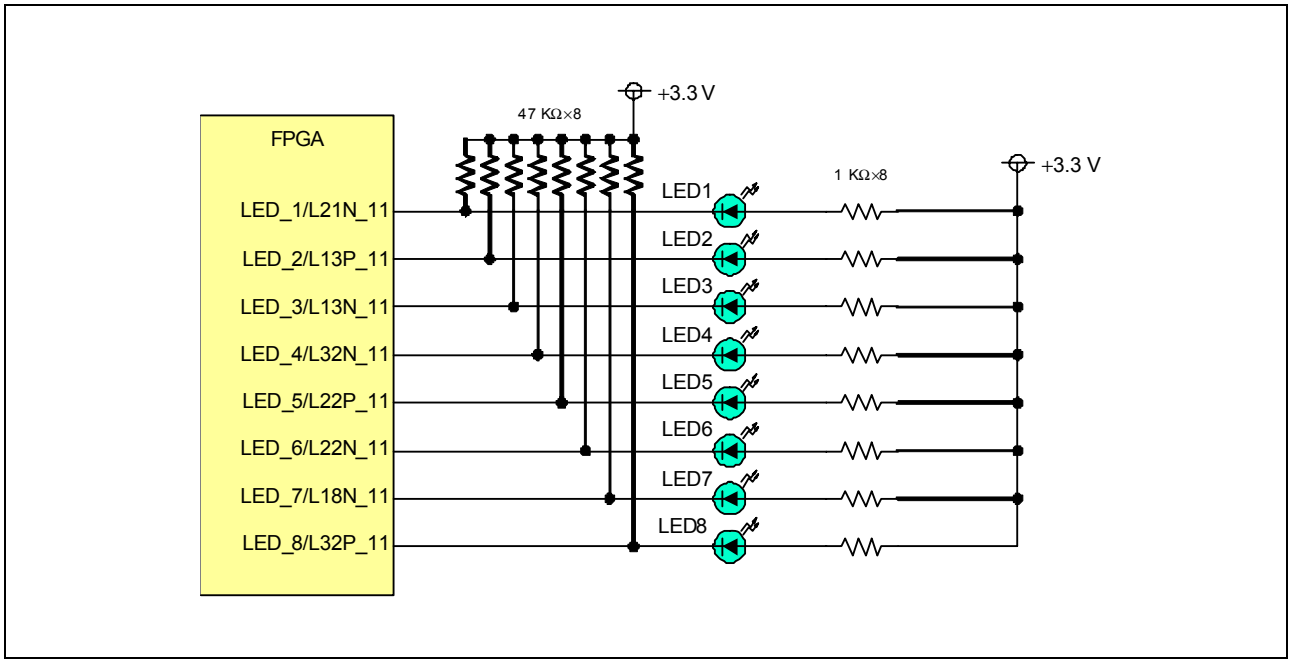
When the FPGA is in the default programming state, the LEDs are connected to port (P20 to P27) of the PFESiP/V850EP1 and all LEDs are lit when the FPGA completes the initialization.

To use these LEDs, set P20 to P27 as output ports using the PM2 register.

Table 7-3. LED Operation with Default Program

P20 to P27	FPGA LEDs (LED1 to LED8)
00H	Turns off LEDs
FFH	Turns on LEDs

Figure 7-4. LED Circuit for FPGA

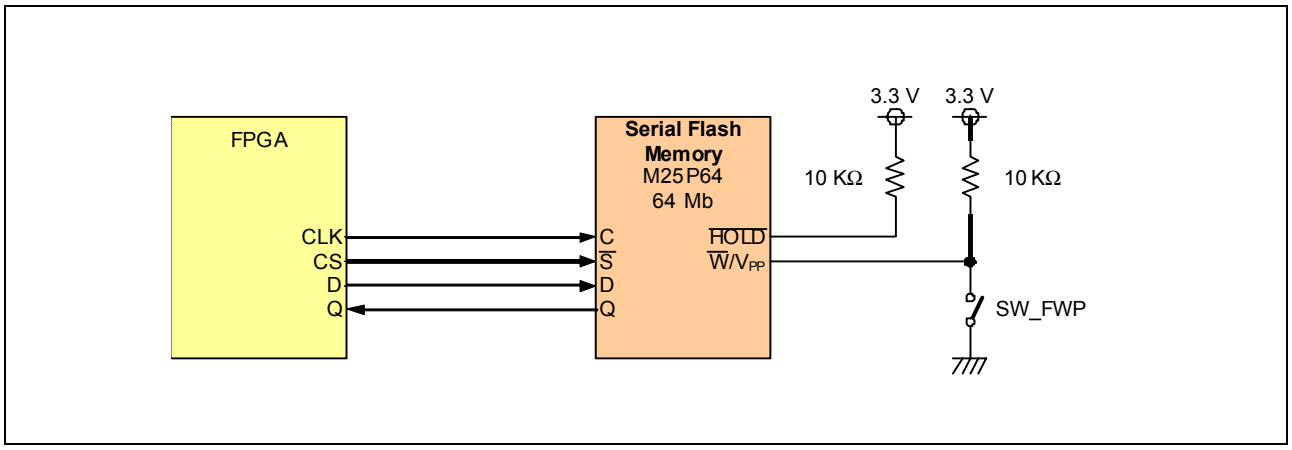


7.6 Serial ROM for FPGA

Position **Figure 1-1 (Appearance) D-6**

A 64 Mb serial ROM (M25P64) made by STMicroelectronics is connected to the FPGA for various applications using the serial ROM.

Figure 7-5. Serial ROM Connections



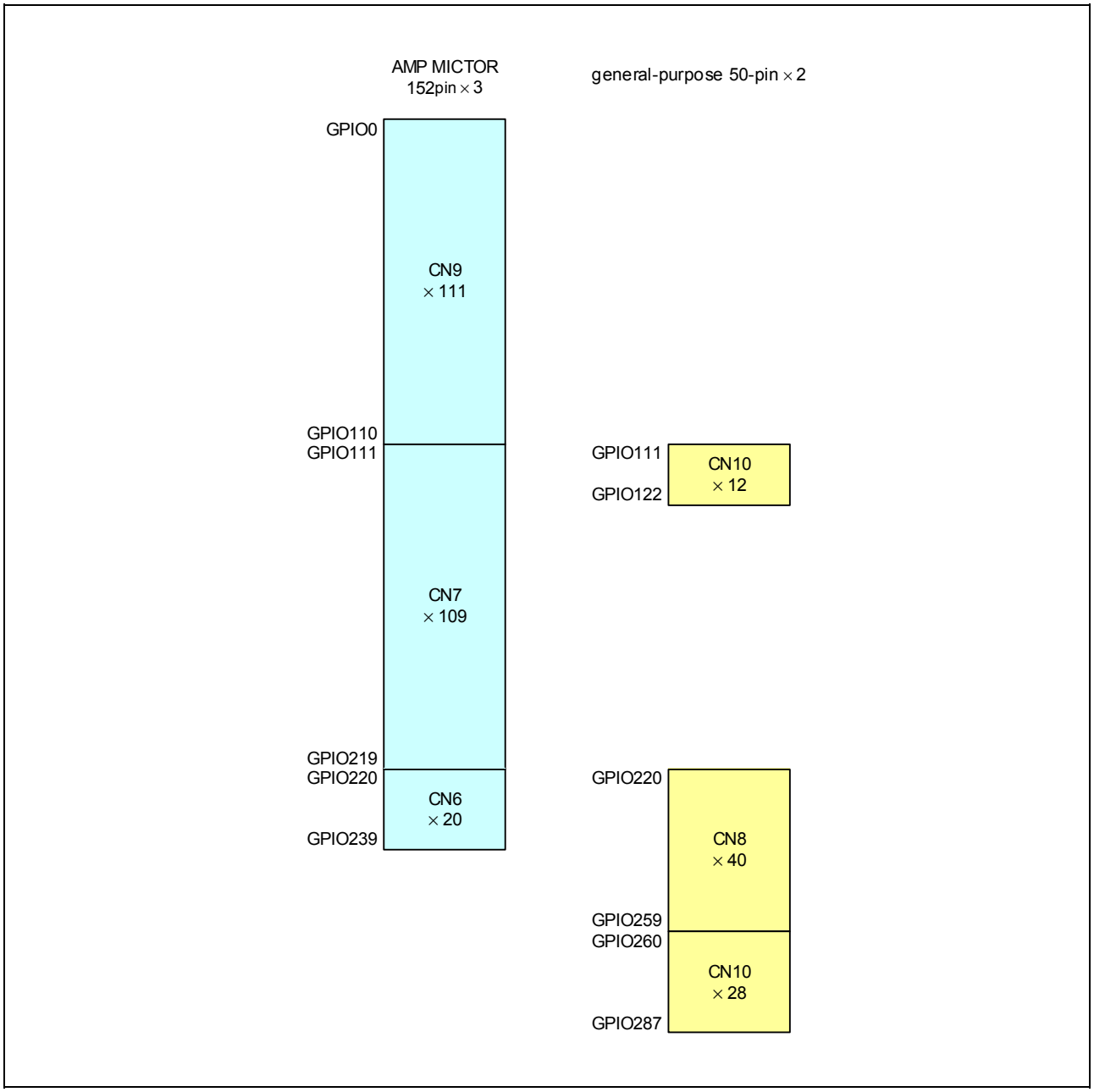
Remark Contact STMicroelectronics for how to use the M25P64.

7.7 Connection of FPGA and Expansion Connectors

The general-purpose signals (GPIOn) for external expansion from the FPGA are connected to expansion connectors (AMP MICTOR, general-purpose 50-pin connectors) CN3 and CN4.

Regardless of the selected FPGA, 228 general-purpose signals (GPIOn) can be used for connection with the expansion connectors.

Figure 7-6. Connection of FPGA Pin and Expansion Connectors



7.8 FPGA Pin Connections

The shaded signals ▭ are those used as global clocks.

(1/17)

BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
0	VCCO_0	T17									
0	VCCO_0	U14									
0	VCCO_0	V21									
0	VCCO_0	W18									
1	IO_L10N_GC_LC_1	N17		NC							
1	IO_L10P_GC_LC_1	M17		NC							
1	IO_L11N_GC_LC_1	D19		NC							
1	IO_L11P_GC_LC_1	E19		STBUSCLK							
1	IO_L12N_GC_VREF_LC_1	D17		NC							
1	IO_L12P_GC_LC_1	C17		P143	SCK1						CN12-25
1	IO_L13N_GC_LC_1	C18		NC							
1	IO_L13P_GC_LC_1	C19		BUSCLK					CN6-108		
1	IO_L14N_GC_LC_1	C15		NC							
1	IO_L14P_GC_LC_1	D16		P140	SCK0						CN12-22
1	IO_L15N_GC_LC_1	C20		NC							
1	IO_L15P_GC_LC_1	D20		VBCLKOUT							
1	IO_L16N_GC_CC_LC_1	N15		NC							
1	IO_L16P_GC_CC_LC_1	M16		NC							
1	IO_L17N_CC_LC_1	A20		NC							
1	IO_L17P_CC_LC_1	B20		NC							
1	IO_L18N_VRP_LC_1	L16		NC							
1	IO_L18P_VRN_LC_1	K16		NC							
1	IO_L19N_LC_1	L19		NC							
1	IO_L19P_LC_1	J20		NC							
1	IO_L1N_D30_LC_1	N18		NC							
1	IO_L1P_D31_LC_1	N19		NC							
1	IO_L20N_VREF_LC_1	J15		NC							
1	IO_L20P_LC_1	H15		NC							
1	IO_L21N_LC_1	H20		NC							
1	IO_L21P_LC_1	G21		NC							
1	IO_L22N_LC_1	F14		NC							
1	IO_L22P_LC_1	G15		NC							
1	IO_L23N_LC_1	F20		NC							
1	IO_L23P_LC_1	F21		NC							
1	IO_L24N_LC_1	B15		NC							
1	IO_L24P_LC_1	A15		NC							
1	IO_L2N_D28_LC_1	L14		NC							
1	IO_L2P_D29_LC_1	L15		NC							
1	IO_L3N_D26_LC_1	D21		NC							
1	IO_L3P_D27_LC_1	E21		NC							
1	IO_L4N_D24_VREF_LC_1	K14		NC							
1	IO_L4P_D25_LC_1	J14		NC							
1	IO_L5N_D22_LC_1	M20		NC							
1	IO_L5P_D23_LC_1	N20		NC							
1	IO_L6N_D20_LC_1	H13		NC							
1	IO_L6P_D21_LC_1	H14		NC							
1	IO_L7N_D18_LC_1	J21		NC							

(2/17)

BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
1	IO_L7P_D19_LC_1	H22		NC							
1	IO_L8N_D16_CC_LC_1	G13		NC							
1	IO_L8P_D17_CC_LC_1	F13		NC							
1	IO_L9N_GC_LC_1	L18		NC							
1	IO_L9P_GC_LC_1	M18		NC							
1	VCCO_1	B19									
1	VCCO_1	C16									
1	VCCO_1	E20									
1	VCCO_1	G14									
1	VCCO_1	H21									
1	VCCO_1	K15									
1	VCCO_1	M19									
1	VCCO_1	N16									
2	IO_L10N_GC_LC_2	AF15		NC							
2	IO_L10P_GC_LC_2	AD16		NC							
2	IO_L11N_GC_LC_2	AP20		NC							
2	IO_L11P_GC_LC_2	AN20		EX_CLK			CN_CLK		CN6-115		
2	IO_L12N_GC_VREF_LC_2	AC17		NC							
2	IO_L12P_GC_LC_2	AD17		NC							
2	IO_L13N_GC_LC_2	AL19		NC							
2	IO_L13P_GC_LC_2	AM20		CLK2P			OSC4				
2	IO_L14N_GC_LC_2	AB16		NC							
2	IO_L14P_GC_LC_2	AB17		NC							
2	IO_L15N_GC_LC_2	AM18		NC							
2	IO_L15P_GC_LC_2	AL18		NC							
2	IO_L16N_GC_LC_2	AM16		NC							
2	IO_L16P_GC_LC_2	AM17		NC							
2	IO_L17N_LC_2	AD20		NC							
2	IO_L17P_LC_2	AD21		NC							
2	IO_L18N_LC_2	AL15		NC							
2	IO_L18P_LC_2	AM15		NC							
2	IO_L19N_LC_2	AL20		NC							
2	IO_L19P_LC_2	AJ20		NC							
2	IO_L1N_D14_CC_LC_2	AJ21		NC							
2	IO_L1P_D15_CC_LC_2	AJ22		NC							
2	IO_L20N_VREF_LC_2	AJ14		NC							
2	IO_L20P_LC_2	AJ15		NC							
2	IO_L21N_LC_2	AH20		NC							
2	IO_L21P_LC_2	AG20		NC							
2	IO_L22N_LC_2	AH14		NC							
2	IO_L22P_LC_2	AG15		NC							
2	IO_L23N_VRP_LC_2	AE19		NC							
2	IO_L23P_VRN_LC_2	AD19		NC							
2	IO_L24N_CC_LC_2	AK16		NC							
2	IO_L24P_CC_LC_2	AL16		NC							
2	IO_L2N_D12_LC_2	AB15		NC							
2	IO_L2P_D13_LC_2	AC15		NC							
2	IO_L3N_D10_LC_2	AH22		NC							
2	IO_L3P_D11_LC_2	AG22		NC							
2	IO_L4N_D8_VREF_LC_2	AK14		NC							
2	IO_L4P_D9_LC_2	AL14		NC							
2	IO_L5N_D6_LC_2	AF20		NC							

(3/17)

BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
2	IO_L5P_D7_LC_2	AG21		NC							
2	IO_L6N_D4_LC_2	AG13		NC							
2	IO_L6P_D5_LC_2	AF14		NC							
2	IO_L7N_D2_LC_2	AF21		NC							
2	IO_L7P_D3_LC_2	AE21		NC							
2	IO_L8N_D0_LC_2	AN15		NC							
2	IO_L8P_D1_LC_2	AP15		NC							
2	IO_L9N_GC_CC_LC_2	AB18		NC							
2	IO_L9P_GC_CC_LC_2	AC19		NC							
2	VCCO_2	AM19									
2	VCCO_2	AB19									
2	VCCO_2	AC16									
2	VCCO_2	AE20									
2	VCCO_2	AG14									
2	VCCO_2	AH21									
2	VCCO_2	AK15									
2	VCCO_2	AN16									
3	IO_L1N_GC_CC_LC_3	G18			A3				CN6-37		
3	IO_L1P_GC_CC_LC_3	F18			A2				CN6-38		
3	IO_L2N_GC_VRP_LC_3	J17		P60	A20				CN6-15		
3	IO_L2P_GC_VRN_LC_3	H17		P61	A21				CN6-14		
3	IO_L3N_GC_LC_3	H18			A4				CN6-35		
3	IO_L3P_GC_LC_3	H19			A6				CN6-33		
3	IO_L4N_GC_VREF_LC_3	E17		P63	A23				CN6-12		
3	IO_L4P_GC_LC_3	E18		P67	A1				CN6-39		
3	IO_L5N_GC_LC_3	K17		P66	A0				CN6-40		
3	IO_L5P_GC_LC_3	K18			A5				CN6-34		
3	IO_L6N_GC_LC_3	F16		P65	A25				CN6-09		
3	IO_L6P_GC_LC_3	E16			VBRESTOZ				CN6-114		
3	IO_L7N_GC_LC_3	J19			A7				CN6-32		
3	IO_L7P_GC_LC_3	K19			A8				CN6-30		
3	IO_L8N_GC_LC_3	G16		P64	A24				CN6-10		
3	IO_L8P_GC_LC_3	G17		P62	A22				CN6-13		
3	VCCO_3	F17									
3	VCCO_3	J18									
4	IO_L1N_GC_LC_4	AE18	PULLUP			GPIO194			CN7-105		
4	IO_L1P_GC_LC_4	AF18	PULLUP			GPIO193			CN7-104		
4	IO_L2N_GC_LC_4	AF16	PULLUP			GPIO201			CN7-114		
4	IO_L2P_GC_LC_4	AG16	PULLUP			GPIO200			CN7-113		
4	IO_L3N_GC_LC_4	AH18	PULLUP			GPIO191			CN7-102		
4	IO_L3P_GC_LC_4	AH19	PULLUP			GPIO189			CN7-99		
4	IO_L4N_GC_VREF_LC_4	AK17	PULLUP			GPIO195			CN7-107		
4	IO_L4P_GC_LC_4	AK18	PULLUP			GPIO190			CN7-100		
4	IO_L5N_GC_LC_4	AG17	PULLUP			GPIO198			CN7-110		
4	IO_L5P_GC_LC_4	AG18	PULLUP			GPIO192			CN7-103		
4	IO_L6N_GC_LC_4	AE16	PULLUP			GPIO202			CN7-115		
4	IO_L6P_GC_LC_4	AE17	PULLUP			GPIO199			CN7-112		
4	IO_L7N_GC_VRP_LC_4	AK19	PULLUP			GPIO187			CN7-97		
4	IO_L7P_GC_VRN_LC_4	AJ19	PULLUP			GPIO188			CN7-98		
4	IO_L8N_GC_CC_LC_4	AH17	PULLUP			GPIO197			CN7-109		
4	IO_L8P_GC_CC_LC_4	AJ17	PULLUP			GPIO196			CN7-108		
4	VCCO_4	AF17									
4	VCCO_4	AJ18									

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
5	IO_L10N_5	E26		P97	D23				CN6-70		
5	IO_L10P_5	D26		P96	D22				CN6-69		
5	IO_L11N_5	E24					INTP7_SW				
5	IO_L11P_5	F24		WRZ0	BENZ0				CN6-04		
5	IO_L12N_VREF_5	E27		P105	D29				CN6-78		
5	IO_L12P_5	D27		P104	D28				CN6-77		
5	IO_L13N_5	H24		WRZ1	BENZ1				CN6-05		
5	IO_L13P_5	G23			DQM2				CN6-103		
5	IO_L14N_5	A29		P83	HLDRQZ				CN6-113		
5	IO_L14P_5	A28		P107	D31				CN6-80		
5	IO_L15N_5	C25		P90	D16				CN6-62		
5	IO_L15P_5	B25		WRZ3	BENZ3				CN6-08		
5	IO_L16N_5	K26		P101	D25				CN6-73		
5	IO_L16P_5	J25			A11				CN6-27		
5	IO_L17N_5	B22			A17				CN6-19		
5	IO_L17P_5	C22			A18				CN6-18		
5	IO_L18N_5	B30		P74	CSZ4				CN6-88		
5	IO_L18P_5	A30		P73	CSZ3				CN6-87		
5	IO_L19N_5	J24			A14				CN6-23		
5	IO_L19P_5	K24			A13				CN6-24		
5	IO_L1N_ADC7_5	A23			SDWEZ				CN6-107		
5	IO_L1P_ADC7_5	B23			SDCASZ				CN6-95		
5	IO_L20N_VREF_5	C30		P75	CSZ5				CN6-89		
5	IO_L20P_5	C29		P84	REFRQZ				CN6-97		
5	IO_L21N_5	A21			A15				CN6-22		
5	IO_L21P_5	B21			A16				CN6-20		
5	IO_L22N_5	F28		P81	IORDZ				CN6-110		
5	IO_L22P_5	E28		P80	IOWRZ				CN6-109		
5	IO_L23N_VRP_5	D22			A19				CN6-17		
5	IO_L23P_VRN_5	E22		P70	WAITZ				CN6-99		
5	IO_L24N_CC_LC_5	B31		P85	SELFREFZ				CN6-105		
5	IO_L24P_CC_LC_5	A31			D0				CN6-42		
5	IO_L25N_CC_LC_5	C28			RDZ				CN6-02		
5	IO_L25P_CC_LC_5	B28			WRSTBZ				CN6-03		
5	IO_L26N_5	D31			D1				CN6-43		
5	IO_L26P_5	D30		P76	CSZ6				CN6-90		
5	IO_L27N_5	G28		P82	HLDAKZ				CN6-112		
5	IO_L27P_5	G27		P106	D30				CN6-79		
5	IO_L28N_VREF_5	F30		P77	CSZ7				CN6-92		
5	IO_L28P_5	F29		P72	CSZ2				CN6-85		
5	IO_L29N_5	E29		P71	CSZ1				CN6-84		
5	IO_L29P_5	D29			CSZ0				CN6-83		
5	IO_L2N_ADC6_5	B26		P95	D21				CN6-68		
5	IO_L2P_ADC6_5	A26		P94	D20				CN6-67		
5	IO_L30N_5	L26			A9				CN6-29		
5	IO_L30P_5	L25			A10				CN6-28		
5	IO_L31N_5	B33			D5				CN6-48		
5	IO_L31P_5	B32			D4				CN6-47		
5	IO_L32N_5	F31			D3				CN6-45		
5	IO_L32P_5	E31			D2				CN6-44		
5	IO_L3N_ADC5_5	A25		WRZ2	BENZ2				CN6-07		
5	IO_L3P_ADC5_5	A24			DQM3				CN6-104		

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
5	IO_L4N_VREF_5	H25			A12				CN6-25		
5	IO_L4P_5	G25		P93	D19				CN6-65		
5	IO_L5N_ADC4_5	C24			SDCKE				CN6-93		
5	IO_L5P_ADC4_5	C23			SDRASZ				CN6-94		
5	IO_L6N_ADC3_5	F26		P100	D24				CN6-72		
5	IO_L6P_ADC3_5	F25		P92	D18				CN6-64		
5	IO_L7N_ADC2_5	D25		P91	D17				CN6-63		
5	IO_L7P_ADC2_5	D24			BCYSTZ				CN6-82		
5	IO_L8N_CC_ADC1_LC_5	C27		P103	D27				CN6-75		
5	IO_L8P_CC_ADC1_LC_5	B27		P102	D26				CN6-74		
5	IO_L9N_CC_LC_5	E23			DQM0				CN6-100		
5	IO_L9P_CC_LC_5	F23			DQM1				CN6-102		
5	VCCO_5	A22									
5	VCCO_5	A32									
5	VCCO_5	B29									
5	VCCO_5	C26									
5	VCCO_5	D23									
5	VCCO_5	E30									
5	VCCO_5	F27									
5	VCCO_5	G24									
5	VCCO_5	K25									
6	IO_L10N_6	B8			SREFRQZ						
6	IO_L10P_6	A8			SHLDRQZ						
6	IO_L11N_6	F11		SBENZ1	SWRZ1						
6	IO_L11P_6	E11		SBENZ0	SWRZ0						
6	IO_L12N_VREF_6	B6			STCZ1						
6	IO_L12P_6	A6			STCZ0						
6	IO_L13N_6	J11			SD10						
6	IO_L13P_6	H12			SD1						
6	IO_L14N_6	C7			SA1						
6	IO_L14P_6	B7			SA0						
6	IO_L15N_6	A9			SA8						
6	IO_L15P_6	A10			SA14						
6	IO_L16N_6	G8			SA7						
6	IO_L16P_6	F8			SA6						
6	IO_L17N_6	A13			SD2						
6	IO_L17P_6	A14			SD6						
6	IO_L18N_6	D6			SDMARQZ0						
6	IO_L18P_6	D7			SA2						
6	IO_L19N_6	E9			SA4						
6	IO_L19P_6	D9			SHLDAKZ						
6	IO_L1N_6	C12			SA19						
6	IO_L1P_6	D12			SA20						
6	IO_L20N_VREF_6	A3		P21	INTPZ17						CN12-43
6	IO_L20P_6	A4		P23	INTPZ19						CN12-45
6	IO_L21N_6	E12			SBCYSTZ						
6	IO_L21P_6	E13			SD5						
6	IO_L22N_6	B5			SCSZ1						
6	IO_L22P_6	A5			SCSZ0						
6	IO_L23N_VRP_6	E7			SA3						
6	IO_L23P_VRN_6	E8			SIORDZ						
6	IO_L24N_CC_LC_6	K9			SD12						

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
6	IO_L24P_CC_LC_6	J9			SRDZ						
6	IO_L25N_CC_LC_6	C13			SD4						
6	IO_L25P_CC_LC_6	C14			SD7						
6	IO_L26N_6	F6			SDMAAKZ0						
6	IO_L26P_6	E6			SDMARQZ1						
6	IO_L27N_6	D5			SCSZ3						
6	IO_L27P_6	C5			SCSZ2						
6	IO_L28N_VREF_6	G6			SDMAAKZ1						
6	IO_L28P_6	G7			SWAITZ		JP40				
6	IO_L29N_6	D14			SD8						
6	IO_L29P_6	E14			SD9						
6	IO_L2N_6	C10			SA16						
6	IO_L2P_6	B10			SA15						
6	IO_L30N_6	B2		P20	INTPZ16						CN12-42
6	IO_L30P_6	B3		P22	INTPZ18						CN12-44
6	IO_L31N_6	H7			SIOWRZ						
6	IO_L31P_6	H8			SD14						
6	IO_L32N_6	J7			SD15						
6	IO_L32P_6	K8			SD13						
6	IO_L3N_6	B11			SA13						
6	IO_L3P_6	A11			SA12						
6	IO_L4N_VREF_6	C8			SRESTOZ						
6	IO_L4P_6	C9			SA9						
6	IO_L5N_6	G11					PAD				
6	IO_L5P_6	G12			SD0						
6	IO_L6N_6	G10			SA11						
6	IO_L6P_6	F10			SA10						
6	IO_L7N_6	D10			SA17						
6	IO_L7P_6	D11			SWRSTBZ						
6	IO_L8N_CC_LC_6	H9			SA5						
6	IO_L8P_CC_LC_6	H10			SD11						
6	IO_L9N_CC_LC_6	B12			SA18						
6	IO_L9P_CC_LC_6	B13			SD3						
6	VCCO_6	A12									
6	VCCO_6	A2									
6	VCCO_6	B9									
6	VCCO_6	C6									
6	VCCO_6	D13									
6	VCCO_6	E10									
6	VCCO_6	F7									
6	VCCO_6	H11									
6	VCCO_6	J8									
7	IO_L10N_7	AL30	PULLUP			GPIO130			CN7-25		
7	IO_L10P_7	AM30	PULLUP			GPIO129			CN7-24		
7	IO_L11N_7	AN27	PULLUP			GPIO144			CN7-43		
7	IO_L11P_7	AP27	PULLUP			GPIO143			CN7-42		
7	IO_L12N_VREF_7	AP32	PULLUP			GPIO124			CN7-18		
7	IO_L12P_7	AP31	PULLUP			GPIO126			CN7-20		
7	IO_L13N_7	AK23	PULLUP			GPIO170			CN7-75		
7	IO_L13P_7	AK22	PULLUP			GPIO176			CN7-83		
7	IO_L14N_7	AL29	PULLUP			GPIO133			CN7-29		
7	IO_L14P_7	AL28	PULLUP			GPIO139			CN7-37		

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
7	IO_L15N_7	AP26	PULLUP			GPIO149			CN7-49		
7	IO_L15P_7	AP25	PULLUP			GPIO155			CN7-57		
7	IO_L16N_7	AH27	PULLUP			GPIO148			CN7-48		
7	IO_L16P_7	AJ27	PULLUP			GPIO147			CN7-47		
7	IO_L17N_7	AP22	PULLUP			GPIO173			CN7-79		
7	IO_L17P_7	AP21	PULLUP			GPIO177			CN7-84		
7	IO_L18N_7	AN29	PULLUP			GPIO132			CN7-28		
7	IO_L18P_7	AP29	PULLUP			GPIO131			CN7-27		
7	IO_L19N_7	AJ24	PULLUP			GPIO165			CN7-69		
7	IO_L19P_7	AK24	PULLUP			GPIO164			CN7-68		
7	IO_L1N_7	AJ29	PULLUP			GPIO135			CN7-32		
7	IO_L1P_7	AK29	PULLUP			GPIO134			CN7-30		
7	IO_L20N_VREF_7	AK28	PULLUP			GPIO140			CN7-38		
7	IO_L20P_7	AK27	PULLUP			GPIO146			CN7-45		
7	IO_L21N_7	AF24	PULLUP			GPIO186			CN7-95		
7	IO_L21P_7	AG23	PULLUP			GPIO172			CN7-78		
7	IO_L22N_7	AG26	PULLUP			GPIO153			CN7-54		
7	IO_L22P_7	AG25	PULLUP			GPIO185			CN7-94		
7	IO_L23N_VRP_7	AH24	PULLUP			GPIO166			CN7-70		
7	IO_L23P_VRN_7	AH23	PULLUP			GPIO171			CN7-77		
7	IO_L24N_CC_LC_7	AM28	PULLUP			GPIO138			CN7-35		
7	IO_L24P_CC_LC_7	AN28	PULLUP			GPIO137			CN7-34		
7	IO_L25N_CC_SM7_LC_7	AL25	PULLUP			GPIO158			CN7-60		
7	IO_L25P_CC_SM7_LC_7	AL24	PULLUP			GPIO163			CN7-67		
7	IO_L26N_SM6_7	AK26	PULLUP			GPIO152			CN7-53		
7	IO_L26P_SM6_7	AL26	PULLUP			GPIO151			CN7-52		
7	IO_L27N_SM5_7	AN23	PULLUP			GPIO167			CN7-72		
7	IO_L27P_SM5_7	AN22	PULLUP			GPIO174			CN7-80		
7	IO_L28N_VREF_7	AH25	PULLUP			GPIO160			CN7-63		
7	IO_L28P_7	AJ25	PULLUP			GPIO159			CN7-62		
7	IO_L29N_SM4_7	AN24	PULLUP			GPIO162			CN7-65		
7	IO_L29P_SM4_7	AP24	PULLUP			GPIO161			CN7-64		
7	IO_L2N_7	AE27	PULLUP			GPIO183			CN7-92		
7	IO_L2P_7	AF28	PULLUP			GPIO181			CN7-89		
7	IO_L30N_SM3_7	AM27	PULLUP			GPIO145			CN7-44		
7	IO_L30P_SM3_7	AM26	PULLUP			GPIO150			CN7-50		
7	IO_L31N_SM2_7	AM23	PULLUP			GPIO168			CN7-73		
7	IO_L31P_SM2_7	AL23	PULLUP			GPIO169			CN7-74		
7	IO_L32N_SM1_7	AM25	PULLUP			GPIO157			CN7-59		
7	IO_L32P_SM1_7	AN25	PULLUP			GPIO156			CN7-58		
7	IO_L3N_7	AE26	PULLUP			GPIO184			CN7-93		
7	IO_L3P_7	AF26	PULLUP			GPIO154			CN7-55		
7	IO_L4N_VREF_7	AN33	PULLUP			GPIO123			CN7-17		
7	IO_L4P_7	AN32	PULLUP			GPIO125			CN7-19		
7	IO_L5N_7	AL21	PULLUP			GPIO179			CN7-87		
7	IO_L5P_7	AK21	PULLUP			GPIO180			CN7-88		
7	IO_L6N_7	AH29	PULLUP			GPIO136			CN7-33		
7	IO_L6P_7	AH28	PULLUP			GPIO141			CN7-39		
7	IO_L7N_7	AN30	PULLUP			GPIO128			CN7-23		
7	IO_L7P_7	AP30	PULLUP			GPIO127			CN7-22		
7	IO_L8N_CC_LC_7	AG28	PULLUP			GPIO142			CN7-40		
7	IO_L8P_CC_LC_7	AG27	PULLUP			GPIO182			CN7-90		

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
7	IO_L9N_CC_LC_7	AM22	PULLUP			GPIO175			CN7-82		
7	IO_L9P_CC_LC_7	AM21	PULLUP			GPIO178			CN7-85		
7	VCCO_7	AF27									
7	VCCO_7	AG24									
7	VCCO_7	AJ28									
7	VCCO_7	AK25									
7	VCCO_7	AL22									
7	VCCO_7	AM29									
7	VCCO_7	AN26									
7	VCCO_7	AP23									
7	VCCO_7	AP33									
8	IO_L10N_8	AK6	PULLUP			GPIO77			CN9-98		
8	IO_L10P_8	AL6	PULLUP			GPIO78			CN9-99		
8	IO_L11N_8	AK8	PULLUP			GPIO88			CN9-112		
8	IO_L11P_8	AL8	PULLUP			GPIO89			CN9-113		
8	IO_L12N_VREF_8	AH7	PULLUP			GPIO81			CN9-103		
8	IO_L12P_8	AH8	PULLUP			GPIO87			CN9-110		
8	IO_L13N_8	AN13	PULLUP			GPIO211			CN7-127		
8	IO_L13P_8	AM13	PULLUP			GPIO212			CN7-128		
8	IO_L14N_8	AM5	PULLUP			GPIO73			CN9-93		
8	IO_L14P_8	AM6	PULLUP			GPIO79			CN9-100		
8	IO_L15N_8	AJ9	PULLUP			GPIO93			CN9-118		
8	IO_L15P_8	AJ10	PULLUP			GPIO99			CN9-125		
8	IO_L16N_8	AN5	PULLUP			GPIO74			CN9-94		
8	IO_L16P_8	AP5	PULLUP			GPIO75			CN9-95		
8	IO_L17N_8	AG11	PULLUP			GPIO104			CN9-132		
8	IO_L17P_8	AH12	PULLUP			GPIO110			CN9-139		
8	IO_L18N_8	AM7	PULLUP			GPIO84			CN9-107		
8	IO_L18P_8	AN7	PULLUP			GPIO85			CN9-108		
8	IO_L19N_8	AM10	PULLUP			GPIO101			CN9-128		
8	IO_L19P_8	AN10	PULLUP			GPIO102			CN9-129		
8	IO_L1N_8	AL4	PULLUP			GPIO68			CN9-87		
8	IO_L1P_8	AL5	PULLUP			GPIO72			CN9-92		
8	IO_L20N_VREF_8	AE9	PULLUP			GPIO92			CN9-117		
8	IO_L20P_8	AF10	PULLUP			GPIO205			CN7-119		
8	IO_L21N_8	AK12	PULLUP			GPIO218			CN7-135		
8	IO_L21P_8	AJ12	PULLUP			GPIO219			CN7-137		
8	IO_L22N_8	AM8	PULLUP			GPIO90			CN9-114		
8	IO_L22P_8	AN8	PULLUP			GPIO91			CN9-115		
8	IO_L23N_VRP_8	AK11	PULLUP			GPIO106			CN9-134		
8	IO_L23P_VRN_8	AJ11	PULLUP			GPIO105			CN9-133		
8	IO_L24N_CC_LC_8	AP6	PULLUP			GPIO80			CN9-102		
8	IO_L24P_CC_LC_8	AP7	PULLUP			GPIO86			CN9-109		
8	IO_L25N_CC_LC_8	AL10	PULLUP			GPIO100			CN9-127		
8	IO_L25P_CC_LC_8	AL11	PULLUP			GPIO107			CN9-135		
8	IO_L26N_8	AF11	PULLUP			GPIO208			CN7-123		
8	IO_L26P_8	AE11	PULLUP			GPIO207			CN7-122		
8	IO_L27N_8	AM11	PULLUP			GPIO108			CN9-137		
8	IO_L27P_8	AM12	PULLUP			GPIO217			CN7-134		
8	IO_L28N_VREF_8	AK9	PULLUP			GPIO94			CN9-119		
8	IO_L28P_8	AL9	PULLUP			GPIO95			CN9-120		
8	IO_L29N_8	AP10	PULLUP			GPIO103			CN9-130		

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESiP/V850EP1 Port Pins
8	IO_L29P_8	AP11	PULLUP			GPIO109			CN9-138		
8	IO_L2N_8	AJ4	PULLUP			GPIO66			CN9-84		
8	IO_L2P_8	AK4	PULLUP			GPIO67			CN9-85		
8	IO_L30N_8	AG10	PULLUP			GPIO206			CN7-120		
8	IO_L30P_8	AH10	PULLUP			GPIO98			CN9-124		
8	IO_L31N_8	AP12	PULLUP			GPIO215			CN7-132		
8	IO_L31P_8	AN12	PULLUP			GPIO216			CN7-133		
8	IO_L32N_8	AN9	PULLUP			GPIO96			CN9-122		
8	IO_L32P_8	AP9	PULLUP			GPIO97			CN9-123		
8	IO_L3N_8	AN4	PULLUP			GPIO69			CN9-88		
8	IO_L3P_8	AP4	PULLUP			GPIO70			CN9-89		
8	IO_L4N_VREF_8	AD9	PULLUP			GPIO203			CN7-117		
8	IO_L4P_8	AD10	PULLUP			GPIO204			CN7-118		
8	IO_L5N_8	AP14	PULLUP			GPIO209			CN7-124		
8	IO_L5P_8	AN14	PULLUP			GPIO210			CN7-125		
8	IO_L6N_8	AJ5	PULLUP			GPIO71			CN9-90		
8	IO_L6P_8	AJ6	PULLUP			GPIO76			CN9-97		
8	IO_L7N_8	AJ7	PULLUP			GPIO82			CN9-104		
8	IO_L7P_8	AK7	PULLUP			GPIO83			CN9-105		
8	IO_L8N_CC_LC_8	AN2	PULLUP			GPIO64			CN9-82		
8	IO_L8P_CC_LC_8	AN3	PULLUP			GPIO65			CN9-83		
8	IO_L9N_CC_LC_8	AL13	PULLUP			GPIO213			CN7-129		
8	IO_L9P_CC_LC_8	AK13	PULLUP			GPIO214			CN7-130		
8	VCCO_8	AE10									
8	VCCO_8	AH11									
8	VCCO_8	AJ8									
8	VCCO_8	AK5									
8	VCCO_8	AL12									
8	VCCO_8	AM9									
8	VCCO_8	AN6									
8	VCCO_8	AP13									
8	VCCO_8	AP3									
9	IO_L10N_9	J30		P151	INTPZ25						CN11-18
9	IO_L10P_9	J29		P150	INTPZ24						CN11-17
9	IO_L11N_9	E33			D12				CN6-57		
9	IO_L11P_9	E32			D11				CN6-55		
9	IO_L12N_VREF_9	P26	PULLUP			GPIO249				CN8-38	
9	IO_L12P_9	N25	PULLUP			GPIO242				CN8-29	
9	IO_L13N_9	R21	PULLUP			GPIO252				CN8-42	
9	IO_L13P_9	P22	PULLUP			GPIO247				CN8-35	
9	IO_L14N_9	F34			D15				CN6-60		
9	IO_L14P_9	F33			D14				CN6-59		
9	IO_L15N_9	K29	PULLUP			GPIO222			CN6-119	CN8-4	
9	IO_L15P_9	K28	PULLUP			GPIO221			CN6-118	CN8-3	
9	IO_L16N_9	G33		P120	TCZ0						CN11-7
9	IO_L16P_9	G32		P130	DMARQZ0						CN11-2
9	IO_L17N_9	R19	PULLUP			GPIO251				CN8-40	
9	IO_L17P_9	P20	PULLUP			GPIO246				CN8-34	
9	IO_L18N_9	L29	PULLUP			GPIO229			CN6-128	CN8-13	
9	IO_L18P_9	L28	PULLUP			GPIO228			CN6-127	CN8-12	
9	IO_L19N_9	R24	PULLUP			GPIO255				CN8-45	

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Parts Name 1	Parts Name 2	MICTOR	50 General -Purpose pin	50 PFESIP/V850EP1 Port Pins
9	IO_L19P_9	P24	PULLUP			GPIO248				CN8-37	
9	IO_L1N_9	H28		P121	TCZ1						CN11-8
9	IO_L1P_9	H27		P133	DMARQZ3						CN11-5
9	IO_L20N_VREF_9	J32		P153	INTPZ27						CN11-20
9	IO_L20P_9	H32		P124	DMAAKZ0						CN11-12
9	IO_L21N_9	M28	PULLUP			GPIO235			CN6-135	CN8-20	
9	IO_L21P_9	M27	PULLUP			GPIO234			CN6-134	CN8-19	
9	IO_L22N_9	H34		P126	DMAAKZ2						CN11-14
9	IO_L22P_9	H33		P125	DMAAKZ1						CN11-13
9	IO_L23N_VRP_9	K31	PULLUP			GPIO223			CN6-120	CN8-5	
9	IO_L23P_VRN_9	J31		P152	INTPZ26						CN11-19
9	IO_L24N_CC_LC_9	L31	PULLUP			GPIO231			CN6-130	CN8-15	
9	IO_L24P_CC_LC_9	L30	PULLUP			GPIO230			CN6-129	CN8-14	
9	IO_L25N_CC_LC_9	R23	PULLUP			GPIO254				CN8-44	
9	IO_L25P_CC_LC_9	R22	PULLUP			GPIO253				CN8-43	
9	IO_L26N_9	K33	PULLUP			GPIO225			CN6-123	CN8-8	
9	IO_L26P_9	K32	PULLUP			GPIO224			CN6-122	CN8-7	
9	IO_L27N_9	P27	PULLUP			GPIO250				CN8-39	
9	IO_L27P_9	N27	PULLUP			GPIO243				CN8-30	
9	IO_L28N_VREF_9	M31	PULLUP			GPIO237			CN6-138	CN8-23	
9	IO_L28P_9	M30	PULLUP			GPIO236			CN6-137	CN8-22	
9	IO_L29N_9	K34	PULLUP			GPIO226			CN6-124	CN8-9	
9	IO_L29P_9	J34	PULLUP			GPIO220			CN6-117	CN8-2	
9	IO_L2N_9	D32			D9				CN6-53		
9	IO_L2P_9	C32			D6				CN6-49		
9	IO_L30N_9	N30	PULLUP			GPIO245				CN8-33	
9	IO_L30P_9	N29	PULLUP			GPIO244				CN8-32	
9	IO_L31N_9	L34	PULLUP			GPIO233			CN6-133	CN8-18	
9	IO_L31P_9	L33	PULLUP			GPIO232			CN6-132	CN8-17	
9	IO_L32N_9	M33	PULLUP			GPIO239			CN6-140	CN8-25	
9	IO_L32P_9	M32	PULLUP			GPIO238			CN6-139	CN8-24	
9	IO_L3N_9	K27	PULLUP			GPIO227			CN6-125	CN8-10	
9	IO_L3P_9	J27		P127	DMAAKZ3						CN11-15
9	IO_L4N_VREF_9	M26	PULLUP			GPIO256				CN8-47	
9	IO_L4P_9	M25	PULLUP			GPIO257				CN8-48	
9	IO_L5N_9	N23	PULLUP			GPIO241				CN8-28	
9	IO_L5P_9	N22	PULLUP			GPIO240				CN8-27	
9	IO_L6N_9	H30		P123	TCZ3						CN11-10
9	IO_L6P_9	H29		P122	TCZ2						CN11-9
9	IO_L7N_9	C34			D8				CN6-52		
9	IO_L7P_9	C33			D7				CN6-50		
9	IO_L8N_CC_LC_9	E34			D13				CN6-58		
9	IO_L8P_CC_LC_9	D34			D10				CN6-54		
9	IO_L9N_CC_LC_9	G31		P131	DMARQZ1						CN11-3
9	IO_L9P_CC_LC_9	G30		P132	DMARQZ2						CN11-4
9	VCCO_9	D33									
9	VCCO_9	G34									
9	VCCO_9	H31									
9	VCCO_9	J28									
9	VCCO_9	L32									
9	VCCO_9	M29									
9	VCCO_9	N26									

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50PFESIP/V850EP1 Port Pins
9	VCCO_9	P23									
9	VCCO_9	R20									
10	IO_L10N_10	J5		P03	INTPZ3						CN12-15
10	IO_L10P_10	J6		P04	INTPZ4						CN12-17
10	IO_L11N_10	H4		P144	SI1						CN12-27
10	IO_L11P_10	H5		P145	SO1						CN12-28
10	IO_L12N_VREF_10	N9		P154	INTPZ28						CN15-1
10	IO_L12P_10	N10		P116	ADTRG						CN11-29
10	IO_L13N_10	P11		P156	INTPZ30						CN15-3
10	IO_L13P_10	P12		P157	INTPZ31						CN15-4
10	IO_L14N_10	G2		P17	INTPZ15						CN11-39
10	IO_L14P_10	G3					NMI_SW				
10	IO_L15N_10	M8		P57	ETCUD1						CN12-10
10	IO_L15P_10	L8		P43	TI3						CN11-44
10	IO_L16N_10	L6		P42	TI2						CN11-43
10	IO_L16P_10	K6		P51	TO1						CN12-3
10	IO_L17N_10	G1		P16	INTPZ14						CN11-38
10	IO_L17P_10	F1		P36	RXD3						CN12-39
10	IO_L18N_10	K4		P50	TO0						CN12-2
10	IO_L18P_10	J4		P02	INTPZ2						CN12-14
10	IO_L19N_10	H2		P142	SO0						CN12-24
10	IO_L19P_10	H3									
10	IO_L1N_10	C3		P25	INTPZ21						CN12-48
10	IO_L1P_10	C4		P26	INTPZ22						CN12-49
10	IO_L20N_VREF_10	P9		P11	INTPZ9						CN11-32
10	IO_L20P_10	P10		P155	INTPZ29						CN15-2
10	IO_L21N_10	N7		P113	ETO1						CN11-25
10	IO_L21P_10	M7		P56	ETCUD0						CN12-9
10	IO_L22N_10	L4		P40	TI0						CN11-40
10	IO_L22P_10	L5		P41	TI1						CN11-42
10	IO_L23N_VRP_10	J1		P00	INTPZ0						CN12-12
10	IO_L23P_VRN_10	J2		P01	INTPZ1						CN12-13
10	IO_L24N_CC_LC_10	T11		P115	DBINT						CN11-28
10	IO_L24P_CC_LC_10	R11		P12	INTPZ10						CN11-33
10	IO_L25N_CC_LC_10	L3		P53	TO3						CN12-5
10	IO_L25P_CC_LC_10	K3		P07	INTPZ7						CN12-20
10	IO_L26N_10	K1		P05	INTPZ5						CN12-18
10	IO_L26P_10	K2		P06	INTPZ6						CN12-19
10	IO_L27N_10	M5		P54	ETIUD0						CN12-7
10	IO_L27P_10	M6		P55	ETIUD1						CN12-8
10	IO_L28N_VREF_10	M2		P47	TCLR3						CN11-49,-50
10	IO_L28P_10	M3					PAD input				
10	IO_L29N_10	M1		P45	TCLR1						CN11-47
10	IO_L29P_10	L1		P52	TO2						CN12-4
10	IO_L2N_10	G5		P141	SI0						CN12-23
10	IO_L2P_10	F5		P15	INTPZ13						CN11-37
10	IO_L30N_10	P5		P146	PWMO0						CN12-29
10	IO_L30P_10	N5		P112	ETO0						CN11-24
10	IO_L31N_10	P6		P147	PWMO1						CN12-30
10	IO_L31P_10	P7		P10	INTPZ8						CN11-30
10	IO_L32N_10	R9		P13	INTPZ11						CN11-34
10	IO_L32P_10	T10		P114	EVTTRG						CN11-27

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50PFESIP/V850EP1 Port Pins
10	IO_L3N_10	E4		P35	TXD2						CN12-38
10	IO_L3P_10	D4		P31	TXD0						CN12-33
10	IO_L4N_VREF_10	L9		P44	TCLR0						CN11-45
10	IO_L4P_10	M10		P46	TCLR2						CN11-48
10	IO_L5N_10	N12		P110	ETCLR0						CN11-22
10	IO_L5P_10	N13		P111	ETCLR1						CN11-23
10	IO_L6N_10	F3		P37	TXD3						CN12-40
10	IO_L6P_10	F4		P14	INTPZ12						CN11-35
10	IO_L7N_10	D2		P30	RXD0						CN12-32
10	IO_L7P_10	C2		P24	INTPZ20						CN12-47
10	IO_L8N_CC_LC_10	E1		P32	RXD1						CN12-34
10	IO_L8P_CC_LC_10	D1		P27	INTPZ23						CN12-50
10	IO_L9N_CC_LC_10	E2		P33	TXD1						CN12-35
10	IO_L9P_CC_LC_10	E3		P34	RXD2						CN12-37
10	VCCO_10	D3									
10	VCCO_10	G4									
10	VCCO_10	H1									
10	VCCO_10	K5									
10	VCCO_10	L2									
10	VCCO_10	M9									
10	VCCO_10	N6									
10	VCCO_10	P13									
10	VCCO_10	R10									
11	IO_L10N_11	AD32					SROM_CLK				
11	IO_L10P_11	AE32					FRESET_OUT				
11	IO_L11N_11	AB28	PULLUP			GPIO276				CN10-22	
11	IO_L11P_11	AC28	PULLUP			GPIO278				CN10-24	
11	IO_L12N_VREF_11	AD31	PULLUP			GPIO287				CN10-35	
11	IO_L12P_11	AD30	PULLUP			GPIO286				CN10-34	
11	IO_L13N_11	AG33					LED_3	TP3			
11	IO_L13P_11	AG32					LED_2	TP2			
11	IO_L14N_11	AF34					DIP_7				
11	IO_L14P_11	AF33					DIP_6				
11	IO_L15N_11	AD29	PULLUP			GPIO285				CN10-33	
11	IO_L15P_11	AE29					SROM_S				
11	IO_L16N_11	AE31					SROM_Q				
11	IO_L16P_11	AF31					DIP_5				
11	IO_L17N_11	AA24	PULLUP			GPIO266				CN10-9	
11	IO_L17P_11	AA23	PULLUP			GPIO265				CN10-8	
11	IO_L18N_11	AH34					LED_7	TP7			
11	IO_L18P_11	AJ34	PULLUP			GPIO121			CN7-14	CN10-49	
11	IO_L19N_11	AC27	PULLUP			GPIO263				CN10-5	
11	IO_L19P_11	AD27	PULLUP			GPIO284				CN10-32	
11	IO_L1N_11	AA29	PULLUP			GPIO270				CN10-14	
11	IO_L1P_11	AA28	PULLUP			GPIO269				CN10-13	
11	IO_L20N_VREF_11	AB26	PULLUP			GPIO275				CN10-20	
11	IO_L20P_11	AB25	PULLUP			GPIO274				CN10-19	
11	IO_L21N_11	AG31					LED_1	TP1			
11	IO_L21P_11	AG30					DIP_8				
11	IO_L22N_11	AH33					LED_6	TP6			
11	IO_L22P_11	AH32					LED_5	TP5			
11	IO_L23N_VRP_11	AD26	PULLUP			GPIO264				CN10-7	
11	IO_L23P_VRN_11	AC25	PULLUP			GPIO262				CN10-4	

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESIP/V850EP1 Port Pins
11	IO_L24N_CC_LC_11	AF30					DIP_4				
11	IO_L24P_CC_LC_11	AF29					DIP_3				
11	IO_L25N_CC_LC_11	AK32	PULLUP			GPIO119			CN7-12	CN10-47	
11	IO_L25P_CC_LC_11	AK31	PULLUP			GPIO120			CN7-13	CN10-48	
11	IO_L26N_11	AK34	PULLUP			GPIO117			CN7-09	CN10-44	
11	IO_L26P_11	AK33	PULLUP			GPIO118			CN7-10	CN10-45	
11	IO_L27N_11	AM33	PULLUP			GPIO111			CN7-02	CN10-37	
11	IO_L27P_11	AM32	PULLUP			GPIO112			CN7-03	CN10-38	
11	IO_L28N_VREF_11	AJ32	PULLUP			GPIO122			CN7-15	CN10-50	
11	IO_L28P_11	AJ31					PAD				
11	IO_L29N_11	AB23	PULLUP			GPIO273				CN10-18	
11	IO_L29P_11	AB22	PULLUP			GPIO272				CN10-17	
11	IO_L2N_11	Y24	PULLUP			GPIO260				CN10-2	
11	IO_L2P_11	W24	PULLUP			GPIO258				CN8-49	
11	IO_L30N_11	AL34	PULLUP			GPIO114			CN7-05	CN10-40	
11	IO_L30P_11	AL33	PULLUP			GPIO115			CN7-07	CN10-42	
11	IO_L31N_11	AL31	PULLUP			GPIO116			CN7-08	CN10-43	
11	IO_L31P_11	AM31	PULLUP			GPIO113			CN7-04	CN10-39	
11	IO_L32N_11	AH30					LED_4	TP4			
11	IO_L32P_11	AJ30					LED_8	TP8			
11	IO_L3N_11	AA30	PULLUP			GPIO271				CN10-15	
11	IO_L3P_11	AB30	PULLUP			GPIO277				CN10-23	
11	IO_L4N_VREF_11	Y26	PULLUP			GPIO261				CN10-3	
11	IO_L4P_11	W25	PULLUP			GPIO259				CN8-50	
11	IO_L5N_11	AE34					DIP_2				
11	IO_L5P_11	AE33					DIP_1				
11	IO_L6N_11	AC33	PULLUP			GPIO282				CN10-29	
11	IO_L6P_11	AC32	PULLUP			GPIO281				CN10-28	
11	IO_L7N_11	AC30	PULLUP			GPIO280				CN10-27	
11	IO_L7P_11	AC29	PULLUP			GPIO279				CN10-25	
11	IO_L8N_CC_LC_11	AC34	PULLUP			GPIO283				CN10-30	
11	IO_L8P_CC_LC_11	AD34					SROM_D				
11	IO_L9N_CC_LC_11	AA26	PULLUP			GPIO268				CN10-12	
11	IO_L9P_CC_LC_11	AA25	PULLUP			GPIO267				CN10-10	
11	VCCO_11	AA22									
11	VCCO_11	AB29									
11	VCCO_11	AC26									
11	VCCO_11	AD33									
11	VCCO_11	AE30									
11	VCCO_11	AG34									
11	VCCO_11	AH31									
11	VCCO_11	AL32									
11	VCCO_11	Y25									
12	IO_L10N_12	AE2	PULLUP			GPIO29			CN9-38		
12	IO_L10P_12	AE3	PULLUP			GPIO30			CN9-39		
12	IO_L11N_12	AD5	PULLUP			GPIO25			CN9-33		
12	IO_L11P_12	AD6	PULLUP			GPIO26			CN9-34		
12	IO_L12N_VREF_12	AB8	PULLUP			GPIO15			CN9-20		
12	IO_L12P_12	AC7	PULLUP			GPIO20			CN9-27		
12	IO_L13N_12	AA15	PULLUP			GPIO7			CN9-10		
12	IO_L13P_12	Y16	PULLUP			GPIO4			CN9-7		
12	IO_L14N_12	AD4	PULLUP			GPIO24			CN9-32		

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESIP/V850EP1 Port Pins
12	IO_L14P_12	AE4	PULLUP			GPIO31			CN9-40		
12	IO_L15N_12	AH2	PULLUP			GPIO46			CN9-59		
12	IO_L15P_12	AH3	PULLUP			GPIO47			CN9-60		
12	IO_L16N_12	AG1	PULLUP			GPIO40			CN9-52		
12	IO_L16P_12	AG2	PULLUP			GPIO41			CN9-53		
12	IO_L17N_12	AC8	PULLUP			GPIO21			CN9-28		
12	IO_L17P_12	AC9	PULLUP			GPIO63			CN9-80		
12	IO_L18N_12	AF3	PULLUP			GPIO35			CN9-45		
12	IO_L18P_12	AG3	PULLUP			GPIO42			CN9-54		
12	IO_L19N_12	AE6	PULLUP			GPIO32			CN9-42		
12	IO_L19P_12	AF6	PULLUP			GPIO38			CN9-49		
12	IO_L1N_12	AB5	PULLUP			GPIO13			CN9-18		
12	IO_L1P_12	AB6	PULLUP			GPIO14			CN9-19		
12	IO_L20N_VREF_12	AF4	PULLUP			GPIO36			CN9-47		
12	IO_L20P_12	AF5	PULLUP			GPIO37			CN9-48		
12	IO_L21N_12	AK1	PULLUP			GPIO52			CN9-67		
12	IO_L21P_12	AL1	PULLUP			GPIO55			CN9-70		
12	IO_L22N_12	AJ1	PULLUP			GPIO50			CN9-64		
12	IO_L22P_12	AJ2	PULLUP			GPIO51			CN9-65		
12	IO_L23N_VRP_12	AG5	PULLUP			GPIO43			CN9-55		
12	IO_L23P_VRN_12	AG6	PULLUP			GPIO44			CN9-57		
12	IO_L24N_CC_LC_12	AD7	PULLUP			GPIO27			CN9-35		
12	IO_L24P_CC_LC_12	AE7	PULLUP			GPIO33			CN9-43		
12	IO_L25N_CC_LC_12	AB10	PULLUP			GPIO10			CN9-14		
12	IO_L25P_CC_LC_12	AC10	PULLUP			GPIO62			CN9-79		
12	IO_L26N_12	AK2	PULLUP			GPIO53			CN9-68		
12	IO_L26P_12	AK3	PULLUP			GPIO54			CN9-69		
12	IO_L27N_12	AE8	PULLUP			GPIO61			CN9-78		
12	IO_L27P_12	AF8	PULLUP			GPIO39			CN9-50		
12	IO_L28N_VREF_12	AH4	PULLUP			GPIO48			CN9-62		
12	IO_L28P_12	AH5	PULLUP			GPIO49			CN9-63		
12	IO_L29N_12	AB12	PULLUP			GPIO11			CN9-15		
12	IO_L29P_12	AB13	PULLUP			GPIO12			CN9-17		
12	IO_L2N_12	AC2	PULLUP			GPIO16			CN9-22		
12	IO_L2P_12	AC3	PULLUP			GPIO17			CN9-23		
12	IO_L30N_12	AM1	PULLUP			GPIO57			CN9-73		
12	IO_L30P_12	AM2	PULLUP			GPIO58			CN9-74		
12	IO_L31N_12	AG7	PULLUP			GPIO45			CN9-58		
12	IO_L31P_12	AG8	PULLUP			GPIO60			CN9-77		
12	IO_L32N_12	AL3	PULLUP			GPIO56			CN9-72		
12	IO_L32P_12	AM3	PULLUP			GPIO59			CN9-75		
12	IO_L3N_12	AA11	PULLUP			GPIO5			CN9-8		
12	IO_L3P_12	Y11	PULLUP			GPIO0			CN9-2		
12	IO_L4N_VREF_12	AD1	PULLUP			GPIO22			CN9-29		
12	IO_L4P_12	AD2	PULLUP			GPIO23			CN9-30		
12	IO_L5N_12	AA13	PULLUP			GPIO6			CN9-9		
12	IO_L5P_12	Y14	PULLUP			GPIO3			CN9-5		
12	IO_L6N_12	AC4	PULLUP			GPIO18			CN9-24		
12	IO_L6P_12	AC5	PULLUP			GPIO19			CN9-25		
12	IO_L7N_12	AE1	PULLUP			GPIO28			CN9-37		
12	IO_L7P_12	AF1	PULLUP			GPIO34			CN9-44		
12	IO_L8N_CC_LC_12	AA8	PULLUP			GPIO8			CN9-12		

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESIP/V850EP1 Port Pins
12	IO_L8P_CC_LC_12	AA9	PULLUP			GPIO9			CN9-13		
12	IO_L9N_CC_LC_12	Y12	PULLUP			GPIO1			CN9-3		
12	IO_L9P_CC_LC_12	Y13	PULLUP			GPIO2			CN9-4		
12	VCCO_12	AA12									
12	VCCO_12	AB9									
12	VCCO_12	AC6									
12	VCCO_12	AD3									
12	VCCO_12	AF7									
12	VCCO_12	AG4									
12	VCCO_12	AH1									
12	VCCO_12	AL2									
12	VCCO_12	Y15									
13	IO_L10N_13	T31		NC							
13	IO_L10P_13	R31		NC							
13	IO_L11N_13	R33		NC							
13	IO_L11P_13	R32		NC							
13	IO_L12N_VREF_13	U28		NC							
13	IO_L12P_13	T28		NC							
13	IO_L13N_13	T30		NC							
13	IO_L13P_13	T29		NC							
13	IO_L14N_13	T34		NC							
13	IO_L14P_13	T33		NC							
13	IO_L15N_13	U27		NC							
13	IO_L15P_13	U26		NC							
13	IO_L16N_13	U31		NC							
13	IO_L16P_13	U30		NC							
13	IO_L17N_13	V34		NC							
13	IO_L17P_13	V33		NC							
13	IO_L18N_13	U33		NC							
13	IO_L18P_13	U32		NC							
13	IO_L19N_13	U25		NC							
13	IO_L19P_13	V25		NC							
13	IO_L1N_13	U23		NC							
13	IO_L1P_13	T23		NC							
13	IO_L20N_VREF_13	V29		NC							
13	IO_L20P_13	V28		NC							
13	IO_L21N_13	V24		NC							
13	IO_L21P_13	V23		NC							
13	IO_L22N_13	V32		NC							
13	IO_L22P_13	W32		NC							
13	IO_L23N_VRP_13	W34		NC							
13	IO_L23P_VRN_13	Y34		NC							
13	IO_L24N_CC_LC_13	V30		NC							
13	IO_L24P_CC_LC_13	W30		NC							
13	IO_L25N_CC_LC_13	Y33		NC							
13	IO_L25P_CC_LC_13	Y32		NC							
13	IO_L26N_13	V27		NC							
13	IO_L26P_13	W27		NC							
13	IO_L27N_13	W29		NC							
13	IO_L27P_13	Y29		NC							
13	IO_L28N_VREF_13	W31		NC							
13	IO_L28P_13	Y31		NC							

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESIP/V850EP1 Port Pins
13	IO_L29N_13	AB33		NC							
13	IO_L29P_13	AB32		NC							
13	IO_L2N_13	T26		NC							
13	IO_L2P_13	R26		NC							
13	IO_L30N_13	AA34		NC							
13	IO_L30P_13	AA33		NC							
13	IO_L31N_13	AA31		NC							
13	IO_L31P_13	AB31		NC							
13	IO_L32N_13	Y28		NC							
13	IO_L32P_13	Y27		NC							
13	IO_L3N_13	T25		NC							
13	IO_L3P_13	T24		NC							
13	IO_L4N_VREF_13	R28		NC							
13	IO_L4P_13	R27		NC							
13	IO_L5N_13	R29		NC							
13	IO_L5P_13	P29		NC							
13	IO_L6N_13	P32		NC							
13	IO_L6P_13	N32		NC							
13	IO_L7N_13	P31		NC							
13	IO_L7P_13	P30		NC							
13	IO_L8N_CC_LC_13	N34		NC							
13	IO_L8P_CC_LC_13	N33		NC							
13	IO_L9N_CC_LC_13	R34		NC							
13	IO_L9P_CC_LC_13	P34		NC							
13	VCCO_13	AA32		NC							
13	VCCO_13	P33		NC							
13	VCCO_13	R30		NC							
13	VCCO_13	T27		NC							
13	VCCO_13	U24		NC							
13	VCCO_13	U34		NC							
13	VCCO_13	V31		NC							
13	VCCO_13	W28		NC							
14	IO_L10N_14	U3		NC							
14	IO_L10P_14	T3		NC							
14	IO_L11N_14	U7		NC							
14	IO_L11P_14	U8		NC							
14	IO_L12N_VREF_14	U1		NC							
14	IO_L12P_14	U2		NC							
14	IO_L13N_14	U11		NC							
14	IO_L13P_14	U12		NC							
14	IO_L14N_14	V10		NC							
14	IO_L14P_14	U10		NC							
14	IO_L15N_14	U5		NC							
14	IO_L15P_14	U6		NC							
14	IO_L16N_14	V2		NC							
14	IO_L16P_14	V3		NC							
14	IO_L17N_14	V8		NC							
14	IO_L17P_14	V9		NC							
14	IO_L18N_14	V4		NC							
14	IO_L18P_14	V5		NC							
14	IO_L19N_14	W5		NC							
14	IO_L19P_14	W6		NC							

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BANK	PIN_NAME	No.	Default	Pin Name	Alternative Function	GPIO	Component Name 1	Component Name 2	MICTOR	50 General -Purpose pin	50 PFESIP/V850EP1 Port Pins
14	IO_L1N_14	P4		NC							
14	IO_L1P_14	N4		NC							
14	IO_L20N_VREF_14	W1		NC							
14	IO_L20P_14	W2		NC							
14	IO_L21N_14	W12		NC							
14	IO_L21P_14	V12		NC							
14	IO_L22N_14	V7		NC							
14	IO_L22P_14	W7		NC							
14	IO_L23N_VRP_14	W4		NC							
14	IO_L23P_VRN_14	Y4		NC							
14	IO_L24N_CC_LC_14	Y2		NC							
14	IO_L24P_CC_LC_14	Y3		NC							
14	IO_L25N_CC_LC_14	AA4		NC							
14	IO_L25P_CC_LC_14	AA5		NC							
14	IO_L26N_14	Y1		NC							
14	IO_L26P_14	AA1		NC							
14	IO_L27N_14	AA3		NC							
14	IO_L27P_14	AB3		NC							
14	IO_L28N_VREF_14	AB1		NC							
14	IO_L28P_14	AB2		NC							
14	IO_L29N_14	Y6		NC							
14	IO_L29P_14	AA6		NC							
14	IO_L2N_14	N2		NC							
14	IO_L2P_14	N3		NC							
14	IO_L30N_14	Y7		NC							
14	IO_L30P_14	Y8		NC							
14	IO_L31N_14	W9		NC							
14	IO_L31P_14	Y9		NC							
14	IO_L32N_14	W10		NC							
14	IO_L32P_14	W11		NC							
14	IO_L3N_14	T8		NC							
14	IO_L3P_14	R8		NC							
14	IO_L4N_VREF_14	R6		NC							
14	IO_L4P_14	R7		NC							
14	IO_L5N_14	P1		NC							
14	IO_L5P_14	P2		NC							
14	IO_L6N_14	T4		NC							
14	IO_L6P_14	R4		NC							
14	IO_L7N_14	R2		NC							
14	IO_L7P_14	R3		NC							
14	IO_L8N_CC_LC_14	T1		NC							
14	IO_L8P_CC_LC_14	R1		NC							
14	IO_L9N_CC_LC_14	T5		NC							
14	IO_L9P_CC_LC_14	T6		NC							
14	VCCO_14	AA2		NC							
14	VCCO_14	P3		NC							
14	VCCO_14	T7		NC							
14	VCCO_14	U4		NC							
14	VCCO_14	V1		NC							
14	VCCO_14	V11		NC							
14	VCCO_14	W8		NC							
14	VCCO_14	Y5		NC							

CHAPTER 8 OTHER FUNCTIONS

8.1 Various LEDs

8.1.1 LED for FPGA (LED1 to LED8)

Positions	Figure 1-1 (Appearance) E-3 to F-3

The FPGA is connected to LEDs. The LEDs (green) can be lit by any signal thanks to the internal connections of the FPGA. The LEDs are lit when the LED connection pin output of the FPGA is “0”.

The LEDs are not lit while the FPGA is performing initialization, because the LED connection pins are pulled up.

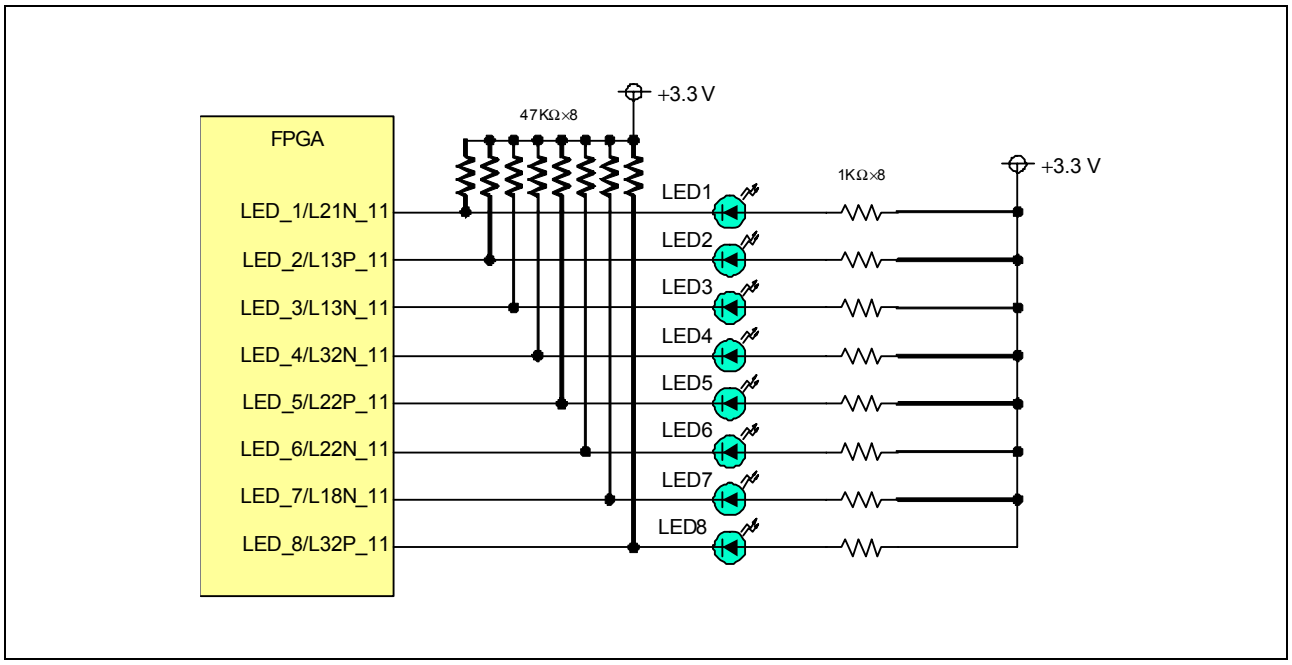
When the FPGA is in the default programming state, the LEDs are connected to a port (P20 to P27) of the PFESiP/V850EP1 and all LEDs are lit when the FPGA completes the initialization.

To use these LEDs, set P20 to P27 as output ports using the PM2 register.

Table 8-1. LED Operation with Default Program

P20 to P27	FPGA LEDs (LED1 to LED8)
00H	Turns off LEDs
FFH	Turns on LEDs

Figure 8-1. LED Circuit for FPGA



8.1.2 USB host port LEDs (LED9, LED10)

Positions **Figure 1-1 (Appearance) A-2 to B-2**

These LEDs indicate that the power of the two USB host ports is turned on. They glow red when the power is turned on.

USB Host Port	LED No.	Coordinates	Connector Stage
Port 0	LED9 (USB0) (red)	A-2	Lower stage
Port 1	LED10 (USB1) (red)	A-3	Upper stage

8.1.3 LED for FPGA DONE (LED11)

Position **Figure 1-1 (Appearance) A-3**

This LED indicates the configuration state of the FPGA.
It glows red during the configuration and is turned off when the configuration is completed.

LED11 State	Configuration State
Lit (red)	During configuration
Turned off	Configuration completed

8.1.4 Power supply LED (LED12)

Position **Figure 1-1 (Appearance) E-6**

Normally, the PFESiP EP-1 Evaluation Board is operated by supplying a single +5 V power supply.
LED12 glows blue when a +5 V is supplied.

LED12 State	Power Supply State
Lit (blue)	ON
Turned off	OFF

8.2 Serial Connectors

Positions **Figure 1-1 (Appearance) A-4, A-5, A-6**

These are connectors for the on-chip asynchronous serial interface (UART) of the PFESiP/V850EP1.
The PFESiP/V850EP1 has four UART channels and pins are assigned as shown below.

Pin Name	IO	Function	Alternative Function	After Reset
P30	IO	Port 3, 3.3 V interface 8-bit I/O ports P30 to P37 are shared with the asynchronous serial interface pins.	RXD0	Hi-Z
P31			TXD0	
P32			RXD1	
P33			TXD1	
P34			RXD2	
P35			TXD2	
P36			RXD3	
P37			TXD3	

The PFESiP EP-1 Evaluation Board is provided with two UART connectors (JSIO1, JSIO2).

In a structure where channels 0 and 2, or channels 1 and 3 are exclusively used, the unused TXD and RXD pins are assigned to CTS and RTS by using jumpers.

Caution To use P30 to P37 as ports, leave JP12, JP14, JP15, and JP17 open.

(1) JSIO1 (channel 0/channel2)

P35 and P34 are assigned to RTS and CTS, respectively, because TXD0 (P31) and RXD0 (P30) are used to generate interface signals and handshaking is performed via ports and software. The interface signals can be changed to be generated by TXD2 (P35) and RXD2 (P34) and handshaking can be changed to be performed via P31 (RTS) and P30 (CTS) by setting jumpers.

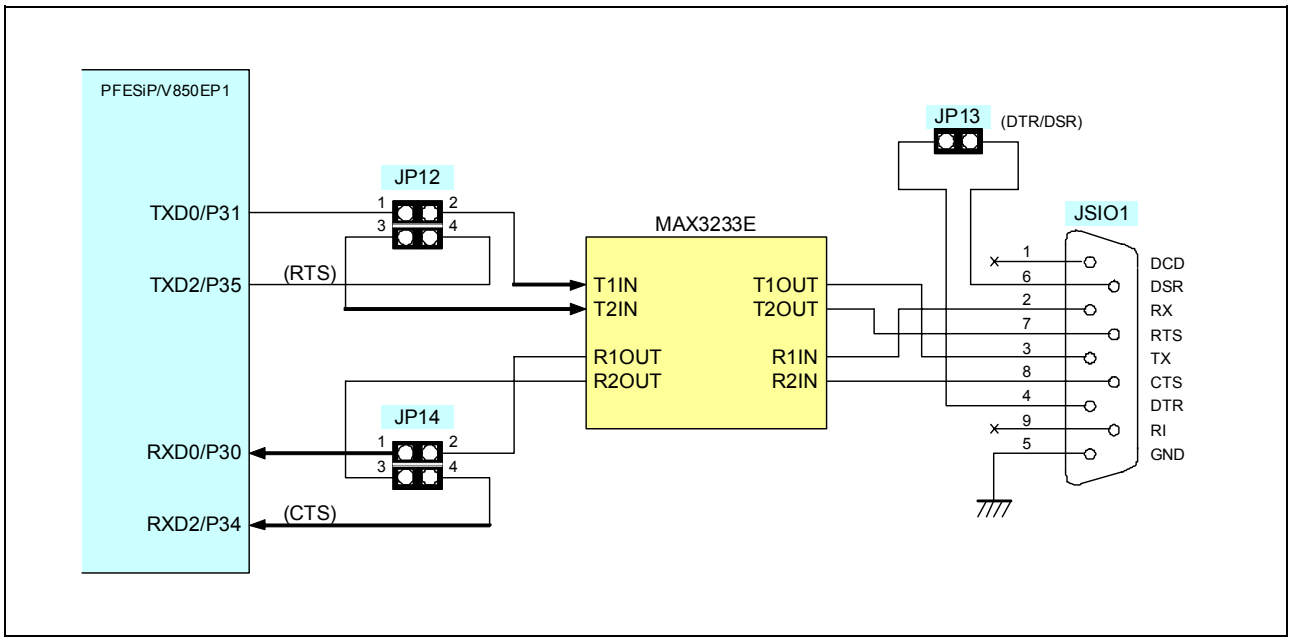
TXD0 (P31), RXD0 (P30), P35 (RTS), and P34 (CTS) of the PFESiP/V850EP1 use the MAX3233E whose voltage is raised to the RS-232C standard, because they are used for the 3.3 V interface.

A D-sub 9-pin connector (male) used for the COM port of an AT-compatible PC is used. Use a cross cable when connecting the host.

Since the pins of TXD0 (P31), TXD2 (P35), RXD0 (P30), and RXD2 (P34) are connected also to the FPGA, when the pins are used as serial interface, the pins on the FPGA side must be set to be unused (or inputs). To use them as general-purpose ports, leave JP12 and JP14 open.

Caution To use P30, P31, P34, and P35 as ports, leave JP12 and JP14 open.

Figure 8-2. JSIO1 Serial Connector



(2) JSIO2 (channel 1/channel 3)

P37 and P36 are assigned to RTS and CTS, respectively, because TXD1 (P33) and RXD1 (P32) are used to generate interface signals and handshaking is performed via ports and software. The interface signals can be changed to be generated by TXD3 (P37) and RXD3 (P36) and handshaking can be changed to be performed via P33 (RTS) and P32 (CTS) by setting jumpers.

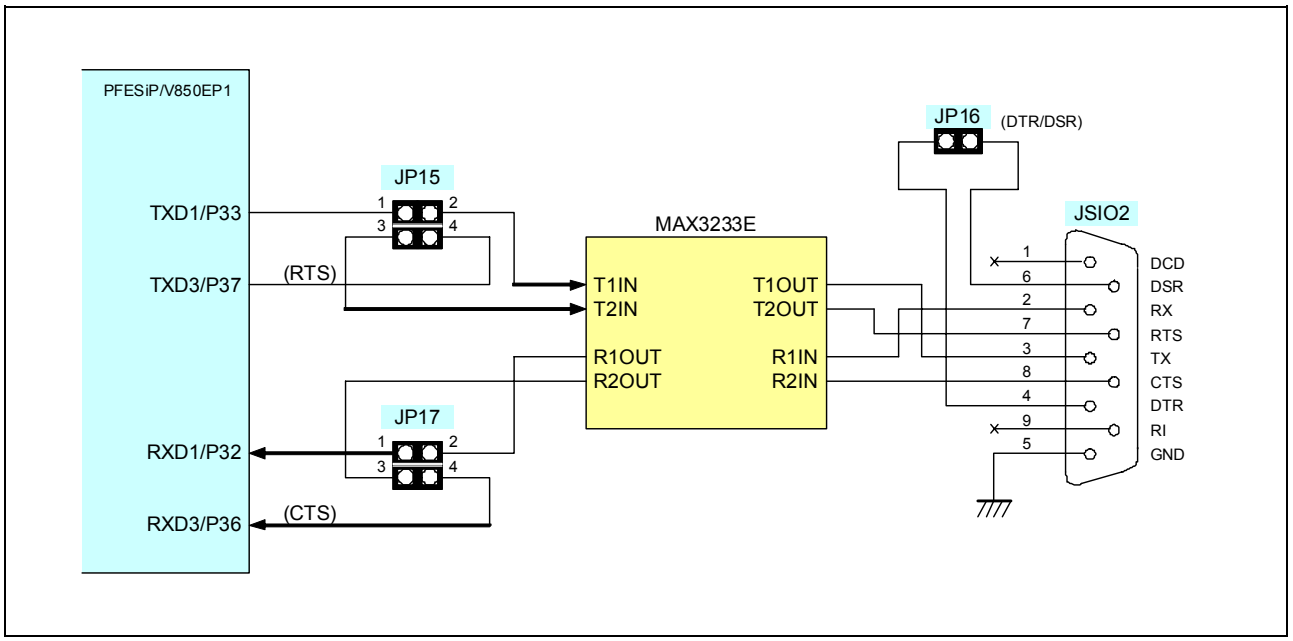
TXD1 (P33), RXD1 (P32), P37 (RTS), and P36 (CTS) of the PFESiP/V850EP1 use the MAX3233E whose voltage is raised to the RS-232C standard, because they are used for the 3.3 V interface.

A D-sub 9-pin connector (male) used for the COM port of an AT-compatible PC is used. Use a cross cable when connecting the host.

Since the pins of TXD1 (P33), TXD3 (P37), RXD1 (P32), and RXD3 (P36) are connected also to the FPGA, when the pins are used as serial interface, the pins on the FPGA side must be set to be unused (or inputs). To use them as general-purpose ports, leave JP15 and JP17 open.

Caution To use P32, P33, P36, and P37 as ports, leave JP15 and JP17 open.

Figure 8-3. JSIO2 Serial Connector



8.3 USB Function

The PFESiP/V850EP1 has an on-chip USB function controller and a USB host controller, both conforming to the Universal Serial Bus Specification.

- USB function controller:
  Supports 12 Mbps (full-speed) transfer
  Provided with 1-ch upstream ports
  Incorporates the following end points for transfer

End Point Name	FIFO Size (Bytes)	Transfer Type	Remark
EP0	64	Control Read/Write	
EP1	64×2	Bulk In	Double-buffer configuration
EP2	64×2	Bulk Out	Double-buffer configuration
EP7	8	Interrupt	

Bulk-in/-out data can be transferred by DMA transfer (2-clock transfer).

- USB host controller:
  Supports 12 Mbps (full-speed) and 1.5 Mbps (low-speed) transfer
  Supports OHCI (open host controller interface) 1.0a
  (The control for transitioning the disabled state of the USB port to the enabled state is restricted.)
  Incorporates a 2-ch root hub function and is provided with two downstream ports
  Uses an 8 KB on-chip SRAM and external SDRAM as shared memories

8.3.1 Peripheral circuit of USB function controller

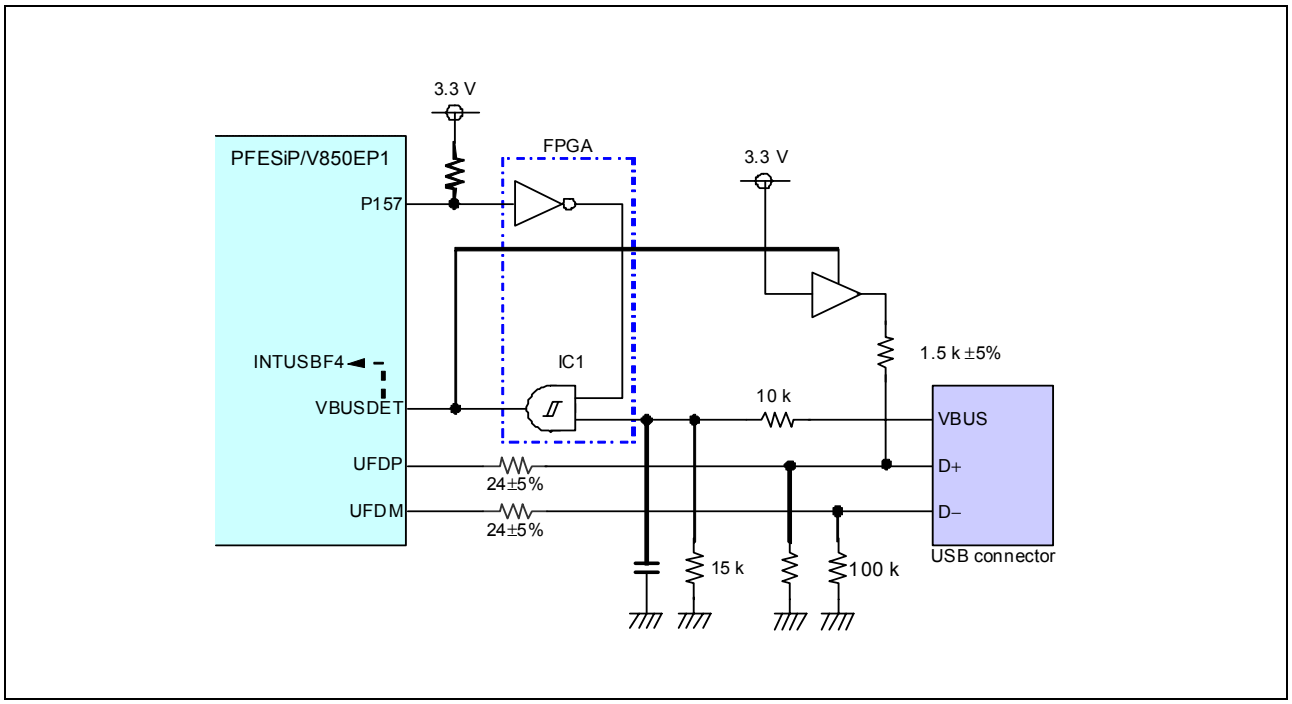
Position **Figure 1-1 (Appearance) A-3**

Resistors of 24 Ω ±5% are connected in series in the vicinity of the D+/D– pins (UFDP, UFDM) of the USB function controller of the PFESiP/V850EP1. The D+ pin (UFDP) is pulled up to 3.3 V at 1.5 kΩ ±5%, because the USB function controller of the PFESiP/V850EP1 supports full-speed (FS) transfer.

VBUS detection is performed using the VBUSDET pin. VBUS detection using the VBUSDET pin can be performed only when low level is output from P157. Pulling up the D+ pin (UFDP) is valid when high level is input to the VBUSDET pin.

The D+/ D– pins are pulled down at 100 kΩ to prevent a floating state of the pins when they are initialized or unused.

Figure 8-4. Peripheral circuit of USB Function Controller



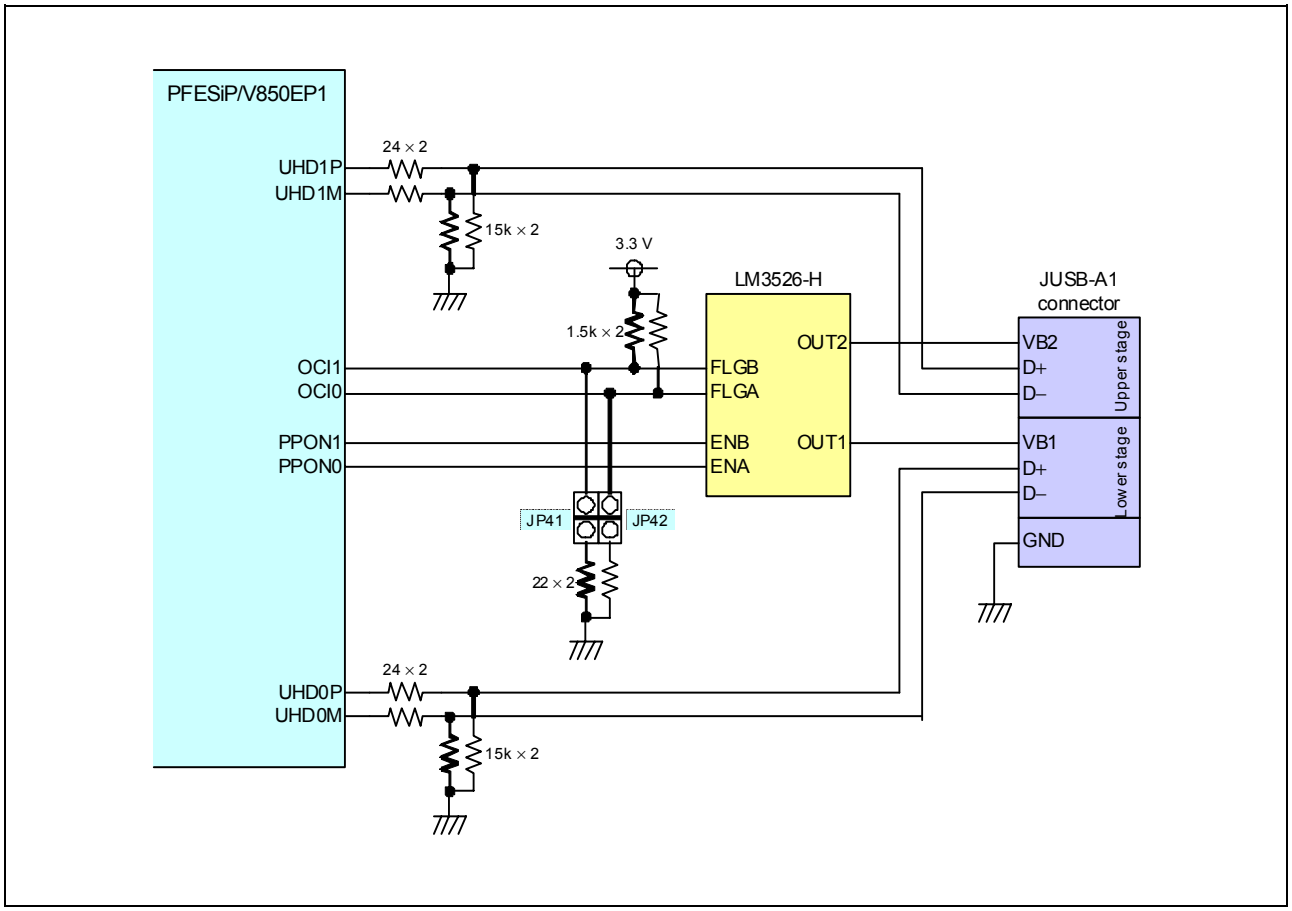
8.3.2 Peripheral circuit of USB host controller

Position **Figure 1-1 (Appearance) A-2**

Resistors of 24 Ω ±5% are connected in series in the vicinity of the D+/ D– pins (UHD0P, UHD0M, UHD1P, UHD1M) of the USB host controller of the PFESiP/V850EP1. The pins are pulled down to GND at 15 kΩ ±5%

The dual-port USB power switch with overcurrent protection (LM3526) is used as the power switch of the host controller.

Figure 8-5. Peripheral Circuit of USB Host Controller



8.3.3 USB host port LEDs (LED9, LED10)

Positions **Figure 1-1 (Appearance) A-2, B-2**

These LEDs indicate that the power of the two USB host ports is turned on. They glow red when the power is turned on.

USB Host Port	LED No.	Coordinates	Connector Stage
Port 0	LED9 (USB0) (red)	A-2	Lower stage
Port 1	LED10 (USB1) (red)	A-3	Upper stage

8.4 Analog Input Function

Position | **Figure 1-1 (Appearance) D-4**

8.4.1 Analog input terminal

AIN0 to AIN7 of the A/D converter of the PFESiP/V850EP1 are connected to terminals where GND and the signals are paired. Normally, AIN0 to AIN5 and AIN7 are shorted by GND and jumpers (JP9, JP11).

Normally, AIN6 is connected to a volume connected to the A/D converter but can also be changed to be connected to GND.

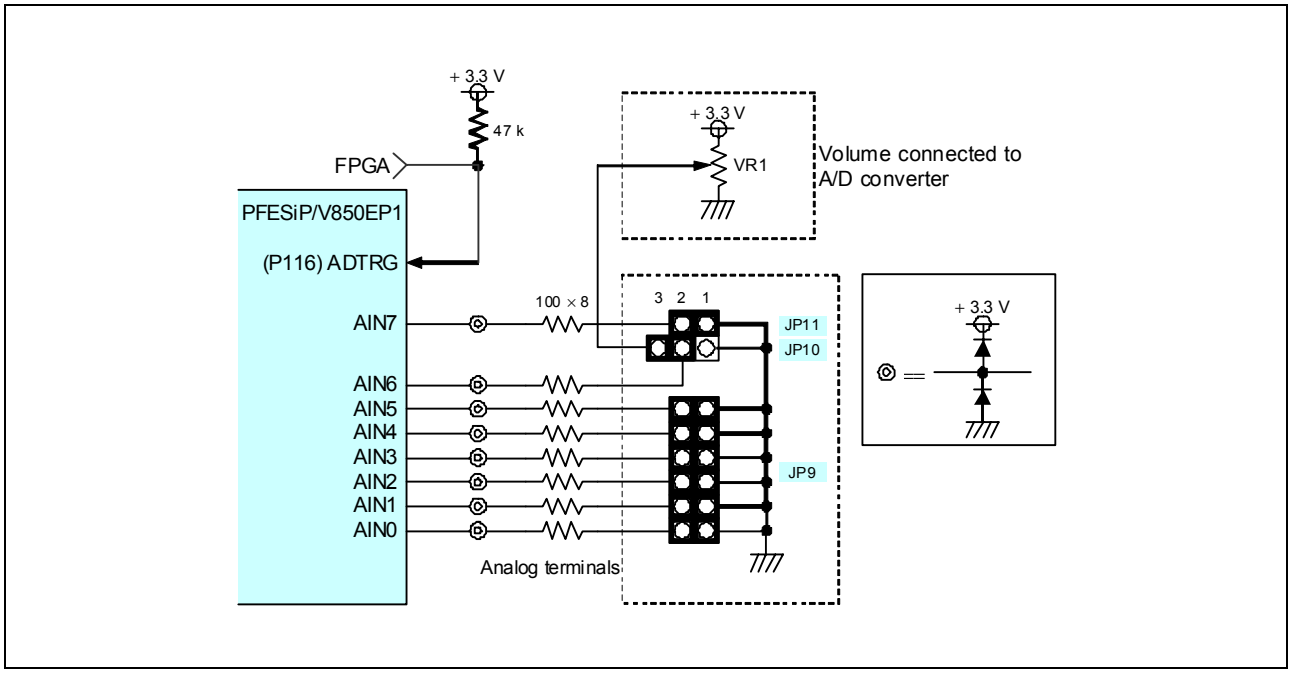
To externally input analog signals, connect the signals to these terminals using twisted pair lines by which each signal is paired with GND.

8.4.2 Volume connected to A/D converter

AIN6 of the A/D converter of the PFESiP/V850EP1 is connected to a volume that divides the 3.3 V power supply. At this time, JP10 is used with 2-3 shorted.

Analog signals can be input via twisted pair lines as with AIN0 to AIN5 and AIN7 by using 1-2 of JP10.

Figure 8-6. A/D Converter Connection Circuit



8.5 Power Supply Circuit

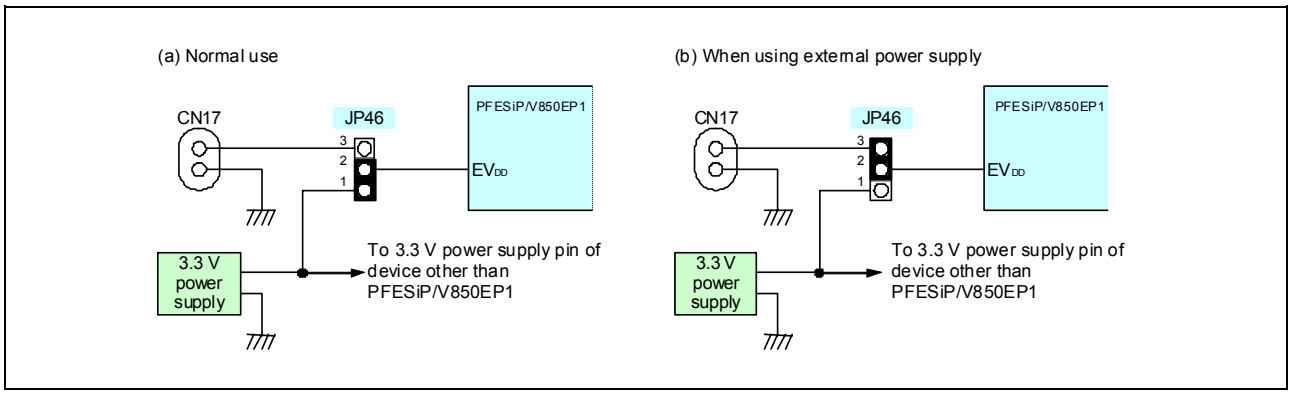
Positions | **Figure 1-1 (Appearance) H-1 to I-4**

Normally, the PFESiP EP-1 Evaluation Board uses only a single +5.0 V power supply. The power supplies required by each device are generated by the on-board power supply modules. At this time, connect an AC adapter to CN21 or CN23.

The on-board power supply modules contain a tiny amount of ripple components, because they are switching regulators. Consequently, an external stabilization power supply can also be used. In particular, +3.3 V and +1.5 V can be separately supplied from CN17 and CN18 only with the PFESiP/V850EP1. Even if CN17 and CN18 are used, however, supply +5.0 V from CN21, CN23, or CN16, because power must be supplied also to devices other than the PFESiP/V850EP1.

8.5.1 PFESiP/V850EP1 EV_{DD}: +3.3 V power supply

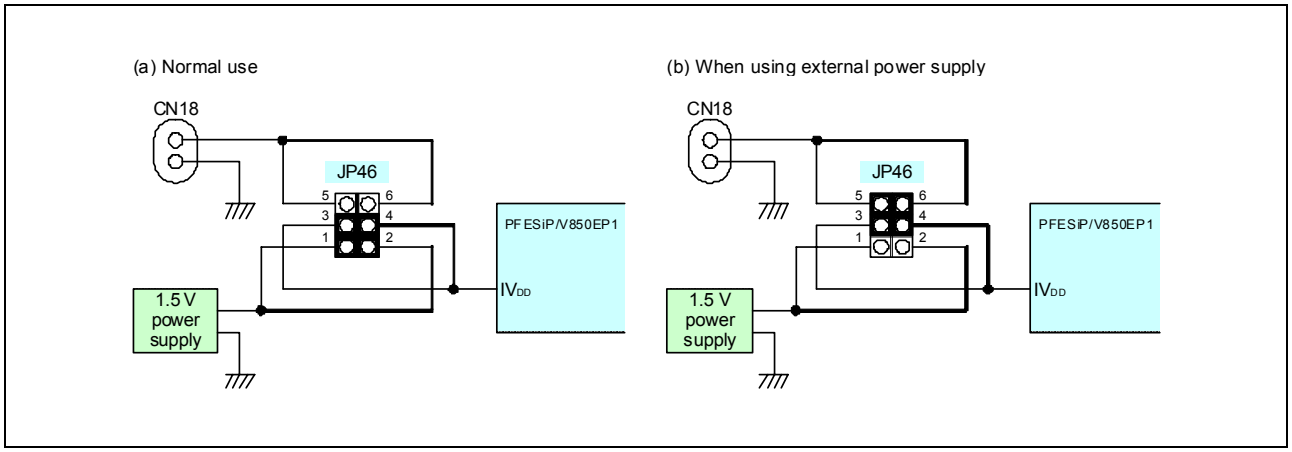
With the PFESiP EP-1 Evaluation Board, an on-board power supply or external power supply (CN17) can be selected as the 3.3 V power supply only used by the PFESiP/V850EP1. Use an external power supply and connect an ammeter when measuring the current.



Caution The 3.3 V power supply of other than the PFESiP/V850EP1 is generated from a 5.0 V power supply. Connect the 5.0 V power supply even when externally supplying EV_{DD}: 3.3 V of the PFESiP/V850EP1 by using CN17.

8.5.2 PFESiP/V850EP1 IV_{DD}: +1.5 V power supply

With the PFESiP EP-1 Evaluation Board, the 1.5 V power supply can be used only as an internal power supply. An on-board power supply or external power supply (CN18) can be selected as the 1.5 V power supply. Use an external power supply and connect an ammeter when measuring the current. Two jumpers are used to secure the current capacity.



8.6 Manipulation Switches

8.6.1 Reset switch

Position | **Figure 1-1 (Appearance) H-7**

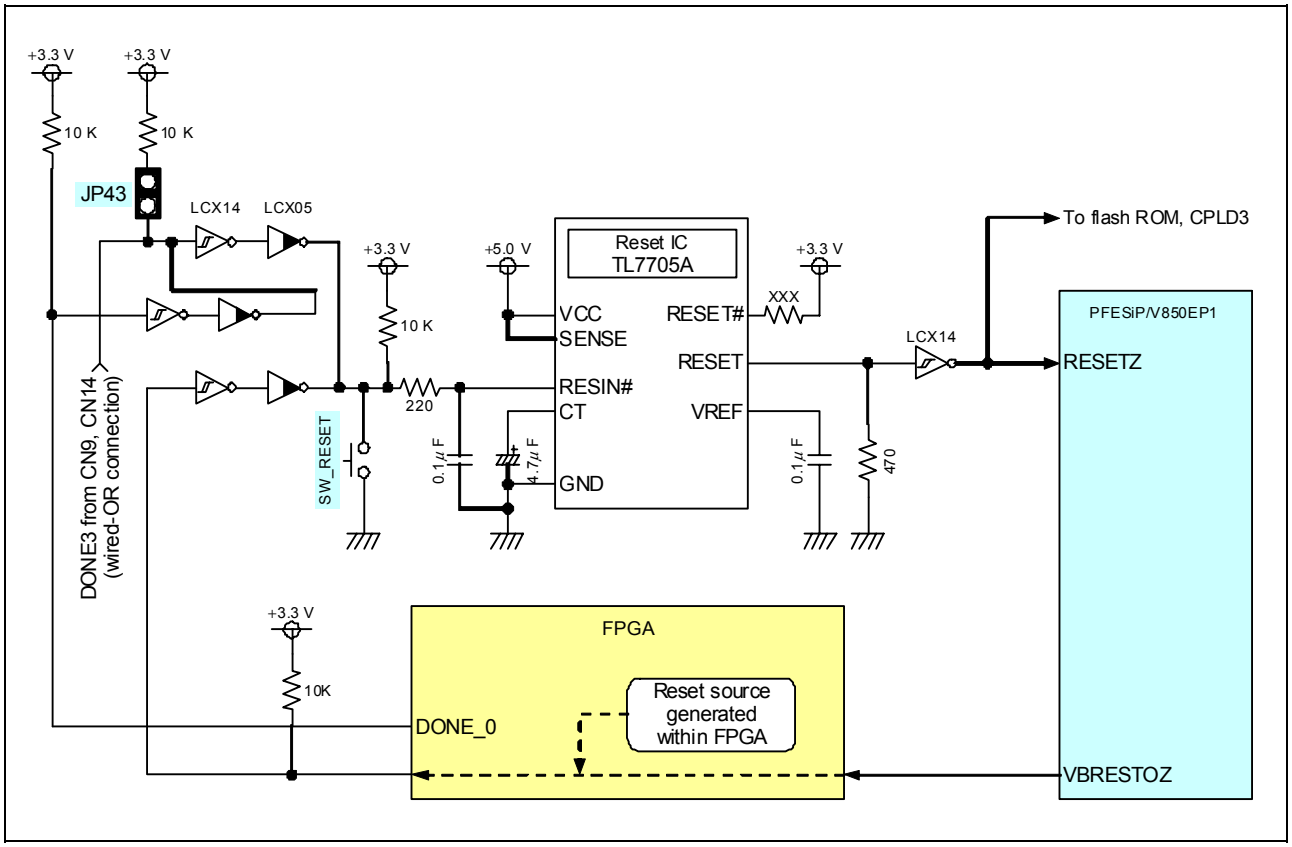
SW_RESET (RESETZ) is provided for reset purposes of the PFESiP/V850EP1.

SW_RESET is provided as a momentary-type toggle switch. The oscillation stabilization wait function, PLL lock wait function, and the reset functions required for clearing the pipeline are incorporated in the PFESiP/V850EP1. The PFESiP/V850EP1 starts waiting for oscillation stabilization when the reset input is released. The PFESiP/V850EP1 enters the reset state also when the FPGA is being configured.

This reset signal is also supplied to the flash ROM and CPLD3 that manages the flash ROM bank.

RESETZ can be manipulated via the FPGA in addition to manipulation with a switch. Manipulation via the FPGA must be performed with the all the switches turned off. As a countermeasure against conflicts due to program or manipulation errors, RESETZ is dumped from the FPGA pin via a 1 kΩ resistor.

Figure 8-7. Power-on-Reset Switch



8.6.2 Interrupt switches

Position	Figure 1-1 (Appearance) H-7

NMI (SW_NMI) and INTPZ7 (SW_INTP7) are on-board push switches with a built-in chattering prevention circuit. These switches operate when the on-board large-capacity FPGA is in the default programming state.

When the switches are not pressed, high level is output to the PFESiP/V850EP1.

When the switches are pressed, low level is output to the PFESiP/V850EP1.

SW_NMI, SW_INTP7	PFESiP/V850EP1 Input
Normal	High-level input
push	Low-level input

Make sure that all interrupt request flags are cleared in the initialization program, because an interrupt request flag will be set during booting if the internal initialization of when the power is turned on is earlier than the rise of the chattering prevention circuit power supply.

Caution To use NMI and INTPZ7 when rewriting the contents of the on-board FPGA, add the processing of NMI and INTPZ7 to the FPGA data.

CHAPTER 9 OPTION BOARD

A connector conversion board is available as an option board of the PFESiP EP-1 Evaluation Board.

9.1 Connector Conversion Boad

AMP MICTOR connectors are impedance-matching connectors and have characteristics suitable for high-speed transfer. However, they cannot be mounted on a general-purpose substrate so a dedicated board must be newly developed.

The connector conversion board converts AMP MICTOR connector (CN6, CN7, CN9) signals to signals of the three 50-pin general-purpose connectors. A variety of external I/O signals can be easily used by using the connector conversion board.

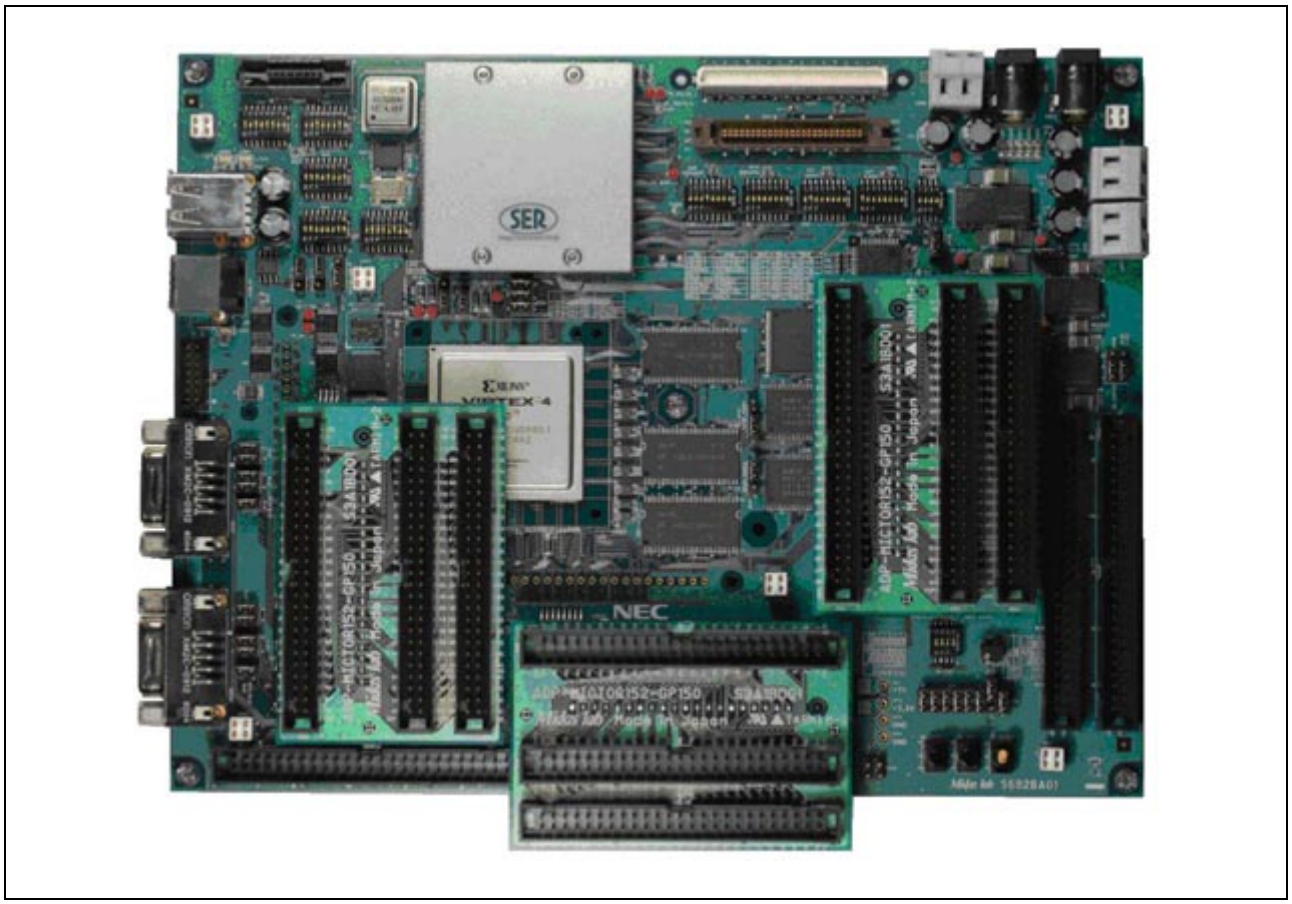
The signals going through the connector conversion board, however, are not suitable for high-speed transfer. Generally, use the signals for simple debugging until a dedicated board using AMP MICTOR connectors is procured or for simple observation of signals.

9.1.1 Shape of connector conversion board

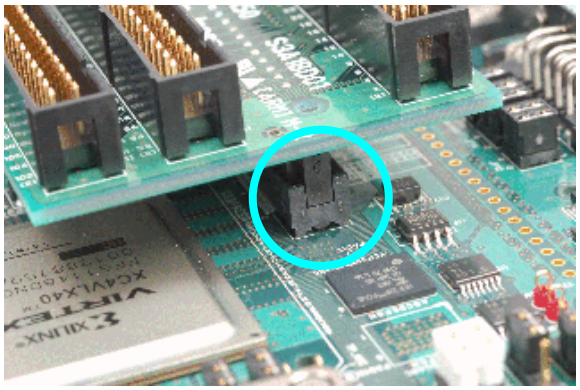
9.1.2 Installing connector conversion boards

Fit the plug (connector conversion board) of the AMP MICTOR connector and the receptacle (PFESiP EP-1 Evaluation Board) as shown in the picture below.

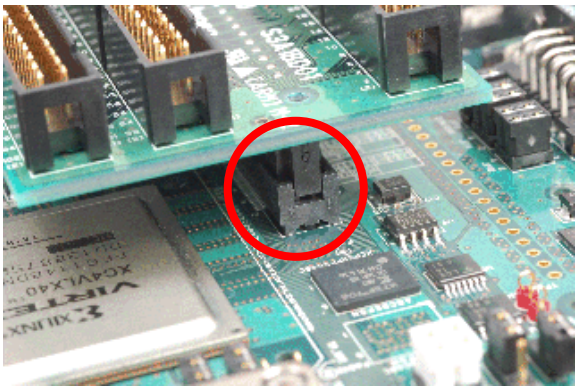
Various switches on the PFESiP EP-1 Evaluation Board will interfere, but the connector conversion boards can be installed to all positions of CN6, CN7, and CN9 at the same time.



Good installation



Bad installation



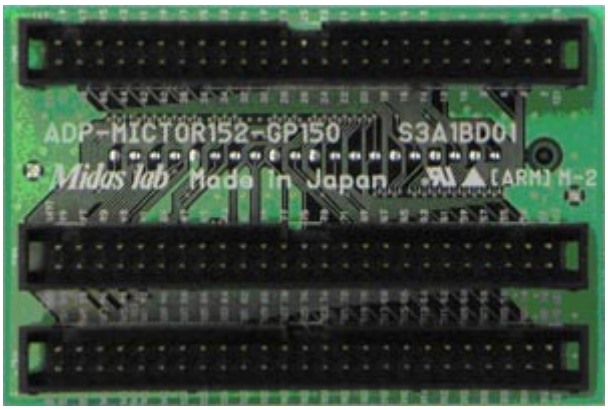
9.1.3 Signal assignment of AMP MICTOR and general-purpose connectors

The AMP MICTOR connectors for expansion of the PFESiP/V850EP1 are 152-pin type connectors.

On the other hand, there are three general-purpose 50-pin connectors supporting up to 150 signals.

Consequently, pins 143 and 144 of the AMP MICTOR connectors are not connected. Other signals are connected in a one-to-one correspondence. The silk marks on the connector conversion boards correspond to the pin numbers of the AMP MICTOR connectors. The ground line located at the center of each AMP MICTOR connector is used as the conversion substrate ground pattern. Pins 143 and 144 of CN6, CN7, and CN9 are the power supply lines as shown below.

	CN6	CN7	CN9
Pin 143	+ 3.3 V		
Pin 144	+ 5.0 V		



APPENDIX A FPGA PIN PROCESSING

A.1 ISE Software User Constraint File (.ucf)

The XC4VLX40FF1148-11 is mounted as the standard on-board FPGA. Generally, the ISE software is used as the design tool of this FPGA.

Pin layout information matching the format of the ISE software user constraint file (.ucf) is provided in response to user request, because the FPGA pins are connected in a layout unique to the PFESiP EP-1 Evaluation Board.

The FPGA pins are defined by grid names, but the ISE software user constraint file (.ucf) to be provided enables the pin names to be specified by the PFESiP/V850EP1 pin names, connector numbers (CNn), and pin numbers. The default ISE software user constraint file (.ucf) is shown below.

Caution Do not use multiple signal names for a single pin.
For example, do not use P0<0> and INTPZ<0> at the same time.

Default .ucf file (1/6)

```
#PACE: Start of PACE I/O Pin Assignments
# --- P2 ---
NET "P2<0>"  LOC = "B2" | IOSTANDARD = LVCMOS33 ;
NET "P2<1>"  LOC = "A3" | IOSTANDARD = LVCMOS33 ;
NET "P2<2>"  LOC = "B3" | IOSTANDARD = LVCMOS33 ;
NET "P2<3>"  LOC = "A4" | IOSTANDARD = LVCMOS33 ;
NET "P2<4>"  LOC = "C2" | IOSTANDARD = LVCMOS33 ;
NET "P2<5>"  LOC = "C3" | IOSTANDARD = LVCMOS33 ;
NET "P2<6>"  LOC = "C4" | IOSTANDARD = LVCMOS33 ;
NET "P2<7>"  LOC = "D1" | IOSTANDARD = LVCMOS33 ;
# --- PORT1 ---
NET "P1<0>"  LOC = "P7" | IOSTANDARD = LVCMOS33 ;
NET "P1<1>"  LOC = "P9" | IOSTANDARD = LVCMOS33 ;
NET "P1<2>"  LOC = "R11" | IOSTANDARD = LVCMOS33 ;
NET "P1<3>"  LOC = "R9" | IOSTANDARD = LVCMOS33 ;
NET "P1<4>"  LOC = "F4" | IOSTANDARD = LVCMOS33 ;
NET "P1<5>"  LOC = "F5" | IOSTANDARD = LVCMOS33 ;
NET "P1<6>"  LOC = "G1" | IOSTANDARD = LVCMOS33 ;
NET "P1<7>"  LOC = "G2" | IOSTANDARD = LVCMOS33 ;
# --- Aurora cont. ---
NET "FRESET"  LOC = "AE32" | IOSTANDARD = LVCMOS33 ;
# --- FPGA1 unused ---
NET "SROM_CLK"  LOC = "AD32" | IOSTANDARD = LVCMOS33 ;
NET "SROM_D"  LOC = "AD34" | IOSTANDARD = LVCMOS33 ;
NET "SROM_S"  LOC = "AE29" | IOSTANDARD = LVCMOS33 ;
NET "SROM_Q"  LOC = "AE31" | IOSTANDARD = LVCMOS33 ;
NET "CSICSZ"  LOC = "T10" | IOSTANDARD = LVCMOS33 ;
NET "PAD<1>"  LOC = "G11" | IOSTANDARD = LVCMOS33 ;
NET "PAD<2>"  LOC = "M3" | IOSTANDARD = LVCMOS33 ;
NET "PAD<3>"  LOC = "AJ31" | IOSTANDARD = LVCMOS33 ;
# --- FPGA1 push switch ---
NET "NMI_IN"  LOC = "G3" | IOSTANDARD = LVCMOS33 ;
NET "NMI_OUT"  LOC = "H3" | IOSTANDARD = LVCMOS33 ;
NET "SW_INTP7"  LOC = "E24" | IOSTANDARD = LVCMOS33 ;
NET "INTPZ<7>"  LOC = "K3" | IOSTANDARD = LVCMOS33 ;

# --- FPGA1 DIPSW ---
NET "DIPSW<1>"  LOC = "AE33" | IOSTANDARD = LVCMOS33 ;
NET "DIPSW<2>"  LOC = "AE34" | IOSTANDARD = LVCMOS33 ;
NET "DIPSW<3>"  LOC = "AF29" | IOSTANDARD = LVCMOS33 ;
NET "DIPSW<4>"  LOC = "AF30" | IOSTANDARD = LVCMOS33 ;
NET "DIPSW<5>"  LOC = "AF31" | IOSTANDARD = LVCMOS33 ;
NET "DIPSW<6>"  LOC = "AF33" | IOSTANDARD = LVCMOS33 ;
NET "DIPSW<7>"  LOC = "AF34" | IOSTANDARD = LVCMOS33 ;
NET "DIPSW<8>"  LOC = "AG30" | IOSTANDARD = LVCMOS33 ;
# --- FPGA1 LED ---
NET "LED<1>"  LOC = "AG31" | IOSTANDARD = LVCMOS33 ;
NET "LED<2>"  LOC = "AG32" | IOSTANDARD = LVCMOS33 ;
NET "LED<3>"  LOC = "AG33" | IOSTANDARD = LVCMOS33 ;
NET "LED<4>"  LOC = "AH30" | IOSTANDARD = LVCMOS33 ;
NET "LED<5>"  LOC = "AH32" | IOSTANDARD = LVCMOS33 ;
NET "LED<6>"  LOC = "AH33" | IOSTANDARD = LVCMOS33 ;
NET "LED<7>"  LOC = "AH34" | IOSTANDARD = LVCMOS33 ;
NET "LED<8>"  LOC = "AJ30" | IOSTANDARD = LVCMOS33 ;

# --- GPIO[287:0]
NET "GPIO<262>"  LOC = "AC25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<263>"  LOC = "AC27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<264>"  LOC = "AD26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<265>"  LOC = "AA23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<266>"  LOC = "AA24" | IOSTANDARD = LVCMOS33 | PULLUP ;
```

Default.ucf file (2/6)

```
NET "GPIO<267>"  LOC = "AA25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<268>"  LOC = "AA26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<269>"  LOC = "AA28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<270>"  LOC = "AA29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<271>"  LOC = "AA30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<272>"  LOC = "AB22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<273>"  LOC = "AB23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<274>"  LOC = "AB25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<275>"  LOC = "AB26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<276>"  LOC = "AB28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<277>"  LOC = "AB30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<278>"  LOC = "AC28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<279>"  LOC = "AC29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<280>"  LOC = "AC30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<281>"  LOC = "AC32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<282>"  LOC = "AC33" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<283>"  LOC = "AC34" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<284>"  LOC = "AD27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<285>"  LOC = "AD29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<286>"  LOC = "AD30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<287>"  LOC = "AD31" | IOSTANDARD = LVCMOS33 | PULLUP ;


NET "GPIO<258>"  LOC = "W24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<259>"  LOC = "W25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<260>"  LOC = "Y24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<261>"  LOC = "Y26" | IOSTANDARD = LVCMOS33 | PULLUP ;


NET "GPIO<220>"  LOC = "J34" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<221>"  LOC = "K28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<222>"  LOC = "K29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<223>"  LOC = "K31" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<224>"  LOC = "K32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<225>"  LOC = "K33" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<226>"  LOC = "K34" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<227>"  LOC = "K27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<228>"  LOC = "L28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<229>"  LOC = "L29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<230>"  LOC = "L30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<231>"  LOC = "L31" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<232>"  LOC = "L33" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<233>"  LOC = "L34" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<234>"  LOC = "M27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<235>"  LOC = "M28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<236>"  LOC = "M30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<237>"  LOC = "M31" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<238>"  LOC = "M32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<239>"  LOC = "M33" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<240>"  LOC = "N22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<241>"  LOC = "N23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<242>"  LOC = "N25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<243>"  LOC = "N27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<244>"  LOC = "N29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<245>"  LOC = "N30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<246>"  LOC = "P20" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<247>"  LOC = "P22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<248>"  LOC = "P24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<249>"  LOC = "P26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<250>"  LOC = "P27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<251>"  LOC = "R19" | IOSTANDARD = LVCMOS33 | PULLUP ;
```

Default .ucf file (3/6)

```
NET "GPIO<252>"  LOC = "R21" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<253>"  LOC = "R22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<254>"  LOC = "R23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<255>"  LOC = "R24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<256>"  LOC = "M26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<257>"  LOC = "M25" | IOSTANDARD = LVCMOS33 | PULLUP ;

NET "GPIO<219>"  LOC = "AJ12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<218>"  LOC = "AK12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<217>"  LOC = "AM12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<216>"  LOC = "AN12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<215>"  LOC = "AP12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<214>"  LOC = "AK13" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<213>"  LOC = "AL13" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<212>"  LOC = "AM13" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<211>"  LOC = "AN13" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<210>"  LOC = "AN14" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<209>"  LOC = "AP14" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<208>"  LOC = "AF11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<207>"  LOC = "AE11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<206>"  LOC = "AG10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<205>"  LOC = "AF10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<204>"  LOC = "AD10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<203>"  LOC = "AD9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<202>"  LOC = "AE16" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<201>"  LOC = "AF16" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<200>"  LOC = "AG16" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<199>"  LOC = "AE17" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<198>"  LOC = "AG17" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<197>"  LOC = "AH17" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<196>"  LOC = "AJ17" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<195>"  LOC = "AK17" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<194>"  LOC = "AE18" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<193>"  LOC = "AF18" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<192>"  LOC = "AG18" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<191>"  LOC = "AH18" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<190>"  LOC = "AK18" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<189>"  LOC = "AH19" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<188>"  LOC = "AJ19" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<187>"  LOC = "AK19" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<186>"  LOC = "AF24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<185>"  LOC = "AG25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<184>"  LOC = "AE26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<183>"  LOC = "AE27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<182>"  LOC = "AG27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<181>"  LOC = "AF28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<180>"  LOC = "AK21" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<179>"  LOC = "AL21" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<178>"  LOC = "AM21" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<177>"  LOC = "AP21" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<176>"  LOC = "AK22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<175>"  LOC = "AM22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<174>"  LOC = "AN22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<173>"  LOC = "AP22" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<172>"  LOC = "AG23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<171>"  LOC = "AH23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<170>"  LOC = "AK23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<169>"  LOC = "AL23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<168>"  LOC = "AM23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<167>"  LOC = "AN23" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<166>"  LOC = "AH24" | IOSTANDARD = LVCMOS33 | PULLUP ;
```

Default .ucf file (4/6)

```
NET "GPIO<165>"  LOC = "AJ24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<164>"  LOC = "AK24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<163>"  LOC = "AL24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<162>"  LOC = "AN24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<161>"  LOC = "AP24" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<160>"  LOC = "AH25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<159>"  LOC = "AJ25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<158>"  LOC = "AL25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<157>"  LOC = "AM25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<156>"  LOC = "AN25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<155>"  LOC = "AP25" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<154>"  LOC = "AF26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<153>"  LOC = "AG26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<152>"  LOC = "AK26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<151>"  LOC = "AL26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<150>"  LOC = "AM26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<149>"  LOC = "AP26" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<148>"  LOC = "AH27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<147>"  LOC = "AJ27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<146>"  LOC = "AK27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<145>"  LOC = "AM27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<144>"  LOC = "AN27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<143>"  LOC = "AP27" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<142>"  LOC = "AG28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<141>"  LOC = "AH28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<140>"  LOC = "AK28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<139>"  LOC = "AL28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<138>"  LOC = "AM28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<137>"  LOC = "AN28" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<136>"  LOC = "AH29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<135>"  LOC = "AJ29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<134>"  LOC = "AK29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<133>"  LOC = "AL29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<132>"  LOC = "AN29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<131>"  LOC = "AP29" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<130>"  LOC = "AL30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<129>"  LOC = "AM30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<128>"  LOC = "AN30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<127>"  LOC = "AP30" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<126>"  LOC = "AP31" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<125>"  LOC = "AN32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<124>"  LOC = "AP32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<123>"  LOC = "AN33" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<122>"  LOC = "AJ32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<121>"  LOC = "AJ34" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<120>"  LOC = "AK31" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<119>"  LOC = "AK32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<118>"  LOC = "AK33" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<117>"  LOC = "AK34" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<116>"  LOC = "AL31" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<115>"  LOC = "AL33" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<114>"  LOC = "AL34" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<113>"  LOC = "AM31" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<112>"  LOC = "AM32" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<111>"  LOC = "AM33" | IOSTANDARD = LVCMOS33 | PULLUP ;

NET "GPIO<64>"  LOC = "AN2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<65>"  LOC = "AN3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<66>"  LOC = "AJ4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<67>"  LOC = "AK4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<68>"  LOC = "AL4" | IOSTANDARD = LVCMOS33 | PULLUP ;
```

Default .ucf file (5/6)

```
NET "GPIO<69>"  LOC = "AN4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<70>"  LOC = "AP4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<71>"  LOC = "AJ5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<72>"  LOC = "AL5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<73>"  LOC = "AM5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<74>"  LOC = "AN5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<75>"  LOC = "AP5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<76>"  LOC = "AJ6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<77>"  LOC = "AK6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<78>"  LOC = "AL6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<79>"  LOC = "AM6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<80>"  LOC = "AP6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<81>"  LOC = "AH7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<82>"  LOC = "AJ7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<83>"  LOC = "AK7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<84>"  LOC = "AM7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<85>"  LOC = "AN7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<86>"  LOC = "AP7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<87>"  LOC = "AH8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<88>"  LOC = "AK8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<89>"  LOC = "AL8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<90>"  LOC = "AM8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<91>"  LOC = "AN8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<92>"  LOC = "AE9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<93>"  LOC = "AJ9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<94>"  LOC = "AK9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<95>"  LOC = "AL9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<96>"  LOC = "AN9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<97>"  LOC = "AP9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<98>"  LOC = "AH10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<99>"  LOC = "AJ10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<100>"  LOC = "AL10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<101>"  LOC = "AM10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<102>"  LOC = "AN10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<103>"  LOC = "AP10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<104>"  LOC = "AG11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<105>"  LOC = "AJ11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<106>"  LOC = "AK11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<107>"  LOC = "AL11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<108>"  LOC = "AM11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<109>"  LOC = "AP11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<110>"  LOC = "AH12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<0>"  LOC = "Y11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<1>"  LOC = "Y12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<2>"  LOC = "Y13" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<3>"  LOC = "Y14" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<4>"  LOC = "Y16" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<5>"  LOC = "AA11" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<6>"  LOC = "AA13" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<7>"  LOC = "AA15" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<8>"  LOC = "AA8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<9>"  LOC = "AA9" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<10>"  LOC = "AB10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<11>"  LOC = "AB12" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<12>"  LOC = "AB13" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<13>"  LOC = "AB5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<14>"  LOC = "AB6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<15>"  LOC = "AB8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<16>"  LOC = "AC2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<17>"  LOC = "AC3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<18>"  LOC = "AC4" | IOSTANDARD = LVCMOS33 | PULLUP ;
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Default .ucf file (6/6)

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NET "GPIO<19>"  LOC = "AC5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<20>"  LOC = "AC7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<21>"  LOC = "AC8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<22>"  LOC = "AD1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<23>"  LOC = "AD2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<24>"  LOC = "AD4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<25>"  LOC = "AD5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<26>"  LOC = "AD6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<27>"  LOC = "AD7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<28>"  LOC = "AE1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<29>"  LOC = "AE2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<30>"  LOC = "AE3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<31>"  LOC = "AE4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<32>"  LOC = "AE6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<33>"  LOC = "AE7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<34>"  LOC = "AF1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<35>"  LOC = "AF3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<36>"  LOC = "AF4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<37>"  LOC = "AF5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<38>"  LOC = "AF6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<39>"  LOC = "AF8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<40>"  LOC = "AG1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<41>"  LOC = "AG2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<42>"  LOC = "AG3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<43>"  LOC = "AG5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<44>"  LOC = "AG6" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<45>"  LOC = "AG7" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<46>"  LOC = "AH2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<47>"  LOC = "AH3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<48>"  LOC = "AH4" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<49>"  LOC = "AH5" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<50>"  LOC = "AJ1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<51>"  LOC = "AJ2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<52>"  LOC = "AK1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<53>"  LOC = "AK2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<54>"  LOC = "AK3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<55>"  LOC = "AL1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<56>"  LOC = "AL3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<57>"  LOC = "AM1" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<58>"  LOC = "AM2" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<59>"  LOC = "AM3" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<60>"  LOC = "AG8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<61>"  LOC = "AE8" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<62>"  LOC = "AC10" | IOSTANDARD = LVCMOS33 | PULLUP ;
NET "GPIO<63>"  LOC = "AC9" | IOSTANDARD = LVCMOS33 | PULLUP ;

#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE
```

[MEMO]

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