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Renesas Electronics Corporation

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RENESAS

User's Manual

PFESiP/V850EP1

32-bit Microcontroller Dedicated to PFESiP® EP-1

Product Data

Document No. A19069EJ2V0UM00 (2nd Edition)
Date published September 2009 NS

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E0904E

Major Revisions in This Edition

Location	Contents
p.16	Modification of **Table.1-8 Input Clock Timing**
p.17	Modification of **1.7.1 (2) Output Clock**

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

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PREFACE

Readers This manual is intended for users who understand the functions of the microcontroller function chip with an on-chip V850E2 CPU core (PFESiP/V850EP1) and wish to evaluate developing PFESiP EP-1 Series products using the chip.

Purpose This manual is intended to give users an understanding of the electrical specifications of the PFESiP/V850EP1.

How to Read This Manual It is assumed that readers of this manual have general knowledge of electricity, logic circuits, microcontrollers, SRAM, Page ROM and SDRAM.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxxZ (Add Z after pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ..... XXXX or XXXXB
	Decimal XXXX
	Hexadecimal ...XXXXH
Prefix indicating power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data type:	Word ... 32 bits
	Halfword ... 16 bits
	Byte ... 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to PFESiP EP-1 Series

Document Name	Document No.
V850E2 Architecture User's Manual	U17135E
EP-1 Series Design Manual	A19068E
PFESiP/V850EP1 Product Data User's Manual	This manual
PFESiP/V850EP1 Hardware (CPU Function) User's Manual	A19070E
PFESiP/V850EP1 Hardware (USB Function) User's Manual	A19071E
PFESiP/V850EP1 Hardware USB Function Sample Software Application Note	A19349E

Documents related to PFESiP EP-1 Evaluation Board

Document Name	Document No.
PFESiP EP-1 Evaluation Board Technical Information User's Manual	A19350E
PFESiP EP-1 Evaluation Board Lite Technical Information User's Manual	A19354E

Documents related to development tools

Document Name			Document No.
RX850 Pro User's Manual	Ver.3.21	Basics	U18165E
	Ver.3.20	Installation	U17421E
	Ver.3.21	Technical	U18164E
	Ver.3.20	Task Debugger	U17422E

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CHAPTER 1 PRODUCT SPECIFCATIONS

1.1 Terminology

Table 1-1. Terminology for Absolute Maximum Ratings

Item	Symbol	Definition
Power supply voltage	V_{DD}	Range of voltages which will not damage or reduce reliability when applied to the V_{DD} pin.
Input voltage	V_I	Range of voltages which will not damage or reduce reliability when applied to the input pin.
Output voltage	V_O	Range of voltages which will not damage or reduce reliability when applied to the output pin.
Input current	I_I	Maximum current which will not cause latchup when applied to the input pin.
Output current	I_O	Maximum DC current which will not cause damage or reduce reliability when flowing to or from the output pin.
Operating temperature	T_A	Range of ambient temperatures for normal logical operation.
Storage temperature	T_{stg}	Range of element temperatures which will not damage or reduce reliability in the state where neither voltage nor current is applied.

Table 1-2. Terminology for Recommended Operating Conditions

Item	Symbol	Definition
Power supply voltage	V_{DD}	Range of voltages for normal logical operation when V_{SS} = 0 V.
High-level input voltage	V_{IH}	For voltage applied to the input of PFESiP/V850EP1, this value indicates the voltage of the high-level state in which the input buffer operates normally. ● If voltage greater than the MIN. value is applied, the input voltage is assured to be high level.
Low-level input voltage	V_{IL}	For voltage applied to the input of the embedded array, this value indicates the voltage of the low-level state in which the input buffer operates normally. ● If a voltage less than the MAX. value is applied, the input voltage is assured to be low level.
Positive trigger voltage	V_P	Input level that inverts the output level when the input of PFESiP/V850EP1 is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Input level that inverts the output level when the input of PFESiP/V850EP1 is changed from the high-level side to the low-level side.
Hysteresis voltage	V_H	Difference between the positive- and negative-trigger voltage.
Input rise time	r_{ri}	Limit value for the rise time from 10% to 90% of the input voltage applied to the input of PFESiP/V850EP1.
Input fall time	t_{fi}	Limit value for the fall time from 90% to 10% of the input voltage applied to the input of PFESiP/V850EP1.

Table 1-3. Terminology for DC Characteristics

Item	Symbol	Definition
Static current consumption	I_{DDS}	In the state where there is no voltage change in the input and output pins, indicates the current that flows in from the power supply pin at the specified power supply voltage.
OFF state output current	I_{OZ}	For a 3-state output, this value indicates the current that flows through the output pin at the specified voltage when the output is at high impedance.
Output short-circuit current	I_{OS}	Current that flows out if the output pin is short-circuited to GND when output is at the high level.
Input leakage current	I_{LI}	Current that flows through the input pin when voltage is applied to the input pin.
Low-level output current	I_{OL}	Current that flows to the output pin at the specified low-level output voltage.
High-level output current	I_{OH}	Current that flows from the output pin at the specified high-level output voltage.
Low-level output voltage	V_{OL}	Output voltage when output is open in the low-level state.
High-level output voltage	V_{OH}	Output voltage when output is open in the high-level state.

1.2 Absolute Maximum Rating Value

Table 1-4. Absolute Maximum Rating Values

Item	Symbol	Definition	Item	Unit
Power supply voltage	V_{DD}	1.5 V system	−0.5 to +2.0	V
		3.3 V system	−0.5 to +4.6	V
Input/Output voltage	V_I /V_O	3.3 V buffer, V_I /V_O < V_{DD} + 0.5 V	−0.5 to +4.6	V
Output current (3.3 V buffer)	I_O	6 mA type (equivalent to TDOPAC33xx06)	21	mA
		9 mA type (equivalent to TDOPAC33xx09)	29	mA
		12 mA type (equivalent to TDOPAC33xx12)	45	mA
		18 mA type (equivalent to TDOPAC33xx18)	58	mA
Analog input voltage	V_{WASN}	ANI0 to ANI7 pins, AV_{DD} = 3.3 V ±0.3 V	−0.3 to AV_{DD}+0.3 Note	V
A/D converter reference input voltage	AV_{REFP}		−0.3 to AV_{DD}+0.3 Note	V
	AV_{REFM}		−0.3 to +0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 2.5 V or 3.3 V must be applied to the input pins only after applying the power supply voltage.

1.3 Recommended Operating Range

Table 1-5. Recommended Operating Range

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	1.5 V (IV_{DD}, AV_{DD1})	1.35	1.5	1.65	V
		3.3 V (EV_{DD}, AV_{DD2})	3.0	3.3	3.6	V
Negative trigger voltage	V_N	3.3 V buffer	0.6		1.8	V
Positive trigger voltage	V_P	3.3 V buffer	1.2		2.4	V
Hysteresis voltage	V_H	3.3 V buffer	0.3		1.5	V
Low-level input voltage	V_{IL}	3.3 V buffer	−0.5		0.8	V
High-level input voltage	V_{IH}	3.3 V buffer	2.0		V_{DD}	V
Input rise time / Input fall time	t_r		0		200	ns
	t_f		0		200	ns
Input rise time / Input fall time (Schmitt input)	t_r		0		10	ms
	t_f		0		10	ms
Operating ambient temperature	T_A		0		70	°C

1.4 DC Characteristics

Table 1-6. DC Characteristics (V_{DD} = 3.3 ±0.3 V, T_A = 0 to +70 °C)

Item		Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	Normal (200 MHz operation)	I_{DD1}				450	690	mA
			EV_{DD} pin			110	150	mA
	HALT	I_{DD2}				140	300	mA
	IDLE	I_{DD3}				10		mA
Output short-circuit current[Note 1]		I_{OS}	V_O = GND				−250	mA
Input leakage current (3.3 V buffer)		I_I	V_I = V_{DD} or GND	Normal input		$\pm10^{-1}$	±10	μA
			V_I = GND	With pull-up resistor(50 kΩ)	−37	−103	−253	μA
				With pull-up resistor(5 kΩ)	−305	−827	−1947	μA
			V_I = V_{DD}	With pull-down resistor(50 kΩ)	26	73	175	μA
Analog pin input leakage current		I_{LWASN}	ANI0 to ANI7				±10	μA
Low-level output current (3.3 V buffer)		I_{OL}	V_{OL} = 0.4 V	6 mA type(TDOPAC33xx06)	6.0			mA
				9 mA type(TDOPAC33xx09)	9.0			mA
				12 mA type(TDOPAC33xx12)	12.0			mA
				18 mA type(TDOPAC33xx18)	18.0			mA
High-level output current (3.3 V buffer)		I_{OH}	V_{OH} = 2.4 V	6 mA type(TDOPAC33xx06)	6.0			mA
				9 mA type(TDOPAC33xx09)	9.0			mA
				12 mA type(TDOPAC33xx12)	12.0			mA
				18 mA type(TDOPAC33xx18)	18.0			mA
Low-level output voltage		V_{OL}	I_{OL} = 0 mA	3.3 V buffer			0.1	V
High-level output voltage		V_{OH}	I_{OL} = 0 mA	3.3 V buffer	V_{DD} −0.1			V
Differential input sensitivity		V_{DI}	|(D+) - (D-)|	USB buffer	0.2			V
Common mode voltage range		V_{CM}	References to local GND	USB buffer	0.8		2.5	V
single-ended 0 reception Threshold		V_{SE}	**Note 2**	USB buffer	0.8		2.0	V
High-level output voltage		V_{OH}	R_L of 15 kΩ to GND	USB buffer	2.8		3.6	V
Low-level output voltage		V_{OL}	RL of 1.5 kΩ to 3.6 V	USB buffer	0		0.3	V
Data line Hi-Z leakage current		I_{LO}	0 V < V_{IN} < 3.3 V	USB buffer	−10		+10	μA
Input pin capacitance		C_{IN}	Pin to GND	USB buffer			20	pF

Notes 1. The output short-circuit time is 1 second or less per pin of the LSI.

2. V_{SE} represents the single-ended receiver input level and complies with LVTTL specification (V_{IL} = 0.8 V, V_{IH} = 2.0 V).

Remark The + and − signs of the current values in the table indicate the direction of the current. Current flowing into device is indicated by +; current flowing out is indicated by −.

1.5 Pull-up/Pull-down Resistance

Table 1-7. Pull-up/Pull-down Resistance (V_{DD} = 3.3 ± 0.3 V, T_A = 0 to +70 °C)

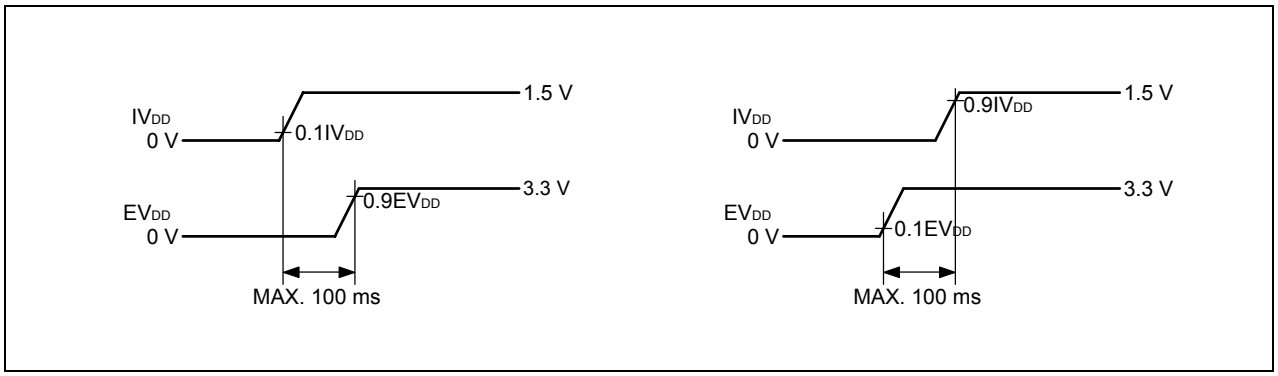
Item	Library Expression	MIN.	TYP.	MAX.	Unit
Pull-up resistor (3.3 V buffer)	5 kΩ	1.8	4.0	9.9	kΩ
	50 kΩ	14.2	31.9	80.7	kΩ
Pull-down resistor (3.3 V buffer)	50 kΩ	20.6	44.9	116.4	kΩ

1.6 Power Supply Application/Interruption Procedure

The PFESiP/V850EP1 has two power supply pins: a power supply pin for internal units (IV_{DD}) and a power supply pin for external pins (EV_{DD}). The I/O status of an alternate-function I/O pin may be undefined outside the range in which the operation is guaranteed.

(1) When turning on power

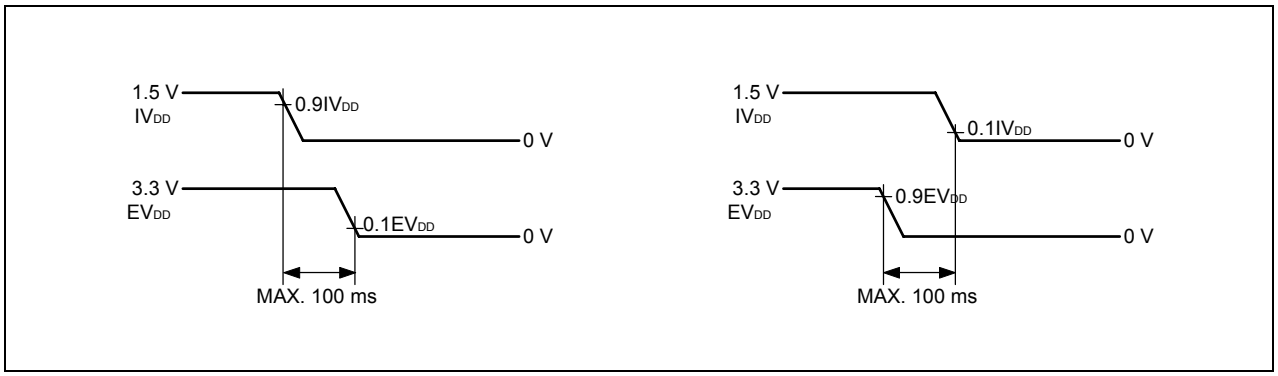
Set to no more than 100 ms the time from when the level of the power supply that starts first becomes $0.1V_{DD}$ until the level of the power supply that starts last becomes $0.9V_{DD}$.



When EV_{DD} (3.3 V) is started before IV_{DD} (1.5 V), the pin statuses become undefined until IV_{DD} (1.5 V) starts.

(2) When turning off power

Please ensure the time interval between "when the falling-edge level of the power supply that terminates first is $0.90 \times V_{DD}$" and "when the falling-edge level of the power supply that terminates last is $0.10 \times V_{DD}$" within 100 ms.



1.7 AC Characteristics

1.7.1 Clock pins

(1) Input clock

Table 1-8. Input Clock Timing

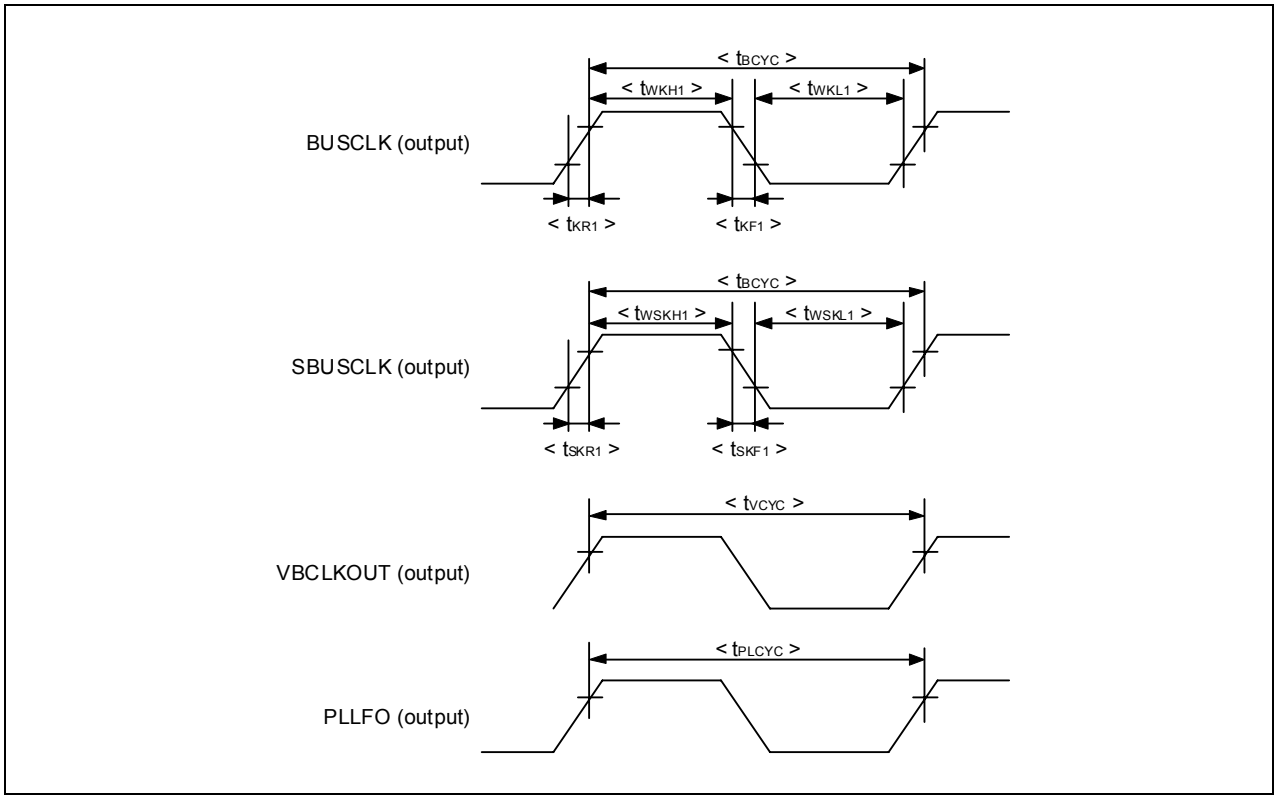
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{SCLK}		20.83	–	ns
PCLKIN input frequency	f_{SPCLK}		25	33	ns
DCK input cycle	t_{SDCK}		40	–	ns
<R> UCLK input frequency	f_{SUCLK}		48 -1500 ppm	48+1500 ppm	MHz
UCLK High-level width	t_{HWS}		8	–	ns
UCLK low-level width	t_{LWS}		8	–	ns

<R> **(2) Output clock**

Table 1-9. Output Clock Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
BUSCLK output cycle	t_{BCYC}	Output load capacitance: 30 pF and less	15	–	ns
BUSCLK high-level width	t_{WKH1}		0.5T–2.7	0.5T+2.7	ns
BUSCLK low-level width	t_{WKL1}		0.5T–2.7	0.5T+2.7	ns
BUSCLK rise time	t_{KR1}			3.3	ns
BUSCLK fall time	t_{KF1}			3.3	ns
SBUSCLK high-level width	t_{WSKH1}		0.5T–2.1	0.5T+2.1	ns
SBUSCLK low-level width	t_{WSKL1}		0.5T–2.1	0.5T+2.1	ns
SBUSCLK rise time	t_{SKR1}			1.85	ns
SBUSCLK fall time	t_{SKF1}			1.85	ns
VBCLKOUT output cycle	t_{VCYC}	Output load capacitance: 30 pF and less	10	–	ns
PLLFO output cycle	t_{PLCYC}	Output load capacitance: 20 pF and less	5	–	ns

Figure 1-1. Output Clock Timing



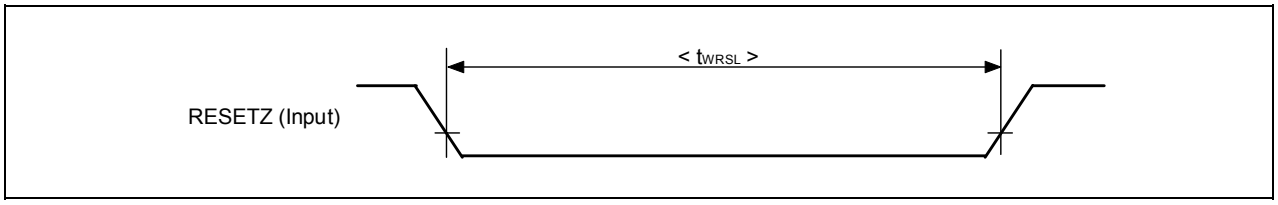
(3) Reset timing

Table 1-10. Reset Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RESET pin low-level width	t_{WRSL}		400		ns

Caution Sufficiently evaluate the oscillation stabilization time.

Figure 1-2. Reset Timing



1.7.2 Cautions on maximum operating frequency

The maximum operating frequency of PFESiP/V850EP1 varies depending on the operating conditions.

Furthermore, CPCLK, VBCLK, and BUSCLK are related as integral multiples, and VBCLK has an additional condition to be one-half or less than CPCLK. The combinations of clock settings are therefore restricted as follows.

Table 1-11. PFESiP/V850EP1 Maximum Operating Frequency on Operating Conditions

SDRAM, Low-speed Mask ROM	Priority clock	Clock		
		CPCLK	VBCLK	BUSCLK
None	CPCLK, VBCLK	200 MHz[Note]	100 MHz	100 MHz
Yes	CPCLK, VBCLK	200 MHz	100 MHz	50 MHz[Note]
	BUSCLK	200 MHz	66.6 MHz	66.6 MHz[Note]

Note This clock assigns the reference of the frequency.

Cautions 1. When performing SiP development by using the PFESiP/V850EP1, the design guarantee values of the PFESiP/V850EP1 may not be achieved, particularly for the maximum operation frequency, due to the SiP internal wiring and the load caused by external memories.

2. The electrical specifications of the external pins of the PFESiP/V850EP1 are calculated under fixed load conditions. In an application design using the PFESiP/V850EP1, these load conditions may be exceeded, depending on the configuration of external circuits. In such a case, the electrical specifications will be inferior to those of the PFESiP/V850EP1 by itself.

1.7.3 External memory interface pins

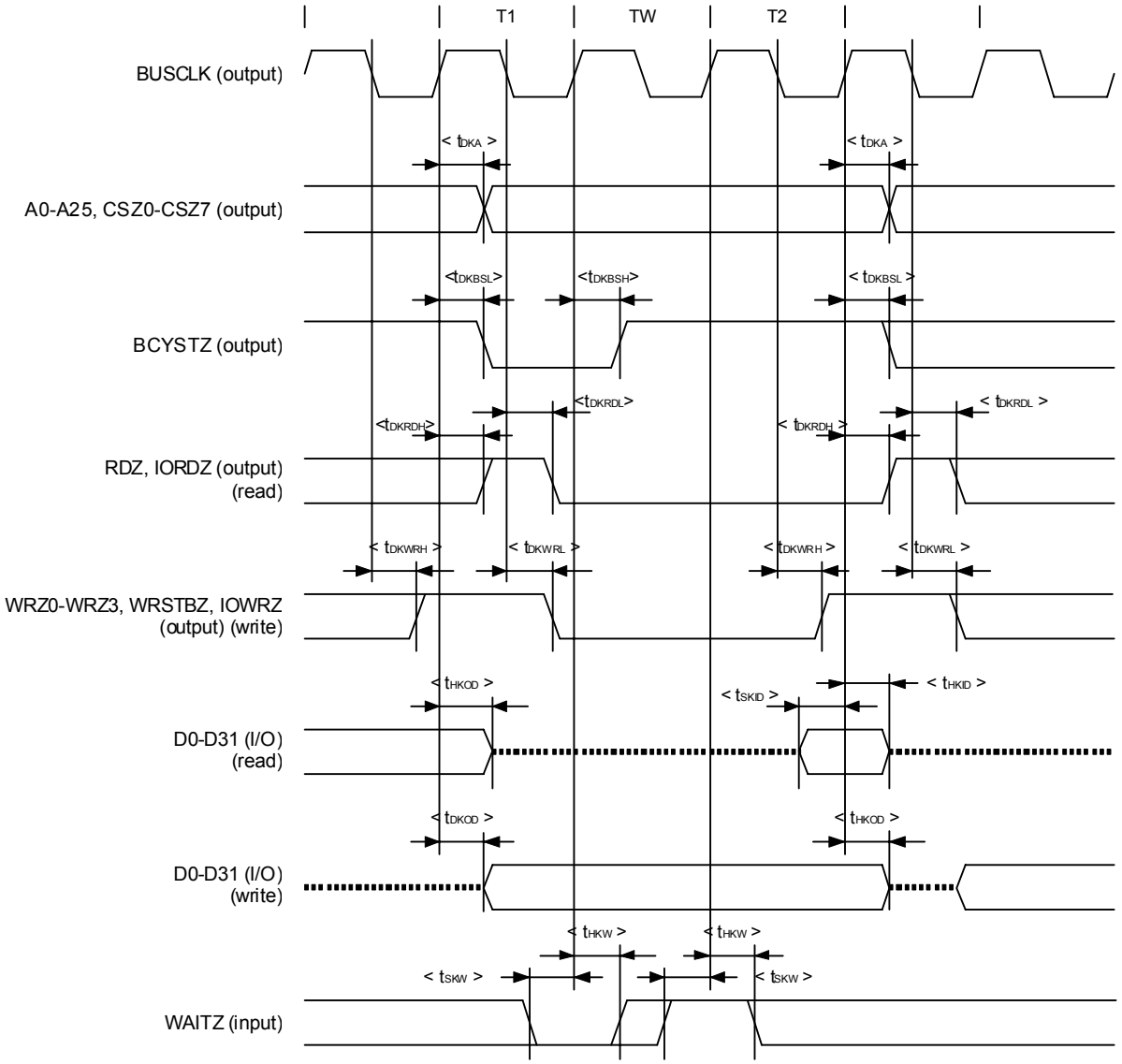
(1) Access Timing (SRAM, external ROM, external I/O)

Table 1-12. Access Timing (SRAM, External ROM, External I/O)

Parameter	Symbol	MIN.	MAX.	Unit
Address, CSZ0-CSZ7 output delay time (from BUSCLK↑)	t_{DKA}	1.5	11.0	ns
RDZ, IORDZ↓ delay time (from BUSCLK↓)	t_{DKRDL}	1.5	11.0	ns
RDZ, IORDZ↑ delay time (from BUSCLK↑)	t_{DKRDH}	1.5	11.0	ns
WRZ0-WRZ3, WRSTBZ, IOWRZ↓ (from BUSCLK↓)	t_{DKWRL}	1.5	11.0	ns
WRZ0-WRZ3, WRSTBZ, IOWRZ↑ (from BUSCLK↓)	t_{DKWRH}	1.5	11.0	ns
BCYSTZ↓ delay time (from BUSCLK ↑)	t_{DKBSL}	1.5	9.0	ns
BCYSTZ↑ delay time (from BUSCLK ↑)	t_{DKBSH}	1.5	9.0	ns
WAITZ setup time (to BUSCLK↑)	t_{SKW}	3.0	–	ns
WAITZ hold time (from BUSCLK↑)	t_{HKW}	1.0	–	ns
Data input setup time (to BUSCLK↑)	t_{SKID}	3.8	–	ns
Data input hold time (from BUSCLK↑)	t_{HKID}	1.0	–	ns
Data output delay time (from BUSCLK↑)	t_{DKOD}	1.5	11.0	ns
Data float delay time (from BUSCLK↑)	t_{HKOD}	1.5	11.0	ns

(a) Access timing (SRAM, external ROM, external I/O)

Figure 1-3. Access Timing (SRAM, External ROM, External I/O)

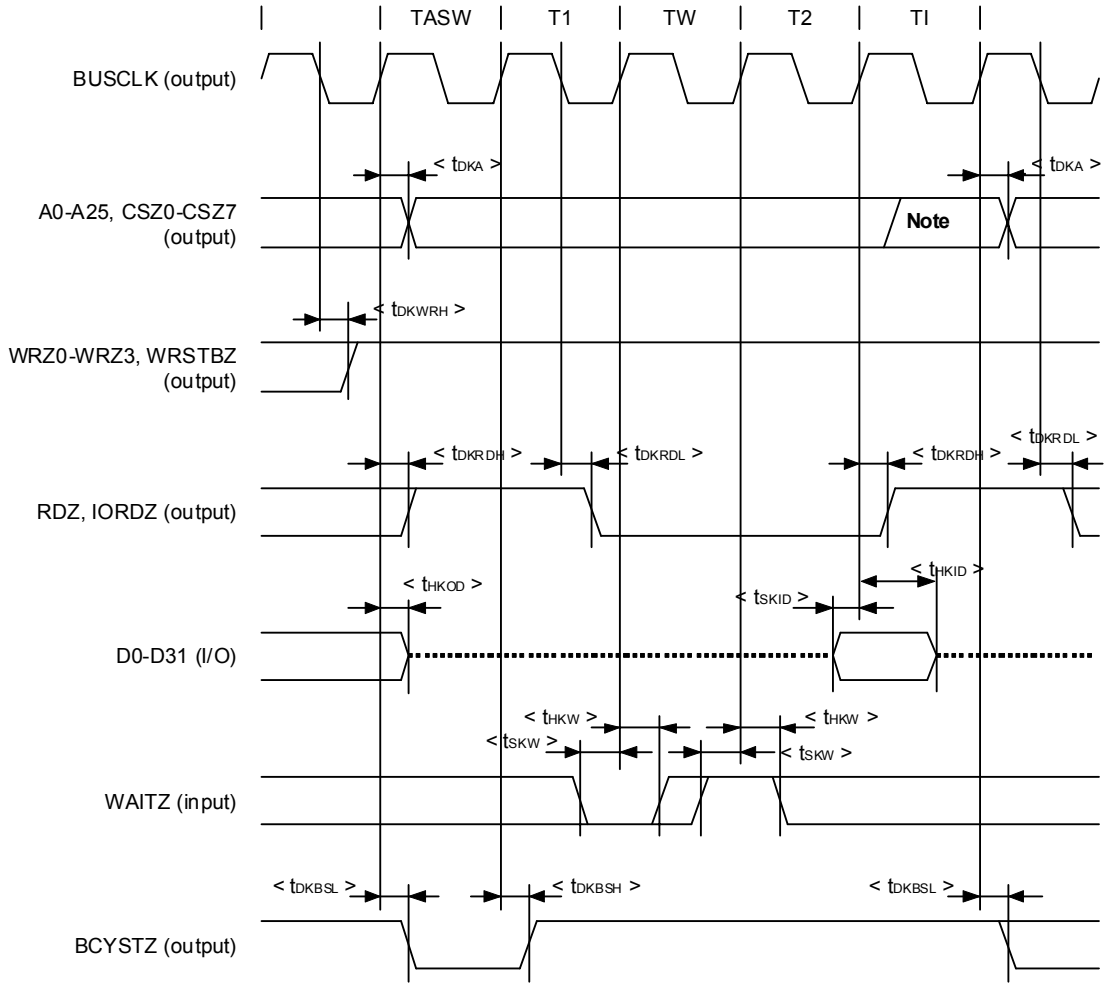


Remarks 1. Timing when the number of waits set by the DWC0 and DWC1 registers is 0.

2. Broken lines indicate high impedance.

(b) Read timing (SRAM, external ROM, external I/O)

Figure 1-4. Read Timing (SRAM, External ROM, External I/O)



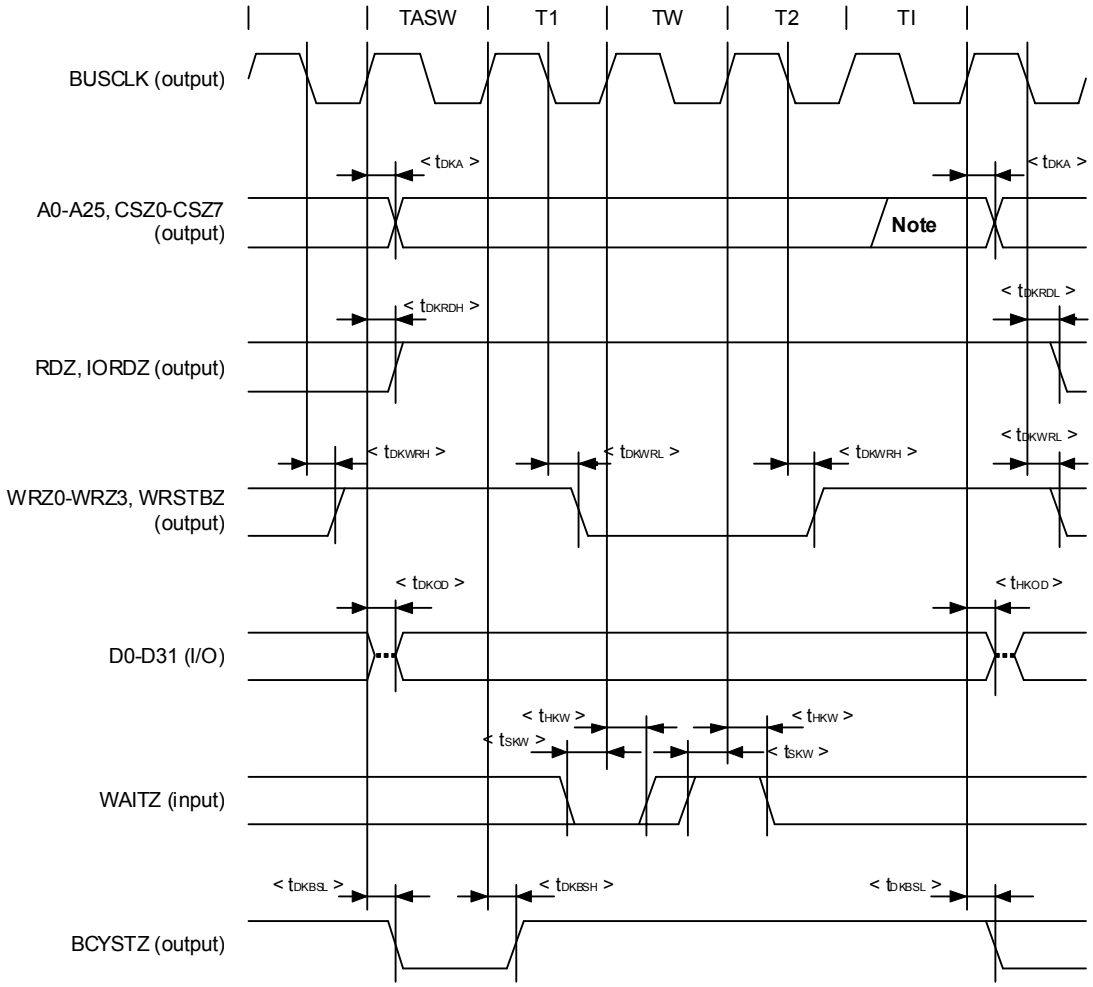
Note In the case of CSZ0-CSZ7

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(c) Write timing (SRAM, external ROM, external I/O)

Figure 1-5. Write Timing (SRAM, External ROM, External I/O)



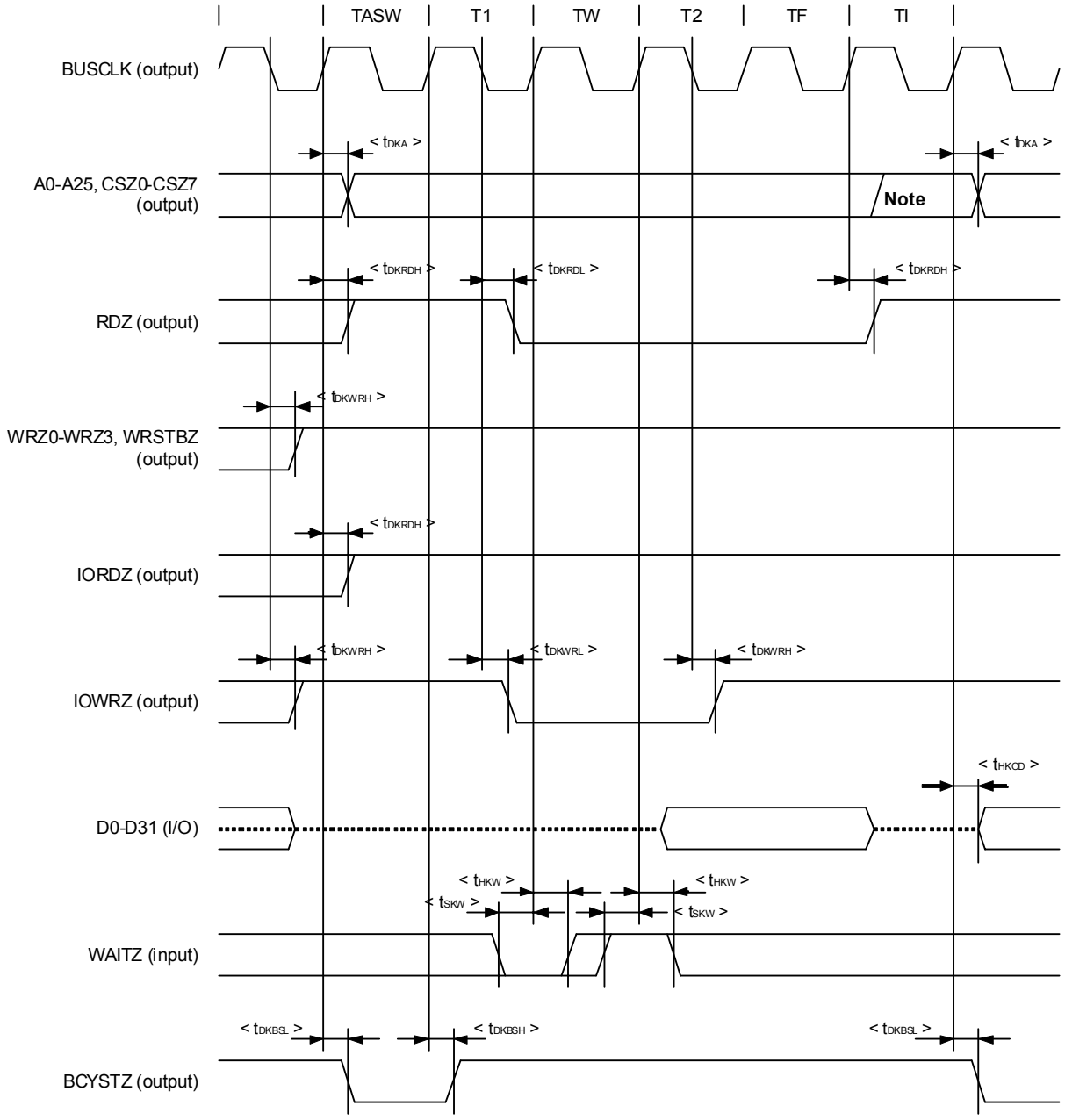
Note In the case of CSZ0-CSZ7

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(d) DMA flyby transfer timing (SRAM → external I/O)

Figure 1-6. DMA Flyby Transfer Timing (SRAM → External I/O)



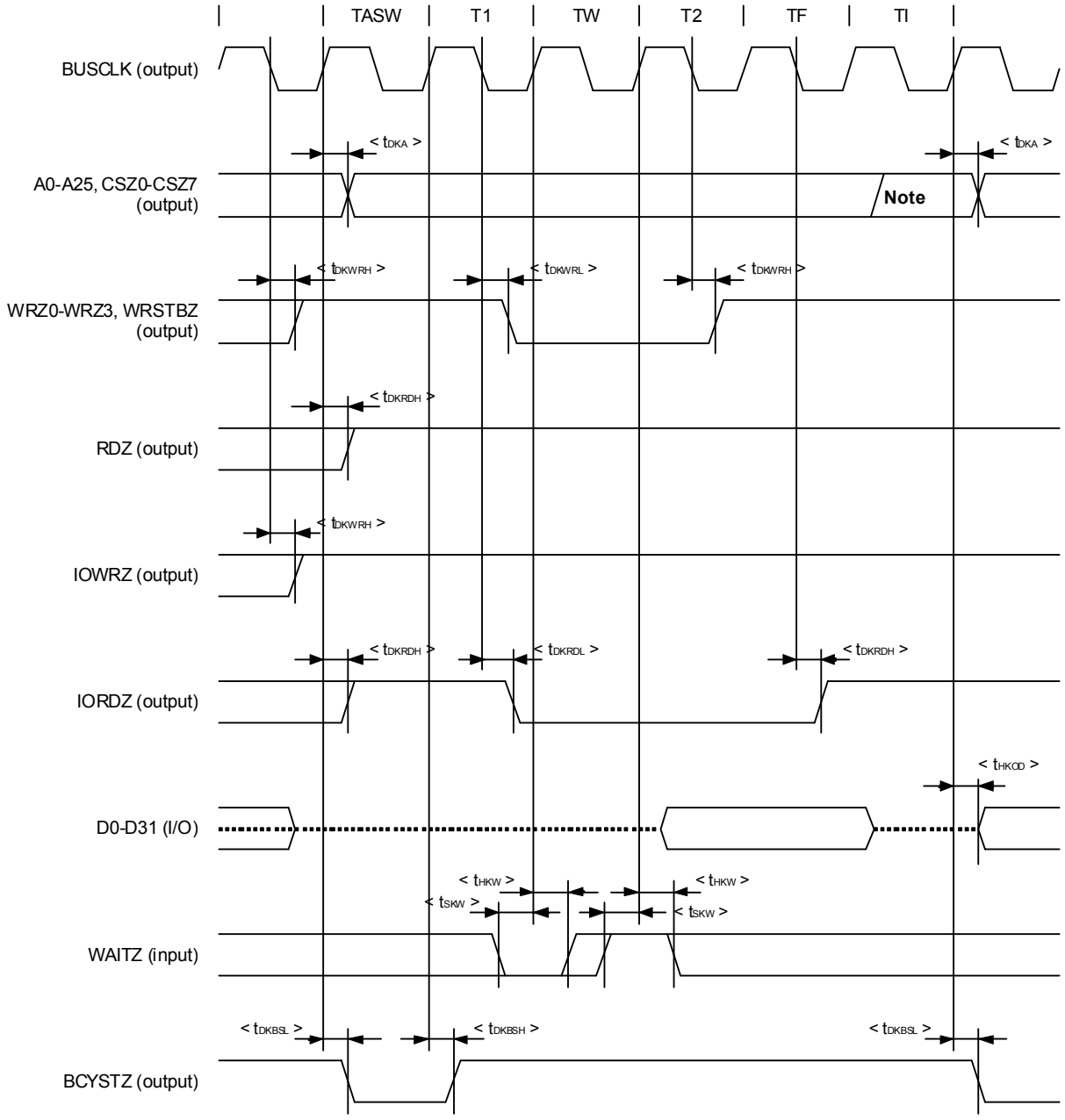
Note In the case of CSZ0-CSZ7

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance

(e) DMA flyby transfer timing (external I/O→SRAM transfer)

Figure 1-7. DMA Flyby Transfer Timing (External I/O → SRAM Transfer)



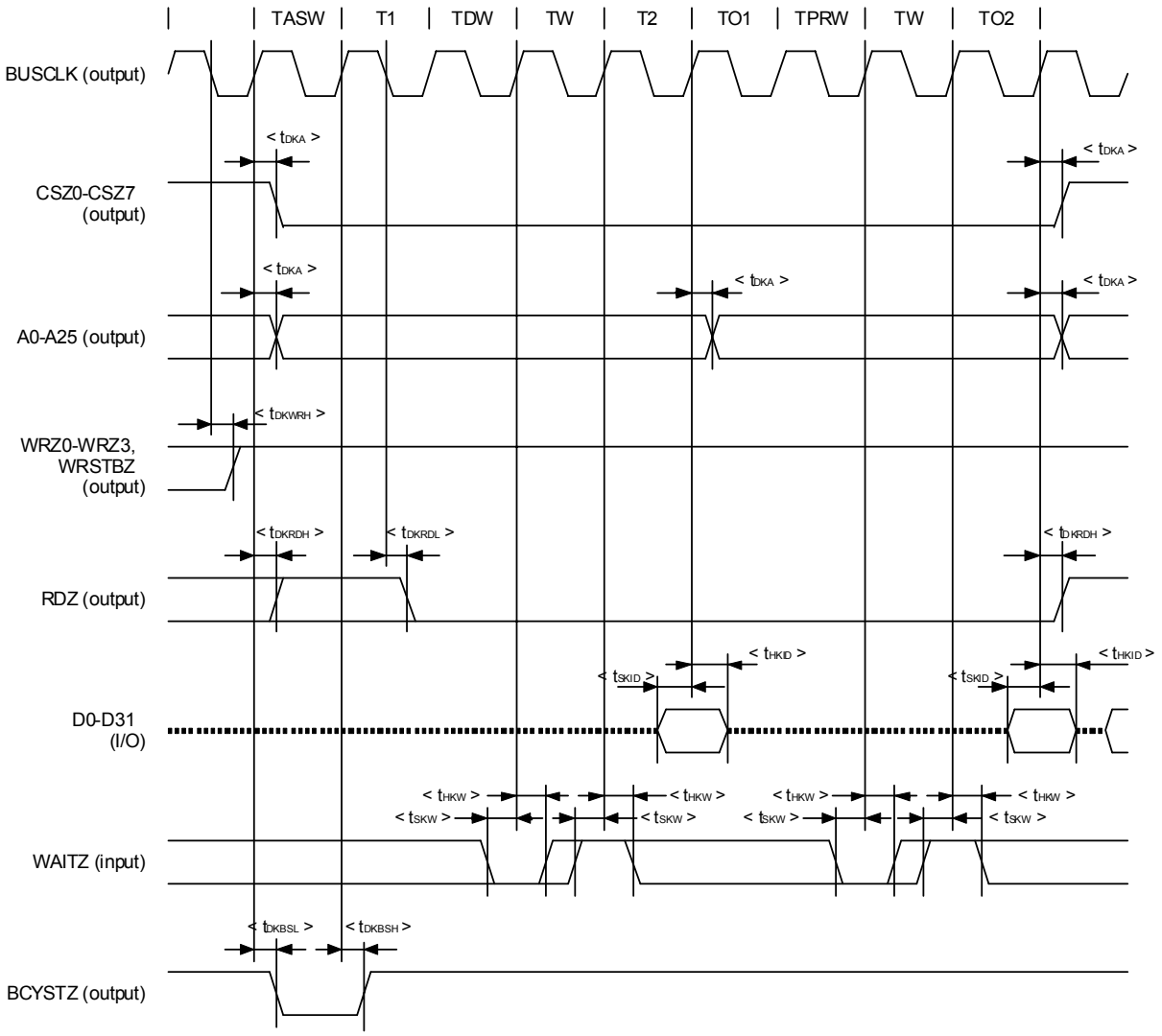
Note In the case of CSZ0-CSZ7

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(f) Page ROM access timing

Figure 1-8. Page ROM Access Timing



Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(2) SDRAM access timing

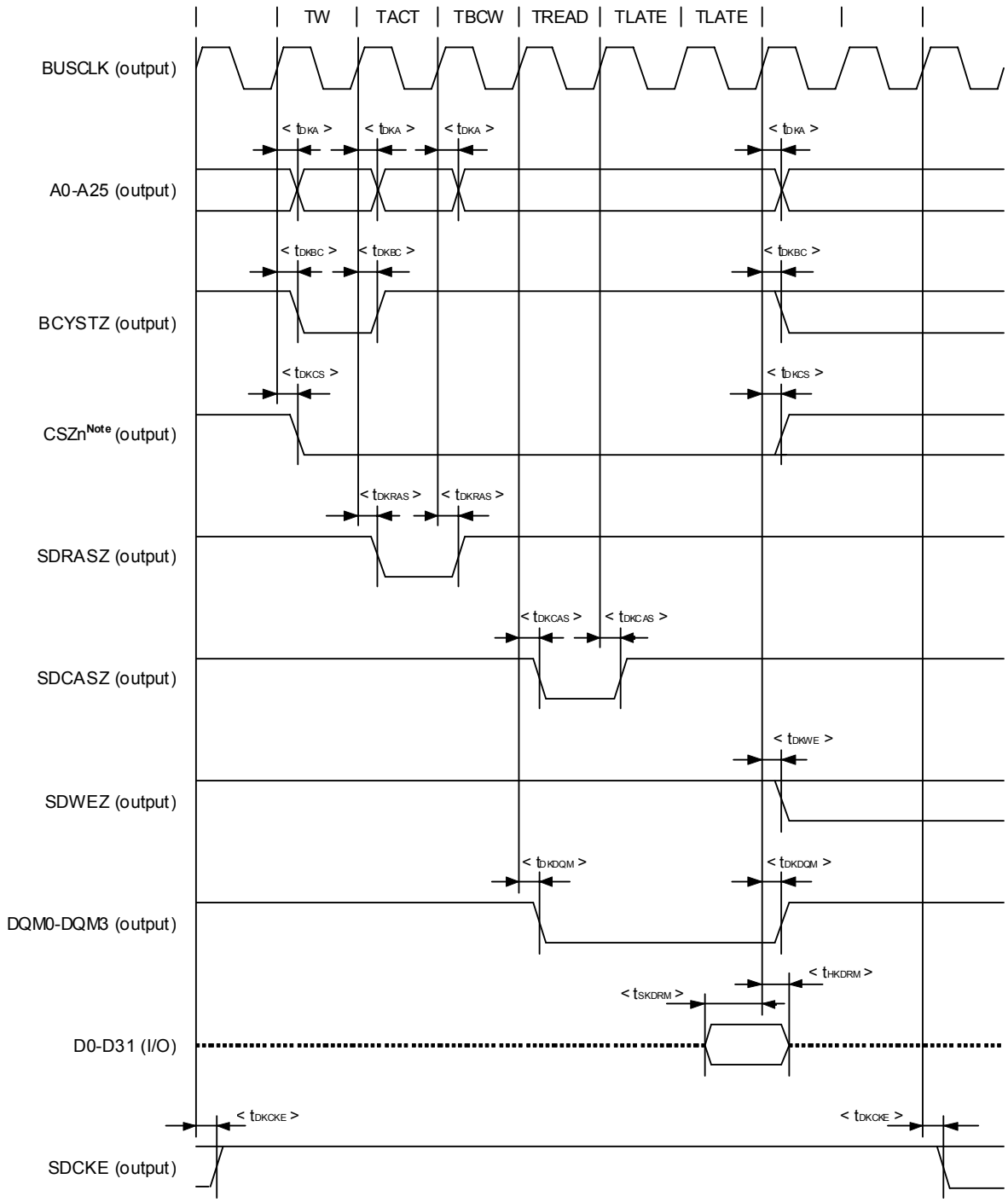
Table 1-13. SDRAM Access Timing

Parameter	Symbol	MIN.	MAX.	Unit
Address delay time (from BUSCLK↑)	t_{DKA}	1.5	11.0	ns
BCYSTZ delay time (from BUSCLK↑)	t_{DKBC}	1.5	9.0	ns
CSZn[Note] delay time (from BUSCLK↑)	t_{DKCS}	1.5	11.0	ns
SDRASZ delay time (from BUSCLK↑)	t_{DKRAS}	1.5	11.0	ns
SDCASZ delay time (from BUSCLK↑)	t_{DKCAS}	1.5	11.0	ns
SDWEZ delay time (from BUSCLK↑)	t_{DKWE}	1.5	11.0	ns
DQM0-DQM3 delay time (from BUSCLK↑)	t_{DKDQM}	1.5	11.0	ns
SDCKE delay time (from BUSCLK↑)	t_{DKCKE}	1.5	11.0	ns
Data input setup time (SDRAM read, from BUSCLK↑)	t_{SKDRM}	3.8	–	ns
Data input hold time (SDRAM read, from BUSCLK↑)	t_{HKDRM}	1.0	–	ns
Data output delay time (from BUSCLK↑)	t_{DKDT1}	1.5	11.0	ns
	t_{DKDT2}	1.5	11.0	ns
Data float delay time (from BUSCLK↑)	t_{HZKDT}	1.5	11.0	ns
REFRQZ time (from BUSCLK↑)	t_{DKREF}	1.5	11.0	ns

Note n = 1, 3, 4, 6

(a) Read timing (SDRAM access)

Figure 1-9. Read Timing (SDRAM Access)



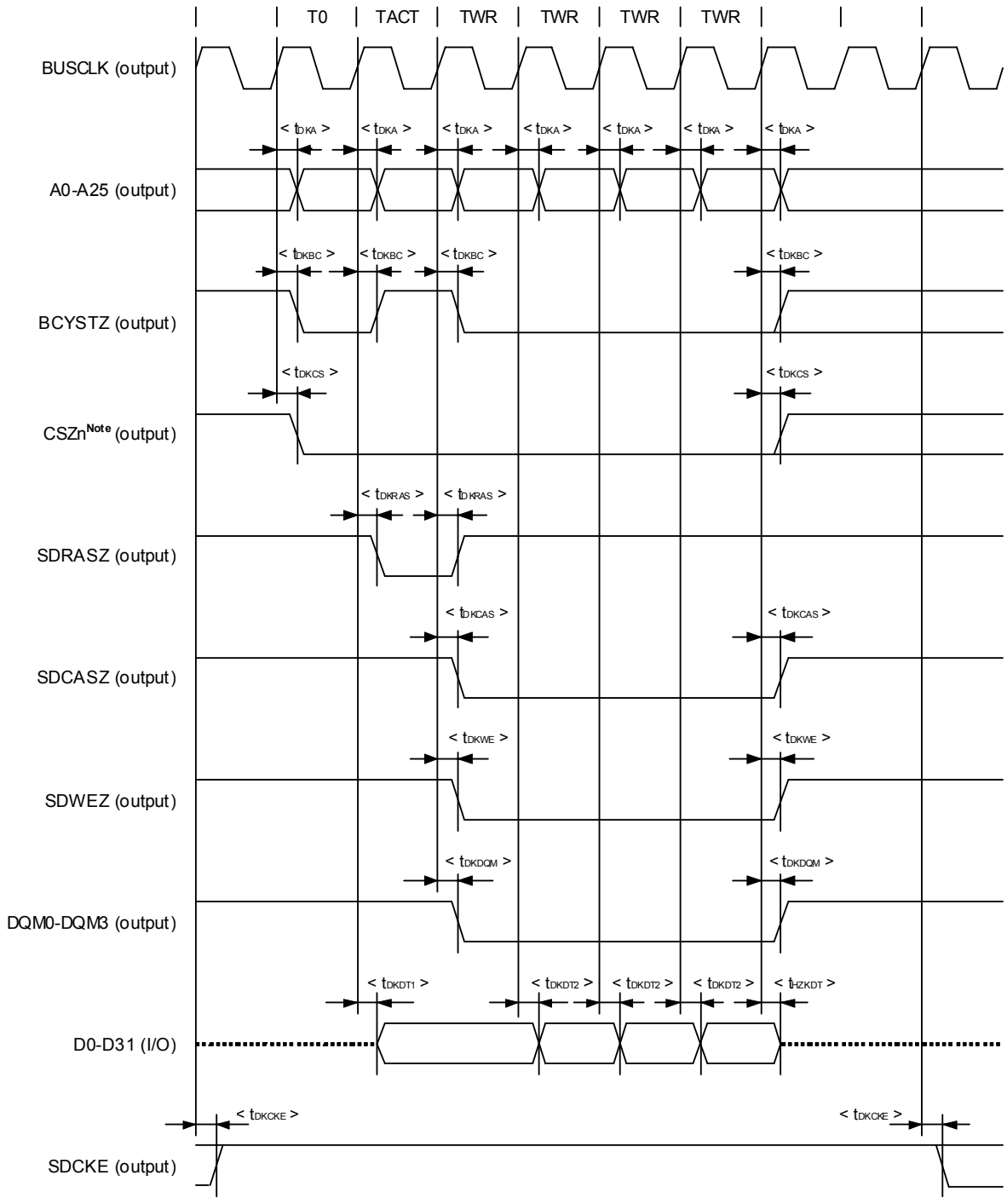
Note n = 1, 3, 4, 6

Remarks 1. Number of waits inserted by BCW1n and BCW0n bits of the SCRn register (TBCW)

2. Broken lines indicate high impedance.

(b) Write timing (SDRAM access)

Figure 1-10. Write Timing (SDRAM Access)

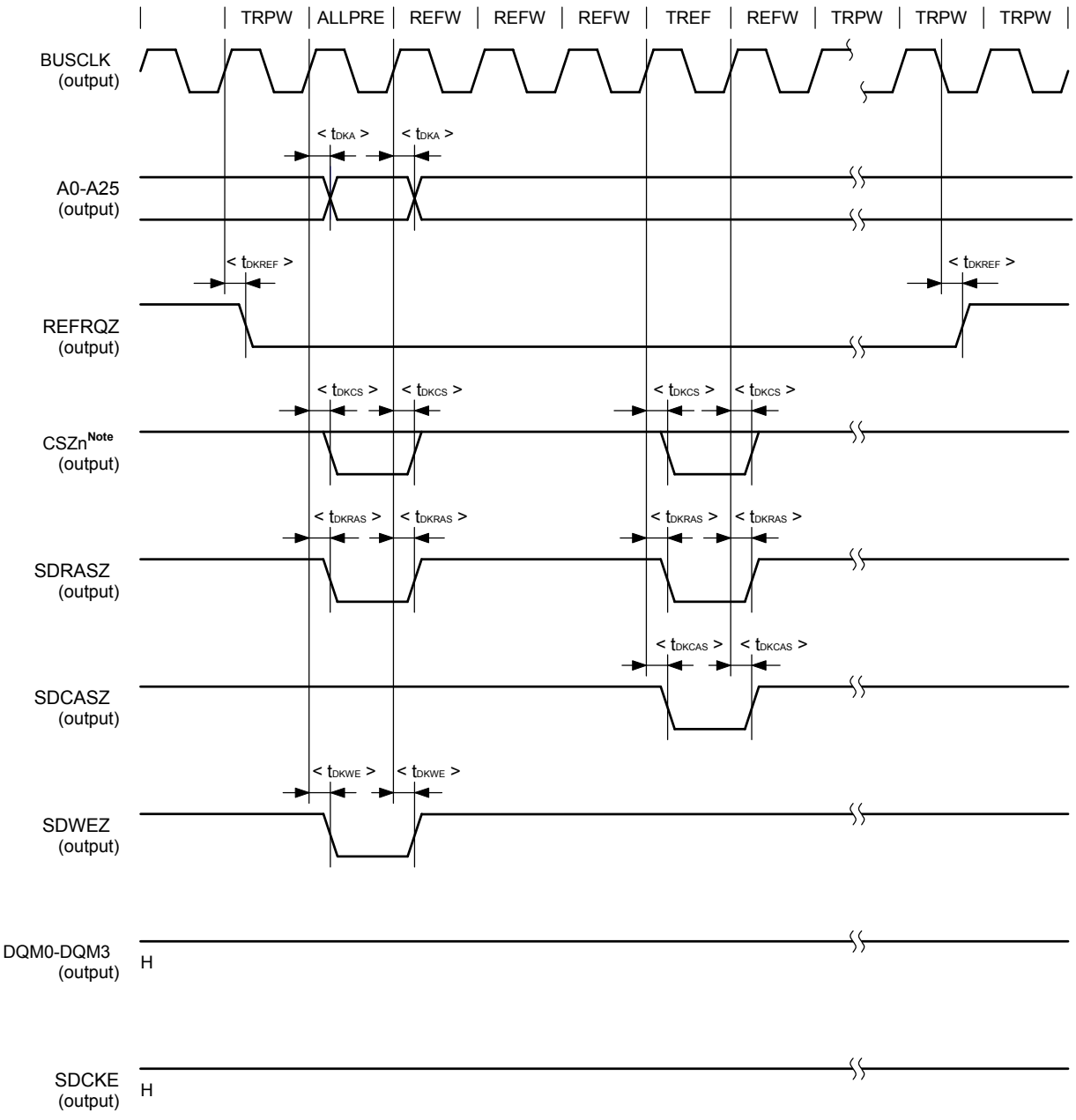


Note n = 1, 3, 4, 6

Remarks Broken lines indicate high impedance.

(c) Refresh Timing (SDRAM access)

Figure 1-11. Refresh Timing (SDRAM Access)



Note n = 1, 3, 4, 6

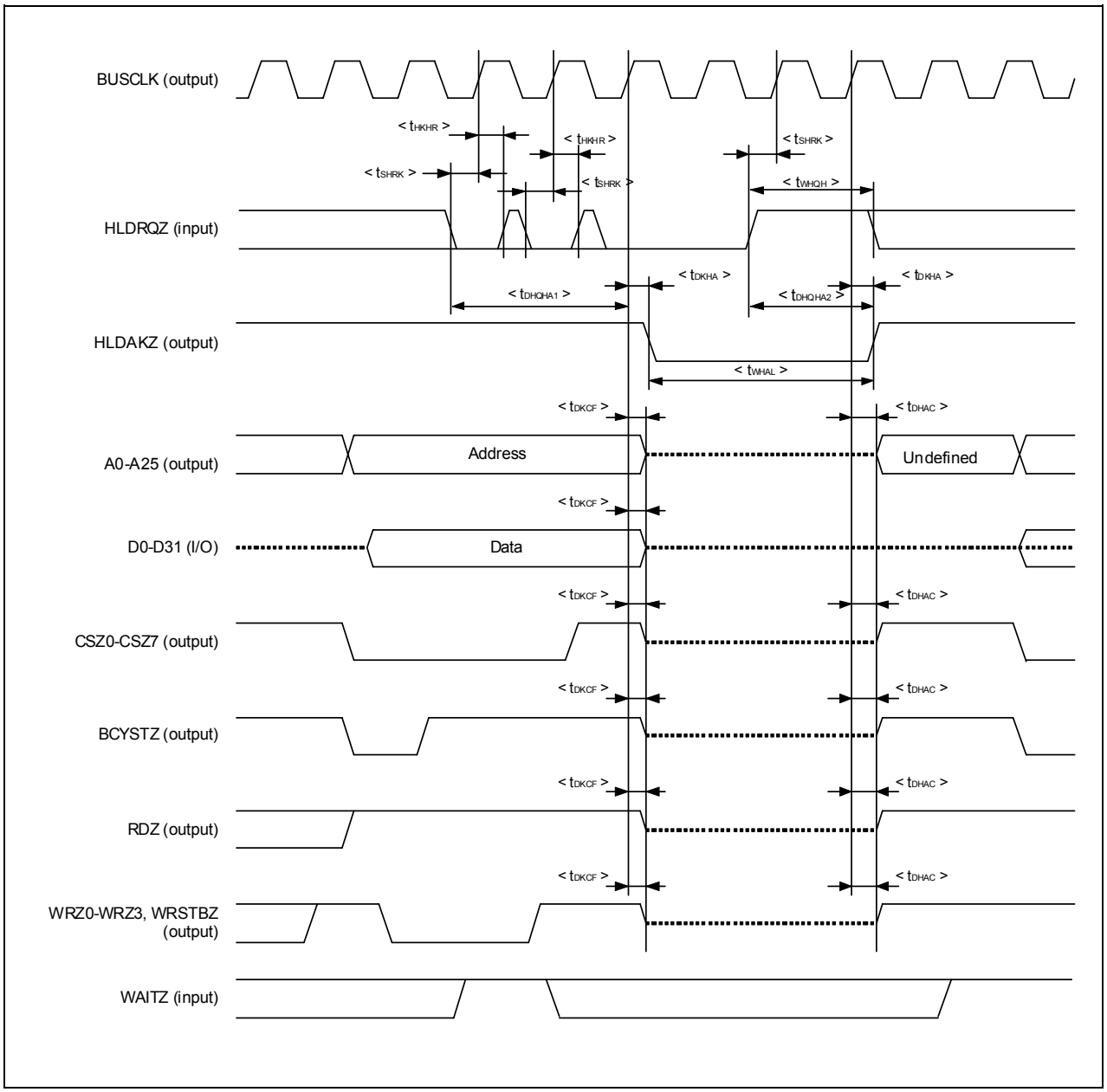
(3) Bus hold timing

Table 1-14. Bus Hold Timing

Parameter	Symbol	MIN.	MAX.	Unit
HLDRQZ setup time (to BUSCLK↑)	t_{SHRK}	3.8	–	ns
HLDRQZ hold time (from BUSCLK↑)	t_{HKHR}	2.0	–	ns
Delay time from BUSCLK↑ to HLDAKZ	t_{DKHA}	1.5	11.0	ns
HLDRQZ high-level width	t_{WHQH}	5.8 + t_{BCLK}	–	ns
HLDAKZ low-level width	t_{WHAL}	–9.5 + t_{BCLK}	–	ns
Delay time from BUSCLK↑ to bus float	t_{DKCF}	1.5	–	ns
Delay time from BUSCLK↑ to bus output	t_{DHAC}	1.5	13.0	ns
Delay time from HLDRQZ↓ to HLDAKZ↓	t_{DHQHA1}	1.5 × t_{BCLK}	–	ns
Delay time from HLDRQZ↑ to HLDAKZ↑	t_{DHQHA2}	0.5 × t_{BCLK}	3 × t_{BCLK} + 3.8	ns

Remark t_{BCLK}: BUSCLK cycle

Figure 1-12. Bus Hold Timing



1.7.4 SiP internal-connection bus interface pins

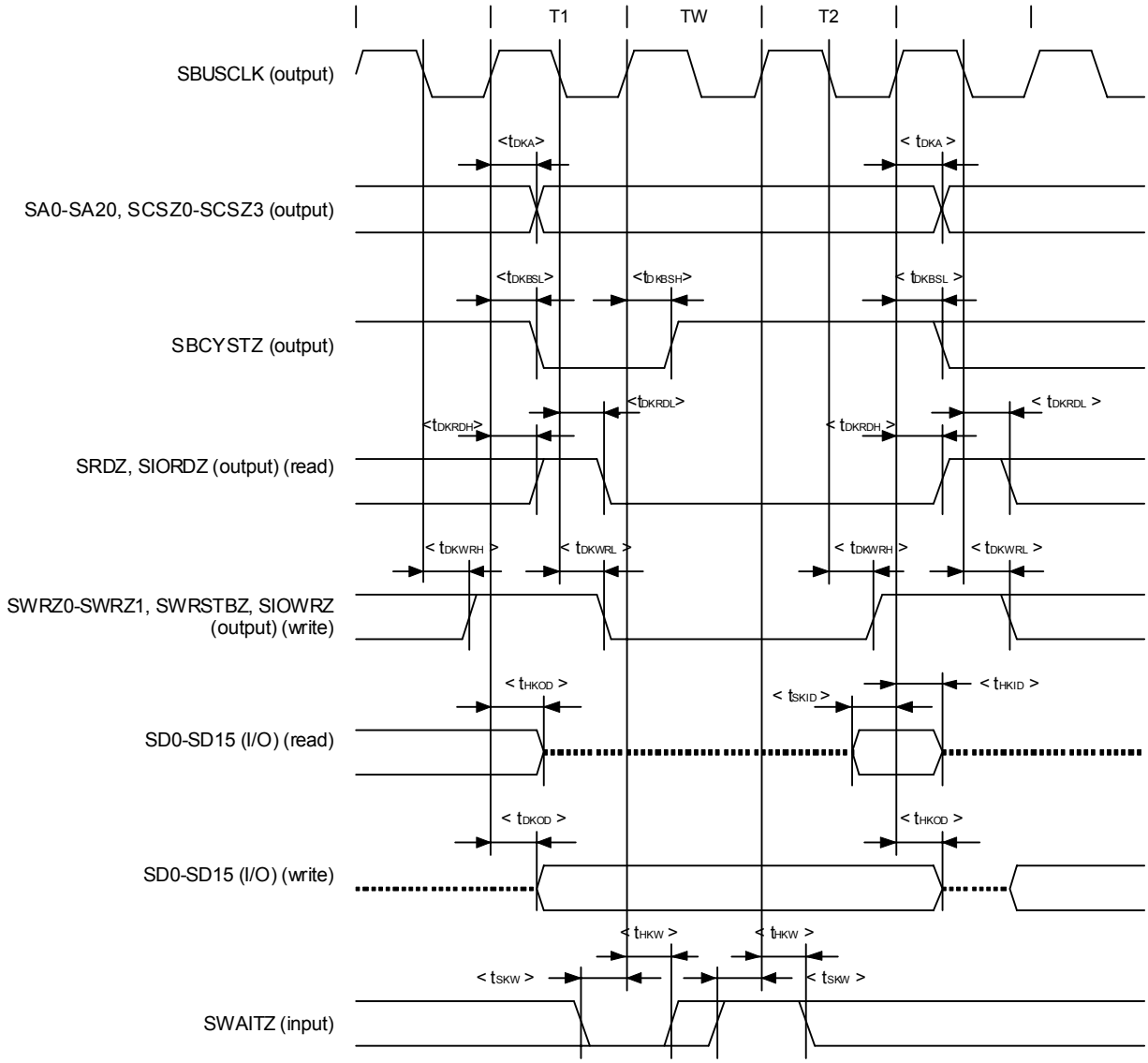
(1) Access timing (SRAM, external ROM, external I/O)

Table 1-15. Access Timing (SRAM, External ROM, External I/O)

Parameter	Symbol	MIN.	MAX.	Unit
Address, SCSZ0-SCSZ3 output delay time (from SBUSCLK↑)	t_{DKA}	1.5	11.0	ns
SRDZ, SIORDZ↓ delay time (from SBUSCLK↓)	t_{DKRDL}	1.5	11.0	ns
SRDZ, SIORDZ↑ delay time (from SBUSCLK↑)	t_{DKRDH}	1.5	11.0	ns
SWRZ0 to SWRZ1, SWRSTBZ, SIOWRZ↓ (from SBUSCLK↓)	t_{DKWRL}	1.5	11.0	ns
SWRZ0 to SWRZ1, SWRSTBZ, SIOWRZ↑ (from SBUSCLK↓)	t_{DKWRH}	1.5	11.0	ns
SBCYSTZ↓ delay time (from SBUSCLK↑)	t_{DKBSL}	1.5	8.0	ns
SBCYSTZ↑ delay time (from SBUSCLK↑)	t_{DKBSH}	1.5	8.0	ns
SWAITZ setup time (to SBUSCLK↑)	t_{SKW}	3.0	–	ns
SWAITZ hold time (from SBUSCLK↑)	t_{HKW}	1.0	–	ns
Data input setup time (to SBUSCLK↑)	t_{SKID}	3.0	–	ns
Data input hold time (from SBUSCLK↑)	t_{HKID}	2.0	–	ns
Data output delay time (from SBUSCLK↑)	t_{DKOD}	1.5	11.0	ns
Data float delay time (from SBUSCLK↑)	t_{HKOD}	1.5	11.0	ns

(a) Base access timing (SRAM, external ROM, external I/O)

Figure 1-13. Base Access Timing (SRAM, External ROM, External I/O)

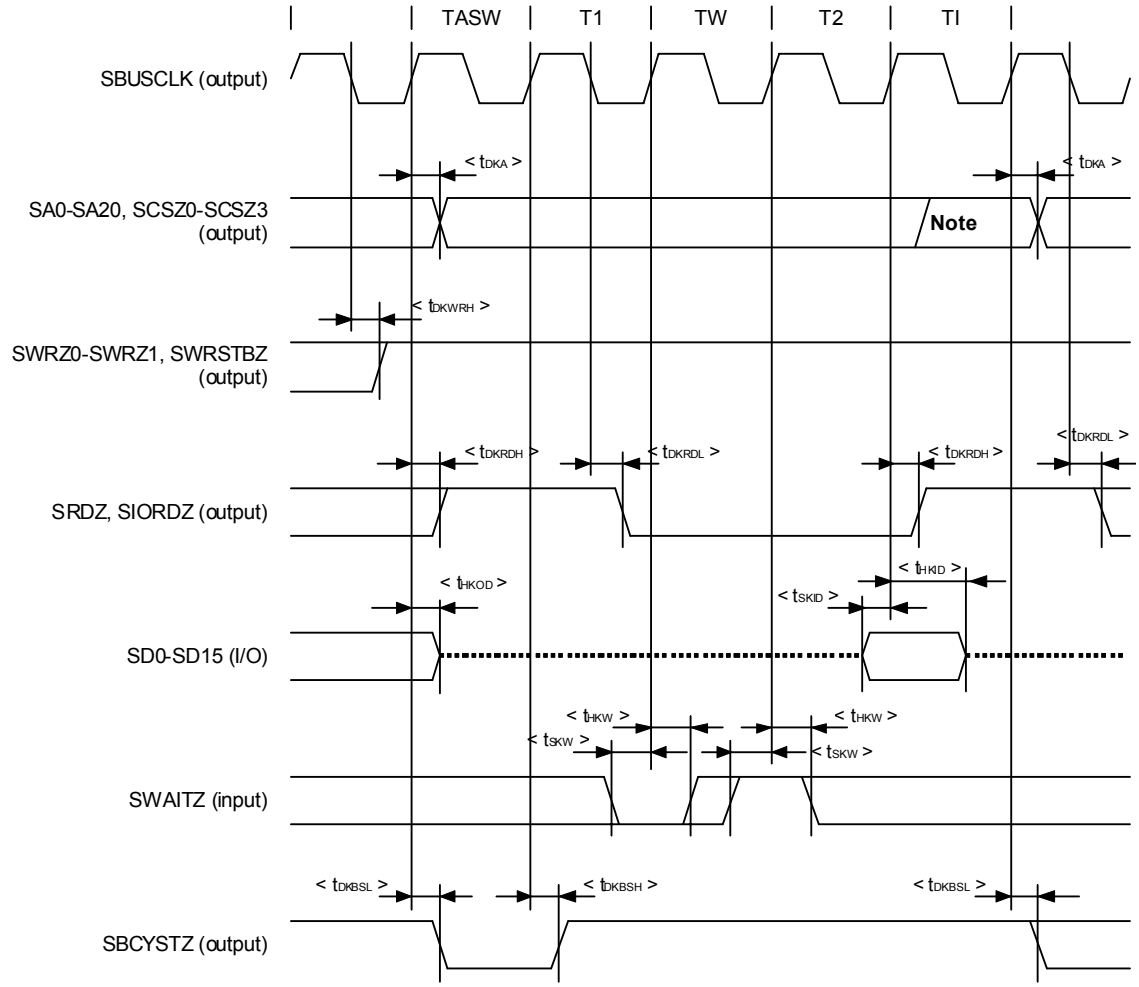


Remarks 1. Timing when the number of waits set by the DWC0 and DWC1 registers is 0.

2. Broken lines indicate high impedance.

(b) Read timing (SRAM, external ROM, external I/O)

Figure 1-14. Read Timing (SRAM, External ROM, External I/O)



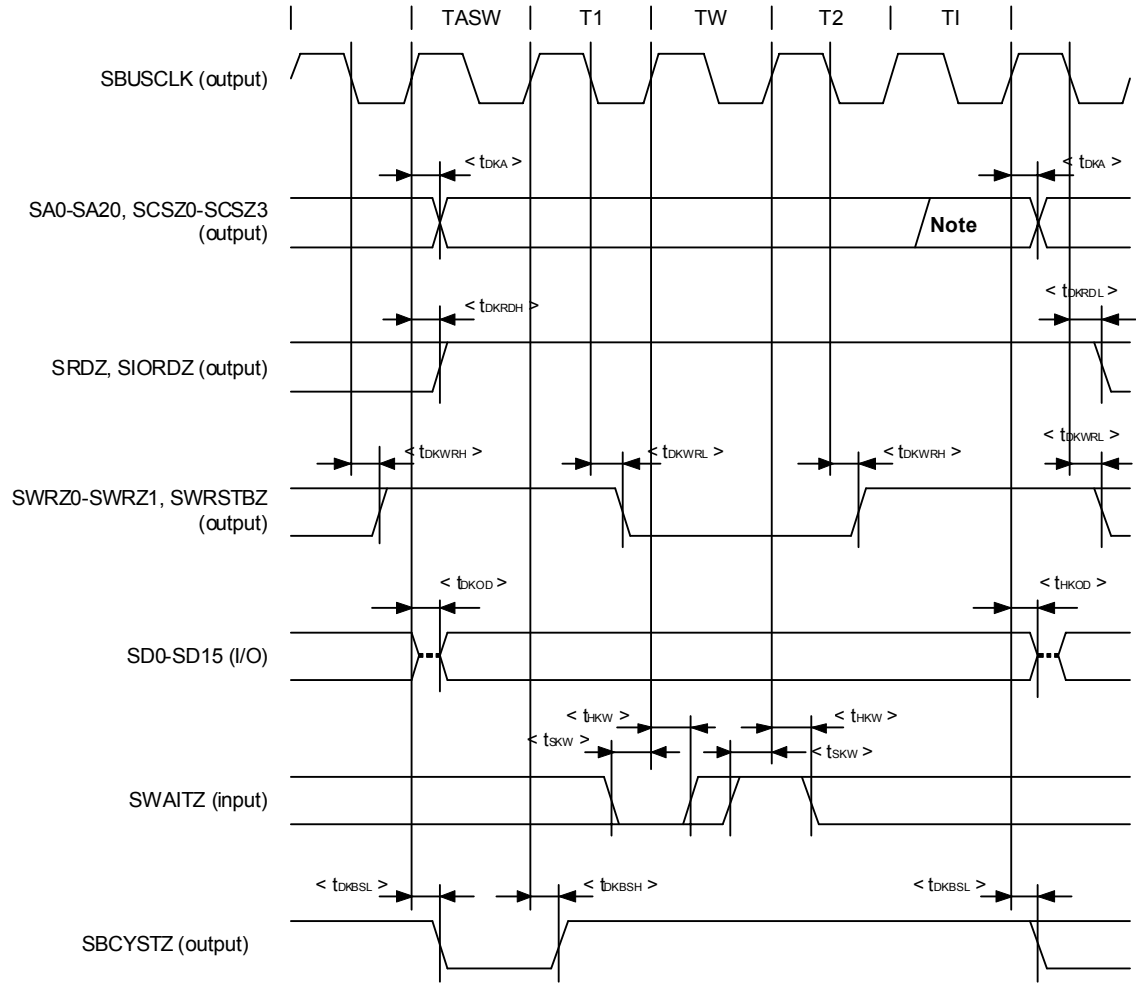
Note In the case of SCSZ0-SCSZ3

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(c) Write timing (SRAM, external ROM, external I/O)

Figure 1-15. Write Timing (SRAM, External ROM, External I/O)



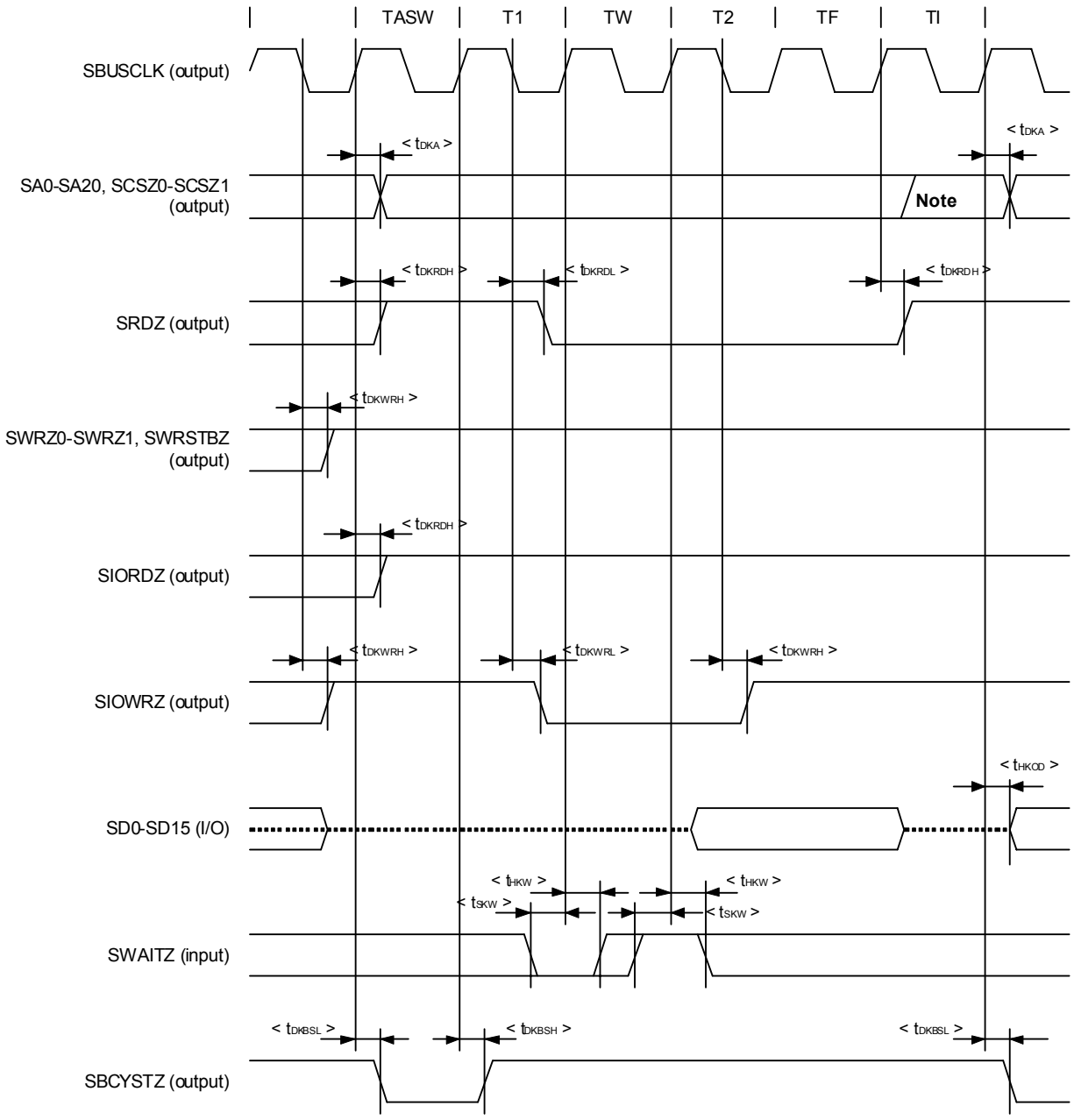
Note In the case of SCSZ0-SCSZ3

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(d) DMA flyby transfer timing (SRAM → external I/O)

Figure 1-16. DMA Flyby Transfer Timing (SRAM → External I/O)



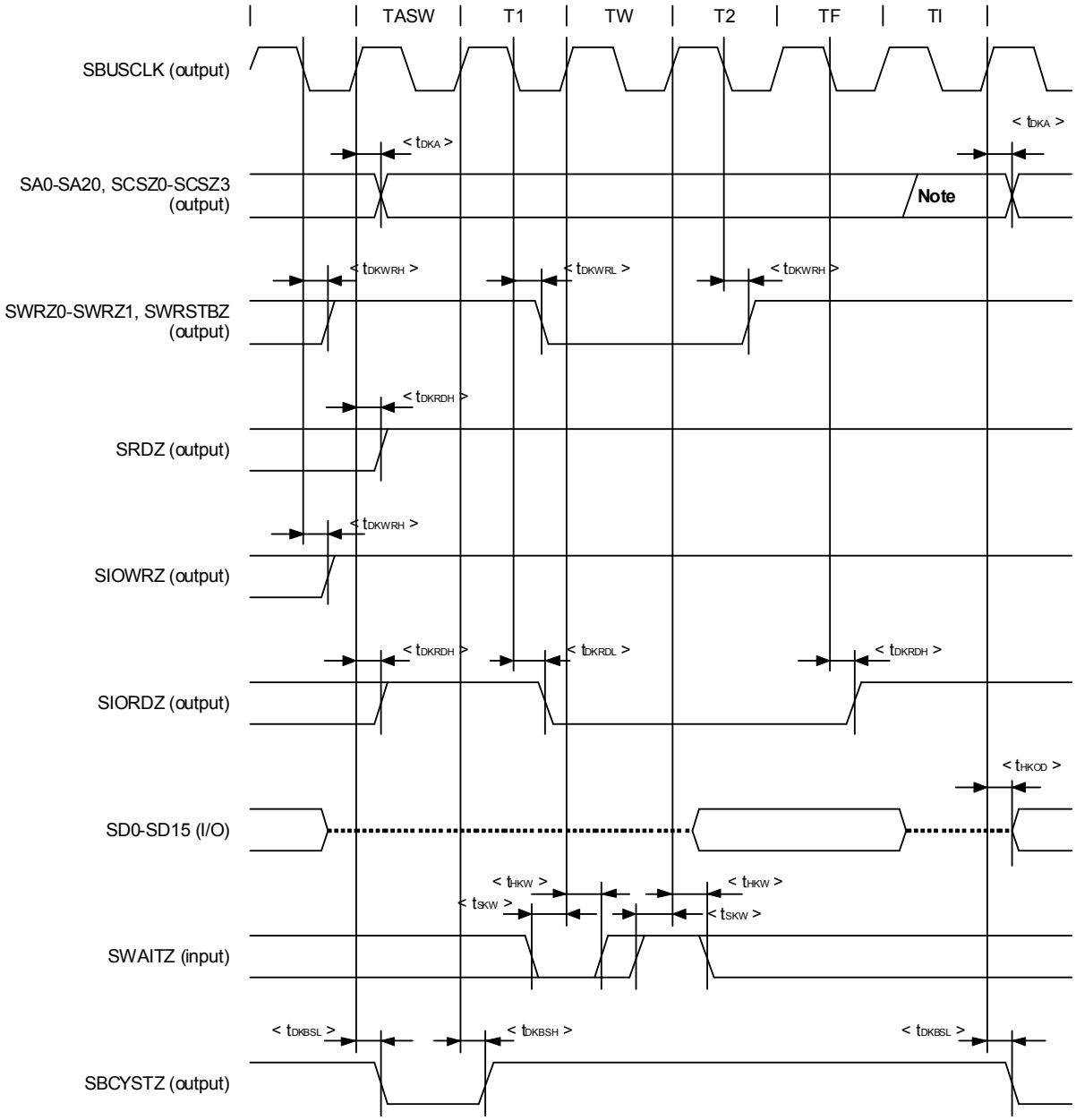
Note In the case of SCSZ0-SCSZ3

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(e) DMA flyby transfer timing (external I/O → SRAM transfer)

Figure 1-17. DMA Flyby Transfer Timing (External I/O → SRAM Transfer)



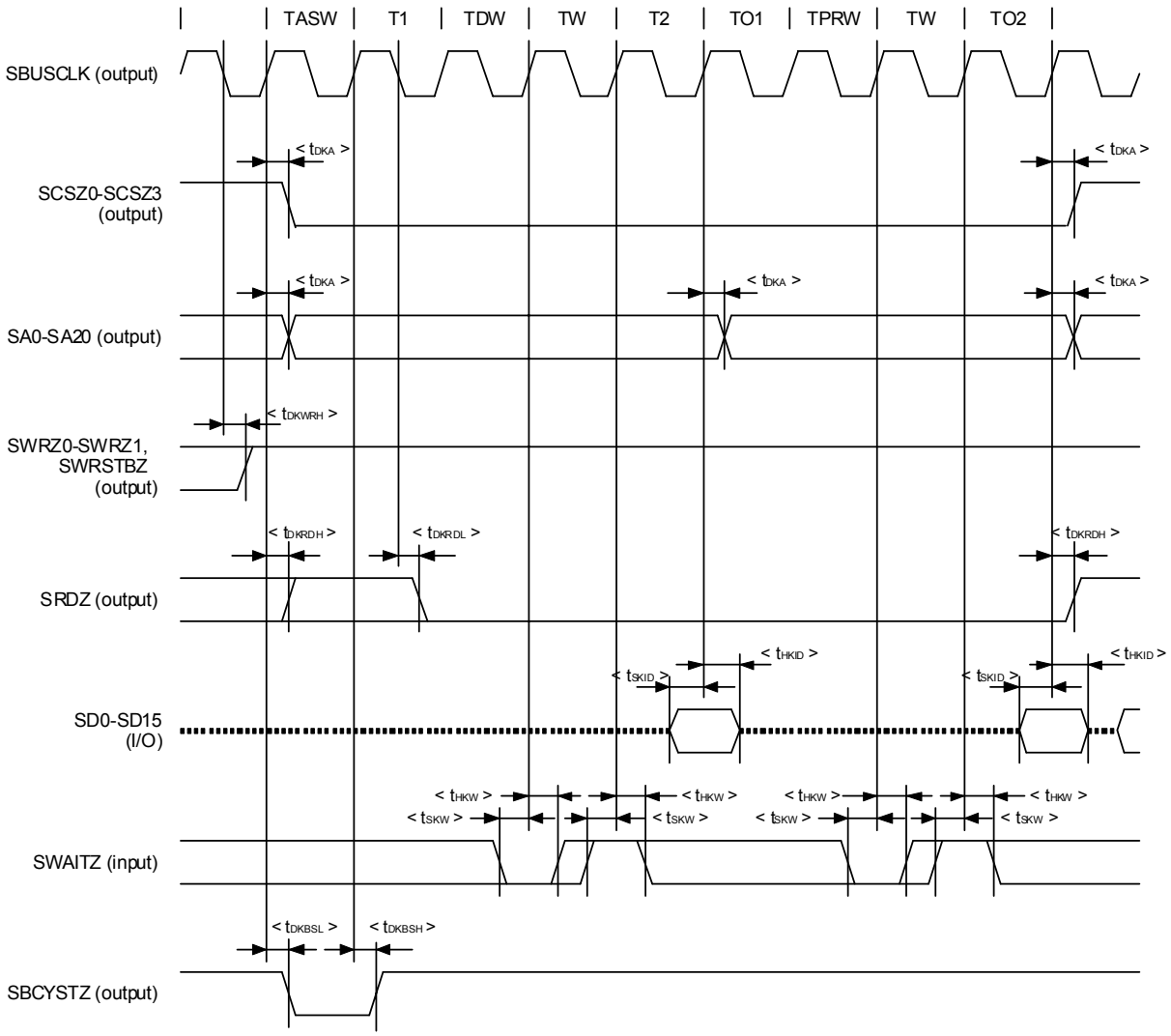
Note In the case of SCSZ0-SCSZ3

Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

(f) Page ROM access timing

Figure 1-18. Page ROM Access Timing



Remarks 1. Timing when the number of waits inserted by the DWC0 or DWC1 register is 0, the number of idle states inserted by the BCC register is 1, and the number of waits inserted by the ASC register is 1.

2. Broken lines indicate high impedance.

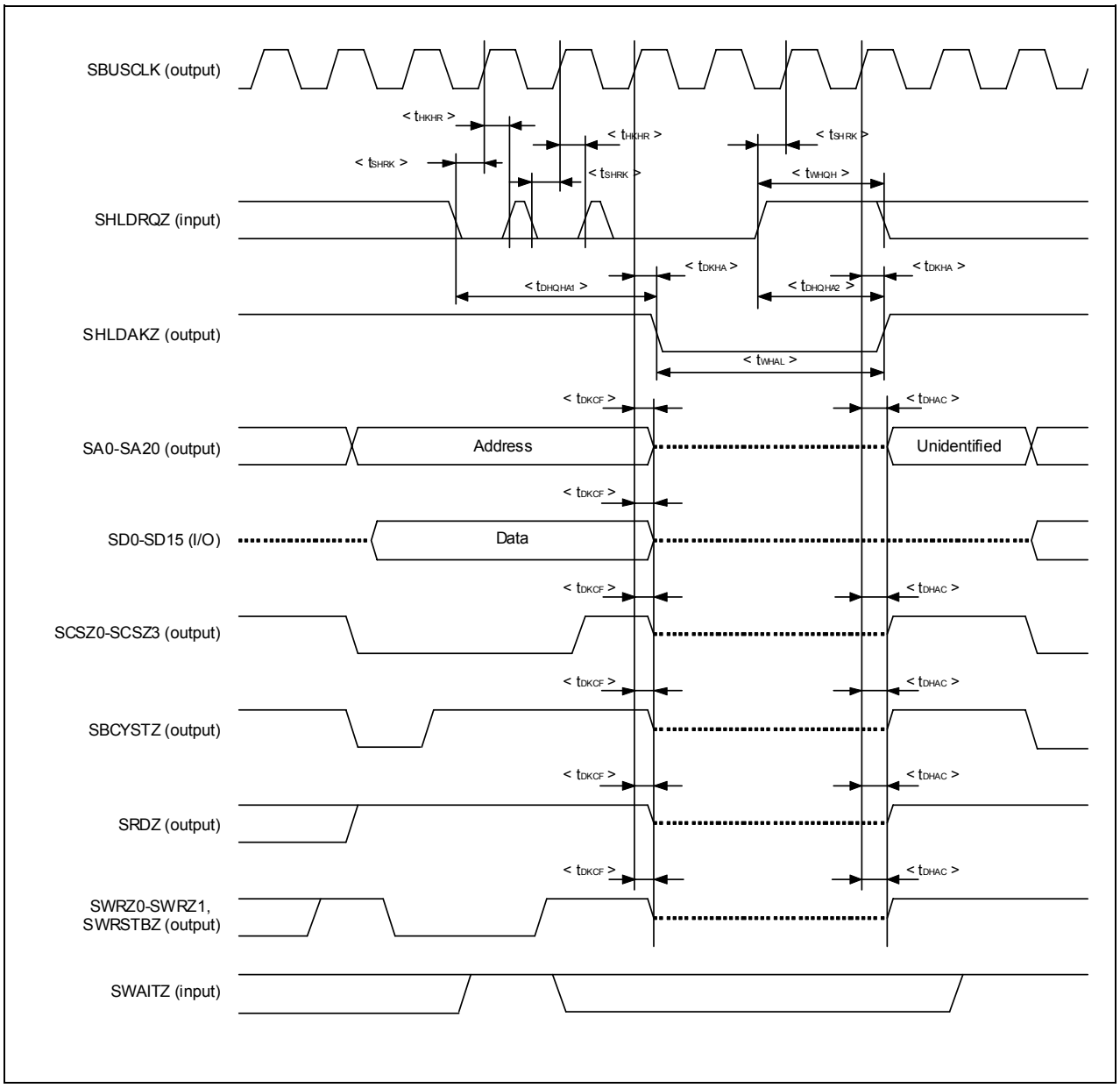
(2) Bus hold timing

Table 1-16. Bus Hold Timing

Parameter	Symbol	MIN.	MAX.	Unit
SHLDRQZ setup time (to SBUSCLK↑)	t_{SHRK}	3.8	–	ns
SHLDRQZ hold time (from SBUSCLK↑)	t_{HKHR}	2.0	–	ns
Delay time from SBUSCLK↑ to SHLDAKZ	t_{DKHA}	1.5	11.0	ns
SHLDRQZ high-level width	t_{WHQH}	$5.8 + t_{BCLK}$	–	ns
SHLDAKZ low-level width	t_{WHAL}	$–9.5 + t_{BCLK}$	–	ns
Delay time from SBUSCLK↑ to bus float	t_{DKCF}	1.5	–	ns
Delay time from SBUSCLK↑ to bus output	t_{DHAC}	1.5	13.0	ns
Delay time from SHLDRQZ↓ to SHLDAKZ↓	t_{DHQHA1}	$1.5 \times t_{BCLK}$	–	ns
Delay time from SHLDRQZ↑ to SHLDAKZ↑	t_{DHQHA2}	$0.5 \times t_{BCLK}$	$3 \times t_{BCLK} + 3.8$	ns

Remark t_{BCLK}: SBUSCLK cycle

Figure 1-19. Bus Hold Timing



1.7.5 DMA interface pins

(3) BUSCLK-synchronization signal

The second DMA transfer request disable timing in single transfer is described below.

Table 1-17. BUSCLK-synchronization Signal

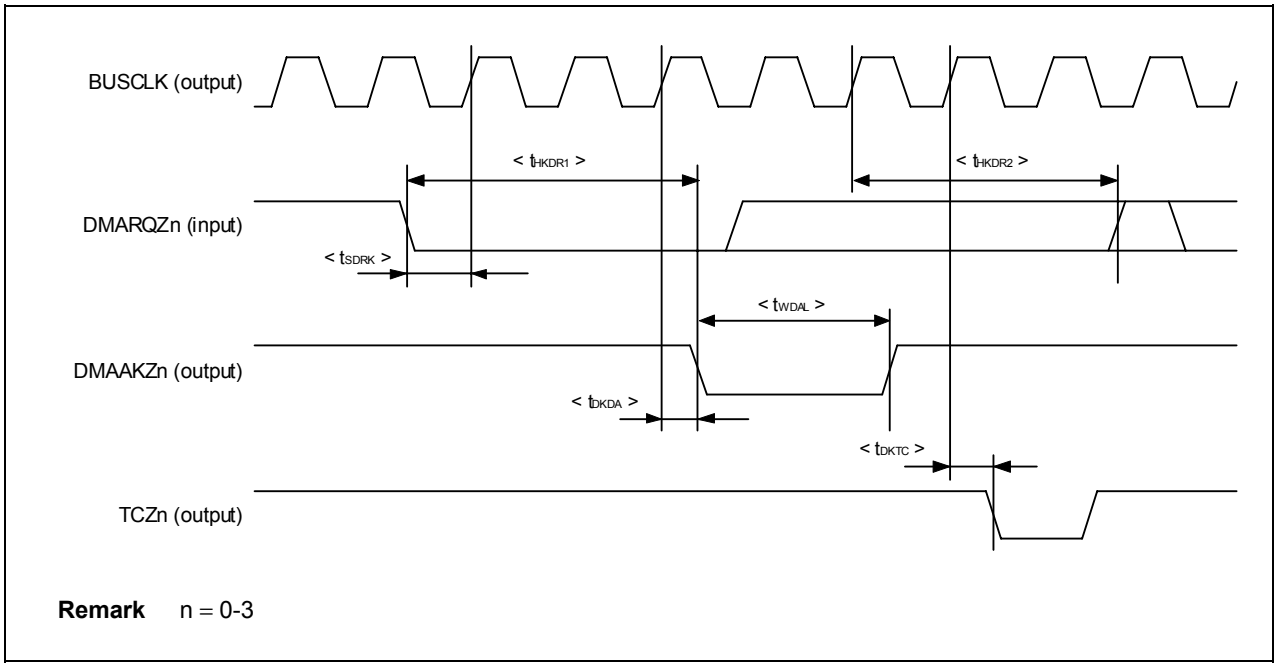
Parameter	Symbol	MIN.	MAX.	Unit
DMARQZ0-DMARQZ3 setup time(from BUSCLK↑)	t_{SDRK}	4.3	–	ns
DMARQZ0-DMARQZ3 hold time 1	t_{HKDR1}	To DMAAKZ↓	–	ns
DMARQZ0-DMARQZ3 hold time 2 (from BUSCLK↑)	t_{HKDR2}	–4.3	$m \times t_{BCLK} - 4.3$	ns
DMAAKZ0-DMAAKZ3 output delay time (from BUSCLK↑)	t_{DKDA}	2.0	11.0	ns
DMAAKZ0-DMAAKZ3 low level width	t_{WDAL}	$-9.0 + n \times t_{BCLK}$	$9.0 + n \times t_{BCLK}$	ns
TCZ0-TCZ3 output delay time (from BUSCLK↑)	t_{DKTC}	2.0	11.0	ns

Remarks 1. t_{BCLK}: BUSCLK cycle

2. m = 0 to 15 (DMARQZ0 to DMARQZ3 signal mask widths set via DMAIFC0 to DMAIFC3 registers)

3. n = 1 to 16 (DMAAKZ0 to DMAAKZ3 signal active-level widths set via DMAIFC0 to DMAIFC3 registers)

Figure 1-20. DMA Interface (BUSCLK-synchronization Signal)



Remark n = 0-3

1.7.6 SiP internal-connection DMA interface pins

(1) SBUSCLK-synchronization signal

The second DMA transfer request disable timing in single transfer is described below.

Table 1-18. SBUSCLK-synchronization Signal

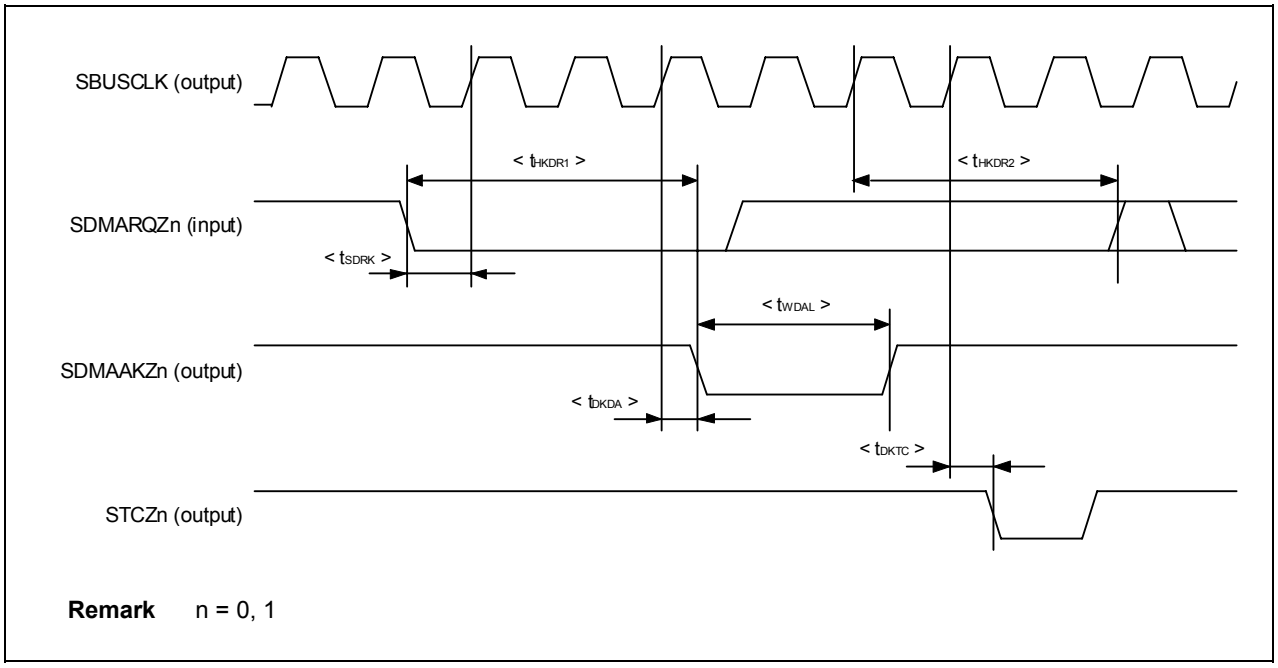
Parameter	Symbol	MIN.	MAX.	Unit
SDMARQZ0-SDMARQZ3 setup time (from SBUSCLK↑)	t_{SDRK}	4.3	–	ns
SDMARQZ0-SDMARQZ3 hold time 1	t_{HKDR1}	To DMAAKZ↓	–	ns
SDMARQZ0-SDMARQZ3 hold time 2 (from SBUSCLK↑)	t_{HKDR2}	–4.3	$m \times t_{BCLK} - 4.3$	ns
SDMAAKZ0-SDMAAKZ3 output delay time (from SBUSCLK↑)	t_{DKDA}	2.0	11.0	ns
SDMAAKZ0-SDMAAKZ3 low level width	t_{WDAL}	$-9.0 + n \times t_{BCLK}$	$9.0 + n \times t_{BCLK}$	ns
STCZ0-STCZ3 output delay time (from SBUSCLK↑)	t_{DKTC}	2.0	11.0	ns

Remarks 1. t_{BCLK}: SBUSCLK cycle

2. m = 0 to 15 (DMARQZ0 to DMARQZ3 signal mask widths set via DMAIFC0 to DMAIFC3 registers)

3. n = 1 to 16 (DMAAKZ0 to DMAAKZ3 signal active-level widths set via DMAIFC0 to DMAIFC3 registers)

Figure 1-21. DMA Interface (SBUSCLK-synchronization Signal)



Remark n = 0, 1

1.7.7 Bus reset output puns

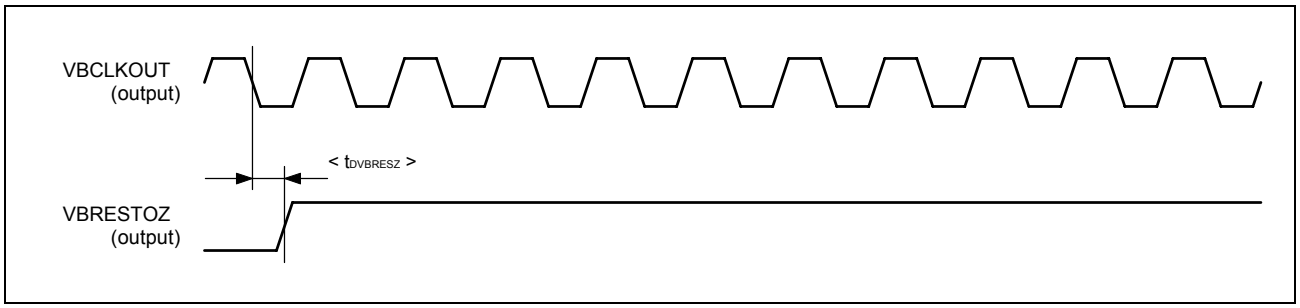
(1) External Memory interface pins

The access timing of the external bus reset output pun is described below.

Table 1-19. External Bus Reset Output Pin

Parameter	Symbol	MIN.	MAX.	Unit
VBRESTOZ output delay time (from VBCLKOUT↓)	$t_{DVBRESZ}$	1.0	10.0	ns

Figure 1-22. External Bus Reset Output Pin



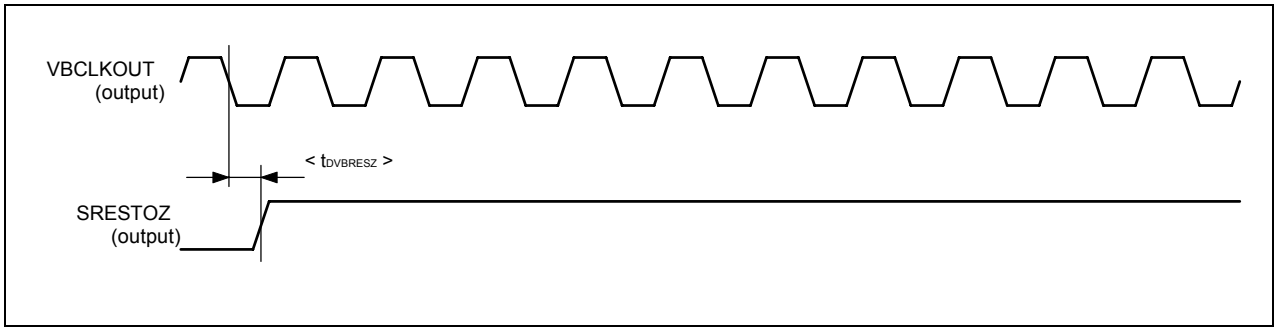
(2) SiP internal-connection bus interface pins

The access timing of the SiP internal-connection bus reset output pin is described below.

Table 1-20. SiP Internal-connection Bus Interface Pin

Parameter	Symbol	MIN.	MAX.	Unit
SRESTOZ output delay time (from VBCLKOUT↓)	$t_{DVBRESZ}$	1.0	8.0	ns

Figure 1-23. SiP Internal-connection Bus Reset Output Pin



1.7.8 CSI interface pins

The access timing of CSI (Clock-synchronized Serial Interface) is shown below.

CSI has a master mode and a slave mode, and they show their respective timings. The operating timing varies depending on CKP and DAP settings.

Table 1-21. CSI Access Timing (Master Mode)

Parameter	Symbol	MIN.	MAX.	Unit
SCKn output cycle	t_{CSICYC}	40.0	–	ns
Sin input setup time (to SCKn↑)	t_{SSI}	14.0	–	ns
Sin input setup time (from SCKn↓)	t_{SSI}	14.0	–	ns
Sin input hold time (from SCKn↑)	t_{HSI}	2.0	–	ns
Sin input hold time (to SCKn↓)	t_{HSI}	2.0	–	ns
SOn output delay time(to SCKn↑)	t_{DSO}	–	6.0	ns
SOn output delay time (from SCKn↓)	t_{DSO}	–	6.0	ns
SOn output hold time (from SCKn↓)	t_{HSO}	$t_{CSICYC} \times 1/2 - 1.5$	–	ns
SOn output hold time (to SCKn↓)	t_{HSO}	$t_{CSICYC} \times 1/2 - 1.5$	–	ns

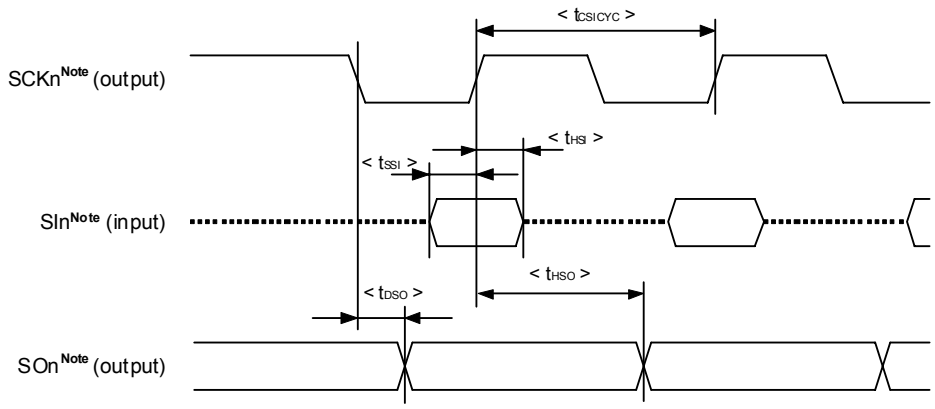
Remark n = 0, 1

Table 1-22. CSI Access Timing (Slave Mode)

Parameter	Symbol	MIN.	MAX.	Unit
SCKn output cycle	t_{CSICYC}	40.0	–	ns
Sin input setup time (to SCKn↑)	t_{SSI}	2.0	–	ns
Sin input setup time (from SCKn↓)	t_{SSI}	2.0	–	ns
Sin input hold time (from SCKn↑)	t_{HSI}	2.0	–	ns
Sin input hold time (to SCKn↓)	t_{HSI}	2.0	–	ns
SOn output delay time(to SCKn↑)	t_{DSO}	–	15.0	ns
SOn output delay time (from SCKn↓)	t_{DSO}	–	15.0	ns
SOn output hold time (from SCKn↓)	t_{HSO}	$t_{CSICYC} \times 1/2 + 2.5$	–	ns
SOn output hold time (to SCKn↓)	t_{HSO}	$t_{CSICYC} \times 1/2 + 2.5$	–	ns

Remark n = 0, 1

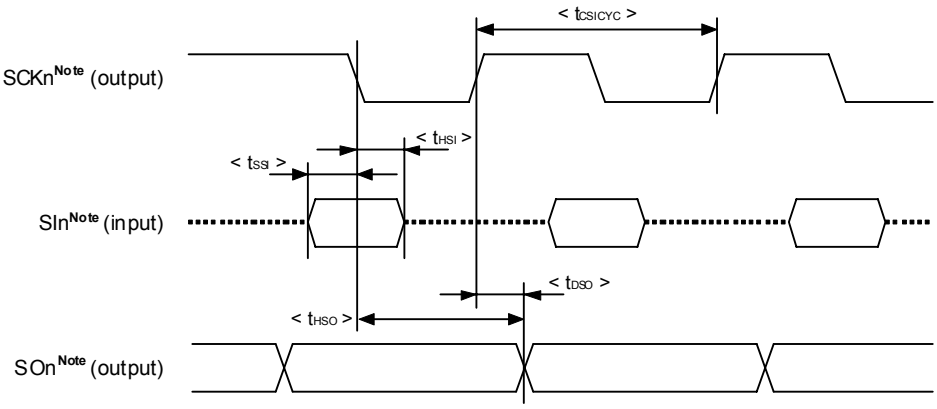
Figure 1-24. CSI Access Timing (CKP, DAP = 00)



Note n = 0, 1

Remark Broken lines indicate high impedance.

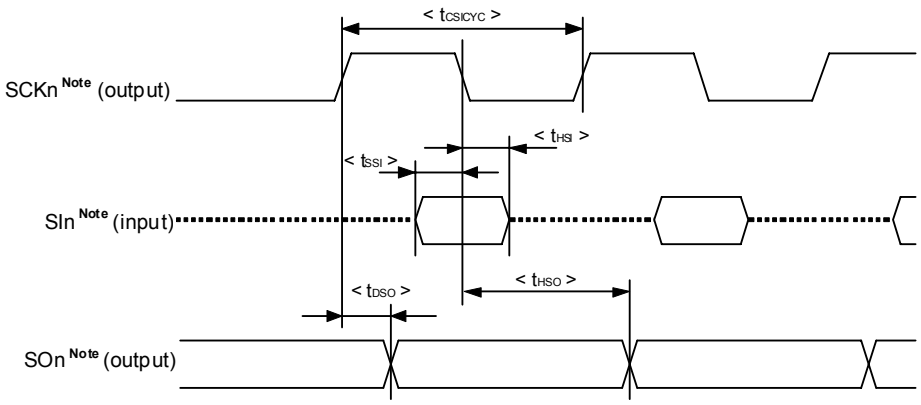
Figure 1-25. CSI Access Timing (CKP, DAP = 01)



Note n = 0, 1

Remark Broken lines indicate high impedance.

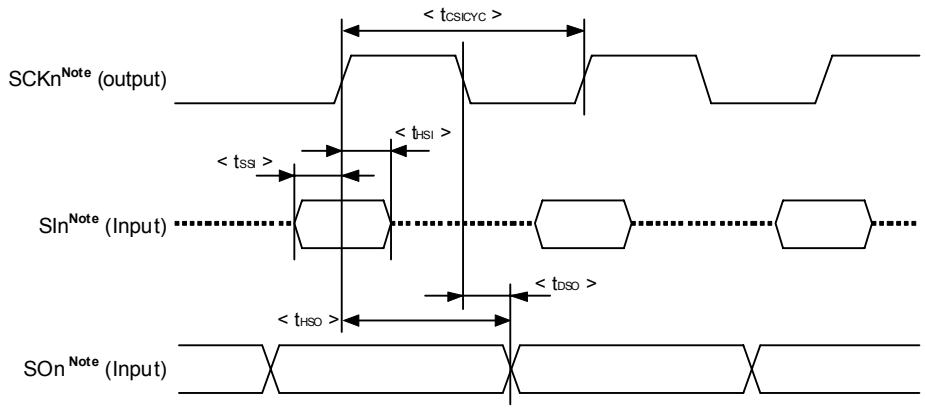
Figure 1-26. CSI Access Timing (CKP, DAP = 10)



Note n = 0, 1

Remark Broken lines indicate high impedance.

Figure 1-27. CSI Access Timing (CKP, DAP = 11)



Note n = 0, 1

Remark Broken lines indicate high impedance.

1.7.9 N-Wire interface pins

(1) Trace interface

The access timing of the trace interface is shown below.

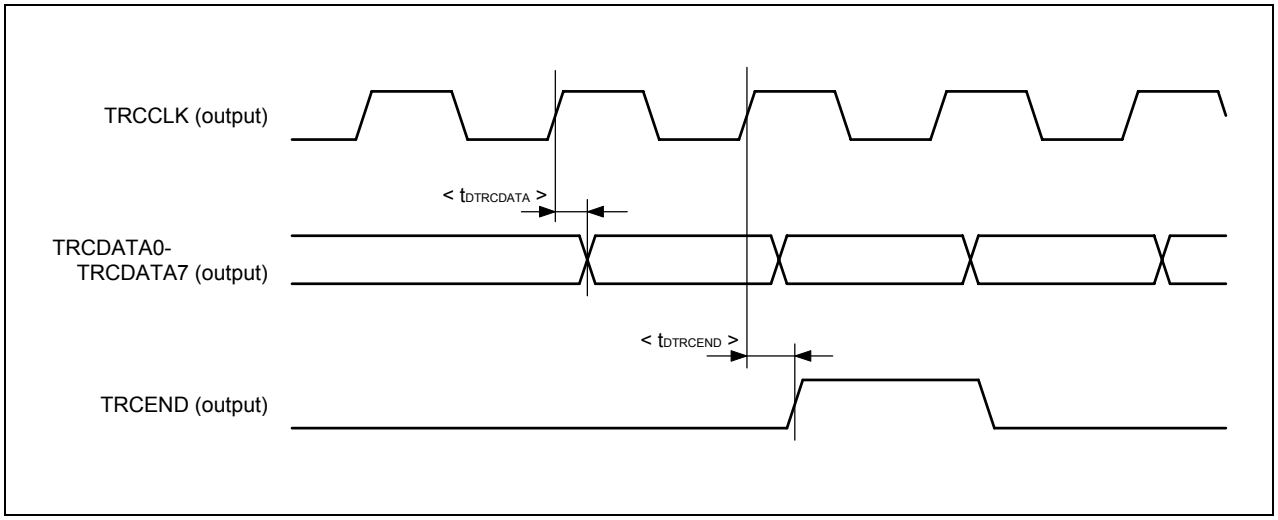
Table 1-23. Trace Interface

Parameter	Symbol	MIN.	MAX.	Unit
TRCDATA output delay time (from TRCCLK↑)[Note]	$t_{DTRCDATA}$	0.0	$t_{CCLK} \times 0.5 + 3.5$	ns
TRCEND output delay time (from TRCCLK↑)[Note]	$t_{DTRCEND}$	0.0	$t_{CCLK} \times 0.5 + 3.5$	ns

Note The data output timing of TRCDATA0-TRCDATA7 or TRCEND can be output at the both rising and falling edges of TRCCLK. It also can be output at the falling edge of TRCCLK. When the timing is output at the falling edge of TRCCLK, each output delay time is the same as that of the timing output at the rising edge of TRCCLK. However, the TRCCLK edge for reference differs.

Remark t_{CCLK}: CPCLK cycle

Figure 1-28. Trace Interface



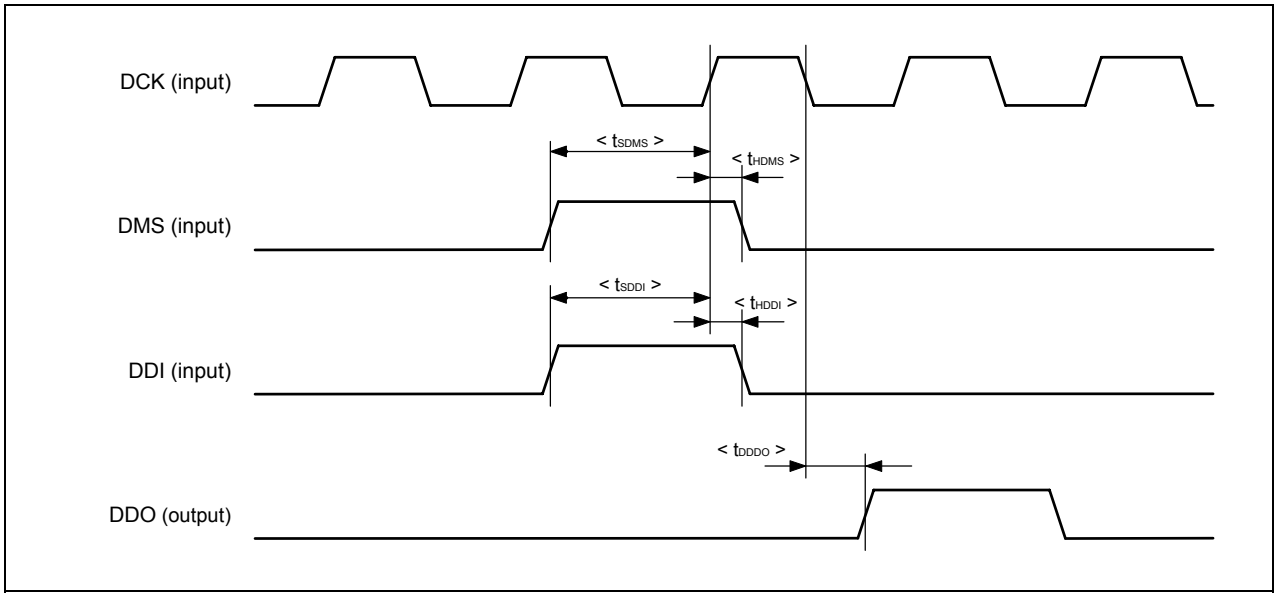
(2) Debug serial interface

The access timing of the debug serial interface is shown below.

Table 1-24. Debug Serial Interface

Parameter	Symbol	MIN.	MAX.	Unit
DMS input setup time (to DCK↑)	t_{SDMS}	10.0	–	ns
DMS input hold time (from DCK↑)	t_{HDMS}	20.0	–	ns
DDI input setup time (to DCK↑)	t_{SDDI}	10.0	–	ns
DDI input hold time (from DCK↑)	t_{HDDI}	20.0	–	ns
DDO output delay time (from DCK↓)	t_{DDDO}	3.0	15.0	ns

Figure 1-29. Debug Serial Interface



1.8 A/D Converter Characteristics

Table 1-25. A/D Converter Characteristics (EV_{DD} = AV_{DD} = AV_{REFP} = 3.0 to 3.6 V, EV_{SS} = AV_{SS} = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Overall error Note 1	–				±0.49	%FSR
Quantization error	–				±1/2	LSB
Conversion time	t_{CONV}		2.00		10	μs
Sampling time	t_{SAMP}		3 × conversion clock Note 2/16			ns
Zero-scale error Note 1	–				±0.49	%FSR
Full-scale error Note 1	–				±0.49	%FSR
Integral linearity error Note 3	–				±4	LSB
Differential linearity error Note 3	–				±4	LSB
Analog input voltage	V_{WASN}		AV_{REFM}		AV_{REFP}	V
AV_{DD} power supply current	AI_{DD}				10	mA
ADTRG high-level width	t_{WAIH}		500			ns
ADTRG low-level width	t_{WAIL}		500			ns

Notes 1. Excluding quantization error (±0.05% FSR).

2. The conversion clock indicates the number of clocks set by the ADM1 register.

3. Excluding quantization error (±0.5LSB).

Remark LSB: Least Significant Bit

FSR: Full Scale Range

%FSR indicates the ratio to the full-scale value.

Figure 1-30. A/D Converter Characteristics

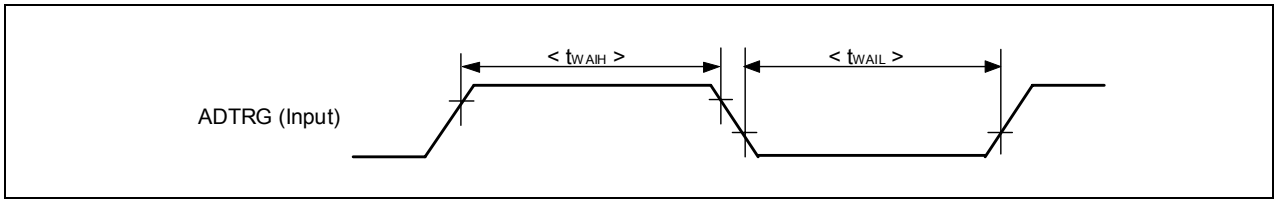


Figure 1-31. Equivalent Circuit of Analog Input Pins

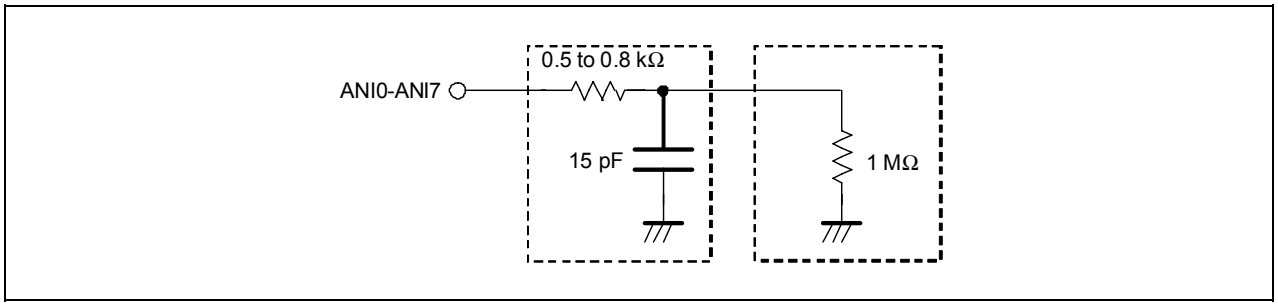


Table 1-26. Analog Input Pin Specifications

Parameter	Symbol	MIN.	MAX.	Unit
Analog input capacitance	–		15	pF
Allowable signal source impedance	–		1	kΩ

1.9 Power Supply Application/Interruption Procedure

Pin capacitance is the sum of the interface block capacitance and the package characteristic capacitance.
Table 1-27 and 1-28 show the capacitance (C_B) of the interface blocks.
The pin capacitance is calculated by the following formula:

Pin capacitance (C_T) = interface block capacitance (C_B) + capacitance (C_P) of each package

1.9.1 Input buffer

Table 1-27. Capacitance of Interface Block (C_B)

Interface Level	$C_{B\ (MIN)}$	$C_{B\ (MAX)}$
3.3 V	2.0 pF	4.0 pF

Remark V_{DD} = 0 V, T_J = 25 °C, f = 1 MHz

1.9.2 Output buffer/bidirectional buffer

Table 1-28. Capacitance of Interface Block (Output Buffer/Bidirectional Buffer) (C_B)

Interface Level	6 mA		9 mA		12 mA		18 mA	
	$C_{B\ (MIN)}$	$C_{B\ (MAX)}$	$C_{B\ (MIN)}$	$C_{B\ (MAX)}$	$C_{B\ (MIN)}$	$C_{B\ (MAX)}$	$C_{B\ (MIN)}$	$C_{B\ (MAX)}$
3.3 V	2.0 pF	4.0 pF	2.0 pF	4.0 pF	2.0 pF	4.0 pF	2.0 pF	4.0 pF

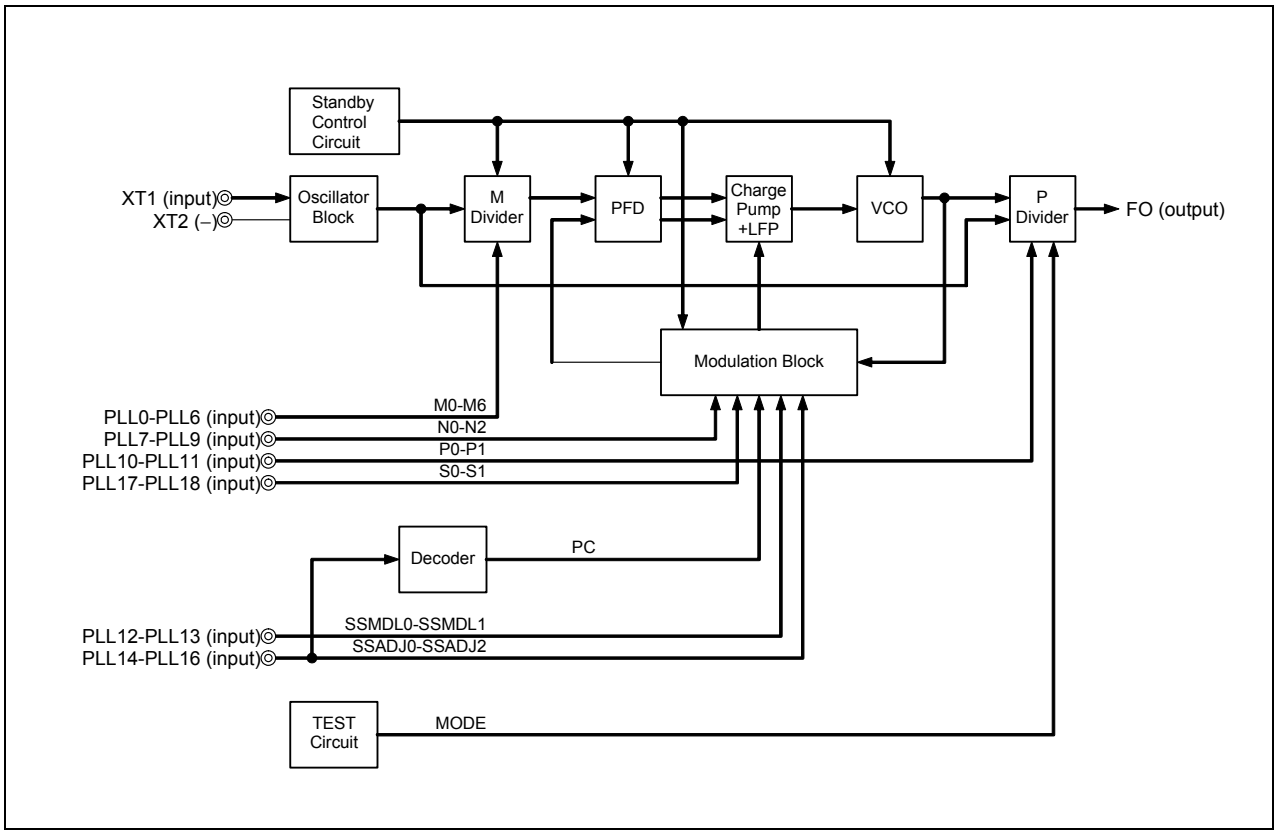
Remark V_{DD} = 0 V, T_J = 25 °C, f = 1 MHz

CHAPTER 2 INTERNAL SSCG-PLL CHARACTERISTICS

The SSCG-PLL incorporated in PFESiP/V850EP1 is a spread spectrum clock generator used to suppress noise, and is effective in reducing the peak value of electromagnetic interference (EMI) noise.

2.1 Block Diagram

Figure 2-1. SSCG-PLL Block Diagram



2.2 Electrical Specifications

2.2.1 Recommended operating range

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Oscillation Block Input Frequency	f_{osc}	–	2.0	50.0	MHz
Input Frequency	f_{std}	–	2.0	200.0	MHz
PFD Input Frequency	f_{pfd}	$f_{pfd} = f_{std} / m$	1.0	2.0	MHz
Input Duty	I_{duty}	–	30	70	%
Multiple Rate	MULT	MULT = n / m / p	0.182	50	–
Frequency Division Ratio Setting	m	–	2	128	–
	n	–	93	100	–
	p	–	1	4	–

2.2.2 Electrical specifications

Parameter	Symbol	Conditions	MIN.	TYP	MAX	Unit	Remark
VCO Output Frequency	f_{vco}	$f_{vco} = f_{std} \times n/m$	100		200	MHz	
Output Frequency	f_{out}	$f_{out} = f_{std} \times n/m/p$	25		200	MHz	
Output Duty	duty	–	47		53	%	$C_L \leq 0.2$pF
Output Period Jitter	t_{pj}	–	−150		150	Ps	Fixed frequency mode
Multiple Rate	MULT	MULT = n/m/p	0.182		50	–	
Modulation Period	f_{mod}	PLL13-PLL12(SSMDL1-SSMDL0)= 00		20		kHz	
		PLL13-PLL12(SSMDL1-SSMDL0)= 01		30		kHz	
		PLL13-PLL12(SSMDL1-SSMDL0)= 10		40		kHz	
		PLL13-PLL12(SSMDL1-SSMDL0)= 11		50		kHz	
Frequency Modulation Rate	f_{dit}	PLL16-PLL14(SSADJ2-SSADJ0)= 000		−0.5		%	The settings are performed without modulation in the setting conditions other than those in the left column.
		PLL16-PLL14(SSADJ2-SSADJ0)= 001		−1.0		%	
		PLL16-PLL14(SSADJ2-SSADJ0)= 010		−2.0		%	
		PLL16-PLL14(SSADJ2-SSADJ0)= 011		−3.0		%	
		PLL16-PLL14(SSADJ2-SSADJ0)= 100		−4.0		%	
		PLL16-PLL14(SSADJ2-SSADJ0)= 101		−5.0		%	

Remark The PFD input frequency is an output frequency of the M divider. Refer to **2.1 Block Diagram**.

2.3 Setting SSCG-PLL Operation Mode with Pins

To set SSCG-PLL Operation mode, PFESiP/V850EP1 has the following pins.
Set the following pins to satisfy the specified operating conditions before turning on power.

<table>
<tr><th>Pin Name</th><th>Internal Signal</th><th>Function</th></tr>
<tr><td>PLL0-PLL6
PLL7-PLL9
PLL10-PLL11</td><td>PLLM0-PLLM6
PLLN0-PLLN2
PLLP0-PLLP1</td><td>Setting internal PLL multiple rate
m = PLLM0-PLLM6 setting value (0 to 127) + 1 : 2 to 128
n = PLLN0-PLLN2 setting value (0 to 7) + 92 + 1 : 93 to 100
$p = 2^{\text{PLLP0 to PLLP1 setting value}}$: 1, 2, 4
multiple rate = n / m / p
<table>
<tr><th>Parameter</th><th>Symbol</th><th>Formula</th><th>MIN.</th><th>MAX</th><th>Unit</th></tr>
<tr><td>Input Frequency</td><td>f_{std}</td><td>–</td><td>2.0</td><td>200</td><td>MHz</td></tr>
<tr><td>PFD Input Frequency</td><td>f_{pfd}</td><td>$f_{pfd} = f_{std} / m$</td><td>1.0</td><td>2.0</td><td>MHz</td></tr>
<tr><td>VCO Output Frequency</td><td>f_{vco}</td><td>$f_{vco} = f_{std} \times n / m$</td><td>100</td><td>200</td><td>MHz</td></tr>
<tr><td>Output Frequency</td><td>f_{out}</td><td>$f_{out} = f_{std} \times n / m / p$</td><td>25</td><td>200</td><td>MHz</td></tr>
<tr><td>Input Duty</td><td>I_{duty}</td><td>–</td><td>30</td><td>70</td><td>%</td></tr>
<tr><td>Multiple Rate</td><td>MULT</td><td>MULT = n / m / p</td><td>0.182</td><td>50</td><td>–</td></tr>
</table></td></tr>
<tr><td>PLL12-PLL13</td><td>SSMDL0-SSMDL1</td><td>Setting SSCG modulation range
<table>
<tr><th>SSMDL1</th><th>SSMDL0</th><th>Modulation Period</th></tr>
<tr><td>0</td><td>0</td><td>15.00 to 26.25 kHz (open)</td></tr>
<tr><td>0</td><td>1</td><td>25.00 to 36.75 kHz</td></tr>
<tr><td>1</td><td>0</td><td>35.00 to 48.30 kHz</td></tr>
<tr><td>1</td><td>1</td><td>45.00 to 68.25 kHz</td></tr>
</table></td></tr>
<tr><td>PLL14-PLL16</td><td>SSADJ0-SSADJ2</td><td>Setting SSCG frequency diffusion mode and its range.
<table>
<tr><th>SSADJ2</th><th>SSADJ1</th><th>SSADJ0</th><th>Frequency Modulation Rate</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Approx. –0.5 %</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Approx. –1.0 %</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Approx. –2.0 %</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Approx. –3.0 %</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Approx. –4.0 %</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Approx. –5.0 %</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>No modulation</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No modulation</td></tr>
</table></td></tr>
<tr><td>PLL17-PLL18</td><td>PLLS0-PLLS1</td><td>Inputs SSCG S selector (Frequency Modulation mode)
<table>
<tr><th>PLLS1</th><th>PLLS0</th><th>PFD Input Frequency</th></tr>
<tr><td>0</td><td>0</td><td>1.00 MHz ≤ f_{pfd} <1.20 MHz (open)</td></tr>
<tr><td>0</td><td>1</td><td>1.20 MHz ≤ f_{pfd} <1.45 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1.45 MHz ≤ f_{pfd} <1.70 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1.70 MHz ≤ f_{pfd} ≤ 2.00 MHz</td></tr>
</table></td></tr>
</table>

2.3.1 PLLM0-PLLM6, PLLN0-PLLN2, PLLP0-PLLP1 (PLLM, N, P-counter select)

These pins set the multiplication factor of an internal PLL.

PLLM0 to PLLM6, and PLLP0 and PLLP1 are directly connected to AAPLSCGH of the internal PLL.

PLLN0 to PLLN2 are connected to AAPLSCGH, while 92 is added to them, because the input range of AAPLSCGH is 92 to 99 in decimal form.

The multiple rates are calculated by the following formula:

m = PLLM0 to PLLM6 setting value (0 to 127) + 1 : 2 to 128
n = PLLN0 to PLLN2 setting value (0 to 7) + 92 + 1 : 93 to 100
$p = 2^{\text{PLLP0 to PLLP1 setting value}}$: 1, 2, 4
Multiple rate = n/m/p

The following specifications are satisfied in AAPLSCGH.

Table 2-1. PLL Operating Conditions

Parameter	Symbol	Formula	MIN.	MAX	Unit
Input Frequency	f_{std}	–	2.0	200	MHz
PFD Input Frequency	f_{pfd}	$f_{pfd} = f_{std} / m$	1.0	2.0	MHz
VCO Output Frequency	f_{vco}	$f_{vco} = f_{std} \times n / m$	100	200	MHz
Output Frequency	f_{out}	$f_{out} = f_{std} \times n / m / p$	25	200	MHz
Input Duty	I_{duty}	–	30	70	%
multiple rate	MULT	MULT = n / m / p	0.182	50	–

PLL11	PLL10	p	PLL Output Frequency [MHz]
PLLP1	PLLP0		
0	0	1	100 to 200
0	1	2	50 to 100
1	0	4	25 to 50
1	1	Through mode	Through mode

Furthermore, when PLLM0 to PLLM6 are all set to low level, and PLLP0 and PLLP1 are both set to high level, these low- and high-level settings being prohibited, both of these PLL settings are set to through mode.

2.3.2 SSMDL0 to SSMDL1 (modulation frequency range) (input)

Set SSCG-output modulation period.

These pins are directly connected to MDL0 and MDL1 of AAPLSCGH.

Table 2-2. Setting SSCG-output Modulation Period by SSMDL0 to SSMDL1

PLL13	PLL12	Modulation Period [kHz]
SSMDL1	SSMDL0	
0	0	15.00 to 26.25 (open)
0	1	25.00 to 36.75
1	0	35.00 to 48.30
1	1	45.00 to 68.25

2.3.3 SSADJ0 to SSADJ2 (dither range / mode) (input)

Set SSCG-output frequency modulation rate.

These pins are connected to ADJ0 to ADJ2 of AAPLSCGH.

If SSADJ2 = 1 and SSADJ1 = 1, the mode with no frequency modulation occurs.

Table 2-3. Setting SSCG-output Frequency Modulation Rate

PLL16	PLL15	PLL14	Frequency Modulation Rate
SSADJ2	SSADJ1	SSADJ0	
0	0	0	Approx. –0.5 %
0	0	1	Approx. –1.0 %
0	1	0	Approx. –2.0 %
0	1	1	Approx. –3.0 %
1	0	0	Approx. –4.0 %
1	0	1	Approx. –5.0 %
1	1	0	No modulation
1	1	1	No modulation

Caution Setting modulation affects the UART baud rate and timer interval time.
For example, with UART, evaluate the permissible baud rate error with the other party of communication.

2.3.4 PLLS0 to PLLS1 (S-selector) (input)

Set the S-selector as below, according to the value of the PFD input frequency (fpfd) specified in Table 2-1 when these pins are used in frequency diffusion mode.

Table 2-4. Setting the S-selector

PLL18	PLL17	PFD Input Frequency [MHz]
PLLS1	PLLS0	
0	0	$1.00 \leq f_{pfd} < 1.20$ (Open)
0	1	$1.20 \leq f_{pfd} < 1.45$
1	0	$1.45 \leq f_{pfd} < 1.70$
1	1	$1.70 \leq f_{pfd} \leq 2.00$

2.3.5 PLLFOEN (PLL FO output enable) (input)

The FO output of the internal PLL can be output from the PLLFO pin.

The IDLE control circuit is not stopped even in the IDLE mode, because it is on the CPU side.

FO is output to PLLFO only when a high level is input to PLLFOEN.

A low level is output when a low level is input to PLLFOEN.

This output control is an enable control configuration. Noise (whiskers) may occur when switching is performed during an operation.

Table 2-5. PLL FO Output Control by PLLFOEN Pin

PLLFOEN	PLL FO Output Control
0	Low-level output
1	Output enabled

CHAPTER 3 DEVELOPMENT TOOLS AND MIDDLEWARE

The following development tools and middleware are provided for developing systems using the PFESiP/V850EP1.

3.1 Development Tools

Real-time OS	Compiler	Debugger	Server	In-circuit emulator	Remark
RX850pro (NEC Electronics Corporation)	CCV850 Note 1 (Green Hills Software, Inc.)	MULTI (Green Hills Software, Inc.)	rteserve (Advanced Data Controls Corporation)	RTE-2000-TP (Midas lab Inc.) RTE-2000H-TP (Midas lab Inc.)	No. of traces: 8
			YDCSERVE Note 2 (Advanced Data Controls Corporation)	advicePLUS (Yokogawa Digital Computer Corporation)	No. of traces: 8
		MicroVIEW-PLUS (Yokogawa Digital Computer Corporation)	–	advicePLUS (Yokogawa Digital Computer Corporation)	No. of traces: 8
	CA850 (NEC Electronics Corporation)	ID850QB Note 3 (NEC Electronics Corporation)	N-EXEC (Midas lab Inc.)	RTE-2000-TP (Midas lab Inc.) RTE-2000H-TP (Midas lab Inc.)	No. of traces: 8
			–	QB-V850MINI(NEC Electronics Corporation) (MINI CUBE)	No trace function
		PARTNER Note 4 (Kyoto Microcomputer Corporation)	–	PARTNER-Jet (Kyoto Microcomputer Corporation)	No. of traces: 4

Notes 1. Ver. 4.0, which supports pipeline optimization, is recommended for utilizing the performance of the V850E2 CPU.

2. “IDE FOR V800 WITH YDCSERVE”, which integrates CCV850, Multi, and YDCSERVE is also provided.

3. QB-V850MINI is provided with ID850QB.

4. PARTNER-Jet is provided with PARTNER.

3.2 Middleware

The PFESiP/V850EP1 has an on-chip USB host controller and USB function controller.
Generally, to use the USB function, a driver for the microcontroller provided with the USB function is required. Accordingly, the mass storage class sample driver of the USB function controller is provided.

USB driver package products are provided by GRAPE SYSTEMS INC.

[MEMO]

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