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## カタログ等資料中の旧社名の扱いについて

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ルネサスエレクトロニクス ホームページ (<http://www.renesas.com>)

2010年4月1日  
ルネサスエレクトロニクス株式会社

【発行】ルネサスエレクトロニクス株式会社 (<http://www.renesas.com>)

【問い合わせ先】 <http://japan.renesas.com/inquiry>

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高品質水準： 輸送機器（自動車、電車、船舶等）、交通用信号機器、防災・防犯装置、各種安全装置、生命維持を目的として設計されていない医療機器（厚生労働省定義の管理医療機器に相当）  
特定水準： 航空機器、航空宇宙機器、海底中継機器、原子力制御システム、生命維持のための医療機器（生命維持装置、人体に埋め込み使用するもの、治療行為（患部切り出し等）を行うもの、その他直接人命に影響を与えるもの）（厚生労働省定義の高度管理医療機器に相当）またはシステム等
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**Block Library**

# **CMOS-N5 Family**

**CMOS Gate Array**

**(5.0 V) Ver.5.0**

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[MEMO]

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    - 特別水準：輸送機器（自動車、列車、船舶等）、交通信号機器、防災／防犯装置、各種安全装置、生命維持を直接の目的としない医療機器
    - 特定水準：航空機器、航空宇宙機器、海底中継機器、原子力制御システム、生命維持のための医療機器、生命維持のための装置またはシステム等
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## 本版で改訂された主な箇所

箇所	内容
全般	構成，数値を全面的に変更

巻末にアンケート・コーナーを設けております。このドキュメントに対するご意見をお気軽にお寄せください。

# はじめに

このマニュアルはCMOS-N5ファミリの5.0 Vのブロックについて記載しています。3.3 VのブロックについてはCMOS-N5 Family (3.3 V) Block Libraryを参照してください。

回路設計を行う際には必ず先にCMOS-N5ファミリ **設計マニュアル (A13826J)** を読んでください。

またマニュアルに記載された事項（一般事項，注意事項，制限事項）は必ずお守りください。お守りいただけない場合，LSI製品の品質や性能の低下，および動作の異常が生じることがあります。

## 1. 構成

このマニュアルは次のような構成になっています。

### (1) はじめに

このマニュアルを活用されるにあたっての注意事項，用語，定義などを説明しています。

### (2) Contents

目次としてブロックを機能別にまとめてあります。

### (3) Chapter 1 Interface Block

### (4) Chapter 2 Function Block

### (5) Chapter 3 Scan Path Block

### (6) Chapter 4 Boundary Scan Block

Chapter 1～4は，それぞれのブロックを機能順に並べてあります。各ページには，論理シンボル，真理値表，入出力データ，スイッチング・スピード（伝達遅延時間）などを2. **ブロック・ライブラリ記載内容の説明**に添って記載してあります。

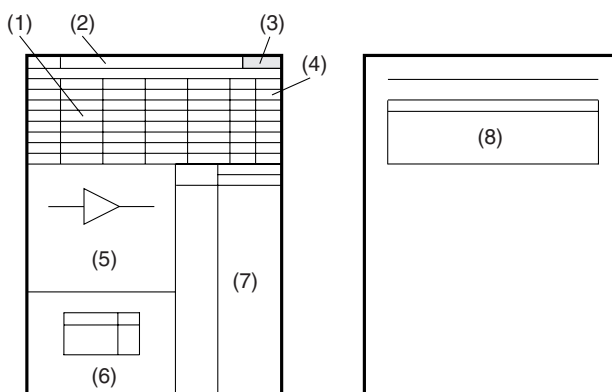
### (7) Index

索引としてブロックをアルファベット順にまとめてあります。

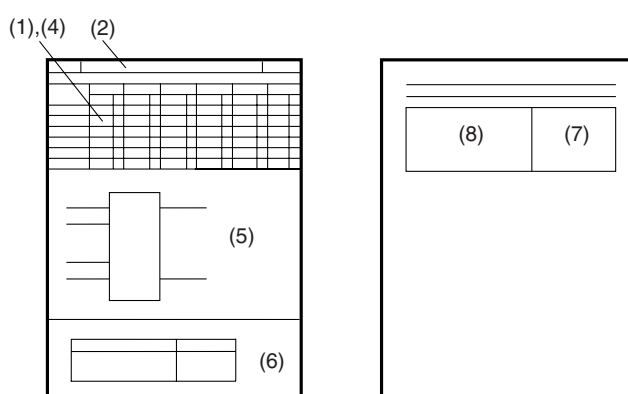


## 2. ブロック・ライブラリ記載内容の説明

(a) インタフェース・ブロック

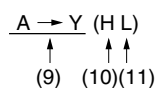


(b) ファンクション・ブロック



- |                       |  |
|-----------------------|--|
| (1) Block type        | : 機能ブロックの名称                                      |
| (2) Function          | : そのブロックの機能名                                     |
| (3) Interface level   | : そのブロックのインタフェース・レベル                             |
| (4) No. of int. cells | : 使用セル数 (内部セル数)                                  |
| (5) Logic Diagram     | : そのブロックの論理シンボル (論理図)                            |
| (6) Truth Table       | : そのブロックの真理値表                                    |
| (7) Input, Output     | : Input (入力端子名, Fan-in), Output (出力端子名, Fan-out) |
| (8) Switching speed   | : そのブロックの伝達遅延時間など                                |

なお、スイッチング・スピードの記号は次のとおりです。



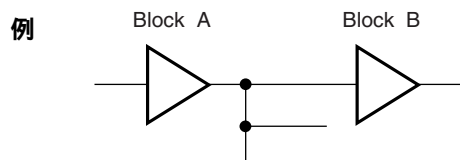
- |              |                                       |
|--------------|---------------------------------------|
| (9) 信号のパス名   | (入力 出力)                               |
| (10) 入力信号の状態 | (H: ハイ・レベル, L: ロウ・レベル, Z: ハイ・インピーダンス) |
| (11) 出力信号の状態 | (H: ハイ・レベル, L: ロウ・レベル, Z: ハイ・インピーダンス) |

Setup time, Hold time, Release time, Removal time, Minimum pulse widthはMIN.条件での最小値をMIN.の欄に, またMAX.条件での最小値をMAX.の欄に記載しています。

### 3. 伝達遅延時間 (t<sub>PD</sub>)

ここで示す計算式は、簡易的に計算するための概略計算式です。この計算式では特に負荷が次の条件を満足する範囲での算出結果が比較的精度よく求められるようになっていました。負荷容量が大きいほど誤差が大きくなり、シミュレータの結果より小さい値を算出します。あらかじめ、ご承知のうえ目安としてご利用ください。

**条件** 遅延計算対象ブロックの前段F/Iの合計が、前段の駆動ブロックF/O制限の15%以内である。



ブロックBが遅延計算対象のブロックとするとブロックAの出力に接続されるF/Iの合計がブロックAのF/O制限15%以内のとき、簡易計算式の精度が高い。

#### 3.1 伝達遅延時間の概算式

##### 3.1.1 入力バッファと内部ファンクション・ブロックの遅延時間

入力バッファと内部ファンクション・ブロックの遅延時間は、メモリ・ブロックを含み、そのブロックに接続されている負荷（ファンアウト数）とその配線長（配線容量）から概算できます。

$$t_{PD} = t_{LD0} + (\Sigma F/O + L) \times t_1 \quad (\text{ns})$$

- $t_{LD0}$  : F/O = 0, L = 0におけるブロック自身の遅延時間  
 $\Sigma F/O$  : 該当出力端子のファンアウト数  
L : 該当出力端子の配線容量 (3.1.3 予測配線容量参照)  
 $t_1$  : 該当出力端子の遅延係数

##### 3.1.2 出力バッファの遅延時間

出力バッファの遅延時間は、その出力端子に接続されている負荷容量によって大きく変わります。また、遅延時間の負荷容量依存性はそのバッファ駆動能力によっても変わります。

出力バッファの遅延時間 (t<sub>PD</sub>) は、負荷容量 (C<sub>L</sub>) に対して次の公式で概算できます。

$$t_{PD} = t_{LD0} + T \times C_L \quad (\text{ns})$$

- $t_{LD0}$  : 基準遅延時間 (ns)  
T : 遅延係数  
C<sub>L</sub> : 負荷容量 (pF) (ただし, C<sub>L</sub> 15 pF)

なお、入出力バッファの遅延時間は、次の条件下で求められています。

CMOSレベル・インタフェース : スレッシユホールド電圧 = 1/2 V<sub>DD</sub>

### 3.1.3 予測配線容量

CMOS-N5ファミリの予測配線容量は次のようになります。

#### 予測配線容量（配線長をFan-in値に換算）

(1/2)

品名	ピンペア数					
	1	2	3	4	5	6
μ PD65880	1.621	3.266	4.911	6.556	8.200	9.845
μ PD65881	1.641	3.356	5.070	6.785	8.500	10.214
μ PD65882	1.684	3.552	5.421	7.289	9.158	11.027
μ PD65883	1.730	3.767	5.803	7.840	9.876	11.913
μ PD65884	1.757	3.892	6.026	8.161	10.295	12.430
μ PD65885	1.780	3.997	6.213	8.430	10.647	12.863
μ PD65887	1.819	4.175	6.532	8.889	11.245	13.602
μ PD65889	1.861	4.372	6.883	9.393	11.904	14.414
μ PD65890	1.904	4.569	7.233	9.897	12.562	15.226
μ PD65893	1.943	4.747	7.552	10.356	13.160	15.965

(2/2)

品名	ピンペア数					
	7	8	9	10	11 to 15	16 to 20
μ PD65880	11.490	13.135	14.779	16.424	24.648	32.871
μ PD65881	11.929	13.644	15.358	17.073	25.647	34.220
μ PD65882	12.895	14.764	16.632	18.501	27.844	37.187
μ PD65883	13.949	15.986	18.022	20.059	30.241	40.424
μ PD65884	14.564	16.699	18.833	20.967	31.640	42.312
μ PD65885	15.080	17.297	19.513	21.730	32.813	43.897
μ PD65887	15.958	18.315	20.672	23.028	34.811	46.594
μ PD65889	16.925	19.435	21.946	24.456	37.009	49.561
μ PD65890	17.891	20.555	23.220	25.884	39.206	52.528
μ PD65893	18.769	21.574	24.378	27.182	41.204	55.226

## 4. 入力インタフェース・レベル

次の4種類の入力インタフェース・レベルを用意してあります。用途に合わせて最適なものを選択してください。

- (1) CMOS レベル入力
- (2) TTL レベル入力
- (3) CMOS シュミット入力
- (4) TTL シュミット入力

## 5. 出力駆動能力

次のような出力駆動能力が異なるバッファを多数用意していますので、用途にあわせて最適なものを選択してください。

CMOS レベル出力 (6 種類) : 3.0 mA, 6.0 mA, 9.0 mA, 12.0 mA, 18.0 mA, 24.0 mA

## 6. 高性能バッファ

### 6.1 プルアップ/プルダウン抵抗付きバッファ

入力/出力/双方向バッファに次のようなプルアップ抵抗付き、プルダウン抵抗付きのものを用意しています。用途にあわせて最適なものを選択してください。

- (1) プルアップ抵抗 : 50 k $\Omega$  (TYP)
- (2) プルダウン抵抗 : 50 k $\Omega$  (TYP)
- (3) プルアップ抵抗 : 5 k $\Omega$  (TYP)

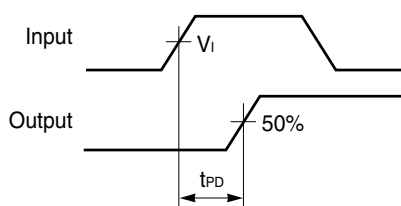
### 6.2 ロウ・スルーレート・バッファ

スルーレートを低くし、ロウ・ノイズ化を図った出力/双方向バッファを用意しており、ロウ・スルーレート・バッファと呼びます。なお、このマニュアルではLow-noiseと表示します。

## 7. 伝達遅延時間の定義

入力/出力バッファの伝達遅延時間は、次の定義による値を記載しています。

### (1) 入力バッファ

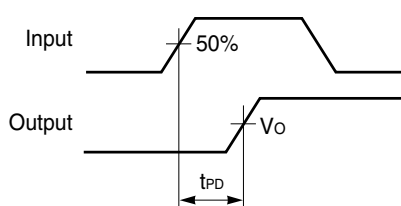


$V_I = 2.5 \text{ V}$  (CMOSレベル)

$V_I = 1.5 \text{ V}$  (TTLレベル)

(内部電圧幅)  $\times 50\%$

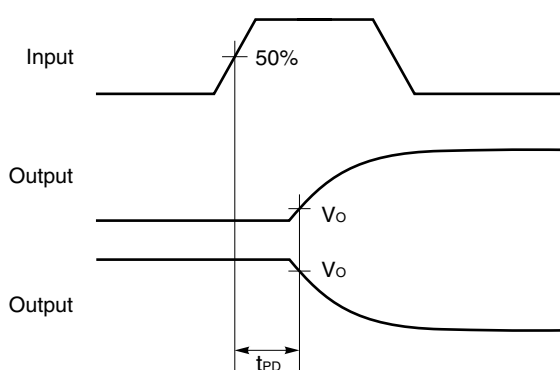
### (2) 出力バッファ (L H, H L, Z H (初期 $V_O = \text{“L”}$ レベル), Z L (初期 $V_O = \text{“H”}$ レベル))



(内部電圧幅)  $\times 50\%$

$V_O = 2.5 \text{ V}$  (CMOSレベル)

### (3) 出力バッファ (L Z, H Z)



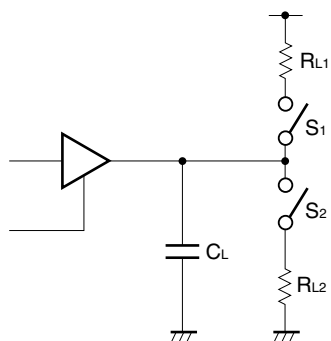
(内部電圧幅)  $\times 50\%$

$V_O = 0.1 \times V_{DD}$  (L Z)

$V_O = 1.2 \times V_{DD}$  (H Z)

## 8. 測定負荷条件

### CMOS レベル出力バッファ



#### (a) 通常出力バッファ

$R_{L1}, R_{L2} = \infty, C_L = 15 \text{ pF}$

( $S_1, S_2$  : OFF)

#### (b) 3ステート出力バッファ

$R_{L1} = 2 \text{ k}\Omega, R_{L2} = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$

$t_{P(HH)}, t_{P(LL)} : S_1 = \text{OFF}, S_2 = \text{OFF}$

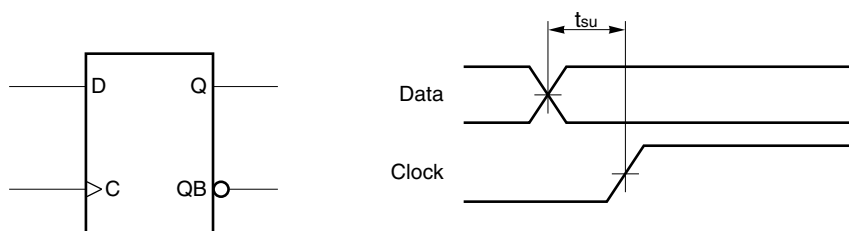
$t_{P(ZL)}, t_{P(LZ)} : S_1 = \text{ON}, S_2 = \text{OFF}$

$t_{P(ZH)}, t_{P(HZ)} : S_1 = \text{OFF}, S_2 = \text{ON}$

## 9. タイミング

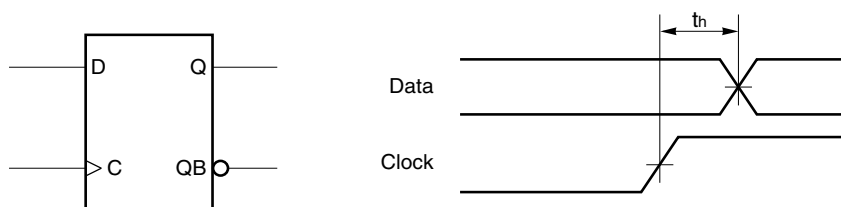
### (1) セットアップ・タイム ( $t_{su}$ )

D-F/Fなどで、クロックが変化する前にデータ信号が確定していなければならない時間。



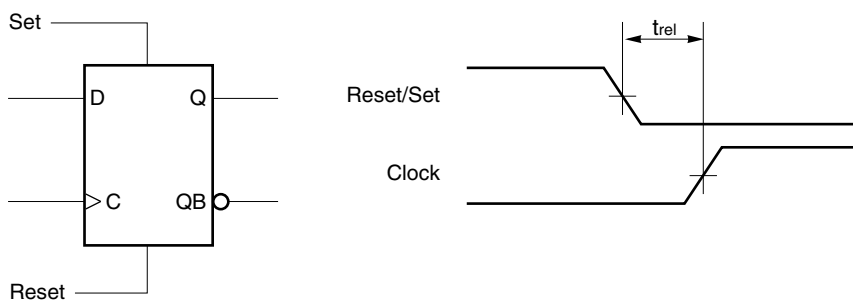
### (2) ホールド・タイム ( $t_h$ )

D-F/Fなどで、クロックが変化したあとにデータ信号を保持していなければならない時間。



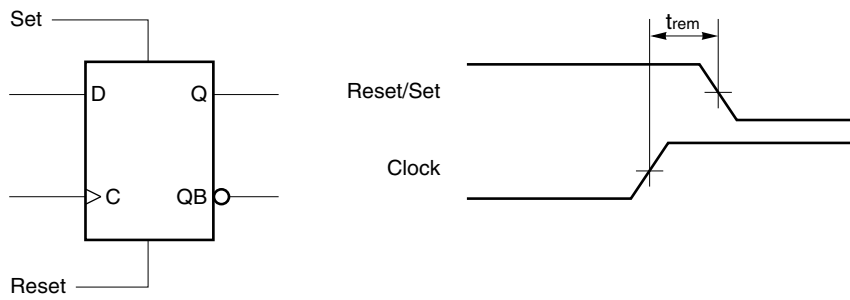
### (3) リリース・タイム ( $t_{rel}$ )

D-F/Fなどで、リセットかセットが解除になってからクロックが有効になるまでの時間。



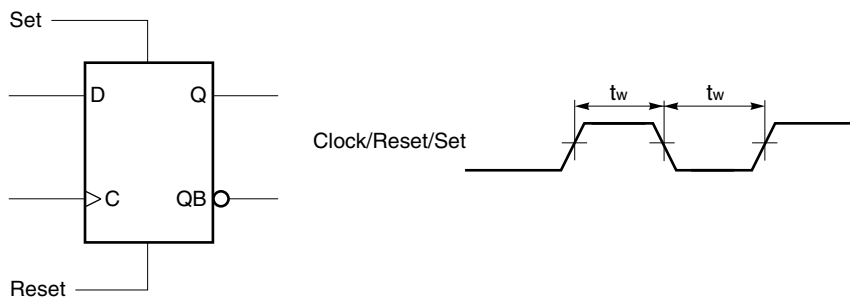
#### (4) リムーバル・タイム ( $t_{rem}$ )

D-F/Fなどで、クロックを無効にするまでのセットまたはリセットの保持時間。



#### (5) 最小パルス幅 ( $t_w$ )

D-F/Fなどで、データを正常に読み込むために必要となるクロック、リセット、セットのパルス幅の最小時間。





## 関連資料

関連資料は暫定版の場合もありますが、この資料では [ 暫定 ] の表示をしておりません。あらかじめご了承ください。

CMOS-N5 ファミリ 設計マニュアル	: A13826J
CMOS-N5 ファミリ 設計マニュアル メガマクロ編	: A14759J
CMOS-N5 Family ( 3.3 V ) Block Library	: A15895J
CMOS-N5 Family ( 5.0 V ) Block Library	: このマニュアル
CMOS-N5 Family Memory Block Library	: A14683J
テスト容易化設計 ユーザーズ・マニュアル	: A14357J
半導体総合セレクション・ガイド -製品・パッケージ情報-	: X13769J

設計する際は最新の資料を使用させていただくため、NEC販売担当または  
特約店にご確認ください。

# Contents

## Chapter 1 Interface Block

### 1.1 CMOS Level

Function	Block	Description	Cells (I/O)	Page
Input Buffer	FI01	-	3 (1)	1-4
	FID1	50k $\Omega$ Pull-down	3 (1)	
	FIU1	50k $\Omega$ Pull-up	3 (1)	
	FIW1	5k $\Omega$ Pull-up	3 (1)	
	FIS1W	Schmitt	6 (1)	
	FDS1W	Schmitt 50k $\Omega$ Pull-down	6 (1)	
	FUS1W	Schmitt 50k $\Omega$ Pull-up	6 (1)	
	FWS1W	Schmitt 5k $\Omega$ Pull-up	6 (1)	
Input Buffer with failsafe	FIA1	-	3 (1)	1-6
	FDA1	50k $\Omega$ Pull-down	3 (1)	
	FIE1W	Schmitt	6 (1)	
	FDE1W	Schmitt 50k $\Omega$ Pull-down	6 (1)	
Input Buffer with EN(AND)	FN11	-	6 (1)	1-8
	FN21	50k $\Omega$ Pull-down	6 (1)	
Input Buffer with EN(OR)	FN13	-	4 (1)	1-10
	FN23	50k $\Omega$ Pull-down	4 (1)	
Output Buffer	FO09	3mA	4 (1)	1-12
	FO04	6mA	4 (1)	
	FO01	9mA	4 (1)	
	FO02	12mA	12 (1)	
	FO03	18mA	12 (1)	
	FO06	24mA	12 (1)	
Low-noise Output Buffer	FE09	3mA	5 (1)	1-14
	FE04	6mA	5 (1)	
	FE01	9mA	5 (1)	
	FE02	12mA	5 (1)	
	FE03	18mA	5 (1)	
	FE06	24mA	5 (1)	

Function	Block	Description	Cells (I/O)	Page
3-State Buffer	B00T	3mA	7 (1)	1-16
	B0DT	3mA 50kΩ Pull-down	7 (1)	
	B0UT	3mA 50kΩ Pull-up	7 (1)	
	B0WT	3mA 5kΩ Pull-up	7 (1)	
	B00E	6mA	7 (1)	
	B0DE	6mA 50kΩ Pull-down	7 (1)	
	B0UE	6mA 50kΩ Pull-up	7 (1)	
	B0WE	6mA 5kΩ Pull-up	7 (1)	
	B008	9mA	7 (1)	
	B0D8	9mA 50kΩ Pull-down	7 (1)	
	B0U8	9mA 50kΩ Pull-up	7 (1)	
	B0W8	9mA 5kΩ Pull-up	7 (1)	
	B007	12mA	17 (1)	
	B0D7	12mA 50kΩ Pull-down	17 (1)	
	B0U7	12mA 50kΩ Pull-up	17 (1)	
	B0W7	12mA 5kΩ Pull-up	17 (1)	
	B009	18mA	17 (1)	
	B0D9	18mA 50kΩ Pull-down	17 (1)	
	B0U9	18mA 50kΩ Pull-up	17 (1)	
	B0W9	18mA 5kΩ Pull-up	17 (1)	
	B00H	24mA	17 (1)	
	B0DH	24mA 50kΩ Pull-down	17 (1)	
	B0UH	24mA 50kΩ Pull-up	17 (1)	
	B0WH	24mA 5kΩ Pull-up	17 (1)	

Function	Block	Description	Cells (I/O)	Page
Low-noise 3-State Buffer	BE0T	3mA	7 (1)	1-20
	BEDT	3mA 50kΩ Pull-down	7 (1)	
	BEUT	3mA 50kΩ Pull-up	7 (1)	
	BEWT	3mA 5kΩ Pull-up	7 (1)	
	BE0E	6mA	7 (1)	
	BEDE	6mA 50kΩ Pull-down	7 (1)	
	BEUE	6mA 50kΩ Pull-up	7 (1)	
	BEWE	6mA 5kΩ Pull-up	7 (1)	
	BE08	9mA	7 (1)	
	BED8	9mA 50kΩ Pull-down	7 (1)	
	BEU8	9mA 50kΩ Pull-up	7 (1)	
	BEW8	9mA 5kΩ Pull-up	7 (1)	
	BE07	12mA	7 (1)	
	BED7	12mA 50kΩ Pull-down	7 (1)	
	BEU7	12mA 50kΩ Pull-up	7 (1)	
	BEW7	12mA 5kΩ Pull-up	7 (1)	
	BE09	18mA	7 (1)	
	BED9	18mA 50kΩ Pull-down	7 (1)	
	BEU9	18mA 50kΩ Pull-up	7 (1)	
	BEW9	18mA 5kΩ Pull-up	7 (1)	
BE0H	24mA	7 (1)		
BEDH	24mA 50kΩ Pull-down	7 (1)		
BEUH	24mA 50kΩ Pull-up	7 (1)		
BEWH	24mA 5kΩ Pull-up	7 (1)		
N-ch open drain Buffer	EXT1	9mA	4 (1)	1-24
	EXT3	9mA 50kΩ Pull-up	4 (1)	
	EXW3	9mA 5kΩ Pull-up	4 (1)	
	EXT9	12mA	4 (1)	
	EXTB	12mA 50kΩ Pull-up	4 (1)	
	EXWB	12mA 5kΩ Pull-up	4 (1)	
	EXT5	18mA	4 (1)	
	EXT7	18mA 50kΩ Pull-up	4 (1)	
	EXW7	18mA 5kΩ Pull-up	4 (1)	
	EXTD	24mA	4 (1)	
	EXTF	24mA 50kΩ Pull-up	4 (1)	
	EXWF	24mA 5kΩ Pull-up	4 (1)	
N-ch open drain Buffer with failsafe	EXO1	9mA	4 (1)	1-26
	EXO9	12mA	4 (1)	
	EXO5	18mA	4 (1)	
	EXOD	24mA	4 (1)	

Function	Block	Description	Cells (I/O)	Page
I/O Buffer	B00U	3mA	10 (1)	1-28
	B0DU	3mA 50k $\Omega$ Pull-down	10 (1)	
	B0UU	3mA 50k $\Omega$ Pull-up	10 (1)	
	B0WU	3mA 5k $\Omega$ Pull-up	10 (1)	
	B00C	6mA	10 (1)	
	B0DC	6mA 50k $\Omega$ Pull-down	10 (1)	
	B0UC	6mA 50k $\Omega$ Pull-up	10 (1)	
	B0WC	6mA 5k $\Omega$ Pull-up	10 (1)	
	B003	9mA	10 (1)	
	B0D3	9mA 50k $\Omega$ Pull-down	10 (1)	
	B0U3	9mA 50k $\Omega$ Pull-up	10 (1)	
	B0W3	9mA 5k $\Omega$ Pull-up	10 (1)	
	B001	12mA	20 (1)	
	B0D1	12mA 50k $\Omega$ Pull-down	20 (1)	
	B0U1	12mA 50k $\Omega$ Pull-up	20 (1)	
	B0W1	12mA 5k $\Omega$ Pull-up	20 (1)	
	B005	18mA	20 (1)	
	B0D5	18mA 50k $\Omega$ Pull-down	20 (1)	
	B0U5	18mA 50k $\Omega$ Pull-up	20 (1)	
	B0W5	18mA 5k $\Omega$ Pull-up	20 (1)	
	B00F	24mA	20 (1)	
	B0DF	24mA 50k $\Omega$ Pull-down	20 (1)	
	B0UF	24mA 50k $\Omega$ Pull-up	20 (1)	
	B0WF	24mA 5k $\Omega$ Pull-up	20 (1)	

Function	Block	Description	Cells (I/O)	Page
Low-noise I/O Buffer	BE0U	3mA	10 (1)	1-34
	BEDU	3mA 50kΩ Pull-down	10 (1)	
	BEUU	3mA 50kΩ Pull-up	10 (1)	
	BEWU	3mA 5kΩ Pull-up	10 (1)	
	BE0C	6mA	10 (1)	
	BEDC	6mA 50kΩ Pull-down	10 (1)	
	BEUC	6mA 50kΩ Pull-up	10 (1)	
	BEWC	6mA 5kΩ Pull-up	10 (1)	
	BE03	9mA	10 (1)	
	BED3	9mA 50kΩ Pull-down	10 (1)	
	BEU3	9mA 50kΩ Pull-up	10 (1)	
	BEW3	9mA 5kΩ Pull-up	10 (1)	
	BE01	12mA	10 (1)	
	BED1	12mA 50kΩ Pull-down	10 (1)	
	BEU1	12mA 50kΩ Pull-up	10 (1)	
	BEW1	12mA 5kΩ Pull-up	10 (1)	
	BE05	18mA	10 (1)	
	BED5	18mA 50kΩ Pull-down	10 (1)	
	BEU5	18mA 50kΩ Pull-up	10 (1)	
	BEW5	18mA 5kΩ Pull-up	10 (1)	
	BE0F	24mA	10 (1)	
	BEDF	24mA 50kΩ Pull-down	10 (1)	
	BEUF	24mA 50kΩ Pull-up	10 (1)	
	BEWF	24mA 5kΩ Pull-up	10 (1)	

Function	Block	Description	Cells (I/O)	Page
Schmitt I/O Buffer	BSIUW	3mA	13 (1)	1-40
	BSDUW	3mA 50k $\Omega$ Pull-down	13 (1)	
	BSUUW	3mA 50k $\Omega$ Pull-up	13 (1)	
	BSWUW	3mA 5k $\Omega$ Pull-up	13 (1)	
	BSICW	6mA	13 (1)	
	BSDCW	6mA 50k $\Omega$ Pull-down	13 (1)	
	BSUCW	6mA 50k $\Omega$ Pull-up	13 (1)	
	BSWCW	6mA 5k $\Omega$ Pull-up	13 (1)	
	BSI3W	9mA	13 (1)	
	BSD3W	9mA 50k $\Omega$ Pull-down	13 (1)	
	BSU3W	9mA 50k $\Omega$ Pull-up	13 (1)	
	BSW3W	9mA 5k $\Omega$ Pull-up	13 (1)	
	BSI1W	12mA	23 (1)	
	BSD1W	12mA 50k $\Omega$ Pull-down	23 (1)	
	BSU1W	12mA 50k $\Omega$ Pull-up	23 (1)	
	BSW1W	12mA 5k $\Omega$ Pull-up	23 (1)	
	BSI5W	18mA	23 (1)	
	BSD5W	18mA 50k $\Omega$ Pull-down	23 (1)	
	BSU5W	18mA 50k $\Omega$ Pull-up	23 (1)	
	BSW5W	18mA 5k $\Omega$ Pull-up	23 (1)	
	BSIFW	24mA	23 (1)	
	BSDFW	24mA 50k $\Omega$ Pull-down	23 (1)	
	BSUFW	24mA 50k $\Omega$ Pull-up	23 (1)	
	BSWFW	24mA 5k $\Omega$ Pull-up	23 (1)	

Function	Block	Description	Cells (I/O)	Page
Low-noise Schmitt I/O Buffer	BFIUW	3mA	13 (1)	1-46
	BFDUW	3mA 50kΩ Pull-down	13 (1)	
	BFUJW	3mA 50kΩ Pull-up	13 (1)	
	BFWUW	3mA 5kΩ Pull-up	13 (1)	
	BFICW	6mA	13 (1)	
	BFDCW	6mA 50kΩ Pull-down	13 (1)	
	BFUCW	6mA 50kΩ Pull-up	13 (1)	
	BFWCW	6mA 5kΩ Pull-up	13 (1)	
	BFI3W	9mA	13 (1)	
	BFD3W	9mA 50kΩ Pull-down	13 (1)	
	BFU3W	9mA 50kΩ Pull-up	13 (1)	
	BFW3W	9mA 5kΩ Pull-up	13 (1)	
	BFI1W	12mA	13 (1)	
	BFD1W	12mA 50kΩ Pull-down	13 (1)	
	BFU1W	12mA 50kΩ Pull-up	13 (1)	
	BFW1W	12mA 5kΩ Pull-up	13 (1)	
	BFI5W	18mA	13 (1)	
	BFD5W	18mA 50kΩ Pull-down	13 (1)	
	BFU5W	18mA 50kΩ Pull-up	13 (1)	
	BFW5W	18mA 5kΩ Pull-up	13 (1)	
	BFIFW	24mA	13 (1)	
	BDFFW	24mA 50kΩ Pull-down	13 (1)	
	BFUFW	24mA 50kΩ Pull-up	13 (1)	
BFWFW	24mA 5kΩ Pull-up	13 (1)		
I/O Buffer with EN(AND)	BN2U	3mA	13 (1)	1-52
	BN4U	3mA 50kΩ Pull-down	13 (1)	
	BN2C	6mA	13 (1)	
	BN4C	6mA 50kΩ Pull-down	13 (1)	
	BN23	9mA	13 (1)	
	BN43	9mA 50kΩ Pull-down	13 (1)	
	BN21	12mA	23 (1)	
	BN41	12mA 50kΩ Pull-down	23 (1)	
	BN25	18mA	23 (1)	
	BN45	18mA 50kΩ Pull-down	23 (1)	
	BN2F	24mA	23 (1)	
	BN4F	24mA 50kΩ Pull-down	23 (1)	



Function	Block	Description	Cells (I/O)	Page
I/O Buffer with EN(OR)	BN3U	3mA	11 (1)	1-56
	BN5U	3mA 50kΩ Pull-down	11 (1)	
	BN3C	6mA	11 (1)	
	BN5C	6mA 50kΩ Pull-down	11 (1)	
	BN33	9mA	11 (1)	
	BN53	9mA 50kΩ Pull-down	11 (1)	
	BN31	12mA	21 (1)	
	BN51	12mA 50kΩ Pull-down	21 (1)	
	BN35	18mA	21 (1)	
	BN55	18mA 50kΩ Pull-down	21 (1)	
	BN3F	24mA	21 (1)	
	BN5F	24mA 50kΩ Pull-down	21 (1)	

## 1.2 TTL Level

Function	Block	Description	Cells (I/O)	Page
Input Buffer	FI02	-	3 (1)	1-64
	FID2	50kΩ Pull-down	3 (1)	
	FIU2	50kΩ Pull-up	3 (1)	
	FIW2	5kΩ Pull-up	3 (1)	
	FIS2W	Schmitt	6 (1)	
	FDS2W	Schmitt 50kΩ Pull-down	6 (1)	
	FUS2W	Schmitt 50kΩ Pull-up	6 (1)	
	FWS2W	Schmitt 5kΩ Pull-up	6 (1)	
Input Buffer with failsafe	FIA2	-	3 (1)	1-66
	FDA2	50kΩ Pull-down	3 (1)	
	FIE2W	Schmitt	6 (1)	
	FDE2W	Schmitt 50kΩ Pull-down	6 (1)	
Input Buffer with EN(AND)	FN12	-	7 (1)	1-68
	FN22	50kΩ Pull-down	7 (1)	
Input Buffer with EN(OR)	FN14	-	4 (1)	1-70
	FN24	50kΩ Pull-down	4 (1)	

Function	Block	Description	Cells (I/O)	Page
I/O Buffer	B00V	3mA	10 (1)	1-72
	B0DV	3mA 50k $\Omega$ Pull-down	10 (1)	
	B0UV	3mA 50k $\Omega$ Pull-up	10 (1)	
	B0WV	3mA 5k $\Omega$ Pull-up	10 (1)	
	B00D	6mA	10 (1)	
	B0DD	6mA 50k $\Omega$ Pull-down	10 (1)	
	B0UD	6mA 50k $\Omega$ Pull-up	10 (1)	
	B0WD	6mA 5k $\Omega$ Pull-up	10 (1)	
	B004	9mA	10 (1)	
	B0D4	9mA 50k $\Omega$ Pull-down	10 (1)	
	B0U4	9mA 50k $\Omega$ Pull-up	10 (1)	
	B0W4	9mA 5k $\Omega$ Pull-up	10 (1)	
	B002	12mA	20 (1)	
	B0D2	12mA 50k $\Omega$ Pull-down	20 (1)	
	B0U2	12mA 50k $\Omega$ Pull-up	20 (1)	
	B0W2	12mA 5k $\Omega$ Pull-up	20 (1)	
	B006	18mA	20 (1)	
	B0D6	18mA 50k $\Omega$ Pull-down	20 (1)	
	B0U6	18mA 50k $\Omega$ Pull-up	20 (1)	
	B0W6	18mA 5k $\Omega$ Pull-up	20 (1)	
	B00G	24mA	20 (1)	
	B0DG	24mA 50k $\Omega$ Pull-down	20 (1)	
	B0UG	24mA 50k $\Omega$ Pull-up	20 (1)	
	B0WG	24mA 5k $\Omega$ Pull-up	20 (1)	

Function	Block	Description	Cells (I/O)	Page
Low-noise I/O Buffer	BE0V	3mA	10 (1)	1-78
	BEDV	3mA 50k $\Omega$ Pull-down	10 (1)	
	BEUV	3mA 50k $\Omega$ Pull-up	10 (1)	
	BEWV	3mA 5k $\Omega$ Pull-up	10 (1)	
	BE0D	6mA	10 (1)	
	BEDD	6mA 50k $\Omega$ Pull-down	10 (1)	
	BEUD	6mA 50k $\Omega$ Pull-up	10 (1)	
	BEWD	6mA 5k $\Omega$ Pull-up	10 (1)	
	BE04	9mA	10 (1)	
	BED4	9mA 50k $\Omega$ Pull-down	10 (1)	
	BEU4	9mA 50k $\Omega$ Pull-up	10 (1)	
	BEW4	9mA 5k $\Omega$ Pull-up	10 (1)	
	BE02	12mA	10 (1)	
	BED2	12mA 50k $\Omega$ Pull-down	10 (1)	
	BEU2	12mA 50k $\Omega$ Pull-up	10 (1)	
	BEW2	12mA 5k $\Omega$ Pull-up	10 (1)	
	BE06	18mA	10 (1)	
	BED6	18mA 50k $\Omega$ Pull-down	10 (1)	
	BEU6	18mA 50k $\Omega$ Pull-up	10 (1)	
	BEW6	18mA 5k $\Omega$ Pull-up	10 (1)	
	BE0G	24mA	10 (1)	
	BEDG	24mA 50k $\Omega$ Pull-down	10 (1)	
	BEUG	24mA 50k $\Omega$ Pull-up	10 (1)	
	BEWG	24mA 5k $\Omega$ Pull-up	10 (1)	

Function	Block	Description	Cells (I/O)	Page
Schmitt I/O Buffer	BSIVW	3mA	13 (1)	1-84
	BSDVW	3mA 50k $\Omega$ Pull-down	13 (1)	
	BSUVW	3mA 50k $\Omega$ Pull-up	13 (1)	
	BSWVW	3mA 5k $\Omega$ Pull-up	13 (1)	
	BSIDW	6mA	13 (1)	
	BSDDW	6mA 50k $\Omega$ Pull-down	13 (1)	
	BSUDW	6mA 50k $\Omega$ Pull-up	13 (1)	
	BSWDW	6mA 5k $\Omega$ Pull-up	13 (1)	
	BSI4W	9mA	13 (1)	
	BSD4W	9mA 50k $\Omega$ Pull-down	13 (1)	
	BSU4W	9mA 50k $\Omega$ Pull-up	13 (1)	
	BSW4W	9mA 5k $\Omega$ Pull-up	13 (1)	
	BSI2W	12mA	23 (1)	
	BSD2W	12mA 50k $\Omega$ Pull-down	23 (1)	
	BSU2W	12mA 50k $\Omega$ Pull-up	23 (1)	
	BSW2W	12mA 5k $\Omega$ Pull-up	23 (1)	
	BSI6W	18mA	23 (1)	
	BSD6W	18mA 50k $\Omega$ Pull-down	23 (1)	
	BSU6W	18mA 50k $\Omega$ Pull-up	23 (1)	
	BSW6W	18mA 5k $\Omega$ Pull-up	23 (1)	
	BSIGW	24mA	23 (1)	
	BSDGW	24mA 50k $\Omega$ Pull-down	23 (1)	
	BSUGW	24mA 50k $\Omega$ Pull-up	23 (1)	
BSWGW	24mA 5k $\Omega$ Pull-up	23 (1)		

Function	Block	Description	Cells (I/O)	Page
Low-noise Schmitt I/O Buffer	BF1VW	3mA	13 (1)	1-90
	BFDVW	3mA 50kΩ Pull-down	13 (1)	
	BFUVW	3mA 50kΩ Pull-up	13 (1)	
	BFWVW	3mA 5kΩ Pull-up	13 (1)	
	BF1DW	6mA	13 (1)	
	BFDDW	6mA 50kΩ Pull-down	13 (1)	
	BFUDW	6mA 50kΩ Pull-up	13 (1)	
	BFWDW	6mA 5kΩ Pull-up	13 (1)	
	BF14W	9mA	13 (1)	
	BFD4W	9mA 50kΩ Pull-down	13 (1)	
	BFU4W	9mA 50kΩ Pull-up	13 (1)	
	BFW4W	9mA 5kΩ Pull-up	13 (1)	
	BF12W	12mA	13 (1)	
	BFD2W	12mA 50kΩ Pull-down	13 (1)	
	BFU2W	12mA 50kΩ Pull-up	13 (1)	
	BFW2W	12mA 5kΩ Pull-up	13 (1)	
	BF16W	18mA	13 (1)	
	BFD6W	18mA 50kΩ Pull-down	13 (1)	
	BFU6W	18mA 50kΩ Pull-up	13 (1)	
	BFW6W	18mA 5kΩ Pull-up	13 (1)	
	BF1GW	24mA	13 (1)	
	BFDGW	24mA 50kΩ Pull-down	13 (1)	
	BFUGW	24mA 50kΩ Pull-up	13 (1)	
BFWGW	24mA 5kΩ Pull-up	13 (1)		
I/O Buffer with EN(AND)	BN2V	3mA	14 (1)	1-96
	BN4V	3mA 50kΩ Pull-down	14 (1)	
	BN2D	6mA	14 (1)	
	BN4D	6mA 50kΩ Pull-down	14 (1)	
	BN24	9mA	14 (1)	
	BN44	9mA 50kΩ Pull-down	14 (1)	
	BN22	12mA	24 (1)	
	BN42	12mA 50kΩ Pull-down	24 (1)	
	BN26	18mA	24 (1)	
	BN46	18mA 50kΩ Pull-down	24 (1)	
	BN2G	24mA	24 (1)	
	BN4G	24mA 50kΩ Pull-down	24 (1)	

Function	Block	Description	Cells (I/O)	Page
I/O Buffer with EN(OR)	BN3V	3mA	11 (1)	1-100
	BN5V	3mA 50k $\Omega$ Pull-down	11 (1)	
	BN3D	6mA	11 (1)	
	BN5D	6mA 50k $\Omega$ Pull-down	11 (1)	
	BN34	9mA	11 (1)	
	BN54	9mA 50k $\Omega$ Pull-down	11 (1)	
	BN32	12mA	21 (1)	
	BN52	12mA 50k $\Omega$ Pull-down	21 (1)	
	BN36	18mA	21 (1)	
	BN56	18mA 50k $\Omega$ Pull-down	21 (1)	
	BN3G	24mA	21 (1)	
	BN5G	24mA 50k $\Omega$ Pull-down	21 (1)	

### 1.3 Oscillator

Function	Block	Description	Cells (I/O)	Page
Oscillator Input Buffer	OSI1	-	0 (1)	1-108
Oscillator Input Buffer for Enable	OSI2	-	0 (1)	1-110
Oscillator Input Buffer for OSO9	OSI4	-	0 (1)	1-112
Oscillator Output Buffer (Internal Feedback Resistor)	OSO1	-	0 (1)	1-114
Oscillator Output Buffer (for Enable Type)	OSO7	-	0 (1)	1-116
Oscillator Output Buffer (External Feedback Resistor)	OSO9	-	0 (1)	1-118

## Chapter 2 Function Block

### 2.1 Level Generator

Function	Block	Description	Cells (I/O)	Page
H, L Level Generator	F091	-	1 (-)	2-4

### 2.2 Inverter, Buffer, CTS Driver, Delay Gate

Function	Block	Description	Cells (I/O)	Page
Inverter	L101	Single Out, Low Power	1 (-)	2-10
	F101	Single Out	1 (-)	
	F102	Single Out, x2-drive	2 (-)	
	F143	Single Out, x3-drive	3 (-)	
	F144	Single Out, x4-drive	4 (-)	
	F145	Single Out, x5-drive	5 (-)	
	F146	Single Out, x6-drive	6 (-)	
	F148	Single Out, x8-drive	12 (-)	
Buffer	L111	Single Out, Low Power	1 (-)	2-12
	F111	Single Out	2 (-)	
	F112	Single Out, x2-drive	3 (-)	
	F153	Single Out, x3-drive	4 (-)	
	F154	Single Out, x4-drive	5 (-)	
	F158	Single Out, x8-drive	11 (-)	
CTS Driver (Inverter Type)	FC42	Single type	132 (-)	2-14
	FC82	Single type, x2-drive	396 (-)	
	FC44	Double type	340 (-)	
	FC84	Double type, x2-drive	1020 (-)	
Delay Gate	F131	-	6 (-)	2-16
	F132	-	10 (-)	

## 2.3 OR(NOR)

Function	Block	Description	Cells (I/O)	Page
2-Input NOR	L202	Low Power	1 (-)	2-22
	F202	-	2 (-)	
	F222	x2-drive	4 (-)	
	F282	x4-drive	6 (-)	
3-Input NOR	L203	Low Power	2 (-)	2-24
	F203	-	3 (-)	
	F223	x2-drive	6 (-)	
4-Input NOR	L204	Low Power	2 (-)	2-26
	F204	-	4 (-)	
5-Input NOR	L205	Low Power	4 (-)	2-28
	F205	-	5 (-)	
	F225	x2-drive	6 (-)	
6-Input NOR	F206	-	5 (-)	2-30
	F226	x2-drive	6 (-)	
8-Input NOR	L208	Low Power	7 (-)	2-32
	F208	-	7 (-)	
	F228	x2-drive	8 (-)	
2-Input OR	L212	Low Power	2 (-)	2-34
	F212	-	2 (-)	
	F232	x2-drive	3 (-)	
	F252	x4-drive	6 (-)	
3-Input OR	L213	Low Power	2 (-)	2-36
	F213	-	3 (-)	
	F233	x2-drive	4 (-)	
4-Input OR	L214	Low Power	3 (-)	2-38
	F214	-	3 (-)	
	F234	x2-drive	4 (-)	
5-Input OR	L215	Low Power	4 (-)	2-40
	F215	-	5 (-)	
	F235	x2-drive	7 (-)	
6-Input OR	L216	Low Power	4 (-)	2-42
	F216	-	5 (-)	
	F236	x2-drive	7 (-)	
8-Input OR	L218	Low Power	6 (-)	2-44
	F218	-	8 (-)	
	F238	x2-drive	9 (-)	



## 2.4 AND(NAND)

Function	Block	Description	Cells (I/O)	Page
2-Input NAND	L302	Low Power	1 (-)	2-50
	F302	-	2 (-)	
	F322	x2-drive	4 (-)	
	F382	x4-drive	6 (-)	
3-Input NAND	L303	Low Power	2 (-)	2-52
	F303	-	3 (-)	
	F323	x2-drive	6 (-)	
4-Input NAND	L304	Low Power	2 (-)	2-54
	F304	-	4 (-)	
	F324	x2-drive	8 (-)	
5-Input NAND	F305	-	5 (-)	2-56
	F325	x2-drive	6 (-)	
6-Input NAND	F306	-	5 (-)	2-58
	F326	x2-drive	6 (-)	
8-Input NAND	F308	-	6 (-)	2-60
	F328	x2-drive	7 (-)	
2-Input AND	L312	Low Power	2 (-)	2-62
	F312	-	2 (-)	
	F332	x2-drive	3 (-)	
	F352	x4-drive	6 (-)	
3-Input AND	L313	Low Power	2 (-)	2-64
	F313	-	3 (-)	
	F333	x2-drive	4 (-)	
4-Input AND	L314	Low Power	3 (-)	2-66
	F314	-	3 (-)	
	F334	x2-drive	4 (-)	
5-Input AND	L315	Low Power	4 (-)	2-68
	F315	-	5 (-)	
	F335	x2-drive	7 (-)	
6-Input AND	L316	Low Power	4 (-)	2-70
	F316	-	5 (-)	
	F336	x2-drive	7 (-)	
8-Input AND	L318	Low Power	5 (-)	2-72
	F318	-	6 (-)	
	F338	x2-drive	8 (-)	

## 2.5 AND-NOR

Function	Block	Description	Cells (I/O)	Page
1-2-Input AND-NOR	L421	Low Power	2 (-)	2-78
	F421	-	3 (-)	
1-1-2-Input AND-NOR	L422	Low Power	2 (-)	2-80
	F422	-	4 (-)	
1-3-Input AND-NOR	L423	Low Power	2 (-)	2-82
	F423	-	4 (-)	
2-2-Input AND-NOR	L424	Low Power	2 (-)	2-84
	F424	-	4 (-)	
2-2-2-Input AND-NOR	L425	Low Power	3 (-)	2-86
	F425	-	6 (-)	
2-3-Input AND-NOR	L427	Low Power	3 (-)	2-88
	F427	-	5 (-)	
1-2-2-Input AND-NOR	L428	Low Power	3 (-)	2-90
	F428	-	5 (-)	
2-2-2-2-Input AND-NOR	L429	Low Power	6 (-)	2-92
	F429	-	6 (-)	
1-4-Input AND-NOR	L440	Low Power	3 (-)	2-94
	F440	-	5 (-)	
1-5-Input AND-NOR	L441	Low Power	5 (-)	2-96
	F441	-	7 (-)	
4-4-4-Input AND-NOR	L444	Low Power	8 (-)	2-98
	F444	-	8 (-)	
1-1-1-2-Input AND-NOR	L446	Low Power	4 (-)	2-100
	F446	-	5 (-)	
1-1-1-3-Input AND-NOR	L447	Low Power	5 (-)	2-102
	F447	-	5 (-)	
1-1-2-2-Input AND-NOR	L448	Low Power	5 (-)	2-104
	F448	-	5 (-)	
3-3-3-3-Input AND-NOR	F449	-	8 (-)	2-106
3-3-3-Input AND-NOR	L460	Low Power	6 (-)	2-108
	F460	-	7 (-)	
1-2-3-Input AND-NOR	F462	-	6 (-)	2-110
1-1-3-Input AND-NOR	L463	Low Power	3 (-)	2-112
	F463	-	5 (-)	
1-1-4-Input AND-NOR	L464	Low Power	5 (-)	2-114
	F464	-	5 (-)	
1-1-1-1-2-Input AND-NOR	F465	-	5 (-)	2-116
4-4-4-4-Input AND-NOR	F466	-	10 (-)	2-118

## 2.6 OR-NAND

Function	Block	Description	Cells (I/O)	Page
1-4-Input OR-NAND	L430	Low Power	4 (-)	2-124
	F430	-	5 (-)	
1-2-Input OR-NAND	L431	Low Power	2 (-)	2-126
	F431	-	3 (-)	
1-1-2-Input OR-NAND	L432	Low Power	2 (-)	2-128
	F432	-	4 (-)	
1-3-Input OR-NAND	L433	Low Power	2 (-)	2-130
	F433	-	4 (-)	
2-2-Input OR-NAND	L434	Low Power	2 (-)	2-132
	F434	-	4 (-)	
2-3-Input OR-NAND	F435	-	5 (-)	2-134
3-3-Input OR-NAND	L436	Low Power	3 (-)	2-136
	F436	-	6 (-)	
1-2-2-Input OR-NAND	F437	-	5 (-)	2-138
2-2-2-Input OR-NAND	F438	-	6 (-)	2-140
1-5-Input OR-NAND	L439	Low Power	5 (-)	2-142
	F439	-	6 (-)	
2-4-Input OR-NAND	L450	Low Power	5 (-)	2-144
	F450	-	6 (-)	
4-4-Input OR-NAND	L451	Low Power	7 (-)	2-146
	F451	-	8 (-)	
1-1-3-Input OR-NAND	L452	Low Power	4 (-)	2-148
	F452	-	5 (-)	
1-1-4-Input OR-NAND	L453	Low Power	5 (-)	2-150
	F453	-	6 (-)	
4-4-4-Input OR-NAND	F457	-	10 (-)	2-152
1-1-1-2-Input OR-NAND	L458	Low Power	3 (-)	2-154
	F458	-	5 (-)	
1-1-1-3-Input OR-NAND	L459	Low Power	5 (-)	2-156
	F459	-	5 (-)	
1-1-1-1-2-Input OR-NAND	F490	-	5 (-)	2-158
1-2-3-Input OR-NAND	L491	Low Power	5 (-)	2-160
	F491	-	5 (-)	
3-3-3-Input OR-NAND	L493	Low Power	6 (-)	2-162
	F493	-	7 (-)	
1-1-2-2-Input OR-NAND	F495	-	6 (-)	2-164
3-3-3-3-Input OR-NAND	F496	-	8 (-)	2-166
4-4-4-4-Input OR-NAND	F498	-	14 (-)	2-168

## 2.7 Exclusive OR, Exclusive NOR

Function	Block	Description	Cells (I/O)	Page
2-Input Exclusive OR	L511	Low Power	3 (-)	2-174
	F511	-	4 (-)	
3-Input Exclusive OR	L516	Low Power	6 (-)	2-176
	F516	-	7 (-)	
2-Input Exclusive NOR	L512	Low Power	3 (-)	2-178
	F512	-	4 (-)	
3-Input Exclusive NOR	L517	Low Power	7 (-)	2-180
	F517	-	7 (-)	

## 2.8 Adder, 3-State Buffer, Decoder, Multiplexer, Generator

Function	Block	Description	Cells (I/O)	Page
1-Bit Full Adder	F521	-	9 (-)	2-186
4-Bit Full Adder	F523	-	32 (-)	2-188
4-Bit Look Ahead Carry Generator	F526	-	34 (-)	2-192
4-Bit Carry Look Ahead Adder	F527	-	69 (-)	2-194
3-State Buffer	L531	with EN, Low Power	4 (-)	2-198
	F531	with EN	5 (-)	
	F533	with EN, x2-drive	7 (-)	
	F53F	with EN, x4-drive	11 (-)	
	L532	with ENB, Low Power	4 (-)	
	F532	with ENB	5 (-)	
	F534	with ENB, x2-drive	7 (-)	
	F53G	with ENB, x4-drive	11 (-)	
	F541	Inverter with EN	6 (-)	
	F543	Inverter with EN, x2-drive	8 (-)	
	F54F	Inverter with EN, x4-drive	12 (-)	
	F542	Inverter with ENB	6 (-)	
	F544	Inverter with ENB, x2-drive	8 (-)	
	F54G	Inverter with ENB, x4-drive	12 (-)	
2 to 4 Decoder	L560	Positive Out, Low Power	6 (-)	2-202
	F560	Positive Out	10 (-)	
	L561	Negative Out, Low Power	6 (-)	
	F561	Negative Out	10 (-)	
2 to 1 Multiplexer (Positive Out)	L565	Low Power	3 (-)	2-206
	F565	-	4 (-)	
	L571	with ENB, Low Power	4 (-)	
	F571	with ENB	6 (-)	
4 to 1 Multiplexer (Positive Out)	F564	-	8 (-)	2-208
	F570	with ENB	10 (-)	
8 to 1 Multiplexer (Positive Out)	F563	-	18 (-)	2-210
	F569	with ENB	18 (-)	
Quad 2 to 1 Multiplexer (Negative Out)	L572	with ENB, Low Power	15 (-)	2-214
	F572	with ENB	17 (-)	
8-Bit Odd Parity Generator	F581	-	19 (-)	2-218
8-Bit Even Parity Generator	F582	-	19 (-)	2-220

## 2.9 RS-Latch, RS-F/F

Function	Block	Description	Cells (I/O)	Page
RS-Latch	F595	-	5 (-)	2-226
RS-F/F with R, S	F596	-	11 (-)	2-228

## 2.10 D-Latch

Function	Block	Description	Cells (I/O)	Page
D-Latch	F601	-	6 (-)	2-234
	L601	Q Out, Low Power	4 (-)	
	F601NQ	Q Out	5 (-)	
	F601NB	QB Out	5 (-)	
D-Latch, High Speed	F6R1	-	6 (-)	2-236
D-Latch with R	F602	-	6 (-)	2-238
	L602	Q Out, Low Power	5 (-)	
	F602NQ	Q Out	6 (-)	
	F602NB	QB Out	5 (-)	
D-Latch with R, High Speed	F6R2	-	7 (-)	2-240
D-Latch with RB	F603	-	7 (-)	2-242
	L603	Q Out, Low Power	5 (-)	
	F603NQ	Q Out	5 (-)	
	F603NB	QB Out	6 (-)	
D-Latch with RB, High Speed	F6R5	-	6 (-)	2-244
D-Latch with SB	F60K	-	7 (-)	2-246
	F60KNQ	Q Out	6 (-)	
	F60KNB	QB Out	5 (-)	
D-Latch with RB, SB	F60J	-	7 (-)	2-248
	F60JNQ	Q Out	6 (-)	
	F60JNB	QB Out	6 (-)	
D-Latch (GB)	F604	-	6 (-)	2-252
	L604	Q Out, Low Power	4 (-)	
	F604NQ	Q Out	5 (-)	
	F604NB	QB Out	5 (-)	
D-Latch (GB), High Speed	F6R8	-	6 (-)	2-254
D-Latch (GB) with RB	F605	-	7 (-)	2-256
	L605	Q Out, Low Power	5 (-)	
	F605NQ	Q Out	5 (-)	
	F605NB	QB Out	6 (-)	
D-Latch (GB) with RB, High Speed	F6R9	-	6 (-)	2-258

## 2.11 D-F/F

Function	Block	Description	Cells (I/O)	Page
D-F/F	F641	-	8 (-)	2-264
	L641	Q Out, Low Power	6 (-)	
	F641NQ	Q Out	7 (-)	
	F641NB	QB Out	7 (-)	
D-F/F with R	F642	-	9 (-)	2-266
	F642NQ	Q Out	8 (-)	
	F642NB	QB Out	8 (-)	
D-F/F with S	F643	-	9 (-)	2-268
	F643NQ	Q Out	8 (-)	
	F643NB	QB Out	8 (-)	
D-F/F with R, S	F644	-	10 (-)	2-270
	L644	Q Out, Low Power	8 (-)	
	F644NQ	Q Out	9 (-)	
	F644NB	QB Out	9 (-)	
D-F/F with RB	F615	-	9 (-)	2-272
	L645	Q Out, Low Power	7 (-)	
	F615NQ	Q Out	8 (-)	
	F615NB	QB Out	8 (-)	
D-F/F with SB	F616	-	9 (-)	2-274
	F616NQ	Q Out	8 (-)	
	F616NB	QB Out	8 (-)	
D-F/F with RB, SB	F647	-	10 (-)	2-276
	L647	Q Out, Low Power	8 (-)	
	F647NQ	Q Out	9 (-)	
	F647NB	QB Out	9 (-)	
D-F/F (CB)	F661	-	8 (-)	2-278
	L661	Q Out, Low Power	6 (-)	
	F661NQ	Q Out	7 (-)	
	F661NB	QB Out	7 (-)	
D-F/F (CB) with RB	F665	-	9 (-)	2-280
	F665NQ	Q Out	8 (-)	
	F665NB	QB Out	8 (-)	
D-F/F (CB) with SB	F666	-	9 (-)	2-282
	F666NQ	Q Out	8 (-)	
	F666NB	QB Out	8 (-)	
D-F/F (CB) with RB, SB	F667	-	10 (-)	2-284
	L667	Q Out, Low Power	8 (-)	
	F667NQ	Q Out	9 (-)	
	F667NB	QB Out	9 (-)	
D-F/F with 2 to 1 Selector	F641S	-	10 (-)	2-286
	F641SQ	Q Out	9 (-)	
	F641SB	QB Out	9 (-)	

Function	Block	Description	Cells (I/O)	Page
D-F/F with R, 2 to 1 Selector	F642S	-	11 (-)	2-288
	F642SQ	Q Out	10 (-)	
	F642SB	QB Out	10 (-)	
D-F/F with S, 2 to 1 Selector	F643S	-	11 (-)	2-290
	F643SQ	Q Out	10 (-)	
	F643SB	QB Out	10 (-)	
D-F/F with R, S, 2 to 1 Selector	F644S	-	12 (-)	2-292
	F644SQ	Q Out	11 (-)	
	F644SB	QB Out	11 (-)	
D-F/F with RB, 2 to 1 Selector	F615S	-	11 (-)	2-294
	F615SQ	Q Out	10 (-)	
	F615SB	QB Out	10 (-)	
D-F/F with SB, 2 to 1 Selector	F616S	-	11 (-)	2-296
	F616SQ	Q Out	10 (-)	
	F616SB	QB Out	10 (-)	
D-F/F with RB, SB, 2 to 1 Selector	F647S	-	12 (-)	2-298
	F647SQ	Q Out	11 (-)	
	F647SB	QB Out	11 (-)	
D-F/F (CB) with 2 to 1 Selector	F661S	-	10 (-)	2-300
	F661SQ	Q Out	9 (-)	
	F661SB	QB Out	9 (-)	
D-F/F (CB) with RB, 2 to 1 Selector	F665S	-	11 (-)	2-302
	F665SQ	Q Out	10 (-)	
	F665SB	QB Out	10 (-)	
D-F/F (CB) with SB, 2 to 1 Selector	F666S	-	11 (-)	2-304
	F666SQ	Q Out	10 (-)	
	F666SB	QB Out	10 (-)	
D-F/F (CB) with RB, SB, 2 to 1 Selector	F667S	-	12 (-)	2-306
	F667SQ	Q Out	11 (-)	
	F667SB	QB Out	11 (-)	
D-F/F with Hold	F641H	-	10 (-)	2-308
	F641HQ	Q Out	9 (-)	
	F641HB	QB Out	9 (-)	
D-F/F with RB, Hold	F615H	-	11 (-)	2-310
	F615HQ	Q Out	10 (-)	
	F615HB	QB Out	10 (-)	
D-F/F with SB, Hold	F616H	-	11 (-)	2-312
	F616HQ	Q Out	10 (-)	
	F616HB	QB Out	10 (-)	
D-F/F with RB, SB, Hold	F647H	-	12 (-)	2-314
	F647HQ	Q Out	11 (-)	
	F647HB	QB Out	11 (-)	
D-F/F (CB) with 2 to 1 Selector(2 CTRL), RB	F673	-	11 (-)	2-316
D-F/F (CB) with Hold, 2 to 1 Selector(2 CTRL), RB	F674	-	12 (-)	2-318



## 2.12 T-F/F, JK-F/F

Function	Block	Description	Cells (I/O)	Page
T-F/F with R, S	F744	-	9 (-)	2-324
	L744	Q Out, Low Power	7 (-)	
	F744NQ	Q Out	8 (-)	
T-F/F with RB	F745	-	8 (-)	2-326
	F745NQ	Q Out	7 (-)	
T-F/F with RB, SB	F747	-	9 (-)	2-328
	L747	Q Out, Low Power	7 (-)	
	F747NQ	Q Out	8 (-)	
T-F/F with Data-Hold R, S	F791	-	12 (-)	2-330
T-F/F (TB) with RB	F765	-	8 (-)	2-332
	F765NQ	Q Out	7 (-)	
T-F/F (TB) with RB, SB	F767	-	9 (-)	2-334
	L767	Q Out, Low Power	7 (-)	
	F767NQ	Q Out	8 (-)	
T-F/F (TB) with Data-Hold RB, SB	F792	-	12 (-)	2-336
JK-F/F	F771	-	10 (-)	2-338
	F771NQ	Q Out	9 (-)	
	F771NB	QB Out	9 (-)	
JK-F/F, High Speed	F7D1	-	10 (-)	2-340
JK-F/F with R, S	F774	-	12 (-)	2-342
	F774NQ	Q Out	11 (-)	
	F774NB	QB Out	11 (-)	
JK-F/F with RB	F775	-	11 (-)	2-344
	F775NQ	Q Out	10 (-)	
	F775NB	QB Out	10 (-)	
JK-F/F with SB	F776	-	11 (-)	2-346
	F776NQ	Q Out	10 (-)	
	F776NB	QB Out	10 (-)	
JK-F/F with RB, SB	F777	-	12 (-)	2-348
	F777NQ	Q Out	11 (-)	
	F777NB	QB Out	11 (-)	
JK-F/F (CB)	F781	-	10 (-)	2-350
	F781NQ	Q Out	9 (-)	
	F781NB	QB Out	9 (-)	
JK-F/F (CB), High Speed	F7E1	-	10 (-)	2-352
JK-F/F (CB) with RB, SB	F787	-	12 (-)	2-354
	F787NQ	Q Out	11 (-)	
	F787NB	QB Out	11 (-)	

## Chapter 3 Scan Path Block

### 3.1 Standard Type

Function	Block	Description	Cells (I/O)	Page
Scan D-F/F with R, S, 2 to 1 Selector	S000	-	12 (-)	3-4
Scan D-F/F with 2 to 1 Selector	S002	-	10 (-)	3-6
Scan D-F/F with 2 to 1 Selector, High Speed	S003	-	11 (-)	3-8
Scan D-F/F with R, S, Hold, 2 to 1 Selector	S050	-	16 (-)	3-10
Scan D-F/F with Hold, 2 to 1 Selector	S052	-	14 (-)	3-12
Scan JK-F/F with R, S, D-F/F Function	S100	-	14 (-)	3-14
Scan JK-F/F with D-F/F Function	S102	-	12 (-)	3-16
Scan JK-F/F with R, S, Hold, D-F/F Function	S150	-	18 (-)	3-18
Scan JK-F/F with Hold, D-F/F Function	S152	-	16 (-)	3-20
Scan D-Latch with R, D-F/F Function	S201	-	13 (-)	3-22
Scan D-Latch with D-F/F Function	S202	-	12 (-)	3-24
Scan D-Latch with D-F/F Function, High Speed	S204	-	12 (-)	3-26
Scan D-Latch with R, Special Function, R	S301	-	8 (-)	3-28
Scan D-Latch with Special Function	S302	-	7 (-)	3-30
Scan D-Latch with Special Function, High Speed	S303	-	7 (-)	3-32

### 3.2 NEC Scan

Function	Block	Description	Cells (I/O)	Page
NEC Scan D-Latch	SE601	-	13 (-)	3-38
NEC Scan D-Latch with R	SE602	-	14 (-)	3-40
NEC Scan D-Latch with RB	SE603	-	14 (-)	3-42
NEC Scan D-Latch(GB)	SE604	-	13 (-)	3-44
NEC Scan D-Latch(GB) with RB	SE605	-	14 (-)	3-46
NEC Scan D-F/F	SE611	-	11 (-)	3-48
NEC Scan D-F/F with R, S	SE614	-	13 (-)	3-50
NEC Scan D-F/F with RB	SE615	-	12 (-)	3-52
NEC Scan D-F/F with SB	SE616	-	12 (-)	3-54
NEC Scan D-F/F with RB, SB	SE617	-	13 (-)	3-56
NEC Scan D-F/F (CB)	SE631	-	11 (-)	3-58
NEC Scan D-F/F (CB) with RB, SB	SE637	-	13 (-)	3-60

### 3.3 Scan Controller

Function	Block	Description	Cells (I/O)	Page
Clock Distributor	SCD1	-	8 (-)	3-66
Clock Distributor with Test (Positive Clock)	SCDC	-	2 (-)	3-68
Clock Distributor with Test (Negative Clock)	SCDD	-	2 (-)	3-70
I/F Control (AMC) with EN	SFEH	-	3 (-)	3-72
I/F Control (AMC) with ENB	SFEL	-	2 (-)	3-74
I/F Control (SMC) with EN	SOEH	-	3 (-)	3-76
I/F Control (SMC) with ENB	SOEL	-	2 (-)	3-78
Mega Macro Skip	SMS1	-	4 (-)	3-80
Set/Reset Control	SRH1	-	2 (-)	3-82
Set-B/Reset-B Control	SRL1	-	2 (-)	3-84
Loop Cut	SRPD	-	12 (-)	3-86
Clock Generator	SCKG	-	16 (-)	3-88
Common Input	SCI1	-	2 (-)	3-90
Common Output	SCO1	-	4 (-)	3-92
GND	SGND	-	2 (-)	3-94

## Chapter 4 Boundary Scan Block

### 4.1 TAP Macro

Function	Block	Description	Cells (I/O)	Page
BScan TAP Macro	SBCJ	-	262 (-)	4-4
BScan TAP Macro with NEC Scan	SBCL	-	315 (-)	4-6

### 4.2 Level Generator

Function	Block	Description	Cells (I/O)	Page
BScan Level Generator (CLANP)	SBZ1	-	1 (-)	4-12

### 4.3 Data Register

Function	Block	Description	Cells (I/O)	Page
BScan Data Register for Input	SVRNI2	-	12 (-)	4-18
BScan Data Register for Output	SVRN22	-	24 (-)	4-20
BScan Data Register for 3-state	SVRN32	-	50 (-)	4-22
BScan Data Register for Bid	SVRNB2	-	57 (-)	4-24

### 4.4 D-latch, Selector, Shift Register

Function	Block	Description	Cells (I/O)	Page
BScan D-Latch with SB Q Out, Low Power	L606	-	5 (-)	4-30
BScan Selector	SBD1	-	4 (-)	4-32
BScan Shift Register	SBR1	-	8 (-)	4-34
BScan Data Selector for Output	SVSNA2	-	7 (-)	4-36
BScan Data Selector for Bid	SVSNB2	-	7 (-)	4-38
BScan Data Enable Selector for 3-state	SVSNC2	-	9 (-)	4-40
BScan Data Enable Selector for Bid	SVSNE2	-	9 (-)	4-42

### 4.5 Soft Macro

Function	Block	Description	Cells (I/O)	Page
BScan TAP Controller	SBCK	-	392 (-)	4-48
BScan Instruction Register (Internal Circuit)	SBM4	-	46 (-)	4-50
BScan Instruction Register	SBM5	-	140 (-)	4-52
BScan Instruction Decoder	SBM6	-	24 (-)	4-54
BScan Instruction Decoder with NEC Scan	SBMC	-	37 (-)	4-56
BScan Bypass Register	SBS3	-	26 (-)	4-58

# **Chapter 1**

## **Interface Block**

## 1.1 CMOS Level

[MEMO]

Chapter 1 Interface Block

Function	Input Buffer					5.0 V	
Block type							
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
Normal	FI01	FID1	FIU1	FIW1	1	3	
Schmitt	FIS1W	FDS1W	FUS1W	FWS1W	1	6	
Clock							

Logic Diagram for "Normal"	Truth Table																			
	<table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>	A	Y	1	1	0	0													
A	Y																			
1	1																			
0	0																			
Logic Diagram for "Schmitt"	Block type																			
	<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FI01 to FIW1</td> <td>A</td> <td>-</td> <td>Y</td> <td>52</td> </tr> <tr> <td>FIS1W to FWS1W</td> <td>A</td> <td>-</td> <td>Y</td> <td>42</td> </tr> </tbody> </table>	Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FI01 to FIW1	A	-	Y	52	FIS1W to FWS1W	A	-	Y	42
Block type	Input		Output																	
	Symbol	Fan-In	Symbol	Fan-Out																
FI01 to FIW1	A	-	Y	52																
FIS1W to FWS1W	A	-	Y	42																
Logic Diagram for "Clock"																				

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FI01	A → Y	(HH)	0.160	0.236	0.452	0.007	0.010	0.014			
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
FID1	A → Y	(HH)	0.160	0.236	0.452	0.007	0.010	0.014			
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
FIU1	A → Y	(HH)	0.160	0.236	0.452	0.007	0.010	0.014			
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
FIW1	A → Y	(HH)	0.160	0.236	0.452	0.007	0.010	0.014			
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
FIS1W	A → Y	(HH)	0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)	0.901	1.332	2.207	0.009	0.012	0.016			
FDS1W	A → Y	(HH)	0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)	0.901	1.332	2.207	0.009	0.012	0.016			
FUS1W	A → Y	(HH)	0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)	0.901	1.332	2.207	0.009	0.012	0.016			
FWS1W	A → Y	(HH)	0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)	0.901	1.332	2.207	0.009	0.012	0.016			

### Chapter 1 Interface Block

Function	Input Buffer with failsafe					5.0 V	
Block type							
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
Normal	FIA1	FDA1			1	3	
Schmitt	FIE1W	FDE1W			1	6	
Clock							

Logic Diagram for "Normal" 	Truth Table <table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>				A	Y	1	1	0	0
	A	Y								
1	1									
0	0									
Logic Diagram for "Schmitt" 	Block type	Input		Output						
		Symbol	Fan-In	Symbol	Fan-Out					
	FIA1 to FDA1	A	-	Y	52					
	FIE1W to FDE1W	A	-	Y	42					
Logic Diagram for "Clock"										

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIA1	A → Y	(HH) (LL)	0.160 0.103	0.236 0.169	0.452 0.328	0.007 0.010	0.010 0.012	0.014 0.017			
FDA1	A → Y	(HH) (LL)	0.160 0.103	0.236 0.169	0.452 0.328	0.007 0.010	0.010 0.012	0.014 0.017			
FIE1W	A → Y	(HH) (LL)	0.672 0.903	0.948 1.328	1.621 2.208	0.008 0.009	0.011 0.012	0.017 0.016			
FDE1W	A → Y	(HH) (LL)	0.672 0.903	0.948 1.328	1.621 2.208	0.008 0.009	0.011 0.012	0.017 0.016			



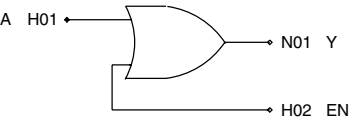
Chapter 1 Interface Block

Function	Input Buffer with EN(AND)					5.0 V															
Block type																					
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells															
Normal	FN11	FN21			1	6															
Schmitt																					
Clock																					
Logic Diagram for "Normal"			Truth Table																		
			<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	0	1	0	0	1	1	1
A	EN	Y																			
0	0	0																			
0	1	0																			
1	0	0																			
1	1	1																			
Logic Diagram for "Schmitt"			<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FN11 to FN21</td> <td>A EN</td> <td>- 3.0</td> <td>Y</td> <td>53</td> </tr> </tbody> </table>				Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FN11 to FN21	A EN	- 3.0	Y	53	
Block type	Input		Output																		
	Symbol	Fan-In	Symbol	Fan-Out																	
FN11 to FN21	A EN	- 3.0	Y	53																	
Logic Diagram for "Clock"																					

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FN11	A → Y	(HH)	0.096	0.166	0.304	0.007	0.010	0.014			
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017			
	EN → Y	(HH)	0.110	0.171	0.289	0.007	0.010	0.014			
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017			
FN21	A → Y	(HH)	0.096	0.166	0.304	0.007	0.010	0.014			
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017			
	EN → Y	(HH)	0.110	0.171	0.289	0.007	0.010	0.014			
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017			

Chapter 1 Interface Block

Function	Input Buffer with EN(OR)					5.0 V																				
Block type																										
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells																				
Normal	FN13	FN23			1	4																				
Schmitt																										
Clock																										
Logic Diagram for "Normal"				Truth Table																						
				<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	1	1	0	1	1	1	1				
A	EN	Y																								
0	0	0																								
0	1	1																								
1	0	1																								
1	1	1																								
Logic Diagram for "Schmitt"				<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FN13 to FN23</td> <td>A</td> <td>-</td> <td>Y</td> <td>52</td> </tr> <tr> <td></td> <td>EN</td> <td>3.0</td> <td></td> <td></td> </tr> </tbody> </table>				Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FN13 to FN23	A	-	Y	52		EN	3.0		
Block type	Input		Output																							
	Symbol	Fan-In	Symbol	Fan-Out																						
FN13 to FN23	A	-	Y	52																						
	EN	3.0																								
Logic Diagram for "Clock"																										

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FN13	A → Y	(HH)	0.117	0.183	0.298	0.007	0.010	0.014			
		(LL)	0.242	0.346	0.553	0.010	0.013	0.018			
	EN → Y	(HH)	0.093	0.160	0.270	0.007	0.010	0.014			
		(LL)	0.240	0.365	0.675	0.010	0.013	0.018			
FN23	A → Y	(HH)	0.117	0.183	0.298	0.007	0.010	0.014			
		(LL)	0.242	0.346	0.553	0.010	0.013	0.018			
	EN → Y	(HH)	0.093	0.160	0.270	0.007	0.010	0.014			
		(LL)	0.240	0.365	0.675	0.010	0.013	0.018			

Chapter 1 Interface Block

Function	Output Buffer						CMOS 5.0 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	FO09				1	4	
6mA	FO04				1	4	
9mA	FO01				1	4	
12mA	FO02				1	12	
18mA	FO03				1	12	
24mA	FO06				1	12	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	FO09	A	6.2	Y	-
	FO04	A	6.2	Y	-
	FO01	A	6.2	Y	-
	FO02	A	18.7	Y	-
	FO03	A	18.7	Y	-
	FO06	A	18.7	Y	-

Truth Table	
A	Y
1	1
0	0

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
FO09	A	→	Y	(HH)	0.459	0.744	1.554				0.042	0.056	0.079
				(LL)	0.563	1.047	2.482				0.077	0.103	0.151
FO04	A	→	Y	(HH)	0.473	0.745	1.534				0.028	0.037	0.053
				(LL)	0.469	0.819	1.792				0.038	0.052	0.075
FO01	A	→	Y	(HH)	0.516	0.806	1.685				0.017	0.023	0.034
				(LL)	0.521	0.867	1.817				0.026	0.035	0.051
FO02	A	→	Y	(HH)	0.361	0.564	1.173				0.014	0.019	0.028
				(LL)	0.315	0.559	1.217				0.019	0.026	0.038
FO03	A	→	Y	(HH)	0.422	0.657	1.358				0.010	0.014	0.022
				(LL)	0.373	0.641	1.358				0.013	0.018	0.026
FO06	A	→	Y	(HH)	0.481	0.746	1.528				0.008	0.012	0.020
				(LL)	0.441	0.746	1.536				0.010	0.014	0.021

Chapter 1 Interface Block

Function	Low-noise Output Buffer						CMOS 5.0 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	FE09				1	5	
6mA	FE04				1	5	
9mA	FE01				1	5	
12mA	FE02				1	5	
18mA	FE03				1	5	
24mA	FE06				1	5	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	FE09	A	9.6	Y	-
	FE04	A	9.6	Y	-
	FE01	A	9.5	Y	-
	FE02	A	9.5	Y	-
	FE03	A	9.6	Y	-
	FE06	A	9.6	Y	-

Truth Table	
A	Y
1	1
0	0

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
FE09	A	→	Y	(HH)	0.916	1.645	4.180				0.044	0.059	0.086
				(LL)	1.084	1.882	3.717				0.078	0.105	0.152
FE04	A	→	Y	(HH)	0.955	1.725	4.512				0.031	0.042	0.065
				(LL)	1.008	1.692	2.976				0.042	0.056	0.080
FE01	A	→	Y	(HH)	1.020	1.884	5.201				0.022	0.031	0.053
				(LL)	1.039	1.708	2.899				0.030	0.041	0.056
FE02	A	→	Y	(HH)	1.057	1.968	5.557				0.020	0.029	0.050
				(LL)	1.073	1.756	2.928				0.025	0.034	0.044
FE03	A	→	Y	(HH)	1.167	2.224	6.635				0.018	0.026	0.049
				(LL)	1.235	1.997	3.380				0.020	0.027	0.032
FE06	A	→	Y	(HH)	1.279	2.473	7.702				0.017	0.026	0.049
				(LL)	1.441	2.307	3.908				0.017	0.022	0.027

Chapter 1 Interface Block

Function	3-State Buffer						CMOS 5.0 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	B00T	B0DT	B0UT	B0WT	1	7	
6mA	B00E	B0DE	B0UE	B0WE	1	7	
9mA	B008	B0D8	B0U8	B0W8	1	7	
12mA	B007	B0D7	B0U7	B0W7	1	17	
18mA	B009	B0D9	B0U9	B0W9	1	17	
24mA	B00H	B0DH	B0UH	B0WH	1	17	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	B00T to B0WT	A	6.3	Y	-
		EN	1.0		
	B00E to B0WE	A	6.3	Y	-
		EN	1.0		
	B008 to B0W8	A	6.3	Y	-
		EN	1.0		
	B007 to B0W7	A	16.9	Y	-
		EN	1.0		
	B009 to B0W9	A	16.9	Y	-
		EN	1.0		
	B00H to B0WH	A	16.9	Y	-
		EN	1.0		

Truth Table		
A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B00T	A → Y	(HH)		0.591	1.045	2.529				0.042	0.056	0.080
		(LL)		0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y	(HZ)		1.088	1.523	2.712						
		(LZ)		0.380	0.577	0.996				0.042	0.056	0.077
		(ZH)		0.832	1.425	3.216				0.077	0.103	0.150
		(ZL)		0.771	1.385	2.985						
B0DT	A → Y	(HH)		0.591	1.045	2.529				0.042	0.056	0.080
		(LL)		0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y	(HZ)		1.088	1.523	2.712						
		(LZ)		0.380	0.577	0.996				0.042	0.056	0.077
		(ZH)		0.832	1.425	3.216				0.077	0.103	0.150
		(ZL)		0.771	1.385	2.985						
B0UT	A → Y	(HH)		0.591	1.045	2.529				0.042	0.056	0.080
		(LL)		0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y	(HZ)		1.088	1.523	2.712						
		(LZ)		0.380	0.577	0.996				0.042	0.056	0.077
		(ZH)		0.832	1.425	3.216				0.077	0.103	0.150
		(ZL)		0.771	1.385	2.985						
B0WT	A → Y	(HH)		0.591	1.045	2.529				0.042	0.056	0.080
		(LL)		0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y	(HZ)		1.088	1.523	2.712						
		(LZ)		0.380	0.577	0.996				0.042	0.056	0.077
		(ZH)		0.832	1.425	3.216				0.077	0.103	0.150
		(ZL)		0.771	1.385	2.985						
B00E	A → Y	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128				0.029	0.039	0.056
		(ZH)		0.851	1.454	3.330				0.039	0.052	0.076
		(ZL)		0.667	1.152	2.242						
B0DE	A → Y	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128				0.029	0.039	0.056
		(ZH)		0.851	1.454	3.330				0.039	0.052	0.076
		(ZL)		0.667	1.152	2.242						
B0UE	A → Y	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128				0.029	0.039	0.056
		(ZH)		0.851	1.454	3.330				0.039	0.052	0.076
		(ZL)		0.667	1.152	2.242						
B0WE	A → Y	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128				0.029	0.039	0.056
		(ZH)		0.851	1.454	3.330				0.039	0.052	0.076
		(ZL)		0.667	1.152	2.242						
B008	A → Y	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213				0.019	0.026	0.041
		(ZH)		0.902	1.553	3.690				0.027	0.036	0.051
		(ZL)		0.653	1.109	2.032						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0D8	A → Y	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
		(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
B0U8	A → Y	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
		(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
B0W8	A → Y	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
		(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
B007	A → Y	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
		(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
B0D7	A → Y	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
		(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
B0U7	A → Y	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
		(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
B0W7	A → Y	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
		(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
B009	A → Y	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
		(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
B0D9	A → Y	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
		(ZL)		0.647	1.048	1.880				0.014	0.019	0.027

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0U9	A → Y	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
		(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
B0W9	A → Y	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
		(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
B00H	A → Y	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
B0DH	A → Y	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
B0UH	A → Y	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
B0WH	A → Y	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022

Chapter 1 Interface Block

Function	Low-noise 3-State Buffer						CMOS 5.0 V	
Block type								
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells		
1mA								
2mA								
3mA	BE0T	BEDT	BEUT	BEWT	1	7		
6mA	BE0E	BEDE	BEUE	BEWE	1	7		
9mA	BE08	BED8	BEU8	BEW8	1	7		
12mA	BE07	BED7	BEU7	BEW7	1	7		
18mA	BE09	BED9	BEU9	BEW9	1	7		
24mA	BE0H	BEDH	BEUH	BEWH	1	7		
Logic Diagram		Block type		Input		Output		
		Symbol	Fan-in	Symbol	Fan-out			
		BE0T to BEWT	A	6.2	Y	-		
			EN	4.0				
		BE0E to BEWE	A	6.1	Y	-		
			EN	4.0				
		BE08 to BEW8	A	6.2	Y	-		
			EN	4.0				
		BE07 to BEW7	A	6.2	Y	-		
			EN	4.0				
		BE09 to BEW9	A	6.2	Y	-		
	EN	4.0						
BE0H to BEWH	A	6.2	Y	-				
	EN	4.0						
Truth Table								
A	EN	Y						
0	1	0						
1	1	1						
X	0	Z						
X:Irrelevant								
Z:High Impedance								

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BE0T	A → Y	(HH)		0.906	1.649	4.217				0.044	0.059	0.086
		(LL)		0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y	(HZ)		0.697	0.916	1.493						
		(LZ)		0.638	0.928	1.536				0.044	0.059	0.086
		(ZH)		0.907	1.682	4.261				0.077	0.104	0.151
		(ZL)		0.940	1.673	3.375						
BEDT	A → Y	(HH)		0.906	1.649	4.217				0.044	0.059	0.086
		(LL)		0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y	(HZ)		0.697	0.916	1.493						
		(LZ)		0.638	0.928	1.536				0.044	0.059	0.086
		(ZH)		0.907	1.682	4.261				0.077	0.104	0.151
		(ZL)		0.940	1.673	3.375						
BEUT	A → Y	(HH)		0.906	1.649	4.217				0.044	0.059	0.086
		(LL)		0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y	(HZ)		0.697	0.916	1.493						
		(LZ)		0.638	0.928	1.536				0.044	0.059	0.086
		(ZH)		0.907	1.682	4.261				0.077	0.104	0.151
		(ZL)		0.940	1.673	3.375						
BEWT	A → Y	(HH)		0.906	1.649	4.217				0.044	0.059	0.086
		(LL)		0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y	(HZ)		0.697	0.916	1.493						
		(LZ)		0.638	0.928	1.536				0.044	0.059	0.086
		(ZH)		0.907	1.682	4.261				0.077	0.104	0.151
		(ZL)		0.940	1.673	3.375						
BE0E	A → Y	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
		(LL)		0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y	(HZ)		0.948	1.269	2.217						
		(LZ)		0.817	1.158	1.799				0.031	0.042	0.066
		(ZH)		0.943	1.755	4.570				0.040	0.054	0.077
		(ZL)		0.868	1.494	2.680						
BEDE	A → Y	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
		(LL)		0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y	(HZ)		0.948	1.269	2.217						
		(LZ)		0.817	1.158	1.799				0.031	0.042	0.066
		(ZH)		0.943	1.755	4.570				0.040	0.054	0.077
		(ZL)		0.868	1.494	2.680						
BEUE	A → Y	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
		(LL)		0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y	(HZ)		0.948	1.269	2.217						
		(LZ)		0.817	1.158	1.799				0.031	0.042	0.066
		(ZH)		0.943	1.755	4.570				0.040	0.054	0.077
		(ZL)		0.868	1.494	2.680						
BEWE	A → Y	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
		(LL)		0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y	(HZ)		0.948	1.269	2.217						
		(LZ)		0.817	1.158	1.799				0.031	0.042	0.066
		(ZH)		0.943	1.755	4.570				0.040	0.054	0.077
		(ZL)		0.868	1.494	2.680						
BE08	A → Y	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
		(ZL)		0.864	1.475	2.488						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BED8	A → Y	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013						
		(ZH)		1.005	1.906	5.246				0.022	0.031	0.053
		(ZL)		0.864	1.475	2.488				0.029	0.038	0.054
BEU8	A → Y	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013						
		(ZH)		1.005	1.906	5.246				0.022	0.031	0.053
		(ZL)		0.864	1.475	2.488				0.029	0.038	0.054
BEW8	A → Y	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013						
		(ZH)		1.005	1.906	5.246				0.022	0.031	0.053
		(ZL)		0.864	1.475	2.488				0.029	0.038	0.054
BE07	A → Y	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214						
		(ZH)		1.039	1.989	5.597				0.021	0.029	0.051
		(ZL)		0.873	1.486	2.412				0.023	0.031	0.043
BED7	A → Y	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214						
		(ZH)		1.039	1.989	5.597				0.021	0.029	0.051
		(ZL)		0.873	1.486	2.412				0.023	0.031	0.043
BEU7	A → Y	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214						
		(ZH)		1.039	1.989	5.597				0.021	0.029	0.051
		(ZL)		0.873	1.486	2.412				0.023	0.031	0.043
BEW7	A → Y	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214						
		(ZH)		1.039	1.989	5.597				0.021	0.029	0.051
		(ZL)		0.873	1.486	2.412				0.023	0.031	0.043
BE09	A → Y	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649						
		(ZH)		1.139	2.241	6.670				0.018	0.026	0.049
		(ZL)		0.902	1.547	2.379				0.019	0.025	0.033
BED9	A → Y	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649						
		(ZH)		1.139	2.241	6.670				0.018	0.026	0.049
		(ZL)		0.902	1.547	2.379				0.019	0.025	0.033

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEU9	A → Y	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649						
		(ZH)		1.139	2.241	6.670				0.018	0.026	0.049
		(ZL)		0.902	1.547	2.379				0.019	0.025	0.033
BEW9	A → Y	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649						
		(ZH)		1.139	2.241	6.670				0.018	0.026	0.049
		(ZL)		0.902	1.547	2.379				0.019	0.025	0.033
BE0H	A → Y	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
		(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
BEDH	A → Y	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
		(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
BEUH	A → Y	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
		(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
BEWH	A → Y	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
		(ZL)		0.934	1.621	2.393				0.017	0.023	0.029



Chapter 1 Interface Block

Function	N-ch open drain Buffer						CMOS 5.0 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA							
6mA							
9mA	EXT1		EXT3	EXW3	1	4	
12mA	EXT9		EXTB	EXWB	1	4	
18mA	EXT5		EXT7	EXW7	1	4	
24mA	EXTD		EXTF	EXWF	1	4	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		EXT1 to EXW3	A	6.2	Y
EXT9 to EXWB	A	6.2	Y	-	
EXT5 to EXW7	A	6.2	Y	-	
EXTD to EXWF	A	6.2	Y	-	

Truth Table	
A	Y
1	Z
0	0

Z:High Impedance  
Connect a pull-up resistor to get a high level

Chapter 1 Interface Block

Block type	Switching speed										
	Path		tLDo (ns)			t1			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EXT1	A → Y	(LZ) (ZL)	0.361 0.264	0.465 0.493	0.633 1.001				0.026	0.035	0.050
EXT3	A → Y	(LZ) (ZL)	0.361 0.264	0.465 0.493	0.633 1.001				0.026	0.035	0.050
EXW3	A → Y	(LZ) (ZL)	0.361 0.264	0.465 0.493	0.633 1.001				0.026	0.035	0.050
EXT9	A → Y	(LZ) (ZL)	0.424 0.259	0.546 0.479	0.714 0.914				0.020	0.026	0.038
EXTB	A → Y	(LZ) (ZL)	0.424 0.259	0.546 0.479	0.714 0.914				0.020	0.026	0.038
EXWB	A → Y	(LZ) (ZL)	0.424 0.259	0.546 0.479	0.714 0.914				0.020	0.026	0.038
EXT5	A → Y	(LZ) (ZL)	0.547 0.266	0.707 0.485	0.885 0.860				0.014	0.019	0.026
EXT7	A → Y	(LZ) (ZL)	0.547 0.266	0.707 0.485	0.885 0.860				0.014	0.019	0.026
EXW7	A → Y	(LZ) (ZL)	0.547 0.266	0.707 0.485	0.885 0.860				0.014	0.019	0.026
EXTD	A → Y	(LZ) (ZL)	0.672 0.275	0.864 0.498	1.051 0.848				0.011	0.015	0.021
EXTF	A → Y	(LZ) (ZL)	0.672 0.275	0.864 0.498	1.051 0.848				0.011	0.015	0.021
EXWF	A → Y	(LZ) (ZL)	0.672 0.275	0.864 0.498	1.051 0.848				0.011	0.015	0.021

### Chapter 1 Interface Block

Function	N-ch open drain Buffer with failsafe						CMOS 5.0 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA							
6mA							
9mA	EXO1				1	4	
12mA	EXO9				1	4	
18mA	EXO5				1	4	
24mA	EXOD				1	4	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		EXO1	A	6.2	Y
EXO9	A	6.2	Y	-	
EXO5	A	6.2	Y	-	
EXOD	A	6.2	Y	-	

Truth Table	
A	Y
1	Z
0	0

Z:High Impedance  
Connect a pull-up resistor to get a high level

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EXO1	A → Y	(LZ) (ZL)	0.361 0.264	0.465 0.493	0.633 1.001				0.026	0.035	0.050
EXO9	A → Y	(LZ) (ZL)	0.424 0.259	0.546 0.479	0.714 0.914				0.020	0.026	0.038
EXO5	A → Y	(LZ) (ZL)	0.547 0.266	0.707 0.485	0.885 0.860				0.014	0.019	0.026
EXOD	A → Y	(LZ) (ZL)	0.672 0.275	0.864 0.498	1.051 0.848				0.011	0.015	0.021

Chapter 1 Interface Block

Function	I/O Buffer					CMOS 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	B00U	B0DU	B0UU	B0WU	1	10	
6mA	B00C	B0DC	B0UC	B0WC	1	10	
9mA	B003	B0D3	B0U3	B0W3	1	10	
12mA	B001	B0D1	B0U1	B0W1	1	20	
18mA	B005	B0D5	B0U5	B0W5	1	20	
24mA	B00F	B0DF	B0UF	B0WF	1	20	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		B00U to B0WU	A	6.3	Y1
B00C to B0WC	A	6.3	Y1	52	
B003 to B0W3	A	6.3	Y1	52	
B001 to B0W1	A	16.9	Y1	52	
B005 to B0W5	A	16.9	Y1	52	
B00F to B0WF	A	16.9	Y1	52	

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
B00U	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.007	0.010	0.014	0.077	0.103
(HH)		0.160	0.236	0.452	0.007	0.010	0.014						
(LL)		0.103	0.168	0.328	0.010	0.012	0.017						
B0DU	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.007	0.010	0.014	0.077	0.103
(HH)		0.160	0.236	0.452	0.007	0.010	0.014						
(LL)		0.103	0.168	0.328	0.010	0.012	0.017						
B0UU	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.007	0.010	0.014	0.077	0.103
(HH)		0.160	0.236	0.452	0.007	0.010	0.014						
(LL)		0.103	0.168	0.328	0.010	0.012	0.017						
B0WU	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.007	0.010	0.014	0.077	0.103
(HH)		0.160	0.236	0.452	0.007	0.010	0.014						
(LL)		0.103	0.168	0.328	0.010	0.012	0.017						
B00C	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
	EN → Y0	(HZ)	1.413	1.971	3.618								
		(LZ)	0.451	0.675	1.128								
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056		
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.007	0.010	0.014	0.039	0.052
(HH)		0.160	0.236	0.452	0.007	0.010	0.014						
(LL)		0.103	0.168	0.328	0.010	0.012	0.017						
B0DC	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
	EN → Y0	(HZ)	1.413	1.971	3.618								
		(LZ)	0.451	0.675	1.128								
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056		
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.007	0.010	0.014	0.039	0.052
(HH)		0.160	0.236	0.452	0.007	0.010	0.014						
(LL)		0.103	0.168	0.328	0.010	0.012	0.017						
B0UC	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
	EN → Y0	(HZ)	1.413	1.971	3.618								
		(LZ)	0.451	0.675	1.128								
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056		
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.007	0.010	0.014	0.039	0.052
(HH)		0.160	0.236	0.452	0.007	0.010	0.014						
(LL)		0.103	0.168	0.328	0.010	0.012	0.017						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0WC	A → Y0	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)	1.413	1.971	3.618							
		(LZ)	0.451	0.675	1.128							
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056	
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.039	0.052	0.076	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B003	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)	1.970	2.727	5.121							
		(LZ)	0.510	0.752	1.213							
		(ZH)	0.902	1.553	3.690				0.019	0.026	0.041	
	Y0 → Y1	(ZL)	0.653	1.109	2.032				0.027	0.036	0.051	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0D3	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)	1.970	2.727	5.121							
		(LZ)	0.510	0.752	1.213							
		(ZH)	0.902	1.553	3.690				0.019	0.026	0.041	
	Y0 → Y1	(ZL)	0.653	1.109	2.032				0.027	0.036	0.051	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0U3	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)	1.970	2.727	5.121							
		(LZ)	0.510	0.752	1.213							
		(ZH)	0.902	1.553	3.690				0.019	0.026	0.041	
	Y0 → Y1	(ZL)	0.653	1.109	2.032				0.027	0.036	0.051	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0W3	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)	1.970	2.727	5.121							
		(LZ)	0.510	0.752	1.213							
		(ZH)	0.902	1.553	3.690				0.019	0.026	0.041	
	Y0 → Y1	(ZL)	0.653	1.109	2.032				0.027	0.036	0.051	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B001	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
			(LL)	0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)	1.692	2.427	4.634							
		(LZ)	0.628	0.961	1.612							
		(ZH)	0.952	1.561	3.392				0.015	0.021	0.032	
	Y0 → Y1	(ZL)	0.646	1.051	1.954				0.020	0.027	0.038	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0D1	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
			(LL)	0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)	1.692	2.427	4.634							
		(LZ)	0.628	0.961	1.612							
		(ZH)	0.952	1.561	3.392				0.015	0.021	0.032	
	Y0 → Y1	(ZL)	0.646	1.051	1.954				0.020	0.027	0.038	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0U1	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
			(LL)	0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)	1.692	2.427	4.634							
		(LZ)	0.628	0.961	1.612							
		(ZH)	0.952	1.561	3.392				0.015	0.021	0.032	
	Y0 → Y1	(ZL)	0.646	1.051	1.954				0.020	0.027	0.038	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0W1	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
			(LL)	0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)	1.692	2.427	4.634							
		(LZ)	0.628	0.961	1.612							
		(ZH)	0.952	1.561	3.392				0.015	0.021	0.032	
	Y0 → Y1	(ZL)	0.646	1.051	1.954				0.020	0.027	0.038	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B005	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
			(LL)	0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)	2.230	3.165	6.099							
		(LZ)	0.713	1.069	1.724							
		(ZH)	0.997	1.655	3.703				0.012	0.017	0.028	
	Y0 → Y1	(ZL)	0.647	1.048	1.880				0.014	0.019	0.027	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0D5	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
			(LL)	0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)	2.230	3.165	6.099							
		(LZ)	0.713	1.069	1.724							
		(ZH)	0.997	1.655	3.703				0.012	0.017	0.028	
	Y0 → Y1	(ZL)	0.647	1.048	1.880				0.014	0.019	0.027	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0U5	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
			(LL)	0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)	2.230	3.165	6.099							
		(LZ)	0.713	1.069	1.724							
		(ZH)	0.997	1.655	3.703				0.012	0.017	0.028	
	Y0 → Y1	(ZL)	0.647	1.048	1.880				0.014	0.019	0.027	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B0W5	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
			(LL)	0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)	2.230	3.165	6.099							
		(LZ)	0.713	1.069	1.724							
		(ZH)	0.997	1.655	3.703				0.012	0.017	0.028	
	Y0 → Y1	(ZL)	0.647	1.048	1.880				0.014	0.019	0.027	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						
B00F	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
			(LL)	0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)	2.768	3.922	7.625							
		(LZ)	0.796	1.176	1.839							
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027	
	Y0 → Y1	(ZL)	0.650	1.054	1.852				0.011	0.016	0.022	
(HH)		0.160	0.236	0.452	0.007	0.010	0.014					
(LL)	0.103	0.168	0.328	0.010	0.012	0.017						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BODF	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
			(LL)	0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)	2.768	3.922	7.625							
		(LZ)	0.796	1.176	1.839							
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027	
	Y0 → Y1	(ZL)	0.650	1.054	1.852				0.011	0.016	0.022	
		(HH)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
	BOUF	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015
(LL)				0.729	1.148	2.184				0.010	0.014	0.021
EN → Y0		(HZ)	2.768	3.922	7.625							
		(LZ)	0.796	1.176	1.839							
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027	
Y0 → Y1		(ZL)	0.650	1.054	1.852				0.011	0.016	0.022	
		(HH)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
BOWF		A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015
	(LL)			0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)	2.768	3.922	7.625							
		(LZ)	0.796	1.176	1.839							
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027	
	Y0 → Y1	(ZL)	0.650	1.054	1.852				0.011	0.016	0.022	
		(HH)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise I/O Buffer					CMOS 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BE0U	BEDU	BEUU	BEWU	1	10	
6mA	BE0C	BEDC	BEUC	BEWC	1	10	
9mA	BE03	BED3	BEU3	BEW3	1	10	
12mA	BE01	BED1	BEU1	BEW1	1	10	
18mA	BE05	BED5	BEU5	BEW5	1	10	
24mA	BE0F	BEDF	BEUF	BEWF	1	10	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			BE0U to BEWU	A	6.2
BE0C to BEWC	A	6.1	Y1	52	
BE03 to BEW3	A	6.2	Y1	52	
BE01 to BEW1	A	6.2	Y1	52	
BE05 to BEW5	A	6.2	Y1	52	
BE0F to BEWF	A	6.2	Y1	52	

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BE0U	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(HZ)	(LZ)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
BEDU	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	(LZ)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
BEUU	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	(LZ)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
BEWU	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	(LZ)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
BE0C	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	(LZ)	0.817	1.158	1.799						
			(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
			(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
Y0 → Y1	(HH)	(LL)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
BEDC	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	(LZ)	0.817	1.158	1.799						
			(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
			(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
Y0 → Y1	(HH)	(LL)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
BEUC	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	(LZ)	0.817	1.158	1.799						
			(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
			(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
Y0 → Y1	(HH)	(LL)	0.160	0.236	0.452	0.007	0.010	0.014				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEWC	A → Y0	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(LZ)	0.817	1.158	1.799						
	EN → Y0	(HZ)		0.948	1.269	2.217						
			(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
			(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BE03	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
			(LL)	1.034	1.615	2.959				0.026	0.035	0.049
			(LZ)	0.981	1.364	2.013						
	EN → Y0	(HZ)		1.369	1.836	3.377						
			(ZH)	1.005	1.906	5.246				0.022	0.031	0.053
			(ZL)	0.864	1.475	2.488				0.029	0.038	0.054
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BED3	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
			(LL)	1.034	1.615	2.959				0.026	0.035	0.049
			(LZ)	0.981	1.364	2.013						
	EN → Y0	(HZ)		1.369	1.836	3.377						
			(ZH)	1.005	1.906	5.246				0.022	0.031	0.053
			(ZL)	0.864	1.475	2.488				0.029	0.038	0.054
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BEU3	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
			(LL)	1.034	1.615	2.959				0.026	0.035	0.049
			(LZ)	0.981	1.364	2.013						
	EN → Y0	(HZ)		1.369	1.836	3.377						
			(ZH)	1.005	1.906	5.246				0.022	0.031	0.053
			(ZL)	0.864	1.475	2.488				0.029	0.038	0.054
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BEW3	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
			(LL)	1.034	1.615	2.959				0.026	0.035	0.049
			(LZ)	0.981	1.364	2.013						
	EN → Y0	(HZ)		1.369	1.836	3.377						
			(ZH)	1.005	1.906	5.246				0.022	0.031	0.053
			(ZL)	0.864	1.475	2.488				0.029	0.038	0.054
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BE01	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
			(LL)	1.107	1.718	3.065				0.021	0.028	0.037
			(LZ)	1.138	1.564	2.214						
	EN → Y0	(HZ)		1.585	2.130	3.959						
			(ZH)	1.039	1.989	5.597				0.021	0.029	0.051
			(ZL)	0.873	1.486	2.412				0.023	0.031	0.043
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BED1	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
			(LL)	1.107	1.718	3.065				0.021	0.028	0.037
			(LZ)	1.138	1.564	2.214						
	EN → Y0	(HZ)		1.585	2.130	3.959						
			(ZH)	1.039	1.989	5.597				0.021	0.029	0.051
			(ZL)	0.873	1.486	2.412				0.023	0.031	0.043
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEU1	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
			(LL)	1.107	1.718	3.065				0.021	0.028	0.037
			(LZ)	1.138	1.564	2.214						
	EN → Y0	(HZ)		1.585	2.130	3.959						
			(ZH)	1.039	1.989	5.597				0.021	0.029	0.051
			(ZL)	0.873	1.486	2.412				0.023	0.031	0.043
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BEW1	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
			(LL)	1.107	1.718	3.065				0.021	0.028	0.037
			(LZ)	1.138	1.564	2.214						
	EN → Y0	(HZ)		1.585	2.130	3.959						
			(ZH)	1.039	1.989	5.597				0.021	0.029	0.051
			(ZL)	0.873	1.486	2.412				0.023	0.031	0.043
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BE05	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
			(LL)	1.391	2.128	3.712				0.015	0.020	0.028
			(LZ)	1.467	1.974	2.649						
	EN → Y0	(HZ)		2.247	3.020	5.777						
			(ZH)	1.139	2.241	6.670				0.018	0.026	0.049
			(ZL)	0.902	1.547	2.379				0.019	0.025	0.033
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BED5	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
			(LL)	1.391	2.128	3.712				0.015	0.020	0.028
			(LZ)	1.467	1.974	2.649						
	EN → Y0	(HZ)		2.247	3.020	5.777						
			(ZH)	1.139	2.241	6.670				0.018	0.026	0.049
			(ZL)	0.902	1.547	2.379				0.019	0.025	0.033
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BEU5	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
			(LL)	1.391	2.128	3.712				0.015	0.020	0.028
			(LZ)	1.467	1.974	2.649						
	EN → Y0	(HZ)		2.247	3.020	5.777						
			(ZH)	1.139	2.241	6.670				0.018	0.026	0.049
			(ZL)	0.902	1.547	2.379				0.019	0.025	0.033
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BEW5	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
			(LL)	1.391	2.128	3.712				0.015	0.020	0.028
			(LZ)	1.467	1.974	2.649						
	EN → Y0	(HZ)		2.247	3.020	5.777						
			(ZH)	1.139	2.241	6.670				0.018	0.026	0.049
			(ZL)	0.902	1.547	2.379				0.019	0.025	0.033
	Y0 → Y1	(HH)		0.160	0.236	0.452	0.007	0.010	0.014			
			(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
			(LZ)									
BE0F	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
			(LL)	1.676	2.541	4.411				0.012	0.017	0.023
			(LZ)	1.791	2.376	3.054						
	EN → Y0	(HZ)		2.920	3.913	7.573						
			(ZH)	1.236	2.487	7.732				0.017	0.026	0.049
			(ZL)	0.934	1.621	2.393						

Chapter 1 Interface Block

Block type	Switching speed										
	Path		tLDo (ns)			t1			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEDF	A → Y0	(HH)	1.429	2.521	7.676				0.015	0.025	0.049
		(LL)	1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)	2.920	3.913	7.573						
		(LZ)	1.791	2.376	3.054						
		(ZH)	1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)	0.934	1.621	2.393				0.017	0.023	0.029
		(HH)	0.160	0.236	0.452	0.007	0.010	0.014			
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
	BEUF	A → Y0	(HH)	1.429	2.521	7.676				0.015	0.025
(LL)			1.676	2.541	4.411				0.012	0.017	0.023
EN → Y0		(HZ)	2.920	3.913	7.573						
		(LZ)	1.791	2.376	3.054						
		(ZH)	1.236	2.487	7.732				0.017	0.026	0.049
Y0 → Y1		(ZL)	0.934	1.621	2.393				0.017	0.023	0.029
		(HH)	0.160	0.236	0.452	0.007	0.010	0.014			
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017			
BEWF		A → Y0	(HH)	1.429	2.521	7.676				0.015	0.025
	(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)	2.920	3.913	7.573						
		(LZ)	1.791	2.376	3.054						
		(ZH)	1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)	0.934	1.621	2.393				0.017	0.023	0.029
		(HH)	0.160	0.236	0.452	0.007	0.010	0.014			
		(LL)	0.103	0.168	0.328	0.010	0.012	0.017			

[MEMO]

Chapter 1 Interface Block



Chapter 1 Interface Block

Function	Schmitt I/O Buffer					CMOS 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BSIUW	BSDUW	BSUUW	BSWUW	1	13	
6mA	BSICW	BSDCW	BSUCW	BSWCW	1	13	
9mA	BSI3W	BSD3W	BSU3W	BSW3W	1	13	
12mA	BSI1W	BSD1W	BSU1W	BSW1W	1	23	
18mA	BSI5W	BSD5W	BSU5W	BSW5W	1	23	
24mA	BSIFW	BSDFW	BSUFW	BSWFW	1	23	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		BSIUW to BSWUW	A	6.3	Y1
BSICW to BSWCW	A	6.3	Y1	42	
	EN	1.0			
BSI3W to BSW3W	A	6.3	Y1	42	
	EN	1.0			
BSI1W to BSW1W	A	16.9	Y1	42	
	EN	1.0			
BSI5W to BSW5W	A	16.9	Y1	42	
	EN	1.0			
BSIFW to BSWFW	A	16.9	Y1	42	
	EN	1.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSIUW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y0	(HZ)	1.088	1.523	2.712							
		(LZ)	0.380	0.577	0.996							
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077	
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.077	0.103	0.150	
(HH)		0.673	0.949	1.621	0.008	0.011	0.017					
(LL)	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
BSDUW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y0	(HZ)	1.088	1.523	2.712							
		(LZ)	0.380	0.577	0.996							
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077	
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.077	0.103	0.150	
(HH)		0.673	0.949	1.621	0.008	0.011	0.017					
(LL)	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
BSUUW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y0	(HZ)	1.088	1.523	2.712							
		(LZ)	0.380	0.577	0.996							
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077	
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.077	0.103	0.150	
(HH)		0.673	0.949	1.621	0.008	0.011	0.017					
(LL)	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
BSWUW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y0	(HZ)	1.088	1.523	2.712							
		(LZ)	0.380	0.577	0.996							
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077	
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.077	0.103	0.150	
(HH)		0.673	0.949	1.621	0.008	0.011	0.017					
(LL)	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
BSICW	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)	1.413	1.971	3.618							
		(LZ)	0.451	0.675	1.128							
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056	
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.039	0.052	0.076	
(HH)		0.673	0.949	1.621	0.008	0.011	0.017					
(LL)	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
BSDCW	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)	1.413	1.971	3.618							
		(LZ)	0.451	0.675	1.128							
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056	
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.039	0.052	0.076	
(HH)		0.673	0.949	1.621	0.008	0.011	0.017					
(LL)	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
BSUCW	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)	1.413	1.971	3.618							
		(LZ)	0.451	0.675	1.128							
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056	
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.039	0.052	0.076	
(HH)		0.673	0.949	1.621	0.008	0.011	0.017					
(LL)	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					
	(LL)	0.901	1.332	2.207	0.009	0.012	0.016					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSWCW	A → Y0	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128						
		(ZH)		0.851	1.454	3.330				0.029	0.039	0.056
	Y0 → Y1	(ZL)		0.667	1.152	2.242				0.039	0.052	0.076
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSI3W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSD3W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSU3W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSW3W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSI1W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSD1W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSU1W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSW1W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSI5W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSD5W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSU5W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSW5W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BSIFW	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				

Chapter 1 Interface Block

Block type	Switching speed										
	Path		tLDo (ns)			t1			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSDFW	A → Y0	(HH)	0.588	1.038	2.740				0.011	0.015	0.028
		(LL)	0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)	2.768	3.922	7.625						
		(LZ)	0.796	1.176	1.839						
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)	0.650	1.054	1.852				0.011	0.016	0.022
		(HH)	0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)	0.901	1.332	2.207	0.009	0.012	0.016			
	BSUFW	A → Y0	(HH)	0.588	1.038	2.740				0.011	0.015
(LL)			0.729	1.148	2.184				0.010	0.014	0.021
EN → Y0		(HZ)	2.768	3.922	7.625						
		(LZ)	0.796	1.176	1.839						
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027
Y0 → Y1		(ZL)	0.650	1.054	1.852				0.011	0.016	0.022
		(HH)	0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)	0.901	1.332	2.207	0.009	0.012	0.016			
BSWFW		A → Y0	(HH)	0.588	1.038	2.740				0.011	0.015
	(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)	2.768	3.922	7.625						
		(LZ)	0.796	1.176	1.839						
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)	0.650	1.054	1.852				0.011	0.016	0.022
		(HH)	0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)	0.901	1.332	2.207	0.009	0.012	0.016			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise Schmitt I/O Buffer					CMOS 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BFIUW	BFDUW	BFUWU	BFWUW	1	13	
6mA	BFICW	BFDCW	BFUCW	BFWCW	1	13	
9mA	BF13W	BFD3W	BFU3W	BFW3W	1	13	
12mA	BF11W	BFD1W	BFU1W	BFW1W	1	13	
18mA	BF15W	BFD5W	BFU5W	BFW5W	1	13	
24mA	BF1FW	BFD5W	BFU5W	BFW5W	1	13	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		BFIUW to BFWUW	A	6.2	Y1
BFICW to BFWCW	A	6.1	Y1	42	
BF13W to BFW3W	A	6.2	Y1	42	
BF11W to BFW1W	A	6.2	Y1	42	
BF15W to BFW5W	A	6.2	Y1	42	
BF1FW to BFW5W	A	6.2	Y1	42	

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed										
	Path		tLDo (ns)			t1			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFIUW	A → Y0	(HH)	0.906	1.649	4.217				0.044	0.059	0.086
		(LL)	0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y0	(HZ)	0.697	0.916	1.493						
		(LZ)	0.638	0.928	1.536						
	Y0 → Y1	(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
		(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
BFDUW	A → Y0	(HH)	0.906	1.649	4.217				0.044	0.059	0.086
		(LL)	0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y0	(HZ)	0.697	0.916	1.493						
		(LZ)	0.638	0.928	1.536						
	Y0 → Y1	(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
		(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
BFUWU	A → Y0	(HH)	0.906	1.649	4.217				0.044	0.059	0.086
		(LL)	0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y0	(HZ)	0.697	0.916	1.493						
		(LZ)	0.638	0.928	1.536						
	Y0 → Y1	(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
		(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
BFWUW	A → Y0	(HH)	0.906	1.649	4.217				0.044	0.059	0.086
		(LL)	0.903	1.561	3.193				0.077	0.103	0.150
	EN → Y0	(HZ)	0.697	0.916	1.493						
		(LZ)	0.638	0.928	1.536						
	Y0 → Y1	(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
		(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
BFICW	A → Y0	(HH)	0.951	1.724	4.530				0.031	0.042	0.066
		(LL)	0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y0	(HZ)	0.948	1.269	2.217						
		(LZ)	0.817	1.158	1.799						
	Y0 → Y1	(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
		(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
BFDCW	A → Y0	(HH)	0.951	1.724	4.530				0.031	0.042	0.066
		(LL)	0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y0	(HZ)	0.948	1.269	2.217						
		(LZ)	0.817	1.158	1.799						
	Y0 → Y1	(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
		(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
BFUCW	A → Y0	(HH)	0.951	1.724	4.530				0.031	0.042	0.066
		(LL)	0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y0	(HZ)	0.948	1.269	2.217						
		(LZ)	0.817	1.158	1.799						
	Y0 → Y1	(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
		(ZL)	0.868	1.494	2.680				0.040	0.054	0.077

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFWCW	A → Y0	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
		(LL)		0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y0	(HZ)		0.948	1.269	2.217						
		(LZ)		0.817	1.158	1.799				0.031	0.042	0.066
		(ZH)		0.943	1.755	4.570				0.040	0.054	0.077
	Y0 → Y1	(ZL)		0.868	1.494	2.680						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFI3W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFD3W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFU3W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFW3W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFI1W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFD1W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFU1W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFW1W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFI5W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFD5W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFU5W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFW5W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				
BFIFW	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054				0.017	0.026	0.049
		(ZH)		1.236	2.487	7.732				0.017	0.023	0.029
	Y0 → Y1	(ZL)		0.934	1.621	2.393						
(HH)			0.673	0.949	1.621	0.008	0.011	0.017				
	(LL)		0.901	1.332	2.207	0.009	0.012	0.016				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFDFW	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
		(HH)		0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)		0.901	1.332	2.207	0.009	0.012	0.016			
	BFUFW	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025
(LL)				1.676	2.541	4.411				0.012	0.017	0.023
EN → Y0		(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
Y0 → Y1		(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
		(HH)		0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)		0.901	1.332	2.207	0.009	0.012	0.016			
BFWFW		A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025
	(LL)			1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
		(HH)		0.673	0.949	1.621	0.008	0.011	0.017			
		(LL)		0.901	1.332	2.207	0.009	0.012	0.016			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	I/O Buffer with EN(AND)					CMOS 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN2U	BN4U			1	13	
6mA	BN2C	BN4C			1	13	
9mA	BN23	BN43			1	13	
12mA	BN21	BN41			1	23	
18mA	BN25	BN45			1	23	
24mA	BN2F	BN4F			1	23	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	BN2U to BN4U	A	6.3	Y1	53
	EN	1.0			
	ENI	3.0			
	BN2C to BN4C	A	6.3	Y1	53
	EN	1.0			
	ENI	3.0			
	BN23 to BN43	A	6.3	Y1	53
	EN	1.0			
	ENI	3.0			
	BN21 to BN41	A	16.9	Y1	53
	EN	1.0			
	ENI	3.0			
BN25 to BN45	A	16.9	Y1	53	
EN	1.0				
ENI	3.0				
BN2F to BN4F	A	16.9	Y1	53	
EN	1.0				
ENI	3.0				

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X: Irrelevant  
Z: High Impedance

Y0	ENI	Y1
0	0	0
0	1	0
1	0	0
1	1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN2U	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
			(HZ)	1.088	1.523	2.712						
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996						
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150
	ENI → Y1	(HH)	(LL)	0.110	0.171	0.289	0.007	0.010	0.014			
			(LL)	0.248	0.353	0.510	0.010	0.012	0.017			
			(HH)	0.096	0.166	0.304	0.007	0.010	0.014			
Y0 → Y1	(HH)	(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
		(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
BN4U	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
			(HZ)	1.088	1.523	2.712						
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996						
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150
	ENI → Y1	(HH)	(LL)	0.110	0.171	0.289	0.007	0.010	0.014			
			(LL)	0.248	0.353	0.510	0.010	0.012	0.017			
			(HH)	0.096	0.166	0.304	0.007	0.010	0.014			
Y0 → Y1	(HH)	(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
		(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
BN2C	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
			(HZ)	1.413	1.971	3.618						
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128						
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076
	ENI → Y1	(HH)	(LL)	0.110	0.171	0.289	0.007	0.010	0.014			
			(LL)	0.248	0.353	0.510	0.010	0.012	0.017			
			(HH)	0.096	0.166	0.304	0.007	0.010	0.014			
Y0 → Y1	(HH)	(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
		(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
BN4C	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
			(HZ)	1.413	1.971	3.618						
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128						
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076
	ENI → Y1	(HH)	(LL)	0.110	0.171	0.289	0.007	0.010	0.014			
			(LL)	0.248	0.353	0.510	0.010	0.012	0.017			
			(HH)	0.096	0.166	0.304	0.007	0.010	0.014			
Y0 → Y1	(HH)	(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
		(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
BN23	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
			(HZ)	1.970	2.727	5.121						
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213						
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051
	ENI → Y1	(HH)	(LL)	0.110	0.171	0.289	0.007	0.010	0.014			
			(LL)	0.248	0.353	0.510	0.010	0.012	0.017			
			(HH)	0.096	0.166	0.304	0.007	0.010	0.014			
Y0 → Y1	(HH)	(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
		(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
BN43	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
			(HZ)	1.970	2.727	5.121						
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213						
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
	ENI → Y1	(HH)	0.110	0.171	0.289	0.007	0.010	0.014				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
	Y0 → Y1	(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
BN21	A → Y0	(HH)	0.491	0.857	2.145				0.015	0.021	0.033	
		(LL)	0.508	0.827	1.674				0.019	0.025	0.036	
	EN → Y0	(HZ)	1.692	2.427	4.634							
		(LZ)	0.628	0.961	1.612							
		(ZH)	0.952	1.561	3.392				0.015	0.021	0.032	
		(ZL)	0.646	1.051	1.954				0.020	0.027	0.038	
	ENI → Y1	(HH)	0.110	0.171	0.289	0.007	0.010	0.014				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
	Y0 → Y1	(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
BN41	A → Y0	(HH)	0.491	0.857	2.145				0.015	0.021	0.033	
		(LL)	0.508	0.827	1.674				0.019	0.025	0.036	
	EN → Y0	(HZ)	1.692	2.427	4.634							
		(LZ)	0.628	0.961	1.612							
		(ZH)	0.952	1.561	3.392				0.015	0.021	0.032	
		(ZL)	0.646	1.051	1.954				0.020	0.027	0.038	
	ENI → Y1	(HH)	0.110	0.171	0.289	0.007	0.010	0.014				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
	Y0 → Y1	(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
BN25	A → Y0	(HH)	0.540	0.952	2.455				0.012	0.017	0.029	
		(LL)	0.619	0.988	1.917				0.013	0.017	0.026	
	EN → Y0	(HZ)	2.230	3.165	6.099							
		(LZ)	0.713	1.069	1.724							
		(ZH)	0.997	1.655	3.703				0.012	0.017	0.028	
		(ZL)	0.647	1.048	1.880				0.014	0.019	0.027	
	ENI → Y1	(HH)	0.110	0.171	0.289	0.007	0.010	0.014				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
	Y0 → Y1	(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
BN45	A → Y0	(HH)	0.540	0.952	2.455				0.012	0.017	0.029	
		(LL)	0.619	0.988	1.917				0.013	0.017	0.026	
	EN → Y0	(HZ)	2.230	3.165	6.099							
		(LZ)	0.713	1.069	1.724							
		(ZH)	0.997	1.655	3.703				0.012	0.017	0.028	
		(ZL)	0.647	1.048	1.880				0.014	0.019	0.027	
	ENI → Y1	(HH)	0.110	0.171	0.289	0.007	0.010	0.014				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
	Y0 → Y1	(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017				
BN2F	A → Y0	(HH)	0.588	1.038	2.740				0.011	0.015	0.028	
		(LL)	0.729	1.148	2.184				0.010	0.014	0.021	
	EN → Y0	(HZ)	2.768	3.922	7.625							
		(LZ)	0.796	1.176	1.839							
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.027	
		(ZL)	0.650	1.054	1.852				0.011	0.016	0.022	
	ENI → Y1	(HH)	0.110	0.171	0.289	0.007	0.010	0.014				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
	Y0 → Y1	(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN4F	A → Y0	(HH)	0.588	1.038	2.740							
		(LL)	0.729	1.148	2.184							
	EN → Y0	(HZ)	2.768	3.922	7.625							
		(LZ)	0.796	1.176	1.839							
		(ZH)	1.036	1.734	3.989				0.011	0.015	0.021	
		(ZL)	0.650	1.054	1.852				0.011	0.016	0.022	
	ENI → Y1	(HH)	0.110	0.171	0.289	0.007	0.010	0.014				
		(LL)	0.248	0.353	0.510	0.010	0.012	0.017				
	Y0 → Y1	(HH)	0.096	0.166	0.304	0.007	0.010	0.014				
		(LL)	0.172	0.254	0.427	0.010	0.012	0.017				



Chapter 1 Interface Block

Function	I/O Buffer with EN(OR)						CMOS 5.0 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN3U	BN5U			1	11	
6mA	BN3C	BN5C			1	11	
9mA	BN33	BN53			1	11	
12mA	BN31	BN51			1	21	
18mA	BN35	BN55			1	21	
24mA	BN3F	BN5F			1	21	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	BN3U to BN5U	A	6.3	Y1	52
		EN	1.0		
		ENI	3.0		
	BN3C to BN5C	A	6.3	Y1	52
		EN	1.0		
		ENI	3.0		
	BN33 to BN53	A	6.3	Y1	52
		EN	1.0		
		ENI	3.0		
	BN31 to BN51	A	16.9	Y1	52
		EN	1.0		
		ENI	3.0		
BN35 to BN55	A	16.9	Y1	52	
	EN	1.0			
	ENI	3.0			
BN3F to BN5F	A	16.9	Y1	52	
	EN	1.0			
	ENI	3.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X: Irrelevant  
Z: High Impedance

Y0	ENI	Y1
0	0	0
0	1	1
1	0	1
1	1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			tLDo (ns)			t1			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BN3U	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
			(HZ)	1.088	1.523	2.712							
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996							
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077	
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150	
	ENI → Y1	(HH)	(LL)	0.093	0.160	0.270	0.007	0.010	0.014				
			(LL)	0.240	0.365	0.675	0.010	0.013	0.018				
			(HH)	0.117	0.183	0.298	0.007	0.010	0.014				
Y0 → Y1	(HH)	(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
		(HH)	0.117	0.183	0.298	0.007	0.010	0.014					
		(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
BN5U	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
			(HZ)	1.088	1.523	2.712							
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996							
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077	
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150	
	ENI → Y1	(HH)	(LL)	0.093	0.160	0.270	0.007	0.010	0.014				
			(LL)	0.240	0.365	0.675	0.010	0.013	0.018				
			(HH)	0.117	0.183	0.298	0.007	0.010	0.014				
Y0 → Y1	(HH)	(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
		(HH)	0.117	0.183	0.298	0.007	0.010	0.014					
		(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
BN3C	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
			(HZ)	1.413	1.971	3.618							
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128							
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056	
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076	
	ENI → Y1	(HH)	(LL)	0.093	0.160	0.270	0.007	0.010	0.014				
			(LL)	0.240	0.365	0.675	0.010	0.013	0.018				
			(HH)	0.117	0.183	0.298	0.007	0.010	0.014				
Y0 → Y1	(HH)	(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
		(HH)	0.117	0.183	0.298	0.007	0.010	0.014					
		(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
BN5C	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
			(HZ)	1.413	1.971	3.618							
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128							
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056	
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076	
	ENI → Y1	(HH)	(LL)	0.093	0.160	0.270	0.007	0.010	0.014				
			(LL)	0.240	0.365	0.675	0.010	0.013	0.018				
			(HH)	0.117	0.183	0.298	0.007	0.010	0.014				
Y0 → Y1	(HH)	(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
		(HH)	0.117	0.183	0.298	0.007	0.010	0.014					
		(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
BN33	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041	
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047	
			(HZ)	1.970	2.727	5.121							
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213							
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041	
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051	
	ENI → Y1	(HH)	(LL)	0.093	0.160	0.270	0.007	0.010	0.014				
			(LL)	0.240	0.365	0.675	0.010	0.013	0.018				
			(HH)	0.117	0.183	0.298	0.007	0.010	0.014				
Y0 → Y1	(HH)	(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
		(HH)	0.117	0.183	0.298	0.007	0.010	0.014					
		(LL)	0.242	0.346	0.553	0.010	0.013	0.018					
BN53	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041	
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047	
			(HZ)	1.970	2.727	5.121							
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213							
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041	
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051	

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN31	ENI → Y1	(HH)		0.093	0.160	0.270	0.007	0.010	0.014			
		(LL)		0.240	0.365	0.675	0.010	0.013	0.018			
	Y0 → Y1	(HH)		0.117	0.183	0.298	0.007	0.010	0.014			
		(LL)		0.242	0.346	0.553	0.010	0.013	0.018			
	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
EN → Y0		(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
(ZH)			0.952	1.561	3.392				0.015	0.021	0.032	
		(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
ENI → Y1	(HH)		0.093	0.160	0.270	0.007	0.010	0.014				
	(LL)		0.240	0.365	0.675	0.010	0.013	0.018				
Y0 → Y1	(HH)		0.117	0.183	0.298	0.007	0.010	0.014				
	(LL)		0.242	0.346	0.553	0.010	0.013	0.018				
BN51	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
	(ZH)		0.952	1.561	3.392				0.015	0.021	0.032	
		(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
ENI → Y1	(HH)		0.093	0.160	0.270	0.007	0.010	0.014				
	(LL)		0.240	0.365	0.675	0.010	0.013	0.018				
Y0 → Y1	(HH)		0.117	0.183	0.298	0.007	0.010	0.014				
	(LL)		0.242	0.346	0.553	0.010	0.013	0.018				
BN35	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
	(ZH)		0.997	1.655	3.703				0.012	0.017	0.028	
		(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
ENI → Y1	(HH)		0.093	0.160	0.270	0.007	0.010	0.014				
	(LL)		0.240	0.365	0.675	0.010	0.013	0.018				
Y0 → Y1	(HH)		0.117	0.183	0.298	0.007	0.010	0.014				
	(LL)		0.242	0.346	0.553	0.010	0.013	0.018				
BN55	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
	(ZH)		0.997	1.655	3.703				0.012	0.017	0.028	
		(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
ENI → Y1	(HH)		0.093	0.160	0.270	0.007	0.010	0.014				
	(LL)		0.240	0.365	0.675	0.010	0.013	0.018				
Y0 → Y1	(HH)		0.117	0.183	0.298	0.007	0.010	0.014				
	(LL)		0.242	0.346	0.553	0.010	0.013	0.018				
BN3F	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
	(ZH)		1.036	1.734	3.989				0.011	0.015	0.027	
		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
ENI → Y1	(HH)		0.093	0.160	0.270	0.007	0.010	0.014				
	(LL)		0.240	0.365	0.675	0.010	0.013	0.018				
Y0 → Y1	(HH)		0.117	0.183	0.298	0.007	0.010	0.014				
	(LL)		0.242	0.346	0.553	0.010	0.013	0.018				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN5F	A → Y0	(HH)		0.588	1.038	2.740						
		(LL)		0.729	1.148	2.184						
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
	(ZH)		1.036	1.734	3.989				0.011	0.015	0.027	
		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
ENI → Y1	(HH)		0.093	0.160	0.270	0.007	0.010	0.014				
	(LL)		0.240	0.365	0.675	0.010	0.013	0.018				
Y0 → Y1	(HH)		0.117	0.183	0.298	0.007	0.010	0.014				
	(LL)		0.242	0.346	0.553	0.010	0.013	0.018				

[MEMO]

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## 1.2 TTL Level

### Chapter 1 Interface Block

Function	Input Buffer					5.0 V	
Block type							
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
Normal	FI02	FID2	FIU2	FIW2	1	3	
Schmitt	FIS2W	FDS2W	FUS2W	FWS2W	1	6	
Clock							

Logic Diagram for "Normal"	Truth Table																			
	<table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>	A	Y	1	1	0	0													
A	Y																			
1	1																			
0	0																			
Logic Diagram for "Schmitt"	Block type																			
	<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FI02 to FIW2</td> <td>A</td> <td>-</td> <td>Y</td> <td>34</td> </tr> <tr> <td>FIS2W to FWS2W</td> <td>A</td> <td>-</td> <td>Y</td> <td>37</td> </tr> </tbody> </table>	Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FI02 to FIW2	A	-	Y	34	FIS2W to FWS2W	A	-	Y	37
Block type	Input		Output																	
	Symbol	Fan-In	Symbol	Fan-Out																
FI02 to FIW2	A	-	Y	34																
FIS2W to FWS2W	A	-	Y	37																
Logic Diagram for "Clock"																				

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LDO</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FI02	A → Y	(HH)	0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012			
FID2	A → Y	(HH)	0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012			
FIU2	A → Y	(HH)	0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012			
FIW2	A → Y	(HH)	0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012			
FIS2W	A → Y	(HH)	1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)	2.208	3.267	5.483	0.012	0.015	0.022			
FDS2W	A → Y	(HH)	1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)	2.208	3.267	5.483	0.012	0.015	0.022			
FUS2W	A → Y	(HH)	1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)	2.208	3.267	5.483	0.012	0.015	0.022			
FWS2W	A → Y	(HH)	1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)	2.208	3.267	5.483	0.012	0.015	0.022			

### Chapter 1 Interface Block

Function	Input Buffer with failsafe					5.0 V	
Block type							
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
Normal	FIA2	FDA2			1	3	
Schmitt	FIE2W	FDE2W			1	6	
Clock							

Logic Diagram for "Normal" 	Truth Table <table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>	A	Y	1	1	0	0													
		A	Y																	
1	1																			
0	0																			
Logic Diagram for "Schmitt" 	<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FIA2 to FDA2</td> <td>A</td> <td>-</td> <td>Y</td> <td>34</td> </tr> <tr> <td>FIE2W to FDE2W</td> <td>A</td> <td>-</td> <td>Y</td> <td>37</td> </tr> </tbody> </table>	Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FIA2 to FDA2	A	-	Y	34	FIE2W to FDE2W	A	-	Y	37
	Block type		Input		Output															
Symbol		Fan-In	Symbol	Fan-Out																
FIA2 to FDA2	A	-	Y	34																
FIE2W to FDE2W	A	-	Y	37																
Logic Diagram for "Clock"																				

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIA2	A → Y	(HH) (LL)	0.176 0.138	0.266 0.198	0.417 0.328	0.011 0.007	0.016 0.009	0.022 0.012			
FDA2	A → Y	(HH) (LL)	0.176 0.138	0.266 0.198	0.417 0.328	0.011 0.007	0.016 0.009	0.022 0.012			
FIE2W	A → Y	(HH) (LL)	1.184 2.208	1.976 3.267	4.048 5.483	0.008 0.012	0.011 0.015	0.017 0.022			
FDE2W	A → Y	(HH) (LL)	1.184 2.208	1.976 3.267	4.048 5.483	0.008 0.012	0.011 0.015	0.017 0.022			

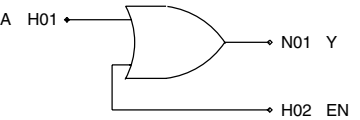
Chapter 1 Interface Block

Function	Input Buffer with EN(AND)					5.0 V																
Block type																						
Function	no resistor	with 50 KΩ P/D	with 50 KΩ P/U	with 5 KΩ P/U	I/O cells	int. Cells																
Normal	FN12	FN22			1	7																
Schmitt																						
Clock																						
Logic Diagram for "Normal"				Truth Table																		
				<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	0	1	0	0	1	1	1
A	EN	Y																				
0	0	0																				
0	1	0																				
1	0	0																				
1	1	1																				
Logic Diagram for "Schmitt"				<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FN12 to FN22</td> <td>A EN</td> <td>- 4.1</td> <td>Y</td> <td>35</td> </tr> </tbody> </table>				Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FN12 to FN22	A EN	- 4.1	Y	35	
Block type	Input		Output																			
	Symbol	Fan-In	Symbol	Fan-Out																		
FN12 to FN22	A EN	- 4.1	Y	35																		
Logic Diagram for "Clock"																						

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FN12	A → Y	(HH)	0.112	0.187	0.315	0.011	0.015	0.021			
		(LL)	0.160	0.234	0.371	0.007	0.008	0.012			
	EN → Y	(HH)	0.122	0.185	0.297	0.011	0.015	0.021			
		(LL)	0.173	0.245	0.345	0.007	0.008	0.011			
FN22	A → Y	(HH)	0.112	0.187	0.315	0.011	0.015	0.021			
		(LL)	0.160	0.234	0.371	0.007	0.008	0.012			
	EN → Y	(HH)	0.122	0.185	0.297	0.011	0.015	0.021			
		(LL)	0.173	0.245	0.345	0.007	0.008	0.011			

Chapter 1 Interface Block

Function	Input Buffer with EN(OR)					5.0 V																
Block type																						
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells																
Normal	FN14	FN24			1	4																
Schmitt																						
Clock																						
Logic Diagram for "Normal"				Truth Table																		
				<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	1	1	0	1	1	1	1
A	EN	Y																				
0	0	0																				
0	1	1																				
1	0	1																				
1	1	1																				
Logic Diagram for "Schmitt"				Block type																		
				Input		Output																
				Symbol	Fan-In	Symbol	Fan-Out															
				FN14 to FN24	A EN	- 2.0	Y 34															
Logic Diagram for "Clock"																						

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FN14	A → Y	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013			
	EN → Y	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
		(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
FN24	A → Y	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013			
	EN → Y	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
		(LL)	0.203	0.331	0.596	0.007	0.009	0.013			



Chapter 1 Interface Block

Function	I/O Buffer					TTL 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	B00V	B0DV	B0UV	B0WV	1	10	
6mA	B00D	B0DD	B0UD	B0WD	1	10	
9mA	B004	B0D4	B0U4	B0W4	1	10	
12mA	B002	B0D2	B0U2	B0W2	1	20	
18mA	B006	B0D6	B0U6	B0W6	1	20	
24mA	B00G	B0DG	B0UG	B0WG	1	20	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			B00V to B0WV	A	6.3
	B00D to B0WD	A	6.3	Y1	34
	B004 to B0W4	A	6.3	Y1	34
	B002 to B0W2	A	16.9	Y1	34
	B006 to B0W6	A	16.9	Y1	34
	B00G to B0WG	A	16.9	Y1	34

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B00V	A → Y0	(HH)		0.591	1.045	2.529				0.042	0.056	0.080
		(LL)		0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y0	(HZ)		1.088	1.523	2.712						
		(LZ)		0.380	0.577	0.996						
	Y0 → Y1	(ZH)		0.832	1.425	3.216				0.042	0.056	0.077
		(ZL)		0.771	1.385	2.985				0.077	0.103	0.150
B0DV	A → Y0	(HH)		0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)		0.138	0.197	0.328	0.007	0.009	0.012			
	EN → Y0	(HZ)		0.591	1.045	2.529				0.042	0.056	0.080
		(LZ)		0.380	0.577	0.996				0.076	0.103	0.149
	Y0 → Y1	(ZH)		0.832	1.425	3.216				0.042	0.056	0.077
		(ZL)		0.771	1.385	2.985				0.077	0.103	0.150
B0UV	A → Y0	(HH)		0.591	1.045	2.529				0.042	0.056	0.080
		(LL)		0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y0	(HZ)		1.088	1.523	2.712						
		(LZ)		0.380	0.577	0.996						
	Y0 → Y1	(ZH)		0.832	1.425	3.216				0.042	0.056	0.077
		(ZL)		0.771	1.385	2.985				0.077	0.103	0.150
B0WV	A → Y0	(HH)		0.591	1.045	2.529				0.042	0.056	0.080
		(LL)		0.710	1.257	2.776				0.076	0.103	0.149
	EN → Y0	(HZ)		1.088	1.523	2.712						
		(LZ)		0.380	0.577	0.996						
	Y0 → Y1	(ZH)		0.832	1.425	3.216				0.042	0.056	0.077
		(ZL)		0.771	1.385	2.985				0.077	0.103	0.150
B00D	A → Y0	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128						
	Y0 → Y1	(ZH)		0.851	1.454	3.330				0.029	0.039	0.056
		(ZL)		0.667	1.152	2.242				0.039	0.052	0.076
B0DD	A → Y0	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128						
	Y0 → Y1	(ZH)		0.851	1.454	3.330				0.029	0.039	0.056
		(ZL)		0.667	1.152	2.242				0.039	0.052	0.076
B0UD	A → Y0	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128						
	Y0 → Y1	(ZH)		0.851	1.454	3.330				0.029	0.039	0.056
		(ZL)		0.667	1.152	2.242				0.039	0.052	0.076

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0WD	A → Y0	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128						
		(ZH)		0.851	1.454	3.330				0.029	0.039	0.056
	Y0 → Y1	(ZL)		0.667	1.152	2.242				0.039	0.052	0.076
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B004	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0D4	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0U4	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0W4	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B002	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0D2	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0U2	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0W2	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B006	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0D6	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0U6	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B0W6	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					
B00G	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
(LL)		0.138	0.197	0.328	0.007	0.009	0.012					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BODG	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
		(HH)		0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)		0.138	0.197	0.328	0.007	0.009	0.012			
	BOUG	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015
(LL)				0.729	1.148	2.184				0.010	0.014	0.021
EN → Y0		(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
Y0 → Y1		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
		(HH)		0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)		0.138	0.197	0.328	0.007	0.009	0.012			
BOWG		A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015
	(LL)			0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
		(HH)		0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)		0.138	0.197	0.328	0.007	0.009	0.012			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise I/O Buffer					TTL 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BE0V	BEDV	BEUV	BEWV	1	10	
6mA	BE0D	BEDD	BEUD	BEWD	1	10	
9mA	BE04	BED4	BEU4	BEW4	1	10	
12mA	BE02	BED2	BEU2	BEW2	1	10	
18mA	BE06	BED6	BEU6	BEW6	1	10	
24mA	BE0G	BEDG	BEUG	BEWG	1	10	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			BE0V to BEWV	A	6.2
BE0D to BEWD	A	6.1	Y1	34	
BE04 to BEW4	A	6.2	Y1	34	
BE02 to BEW2	A	6.2	Y1	34	
BE06 to BEW6	A	6.2	Y1	34	
BE0G to BEWG	A	6.2	Y1	34	

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BE0V	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(HZ)	(LZ)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.176	0.266	0.417	0.011	0.016	0.022				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
BEDV	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	(ZH)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.176	0.266	0.417	0.011	0.016	0.022				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
BEUV	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	(ZH)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.176	0.266	0.417	0.011	0.016	0.022				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
BEWV	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	(ZH)	0.638	0.928	1.536						
			(ZH)	0.907	1.682	4.261				0.044	0.059	0.086
			(ZL)	0.940	1.673	3.375				0.077	0.104	0.151
Y0 → Y1	(HH)	(LL)	0.176	0.266	0.417	0.011	0.016	0.022				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
BE0D	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	(ZH)	0.817	1.158	1.799						
			(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
			(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
Y0 → Y1	(HH)	(LL)	0.176	0.266	0.417	0.011	0.016	0.022				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
BEDD	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	(ZH)	0.817	1.158	1.799						
			(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
			(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
Y0 → Y1	(HH)	(LL)	0.176	0.266	0.417	0.011	0.016	0.022				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
BEUD	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	(ZH)	0.817	1.158	1.799						
			(ZH)	0.943	1.755	4.570				0.031	0.042	0.066
			(ZL)	0.868	1.494	2.680				0.040	0.054	0.077
Y0 → Y1	(HH)	(LL)	0.176	0.266	0.417	0.011	0.016	0.022				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEWD	A → Y0	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
		(LL)		0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y0	(HZ)		0.948	1.269	2.217						
		(LZ)		0.817	1.158	1.799				0.031	0.042	0.066
		(ZH)		0.943	1.755	4.570				0.040	0.054	0.077
	Y0 → Y1	(ZL)		0.868	1.494	2.680						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BE04	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BED4	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BEU4	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BEW4	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BE02	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BED2	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEU2	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BEW2	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BE06	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BED6	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BEU6	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BEW6	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				
BE0G	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054				0.017	0.026	0.049
		(ZH)		1.236	2.487	7.732				0.017	0.023	0.029
	Y0 → Y1	(ZL)		0.934	1.621	2.393						
(HH)			0.176	0.266	0.417	0.011	0.016	0.022				
	(LL)		0.138	0.197	0.328	0.007	0.009	0.012				

Chapter 1 Interface Block

Block type	Switching speed										
	Path		tLDo (ns)			t1			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEDG	A → Y0	(HH)	1.429	2.521	7.676				0.015	0.025	0.049
		(LL)	1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)	2.920	3.913	7.573						
		(LZ)	1.791	2.376	3.054						
		(ZH)	1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)	0.934	1.621	2.393				0.017	0.023	0.029
		(HH)	0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012			
	BEUG	A → Y0	(HH)	1.429	2.521	7.676				0.015	0.025
(LL)			1.676	2.541	4.411				0.012	0.017	0.023
EN → Y0		(HZ)	2.920	3.913	7.573						
		(LZ)	1.791	2.376	3.054						
		(ZH)	1.236	2.487	7.732				0.017	0.026	0.049
Y0 → Y1		(ZL)	0.934	1.621	2.393				0.017	0.023	0.029
		(HH)	0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012			
BEWG		A → Y0	(HH)	1.429	2.521	7.676				0.015	0.025
	(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)	2.920	3.913	7.573						
		(LZ)	1.791	2.376	3.054						
		(ZH)	1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)	0.934	1.621	2.393				0.017	0.023	0.029
		(HH)	0.176	0.266	0.417	0.011	0.016	0.022			
		(LL)	0.138	0.197	0.328	0.007	0.009	0.012			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Schmitt I/O Buffer					TTL 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BSIVW	BSDVW	BSUVW	BSWVW	1	13	
6mA	BSIDW	BSDDW	BSUDW	BSWDW	1	13	
9mA	BSI4W	BSD4W	BSU4W	BSW4W	1	13	
12mA	BSI2W	BSD2W	BSU2W	BSW2W	1	23	
18mA	BSI6W	BSD6W	BSU6W	BSW6W	1	23	
24mA	BSIGW	BSDGW	BSUGW	BSGW	1	23	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		BSIVW to BSWVW	A	6.3	Y1
BSIDW to BSWDW	A	6.3	Y1	37	
	EN	1.0			
BSI4W to BSW4W	A	6.3	Y1	37	
	EN	1.0			
BSI2W to BSW2W	A	16.9	Y1	37	
	EN	1.0			
BSI6W to BSW6W	A	16.9	Y1	37	
	EN	1.0			
BSIGW to BSGW	A	16.9	Y1	37	
	EN	1.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			tLDo (ns)			t1			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BSIVW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.008	0.011	0.017	0.077	0.103
(HH)		1.184	1.976	4.048	0.008	0.011	0.017						
(LL)	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
BSDVW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.008	0.011	0.017	0.077	0.103
(HH)		1.184	1.976	4.048	0.008	0.011	0.017						
(LL)	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
BSUVW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.008	0.011	0.017	0.077	0.103
(HH)		1.184	1.976	4.048	0.008	0.011	0.017						
(LL)	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
BSWVW	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080	
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149	
	EN → Y0	(HZ)	1.088	1.523	2.712								
		(LZ)	0.380	0.577	0.996								
		(ZH)	0.832	1.425	3.216				0.042	0.056	0.077		
	Y0 → Y1	(ZL)	0.771	1.385	2.985				0.008	0.011	0.017	0.077	0.103
(HH)		1.184	1.976	4.048	0.008	0.011	0.017						
(LL)	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
BSIDW	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
	EN → Y0	(HZ)	1.413	1.971	3.618								
		(LZ)	0.451	0.675	1.128								
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056		
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.008	0.011	0.017	0.039	0.052
(HH)		1.184	1.976	4.048	0.008	0.011	0.017						
(LL)	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
BSDDW	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
	EN → Y0	(HZ)	1.413	1.971	3.618								
		(LZ)	0.451	0.675	1.128								
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056		
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.008	0.011	0.017	0.039	0.052
(HH)		1.184	1.976	4.048	0.008	0.011	0.017						
(LL)	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
BSUDW	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057	
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073	
	EN → Y0	(HZ)	1.413	1.971	3.618								
		(LZ)	0.451	0.675	1.128								
		(ZH)	0.851	1.454	3.330				0.029	0.039	0.056		
	Y0 → Y1	(ZL)	0.667	1.152	2.242				0.008	0.011	0.017	0.039	0.052
(HH)		1.184	1.976	4.048	0.008	0.011	0.017						
(LL)	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSWDW	A → Y0	(HH)		0.613	1.080	2.673				0.029	0.039	0.057
		(LL)		0.650	1.081	2.183				0.038	0.051	0.073
	EN → Y0	(HZ)		1.413	1.971	3.618						
		(LZ)		0.451	0.675	1.128						
		(ZH)		0.851	1.454	3.330				0.029	0.039	0.056
	Y0 → Y1	(ZL)		0.667	1.152	2.242				0.039	0.052	0.076
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSI4W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSD4W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSU4W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSW4W	A → Y0	(HH)		0.663	1.177	3.036				0.019	0.026	0.041
		(LL)		0.787	1.252	2.495				0.025	0.033	0.047
	EN → Y0	(HZ)		1.970	2.727	5.121						
		(LZ)		0.510	0.752	1.213						
		(ZH)		0.902	1.553	3.690				0.019	0.026	0.041
	Y0 → Y1	(ZL)		0.653	1.109	2.032				0.027	0.036	0.051
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSI2W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSD2W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSU2W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSW2W	A → Y0	(HH)		0.491	0.857	2.145				0.015	0.021	0.033
		(LL)		0.508	0.827	1.674				0.019	0.025	0.036
	EN → Y0	(HZ)		1.692	2.427	4.634						
		(LZ)		0.628	0.961	1.612						
		(ZH)		0.952	1.561	3.392				0.015	0.021	0.032
	Y0 → Y1	(ZL)		0.646	1.051	1.954				0.020	0.027	0.038
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSI6W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSD6W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSU6W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSW6W	A → Y0	(HH)		0.540	0.952	2.455				0.012	0.017	0.029
		(LL)		0.619	0.988	1.917				0.013	0.017	0.026
	EN → Y0	(HZ)		2.230	3.165	6.099						
		(LZ)		0.713	1.069	1.724						
		(ZH)		0.997	1.655	3.703				0.012	0.017	0.028
	Y0 → Y1	(ZL)		0.647	1.048	1.880				0.014	0.019	0.027
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BSIGW	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				



Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSDGW	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015	0.028
		(LL)		0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
		(HH)		1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)		2.208	3.267	5.483	0.012	0.015	0.022			
	BSUGW	A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015
(LL)				0.729	1.148	2.184				0.010	0.014	0.021
EN → Y0		(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
Y0 → Y1		(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
		(HH)		1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)		2.208	3.267	5.483	0.012	0.015	0.022			
BSWGW		A → Y0	(HH)		0.588	1.038	2.740				0.011	0.015
	(LL)			0.729	1.148	2.184				0.010	0.014	0.021
	EN → Y0	(HZ)		2.768	3.922	7.625						
		(LZ)		0.796	1.176	1.839						
		(ZH)		1.036	1.734	3.989				0.011	0.015	0.027
	Y0 → Y1	(ZL)		0.650	1.054	1.852				0.011	0.016	0.022
		(HH)		1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)		2.208	3.267	5.483	0.012	0.015	0.022			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise Schmitt I/O Buffer					TTL 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BF1VW	BFDVW	BFUVW	BFVWW	1	13	
6mA	BF1DW	BFDDW	BFUDW	BFVDW	1	13	
9mA	BF14W	BFD4W	BFU4W	BFV4W	1	13	
12mA	BF12W	BFD2W	BFU2W	BFV2W	1	13	
18mA	BF16W	BFD6W	BFU6W	BFV6W	1	13	
24mA	BF1GW	BFDGW	BFUGW	BFVGW	1	13	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			BF1VW to BFVWW	A	6.2
EN	4.0				
	BF1DW to BFVDW	A	6.1	Y1	37
	EN	4.0			
	BF14W to BFV4W	A	6.2	Y1	37
	EN	4.0			
	BF12W to BFV2W	A	6.2	Y1	37
	EN	4.0			
	BF16W to BFV6W	A	6.2	Y1	37
	EN	4.0			
	BF1GW to BFVGW	A	6.2	Y1	37
	EN	4.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BF1VW	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	0.638	0.928	1.536							
		(ZH)	0.907	1.682	4.261				0.044	0.059	0.086	
		(ZL)	0.940	1.673	3.375				0.077	0.104	0.151	
Y0 → Y1	(HH)	1.184	1.976	4.048	0.008	0.011	0.017					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
BFDDW	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	0.638	0.928	1.536							
		(ZH)	0.907	1.682	4.261				0.044	0.059	0.086	
		(ZL)	0.940	1.673	3.375				0.077	0.104	0.151	
Y0 → Y1	(HH)	1.184	1.976	4.048	0.008	0.011	0.017					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
BFVWW	A → Y0	(HH)	(LL)	0.906	1.649	4.217				0.044	0.059	0.086
			(LL)	0.903	1.561	3.193				0.077	0.103	0.150
			(HZ)	0.697	0.916	1.493						
	EN → Y0	(LZ)	0.638	0.928	1.536							
		(ZH)	0.907	1.682	4.261				0.044	0.059	0.086	
		(ZL)	0.940	1.673	3.375				0.077	0.104	0.151	
Y0 → Y1	(HH)	1.184	1.976	4.048	0.008	0.011	0.017					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
BF1DW	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	0.817	1.158	1.799							
		(ZH)	0.943	1.755	4.570				0.031	0.042	0.066	
		(ZL)	0.868	1.494	2.680				0.040	0.054	0.077	
Y0 → Y1	(HH)	1.184	1.976	4.048	0.008	0.011	0.017					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
BFDDW	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	0.817	1.158	1.799							
		(ZH)	0.943	1.755	4.570				0.031	0.042	0.066	
		(ZL)	0.868	1.494	2.680				0.040	0.054	0.077	
Y0 → Y1	(HH)	1.184	1.976	4.048	0.008	0.011	0.017					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
BFUDW	A → Y0	(HH)	(LL)	0.951	1.724	4.530				0.031	0.042	0.066
			(LL)	0.874	1.428	2.630				0.039	0.053	0.075
			(HZ)	0.948	1.269	2.217						
	EN → Y0	(LZ)	0.817	1.158	1.799							
		(ZH)	0.943	1.755	4.570				0.031	0.042	0.066	
		(ZL)	0.868	1.494	2.680				0.040	0.054	0.077	
Y0 → Y1	(HH)	1.184	1.976	4.048	0.008	0.011	0.017					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					
	(LL)	2.208	3.267	5.483	0.012	0.015	0.022					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFWDW	A → Y0	(HH)		0.951	1.724	4.530				0.031	0.042	0.066
		(LL)		0.874	1.428	2.630				0.039	0.053	0.075
	EN → Y0	(HZ)		0.948	1.269	2.217						
		(LZ)		0.817	1.158	1.799				0.031	0.042	0.066
		(ZH)		0.943	1.755	4.570				0.040	0.054	0.077
	Y0 → Y1	(ZL)		0.868	1.494	2.680						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFI4W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFD4W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFU4W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFW4W	A → Y0	(HH)		1.027	1.876	5.188				0.022	0.031	0.053
		(LL)		1.034	1.615	2.959				0.026	0.035	0.049
	EN → Y0	(HZ)		1.369	1.836	3.377						
		(LZ)		0.981	1.364	2.013				0.022	0.031	0.053
		(ZH)		1.005	1.906	5.246				0.029	0.038	0.054
	Y0 → Y1	(ZL)		0.864	1.475	2.488						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFI2W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFD2W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFU2W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFW2W	A → Y0	(HH)		1.086	1.963	5.554				0.020	0.029	0.051
		(LL)		1.107	1.718	3.065				0.021	0.028	0.037
	EN → Y0	(HZ)		1.585	2.130	3.959						
		(LZ)		1.138	1.564	2.214				0.021	0.029	0.051
		(ZH)		1.039	1.989	5.597				0.023	0.031	0.043
	Y0 → Y1	(ZL)		0.873	1.486	2.412						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFI6W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFD6W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFU6W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFW6W	A → Y0	(HH)		1.249	2.239	6.618				0.017	0.026	0.049
		(LL)		1.391	2.128	3.712				0.015	0.020	0.028
	EN → Y0	(HZ)		2.247	3.020	5.777						
		(LZ)		1.467	1.974	2.649				0.018	0.026	0.049
		(ZH)		1.139	2.241	6.670				0.019	0.025	0.033
	Y0 → Y1	(ZL)		0.902	1.547	2.379						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				
BFIGW	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054				0.017	0.026	0.049
		(ZH)		1.236	2.487	7.732				0.017	0.023	0.029
	Y0 → Y1	(ZL)		0.934	1.621	2.393						
(HH)			1.184	1.976	4.048	0.008	0.011	0.017				
	(LL)		2.208	3.267	5.483	0.012	0.015	0.022				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFDGW	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025	0.049
		(LL)		1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
		(HH)		1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)		2.208	3.267	5.483	0.012	0.015	0.022			
	BFUGW	A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025
(LL)				1.676	2.541	4.411				0.012	0.017	0.023
EN → Y0		(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
Y0 → Y1		(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
		(HH)		1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)		2.208	3.267	5.483	0.012	0.015	0.022			
BFWGW		A → Y0	(HH)		1.429	2.521	7.676				0.015	0.025
	(LL)			1.676	2.541	4.411				0.012	0.017	0.023
	EN → Y0	(HZ)		2.920	3.913	7.573						
		(LZ)		1.791	2.376	3.054						
		(ZH)		1.236	2.487	7.732				0.017	0.026	0.049
	Y0 → Y1	(ZL)		0.934	1.621	2.393				0.017	0.023	0.029
		(HH)		1.184	1.976	4.048	0.008	0.011	0.017			
		(LL)		2.208	3.267	5.483	0.012	0.015	0.022			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	I/O Buffer with EN(AND)						TTL 5.0 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN2V	BN4V			1	14	
6mA	BN2D	BN4D			1	14	
9mA	BN24	BN44			1	14	
12mA	BN22	BN42			1	24	
18mA	BN26	BN46			1	24	
24mA	BN2G	BN4G			1	24	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	BN2V to BN4V	A	6.3	Y1	35
		EN	1.0		
		ENI	4.1		
	BN2D to BN4D	A	6.3	Y1	35
		EN	1.0		
		ENI	4.1		
	BN24 to BN44	A	6.3	Y1	35
		EN	1.0		
		ENI	4.1		
	BN22 to BN42	A	16.9	Y1	35
		EN	1.0		
		ENI	4.1		
BN26 to BN46	A	16.9	Y1	35	
	EN	1.0			
	ENI	4.1			
BN2G to BN4G	A	16.9	Y1	35	
	EN	1.0			
	ENI	4.1			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	0
1	0	0
1	1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN2V	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
			(HZ)	1.088	1.523	2.712						
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996						
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150
	ENI → Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021				
		(LL)	0.173	0.245	0.345	0.007	0.008	0.011				
	Y0 → Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021				
		(LL)	0.160	0.234	0.371	0.007	0.008	0.012				
BN4V	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
			(HZ)	1.088	1.523	2.712						
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996						
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150
	ENI → Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021				
		(LL)	0.173	0.245	0.345	0.007	0.008	0.011				
	Y0 → Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021				
		(LL)	0.160	0.234	0.371	0.007	0.008	0.012				
BN2D	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
			(HZ)	1.413	1.971	3.618						
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128						
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076
	ENI → Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021				
		(LL)	0.173	0.245	0.345	0.007	0.008	0.011				
	Y0 → Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021				
		(LL)	0.160	0.234	0.371	0.007	0.008	0.012				
BN4D	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
			(HZ)	1.413	1.971	3.618						
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128						
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076
	ENI → Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021				
		(LL)	0.173	0.245	0.345	0.007	0.008	0.011				
	Y0 → Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021				
		(LL)	0.160	0.234	0.371	0.007	0.008	0.012				
BN24	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
			(HZ)	1.970	2.727	5.121						
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213						
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051
	ENI → Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021				
		(LL)	0.173	0.245	0.345	0.007	0.008	0.011				
	Y0 → Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021				
		(LL)	0.160	0.234	0.371	0.007	0.008	0.012				
BN44	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
			(HZ)	1.970	2.727	5.121						
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213						
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	ENI	→	Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021			
				(LL)	0.173	0.245	0.345	0.007	0.008	0.011			
	Y0	→	Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021			
BN22	A	→	Y0	(HH)	0.491	0.857	2.145				0.015	0.021	0.033
				(LL)	0.508	0.827	1.674				0.019	0.025	0.036
				(LZ)	0.628	0.961	1.612						
	EN	→	Y0	(HZ)	1.692	2.427	4.634						
				(ZH)	0.952	1.561	3.392				0.015	0.021	0.032
				(ZL)	0.646	1.051	1.954				0.020	0.027	0.038
	ENI	→	Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021			
				(LL)	0.173	0.245	0.345	0.007	0.008	0.011			
				(HH)	0.112	0.187	0.315	0.011	0.015	0.021			
	Y0	→	Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021			
				(LL)	0.160	0.234	0.371	0.007	0.008	0.012			

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BN4G	A	→	Y0	(HH)	0.588	1.038	2.740				0.011	0.015	0.028
				(LL)	0.729	1.148	2.184				0.010	0.014	0.021
				(LZ)	0.796	1.176	1.839						
	EN	→	Y0	(HZ)	2.768	3.922	7.625						
				(ZH)	1.036	1.734	3.989				0.011	0.015	0.021
				(ZL)	0.650	1.054	1.852				0.011	0.016	0.022
	ENI	→	Y1	(HH)	0.122	0.185	0.297	0.011	0.015	0.021			
				(LL)	0.173	0.245	0.345	0.007	0.008	0.011			
				(HH)	0.112	0.187	0.315	0.011	0.015	0.021			
	Y0	→	Y1	(HH)	0.112	0.187	0.315	0.011	0.015	0.021			
				(LL)	0.160	0.234	0.371	0.007	0.008	0.012			

Chapter 1 Interface Block

Function	I/O Buffer with EN(OR)					TTL 5.0 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN3V	BN5V			1	11	
6mA	BN3D	BN5D			1	11	
9mA	BN34	BN54			1	11	
12mA	BN32	BN52			1	21	
18mA	BN36	BN56			1	21	
24mA	BN3G	BN5G			1	21	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			BN3V to BN5V	A	6.3
	EN	1.0			
		ENI	2.0		
	BN3D to BN5D	A	6.3	Y1	34
		EN	1.0		
		ENI	2.0		
	BN34 to BN54	A	6.3	Y1	34
		EN	1.0		
		ENI	2.0		
	BN32 to BN52	A	16.9	Y1	34
		EN	1.0		
		ENI	2.0		
	BN36 to BN56	A	16.9	Y1	34
		EN	1.0		
		ENI	2.0		
	BN3G to BN5G	A	16.9	Y1	34
		EN	1.0		
		ENI	2.0		

A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	1
1	0	1
1	1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN3V	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
			(HZ)	1.088	1.523	2.712						
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996						
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150
	ENI → Y1	(HH)	(LL)	0.164	0.241	0.365	0.011	0.015	0.022			
			(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
			(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
Y0 → Y1	(HH)	(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
BN5V	A → Y0	(HH)	(LL)	0.591	1.045	2.529				0.042	0.056	0.080
			(LL)	0.710	1.257	2.776				0.076	0.103	0.149
			(HZ)	1.088	1.523	2.712						
	EN → Y0	(HZ)	(LZ)	0.380	0.577	0.996						
			(ZH)	0.832	1.425	3.216				0.042	0.056	0.077
			(ZL)	0.771	1.385	2.985				0.077	0.103	0.150
	ENI → Y1	(HH)	(LL)	0.164	0.241	0.365	0.011	0.015	0.022			
			(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
			(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
Y0 → Y1	(HH)	(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
BN3D	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
			(HZ)	1.413	1.971	3.618						
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128						
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076
	ENI → Y1	(HH)	(LL)	0.164	0.241	0.365	0.011	0.015	0.022			
			(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
			(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
Y0 → Y1	(HH)	(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
BN5D	A → Y0	(HH)	(LL)	0.613	1.080	2.673				0.029	0.039	0.057
			(LL)	0.650	1.081	2.183				0.038	0.051	0.073
			(HZ)	1.413	1.971	3.618						
	EN → Y0	(HZ)	(LZ)	0.451	0.675	1.128						
			(ZH)	0.851	1.454	3.330				0.029	0.039	0.056
			(ZL)	0.667	1.152	2.242				0.039	0.052	0.076
	ENI → Y1	(HH)	(LL)	0.164	0.241	0.365	0.011	0.015	0.022			
			(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
			(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
Y0 → Y1	(HH)	(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
BN34	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
			(HZ)	1.970	2.727	5.121						
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213						
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051
	ENI → Y1	(HH)	(LL)	0.164	0.241	0.365	0.011	0.015	0.022			
			(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
			(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
Y0 → Y1	(HH)	(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
		(LL)	0.223	0.311	0.432	0.007	0.009	0.013				
BN54	A → Y0	(HH)	(LL)	0.663	1.177	3.036				0.019	0.026	0.041
			(LL)	0.787	1.252	2.495				0.025	0.033	0.047
			(HZ)	1.970	2.727	5.121						
	EN → Y0	(HZ)	(LZ)	0.510	0.752	1.213						
			(ZH)	0.902	1.553	3.690				0.019	0.026	0.041
			(ZL)	0.653	1.109	2.032				0.027	0.036	0.051

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	ENI	→	Y1	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
				(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
	Y0	→	Y1	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
				(LL)	0.223	0.311	0.432	0.007	0.009	0.013			
BN32	A	→	Y0	(HH)	0.491	0.857	2.145				0.015	0.021	0.033
				(LL)	0.508	0.827	1.674				0.019	0.025	0.036
	EN	→	Y0	(HZ)	1.692	2.427	4.634						
				(LZ)	0.628	0.961	1.612						
				(ZH)	0.952	1.561	3.392				0.015	0.021	0.032
				(ZL)	0.646	1.051	1.954				0.020	0.027	0.038
	ENI	→	Y1	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
				(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
	Y0	→	Y1	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
				(LL)	0.223	0.311	0.432	0.007	0.009	0.013			
BN52	A	→	Y0	(HH)	0.491	0.857	2.145				0.015	0.021	0.033
				(LL)	0.508	0.827	1.674				0.019	0.025	0.036
	EN	→	Y0	(HZ)	1.692	2.427	4.634						
				(LZ)	0.628	0.961	1.612						
				(ZH)	0.952	1.561	3.392				0.015	0.021	0.032
				(ZL)	0.646	1.051	1.954				0.020	0.027	0.038
	ENI	→	Y1	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
				(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
	Y0	→	Y1	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
				(LL)	0.223	0.311	0.432	0.007	0.009	0.013			
BN36	A	→	Y0	(HH)	0.540	0.952	2.455				0.012	0.017	0.029
				(LL)	0.619	0.988	1.917				0.013	0.017	0.026
	EN	→	Y0	(HZ)	2.230	3.165	6.099						
				(LZ)	0.713	1.069	1.724						
				(ZH)	0.997	1.655	3.703				0.012	0.017	0.028
				(ZL)	0.647	1.048	1.880				0.014	0.019	0.027
	ENI	→	Y1	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
				(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
	Y0	→	Y1	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
				(LL)	0.223	0.311	0.432	0.007	0.009	0.013			
BN56	A	→	Y0	(HH)	0.540	0.952	2.455				0.012	0.017	0.029
				(LL)	0.619	0.988	1.917				0.013	0.017	0.026
	EN	→	Y0	(HZ)	2.230	3.165	6.099						
				(LZ)	0.713	1.069	1.724						
				(ZH)	0.997	1.655	3.703				0.012	0.017	0.028
				(ZL)	0.647	1.048	1.880				0.014	0.019	0.027
	ENI	→	Y1	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
				(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
	Y0	→	Y1	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
				(LL)	0.223	0.311	0.432	0.007	0.009	0.013			
BN3G	A	→	Y0	(HH)	0.588	1.038	2.740				0.011	0.015	0.028
				(LL)	0.729	1.148	2.184				0.010	0.014	0.021
	EN	→	Y0	(HZ)	2.768	3.922	7.625						
				(LZ)	0.796	1.176	1.839						
				(ZH)	1.036	1.734	3.989				0.011	0.015	0.027
				(ZL)	0.650	1.054	1.852				0.011	0.016	0.022
	ENI	→	Y1	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
				(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
	Y0	→	Y1	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
				(LL)	0.223	0.311	0.432	0.007	0.009	0.013			

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BN5G	A	→	Y0	(HH)	0.588	1.038	2.740						
				(LL)	0.729	1.148	2.184						
	EN	→	Y0	(HZ)	2.768	3.922	7.625						
				(LZ)	0.796	1.176	1.839						
				(ZH)	1.036	1.734	3.989				0.011	0.015	0.027
				(ZL)	0.650	1.054	1.852				0.011	0.016	0.022
	ENI	→	Y1	(HH)	0.164	0.241	0.365	0.011	0.015	0.022			
				(LL)	0.203	0.331	0.596	0.007	0.009	0.013			
	Y0	→	Y1	(HH)	0.103	0.166	0.247	0.011	0.015	0.021			
				(LL)	0.223	0.311	0.432	0.007	0.009	0.013			



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## 1.3 Oscillator

[MEMO]

Chapter 1 Interface Block

Function	Oscillator Input Buffer											
Block type												
Function				I/O cells	int. cells							
Normal	OSI1			1	0							
Oscillation stop function												
-												
Logic Diagram		Block type	Input		Output							
		OSI1	Symbol	Fan-in	Symbol	Fan-out						
Truth Table												
<table border="1"> <tr> <td>XT1</td> <td>O</td> </tr> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>							XT1	O	0	0	1	1
XT1	O											
0	0											
1	1											

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI1	XT1 → O	(HH) (LL)	0.010 0.010	0.010 0.010	0.010 0.010	0.001 0.001	0.001 0.001	0.001 0.001			

Chapter 1 Interface Block

Function	Oscillator Input Buffer for Enable																			
Block type																				
Function				I/O cells	int. cells															
Normal																				
Oscillation stop function	OSI2			1	0															
-																				
Logic Diagram	Block type		Input		Output															
		Symbol	Fan-in	Symbol	Fan-out															
	OSI2	XT1 EN	- 3.0	O	10															
Truth Table																				
<table border="1"> <thead> <tr> <th>XT1</th> <th>EN</th> <th>O</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>X</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>						XT1	EN	O	0	0	0	1	0	1	1	1	1	0	1	X
XT1	EN	O																		
0	0	0																		
1	0	1																		
1	1	1																		
0	1	X																		

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI2	XT1 → O	(HH) (LL)	0.010 0.010	0.010 0.010	0.010 0.010	0.001 0.001	0.001 0.001	0.001 0.001			

Chapter 1 Interface Block

Function	Oscillator Input Buffer for OSO9											
Block type												
Function				I/O cells	int. cells							
Normal	OSI4			1	0							
Oscillation stop function												
-												
Logic Diagram		Block type	Input		Output							
		OSI4	Symbol	Fan-in	Symbol	Fan-out						
			XT1	-	O	10						
Truth Table												
<table border="1"> <tr> <td>XT1</td> <td>O</td> </tr> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>							XT1	O	0	0	1	1
XT1	O											
0	0											
1	1											

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI4	XT1 → O	(HH) (LL)	0.010 0.010	0.010 0.010	0.010 0.010	0.001 0.001	0.001 0.001	0.001 0.001			

Chapter 1 Interface Block

Function	Oscillator Output Buffer (Internal Feedback Resistor)					
Block type						
Function	MHz range	kHz range		I/O cells	int. cells	
External feedback Resistor						
Internal feedback Resistor	oso1			1	0	
Internal feedback Resistor Oscillation stop function						
Logic Diagram	Block type		Input		Output	
	oso1		Symbol	Fan-in	Symbol	Fan-out
			1.0	XT2 O2	- 52	
Truth Table						
I1	XT2	O2				
0	1	1				
1	0	0				

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
OSO1	I1	→	XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
				(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1	→	O2	(HL)	8.240	17.530	17.530	0.009	0.017	0.017			
				(LH)	4.649	9.408	9.408	0.008	0.014	0.014			

Chapter 1 Interface Block

Function	Oscillator Output Buffer (for Enable Type)																								
Block type																									
Function	MHz range	kHz range		I/O cells	int. cells																				
External feedback Resistor																									
Internal feedback Resistor																									
Internal feedback Resistor Oscillation stop function	OSO7			1	0																				
Logic Diagram	Block type		Input		Output																				
			Symbol	Fan-in	Symbol	Fan-out																			
	OSO7		I1	1.0	XT2	-																			
		EN	3.0	O2	52																				
Truth Table																									
<table border="1"> <thead> <tr> <th>I1</th> <th>EN</th> <th>XT2</th> <th>O2</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>X</td> <td>X</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>						I1	EN	XT2	O2	0	0	1	1	1	0	0	0	1	1	0	0	0	1	X	X
I1	EN	XT2	O2																						
0	0	1	1																						
1	0	0	0																						
1	1	0	0																						
0	1	X	X																						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSO7	I1	→	XT2 (HL)	0.010	0.010	0.010				0.001	0.001	0.001
			(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1	→	O2 (HL)	8.240	17.530	17.530	0.009	0.017	0.017			
			(LH)	4.649	9.408	9.408	0.008	0.014	0.014			

Chapter 1 Interface Block

Function	Oscillator Output Buffer (External Feedback Resistor)				
Block type					
Function	MHz range	kHz range		I/O cells	int. cells
External feedback Resistor	OSO9			1	0
Internal feedback Resistor					
Internal feedback Resistor Oscillation stop function					
Logic Diagram		Input		Output	
		Block type			
		Symbol	Fan-in	Symbol	Fan-out
		OSO9	I1 1.0	XT2 O2	- 52
Truth Table					
I1	XT2	O2			
0	1	1			
1	0	0			

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LDO</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
OSO9	I1	→	XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
				(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1	→	O2	(HL)	8.240	17.530	17.530	0.009	0.017	0.017			
				(LH)	4.649	9.408	9.408	0.008	0.014	0.014			



# **Chapter 2**

## **Function Block**

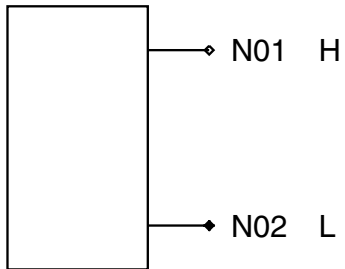
[MEMO]

## 2.1 Level Generator

Chapter 2 Function Block

Function	H, L Level Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
-	F091	1								
-										
-										
-										

Logic Diagram



Truth Table

H	L
1	0

Chapter 2 Function Block

Block type	Switching speed							Input		Output		
	Path			t LDo (ns)			t 1					
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol
F091											H	152
											L	152

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## 2.2 Inverter, Buffer, CTS Driver, Delay Gate

Chapter 2 Function Block

Function	Inverter											
Block type	Single output type						Multi output type					
	Name	cells					Name	cells				
Low Power	L101	1										
x1	F101	1										
x2	F102	2										
x3	F143	3										
x4	F144	4										
x5	F145	5										
x6	F146	6										
x8	F148	12										
Logic Diagram for "Single output type"												
Logic Diagram for "Multi output type 1"												
Logic Diagram for "Multi output type 2"												

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L101	A	→	Y	(HL) 0.089	(LH) 0.115	0.166	0.020	0.024	0.032	A	1.0	Y	17
F101	A	→	Y	(HL) 0.069	(LH) 0.088	0.122	0.010	0.012	0.016	A	2.0	Y	34
F102	A	→	Y	(HL) 0.065	(LH) 0.085	0.119	0.005	0.006	0.008	A	4.1	Y	69
F143	A	→	Y	(HL) 0.070	(LH) 0.090	0.123	0.003	0.004	0.005	A	6.2	Y	103
F144	A	→	Y	(HL) 0.067	(LH) 0.088	0.121	0.003	0.003	0.004	A	8.3	Y	139
F145	A	→	Y	(HL) 0.070	(LH) 0.090	0.123	0.002	0.002	0.003	A	10.4	Y	172
F146	A	→	Y	(HL) 0.069	(LH) 0.088	0.122	0.002	0.002	0.003	A	12.4	Y	207
F148	A	→	Y	(HL) 0.224	(LH) 0.351	0.623	0.001	0.002	0.002	A	4.1	Y	280

### Chapter 2 Function Block

Function	Buffer											
Block type	Single output type						Multi output type					
	Name	cells					Name	cells				
Low Power	L111	1										
x1	F111	2										
x2	F112	3										
x3	F153	4										
x4	F154	5										
x5												
x6												
x8	F158	11										
x12												

Logic Diagram for "Single output type"												
Logic Diagram for "Multi output type 1"												
Logic Diagram for "Multi output type 2"												

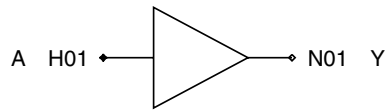
### Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L111	A	→	Y	(HH) 0.128	(LL) 0.126	(HH) 0.196 (LL) 0.198	(HH) 0.334 (LL) 0.356	(HH) 0.022 (LL) 0.020	(HH) 0.030 (LL) 0.024	(HH) 0.042 (LL) 0.033	A	1.0	Y	17
F111	A	→	Y	(HH) 0.095	(LL) 0.099	(HH) 0.144 (LL) 0.149	(HH) 0.243 (LL) 0.259	(HH) 0.011 (LL) 0.010	(HH) 0.015 (LL) 0.012	(HH) 0.021 (LL) 0.016	A	2.1	Y	35
F112	A	→	Y	(HH) 0.126	(LL) 0.129	(HH) 0.182 (LL) 0.194	(HH) 0.296 (LL) 0.333	(HH) 0.006 (LL) 0.005	(HH) 0.008 (LL) 0.006	(HH) 0.011 (LL) 0.008	A	2.1	Y	70
F153	A	→	Y	(HH) 0.151	(LL) 0.159	(HH) 0.216 (LL) 0.237	(HH) 0.350 (LL) 0.413	(HH) 0.004 (LL) 0.003	(HH) 0.005 (LL) 0.004	(HH) 0.007 (LL) 0.006	A	2.1	Y	104
F154	A	→	Y	(HH) 0.175	(LL) 0.183	(HH) 0.245 (LL) 0.276	(HH) 0.396 (LL) 0.482	(HH) 0.003 (LL) 0.003	(HH) 0.004 (LL) 0.004	(HH) 0.005 (LL) 0.004	A	2.1	Y	139
F158	A	→	Y	(HH) 0.148	(LL) 0.151	(HH) 0.210 (LL) 0.226	(HH) 0.336 (LL) 0.389	(HH) 0.001 (LL) 0.001	(HH) 0.002 (LL) 0.002	(HH) 0.003 (LL) 0.002	A	6.2	Y	278

### Chapter 2 Function Block

Function	CTS Driver (Inverter Type)										
Block type	Single type (Small scale circuit)			Standard type (Middle scale circuit)			Double type (Large scale circuit)				
	Name	cells		Name	cells		Name	cells			
x1	FC42	132					FC44	340			
x2	FC82	396					FC84	1020			
x3											
x4											
x5											
-											
-											
-											

Logic Diagram



### Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
FC42	A	→	Y	(HH)	0.628	1.048	1.081	0.000	0.000	0.000	A	7.7	Y	4449
				(LL)	0.720	1.370	1.419	0.000	0.000	0.000				
FC82	A	→	Y	(HH)	0.480	0.807	1.285	0.000	0.000	0.000	A	3.8	Y	8963
				(LL)	0.480	0.834	1.277	0.000	0.000	0.000				
FC44	A	→	Y	(HH)	0.294	0.507	0.572	0.000	0.000	0.000	A	7.7	Y	8899
				(LL)	0.313	0.564	0.663	0.000	0.000	0.000				
FC84	A	→	Y	(HH)	0.702	1.178	2.133	0.000	0.000	0.000	A	3.8	Y	17926
				(LL)	0.681	1.124	2.008	0.000	0.000	0.000				



Chapter 2 Function Block

Function	Delay Gate									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
-	F131	6								
-	F132	10								
-										
-										

Logic Diagram



Truth Table

A	Y
0	0
1	1

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F131	A	→	Y	(HH) (LL)	0.968 0.901	1.620 1.492	3.278 2.893	0.011 0.011	0.016 0.015	0.022 0.022	A	1.0	Y	32
F132	A	→	Y	(HH) (LL)	1.899 1.829	3.212 3.085	6.581 6.198	0.011 0.011	0.016 0.015	0.022 0.022	A	1.0	Y	32

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## 2.3 OR(NOR)

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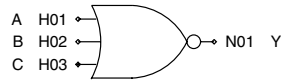
Chapter 2 Function Block

Function	2-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L202	1									
x1	F202	2									
x2	F222	4									
x4	F282	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L202	A	→	Y (HL)	0.079	0.113	0.167	0.020	0.024	0.033	A	1.0	Y	8
			(LH)	0.078	0.115	0.196	0.037	0.053	0.077				
	B	→	Y (HL)	0.093	0.128	0.196	0.020	0.024	0.033	B	1.0		
			(LH)	0.064	0.111	0.253	0.037	0.053	0.077				
F202	A	→	Y (HL)	0.086	0.121	0.182	0.010	0.012	0.016	A	2.1	Y	17
			(LH)	0.074	0.116	0.227	0.019	0.026	0.039				
	B	→	Y (HL)	0.086	0.121	0.182	0.010	0.012	0.016	B	2.1		
			(LH)	0.074	0.116	0.227	0.019	0.026	0.039				
F222	A	→	Y (HL)	0.084	0.121	0.183	0.005	0.006	0.008	A	4.1	Y	34
			(LH)	0.081	0.122	0.235	0.009	0.013	0.019				
	B	→	Y (HL)	0.084	0.121	0.183	0.005	0.006	0.008	B	4.1		
			(LH)	0.081	0.122	0.235	0.009	0.013	0.019				
F282	A	→	Y (HL)	0.263	0.414	0.734	0.003	0.003	0.004	A	1.0	Y	139
			(LH)	0.308	0.484	0.897	0.003	0.004	0.005				
	B	→	Y (HL)	0.278	0.434	0.774	0.003	0.003	0.004	B	1.0		
			(LH)	0.293	0.479	0.956	0.003	0.004	0.005				

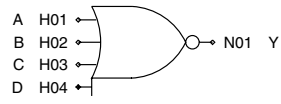
Chapter 2 Function Block

Function	3-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L203	2									
x1	F203	3									
x2	F223	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout				
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.								
L203	A → Y	(HL)		0.089	0.126	0.175	0.020	0.024	0.032	A	1.0	Y	4				
		(LH)		0.117	0.165	0.215	0.058	0.081	0.118								
	B → Y	(HL)		0.102	0.143	0.207	0.020	0.024	0.033					B	1.0		
		(LH)		0.121	0.199	0.374	0.058	0.082	0.118								
	C → Y	(HL)		0.110	0.155	0.213	0.020	0.025	0.035							C	1.0
		(LH)		0.126	0.256	0.548	0.059	0.082	0.119								
F203	A → Y	(HL)		0.083	0.118	0.151	0.011	0.013	0.017	A	2.1	Y	10				
		(LH)		0.106	0.162	0.256	0.029	0.041	0.059								
	B → Y	(HL)		0.093	0.134	0.178	0.010	0.013	0.018					B	2.1		
		(LH)		0.116	0.199	0.406	0.029	0.041	0.060								
	C → Y	(HL)		0.084	0.118	0.150	0.010	0.013	0.017							C	2.1
		(LH)		0.106	0.164	0.258	0.029	0.041	0.059								
F223	A → Y	(HL)		0.096	0.139	0.189	0.005	0.006	0.009	A	4.4	Y	17				
		(LH)		0.138	0.228	0.396	0.015	0.021	0.030								
	B → Y	(HL)		0.100	0.145	0.207	0.005	0.006	0.008					B	4.2		
		(LH)		0.137	0.215	0.391	0.015	0.021	0.030								
	C → Y	(HL)		0.096	0.139	0.189	0.005	0.006	0.009							C	4.3
		(LH)		0.139	0.228	0.397	0.015	0.021	0.030								

Chapter 2 Function Block

Function	4-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L204	2									
x1	F204	4									
x2											
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L204	A → Y	(HL)		0.087	0.125	0.173	0.020	0.024	0.032	A	1.0	Y	2		
		(LH)		0.114	0.153	0.157	0.074	0.104	0.152						
	B → Y	(HL)		0.099	0.142	0.205	0.020	0.024	0.033					B	1.0
		(LH)		0.132	0.211	0.377	0.074	0.105	0.153						
	C → Y	(HL)		0.106	0.154	0.213	0.020	0.025	0.035	C	1.0				
		(LH)		0.161	0.333	0.732	0.075	0.105	0.153						
	D → Y	(HL)		0.108	0.151	0.205	0.020	0.025	0.035	D	1.0				
		(LH)		0.158	0.342	0.797	0.075	0.105	0.153						
F204	A → Y	(HL)		0.197	0.325	0.585	0.010	0.012	0.017	A	1.0	Y	34		
		(LH)		0.272	0.446	0.878	0.011	0.015	0.022						
	B → Y	(HL)		0.214	0.345	0.622	0.010	0.012	0.017					B	1.0
		(LH)		0.257	0.440	0.936	0.011	0.015	0.022						
	C → Y	(HL)		0.215	0.351	0.609	0.010	0.013	0.017	C	1.0				
		(LH)		0.262	0.421	0.798	0.011	0.015	0.022						
	D → Y	(HL)		0.232	0.372	0.646	0.010	0.013	0.017	D	1.0				
		(LH)		0.248	0.416	0.854	0.011	0.015	0.022						

Chapter 2 Function Block

5-Input NOR											
Function											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L205	4									
x1	F205	5									
x2	F225	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L205	A → Y	(HL)		0.182	0.303	0.554	0.020	0.024	0.033	A	1.0	Y	16		
		(LH)		0.248	0.410	0.807	0.022	0.030	0.042						
	B → Y	(HL)		0.199	0.324	0.589	0.020	0.024	0.033					B	1.0
		(LH)		0.236	0.405	0.865	0.022	0.030	0.042						
	C → Y	(HL)		0.214	0.350	0.589	0.020	0.024	0.033					C	1.0
		(LH)		0.337	0.521	0.883	0.022	0.030	0.042						
	D → Y	(HL)		0.230	0.370	0.629	0.020	0.024	0.033	D	1.0				
		(LH)		0.340	0.551	1.043	0.022	0.030	0.042						
	E → Y	(HL)		0.241	0.386	0.651	0.020	0.025	0.033	E	1.0				
		(LH)		0.343	0.606	1.217	0.022	0.030	0.042						
F205	A → Y	(HL)		0.198	0.327	0.589	0.010	0.012	0.017	A	1.0	Y	34		
		(LH)		0.270	0.445	0.878	0.011	0.015	0.022						
	B → Y	(HL)		0.215	0.348	0.626	0.010	0.012	0.017					B	1.0
		(LH)		0.258	0.440	0.937	0.011	0.015	0.022						
	C → Y	(HL)		0.228	0.371	0.622	0.010	0.013	0.017					C	1.0
		(LH)		0.354	0.549	0.940	0.011	0.015	0.022						
	D → Y	(HL)		0.244	0.391	0.662	0.010	0.013	0.017	D	1.0				
		(LH)		0.357	0.578	1.101	0.011	0.015	0.022						
	E → Y	(HL)		0.254	0.406	0.688	0.010	0.013	0.017	E	1.0				
		(LH)		0.359	0.632	1.284	0.011	0.015	0.022						
F225	A → Y	(HL)		0.243	0.399	0.719	0.005	0.006	0.009	A	1.0	Y	66		
		(LH)		0.325	0.534	1.064	0.006	0.008	0.011						
	B → Y	(HL)		0.259	0.419	0.756	0.005	0.006	0.009					B	1.0
		(LH)		0.311	0.531	1.123	0.006	0.008	0.011						
	C → Y	(HL)		0.271	0.440	0.750	0.005	0.006	0.009					C	1.0
		(LH)		0.408	0.637	1.120	0.006	0.008	0.011						
	D → Y	(HL)		0.286	0.461	0.792	0.005	0.006	0.009	D	1.0				
		(LH)		0.410	0.666	1.279	0.006	0.008	0.011						
	E → Y	(HL)		0.297	0.477	0.826	0.005	0.006	0.009	E	1.0				
		(LH)		0.413	0.720	1.462	0.006	0.008	0.011						

Chapter 2 Function Block

Function	6-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F206	5									
x2	F226	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F206	A → Y	(HL)		0.210	0.344	0.596	0.010	0.012	0.017	A	1.0	Y	34
		(LH)		0.369	0.591	1.061	0.011	0.015	0.022	B	1.0		
	B → Y	(HL)		0.226	0.364	0.636	0.010	0.012	0.017	C	1.0		
		(LH)		0.374	0.622	1.225	0.011	0.015	0.022	D	1.0		
	C → Y	(HL)		0.235	0.378	0.659	0.010	0.012	0.017	E	1.0		
		(LH)		0.377	0.677	1.409	0.011	0.015	0.022	F	1.0		
	D → Y	(HL)		0.231	0.370	0.618	0.010	0.012	0.017				
		(LH)		0.358	0.555	0.949	0.011	0.015	0.022				
	E → Y	(HL)		0.245	0.390	0.659	0.010	0.012	0.017				
		(LH)		0.361	0.585	1.110	0.011	0.015	0.022				
	F → Y	(HL)		0.255	0.406	0.683	0.010	0.012	0.017				
		(LH)		0.365	0.639	1.296	0.011	0.015	0.022				
F226	A → Y	(HL)		0.264	0.429	0.746	0.005	0.006	0.009	A	1.0	Y	66
		(LH)		0.435	0.701	1.280	0.006	0.008	0.011	B	1.0		
	B → Y	(HL)		0.279	0.448	0.785	0.005	0.006	0.009	C	1.0		
		(LH)		0.440	0.732	1.444	0.006	0.008	0.011	D	1.0		
	C → Y	(HL)		0.289	0.466	0.821	0.005	0.006	0.009	E	1.0		
		(LH)		0.443	0.786	1.628	0.006	0.008	0.011	F	1.0		
	D → Y	(HL)		0.277	0.448	0.761	0.005	0.006	0.009				
		(LH)		0.409	0.640	1.125	0.006	0.008	0.011				
	E → Y	(HL)		0.292	0.469	0.803	0.005	0.006	0.009				
		(LH)		0.412	0.670	1.285	0.006	0.008	0.011				
	F → Y	(HL)		0.304	0.486	0.838	0.005	0.006	0.009				
		(LH)		0.416	0.725	1.472	0.006	0.008	0.011				



Chapter 2 Function Block

Function	8-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L208	7									
x1	F208	7									
x2	F228	8									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L208	A → Y	(HL)	0.202	0.344	0.659	0.020	0.025	0.033	A	1.0	Y	15	
		(LH)	0.333	0.582	1.326	0.022	0.030	0.044					
	B → Y	(HL)	0.217	0.364	0.696	0.020	0.025	0.033	B	1.0			
		(LH)	0.318	0.578	1.384	0.022	0.030	0.044					
	C → Y	(HL)	0.220	0.369	0.680	0.020	0.025	0.033	C	1.0			
		(LH)	0.343	0.593	1.299	0.022	0.030	0.044					
	D → Y	(HL)	0.234	0.389	0.718	0.020	0.025	0.033	D	1.0			
		(LH)	0.329	0.587	1.357	0.022	0.030	0.044					
	E → Y	(HL)	0.249	0.409	0.712	0.020	0.025	0.034	E	1.0			
		(LH)	0.368	0.626	1.299	0.022	0.030	0.044					
	F → Y	(HL)	0.265	0.429	0.749	0.020	0.025	0.034	F	1.0			
		(LH)	0.354	0.620	1.358	0.022	0.030	0.044					
	G → Y	(HL)	0.262	0.425	0.730	0.020	0.025	0.034	G	1.0			
		(LH)	0.375	0.632	1.289	0.022	0.030	0.044					
	H → Y	(HL)	0.275	0.445	0.767	0.020	0.025	0.034	H	1.0			
		(LH)	0.360	0.625	1.345	0.022	0.030	0.044					
F208	A → Y	(HL)	0.208	0.352	0.667	0.010	0.013	0.017	A	1.0	Y	31	
		(LH)	0.355	0.623	1.424	0.011	0.016	0.023					
	B → Y	(HL)	0.224	0.373	0.705	0.010	0.013	0.017	B	1.0			
		(LH)	0.340	0.618	1.482	0.011	0.016	0.023					
	C → Y	(HL)	0.226	0.377	0.688	0.010	0.013	0.017	C	1.0			
		(LH)	0.367	0.634	1.401	0.011	0.016	0.023					
	D → Y	(HL)	0.242	0.398	0.727	0.010	0.013	0.017	D	1.0			
		(LH)	0.351	0.628	1.457	0.011	0.016	0.023					
	E → Y	(HL)	0.253	0.418	0.723	0.010	0.013	0.017	E	1.0			
		(LH)	0.393	0.671	1.406	0.011	0.016	0.023					
	F → Y	(HL)	0.269	0.437	0.761	0.010	0.013	0.017	F	1.0			
		(LH)	0.379	0.664	1.464	0.011	0.016	0.023					
	G → Y	(HL)	0.264	0.431	0.738	0.010	0.013	0.017	G	1.0			
		(LH)	0.399	0.673	1.392	0.011	0.016	0.023					
	H → Y	(HL)	0.279	0.452	0.776	0.010	0.013	0.017	H	1.0			
		(LH)	0.383	0.667	1.447	0.011	0.016	0.023					
F228	A → Y	(HL)	0.259	0.429	0.801	0.005	0.007	0.009	A	1.0	Y	57	
		(LH)	0.452	0.790	1.782	0.006	0.008	0.012					
	B → Y	(HL)	0.273	0.450	0.840	0.005	0.007	0.009	B	1.0			
		(LH)	0.437	0.785	1.840	0.006	0.008	0.012					
	C → Y	(HL)	0.271	0.449	0.817	0.005	0.007	0.009	C	1.0			
		(LH)	0.456	0.790	1.738	0.006	0.008	0.012					
	D → Y	(HL)	0.286	0.470	0.856	0.005	0.007	0.009	D	1.0			
		(LH)	0.439	0.784	1.795	0.006	0.008	0.012					
	E → Y	(HL)	0.302	0.491	0.852	0.005	0.007	0.009	E	1.0			
		(LH)	0.487	0.831	1.750	0.006	0.008	0.012					
	F → Y	(HL)	0.316	0.513	0.892	0.005	0.007	0.009	F	1.0			
		(LH)	0.469	0.825	1.805	0.006	0.008	0.012					
	G → Y	(HL)	0.313	0.507	0.868	0.005	0.007	0.009	G	1.0			
		(LH)	0.491	0.832	1.730	0.006	0.008	0.012					
	H → Y	(HL)	0.327	0.527	0.907	0.005	0.007	0.009	H	1.0			
		(LH)	0.474	0.825	1.790	0.006	0.008	0.012					

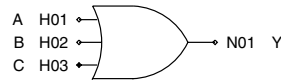
Chapter 2 Function Block

Function	2-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L212	2									
x1	F212	2									
x2	F232	3									
x4	F252	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.					MAX.
L212	A	→	Y (HH)	0.117	0.193	0.337	0.021	0.029	0.042	A	1.0	Y	17
			(LL)	0.182	0.283	0.515	0.020	0.025	0.034				
	B	→	Y (HH)	0.134	0.214	0.373	0.021	0.029	0.042	B	1.0		
			(LL)	0.169	0.279	0.573	0.020	0.025	0.034				
F212	A	→	Y (HH)	0.133	0.205	0.345	0.011	0.015	0.021	A	1.0	Y	34
			(LL)	0.207	0.320	0.579	0.010	0.013	0.018				
	B	→	Y (HH)	0.148	0.224	0.382	0.011	0.015	0.021	B	1.0		
			(LL)	0.194	0.317	0.639	0.010	0.013	0.018				
F232	A	→	Y (HH)	0.182	0.264	0.440	0.006	0.008	0.011	A	1.0	Y	68
			(LL)	0.280	0.445	0.815	0.005	0.007	0.010				
	B	→	Y (HH)	0.194	0.282	0.480	0.006	0.008	0.011	B	1.0		
			(LL)	0.265	0.442	0.875	0.005	0.007	0.010				
F252	A	→	Y (HH)	0.190	0.276	0.465	0.003	0.004	0.005	A	2.0	Y	139
			(LL)	0.278	0.449	0.852	0.003	0.003	0.005				
	B	→	Y (HH)	0.190	0.276	0.465	0.003	0.004	0.005	B	2.1		
			(LL)	0.278	0.449	0.853	0.003	0.003	0.005				

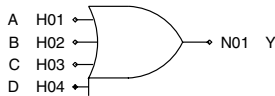
Chapter 2 Function Block

Function	3-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L213	2									
x1	F213	3									
x2	F233	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L213	A → Y	(HH)		0.130	0.212	0.347	0.022	0.030	0.042	A	1.0	Y	16
		(LL)		0.267	0.404	0.645	0.021	0.027	0.038				
	B → Y	(HH)		0.145	0.232	0.384	0.022	0.030	0.042	B	1.0		
		(LL)		0.270	0.433	0.803	0.021	0.027	0.038				
	C → Y	(HH)		0.153	0.244	0.404	0.022	0.030	0.043	C	1.0		
		(LL)		0.272	0.485	0.985	0.021	0.027	0.037				
F213	A → Y	(HH)		0.145	0.223	0.355	0.011	0.015	0.021	A	1.0	Y	34
		(LL)		0.307	0.468	0.759	0.011	0.014	0.020				
	B → Y	(HH)		0.159	0.241	0.397	0.011	0.015	0.021	B	1.0		
		(LL)		0.312	0.500	0.927	0.011	0.014	0.020				
	C → Y	(HH)		0.170	0.258	0.419	0.011	0.015	0.022	C	1.0		
		(LL)		0.317	0.557	1.113	0.011	0.014	0.020				
F233	A → Y	(HH)		0.191	0.278	0.449	0.006	0.008	0.011	A	1.0	Y	68
		(LL)		0.412	0.642	1.101	0.006	0.008	0.011				
	B → Y	(HH)		0.203	0.296	0.493	0.006	0.008	0.011	B	1.0		
		(LL)		0.416	0.679	1.274	0.006	0.008	0.011				
	C → Y	(HH)		0.215	0.315	0.525	0.006	0.008	0.011	C	1.0		
		(LL)		0.420	0.736	1.457	0.006	0.008	0.011				

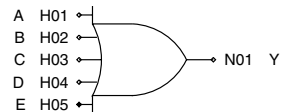
Chapter 2 Function Block

Function	4-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L214	3									
x1	F214	3									
x2	F234	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L214	A → Y	(HH)		0.127	0.211	0.346	0.021	0.030	0.042	A	1.0	Y	16		
		(LL)		0.298	0.446	0.678	0.022	0.028	0.040						
	B → Y	(HH)		0.142	0.232	0.386	0.021	0.029	0.042					B	1.0
		(LL)		0.315	0.500	0.901	0.022	0.028	0.041						
	C → Y	(HH)		0.153	0.247	0.409	0.021	0.030	0.043	C	1.0				
		(LL)		0.339	0.611	1.262	0.022	0.028	0.040						
	D → Y	(HH)		0.153	0.247	0.404	0.021	0.030	0.044	D	1.0				
		(LL)		0.336	0.626	1.331	0.022	0.028	0.041						
F214	A → Y	(HH)		0.142	0.220	0.353	0.011	0.015	0.021	A	1.0	Y	34		
		(LL)		0.343	0.517	0.804	0.011	0.015	0.021						
	B → Y	(HH)		0.155	0.239	0.393	0.011	0.015	0.021					B	1.0
		(LL)		0.359	0.574	1.049	0.011	0.015	0.022						
	C → Y	(HH)		0.167	0.255	0.419	0.011	0.015	0.022	C	1.0				
		(LL)		0.389	0.698	1.418	0.011	0.015	0.022						
	D → Y	(HH)		0.167	0.256	0.413	0.011	0.015	0.022	D	1.0				
		(LL)		0.383	0.708	1.487	0.011	0.015	0.022						
F234	A → Y	(HH)		0.188	0.276	0.446	0.006	0.008	0.011	A	1.0	Y	67		
		(LL)		0.471	0.736	1.233	0.006	0.008	0.012						
	B → Y	(HH)		0.200	0.295	0.491	0.006	0.008	0.011					B	1.0
		(LL)		0.490	0.802	1.496	0.006	0.008	0.012						
	C → Y	(HH)		0.213	0.314	0.525	0.006	0.008	0.011	C	1.0				
		(LL)		0.522	0.928	1.871	0.006	0.008	0.012						
	D → Y	(HH)		0.213	0.314	0.520	0.006	0.008	0.011	D	1.0				
		(LL)		0.517	0.937	1.936	0.006	0.008	0.012						

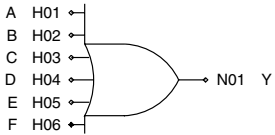
Chapter 2 Function Block

Function	5-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L215	4									
x1	F215	5									
x2	F235	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L215	A → Y	(HH)		0.115	0.192	0.335	0.022	0.030	0.042	A	1.0	Y	12
			(LL)	0.187	0.304	0.587	0.030	0.041	0.063				
	B → Y	(HH)		0.132	0.212	0.370	0.022	0.030	0.042	B	1.0		
			(LL)	0.176	0.299	0.645	0.030	0.041	0.063				
	C → Y	(HH)		0.139	0.226	0.361	0.022	0.030	0.042	C	1.0		
			(LL)	0.264	0.397	0.635	0.030	0.041	0.063				
	D → Y	(HH)		0.154	0.246	0.400	0.022	0.030	0.042	D	1.0		
			(LL)	0.266	0.426	0.792	0.030	0.041	0.062				
	E → Y	(HH)		0.164	0.262	0.421	0.022	0.030	0.043	E	1.0		
			(LL)	0.268	0.479	0.976	0.030	0.041	0.062				
F215	A → Y	(HH)		0.150	0.234	0.393	0.011	0.015	0.021	A	1.0	Y	24
			(LL)	0.228	0.359	0.676	0.015	0.021	0.031				
	B → Y	(HH)		0.164	0.253	0.430	0.011	0.015	0.021	B	1.0		
			(LL)	0.212	0.355	0.735	0.015	0.020	0.031				
	C → Y	(HH)		0.161	0.250	0.402	0.011	0.015	0.021	C	1.0		
			(LL)	0.333	0.519	0.878	0.015	0.021	0.032				
	D → Y	(HH)		0.174	0.269	0.443	0.011	0.015	0.021	D	1.0		
			(LL)	0.339	0.550	1.046	0.015	0.021	0.032				
	E → Y	(HH)		0.185	0.285	0.467	0.011	0.015	0.022	E	1.0		
			(LL)	0.341	0.606	1.230	0.015	0.021	0.032				
F235	A → Y	(HH)		0.252	0.415	0.761	0.006	0.008	0.011	A	1.0	Y	70
			(LL)	0.352	0.573	1.121	0.005	0.006	0.008				
	B → Y	(HH)		0.268	0.435	0.798	0.006	0.008	0.011	B	1.0		
			(LL)	0.337	0.569	1.180	0.005	0.006	0.008				
	C → Y	(HH)		0.279	0.456	0.789	0.006	0.008	0.011	C	1.0		
			(LL)	0.429	0.671	1.176	0.005	0.006	0.008				
	D → Y	(HH)		0.295	0.476	0.830	0.006	0.008	0.011	D	1.0		
			(LL)	0.432	0.702	1.336	0.005	0.006	0.008				
	E → Y	(HH)		0.305	0.491	0.856	0.006	0.008	0.011	E	1.0		
			(LL)	0.437	0.755	1.521	0.005	0.006	0.008				

Chapter 2 Function Block

6-Input OR											
Function											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L216	4									
x1	F216	5									
x2	F236	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout				
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.								
L216	A → Y	(HH)		0.136	0.219	0.357	0.023	0.031	0.043	A	1.0	Y	12				
		(LL)		0.299	0.467	0.790	0.031	0.042	0.066								
	B → Y	(HH)		0.150	0.239	0.395	0.023	0.031	0.043					B	1.0		
		(LL)		0.305	0.498	0.954	0.031	0.042	0.066								
	C → Y	(HH)		0.160	0.253	0.416	0.023	0.031	0.044							C	1.0
		(LL)		0.308	0.550	1.139	0.031	0.042	0.066								
	D → Y	(HH)		0.144	0.232	0.368	0.022	0.031	0.043	D	1.0						
		(LL)		0.271	0.406	0.647	0.030	0.041	0.063								
	E → Y	(HH)		0.158	0.252	0.408	0.022	0.031	0.043			E	1.0				
		(LL)		0.274	0.437	0.808	0.030	0.041	0.063								
	F → Y	(HH)		0.169	0.268	0.430	0.022	0.031	0.044					F	1.0		
		(LL)		0.278	0.491	0.994	0.030	0.041	0.063								
F216	A → Y	(HH)		0.168	0.265	0.441	0.011	0.015	0.021	A	1.0					Y	22
		(LL)		0.345	0.542	0.960	0.016	0.022	0.033								
	B → Y	(HH)		0.181	0.283	0.483	0.011	0.015	0.021			B	1.0				
		(LL)		0.349	0.576	1.126	0.016	0.022	0.033								
	C → Y	(HH)		0.191	0.299	0.508	0.011	0.015	0.022					C	1.0		
		(LL)		0.352	0.629	1.304	0.016	0.021	0.033								
	D → Y	(HH)		0.171	0.267	0.443	0.011	0.015	0.021	D	1.0						
		(LL)		0.353	0.556	0.976	0.016	0.022	0.033								
	E → Y	(HH)		0.184	0.285	0.484	0.011	0.015	0.021			E	1.0				
		(LL)		0.358	0.587	1.143	0.016	0.022	0.033								
	F → Y	(HH)		0.194	0.301	0.511	0.011	0.015	0.022					F	1.0		
		(LL)		0.362	0.646	1.329	0.016	0.022	0.033								
F236	A → Y	(HH)		0.268	0.439	0.780	0.006	0.008	0.011	A	1.0					Y	71
		(LL)		0.447	0.717	1.301	0.005	0.006	0.008								
	B → Y	(HH)		0.283	0.459	0.820	0.006	0.008	0.011			B	1.0				
		(LL)		0.451	0.747	1.466	0.005	0.006	0.008								
	C → Y	(HH)		0.293	0.473	0.843	0.006	0.008	0.011					C	1.0		
		(LL)		0.454	0.802	1.652	0.005	0.006	0.008								
	D → Y	(HH)		0.285	0.464	0.801	0.006	0.008	0.011	D	1.0						
		(LL)		0.432	0.677	1.182	0.005	0.006	0.008								
	E → Y	(HH)		0.301	0.484	0.842	0.006	0.008	0.011			E	1.0				
		(LL)		0.436	0.706	1.343	0.005	0.006	0.008								
	F → Y	(HH)		0.311	0.500	0.868	0.006	0.008	0.011					F	1.0		
		(LL)		0.439	0.761	1.528	0.005	0.006	0.008								

Chapter 2 Function Block

Function	8-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L218	6									
x1	F218	8									
x2	F238	9									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDo (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L218	A → Y	(HH)		0.128	0.216	0.401	0.022	0.030	0.042	A	1.0	Y	4
		(LL)		0.224	0.389	0.923	0.051	0.075	0.123	B	1.0		
	B → Y	(HH)		0.143	0.236	0.437	0.022	0.030	0.042	C	1.0	D	1.0
		(LL)		0.209	0.386	0.982	0.051	0.075	0.123	E	1.0		
	C → Y	(HH)		0.139	0.233	0.415	0.022	0.030	0.042	F	1.0	G	1.0
		(LL)		0.231	0.397	0.891	0.051	0.075	0.123	H	1.0		
	D → Y	(HH)		0.154	0.253	0.453	0.022	0.030	0.042				
		(LL)		0.217	0.392	0.948	0.051	0.075	0.123				
	E → Y	(HH)		0.158	0.261	0.440	0.022	0.030	0.042				
		(LL)		0.257	0.433	0.893	0.051	0.075	0.123				
	F → Y	(HH)		0.173	0.281	0.477	0.022	0.030	0.042				
		(LL)		0.243	0.427	0.951	0.051	0.075	0.123				
	G → Y	(HH)		0.163	0.267	0.448	0.022	0.030	0.042				
		(LL)		0.262	0.430	0.874	0.051	0.075	0.123				
	H → Y	(HH)		0.178	0.287	0.485	0.022	0.030	0.042				
		(LL)		0.246	0.426	0.930	0.051	0.075	0.123				
F218	A → Y	(HH)		0.241	0.408	0.781	0.011	0.015	0.021	A	1.0	Y	35
		(LL)		0.409	0.711	1.606	0.010	0.012	0.017	B	1.0		
	B → Y	(HH)		0.255	0.429	0.819	0.011	0.015	0.021	C	1.0	D	1.0
		(LL)		0.394	0.707	1.665	0.010	0.012	0.017	E	1.0		
	C → Y	(HH)		0.255	0.430	0.799	0.011	0.015	0.021	F	1.0	G	1.0
		(LL)		0.416	0.717	1.571	0.010	0.012	0.017	H	1.0		
	D → Y	(HH)		0.271	0.450	0.838	0.011	0.015	0.021				
		(LL)		0.401	0.711	1.628	0.010	0.012	0.017				
	E → Y	(HH)		0.287	0.476	0.843	0.011	0.015	0.021				
		(LL)		0.455	0.767	1.598	0.010	0.012	0.017				
	F → Y	(HH)		0.302	0.496	0.881	0.011	0.015	0.021				
		(LL)		0.439	0.762	1.655	0.010	0.012	0.017				
	G → Y	(HH)		0.291	0.484	0.853	0.011	0.015	0.021				
		(LL)		0.454	0.762	1.573	0.010	0.012	0.017				
	H → Y	(HH)		0.307	0.504	0.892	0.011	0.015	0.021				
		(LL)		0.439	0.757	1.628	0.010	0.012	0.017				
F238	A → Y	(HH)		0.266	0.447	0.852	0.006	0.008	0.011	A	1.0	Y	70
		(LL)		0.445	0.768	1.713	0.005	0.006	0.008	B	1.0		
	B → Y	(HH)		0.282	0.467	0.890	0.006	0.008	0.011	C	1.0	D	1.0
		(LL)		0.430	0.763	1.771	0.005	0.006	0.008	E	1.0		
	C → Y	(HH)		0.281	0.471	0.871	0.006	0.008	0.011	F	1.0	G	1.0
		(LL)		0.453	0.774	1.678	0.005	0.006	0.008	H	1.0		
	D → Y	(HH)		0.297	0.491	0.910	0.006	0.008	0.011				
		(LL)		0.438	0.768	1.734	0.005	0.006	0.008				
	E → Y	(HH)		0.322	0.528	0.930	0.006	0.008	0.011				
		(LL)		0.490	0.825	1.705	0.005	0.006	0.008				
	F → Y	(HH)		0.337	0.547	0.966	0.006	0.008	0.011				
		(LL)		0.476	0.819	1.762	0.005	0.006	0.008				
	G → Y	(HH)		0.324	0.531	0.931	0.006	0.008	0.011				
		(LL)		0.495	0.825	1.688	0.005	0.006	0.008				
	H → Y	(HH)		0.340	0.552	0.970	0.006	0.008	0.011				
		(LL)		0.479	0.819	1.742	0.005	0.006	0.008				

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## 2.4 AND(NAND)

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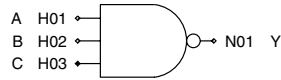
Chapter 2 Function Block

Function	2-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L302	1									
x1	F302	2									
x2	F322	4									
x4	F382	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L302	A	→	Y (HL)	0.104	0.137	0.225	0.030	0.040	0.061	A	1.0	Y	13
			(LH)	0.047	0.080	0.139	0.022	0.030	0.042	B	1.0		
F302	A	→	Y (HL)	0.093	0.128	0.211	0.015	0.020	0.031	A	2.1	Y	26
			(LH)	0.057	0.091	0.147	0.011	0.015	0.021	B	2.1		
F322	A	→	Y (HL)	0.095	0.133	0.216	0.007	0.010	0.015	A	4.2	Y	53
			(LH)	0.060	0.094	0.151	0.005	0.007	0.010	B	4.2		
F382	A	→	Y (HL)	0.318	0.489	0.901	0.003	0.003	0.004	A	1.0	Y	140
			(LH)	0.227	0.366	0.672	0.003	0.004	0.005	B	1.0		
			(HL)	0.298	0.464	0.869	0.003	0.003	0.004				
			(LH)	0.252	0.390	0.693	0.003	0.004	0.005				

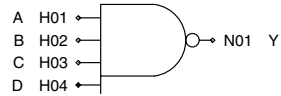
Chapter 2 Function Block

Function	3-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L303	2									
x1	F303	3									
x2	F323	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L303	A → Y	(HL)		0.138	0.210	0.460	0.041	0.058	0.093	A	1.0	Y	6
		(LH)		0.055	0.103	0.201	0.022	0.030	0.042				
	B → Y	(HL)		0.132	0.208	0.457	0.041	0.058	0.093	B	1.0	Y	6
		(LH)		0.071	0.121	0.217	0.021	0.029	0.042				
	C → Y	(HL)		0.128	0.211	0.456	0.041	0.058	0.093	C	1.0	Y	6
		(LH)		0.091	0.149	0.241	0.021	0.029	0.042				
F303	A → Y	(HL)		0.115	0.168	0.349	0.020	0.029	0.047	A	2.1	Y	15
		(LH)		0.062	0.106	0.187	0.011	0.015	0.021				
	B → Y	(HL)		0.124	0.183	0.363	0.020	0.029	0.047	B	2.1	Y	15
		(LH)		0.073	0.120	0.196	0.011	0.015	0.021				
	C → Y	(HL)		0.115	0.169	0.350	0.020	0.029	0.047	C	2.1	Y	15
		(LH)		0.063	0.107	0.188	0.011	0.015	0.021				
F323	A → Y	(HL)		0.141	0.220	0.472	0.010	0.015	0.023	A	4.3	Y	26
		(LH)		0.076	0.129	0.224	0.005	0.007	0.010				
	B → Y	(HL)		0.140	0.215	0.469	0.010	0.015	0.023	B	4.2	Y	26
		(LH)		0.073	0.126	0.221	0.005	0.007	0.010				
	C → Y	(HL)		0.142	0.220	0.471	0.010	0.015	0.023	C	4.3	Y	26
		(LH)		0.076	0.129	0.224	0.005	0.007	0.010				

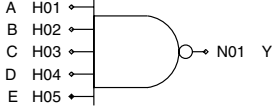
Chapter 2 Function Block

Function	4-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L304	2									
x1	F304	4									
x2	F324	8									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L304	A → Y	(HL)		0.142	0.215	0.535	0.051	0.074	0.123	A	1.0	Y	4		
		(LH)		0.052	0.100	0.200	0.022	0.030	0.042						
	B → Y	(HL)		0.145	0.229	0.549	0.051	0.074	0.123					B	1.0
		(LH)		0.067	0.119	0.216	0.022	0.029	0.042						
	C → Y	(HL)		0.158	0.258	0.576	0.051	0.075	0.123	C	1.0				
		(LH)		0.088	0.147	0.239	0.022	0.030	0.042						
	D → Y	(HL)		0.149	0.251	0.567	0.051	0.075	0.123			D	1.0		
		(LH)		0.094	0.154	0.249	0.022	0.030	0.042						
F304	A → Y	(HL)		0.156	0.249	0.572	0.025	0.037	0.062	A	2.1	Y	8		
		(LH)		0.075	0.129	0.228	0.011	0.015	0.021						
	B → Y	(HL)		0.163	0.259	0.584	0.025	0.037	0.062					B	2.1
		(LH)		0.081	0.137	0.233	0.011	0.015	0.021						
	C → Y	(HL)		0.163	0.259	0.583	0.025	0.037	0.062	C	2.1				
		(LH)		0.081	0.138	0.234	0.011	0.015	0.021						
	D → Y	(HL)		0.156	0.249	0.572	0.025	0.037	0.062			D	2.2		
		(LH)		0.074	0.129	0.228	0.011	0.015	0.021						
F324	A → Y	(HL)		0.157	0.251	0.572	0.013	0.019	0.031	A	4.4	Y	17		
		(LH)		0.074	0.130	0.229	0.005	0.008	0.011						
	B → Y	(HL)		0.164	0.259	0.586	0.013	0.019	0.031					B	4.4
		(LH)		0.081	0.138	0.234	0.005	0.007	0.010						
	C → Y	(HL)		0.164	0.260	0.585	0.013	0.019	0.031	C	4.4				
		(LH)		0.081	0.138	0.234	0.005	0.007	0.010						
	D → Y	(HL)		0.157	0.250	0.571	0.013	0.019	0.031			D	4.4		
		(LH)		0.074	0.130	0.228	0.006	0.008	0.011						

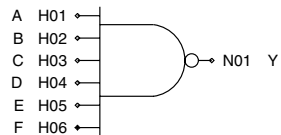
Chapter 2 Function Block

Function	5-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F305	5									
x2	F325	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F305	A → Y	(HL)	0.306	0.488	0.904	0.010	0.013	0.018	A	1.0	Y	35	
		(LH)	0.172	0.289	0.544	0.011	0.015	0.021					
	B → Y	(HL)	0.288	0.465	0.872	0.010	0.013	0.018	B	1.0			
		(LH)	0.194	0.318	0.563	0.011	0.015	0.021	C	1.0			
	C → Y	(HL)	0.366	0.601	1.266	0.010	0.013	0.018	D	1.0	E	1.0	
		(LH)	0.191	0.339	0.683	0.011	0.015	0.021					
	D → Y	(HL)	0.359	0.596	1.260	0.010	0.013	0.018	E	1.0			
		(LH)	0.215	0.365	0.702	0.011	0.015	0.021					
	E → Y	(HL)	0.356	0.600	1.262	0.010	0.013	0.018					
		(LH)	0.245	0.401	0.733	0.011	0.015	0.021					
F325	A → Y	(HL)	0.378	0.608	1.132	0.005	0.007	0.010	A	1.0	Y	69	
		(LH)	0.207	0.341	0.640	0.006	0.008	0.011					
	B → Y	(HL)	0.361	0.585	1.100	0.005	0.007	0.010	B	1.0	C	1.0	
		(LH)	0.234	0.370	0.661	0.006	0.008	0.011					
	C → Y	(HL)	0.440	0.725	1.500	0.005	0.007	0.010	C	1.0	D	1.0	
		(LH)	0.231	0.399	0.795	0.006	0.008	0.011					
	D → Y	(HL)	0.432	0.718	1.492	0.005	0.007	0.010	D	1.0	E	1.0	
		(LH)	0.255	0.426	0.814	0.006	0.008	0.011					
	E → Y	(HL)	0.429	0.722	1.493	0.005	0.007	0.010	E	1.0			
		(LH)	0.286	0.463	0.845	0.006	0.008	0.011					

Chapter 2 Function Block

Function	6-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F306	5									
x2	F326	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
F306	A → Y	(HL)		0.372	0.607	1.254	0.010	0.013	0.018	A	1.0	Y	35		
		(LH)		0.180	0.321	0.639	0.011	0.015	0.021						
	B → Y	(HL)		0.366	0.603	1.247	0.010	0.013	0.018					B	1.0
		(LH)		0.204	0.346	0.657	0.011	0.015	0.021					C	1.0
	C → Y	(HL)		0.362	0.606	1.248	0.010	0.013	0.018					D	1.0
		(LH)		0.233	0.383	0.688	0.011	0.015	0.021					E	1.0
	D → Y	(HL)		0.371	0.609	1.276	0.010	0.013	0.018	F	1.0				
		(LH)		0.195	0.344	0.686	0.011	0.015	0.021						
	E → Y	(HL)		0.365	0.604	1.272	0.010	0.013	0.018						
		(LH)		0.218	0.370	0.708	0.011	0.015	0.021						
	F → Y	(HL)		0.361	0.607	1.273	0.010	0.013	0.018						
		(LH)		0.249	0.407	0.740	0.011	0.015	0.021						
F326	A → Y	(HL)		0.448	0.730	1.488	0.005	0.007	0.010	A	1.0	Y	69		
		(LH)		0.219	0.378	0.746	0.006	0.008	0.011						
	B → Y	(HL)		0.440	0.727	1.482	0.005	0.007	0.010					B	1.0
		(LH)		0.242	0.405	0.765	0.006	0.008	0.011					C	1.0
	C → Y	(HL)		0.439	0.731	1.483	0.005	0.007	0.010					D	1.0
		(LH)		0.275	0.444	0.797	0.006	0.008	0.011					E	1.0
	D → Y	(HL)		0.446	0.734	1.514	0.005	0.007	0.010	F	1.0				
		(LH)		0.235	0.404	0.800	0.006	0.008	0.011						
	E → Y	(HL)		0.439	0.728	1.509	0.005	0.007	0.010						
		(LH)		0.259	0.431	0.822	0.006	0.008	0.011						
	F → Y	(HL)		0.435	0.731	1.508	0.005	0.007	0.010						
		(LH)		0.290	0.469	0.852	0.006	0.008	0.011						

Chapter 2 Function Block

Function	8-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F308	6									
x2	F328	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F308	A → Y	(HL)		0.397	0.648	1.401	0.010	0.013	0.018	A	1.0	Y	35
		(LH)		0.174	0.314	0.631	0.011	0.015	0.021				
	B → Y	(HL)		0.402	0.661	1.413	0.010	0.013	0.018	B	1.0		
		(LH)		0.196	0.340	0.651	0.011	0.015	0.021				
	C → Y	(HL)		0.411	0.688	1.443	0.010	0.013	0.018	C	1.0		
		(LH)		0.225	0.376	0.682	0.011	0.015	0.021				
	D → Y	(HL)		0.402	0.682	1.432	0.010	0.013	0.018	D	1.0		
		(LH)		0.234	0.388	0.694	0.011	0.015	0.021				
	E → Y	(HL)		0.390	0.639	1.403	0.010	0.013	0.018	E	1.0		
		(LH)		0.186	0.333	0.676	0.011	0.015	0.021				
	F → Y	(HL)		0.392	0.648	1.418	0.010	0.013	0.018	F	1.0		
		(LH)		0.208	0.360	0.696	0.011	0.015	0.021				
	G → Y	(HL)		0.402	0.676	1.444	0.010	0.013	0.018	G	1.0		
		(LH)		0.238	0.398	0.729	0.011	0.015	0.021				
	H → Y	(HL)		0.395	0.671	1.435	0.010	0.013	0.018	H	1.0		
		(LH)		0.248	0.410	0.742	0.011	0.015	0.021				
F328	A → Y	(HL)		0.475	0.778	1.646	0.005	0.007	0.010	A	1.0	Y	69
		(LH)		0.213	0.372	0.739	0.006	0.008	0.011				
	B → Y	(HL)		0.479	0.790	1.659	0.005	0.007	0.010	B	1.0		
		(LH)		0.236	0.399	0.759	0.006	0.008	0.011				
	C → Y	(HL)		0.490	0.819	1.687	0.005	0.007	0.010	C	1.0		
		(LH)		0.268	0.439	0.794	0.006	0.008	0.011				
	D → Y	(HL)		0.481	0.814	1.680	0.005	0.007	0.010	D	1.0		
		(LH)		0.278	0.453	0.806	0.006	0.008	0.011				
	E → Y	(HL)		0.467	0.768	1.646	0.005	0.007	0.010	E	1.0		
		(LH)		0.227	0.396	0.792	0.006	0.008	0.011				
	F → Y	(HL)		0.469	0.777	1.660	0.005	0.007	0.010	F	1.0		
		(LH)		0.250	0.422	0.811	0.006	0.008	0.011				
	G → Y	(HL)		0.481	0.806	1.689	0.005	0.007	0.010	G	1.0		
		(LH)		0.283	0.463	0.847	0.006	0.008	0.011				
	H → Y	(HL)		0.473	0.801	1.682	0.005	0.007	0.010	H	1.0		
		(LH)		0.294	0.476	0.859	0.006	0.008	0.011				

Chapter 2 Function Block

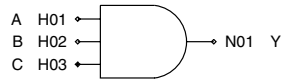
Function	2-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L312	2									
x1	F312	2									
x2	F332	3									
x4	F352	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L312	A	→	Y (HH)	0.165	0.251	0.452	0.021	0.030	0.042	A	1.0	Y	17
			(LL)	0.116	0.193	0.355	0.020	0.024	0.033				
	B	→	Y (HH)	0.149	0.227	0.421	0.021	0.030	0.042	B	1.0		
			(LL)	0.143	0.221	0.375	0.020	0.024	0.033				
F312	A	→	Y (HH)	0.184	0.274	0.499	0.011	0.015	0.022	A	1.0	Y	34
			(LL)	0.132	0.213	0.380	0.010	0.012	0.017				
	B	→	Y (HH)	0.164	0.248	0.467	0.011	0.015	0.022	B	1.0		
			(LL)	0.155	0.236	0.400	0.010	0.012	0.017				
F332	A	→	Y (HH)	0.242	0.361	0.673	0.006	0.008	0.011	A	1.0	Y	67
			(LL)	0.183	0.288	0.515	0.005	0.006	0.009				
	B	→	Y (HH)	0.217	0.334	0.640	0.006	0.008	0.011	B	1.0		
			(LL)	0.200	0.309	0.534	0.005	0.006	0.009				
F352	A	→	Y (HH)	0.231	0.351	0.663	0.003	0.004	0.006	A	2.1	Y	134
			(LL)	0.194	0.303	0.531	0.003	0.003	0.004				
	B	→	Y (HH)	0.231	0.350	0.662	0.003	0.004	0.006	B	2.1		
			(LL)	0.194	0.303	0.530	0.003	0.003	0.004				



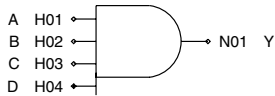
Chapter 2 Function Block

Function	3-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L313	2									
x1	F313	3									
x2	F333	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L313	A → Y	(HH)		0.225	0.360	0.776	0.022	0.030	0.043	A	1.0	Y	16
		(LL)		0.127	0.226	0.452	0.020	0.025	0.034				
	B → Y	(HH)		0.219	0.355	0.770	0.022	0.030	0.043				
		(LL)		0.150	0.253	0.471	0.020	0.025	0.034				
	C → Y	(HH)		0.213	0.358	0.770	0.022	0.030	0.043				
		(LL)		0.174	0.281	0.491	0.020	0.025	0.033				
F313	A → Y	(HH)		0.252	0.400	0.863	0.011	0.015	0.022	A	1.0	Y	33
		(LL)		0.142	0.243	0.470	0.010	0.013	0.017				
	B → Y	(HH)		0.243	0.394	0.854	0.011	0.015	0.022				
		(LL)		0.162	0.268	0.488	0.010	0.013	0.017				
	C → Y	(HH)		0.239	0.400	0.859	0.011	0.015	0.022				
		(LL)		0.190	0.304	0.518	0.010	0.013	0.017				
F333	A → Y	(HH)		0.322	0.515	1.112	0.006	0.008	0.012	A	1.0	Y	62
		(LL)		0.190	0.313	0.593	0.005	0.007	0.009				
	B → Y	(HH)		0.312	0.512	1.106	0.006	0.008	0.012				
		(LL)		0.207	0.338	0.613	0.005	0.007	0.009				
	C → Y	(HH)		0.306	0.516	1.106	0.006	0.008	0.012				
		(LL)		0.232	0.373	0.642	0.005	0.007	0.009				

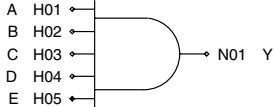
Chapter 2 Function Block

Function	4-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L314	3									
x1	F314	3									
x2	F334	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L314	A → Y	(HH)		0.254	0.408	0.928	0.022	0.030	0.044	A	1.0	Y	16		
		(LL)		0.124	0.224	0.452	0.020	0.025	0.033						
	B → Y	(HH)		0.257	0.418	0.941	0.022	0.030	0.044					B	1.0
		(LL)		0.146	0.251	0.472	0.020	0.025	0.033						
	C → Y	(HH)		0.267	0.446	0.967	0.022	0.030	0.044	C	1.0				
		(LL)		0.177	0.290	0.502	0.020	0.025	0.034						
	D → Y	(HH)		0.258	0.440	0.959	0.022	0.030	0.044	D	1.0				
		(LL)		0.187	0.303	0.518	0.020	0.025	0.034						
F314	A → Y	(HH)		0.280	0.450	1.033	0.011	0.016	0.023	A	1.0	Y	31		
		(LL)		0.136	0.237	0.463	0.010	0.013	0.017						
	B → Y	(HH)		0.281	0.461	1.045	0.011	0.016	0.023					B	1.0
		(LL)		0.155	0.262	0.483	0.010	0.013	0.017						
	C → Y	(HH)		0.293	0.492	1.077	0.011	0.016	0.023	C	1.0				
		(LL)		0.186	0.300	0.516	0.010	0.013	0.017						
	D → Y	(HH)		0.282	0.486	1.065	0.011	0.016	0.023	D	1.0				
		(LL)		0.194	0.312	0.528	0.010	0.013	0.017						
F334	A → Y	(HH)		0.365	0.599	1.364	0.006	0.008	0.012	A	1.0	Y	58		
		(LL)		0.186	0.309	0.588	0.005	0.006	0.009						
	B → Y	(HH)		0.366	0.612	1.377	0.006	0.008	0.012					B	1.0
		(LL)		0.202	0.334	0.610	0.005	0.007	0.009						
	C → Y	(HH)		0.377	0.643	1.406	0.006	0.008	0.012	C	1.0				
		(LL)		0.229	0.371	0.639	0.005	0.007	0.009						
	D → Y	(HH)		0.368	0.634	1.398	0.006	0.008	0.012	D	1.0				
		(LL)		0.237	0.384	0.655	0.005	0.007	0.009						

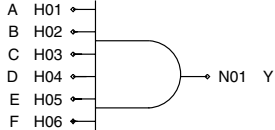
Chapter 2 Function Block

Function	5-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L315	4									
x1	F315	5									
x2	F335	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L315	A → Y	(HH)		0.178	0.278	0.508	0.038	0.053	0.077	A	1.0	Y	8
		(LL)		0.116	0.195	0.360	0.020	0.025	0.033				
	B → Y	(HH)		0.163	0.255	0.475	0.038	0.053	0.077	B	1.0		
		(LL)		0.141	0.223	0.381	0.020	0.025	0.033				
	C → Y	(HH)		0.238	0.391	0.867	0.038	0.053	0.077	C	1.0		
		(LL)		0.136	0.245	0.492	0.020	0.025	0.034				
	D → Y	(HH)		0.233	0.387	0.862	0.038	0.053	0.077	D	1.0		
		(LL)		0.160	0.271	0.514	0.020	0.025	0.034				
	E → Y	(HH)		0.228	0.390	0.862	0.038	0.053	0.077	E	1.0		
		(LL)		0.188	0.307	0.542	0.020	0.025	0.034				
F315	A → Y	(HH)		0.218	0.336	0.631	0.019	0.027	0.039	A	1.0	Y	16
		(LL)		0.152	0.248	0.450	0.010	0.013	0.017				
	B → Y	(HH)		0.197	0.310	0.598	0.019	0.027	0.039	B	1.0		
		(LL)		0.172	0.273	0.469	0.010	0.013	0.017				
	C → Y	(HH)		0.286	0.459	0.993	0.019	0.027	0.039	C	1.0		
		(LL)		0.159	0.275	0.534	0.010	0.013	0.018				
	D → Y	(HH)		0.277	0.454	0.986	0.019	0.027	0.039	D	1.0		
		(LL)		0.179	0.299	0.552	0.010	0.013	0.018				
	E → Y	(HH)		0.272	0.458	0.989	0.019	0.027	0.039	E	1.0		
		(LL)		0.205	0.334	0.582	0.010	0.013	0.018				
F335	A → Y	(HH)		0.358	0.578	1.087	0.006	0.008	0.011	A	1.0	Y	70
		(LL)		0.249	0.414	0.779	0.005	0.006	0.008				
	B → Y	(HH)		0.341	0.554	1.055	0.006	0.008	0.011	B	1.0		
		(LL)		0.271	0.442	0.800	0.005	0.006	0.008				
	C → Y	(HH)		0.420	0.691	1.451	0.006	0.008	0.011	C	1.0		
		(LL)		0.269	0.465	0.921	0.005	0.006	0.008				
	D → Y	(HH)		0.412	0.685	1.443	0.006	0.008	0.011	D	1.0		
		(LL)		0.292	0.491	0.940	0.005	0.006	0.008				
	E → Y	(HH)		0.409	0.689	1.446	0.006	0.008	0.011	E	1.0		
		(LL)		0.322	0.528	0.971	0.005	0.006	0.008				

Chapter 2 Function Block

Function	6-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L316	4									
x1	F316	5									
x2	F336	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L316	A → Y	(HH)		0.246	0.398	0.856	0.038	0.053	0.077	A	1.0	Y	8
		(LL)		0.128	0.230	0.460	0.020	0.025	0.034	B	1.0		
	B → Y	(HH)		0.241	0.394	0.850	0.038	0.053	0.077	C	1.0		
		(LL)		0.151	0.255	0.480	0.020	0.025	0.034	D	1.0		
	C → Y	(HH)		0.237	0.399	0.851	0.038	0.053	0.077	E	1.0		
		(LL)		0.180	0.293	0.511	0.020	0.025	0.034	F	1.0		
	D → Y	(HH)		0.242	0.397	0.876	0.038	0.053	0.077				
		(LL)		0.138	0.247	0.497	0.020	0.025	0.034				
	E → Y	(HH)		0.236	0.392	0.870	0.038	0.053	0.077				
		(LL)		0.161	0.273	0.515	0.020	0.025	0.034				
	F → Y	(HH)		0.232	0.395	0.870	0.038	0.053	0.077				
		(LL)		0.191	0.311	0.546	0.020	0.025	0.034				
F316	A → Y	(HH)		0.288	0.465	1.005	0.019	0.027	0.039	A	1.0	Y	16
		(LL)		0.164	0.282	0.550	0.010	0.012	0.017	B	1.0		
	B → Y	(HH)		0.278	0.459	0.999	0.019	0.027	0.039	C	1.0		
		(LL)		0.183	0.307	0.568	0.010	0.012	0.017	D	1.0		
	C → Y	(HH)		0.274	0.463	0.999	0.019	0.027	0.039	E	1.0		
		(LL)		0.211	0.344	0.599	0.010	0.013	0.017	F	1.0		
	D → Y	(HH)		0.290	0.466	1.010	0.019	0.027	0.039				
		(LL)		0.165	0.284	0.552	0.010	0.012	0.017				
	E → Y	(HH)		0.281	0.462	1.003	0.019	0.027	0.039				
		(LL)		0.185	0.308	0.572	0.010	0.013	0.017				
	F → Y	(HH)		0.277	0.467	1.005	0.019	0.027	0.039				
		(LL)		0.213	0.346	0.603	0.010	0.013	0.017				
F336	A → Y	(HH)		0.426	0.697	1.438	0.006	0.008	0.011	A	1.0	Y	70
		(LL)		0.258	0.446	0.875	0.005	0.006	0.008	B	1.0		
	B → Y	(HH)		0.419	0.694	1.432	0.006	0.008	0.011	C	1.0		
		(LL)		0.280	0.472	0.894	0.005	0.006	0.008	D	1.0		
	C → Y	(HH)		0.415	0.696	1.431	0.006	0.008	0.011	E	1.0		
		(LL)		0.309	0.508	0.925	0.005	0.006	0.008	F	1.0		
	D → Y	(HH)		0.425	0.698	1.462	0.006	0.008	0.011				
		(LL)		0.273	0.470	0.922	0.005	0.006	0.008				
	E → Y	(HH)		0.418	0.693	1.456	0.006	0.008	0.011				
		(LL)		0.295	0.495	0.945	0.005	0.006	0.008				
	F → Y	(HH)		0.414	0.697	1.457	0.006	0.008	0.011				
		(LL)		0.327	0.533	0.978	0.005	0.006	0.008				

Chapter 2 Function Block

Function	8-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L318	5									
x1	F318	6									
x2	F338	8									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L318	A → Y	(HH)		0.273	0.442	1.006	0.038	0.053	0.078	A	1.0	Y	8
		(LL)		0.122	0.224	0.454	0.020	0.025	0.033	B	1.0		
	B → Y	(HH)		0.276	0.453	1.018	0.038	0.053	0.078	C	1.0	Y	8
		(LL)		0.142	0.250	0.473	0.020	0.025	0.033	D	1.0		
	C → Y	(HH)		0.288	0.483	1.049	0.038	0.053	0.078	E	1.0	Y	8
		(LL)		0.173	0.289	0.507	0.020	0.025	0.034	F	1.0		
	D → Y	(HH)		0.278	0.477	1.040	0.038	0.053	0.078	G	1.0	Y	8
		(LL)		0.181	0.300	0.518	0.020	0.025	0.034	H	1.0		
	E → Y	(HH)		0.265	0.435	1.012	0.038	0.053	0.077			Y	8
		(LL)		0.133	0.242	0.492	0.020	0.025	0.034				
	F → Y	(HH)		0.269	0.444	1.025	0.038	0.053	0.077			Y	8
		(LL)		0.155	0.268	0.511	0.020	0.025	0.034				
	G → Y	(HH)		0.279	0.473	1.055	0.038	0.053	0.077			Y	8
		(LL)		0.186	0.308	0.545	0.020	0.025	0.034				
	H → Y	(HH)		0.270	0.468	1.046	0.038	0.053	0.077			Y	8
		(LL)		0.197	0.319	0.557	0.020	0.025	0.034				
F318	A → Y	(HH)		0.323	0.524	1.194	0.019	0.027	0.039	A	1.0	Y	16
		(LL)		0.159	0.277	0.544	0.010	0.012	0.017	B	1.0		
	B → Y	(HH)		0.324	0.536	1.207	0.019	0.027	0.039	C	1.0	Y	16
		(LL)		0.178	0.302	0.563	0.010	0.013	0.017	D	1.0		
	C → Y	(HH)		0.335	0.564	1.237	0.019	0.027	0.039	E	1.0	Y	16
		(LL)		0.206	0.340	0.596	0.010	0.013	0.017	F	1.0		
	D → Y	(HH)		0.326	0.559	1.224	0.019	0.027	0.039	G	1.0	Y	16
		(LL)		0.216	0.353	0.609	0.010	0.013	0.017	H	1.0		
	E → Y	(HH)		0.324	0.525	1.197	0.019	0.027	0.039			Y	16
		(LL)		0.159	0.278	0.545	0.010	0.012	0.017				
	F → Y	(HH)		0.325	0.537	1.209	0.019	0.027	0.039			Y	16
		(LL)		0.179	0.303	0.565	0.010	0.012	0.017				
	G → Y	(HH)		0.336	0.566	1.239	0.019	0.027	0.039			Y	16
		(LL)		0.207	0.341	0.598	0.010	0.013	0.017				
	H → Y	(HH)		0.327	0.561	1.227	0.019	0.027	0.039			Y	16
		(LL)		0.217	0.353	0.610	0.010	0.013	0.017				
F338	A → Y	(HH)		0.454	0.741	1.591	0.006	0.008	0.011	A	1.0	Y	70
		(LL)		0.252	0.441	0.869	0.005	0.006	0.008	B	1.0		
	B → Y	(HH)		0.458	0.754	1.605	0.006	0.008	0.011	C	1.0	Y	70
		(LL)		0.274	0.467	0.889	0.005	0.006	0.008	D	1.0		
	C → Y	(HH)		0.467	0.781	1.634	0.006	0.008	0.011	E	1.0	Y	70
		(LL)		0.303	0.503	0.920	0.005	0.006	0.008	F	1.0		
	D → Y	(HH)		0.459	0.777	1.624	0.006	0.008	0.011	G	1.0	Y	70
		(LL)		0.313	0.515	0.933	0.005	0.006	0.008	H	1.0		
	E → Y	(HH)		0.455	0.743	1.611	0.006	0.008	0.011			Y	70
		(LL)		0.269	0.467	0.925	0.005	0.006	0.008				
	F → Y	(HH)		0.456	0.752	1.624	0.006	0.008	0.011			Y	70
		(LL)		0.291	0.493	0.944	0.005	0.006	0.008				
	G → Y	(HH)		0.467	0.779	1.652	0.006	0.008	0.011			Y	70
		(LL)		0.321	0.531	0.977	0.005	0.006	0.008				
	H → Y	(HH)		0.459	0.774	1.643	0.006	0.008	0.011			Y	70
		(LL)		0.331	0.543	0.990	0.005	0.006	0.008				

[MEMO]

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## 2.5 AND-NOR

[MEMO]

Chapter 2 Function Block

Function	1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L421	2										
x1	F421	3										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L421	A → Y	(HL)		0.081	0.124	0.172	0.020	0.024	0.033	A	1.0	Y	7
		(LH)		0.070	0.194	0.247	0.029	0.058	0.082				
	B → Y	(HL)		0.132	0.196	0.385	0.031	0.042	0.064	B	1.0		
		(LH)		0.067	0.141	0.328	0.038	0.053	0.077				
	C → Y	(HL)		0.115	0.182	0.362	0.031	0.042	0.064	C	1.0		
		(LH)		0.116	0.215	0.401	0.042	0.058	0.082				
F421	A → Y	(HL)		0.070	0.104	0.134	0.010	0.013	0.016	A	2.1	Y	15
		(LH)		0.079	0.132	0.148	0.017	0.029	0.041				
	B → Y	(HL)		0.109	0.165	0.282	0.015	0.021	0.033	B	2.1		
		(LH)		0.087	0.158	0.305	0.021	0.029	0.042				
	C → Y	(HL)		0.109	0.166	0.282	0.015	0.020	0.033	C	2.1		
		(LH)		0.087	0.158	0.305	0.021	0.029	0.042				



Chapter 2 Function Block

Function	1-1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L422	2										
x1	F422	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output				
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.							
L422	A	→	Y	(HL)	0.091	0.134	0.180	0.020	0.024	0.032	A	1.0	Y	4		
				(LH)	0.113	0.233	0.279	0.049	0.082	0.118						
	B	→	Y	(HL)	0.103	0.152	0.213	0.020	0.024	0.033					B	1.0
				(LH)	0.110	0.267	0.444	0.049	0.082	0.118					C	1.0
	C	→	Y	(HL)	0.147	0.223	0.401	0.030	0.041	0.065	D	1.0				
				(LH)	0.125	0.264	0.562	0.059	0.082	0.119						
	D	→	Y	(HL)	0.120	0.195	0.367	0.030	0.041	0.065						
			(LH)	0.159	0.313	0.606	0.059	0.082	0.118							
F422	A	→	Y	(HL)	0.074	0.111	0.137	0.011	0.012	0.016	A	2.1	Y	8		
				(LH)	0.107	0.153	0.114	0.028	0.044	0.062						
	B	→	Y	(HL)	0.096	0.143	0.181	0.010	0.013	0.018					B	2.1
				(LH)	0.121	0.265	0.464	0.028	0.045	0.064					C	2.0
	C	→	Y	(HL)	0.118	0.187	0.307	0.016	0.021	0.035	D	2.0				
				(LH)	0.151	0.291	0.573	0.033	0.045	0.064						
	D	→	Y	(HL)	0.121	0.188	0.306	0.015	0.021	0.035						
			(LH)	0.150	0.293	0.577	0.033	0.045	0.064							

Chapter 2 Function Block

Function	1-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L423	2										
x1	F423	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L423	A → Y	(HL)		0.082	0.124	0.173	0.020	0.025	0.032	A	1.0	Y	5		
		(LH)		0.068	0.234	0.287	0.027	0.058	0.082						
	B → Y	(HL)		0.148	0.232	0.531	0.041	0.058	0.094					B	1.0
		(LH)		0.062	0.139	0.326	0.038	0.053	0.077						
	C → Y	(HL)		0.151	0.247	0.544	0.041	0.058	0.094	C	1.0				
		(LH)		0.111	0.215	0.396	0.042	0.058	0.083						
	D → Y	(HL)		0.134	0.236	0.530	0.041	0.058	0.094	D	1.0				
		(LH)		0.132	0.245	0.431	0.042	0.058	0.083						
F423	A → Y	(HL)		0.065	0.102	0.130	0.010	0.013	0.017	A	2.1	Y	11		
		(LH)		0.065	0.172	0.175	0.015	0.029	0.041						
	B → Y	(HL)		0.137	0.219	0.467	0.021	0.029	0.049					B	2.0
		(LH)		0.097	0.185	0.351	0.021	0.030	0.042						
	C → Y	(HL)		0.149	0.237	0.483	0.020	0.029	0.049	C	2.1				
		(LH)		0.112	0.208	0.370	0.021	0.030	0.042						
	D → Y	(HL)		0.135	0.219	0.468	0.021	0.030	0.049	D	2.1				
		(LH)		0.097	0.185	0.352	0.021	0.030	0.042						

Chapter 2 Function Block

Function	2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L424	2										
x1	F424	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L424	A → Y	(HL)		0.113	0.170	0.249	0.030	0.040	0.062	A	1.0	Y	6		
		(LH)		0.084	0.172	0.202	0.033	0.058	0.082						
	B → Y	(HL)		0.091	0.144	0.218	0.030	0.040	0.061					B	1.0
		(LH)		0.103	0.204	0.230	0.033	0.058	0.082						
	C → Y	(HL)		0.162	0.257	0.526	0.030	0.041	0.064	C	1.0				
		(LH)		0.085	0.244	0.459	0.032	0.058	0.083						
	D → Y	(HL)		0.137	0.232	0.494	0.029	0.041	0.064	D	1.0				
		(LH)		0.104	0.279	0.495	0.032	0.058	0.082						
F424	A → Y	(HL)		0.122	0.197	0.362	0.015	0.020	0.031	A	2.1	Y	11		
		(LH)		0.116	0.228	0.359	0.016	0.029	0.041						
	B → Y	(HL)		0.123	0.196	0.362	0.015	0.020	0.031					B	2.1
		(LH)		0.116	0.229	0.360	0.016	0.029	0.041						
	C → Y	(HL)		0.152	0.255	0.542	0.015	0.020	0.032	C	2.0				
		(LH)		0.106	0.259	0.517	0.016	0.029	0.041						
	D → Y	(HL)		0.152	0.255	0.540	0.015	0.020	0.032	D	2.0				
		(LH)		0.106	0.260	0.513	0.016	0.029	0.042						

Chapter 2 Function Block

Function	2-2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L425	3										
x1	F425	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L425	A → Y	(HL)		0.129	0.201	0.271	0.030	0.040	0.061	A	1.0	Y	2		
		(LH)		0.109	0.271	0.200	0.044	0.086	0.121						
	B → Y	(HL)		0.105	0.174	0.240	0.030	0.040	0.061					B	1.0
		(LH)		0.131	0.317	0.235	0.044	0.086	0.121					D	1.0
	C → Y	(HL)		0.181	0.281	0.547	0.029	0.041	0.064					E	1.0
		(LH)		0.139	0.467	0.735	0.044	0.087	0.124					F	1.0
	D → Y	(HL)		0.155	0.254	0.515	0.029	0.041	0.064						
		(LH)		0.163	0.519	0.783	0.044	0.086	0.123						
	E → Y	(HL)		0.208	0.348	0.731	0.030	0.042	0.068						
		(LH)		0.159	0.560	1.004	0.043	0.087	0.124						
	F → Y	(HL)		0.179	0.319	0.695	0.030	0.042	0.068						
		(LH)		0.186	0.610	1.060	0.043	0.086	0.123						
F425	A → Y	(HL)		0.140	0.228	0.388	0.015	0.020	0.031	A	2.1	Y	2		
		(LH)		0.154	0.326	0.372	0.022	0.043	0.061						
	B → Y	(HL)		0.141	0.227	0.387	0.015	0.020	0.031					B	2.1
		(LH)		0.154	0.327	0.373	0.022	0.043	0.061					D	2.0
	C → Y	(HL)		0.189	0.318	0.674	0.015	0.021	0.033					E	2.0
		(LH)		0.183	0.519	0.938	0.022	0.043	0.062					F	2.1
	D → Y	(HL)		0.190	0.320	0.673	0.015	0.021	0.033						
		(LH)		0.184	0.519	0.934	0.022	0.044	0.062						
	E → Y	(HL)		0.195	0.358	0.781	0.015	0.021	0.035						
		(LH)		0.190	0.567	1.097	0.022	0.043	0.062						
	F → Y	(HL)		0.196	0.359	0.782	0.015	0.021	0.035						
		(LH)		0.191	0.568	1.092	0.022	0.043	0.062						

Chapter 2 Function Block

Function	2-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L427	3										
x1	F427	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L427	A → Y	(HL)		0.173	0.338	0.803	0.031	0.042	0.065	A	1.0	Y	3
		(LH)		0.088	0.328	0.705	0.028	0.058	0.082				
	B → Y	(HL)		0.157	0.327	0.784	0.030	0.042	0.065	B	1.0	C	1.0
		(LH)		0.123	0.397	0.762	0.029	0.058	0.082				
	C → Y	(HL)		0.158	0.291	0.670	0.041	0.058	0.093	C	1.0	D	1.0
		(LH)		0.084	0.264	0.453	0.029	0.058	0.082				
	D → Y	(HL)		0.161	0.308	0.682	0.041	0.058	0.093	D	1.0	E	1.0
		(LH)		0.126	0.333	0.509	0.032	0.058	0.082				
	E → Y	(HL)		0.147	0.295	0.666	0.041	0.058	0.093	E	1.0		
		(LH)		0.140	0.362	0.536	0.032	0.058	0.082				
F427	A → Y	(HL)		0.157	0.304	0.682	0.015	0.021	0.034	A	2.0	Y	8
		(LH)		0.096	0.328	0.618	0.014	0.029	0.042				
	B → Y	(HL)		0.158	0.305	0.682	0.015	0.021	0.034	B	2.0	C	2.1
		(LH)		0.096	0.328	0.616	0.014	0.029	0.042				
	C → Y	(HL)		0.124	0.200	0.373	0.020	0.029	0.047	C	2.1	D	2.1
		(LH)		0.103	0.187	0.244	0.016	0.029	0.041				
	D → Y	(HL)		0.135	0.213	0.388	0.020	0.029	0.046	D	2.1	E	2.1
		(LH)		0.115	0.207	0.258	0.016	0.029	0.041				
	E → Y	(HL)		0.124	0.199	0.373	0.020	0.029	0.046	E	2.1		
		(LH)		0.102	0.185	0.242	0.016	0.029	0.041				

Chapter 2 Function Block

Function	1-2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L428	3										
x1	F428	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L428	A → Y	(HL)		0.094	0.146	0.184	0.020	0.024	0.032	A	1.0	Y	2
		(LH)		0.093	0.343	0.293	0.038	0.082	0.118				
	B → Y	(HL)		0.146	0.241	0.426	0.031	0.042	0.064	B	1.0		
		(LH)		0.113	0.375	0.596	0.050	0.087	0.123				
	C → Y	(HL)		0.133	0.233	0.408	0.031	0.042	0.064	C	1.0		
		(LH)		0.171	0.457	0.656	0.048	0.082	0.118				
	D → Y	(HL)		0.167	0.291	0.512	0.031	0.043	0.069	D	1.0		
		(LH)		0.145	0.455	0.851	0.048	0.082	0.119				
	E → Y	(HL)		0.150	0.279	0.491	0.031	0.043	0.069	E	1.0		
		(LH)		0.207	0.554	0.929	0.050	0.082	0.118				
F428	A → Y	(HL)		0.084	0.124	0.145	0.010	0.012	0.016	A	2.1	Y	7
		(LH)		0.107	0.197	0.147	0.022	0.043	0.060				
	B → Y	(HL)		0.123	0.196	0.314	0.015	0.021	0.033	B	2.0		
		(LH)		0.142	0.299	0.457	0.027	0.044	0.063				
	C → Y	(HL)		0.123	0.197	0.314	0.015	0.021	0.033	C	2.0		
		(LH)		0.141	0.300	0.455	0.027	0.044	0.063				
	D → Y	(HL)		0.137	0.219	0.348	0.016	0.022	0.037	D	2.0		
		(LH)		0.175	0.405	0.730	0.027	0.044	0.063				
	E → Y	(HL)		0.137	0.216	0.347	0.016	0.022	0.037	E	2.0		
		(LH)		0.175	0.404	0.730	0.027	0.044	0.063				

Chapter 2 Function Block

Function	2-2-2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L429	6										
x1	F429	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L429	A → Y	(HL)		0.243	0.405	0.712	0.020	0.024	0.033	A	1.0	Y	17
		(LH)		0.256	0.517	0.868	0.021	0.029	0.042				
	B → Y	(HL)		0.225	0.380	0.680	0.020	0.024	0.033	B	1.0		
		(LH)		0.286	0.567	0.908	0.021	0.029	0.042				
	C → Y	(HL)		0.301	0.493	0.994	0.020	0.024	0.033	C	1.0		
		(LH)		0.254	0.592	1.138	0.021	0.029	0.042				
	D → Y	(HL)		0.275	0.465	0.961	0.020	0.024	0.033	D	1.0		
		(LH)		0.284	0.644	1.180	0.021	0.029	0.042				
	E → Y	(HL)		0.261	0.432	0.732	0.020	0.024	0.033	E	1.0		
		(LH)		0.248	0.482	0.782	0.021	0.029	0.042				
	F → Y	(HL)		0.242	0.406	0.700	0.020	0.024	0.033	F	1.0		
		(LH)		0.276	0.524	0.817	0.021	0.029	0.042				
	G → Y	(HL)		0.321	0.520	1.023	0.020	0.025	0.033	G	1.0		
		(LH)		0.244	0.556	1.045	0.021	0.029	0.042				
	H → Y	(HL)		0.296	0.494	0.990	0.020	0.025	0.033	H	1.0		
		(LH)		0.271	0.602	1.080	0.021	0.029	0.042				
F429	A → Y	(HL)		0.256	0.427	0.744	0.010	0.012	0.017	A	1.0	Y	34
		(LH)		0.272	0.547	0.934	0.011	0.015	0.022				
	B → Y	(HL)		0.237	0.401	0.712	0.010	0.012	0.017	B	1.0		
		(LH)		0.304	0.598	0.974	0.011	0.015	0.022				
	C → Y	(HL)		0.316	0.515	1.031	0.010	0.012	0.017	C	1.0		
		(LH)		0.273	0.622	1.203	0.011	0.015	0.022				
	D → Y	(HL)		0.290	0.487	0.998	0.010	0.012	0.017	D	1.0		
		(LH)		0.304	0.674	1.245	0.011	0.015	0.022				
	E → Y	(HL)		0.272	0.450	0.760	0.010	0.012	0.017	E	1.0		
		(LH)		0.261	0.506	0.833	0.011	0.015	0.022				
	F → Y	(HL)		0.253	0.424	0.730	0.010	0.012	0.017	F	1.0		
		(LH)		0.290	0.549	0.869	0.011	0.015	0.022				
	G → Y	(HL)		0.332	0.538	1.055	0.010	0.013	0.017	G	1.0		
		(LH)		0.259	0.579	1.096	0.011	0.015	0.022				
	H → Y	(HL)		0.308	0.512	1.022	0.010	0.012	0.017	H	1.0		
		(LH)		0.288	0.627	1.132	0.011	0.015	0.022				

Chapter 2 Function Block

Function	1-4-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L440	3										
x1	F440	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L440	A → Y	(HL)		0.081	0.124	0.171	0.020	0.025	0.033	A	1.0	Y	1		
		(LH)		0.064	0.279	0.300	0.026	0.058	0.083						
	B → Y	(HL)		0.183	0.314	0.854	0.053	0.076	0.127					B	1.0
		(LH)		0.073	0.165	0.380	0.038	0.053	0.077						
	C → Y	(HL)		0.207	0.360	0.898	0.052	0.076	0.127					C	1.0
		(LH)		0.124	0.249	0.470	0.042	0.058	0.083						
	D → Y	(HL)		0.206	0.371	0.906	0.053	0.076	0.127	D	1.0				
		(LH)		0.146	0.279	0.502	0.042	0.058	0.082						
	E → Y	(HL)		0.213	0.383	0.919	0.052	0.076	0.127	E	1.0				
		(LH)		0.181	0.330	0.546	0.043	0.059	0.083						
F440	A → Y	(HL)		0.076	0.110	0.136	0.010	0.013	0.016	A	2.1	Y	4		
		(LH)		0.072	0.187	0.181	0.014	0.029	0.041						
	B → Y	(HL)		0.185	0.317	0.732	0.026	0.038	0.065					B	2.1
		(LH)		0.120	0.228	0.408	0.022	0.030	0.042						
	C → Y	(HL)		0.193	0.326	0.743	0.026	0.038	0.065					C	2.1
		(LH)		0.127	0.239	0.421	0.021	0.030	0.042						
	D → Y	(HL)		0.193	0.327	0.743	0.026	0.038	0.065	D	2.1				
		(LH)		0.127	0.239	0.421	0.021	0.030	0.042						
	E → Y	(HL)		0.185	0.317	0.732	0.026	0.038	0.065	E	2.1				
		(LH)		0.120	0.228	0.411	0.022	0.030	0.042						



Chapter 2 Function Block

Function	1-5-Input AND-NOR													
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L441	5												
x1	F441	7												
x2														
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H		-		-		-			
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"			Logic Diagram for "with inv. B type"								
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"			Logic Diagram for "with inv. E type"								
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"			Logic Diagram for "with inv. H type"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L441	A → Y	(HL)		0.080	0.121	0.171	0.020	0.025	0.032	A	1.0	Y	7		
		(LH)		0.069	0.191	0.241	0.029	0.058	0.082						
	B → Y	(HL)		0.270	0.445	0.905	0.031	0.042	0.065					B	1.0
		(LH)		0.201	0.356	0.718	0.038	0.053	0.077					C	1.0
	C → Y	(HL)		0.253	0.422	0.873	0.031	0.042	0.065					D	1.0
		(LH)		0.225	0.383	0.738	0.038	0.053	0.077					E	1.0
	D → Y	(HL)		0.339	0.557	1.182	0.031	0.042	0.064	F	1.0				
		(LH)		0.261	0.464	0.881	0.043	0.058	0.082						
	E → Y	(HL)		0.332	0.551	1.176	0.031	0.042	0.064						
		(LH)		0.283	0.491	0.900	0.043	0.058	0.082						
	F → Y	(HL)		0.326	0.554	1.176	0.031	0.042	0.064						
		(LH)		0.304	0.517	0.921	0.043	0.058	0.082						
F441	A → Y	(HL)		0.072	0.105	0.135	0.010	0.013	0.016	A	2.1	Y	16		
		(LH)		0.081	0.133	0.152	0.016	0.029	0.041						
	B → Y	(HL)		0.289	0.464	0.873	0.015	0.021	0.033					B	1.0
		(LH)		0.240	0.404	0.749	0.022	0.030	0.042					C	1.0
	C → Y	(HL)		0.272	0.439	0.842	0.015	0.021	0.033					D	1.0
		(LH)		0.264	0.433	0.769	0.022	0.030	0.042					E	1.0
	D → Y	(HL)		0.356	0.582	1.214	0.015	0.021	0.033	F	1.0				
		(LH)		0.251	0.440	0.851	0.022	0.030	0.042						
	E → Y	(HL)		0.350	0.579	1.208	0.015	0.021	0.033						
		(LH)		0.275	0.468	0.871	0.022	0.030	0.042						
	F → Y	(HL)		0.343	0.581	1.210	0.015	0.021	0.033						
		(LH)		0.298	0.497	0.891	0.022	0.030	0.042						

Chapter 2 Function Block

Function	4-4-4-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L444	8										
x1	F444	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L444	A	→	Y (HL)	0.316	0.512	1.131	0.020	0.025	0.033	A	1.0	Y	16
			(LH)	0.197	0.361	0.755	0.022	0.030	0.042	B	1.0		
	B	→	Y (HL)	0.318	0.522	1.143	0.020	0.025	0.033	C	1.0		
			(LH)	0.220	0.389	0.776	0.022	0.030	0.042	D	1.0		
	C	→	Y (HL)	0.327	0.549	1.171	0.020	0.025	0.033	E	1.0		
			(LH)	0.255	0.428	0.808	0.021	0.030	0.042	F	1.0		
	D	→	Y (HL)	0.320	0.544	1.163	0.020	0.025	0.033	G	1.0		
			(LH)	0.265	0.442	0.821	0.021	0.029	0.042	H	1.0		
	E	→	Y (HL)	0.364	0.689	1.296	0.020	0.025	0.033	I	1.0		
			(LH)	0.242	0.630	0.967	0.021	0.030	0.042	J	1.0		
	F	→	Y (HL)	0.366	0.701	1.310	0.020	0.025	0.033	K	1.0		
			(LH)	0.266	0.678	1.003	0.021	0.030	0.042	L	1.0		
	G	→	Y (HL)	0.379	0.729	1.335	0.020	0.025	0.033				
			(LH)	0.301	0.759	1.063	0.021	0.030	0.042				
	H	→	Y (HL)	0.371	0.725	1.325	0.020	0.025	0.033				
			(LH)	0.313	0.794	1.090	0.021	0.030	0.042				
I	→	Y (HL)	0.576	1.051	2.671	0.020	0.025	0.033					
		(LH)	0.278	0.818	1.508	0.021	0.030	0.042					
J	→	Y (HL)	0.579	1.066	2.684	0.020	0.025	0.033					
		(LH)	0.300	0.866	1.567	0.021	0.030	0.042					
K	→	Y (HL)	0.593	1.100	2.720	0.020	0.025	0.034					
		(LH)	0.331	0.956	1.625	0.021	0.030	0.042					
L	→	Y (HL)	0.584	1.091	2.710	0.020	0.025	0.034					
		(LH)	0.346	0.992	1.670	0.021	0.030	0.042					
F444	A	→	Y (HL)	0.326	0.532	1.170	0.010	0.012	0.017	A	1.0	Y	34
			(LH)	0.207	0.377	0.798	0.011	0.015	0.022	B	1.0		
	B	→	Y (HL)	0.331	0.543	1.183	0.010	0.012	0.017	C	1.0		
			(LH)	0.232	0.405	0.819	0.011	0.015	0.022	D	1.0		
	C	→	Y (HL)	0.340	0.571	1.210	0.010	0.012	0.017	E	1.0		
			(LH)	0.265	0.445	0.850	0.011	0.015	0.022	F	1.0		
	D	→	Y (HL)	0.332	0.566	1.201	0.010	0.012	0.017	G	1.0		
			(LH)	0.277	0.460	0.866	0.011	0.015	0.022	H	1.0		
	E	→	Y (HL)	0.377	0.712	1.338	0.010	0.013	0.017	I	1.0		
			(LH)	0.251	0.655	1.011	0.011	0.015	0.022	J	1.0		
	F	→	Y (HL)	0.380	0.725	1.352	0.010	0.013	0.017	K	1.0		
			(LH)	0.275	0.703	1.050	0.011	0.015	0.022	L	1.0		
	G	→	Y (HL)	0.390	0.752	1.373	0.010	0.013	0.017				
			(LH)	0.312	0.785	1.109	0.011	0.015	0.022				
	H	→	Y (HL)	0.383	0.748	1.366	0.010	0.013	0.017				
			(LH)	0.324	0.821	1.141	0.011	0.015	0.022				
I	→	Y (HL)	0.588	1.071	2.709	0.010	0.013	0.017					
		(LH)	0.289	0.839	1.568	0.011	0.015	0.022					
J	→	Y (HL)	0.589	1.083	2.728	0.010	0.013	0.017					
		(LH)	0.313	0.889	1.601	0.011	0.015	0.022					
K	→	Y (HL)	0.603	1.118	2.756	0.010	0.013	0.017					
		(LH)	0.343	0.980	1.681	0.011	0.015	0.022					
L	→	Y (HL)	0.593	1.109	2.748	0.010	0.013	0.017					
		(LH)	0.357	1.017	1.704	0.011	0.015	0.022					

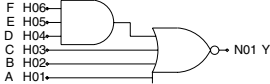
Chapter 2 Function Block

Function	1-1-1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L446	4										
x1	F446	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L446	A → Y	(HL)		0.184	0.307	0.560	0.020	0.024	0.033	A	1.0	Y	16
		(LH)		0.251	0.415	0.814	0.022	0.030	0.042				
	B → Y	(HL)		0.202	0.328	0.595	0.020	0.024	0.033	B	1.0		
		(LH)		0.239	0.410	0.873	0.022	0.030	0.042				
	C → Y	(HL)		0.207	0.356	0.598	0.020	0.024	0.033	C	1.0		
		(LH)		0.230	0.516	0.842	0.022	0.030	0.042				
	D → Y	(HL)		0.289	0.465	0.894	0.020	0.024	0.033	D	1.0		
		(LH)		0.238	0.424	0.891	0.022	0.030	0.042				
	E → Y	(HL)		0.277	0.451	0.872	0.020	0.024	0.033	E	1.0		
		(LH)		0.314	0.532	0.989	0.022	0.030	0.042				
F446	A → Y	(HL)		0.197	0.324	0.584	0.010	0.012	0.017	A	1.0	Y	34
		(LH)		0.272	0.445	0.877	0.011	0.015	0.022				
	B → Y	(HL)		0.214	0.345	0.621	0.010	0.012	0.017	B	1.0		
		(LH)		0.257	0.440	0.935	0.011	0.015	0.022				
	C → Y	(HL)		0.217	0.373	0.622	0.010	0.012	0.017	C	1.0		
		(LH)		0.242	0.536	0.889	0.011	0.015	0.022				
	D → Y	(HL)		0.300	0.481	0.925	0.010	0.012	0.017	D	1.0		
		(LH)		0.253	0.449	0.940	0.011	0.015	0.022				
	E → Y	(HL)		0.287	0.467	0.904	0.010	0.012	0.017	E	1.0		
		(LH)		0.327	0.552	1.039	0.011	0.015	0.022				

Chapter 2 Function Block

Function	1-1-1-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L447	5										
x1	F447	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
												
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L447	A → Y	(HL)		0.190	0.314	0.570	0.020	0.024	0.033	A	1.0	Y	16		
		(LH)		0.257	0.422	0.824	0.022	0.030	0.043						
	B → Y	(HL)		0.207	0.335	0.605	0.020	0.024	0.033					B	1.0
		(LH)		0.244	0.417	0.883	0.022	0.030	0.043					D	1.0
	C → Y	(HL)		0.208	0.365	0.608	0.020	0.024	0.033					E	1.0
		(LH)		0.225	0.564	0.890	0.022	0.030	0.043					F	1.0
	D → Y	(HL)		0.328	0.534	1.112	0.020	0.024	0.033						
		(LH)		0.235	0.426	0.896	0.022	0.030	0.043						
	E → Y	(HL)		0.332	0.548	1.125	0.020	0.024	0.033						
		(LH)		0.307	0.528	0.984	0.022	0.030	0.043						
	F → Y	(HL)		0.316	0.538	1.109	0.020	0.024	0.033						
		(LH)		0.335	0.568	1.028	0.022	0.030	0.043						
F447	A → Y	(HL)		0.196	0.324	0.584	0.010	0.012	0.017	A	1.0	Y	34		
		(LH)		0.268	0.441	0.873	0.011	0.015	0.022						
	B → Y	(HL)		0.212	0.344	0.621	0.010	0.012	0.017					B	1.0
		(LH)		0.255	0.436	0.930	0.011	0.015	0.022					C	1.0
	C → Y	(HL)		0.221	0.386	0.637	0.010	0.013	0.017					D	1.0
		(LH)		0.241	0.596	0.954	0.011	0.015	0.022					E	1.0
	D → Y	(HL)		0.347	0.564	1.165	0.010	0.012	0.017	F	1.0				
		(LH)		0.254	0.457	0.957	0.011	0.015	0.022						
	E → Y	(HL)		0.351	0.579	1.181	0.010	0.012	0.017						
		(LH)		0.330	0.564	1.049	0.011	0.015	0.022						
	F → Y	(HL)		0.335	0.569	1.165	0.010	0.012	0.017						
		(LH)		0.359	0.604	1.093	0.011	0.015	0.022						

Chapter 2 Function Block

Function	1-1-2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L448	5										
x1	F448	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L448	A → Y	(HL)		0.184	0.306	0.557	0.020	0.024	0.033	A	1.0	Y	17		
		(LH)		0.253	0.416	0.815	0.022	0.029	0.042						
	B → Y	(HL)		0.201	0.326	0.592	0.020	0.024	0.033					B	1.0
		(LH)		0.239	0.410	0.872	0.021	0.029	0.042					C	1.0
	C → Y	(HL)		0.262	0.435	0.738	0.020	0.025	0.033					D	1.0
		(LH)		0.250	0.488	0.791	0.021	0.029	0.042					E	1.0
	D → Y	(HL)		0.244	0.409	0.707	0.020	0.024	0.033	F	1.0				
		(LH)		0.279	0.532	0.825	0.021	0.029	0.042						
	E → Y	(HL)		0.306	0.525	1.029	0.020	0.024	0.033						
		(LH)		0.246	0.560	1.052	0.021	0.030	0.042						
	F → Y	(HL)		0.282	0.498	0.996	0.020	0.024	0.033						
		(LH)		0.274	0.607	1.092	0.021	0.029	0.042						
F448	A → Y	(HL)		0.195	0.324	0.583	0.010	0.012	0.017	A	1.0	Y	34		
		(LH)		0.267	0.440	0.872	0.011	0.015	0.022						
	B → Y	(HL)		0.212	0.344	0.620	0.010	0.012	0.017					B	1.0
		(LH)		0.255	0.436	0.930	0.011	0.015	0.022					C	1.0
	C → Y	(HL)		0.283	0.465	0.785	0.010	0.012	0.017					D	1.0
		(LH)		0.275	0.527	0.864	0.011	0.015	0.022					E	1.0
	D → Y	(HL)		0.263	0.438	0.755	0.010	0.012	0.017	F	1.0				
		(LH)		0.303	0.573	0.899	0.011	0.015	0.022						
	E → Y	(HL)		0.326	0.553	1.080	0.010	0.012	0.017						
		(LH)		0.272	0.602	1.128	0.011	0.015	0.022						
	F → Y	(HL)		0.301	0.527	1.046	0.010	0.013	0.017						
		(LH)		0.300	0.649	1.167	0.011	0.015	0.022						

Chapter 2 Function Block

Function	3-3-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F449	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-	-	-			
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F449	A → Y	(HL)		0.300	0.553	1.088	0.010	0.012	0.017	A	1.0	Y	34
		(LH)		0.243	0.662	1.155	0.011	0.015	0.022				
	B → Y	(HL)		0.309	0.570	1.100	0.010	0.012	0.017	B	1.0		
		(LH)		0.302	0.763	1.226	0.011	0.015	0.022				
	C → Y	(HL)		0.293	0.559	1.087	0.010	0.012	0.017	C	1.0		
		(LH)		0.321	0.808	1.265	0.011	0.015	0.022				
	D → Y	(HL)		0.369	0.716	1.719	0.010	0.013	0.017	D	1.0		
		(LH)		0.266	0.775	1.521	0.011	0.015	0.022				
	E → Y	(HL)		0.371	0.734	1.733	0.010	0.012	0.017	E	1.0		
		(LH)		0.317	0.876	1.599	0.011	0.015	0.022				
	F → Y	(HL)		0.353	0.722	1.716	0.010	0.012	0.017	F	1.0		
		(LH)		0.338	0.923	1.628	0.011	0.015	0.022				
	G → Y	(HL)		0.320	0.590	1.119	0.010	0.012	0.017	G	1.0		
		(LH)		0.234	0.608	1.018	0.011	0.015	0.022				
H → Y	(HL)		0.326	0.606	1.132	0.010	0.012	0.017	H	1.0			
	(LH)		0.290	0.694	1.082	0.011	0.015	0.022					
I → Y	(HL)		0.312	0.594	1.117	0.010	0.012	0.017	I	1.0			
	(LH)		0.308	0.734	1.115	0.011	0.015	0.022					
J → Y	(HL)		0.393	0.757	1.771	0.010	0.012	0.017	J	1.0			
	(LH)		0.250	0.717	1.380	0.011	0.015	0.022					
K → Y	(HL)		0.394	0.775	1.784	0.010	0.012	0.017	K	1.0			
	(LH)		0.299	0.809	1.443	0.011	0.015	0.022					
L → Y	(HL)		0.379	0.762	1.767	0.010	0.012	0.017	L	1.0			
	(LH)		0.317	0.849	1.487	0.011	0.015	0.022					

Chapter 2 Function Block

Function	3-3-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L460	6										
x1	F460	7										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L460	A → Y	(HL)		0.292	0.472	0.992	0.020	0.024	0.033	A	1.0	Y	16
		(LH)		0.201	0.362	0.754	0.022	0.030	0.042				
	B → Y	(HL)		0.286	0.468	0.985	0.020	0.024	0.033	B	1.0		
		(LH)		0.225	0.390	0.775	0.022	0.030	0.042				
	C → Y	(HL)		0.281	0.470	0.986	0.020	0.024	0.033	C	1.0		
		(LH)		0.262	0.431	0.810	0.022	0.030	0.042				
	D → Y	(HL)		0.339	0.634	1.300	0.020	0.024	0.033	D	1.0		
		(LH)		0.241	0.650	1.157	0.022	0.030	0.042				
	E → Y	(HL)		0.345	0.651	1.314	0.020	0.024	0.033	E	1.0		
		(LH)		0.295	0.739	1.227	0.022	0.030	0.042				
	F → Y	(HL)		0.329	0.639	1.299	0.020	0.024	0.033	F	1.0		
		(LH)		0.310	0.777	1.261	0.022	0.030	0.042				
	G → Y	(HL)		0.431	0.755	1.774	0.020	0.024	0.033	G	1.0		
		(LH)		0.245	0.721	1.409	0.022	0.030	0.042				
	H → Y	(HL)		0.433	0.772	1.786	0.020	0.024	0.033	H	1.0		
		(LH)		0.291	0.807	1.471	0.022	0.030	0.042				
	I → Y	(HL)		0.417	0.760	1.771	0.020	0.024	0.033	I	1.0		
		(LH)		0.309	0.847	1.514	0.022	0.030	0.042				
F460	A → Y	(HL)		0.312	0.502	1.042	0.010	0.012	0.017	A	1.0	Y	34
		(LH)		0.219	0.390	0.813	0.011	0.015	0.022				
	B → Y	(HL)		0.304	0.497	1.036	0.010	0.012	0.017	B	1.0		
		(LH)		0.243	0.417	0.833	0.011	0.015	0.022				
	C → Y	(HL)		0.302	0.501	1.038	0.010	0.012	0.017	C	1.0		
		(LH)		0.276	0.457	0.865	0.011	0.015	0.022				
	D → Y	(HL)		0.352	0.656	1.338	0.010	0.012	0.017	D	1.0		
		(LH)		0.253	0.678	1.214	0.011	0.015	0.022				
	E → Y	(HL)		0.353	0.672	1.352	0.010	0.012	0.017	E	1.0		
		(LH)		0.306	0.766	1.280	0.011	0.015	0.022				
	F → Y	(HL)		0.338	0.659	1.336	0.010	0.012	0.017	F	1.0		
		(LH)		0.323	0.806	1.315	0.011	0.015	0.022				
	G → Y	(HL)		0.440	0.770	1.806	0.010	0.012	0.017	G	1.0		
		(LH)		0.258	0.742	1.453	0.011	0.015	0.022				
	H → Y	(HL)		0.442	0.790	1.822	0.010	0.012	0.017	H	1.0		
		(LH)		0.305	0.832	1.530	0.011	0.015	0.022				
	I → Y	(HL)		0.427	0.778	1.805	0.010	0.012	0.017	I	1.0		
		(LH)		0.323	0.873	1.562	0.011	0.015	0.022				

Chapter 2 Function Block

Function	1-2-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F462	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F462	A → Y	(HL)		0.196	0.337	0.756	0.021	0.031	0.053	A	2.1	Y	1		
		(LH)		0.210	0.473	0.867	0.028	0.045	0.063						
	B → Y	(HL)		0.208	0.354	0.772	0.021	0.031	0.053					B	2.0
		(LH)		0.227	0.505	0.897	0.028	0.045	0.063					C	2.1
	C → Y	(HL)		0.196	0.336	0.755	0.021	0.031	0.053					D	2.1
		(LH)		0.209	0.471	0.864	0.028	0.045	0.063					E	2.0
	D → Y	(HL)		0.122	0.210	0.359	0.015	0.021	0.032					F	2.1
		(LH)		0.127	0.382	0.561	0.026	0.045	0.063						
	E → Y	(HL)		0.123	0.211	0.359	0.015	0.020	0.032						
		(LH)		0.127	0.382	0.559	0.026	0.045	0.063						
	F → Y	(HL)		0.089	0.140	0.184	0.010	0.012	0.016						
		(LH)		0.112	0.320	0.324	0.021	0.044	0.062						



Chapter 2 Function Block

Function	1-1-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L463	3										
x1	F463	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L463	A → Y	(HL)		0.091	0.136	0.180	0.020	0.025	0.033	A	1.0	Y	2
		(LH)		0.109	0.327	0.345	0.045	0.082	0.118				
	B → Y	(HL)		0.102	0.154	0.213	0.020	0.025	0.033	B	1.0		
		(LH)		0.101	0.362	0.504	0.045	0.082	0.118				
	C → Y	(HL)		0.189	0.311	0.693	0.041	0.060	0.099	C	1.0		
		(LH)		0.141	0.302	0.641	0.059	0.082	0.119				
	D → Y	(HL)		0.183	0.310	0.687	0.041	0.060	0.099	D	1.0		
		(LH)		0.176	0.354	0.702	0.059	0.082	0.119				
	E → Y	(HL)		0.180	0.315	0.687	0.041	0.060	0.099	E	1.0		
		(LH)		0.239	0.449	0.774	0.059	0.082	0.118				
F463	A → Y	(HL)		0.077	0.127	0.177	0.011	0.012	0.016	A	2.1	Y	6
		(LH)		0.114	0.289	0.330	0.027	0.045	0.064				
	B → Y	(HL)		0.090	0.145	0.204	0.010	0.012	0.017	B	2.0		
		(LH)		0.101	0.319	0.489	0.027	0.046	0.065				
	C → Y	(HL)		0.157	0.270	0.586	0.021	0.030	0.051	C	2.1		
		(LH)		0.189	0.365	0.691	0.034	0.046	0.065				
	D → Y	(HL)		0.174	0.289	0.600	0.021	0.030	0.051	D	2.1		
		(LH)		0.212	0.398	0.722	0.034	0.046	0.064				
	E → Y	(HL)		0.158	0.271	0.587	0.021	0.030	0.051	E	2.1		
		(LH)		0.191	0.368	0.693	0.034	0.046	0.064				

Chapter 2 Function Block

Function	1-1-4-Input AND-NOR													
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L464	5												
x1	F464	5												
x2														
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H		-		-		-			
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"			Logic Diagram for "with inv. B type"								
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"			Logic Diagram for "with inv. E type"								
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"			Logic Diagram for "with inv. H type"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L464	A → Y	(HL)		0.184	0.306	0.558	0.020	0.024	0.033	A	1.0	Y	17
		(LH)		0.253	0.416	0.815	0.022	0.029	0.042				
	B → Y	(HL)		0.201	0.326	0.593	0.020	0.024	0.033	B	1.0		
		(LH)		0.239	0.410	0.872	0.021	0.029	0.042				
	C → Y	(HL)		0.335	0.540	1.162	0.020	0.024	0.033	C	1.0		
		(LH)		0.190	0.344	0.692	0.021	0.029	0.042				
	D → Y	(HL)		0.337	0.552	1.176	0.020	0.024	0.033	D	1.0		
		(LH)		0.212	0.369	0.710	0.022	0.029	0.042				
	E → Y	(HL)		0.348	0.579	1.202	0.020	0.024	0.033	E	1.0		
		(LH)		0.241	0.401	0.737	0.022	0.030	0.042				
	F → Y	(HL)		0.338	0.573	1.194	0.020	0.024	0.033	F	1.0		
		(LH)		0.250	0.412	0.750	0.021	0.029	0.042				
F464	A → Y	(HL)		0.198	0.326	0.586	0.010	0.012	0.017	A	1.0	Y	34
		(LH)		0.273	0.447	0.880	0.011	0.015	0.022				
	B → Y	(HL)		0.214	0.346	0.623	0.010	0.012	0.017	B	1.0		
		(LH)		0.258	0.441	0.938	0.011	0.015	0.022				
	C → Y	(HL)		0.350	0.562	1.202	0.010	0.012	0.017	C	1.0		
		(LH)		0.204	0.366	0.740	0.011	0.015	0.022				
	D → Y	(HL)		0.352	0.573	1.216	0.010	0.012	0.017	D	1.0		
		(LH)		0.225	0.391	0.759	0.011	0.015	0.022				
	E → Y	(HL)		0.365	0.604	1.244	0.010	0.012	0.017	E	1.0		
		(LH)		0.256	0.424	0.789	0.011	0.015	0.022				
	F → Y	(HL)		0.355	0.597	1.236	0.010	0.012	0.017	F	1.0		
		(LH)		0.265	0.435	0.801	0.011	0.015	0.022				

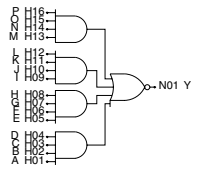
Chapter 2 Function Block

Function	1-1-1-1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F465	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F465	A → Y	(HL)		0.213	0.348	0.603	0.010	0.012	0.017	A	1.0	Y	34
		(LH)		0.368	0.589	1.057	0.011	0.015	0.022				
	B → Y	(HL)		0.228	0.368	0.642	0.010	0.012	0.017	B	1.0		
		(LH)		0.372	0.619	1.223	0.011	0.015	0.022				
	C → Y	(HL)		0.239	0.382	0.666	0.010	0.012	0.017	C	1.0		
		(LH)		0.376	0.674	1.406	0.011	0.015	0.022				
	D → Y	(HL)		0.217	0.374	0.623	0.010	0.012	0.017	D	1.0		
		(LH)		0.242	0.539	0.893	0.011	0.015	0.022				
	E → Y	(HL)		0.301	0.483	0.927	0.010	0.012	0.017	E	1.0		
		(LH)		0.254	0.451	0.946	0.011	0.015	0.022				
	F → Y	(HL)		0.288	0.470	0.906	0.010	0.012	0.017	F	1.0		
		(LH)		0.331	0.557	1.047	0.011	0.015	0.022				

Chapter 2 Function Block

Function	4-4-4-4-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F466	10										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-	-	-			
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
												
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F466	A	→	Y	(HL)	0.367	0.683	1.325	0.010	0.013	0.017	A	1.0	Y	34
				(LH)	0.275	0.744	1.184	0.011	0.015	0.022	B	1.0		
	B	→	Y	(HL)	0.369	0.696	1.338	0.010	0.013	0.017	C	1.0		
				(LH)	0.301	0.798	1.225	0.011	0.015	0.022	D	1.0		
	C	→	Y	(HL)	0.380	0.723	1.362	0.010	0.013	0.017	E	1.0		
				(LH)	0.340	0.893	1.295	0.011	0.015	0.022	F	1.0		
	D	→	Y	(HL)	0.374	0.719	1.354	0.010	0.013	0.017	G	1.0		
				(LH)	0.357	0.935	1.330	0.011	0.015	0.022	H	1.0		
	E	→	Y	(HL)	0.564	1.034	2.639	0.010	0.013	0.017	I	1.0		
				(LH)	0.320	0.930	1.745	0.011	0.015	0.022	J	1.0		
	F	→	Y	(HL)	0.567	1.048	2.656	0.010	0.013	0.017	K	1.0		
				(LH)	0.343	0.985	1.803	0.011	0.015	0.022	L	1.0		
	G	→	Y	(HL)	0.580	1.083	2.687	0.010	0.013	0.017	M	1.0		
				(LH)	0.381	1.087	1.867	0.011	0.015	0.022	N	1.0		
	H	→	Y	(HL)	0.572	1.074	2.678	0.010	0.013	0.017	O	1.0		
				(LH)	0.397	1.129	1.914	0.011	0.015	0.022	P	1.0		
	I	→	Y	(HL)	0.390	0.731	1.366	0.010	0.013	0.017				
				(LH)	0.261	0.671	1.033	0.011	0.015	0.022				
	J	→	Y	(HL)	0.392	0.744	1.380	0.010	0.013	0.017				
				(LH)	0.285	0.720	1.071	0.011	0.015	0.022				
	K	→	Y	(HL)	0.402	0.770	1.402	0.010	0.013	0.017				
				(LH)	0.321	0.802	1.132	0.011	0.015	0.022				
	L	→	Y	(HL)	0.394	0.767	1.397	0.010	0.013	0.017				
				(LH)	0.335	0.837	1.163	0.011	0.015	0.022				
M	→	Y	(HL)	0.597	1.082	2.732	0.010	0.013	0.017					
			(LH)	0.302	0.865	1.595	0.011	0.015	0.022					
N	→	Y	(HL)	0.597	1.096	2.746	0.010	0.013	0.017					
			(LH)	0.326	0.915	1.638	0.011	0.015	0.022					
O	→	Y	(HL)	0.611	1.130	2.782	0.010	0.013	0.017					
			(LH)	0.359	1.008	1.710	0.011	0.015	0.022					
P	→	Y	(HL)	0.602	1.120	2.771	0.010	0.013	0.017					
			(LH)	0.363	1.030	1.728	0.011	0.015	0.022					

[MEMO]

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## 2.6 OR-NAND

[MEMO]

Chapter 2 Function Block

Function	1-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L430	4										
x1	F430	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L430	A → Y	(HL)		0.104	0.139	0.225	0.030	0.040	0.061	A	1.0	Y	13		
		(LH)		0.048	0.080	0.140	0.022	0.030	0.042						
	B → Y	(HL)		0.192	0.315	0.574	0.030	0.040	0.061					B	1.0
		(LH)		0.267	0.437	0.838	0.022	0.030	0.042						
	C → Y	(HL)		0.206	0.335	0.608	0.030	0.040	0.061					C	1.0
		(LH)		0.253	0.433	0.896	0.022	0.030	0.042						
	D → Y	(HL)		0.202	0.332	0.588	0.030	0.040	0.061	D	1.0				
		(LH)		0.259	0.414	0.761	0.022	0.030	0.042						
	E → Y	(HL)		0.217	0.352	0.623	0.030	0.040	0.061	E	1.0				
		(LH)		0.244	0.408	0.817	0.022	0.030	0.042						
F430	A → Y	(HL)		0.092	0.128	0.215	0.015	0.020	0.031	A	2.1	Y	26		
		(LH)		0.057	0.090	0.145	0.011	0.015	0.021						
	B → Y	(HL)		0.217	0.360	0.671	0.015	0.020	0.031					B	1.0
		(LH)		0.292	0.478	0.931	0.011	0.015	0.021						
	C → Y	(HL)		0.234	0.381	0.707	0.015	0.020	0.031					C	1.0
		(LH)		0.278	0.474	0.990	0.011	0.015	0.021						
	D → Y	(HL)		0.230	0.381	0.686	0.015	0.020	0.031	D	1.0				
		(LH)		0.282	0.454	0.849	0.011	0.015	0.021						
	E → Y	(HL)		0.247	0.402	0.724	0.015	0.020	0.031	E	1.0				
		(LH)		0.268	0.449	0.905	0.011	0.015	0.021						

Chapter 2 Function Block

Function	1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L431	2										
x1	F431	3										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L431	A → Y	(HL)		0.097	0.204	0.388	0.024	0.042	0.065	A	1.0	Y	7
		(LH)		0.049	0.086	0.146	0.022	0.030	0.042				
	B → Y	(HL)		0.087	0.128	0.210	0.029	0.040	0.061	B	1.0		
		(LH)		0.121	0.173	0.225	0.042	0.058	0.082				
	C → Y	(HL)		0.115	0.181	0.360	0.031	0.042	0.064	C	1.0		
		(LH)		0.115	0.212	0.397	0.042	0.058	0.082				
F431	A → Y	(HL)		0.095	0.166	0.323	0.013	0.021	0.032	A	2.1	Y	14
		(LH)		0.045	0.082	0.164	0.011	0.015	0.022				
	B → Y	(HL)		0.098	0.152	0.303	0.015	0.021	0.032	B	2.0		
		(LH)		0.108	0.178	0.326	0.018	0.026	0.039				
	C → Y	(HL)		0.098	0.152	0.303	0.015	0.021	0.032	C	2.0		
		(LH)		0.108	0.178	0.326	0.018	0.026	0.039				



Chapter 2 Function Block

Function	1-1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L432	2										
x1	F432	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L432	A	→	Y	(HL)	0.131	0.258	0.605	0.035	0.058	0.093	A	1.0	Y	5
				(LH)	0.055	0.106	0.204	0.022	0.030	0.042	B	1.0		
	B	→	Y	(HL)	0.118	0.254	0.600	0.035	0.058	0.093	C	1.0		
				(LH)	0.071	0.124	0.219	0.021	0.030	0.042	D	1.0		
	C	→	Y	(HL)	0.123	0.213	0.465	0.041	0.058	0.093				
				(LH)	0.144	0.235	0.390	0.038	0.053	0.077				
F432	D	→	Y	(HL)	0.145	0.250	0.587	0.041	0.058	0.093				
				(LH)	0.125	0.235	0.449	0.038	0.053	0.077				
	A	→	Y	(HL)	0.123	0.229	0.523	0.018	0.029	0.047	A	2.1	Y	12
				(LH)	0.062	0.112	0.207	0.011	0.015	0.021	B	2.1		
	B	→	Y	(HL)	0.122	0.230	0.522	0.018	0.029	0.047	C	2.0		
				(LH)	0.062	0.112	0.207	0.011	0.015	0.021	D	2.0		
	C	→	Y	(HL)	0.136	0.231	0.523	0.020	0.029	0.047				
				(LH)	0.138	0.236	0.419	0.019	0.027	0.039				
	D	→	Y	(HL)	0.136	0.231	0.523	0.020	0.029	0.047				
				(LH)	0.138	0.236	0.419	0.019	0.027	0.039				

Chapter 2 Function Block

Function	1-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L433	2										
x1	F433	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L433	A → Y	(HL)		0.093	0.223	0.428	0.023	0.042	0.066	A	1.0	Y	4		
		(LH)		0.050	0.087	0.146	0.022	0.030	0.042						
	B → Y	(HL)		0.085	0.127	0.208	0.030	0.040	0.061					B	1.0
		(LH)		0.136	0.189	0.208	0.057	0.080	0.116						
	C → Y	(HL)		0.114	0.184	0.367	0.031	0.042	0.065	C	1.0				
		(LH)		0.161	0.295	0.558	0.058	0.081	0.117						
	D → Y	(HL)		0.119	0.195	0.386	0.031	0.042	0.066	D	1.0				
		(LH)		0.154	0.305	0.617	0.058	0.081	0.117						
F433	A → Y	(HL)		0.080	0.187	0.362	0.012	0.021	0.034	A	2.1	Y	7		
		(LH)		0.039	0.071	0.134	0.011	0.015	0.022						
	B → Y	(HL)		0.103	0.154	0.268	0.016	0.022	0.034					B	2.0
		(LH)		0.165	0.270	0.417	0.029	0.041	0.059						
	C → Y	(HL)		0.116	0.181	0.354	0.015	0.021	0.033	C	2.1				
		(LH)		0.179	0.317	0.572	0.029	0.041	0.059						
	D → Y	(HL)		0.103	0.154	0.268	0.016	0.022	0.034	D	2.1				
		(LH)		0.166	0.272	0.418	0.029	0.041	0.059						

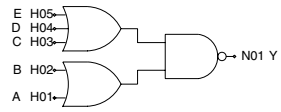
Chapter 2 Function Block

Function	2-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L434	2										
x1	F434	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L434	A → Y	(HL)		0.127	0.241	0.479	0.025	0.041	0.063	A	1.0	Y	5		
		(LH)		0.113	0.193	0.351	0.038	0.053	0.078						
	B → Y	(HL)		0.141	0.266	0.558	0.025	0.041	0.063					B	1.0
		(LH)		0.095	0.191	0.408	0.038	0.053	0.078					C	1.0
	C → Y	(HL)		0.124	0.231	0.454	0.023	0.041	0.063					D	1.0
		(LH)		0.151	0.265	0.419	0.037	0.053	0.077						
	D → Y	(HL)		0.135	0.259	0.535	0.023	0.041	0.063						
		(LH)		0.133	0.264	0.479	0.037	0.053	0.077						
F434	A → Y	(HL)		0.114	0.210	0.443	0.013	0.021	0.032	A	2.0	Y	11		
		(LH)		0.084	0.154	0.346	0.019	0.027	0.039						
	B → Y	(HL)		0.115	0.210	0.444	0.013	0.021	0.032					B	2.0
		(LH)		0.084	0.154	0.346	0.019	0.027	0.039					C	2.0
	C → Y	(HL)		0.124	0.217	0.434	0.012	0.021	0.032					D	2.0
		(LH)		0.142	0.263	0.446	0.019	0.027	0.039						
	D → Y	(HL)		0.124	0.217	0.434	0.012	0.021	0.032						
		(LH)		0.142	0.263	0.446	0.019	0.027	0.039						

Chapter 2 Function Block

Function	2-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F435	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
												
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F435	A → Y	(HL)		0.104	0.214	0.430	0.012	0.021	0.033	A	2.1	Y	4
		(LH)		0.081	0.141	0.299	0.019	0.027	0.039				
	B → Y	(HL)		0.104	0.214	0.429	0.012	0.021	0.033	B	2.1		
		(LH)		0.081	0.141	0.300	0.019	0.027	0.039				
	C → Y	(HL)		0.130	0.226	0.425	0.012	0.021	0.033	C	2.1		
		(LH)		0.219	0.404	0.623	0.029	0.041	0.059				
	D → Y	(HL)		0.138	0.254	0.512	0.012	0.021	0.033	D	2.1		
		(LH)		0.234	0.451	0.780	0.029	0.041	0.059				
	E → Y	(HL)		0.130	0.226	0.425	0.012	0.021	0.033	E	2.1		
		(LH)		0.219	0.405	0.625	0.029	0.041	0.059				

Chapter 2 Function Block

Function	3-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L436	3										
x1	F436	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L436	A → Y	(HL)		0.099	0.241	0.446	0.023	0.042	0.066	A	1.0	Y	1
		(LH)		0.106	0.167	0.192	0.057	0.082	0.119				
	B → Y	(HL)		0.124	0.304	0.670	0.023	0.042	0.066	B	1.0		
		(LH)		0.130	0.270	0.533	0.058	0.082	0.119				
	C → Y	(HL)		0.128	0.325	0.721	0.023	0.043	0.067	C	1.0		
		(LH)		0.123	0.280	0.595	0.058	0.082	0.119				
	D → Y	(HL)		0.126	0.253	0.442	0.021	0.042	0.066	D	1.0		
		(LH)		0.209	0.394	0.402	0.058	0.081	0.119				
	E → Y	(HL)		0.147	0.325	0.668	0.021	0.042	0.066	E	1.0		
		(LH)		0.236	0.504	0.762	0.058	0.082	0.119				
	F → Y	(HL)		0.152	0.345	0.724	0.021	0.042	0.066	F	1.0		
		(LH)		0.228	0.516	0.826	0.058	0.082	0.119				
F436	A → Y	(HL)		0.103	0.253	0.518	0.012	0.022	0.034	A	2.1	Y	3
		(LH)		0.116	0.209	0.381	0.029	0.041	0.061				
	B → Y	(HL)		0.117	0.276	0.606	0.012	0.022	0.034	B	2.1		
		(LH)		0.128	0.251	0.530	0.029	0.042	0.060				
	C → Y	(HL)		0.105	0.253	0.518	0.012	0.022	0.034	C	2.1		
		(LH)		0.115	0.208	0.380	0.029	0.041	0.060				
	D → Y	(HL)		0.142	0.283	0.529	0.011	0.021	0.034	D	2.1		
		(LH)		0.248	0.484	0.645	0.029	0.041	0.060				
	E → Y	(HL)		0.150	0.311	0.618	0.011	0.021	0.034	E	2.1		
		(LH)		0.264	0.530	0.801	0.029	0.041	0.060				
	F → Y	(HL)		0.142	0.283	0.530	0.011	0.021	0.034	F	2.1		
		(LH)		0.249	0.484	0.647	0.029	0.041	0.060				

Chapter 2 Function Block

Function	1-2-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F437	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F437	A	→	Y	(HL)	0.138	0.296	0.721	0.016	0.030	0.048	A	2.1	Y	8
				(LH)	0.066	0.123	0.243	0.011	0.015	0.022	B	2.0		
	B	→	Y	(HL)	0.148	0.306	0.735	0.018	0.030	0.048	C	2.0		
				(LH)	0.129	0.234	0.467	0.019	0.027	0.039	D	2.0		
	C	→	Y	(HL)	0.148	0.306	0.735	0.018	0.030	0.048	E	2.0		
				(LH)	0.129	0.234	0.467	0.019	0.027	0.039				
	D	→	Y	(HL)	0.171	0.333	0.750	0.018	0.030	0.048				
				(LH)	0.178	0.326	0.556	0.019	0.027	0.039				
	E	→	Y	(HL)	0.171	0.333	0.750	0.018	0.030	0.048				
				(LH)	0.178	0.326	0.556	0.019	0.027	0.039				

Chapter 2 Function Block

Function	2-2-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F438	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"			Logic Diagram for "with inv. B type"						
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"			Logic Diagram for "with inv. E type"						
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"			Logic Diagram for "with inv. H type"						

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
F438	A → Y	(HL)		0.169	0.379	0.932	0.015	0.030	0.047	A	2.1	Y	4		
		(LH)		0.127	0.240	0.511	0.019	0.027	0.039						
	B → Y	(HL)		0.169	0.379	0.932	0.015	0.030	0.047					B	2.1
		(LH)		0.127	0.240	0.511	0.019	0.027	0.039						
	C → Y	(HL)		0.174	0.398	0.934	0.014	0.029	0.047					C	2.0
		(LH)		0.165	0.317	0.577	0.019	0.027	0.039						
	D → Y	(HL)		0.175	0.399	0.937	0.014	0.029	0.047	D	2.0				
		(LH)		0.165	0.316	0.577	0.019	0.027	0.039						
	E → Y	(HL)		0.185	0.421	0.956	0.014	0.030	0.047	E	2.0				
		(LH)		0.215	0.422	0.678	0.019	0.027	0.039						
	F → Y	(HL)		0.185	0.421	0.956	0.014	0.030	0.047	F	2.0				
		(LH)		0.215	0.422	0.678	0.019	0.027	0.039						

Chapter 2 Function Block

1-5-Input OR-NAND												
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L439	5										
x1	F439	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L439	A → Y	(HL)		0.104	0.139	0.225	0.030	0.040	0.061	A	1.0	Y	13		
		(LH)		0.048	0.080	0.139	0.022	0.030	0.042						
	B → Y	(HL)		0.189	0.315	0.575	0.030	0.041	0.061					B	1.0
		(LH)		0.266	0.435	0.833	0.022	0.030	0.042					C	1.0
	C → Y	(HL)		0.206	0.335	0.609	0.030	0.041	0.061					D	1.0
		(LH)		0.252	0.430	0.892	0.022	0.030	0.042					E	1.0
	D → Y	(HL)		0.221	0.359	0.610	0.030	0.040	0.061	F	1.0				
		(LH)		0.345	0.536	0.898	0.022	0.030	0.042						
	E → Y	(HL)		0.237	0.379	0.649	0.030	0.040	0.061						
		(LH)		0.348	0.565	1.058	0.022	0.030	0.042						
	F → Y	(HL)		0.246	0.393	0.666	0.030	0.040	0.061						
		(LH)		0.350	0.619	1.240	0.022	0.030	0.042						
F439	A → Y	(HL)		0.094	0.129	0.215	0.015	0.020	0.031	A	2.1	Y	26		
		(LH)		0.057	0.090	0.145	0.011	0.015	0.021						
	B → Y	(HL)		0.213	0.358	0.667	0.015	0.020	0.031					B	1.0
		(LH)		0.285	0.470	0.918	0.011	0.015	0.021					C	1.0
	C → Y	(HL)		0.230	0.378	0.703	0.015	0.020	0.031					D	1.0
		(LH)		0.273	0.466	0.977	0.011	0.015	0.021					E	1.0
	D → Y	(HL)		0.247	0.404	0.702	0.015	0.020	0.031	F	1.0				
		(LH)		0.374	0.582	0.994	0.011	0.015	0.021						
	E → Y	(HL)		0.262	0.426	0.743	0.015	0.020	0.031						
		(LH)		0.377	0.612	1.153	0.011	0.015	0.021						
	F → Y	(HL)		0.273	0.439	0.767	0.015	0.020	0.031						
		(LH)		0.380	0.665	1.335	0.011	0.015	0.021						



Chapter 2 Function Block

Function	2-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L450	5										
x1	F450	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L450	A → Y	(HL)		0.115	0.184	0.366	0.031	0.042	0.065	A	1.0	Y	7		
		(LH)		0.112	0.211	0.393	0.042	0.058	0.082						
	B → Y	(HL)		0.085	0.129	0.214	0.030	0.040	0.062					B	1.0
		(LH)		0.119	0.171	0.222	0.042	0.058	0.082						
	C → Y	(HL)		0.190	0.392	0.800	0.024	0.042	0.065					C	1.0
		(LH)		0.256	0.426	0.826	0.022	0.030	0.043						
	D → Y	(HL)		0.206	0.412	0.835	0.024	0.042	0.065	D	1.0				
		(LH)		0.243	0.421	0.885	0.022	0.030	0.043						
	E → Y	(HL)		0.210	0.420	0.822	0.024	0.042	0.064	E	1.0				
		(LH)		0.255	0.413	0.764	0.022	0.030	0.043						
	F → Y	(HL)		0.227	0.441	0.859	0.024	0.042	0.065	F	1.0				
		(LH)		0.240	0.408	0.822	0.022	0.030	0.043						
F450	A → Y	(HL)		0.098	0.158	0.317	0.015	0.021	0.032	A	2.0	Y	14		
		(LH)		0.107	0.178	0.323	0.019	0.027	0.039						
	B → Y	(HL)		0.098	0.158	0.317	0.015	0.021	0.032					B	2.0
		(LH)		0.107	0.178	0.323	0.019	0.027	0.039						
	C → Y	(HL)		0.214	0.392	0.801	0.013	0.021	0.032					C	1.0
		(LH)		0.282	0.468	0.942	0.011	0.016	0.022						
	D → Y	(HL)		0.230	0.412	0.838	0.013	0.021	0.032	D	1.0				
		(LH)		0.267	0.464	1.000	0.011	0.016	0.022						
	E → Y	(HL)		0.228	0.414	0.817	0.013	0.021	0.032	E	1.0				
		(LH)		0.271	0.443	0.858	0.011	0.016	0.022						
	F → Y	(HL)		0.244	0.435	0.855	0.013	0.021	0.032	F	1.0				
		(LH)		0.257	0.437	0.915	0.011	0.016	0.022						

Chapter 2 Function Block

Function	4-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L451	7										
x1	F451	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L451	A → Y	(HL)		0.188	0.320	0.614	0.030	0.041	0.062	A	1.0	Y	13
		(LH)		0.250	0.412	0.807	0.022	0.030	0.042				
	B → Y	(HL)		0.205	0.341	0.649	0.030	0.041	0.062	B	1.0		
		(LH)		0.237	0.408	0.866	0.022	0.030	0.042				
	C → Y	(HL)		0.208	0.348	0.636	0.030	0.040	0.062	C	1.0		
		(LH)		0.250	0.400	0.746	0.022	0.030	0.042				
	D → Y	(HL)		0.226	0.368	0.673	0.030	0.040	0.062	D	1.0		
		(LH)		0.234	0.395	0.803	0.022	0.030	0.042				
	E → Y	(HL)		0.192	0.319	0.580	0.030	0.041	0.062	E	1.0		
		(LH)		0.266	0.436	0.837	0.022	0.030	0.042				
	F → Y	(HL)		0.206	0.339	0.614	0.030	0.041	0.062	F	1.0		
		(LH)		0.252	0.432	0.895	0.022	0.030	0.042				
	G → Y	(HL)		0.205	0.336	0.596	0.030	0.041	0.062	G	1.0		
		(LH)		0.261	0.418	0.766	0.022	0.030	0.042				
	H → Y	(HL)		0.221	0.358	0.631	0.030	0.040	0.062	H	1.0		
		(LH)		0.245	0.412	0.822	0.022	0.030	0.042				
F451	A → Y	(HL)		0.218	0.367	0.679	0.015	0.020	0.031	A	1.0	Y	27
		(LH)		0.293	0.481	0.935	0.011	0.015	0.021				
	B → Y	(HL)		0.235	0.386	0.715	0.015	0.020	0.031	B	1.0		
		(LH)		0.279	0.476	0.991	0.011	0.015	0.021				
	C → Y	(HL)		0.235	0.388	0.698	0.015	0.020	0.031	C	1.0		
		(LH)		0.289	0.462	0.859	0.011	0.015	0.021				
	D → Y	(HL)		0.253	0.411	0.737	0.015	0.020	0.031	D	1.0		
		(LH)		0.272	0.456	0.917	0.011	0.015	0.021				
	E → Y	(HL)		0.220	0.366	0.680	0.015	0.020	0.031	E	1.0		
		(LH)		0.295	0.482	0.936	0.011	0.015	0.021				
	F → Y	(HL)		0.237	0.387	0.716	0.015	0.020	0.031	F	1.0		
		(LH)		0.280	0.478	0.995	0.011	0.015	0.021				
	G → Y	(HL)		0.234	0.387	0.696	0.015	0.020	0.031	G	1.0		
		(LH)		0.285	0.457	0.855	0.011	0.015	0.021				
	H → Y	(HL)		0.250	0.408	0.733	0.015	0.020	0.031	H	1.0		
		(LH)		0.270	0.452	0.911	0.011	0.015	0.021				

Chapter 2 Function Block

Function	1-1-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L452	4										
x1	F452	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L452	A → Y	(HL)		0.239	0.390	0.712	0.020	0.025	0.034	A	1.0	Y	17		
		(LH)		0.179	0.293	0.539	0.022	0.030	0.042						
	B → Y	(HL)		0.253	0.544	1.109	0.020	0.025	0.034					B	1.0
		(LH)		0.173	0.324	0.620	0.022	0.030	0.042						
	C → Y	(HL)		0.259	0.446	0.874	0.020	0.025	0.034					C	1.0
		(LH)		0.337	0.530	0.854	0.021	0.029	0.042						
	D → Y	(HL)		0.294	0.502	1.039	0.020	0.025	0.034	D	1.0				
		(LH)		0.356	0.627	1.209	0.022	0.029	0.042						
	E → Y	(HL)		0.301	0.514	1.067	0.020	0.025	0.034	E	1.0				
		(LH)		0.349	0.637	1.270	0.022	0.029	0.042						
F452	A → Y	(HL)		0.268	0.431	0.780	0.010	0.013	0.018	A	1.0	Y	34		
		(LH)		0.187	0.300	0.552	0.011	0.015	0.021						
	B → Y	(HL)		0.277	0.581	1.172	0.010	0.013	0.018					B	1.0
		(LH)		0.179	0.336	0.643	0.011	0.015	0.021						
	C → Y	(HL)		0.284	0.482	0.937	0.010	0.013	0.018					C	1.0
		(LH)		0.353	0.551	0.887	0.011	0.015	0.021						
	D → Y	(HL)		0.316	0.540	1.102	0.010	0.013	0.018	D	1.0				
		(LH)		0.372	0.647	1.243	0.011	0.015	0.021						
	E → Y	(HL)		0.323	0.550	1.132	0.010	0.013	0.018	E	1.0				
		(LH)		0.365	0.658	1.305	0.011	0.015	0.021						

Chapter 2 Function Block

Function	1-1-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L453	5										
x1	F453	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L453	A → Y	(HL)		0.168	0.272	0.659	0.041	0.058	0.093	A	1.0	Y	5		
		(LH)		0.069	0.129	0.267	0.022	0.030	0.042						
	B → Y	(HL)		0.159	0.273	0.653	0.041	0.058	0.093					B	1.0
		(LH)		0.084	0.146	0.279	0.021	0.029	0.042					C	1.0
	C → Y	(HL)		0.277	0.488	1.039	0.041	0.058	0.093					D	1.0
		(LH)		0.312	0.520	1.003	0.022	0.030	0.042					E	1.0
	D → Y	(HL)		0.291	0.508	1.072	0.041	0.058	0.093	F	1.0				
		(LH)		0.298	0.514	1.062	0.022	0.030	0.042						
	E → Y	(HL)		0.284	0.499	1.049	0.041	0.058	0.093						
		(LH)		0.302	0.494	0.924	0.022	0.030	0.042						
	F → Y	(HL)		0.300	0.522	1.083	0.041	0.058	0.093						
		(LH)		0.288	0.488	0.981	0.022	0.030	0.042						
F453	A → Y	(HL)		0.111	0.165	0.346	0.020	0.029	0.047	A	2.1	Y	15		
		(LH)		0.061	0.104	0.184	0.011	0.015	0.021						
	B → Y	(HL)		0.121	0.177	0.359	0.020	0.029	0.047					B	2.1
		(LH)		0.071	0.118	0.193	0.011	0.015	0.021					C	1.0
	C → Y	(HL)		0.235	0.400	0.808	0.021	0.029	0.047					D	1.0
		(LH)		0.302	0.496	0.973	0.011	0.016	0.022					E	1.0
	D → Y	(HL)		0.251	0.421	0.843	0.021	0.029	0.047	F	1.0				
		(LH)		0.287	0.492	1.031	0.011	0.016	0.022						
	E → Y	(HL)		0.249	0.420	0.823	0.021	0.029	0.047						
		(LH)		0.292	0.473	0.892	0.011	0.015	0.022						
	F → Y	(HL)		0.266	0.442	0.860	0.021	0.029	0.047						
		(LH)		0.278	0.467	0.949	0.011	0.015	0.022						

Chapter 2 Function Block

Function	4-4-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F457	10										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F457	A	→	Y	(HL)	0.358	0.582	0.981	0.011	0.014	0.020	A	1.0	Y	31
				(LH)	0.333	0.559	1.100	0.011	0.015	0.022	B	1.0		
	B	→	Y	(HL)	0.373	0.602	1.019	0.011	0.014	0.020	C	1.0		
				(LH)	0.318	0.554	1.157	0.011	0.015	0.022	D	1.0		
	C	→	Y	(HL)	0.381	0.617	1.008	0.011	0.014	0.020	E	1.0		
				(LH)	0.317	0.525	0.998	0.011	0.015	0.022	F	1.0		
	D	→	Y	(HL)	0.398	0.639	1.047	0.011	0.014	0.020	G	1.0		
				(LH)	0.304	0.518	1.055	0.011	0.015	0.022	H	1.0		
	E	→	Y	(HL)	0.401	0.912	1.595	0.011	0.015	0.022	I	1.0		
				(LH)	0.367	0.649	1.341	0.011	0.015	0.022	J	1.0		
	F	→	Y	(HL)	0.415	0.927	1.622	0.011	0.015	0.022	K	1.0		
				(LH)	0.350	0.645	1.399	0.011	0.015	0.022	L	1.0		
	G	→	Y	(HL)	0.431	0.969	1.642	0.011	0.016	0.022				
				(LH)	0.353	0.617	1.235	0.011	0.015	0.022				
	H	→	Y	(HL)	0.443	0.986	1.671	0.011	0.016	0.022				
				(LH)	0.336	0.611	1.293	0.011	0.015	0.022				
I	→	Y	(HL)	0.445	1.022	1.885	0.011	0.015	0.022					
			(LH)	0.391	0.737	1.581	0.011	0.016	0.023					
J	→	Y	(HL)	0.456	1.036	1.914	0.011	0.015	0.022					
			(LH)	0.375	0.732	1.637	0.011	0.016	0.023					
K	→	Y	(HL)	0.466	1.070	1.922	0.011	0.016	0.022					
			(LH)	0.364	0.684	1.443	0.011	0.016	0.023					
L	→	Y	(HL)	0.478	1.087	1.954	0.011	0.016	0.022					
			(LH)	0.350	0.680	1.498	0.011	0.016	0.023					

Chapter 2 Function Block

Function	1-1-1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L458	3										
x1	F458	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L458	A → Y	(HL)		0.137	0.348	0.950	0.046	0.076	0.126	A	1.0	Y	1		
		(LH)		0.053	0.104	0.205	0.022	0.030	0.042						
	B → Y	(HL)		0.135	0.362	0.965	0.046	0.076	0.126					B	1.0
		(LH)		0.068	0.122	0.219	0.022	0.030	0.042						
	C → Y	(HL)		0.141	0.396	1.001	0.046	0.076	0.126					C	1.0
		(LH)		0.089	0.155	0.246	0.022	0.030	0.042						
	D → Y	(HL)		0.163	0.280	0.600	0.051	0.075	0.123	D	1.0				
		(LH)		0.185	0.290	0.421	0.042	0.058	0.083						
	E → Y	(HL)		0.219	0.404	1.000	0.053	0.076	0.126	E	1.0				
		(LH)		0.182	0.338	0.600	0.043	0.059	0.082						
F458	A → Y	(HL)		0.160	0.297	0.780	0.025	0.039	0.064	A	2.1	Y	5		
		(LH)		0.057	0.114	0.234	0.011	0.015	0.021						
	B → Y	(HL)		0.168	0.329	0.815	0.025	0.039	0.064					B	2.0
		(LH)		0.080	0.144	0.257	0.011	0.015	0.021						
	C → Y	(HL)		0.160	0.341	0.829	0.025	0.039	0.064					C	2.1
		(LH)		0.093	0.159	0.275	0.011	0.015	0.021						
	D → Y	(HL)		0.199	0.356	0.849	0.027	0.039	0.064	D	2.1				
		(LH)		0.166	0.292	0.521	0.019	0.027	0.039						
	E → Y	(HL)		0.197	0.356	0.849	0.027	0.039	0.064	E	2.0				
		(LH)		0.166	0.292	0.521	0.019	0.027	0.039						

Chapter 2 Function Block

Function	1-1-1-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L459	5										
x1	F459	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L459	A → Y	(HL)		0.278	0.448	0.835	0.020	0.025	0.034	A	1.0	Y	17		
		(LH)		0.163	0.279	0.527	0.022	0.030	0.042						
	B → Y	(HL)		0.263	0.424	0.804	0.020	0.025	0.034					B	1.0
		(LH)		0.188	0.306	0.548	0.022	0.030	0.042					C	1.0
	C → Y	(HL)		0.259	0.551	1.119	0.020	0.025	0.035					D	1.0
		(LH)		0.175	0.326	0.623	0.021	0.030	0.042					E	1.0
	D → Y	(HL)		0.264	0.453	0.886	0.020	0.025	0.034	F	1.0				
		(LH)		0.341	0.536	0.863	0.021	0.029	0.042						
	E → Y	(HL)		0.298	0.511	1.051	0.020	0.025	0.035						
		(LH)		0.361	0.633	1.218	0.021	0.029	0.042						
	F → Y	(HL)		0.305	0.521	1.078	0.020	0.025	0.035						
		(LH)		0.353	0.643	1.280	0.021	0.029	0.042						
F459	A → Y	(HL)		0.304	0.487	0.902	0.010	0.013	0.018	A	1.0	Y	34		
		(LH)		0.171	0.288	0.542	0.011	0.015	0.021						
	B → Y	(HL)		0.287	0.463	0.870	0.010	0.013	0.018					B	1.0
		(LH)		0.193	0.316	0.562	0.011	0.015	0.021					C	1.0
	C → Y	(HL)		0.279	0.583	1.179	0.010	0.013	0.018					D	1.0
		(LH)		0.179	0.336	0.642	0.011	0.015	0.021					E	1.0
	D → Y	(HL)		0.286	0.486	0.946	0.010	0.013	0.018	F	1.0				
		(LH)		0.356	0.554	0.893	0.011	0.015	0.021						
	E → Y	(HL)		0.319	0.543	1.109	0.010	0.013	0.018						
		(LH)		0.377	0.655	1.250	0.011	0.015	0.021						
	F → Y	(HL)		0.327	0.554	1.136	0.010	0.013	0.018						
		(LH)		0.369	0.663	1.307	0.011	0.015	0.021						

Chapter 2 Function Block

Function	1-1-1-1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F490	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F490	A → Y	(HL)		0.372	0.606	1.252	0.010	0.013	0.018	A	1.0	Y	35
		(LH)		0.180	0.320	0.638	0.011	0.015	0.021				
	B → Y	(HL)		0.365	0.603	1.247	0.010	0.013	0.018	B	1.0		
		(LH)		0.203	0.346	0.656	0.011	0.015	0.021				
	C → Y	(HL)		0.361	0.605	1.246	0.010	0.013	0.018	C	1.0		
		(LH)		0.233	0.382	0.687	0.011	0.015	0.021				
	D → Y	(HL)		0.291	0.575	1.149	0.010	0.013	0.018	D	1.0		
		(LH)		0.186	0.340	0.649	0.011	0.015	0.021				
	E → Y	(HL)		0.296	0.495	0.959	0.010	0.013	0.018	E	1.0		
		(LH)		0.321	0.497	0.827	0.011	0.015	0.021				
	F → Y	(HL)		0.332	0.553	1.120	0.010	0.013	0.018	F	1.0		
		(LH)		0.314	0.535	1.006	0.011	0.015	0.021				



Chapter 2 Function Block

Function	1-2-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L491	5										
x1	F491	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1										
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout				
L491	A → Y	(HL)		0.244	0.397	0.722	0.020	0.025	0.034	A	1.0	Y	16				
		(LH)		0.183	0.298	0.545	0.022	0.030	0.042								
	B → Y	(HL)		0.271	0.588	1.257	0.020	0.025	0.034					B	1.0		
		(LH)		0.251	0.464	0.948	0.022	0.030	0.042								
	C → Y	(HL)		0.288	0.624	1.365	0.020	0.025	0.034							C	1.0
		(LH)		0.233	0.461	1.007	0.022	0.030	0.042								
	D → Y	(HL)		0.296	0.571	1.150	0.020	0.025	0.034	D	1.0						
		(LH)		0.432	0.765	1.268	0.021	0.029	0.042								
	E → Y	(HL)		0.308	0.605	1.244	0.020	0.025	0.034			E	1.0				
		(LH)		0.437	0.805	1.440	0.021	0.029	0.042								
	F → Y	(HL)		0.320	0.653	1.376	0.020	0.025	0.034					F	1.0		
		(LH)		0.443	0.868	1.621	0.021	0.029	0.042								
F491	A → Y	(HL)		0.265	0.430	0.780	0.010	0.013	0.018	A	1.0					Y	34
		(LH)		0.186	0.300	0.550	0.011	0.015	0.021								
	B → Y	(HL)		0.312	0.651	1.346	0.010	0.013	0.018			B	1.0				
		(LH)		0.290	0.526	1.025	0.011	0.015	0.021								
	C → Y	(HL)		0.327	0.685	1.450	0.010	0.013	0.018					C	1.0		
		(LH)		0.272	0.524	1.085	0.011	0.015	0.021								
	D → Y	(HL)		0.317	0.618	1.222	0.010	0.013	0.018	D	1.0						
		(LH)		0.457	0.802	1.332	0.011	0.015	0.021								
	E → Y	(HL)		0.330	0.651	1.314	0.010	0.013	0.018			E	1.0				
		(LH)		0.461	0.841	1.502	0.011	0.015	0.021								
	F → Y	(HL)		0.343	0.700	1.452	0.010	0.013	0.018					F	1.0		
		(LH)		0.470	0.905	1.688	0.011	0.015	0.021								

Chapter 2 Function Block

Function	3-3-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L493	6										
x1	F493	7										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L493	A → Y	(HL)		0.245	0.412	0.735	0.020	0.025	0.034	A	1.0	Y	16
		(LH)		0.305	0.481	0.815	0.022	0.030	0.042				
	B → Y	(HL)		0.262	0.433	0.776	0.020	0.025	0.034	B	1.0		
		(LH)		0.308	0.510	0.973	0.022	0.030	0.042				
	C → Y	(HL)		0.273	0.449	0.800	0.020	0.025	0.034	C	1.0		
		(LH)		0.310	0.564	1.155	0.022	0.030	0.042				
	D → Y	(HL)		0.281	0.601	1.167	0.020	0.025	0.034	D	1.0		
		(LH)		0.339	0.596	0.985	0.022	0.030	0.042				
	E → Y	(HL)		0.312	0.678	1.407	0.020	0.025	0.034	E	1.0		
		(LH)		0.363	0.695	1.340	0.022	0.030	0.042				
	F → Y	(HL)		0.317	0.702	1.466	0.020	0.025	0.034	F	1.0		
		(LH)		0.355	0.704	1.405	0.022	0.030	0.042				
	G → Y	(HL)		0.295	0.616	1.163	0.020	0.025	0.034	G	1.0		
		(LH)		0.455	0.766	1.092	0.022	0.030	0.042				
H → Y	(HL)		0.314	0.699	1.402	0.020	0.025	0.034	H	1.0			
	(LH)		0.478	0.872	1.454	0.022	0.030	0.042					
I → Y	(HL)		0.316	0.722	1.467	0.020	0.025	0.034	I	1.0			
	(LH)		0.471	0.879	1.518	0.022	0.030	0.042					
F493	A → Y	(HL)		0.266	0.443	0.791	0.010	0.013	0.018	A	1.0	Y	34
		(LH)		0.317	0.497	0.845	0.011	0.015	0.021				
	B → Y	(HL)		0.283	0.464	0.831	0.010	0.013	0.018	B	1.0		
		(LH)		0.320	0.527	1.004	0.011	0.015	0.021				
	C → Y	(HL)		0.294	0.481	0.863	0.010	0.013	0.018	C	1.0		
		(LH)		0.323	0.581	1.187	0.011	0.015	0.021				
	D → Y	(HL)		0.330	0.686	1.379	0.010	0.013	0.018	D	1.0		
		(LH)		0.406	0.727	1.319	0.011	0.015	0.021				
	E → Y	(HL)		0.344	0.722	1.494	0.010	0.013	0.018	E	1.0		
		(LH)		0.412	0.765	1.487	0.011	0.015	0.021				
	F → Y	(HL)		0.357	0.773	1.652	0.010	0.013	0.018	F	1.0		
		(LH)		0.420	0.826	1.671	0.011	0.015	0.021				
	G → Y	(HL)		0.334	0.707	1.380	0.010	0.013	0.018	G	1.0		
		(LH)		0.525	0.912	1.451	0.011	0.015	0.021				
H → Y	(HL)		0.346	0.744	1.491	0.010	0.013	0.018	H	1.0			
	(LH)		0.531	0.952	1.621	0.011	0.015	0.021					
I → Y	(HL)		0.355	0.796	1.653	0.010	0.013	0.018	I	1.0			
	(LH)		0.542	1.016	1.801	0.011	0.015	0.021					

Chapter 2 Function Block

Function	1-1-2-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F495	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-	-	-			
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
F495	A → Y	(HL)		0.164	0.366	1.018	0.022	0.039	0.064	A	2.1	Y	2		
		(LH)		0.065	0.128	0.267	0.011	0.015	0.021						
	B → Y	(HL)		0.163	0.398	1.048	0.022	0.039	0.064					B	2.0
		(LH)		0.087	0.158	0.290	0.011	0.015	0.021						
	C → Y	(HL)		0.191	0.424	1.085	0.024	0.039	0.064					C	2.0
		(LH)		0.155	0.288	0.553	0.019	0.027	0.039						
	D → Y	(HL)		0.191	0.424	1.085	0.024	0.039	0.064	D	2.0				
		(LH)		0.155	0.288	0.553	0.019	0.027	0.039						
	E → Y	(HL)		0.222	0.456	1.103	0.025	0.039	0.064	E	2.0				
		(LH)		0.193	0.354	0.623	0.019	0.028	0.039						
	F → Y	(HL)		0.222	0.456	1.103	0.025	0.039	0.064	F	2.0				
		(LH)		0.193	0.354	0.623	0.019	0.028	0.039						

Chapter 2 Function Block

Function	3-3-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F496	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F496	A	→	Y	(HL)	0.327	0.698	1.386	0.010	0.013	0.018	A	1.0	Y	34
				(LH)	0.373	0.663	1.193	0.011	0.015	0.021	B	1.0		
	B	→	Y	(HL)	0.343	0.737	1.510	0.010	0.013	0.018	C	1.0		
				(LH)	0.378	0.701	1.359	0.011	0.015	0.021	D	1.0		
	C	→	Y	(HL)	0.358	0.793	1.683	0.010	0.013	0.018	E	1.0		
				(LH)	0.387	0.761	1.548	0.011	0.015	0.021	F	1.0		
	D	→	Y	(HL)	0.336	0.721	1.388	0.010	0.013	0.018	G	1.0		
				(LH)	0.459	0.848	1.343	0.011	0.015	0.021	H	1.0		
	E	→	Y	(HL)	0.349	0.758	1.508	0.010	0.013	0.018	I	1.0		
				(LH)	0.464	0.888	1.513	0.011	0.015	0.021	J	1.0		
	F	→	Y	(HL)	0.360	0.815	1.691	0.010	0.013	0.018	K	1.0		
				(LH)	0.475	0.953	1.699	0.011	0.015	0.021	L	1.0		
	G	→	Y	(HL)	0.330	0.685	1.379	0.010	0.013	0.018				
				(LH)	0.403	0.723	1.314	0.011	0.015	0.021				
H	→	Y	(HL)	0.345	0.723	1.493	0.010	0.013	0.018					
			(LH)	0.408	0.761	1.481	0.011	0.015	0.021					
I	→	Y	(HL)	0.356	0.774	1.649	0.010	0.013	0.018					
			(LH)	0.418	0.823	1.669	0.011	0.015	0.021					
J	→	Y	(HL)	0.331	0.706	1.376	0.010	0.013	0.018					
			(LH)	0.487	0.897	1.430	0.011	0.015	0.021					
K	→	Y	(HL)	0.342	0.741	1.487	0.010	0.013	0.018					
			(LH)	0.492	0.939	1.600	0.011	0.015	0.021					
L	→	Y	(HL)	0.350	0.792	1.646	0.010	0.013	0.018					
			(LH)	0.503	1.003	1.788	0.011	0.015	0.021					

Chapter 2 Function Block

Function	4-4-4-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F498	14										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F498	A → Y	(HL)		0.316	0.658	1.154	0.015	0.021	0.032	A	1.0	Y	25
		(LH)		0.343	0.592	1.161	0.011	0.015	0.022	B	1.0		
	B → Y	(HL)		0.332	0.678	1.191	0.015	0.021	0.032	C	1.0		
		(LH)		0.328	0.588	1.219	0.011	0.015	0.022	D	1.0		
	C → Y	(HL)		0.336	0.693	1.181	0.015	0.021	0.032	E	1.0		
		(LH)		0.323	0.552	1.048	0.011	0.015	0.022	F	1.0		
	D → Y	(HL)		0.352	0.713	1.218	0.015	0.021	0.032	G	1.0		
		(LH)		0.308	0.547	1.104	0.011	0.015	0.022	H	1.0		
	E → Y	(HL)		0.332	0.704	1.315	0.015	0.021	0.032	I	1.0		
		(LH)		0.363	0.646	1.352	0.011	0.015	0.022	J	1.0		
	F → Y	(HL)		0.346	0.722	1.345	0.015	0.021	0.032	K	1.0		
		(LH)		0.347	0.642	1.409	0.011	0.015	0.022	L	1.0		
	G → Y	(HL)		0.348	0.742	1.342	0.015	0.021	0.032	M	1.0		
		(LH)		0.342	0.604	1.228	0.011	0.015	0.022	N	1.0		
	H → Y	(HL)		0.360	0.759	1.373	0.015	0.021	0.032	O	1.0		
		(LH)		0.327	0.598	1.287	0.011	0.015	0.022	P	1.0		
	I → Y	(HL)		0.318	0.657	1.156	0.015	0.021	0.032				
		(LH)		0.344	0.595	1.162	0.011	0.015	0.022				
	J → Y	(HL)		0.333	0.679	1.192	0.015	0.021	0.032				
		(LH)		0.328	0.589	1.220	0.011	0.015	0.022				
K → Y	(HL)		0.335	0.692	1.181	0.015	0.021	0.032					
	(LH)		0.324	0.553	1.049	0.011	0.015	0.022					
L → Y	(HL)		0.351	0.713	1.219	0.015	0.021	0.032					
	(LH)		0.308	0.547	1.105	0.011	0.015	0.022					
M → Y	(HL)		0.331	0.705	1.316	0.015	0.021	0.032					
	(LH)		0.363	0.646	1.352	0.011	0.015	0.022					
N → Y	(HL)		0.345	0.721	1.345	0.015	0.021	0.032					
	(LH)		0.347	0.643	1.410	0.011	0.015	0.022					
O → Y	(HL)		0.349	0.742	1.342	0.015	0.021	0.032					
	(LH)		0.343	0.604	1.232	0.011	0.015	0.022					
P → Y	(HL)		0.362	0.759	1.375	0.015	0.021	0.032					
	(LH)		0.328	0.599	1.288	0.011	0.015	0.022					

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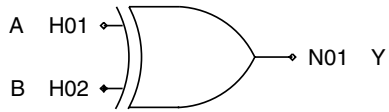
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## 2.7 Exclusive OR, Exclusive NOR

Chapter 2 Function Block

Function	2-Input Exclusive OR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L511	3								
x1	F511	4								
x2										
x4										

Logic Diagram



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Chapter 2 Function Block

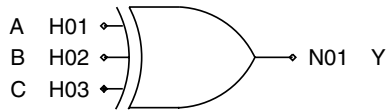
Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L511	A → Y	(HH)		0.187	0.308	0.624	0.022	0.030	0.043	A	2.0	Y	16
		(HL)		0.233	0.365	0.677	0.020	0.025	0.033				
		(LH)		0.186	0.324	0.650	0.022	0.030	0.042	B	2.0		
	(LL)		0.242	0.408	0.745	0.020	0.025	0.035					
	B → Y	(HH)		0.155	0.246	0.443	0.022	0.030	0.042				
		(HL)		0.216	0.339	0.640	0.020	0.024	0.033				
		(LH)		0.246	0.416	0.832	0.022	0.030	0.043				
		(LL)		0.252	0.374	0.573	0.020	0.025	0.035				
F511	A → Y	(HH)		0.203	0.334	0.675	0.011	0.015	0.022	A	2.0	Y	33
		(HL)		0.248	0.386	0.709	0.010	0.012	0.017				
		(LH)		0.202	0.346	0.700	0.011	0.015	0.022	B	2.0		
		(LL)		0.267	0.449	0.814	0.010	0.013	0.018				
	B → Y	(HH)		0.168	0.263	0.483	0.011	0.015	0.022				
		(HL)		0.229	0.360	0.671	0.010	0.012	0.017				
		(LH)		0.263	0.442	0.888	0.011	0.015	0.022				
		(LL)		0.274	0.410	0.639	0.010	0.013	0.018				



Chapter 2 Function Block

Function	3-Input Exclusive OR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L516	6								
x1	F516	7								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

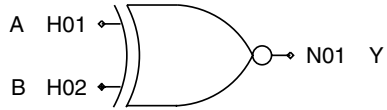
Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L516	A → Y	(HH)		0.428	0.720	1.409	0.021	0.029	0.042	A	1.0	Y	16	
		(HL)		0.370	0.584	1.082	0.020	0.026	0.035					
		(LH)		0.332	0.586	1.164	0.021	0.030	0.042					
	B → Y	(LL)		0.445	0.784	1.537	0.020	0.026	0.036	B	1.0			
		(HH)		0.326	0.529	0.985	0.021	0.030	0.042					
		(HL)		0.351	0.588	1.108	0.020	0.026	0.036					
	C → Y	(LH)		0.319	0.560	1.097	0.021	0.030	0.042	C	1.0			
		(LL)		0.330	0.560	1.072	0.020	0.026	0.035					
		(HH)		0.237	0.361	0.650	0.021	0.030	0.042					
	F516	A → Y	(HL)		0.318	0.524	0.982	0.020	0.026	0.036	A	1.0	Y	34
			(LH)		0.278	0.469	0.907	0.021	0.030	0.042				
			(LL)		0.251	0.413	0.782	0.021	0.026	0.036				
B → Y		(HH)		0.442	0.743	1.453	0.011	0.015	0.022	B	1.0			
		(HL)		0.400	0.628	1.156	0.010	0.013	0.018					
		(LH)		0.357	0.625	1.234	0.011	0.015	0.022					
C → Y		(LL)		0.451	0.797	1.566	0.010	0.013	0.019	C	1.0			
		(HH)		0.341	0.552	1.035	0.011	0.015	0.022					
		(HL)		0.361	0.607	1.147	0.010	0.013	0.019					
C → Y		(LH)		0.333	0.581	1.141	0.011	0.015	0.022					
		(LL)		0.344	0.592	1.134	0.010	0.013	0.019					
		(HH)		0.245	0.372	0.675	0.011	0.015	0.022					
C → Y	(HL)		0.323	0.535	1.006	0.010	0.013	0.019						
	(LH)		0.283	0.478	0.932	0.011	0.015	0.022						
	(LL)		0.255	0.420	0.802	0.011	0.014	0.019						

Chapter 2 Function Block

Function	2-Input Exclusive NOR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L512	3								
x1	F512	4								
x2										
x4										

Logic Diagram



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

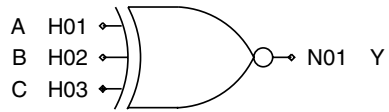
Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L512	A → Y	(HH)		0.187	0.309	0.628	0.022	0.030	0.043	A	2.0	Y	16
		(HL)		0.219	0.376	0.681	0.020	0.025	0.035				
		(LH)		0.226	0.363	0.673	0.022	0.029	0.042	B	2.0		
	(LL)		0.245	0.417	0.770	0.020	0.025	0.035					
	B → Y	(HH)		0.202	0.324	0.651	0.022	0.030	0.043				
		(HL)		0.298	0.490	0.812	0.020	0.026	0.035				
		(LH)		0.211	0.357	0.725	0.022	0.029	0.042				
		(LL)		0.172	0.313	0.660	0.020	0.025	0.035				
F512	A → Y	(HH)		0.203	0.332	0.678	0.011	0.015	0.022	A	2.0	Y	33
		(HL)		0.243	0.411	0.738	0.010	0.013	0.018				
		(LH)		0.239	0.379	0.703	0.011	0.015	0.021	B	2.0		
	(LL)		0.269	0.457	0.841	0.010	0.013	0.018					
	B → Y	(HH)		0.219	0.344	0.699	0.011	0.015	0.022				
		(HL)		0.326	0.530	0.881	0.010	0.013	0.018				
		(LH)		0.224	0.372	0.756	0.011	0.015	0.021				
		(LL)		0.192	0.347	0.718	0.010	0.013	0.018				

Chapter 2 Function Block

Function	3-Input Exclusive NOR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L517	7								
x1	F517	7								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L517	A → Y	(HH)		0.428	0.719	1.406	0.021	0.029	0.042	A	1.0	Y	16
		(HL)		0.368	0.588	1.089	0.020	0.026	0.035				
		(LH)		0.334	0.582	1.157	0.021	0.030	0.042				
	B → Y	(LL)		0.448	0.782	1.535	0.020	0.026	0.036	B	1.0		
		(HH)		0.327	0.528	0.985	0.021	0.030	0.042				
		(HL)		0.353	0.586	1.104	0.020	0.026	0.036				
	C → Y	(LH)		0.322	0.556	1.091	0.021	0.030	0.042	C	1.0		
		(LL)		0.330	0.562	1.083	0.020	0.026	0.035				
		(HH)		0.237	0.360	0.650	0.021	0.030	0.042				
		(HL)		0.318	0.525	0.982	0.020	0.026	0.036				
		(LH)		0.279	0.468	0.908	0.021	0.030	0.042				
		(LL)		0.250	0.413	0.782	0.021	0.026	0.036				
F517	A → Y	(HH)		0.442	0.741	1.451	0.011	0.015	0.022	A	1.0	Y	33
		(HL)		0.398	0.632	1.164	0.010	0.013	0.018				
		(LH)		0.359	0.622	1.228	0.011	0.015	0.022				
	B → Y	(LL)		0.452	0.796	1.565	0.010	0.013	0.019	B	1.0		
		(HH)		0.341	0.551	1.034	0.011	0.015	0.022				
		(HL)		0.362	0.604	1.142	0.010	0.013	0.019				
	C → Y	(LH)		0.336	0.578	1.135	0.011	0.015	0.022	C	1.0		
		(LL)		0.347	0.591	1.138	0.010	0.013	0.019				
		(HH)		0.245	0.372	0.675	0.011	0.015	0.022				
		(HL)		0.323	0.535	1.005	0.010	0.013	0.019				
		(LH)		0.283	0.478	0.932	0.011	0.015	0.022				
		(LL)		0.255	0.420	0.802	0.011	0.014	0.019				

[MEMO]

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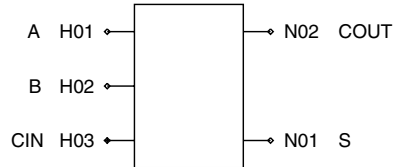
[MEMO]

## 2.8 Adder, 3-State Buffer, Decoder, Multiplexer, Generator

Chapter 2 Function Block

Function	1-Bit Full Adder									
Block type	Standard type									
	Normal			High speed						
Drivability	Name	cells	Name	cells						
Low Power										
x1	F521	9								
x2										
x4										

Logic Diagram



Truth Table

A	B	CIN	S	COUT
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.					MAX.
F521	A → S	(HH)		0.410	0.787	1.548	0.011	0.015	0.022	A	1.7	S	33
		(HL)		0.481	0.832	1.570	0.010	0.013	0.018				
		(LH)		0.479	1.078	2.172	0.011	0.015	0.022				
	A → COUT	(LL)		0.519	1.169	2.268	0.010	0.013	0.018	B	2.0	COUT	32
		(HH)		0.357	0.780	1.524	0.011	0.016	0.023				
		(LL)		0.247	0.807	1.391	0.010	0.013	0.018				
	B → S	(HH)		0.445	0.760	1.530	0.011	0.015	0.022	CIN	1.0		
		(HL)		0.484	0.853	1.641	0.010	0.013	0.018				
		(LH)		0.483	1.008	1.954	0.011	0.015	0.022				
	B → COUT	(LL)		0.515	1.111	2.072	0.010	0.013	0.018				
		(HH)		0.394	0.754	1.495	0.011	0.016	0.023				
		(LL)		0.216	0.883	1.575	0.010	0.013	0.018				
	CIN → S	(HH)		0.382	0.621	1.218	0.011	0.015	0.022				
		(HL)		0.470	0.703	1.157	0.011	0.013	0.018				
		(LH)		0.339	0.551	1.004	0.011	0.015	0.022				
	CIN → COUT	(LL)		0.345	0.571	1.098	0.010	0.012	0.017				
		(HH)		0.271	0.406	0.735	0.011	0.015	0.022				
		(LL)		0.287	0.472	0.886	0.011	0.014	0.019				

Chapter 2 Function Block

Function	4-Bit Full Adder									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power										
x1	F523	32								
x2										
x4										

Logic Diagram

Truth Table

An	Bn	CIN	Sn	COU
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

(Condition of one stage, n=1,2,3,4)

Chapter 2 Function Block

Block type	Switching speed								Input		Output						
	Path			t LDO (ns)			t 1										
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout				
F523	A1 → S1	(HH)		0.424	0.717	1.454	0.011	0.015	0.021	A1	1.7	S1	31				
		(HL)		0.519	0.853	1.667	0.010	0.012	0.017					B1	2.1	S2	30
		(LH)		0.810	1.352	2.673	0.011	0.015	0.022								
	A1 → S2	(LL)		0.537	0.874	1.585	0.010	0.012	0.017	A2	1.7	S3	29				
		(HH)		0.723	1.207	2.394	0.011	0.015	0.021					A3	1.7	COU	18
		(HL)		1.292	2.030	3.804	0.010	0.013	0.019								
	A1 → S3	(LH)		0.730	1.241	2.343	0.011	0.015	0.022	B3	2.1						
		(LL)		0.474	0.806	1.564	0.010	0.012	0.017					A4	1.7		
		(HH)		0.974	1.638	3.315	0.011	0.015	0.021								
	A1 → S4	(HL)		1.476	2.418	4.776	0.010	0.013	0.019	B4	2.0						
		(LH)		0.876	1.538	3.068	0.011	0.015	0.022					CIN	2.1		
		(LL)		0.665	1.144	2.255	0.010	0.012	0.017								
	A1 → COUT	(HH)		1.239	2.110	4.360	0.011	0.015	0.021								
		(HL)		1.579	2.625	5.315	0.010	0.013	0.018								
		(LH)		0.976	1.741	3.601	0.011	0.015	0.022								
	B1 → S1	(LL)		0.851	1.481	3.002	0.010	0.012	0.017								
		(HH)		1.302	2.207	4.624	0.013	0.019	0.029								
		(LL)		0.865	1.531	3.140	0.015	0.021	0.031								
	B1 → S2	(HH)		0.457	0.783	1.652	0.011	0.015	0.021								
		(HL)		0.498	0.827	1.637	0.010	0.012	0.017								
		(LH)		0.774	1.273	2.421	0.011	0.015	0.022								
	B1 → S3	(LL)		0.529	0.917	1.765	0.010	0.012	0.017								
		(HH)		0.701	1.181	2.366	0.011	0.015	0.021								
		(HL)		1.270	2.004	3.774	0.011	0.013	0.019								
	B1 → S4	(LH)		0.745	1.260	2.333	0.011	0.015	0.022								
		(LL)		0.492	0.831	1.575	0.010	0.012	0.017								
		(HH)		0.953	1.613	3.286	0.011	0.015	0.021								
	B1 → COUT	(HL)		1.455	2.392	4.746	0.010	0.013	0.019								
		(LH)		0.885	1.553	3.070	0.011	0.015	0.022								
		(LL)		0.678	1.157	2.237	0.010	0.012	0.017								
	A2 → S2	(HH)		1.217	2.084	4.331	0.011	0.015	0.021								
		(HL)		1.558	2.600	5.286	0.010	0.013	0.018								
		(LH)		0.985	1.757	3.598	0.011	0.015	0.022								
	A2 → S3	(LL)		0.864	1.495	2.996	0.010	0.012	0.017								
		(HH)		1.281	2.182	4.595	0.013	0.019	0.029								
		(LL)		0.874	1.546	3.140	0.015	0.021	0.031								
	A2 → S4	(HH)		0.422	0.713	1.450	0.011	0.015	0.021								
		(HL)		0.511	0.842	1.647	0.010	0.012	0.017								
		(LH)		0.784	1.318	2.633	0.011	0.015	0.022								
	A2 → COUT	(LL)		0.536	0.871	1.581	0.010	0.012	0.017								
		(HH)		0.733	1.222	2.420	0.011	0.015	0.021								
		(HL)		1.131	1.816	3.478	0.010	0.013	0.018								
	B2 → S2	(LH)		0.665	1.134	2.176	0.011	0.015	0.022								
		(LL)		0.481	0.818	1.580	0.010	0.012	0.017								
		(HH)		0.964	1.625	3.294	0.011	0.015	0.021								
	B2 → S3	(HL)		1.243	2.039	4.036	0.010	0.013	0.018								
		(LH)		0.768	1.340	2.698	0.011	0.015	0.022								
		(LL)		0.654	1.131	2.242	0.010	0.012	0.017								
B2 → S4	(HH)		0.996	1.667	3.421	0.012	0.018	0.027									
	(HL)		0.655	1.136	2.266	0.014	0.020	0.029									
	(LH)		0.457	0.782	1.646	0.011	0.015	0.022									
B2 → COUT	(HL)		0.490	0.817	1.619	0.010	0.012	0.017									
	(LH)		0.751	1.241	2.385	0.011	0.015	0.022									
	(LL)		0.530	0.915	1.759	0.010	0.012	0.017									
B2 → S3	(HH)		0.712	1.197	2.392	0.011	0.015	0.021									
	(HL)		1.110	1.790	3.449	0.010	0.013	0.018									

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B2 → S4	(LH)		0.681	1.153	2.175	0.011	0.015	0.022				
		(LL)		0.498	0.839	1.589	0.010	0.010	0.017				
	B2 → COUT	(HH)		0.943	1.600	3.266	0.011	0.015	0.021				
		(HL)		1.221	2.014	4.008	0.010	0.013	0.018				
	A3 → S3	(LH)		0.784	1.364	2.732	0.011	0.015	0.022				
		(LL)		0.669	1.144	2.229	0.010	0.012	0.017				
	A3 → S4	(HH)		0.975	1.642	3.393	0.012	0.018	0.027				
		(LL)		0.670	1.154	2.280	0.015	0.020	0.030				
	A3 → COUT	(HH)		0.424	0.718	1.454	0.011	0.015	0.021				
		(HL)		0.519	0.852	1.665	0.010	0.012	0.017				
	B3 → S3	(LH)		0.741	1.260	2.546	0.011	0.015	0.022				
		(LL)		0.537	0.874	1.584	0.010	0.012	0.017				
	A3 → S4	(HH)		0.723	1.208	2.399	0.011	0.015	0.021				
		(HL)		0.948	1.536	2.959	0.010	0.013	0.018				
	A3 → COUT	(LH)		0.564	0.966	1.886	0.011	0.015	0.022				
		(LL)		0.474	0.806	1.567	0.010	0.012	0.017				
	B3 → S3	(HH)		0.729	1.201	2.405	0.012	0.017	0.025				
		(LL)		0.456	0.784	1.522	0.012	0.016	0.022				
	B3 → S4	(HH)		0.459	0.784	1.650	0.011	0.015	0.022				
		(HL)		0.497	0.827	1.636	0.010	0.012	0.017				
	B3 → COUT	(LH)		0.712	1.190	2.320	0.011	0.015	0.022				
		(LL)		0.529	0.916	1.762	0.010	0.012	0.017				
	A4 → S4	(HH)		0.702	1.183	2.371	0.011	0.015	0.021				
		(HL)		0.927	1.511	2.930	0.010	0.013	0.018				
	B3 → COUT	(LH)		0.578	0.980	1.875	0.011	0.015	0.022				
		(LL)		0.491	0.831	1.577	0.010	0.012	0.017				
	A4 → S4	(HH)		0.708	1.176	2.376	0.012	0.017	0.025				
		(LL)		0.473	0.803	1.513	0.012	0.016	0.023				
	A4 → COUT	(HH)		0.422	0.715	1.449	0.011	0.015	0.022				
		(HL)		0.511	0.843	1.648	0.010	0.012	0.017				
	B4 → S4	(LH)		0.652	1.127	2.327	0.011	0.015	0.021				
		(LL)		0.536	0.871	1.581	0.010	0.012	0.017				
	B4 → COUT	(HH)		0.495	0.806	1.561	0.011	0.016	0.023				
		(LL)		0.279	0.467	0.883	0.011	0.013	0.018				
	CIN → S1	(HH)		0.457	0.783	1.646	0.011	0.015	0.022				
		(HL)		0.490	0.817	1.621	0.010	0.012	0.017				
	CIN → S2	(LH)		0.629	1.065	2.121	0.011	0.015	0.021				
		(LL)		0.530	0.915	1.760	0.010	0.012	0.017				
	CIN → S3	(HH)		0.475	0.780	1.533	0.011	0.016	0.023				
		(LL)		0.295	0.488	0.894	0.011	0.013	0.018				
	CIN → S4	(HH)		0.315	0.514	0.965	0.011	0.015	0.021				
		(HL)		0.427	0.666	1.160	0.010	0.013	0.018				
	CIN → S2	(LH)		0.361	0.571	1.072	0.011	0.015	0.022				
		(LL)		0.298	0.488	0.923	0.010	0.012	0.017				
	CIN → S3	(HH)		0.422	0.684	1.301	0.011	0.015	0.021				
		(HL)		0.684	1.020	1.822	0.010	0.013	0.019				
	CIN → S4	(LH)		0.551	0.951	1.879	0.011	0.016	0.022				
		(LL)		0.396	0.665	1.291	0.010	0.012	0.017				
	CIN → S1	(HH)		0.580	0.960	1.883	0.011	0.015	0.021				
		(HL)		0.908	1.447	2.721	0.010	0.013	0.018				
	CIN → S2	(LH)		0.708	1.282	2.669	0.011	0.016	0.022				
		(LL)		0.540	0.931	1.885	0.010	0.012	0.017				
	CIN → S3	(HH)		0.773	1.305	2.636	0.011	0.015	0.021				
		(HL)		1.023	1.674	3.286	0.010	0.013	0.018				
	CIN → S4	(LH)		0.814	1.493	3.204	0.011	0.015	0.022				
		(LL)		0.698	1.245	2.623	0.010	0.012	0.017				

Chapter 2 Function Block

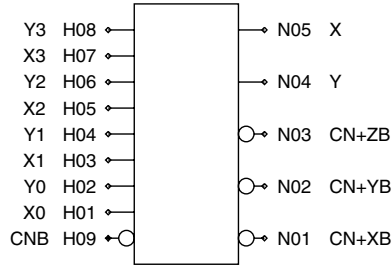
Block type	Switching speed								Input		Output			
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
	CIN	→	COUT	(HH)	0.783	1.313	2.692	0.012	0.017	0.026				
				(LL)	0.699	1.280	2.747	0.015	0.021	0.031				



Chapter 2 Function Block

Function	4-Bit Look Ahead Carry Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power										
x1	F526	34								
x2										
x4										

Logic Diagram



Truth Table

Y3	Y2	Y1	Y0	X3	X2	X1	Y
0	X	X	X	X	X	X	0
X	0	X	X	0	X	X	0
X	X	0	X	0	0	X	0
X	X	X	0	0	0	0	0
All other combinations							1

Y0	X0	CnB	Cn+xB
0	X	X	1
X	0	1	1
All other combinations			0

Y2	Y1	Y0	X2	X1	X0	CnB	Cn+zB
0	X	X	X	X	X	X	1
X	0	X	0	X	X	X	1
X	X	0	0	0	X	X	1
X	X	X	0	0	0	1	1
All other combinations							0

X3	X2	X1	X0	X
0	0	0	0	0
All other combinations				1

Y1	Y0	X1	X0	CnB	Cn+yB
0	X	X	X	X	1
X	0	0	X	X	1
X	X	0	0	1	1
All other combinations					0

Chapter 2 Function Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F526	X0	→	CN+XB (HL)	0.129	0.196	0.361	0.015	0.020	0.031	X0	7.1	CN+XB	11
			(LH)	0.148	0.229	0.361	0.021	0.029	0.041	Y0	10.9	CN+YB	10
	X0	→	CN+YB (HL)	0.336	0.542	1.094	0.010	0.013	0.018	X1	5.4	CN+ZB	34
			(LH)	0.241	0.423	0.791	0.029	0.041	0.059	Y1	9.1	Y	22
	X0	→	CN+ZB (HL)	0.557	0.976	2.329	0.010	0.012	0.017	X2	3.9	X	34
			(LH)	0.516	0.910	1.732	0.011	0.015	0.022	Y2	7.7		
	X0	→	X (HH)	0.142	0.221	0.353	0.011	0.015	0.021	X3	2.8		
			(LL)	0.348	0.521	0.807	0.011	0.015	0.022	Y3	4.3		
	Y0	→	CN+XB (HL)	0.126	0.262	0.575	0.015	0.020	0.031	CNB	2.1		
			(LH)	0.103	0.248	0.477	0.016	0.023	0.032				
	Y0	→	CN+YB (HL)	0.317	0.565	1.118	0.010	0.013	0.018				
			(LH)	0.255	0.465	0.933	0.029	0.041	0.059				
	Y0	→	CN+ZB (HL)	0.347	0.920	2.391	0.010	0.012	0.017				
			(LH)	0.300	0.754	1.511	0.011	0.015	0.022				
	Y0	→	Y (HH)	0.453	0.840	2.183	0.011	0.016	0.025				
			(LL)	0.329	0.616	1.325	0.015	0.021	0.033				
	X1	→	CN+YB (HL)	0.267	0.419	0.747	0.010	0.013	0.017				
			(LH)	0.226	0.383	0.683	0.029	0.041	0.059				
	X1	→	CN+ZB (HL)	0.345	0.585	1.278	0.010	0.012	0.017				
			(LH)	0.289	0.500	1.034	0.011	0.015	0.022				
	X1	→	Y (HH)	0.331	0.541	1.146	0.011	0.016	0.023				
			(LL)	0.275	0.436	0.769	0.015	0.021	0.033				
	X1	→	X (HH)	0.156	0.241	0.395	0.011	0.015	0.021				
			(LL)	0.364	0.580	1.051	0.011	0.015	0.022				
	Y1	→	CN+YB (HL)	0.241	0.559	1.121	0.010	0.013	0.018				
			(LH)	0.242	0.497	0.951	0.029	0.041	0.059				
	Y1	→	CN+ZB (HL)	0.305	0.932	2.386	0.010	0.012	0.017				
			(LH)	0.254	0.792	1.535	0.011	0.015	0.022				
	Y1	→	Y (HH)	0.319	0.906	2.352	0.011	0.016	0.025				
			(LL)	0.251	0.587	1.209	0.015	0.021	0.033				
	X2	→	CN+ZB (HL)	0.366	0.613	1.342	0.010	0.012	0.017				
			(LH)	0.276	0.507	1.134	0.011	0.015	0.022				
	X2	→	Y (HH)	0.300	0.506	1.138	0.011	0.016	0.023				
			(LL)	0.270	0.465	0.953	0.015	0.021	0.033				
	X2	→	X (HH)	0.167	0.257	0.419	0.011	0.015	0.022				
			(LL)	0.390	0.703	1.430	0.011	0.015	0.022				
	Y2	→	CN+ZB (HL)	0.316	1.076	2.521	0.010	0.012	0.017				
			(LH)	0.321	0.941	1.672	0.011	0.015	0.022				
	Y2	→	Y (HH)	0.288	0.947	2.388	0.011	0.016	0.025				
			(LL)	0.292	0.653	1.269	0.015	0.021	0.033				
X3	→	Y (HH)	0.309	0.518	1.167	0.011	0.015	0.022					
		(LL)	0.252	0.461	1.039	0.015	0.021	0.032					
X3	→	X (HH)	0.168	0.257	0.414	0.011	0.015	0.022					
		(LL)	0.387	0.715	1.491	0.011	0.015	0.022					
Y3	→	Y (HH)	0.278	0.937	2.379	0.011	0.016	0.025					
		(LL)	0.294	0.669	1.282	0.015	0.021	0.032					
CNB	→	CN+XB (HH)	0.252	0.415	0.744	0.021	0.029	0.041					
		(LL)	0.224	0.370	0.747	0.015	0.020	0.031					
CNB	→	CN+YB (HH)	0.399	0.659	1.199	0.029	0.041	0.059					
		(LL)	0.403	0.676	1.336	0.010	0.013	0.018					
CNB	→	CN+ZB (HH)	0.537	0.837	1.359	0.011	0.015	0.022					
		(LL)	0.443	0.746	1.476	0.010	0.012	0.017					

F526

### Chapter 2 Function Block

Function	4-Bit Carry Look Ahead Adder											
Block type	Standard type											
	Normal			High speed								
Drivability	Name	cells	Name	cells								
Low Power												
x1	F527	69										
x2												
x4												

Logic Diagram

Truth Table

A0	B0	A1	B1	A2	B2	A3	B3	*1	S0	S1	S2	S3	*2	X	Y	
0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	
0	1	0	1	0	1	0	1	0	0	1	1	1	1	1	0	0
1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	
0	1	0	1	0	1	0	1	1	1	0	1	1	1	1	0	0
1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	

(m=0,1,2,3), \*1:CinB, \*2:CoutB  
 $S_n = (A_n + B_n + CinB)$   
 $X = (A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$   
 $Y = 1; (A_n + B_n) \geq 1111$   
 $Y = 0; (A_n + B_n) < 1111$

### Chapter 2 Function Block

Block type	Switching speed								Input		Output										
	Path			t LDO (ns)			t 1														
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout								
F527	A0 → F0	(HH)		0.461	0.890	1.705	0.011	0.015	0.022	A0	2.9	F0	31								
		(HL)		0.513	0.917	1.755	0.010	0.013	0.018					B0	3.0	F1	31				
		(LH)		0.509	0.933	1.773	0.011	0.015	0.022									A1	2.9	F2	31
		(LL)		0.498	0.951	1.815	0.010	0.013	0.018												
	A0 → F1	(HH)		0.467	0.940	1.814	0.011	0.015	0.021	A2	2.9	COUTB	25								
		(HL)		0.486	0.807	1.528	0.010	0.013	0.018					B2	3.1	X	8				
		(LH)		0.488	0.791	1.513	0.011	0.015	0.022									A3	2.8	Y	28
		(LL)		0.489	0.923	1.732	0.010	0.013	0.018												
	A0 → F2	(HH)		0.693	1.163	2.308	0.011	0.015	0.021	CINB	2.1										
		(HL)		0.717	1.200	2.337	0.010	0.013	0.018												
		(LH)		0.708	1.154	2.201	0.011	0.015	0.022												
		(LL)		0.725	1.195	2.268	0.010	0.013	0.018												
	A0 → F3	(HH)		0.800	1.348	2.670	0.011	0.015	0.021												
		(HL)		0.826	1.386	2.694	0.010	0.013	0.018												
		(LH)		0.817	1.350	2.611	0.011	0.015	0.022												
		(LL)		0.837	1.389	2.672	0.010	0.013	0.018												
	A0 → COUTB	(HL)		0.877	1.454	2.860	0.015	0.020	0.030												
		(LH)		0.855	1.409	2.698	0.011	0.015	0.021												
	A0 → X	(HH)		0.311	0.507	0.925	0.011	0.015	0.022												
		(LL)		0.314	0.535	1.068	0.026	0.037	0.062												
	A0 → Y	(HH)		0.811	1.348	2.629	0.011	0.016	0.023												
		(LL)		0.821	1.350	2.569	0.010	0.013	0.017												
	B0 → F0	(HH)		0.471	0.891	1.705	0.011	0.015	0.022												
		(HL)		0.519	0.937	1.794	0.010	0.013	0.018												
		(LH)		0.484	0.960	1.839	0.011	0.015	0.022												
		(LL)		0.504	0.940	1.812	0.010	0.013	0.018												
	B0 → F1	(HH)		0.482	0.943	1.815	0.011	0.015	0.021												
		(HL)		0.502	0.827	1.568	0.010	0.013	0.017												
		(LH)		0.472	0.786	1.571	0.011	0.015	0.022												
		(LL)		0.488	0.923	1.732	0.010	0.013	0.018												
	B0 → F2	(HH)		0.707	1.183	2.348	0.011	0.015	0.021												
		(HL)		0.733	1.220	2.377	0.010	0.013	0.018												
		(LH)		0.692	1.150	2.259	0.011	0.015	0.022												
		(LL)		0.710	1.190	2.326	0.010	0.013	0.018												
	B0 → F3	(HH)		0.816	1.368	2.711	0.011	0.015	0.021												
		(HL)		0.841	1.406	2.734	0.010	0.013	0.018												
		(LH)		0.801	1.345	2.669	0.011	0.015	0.022												
		(LL)		0.822	1.385	2.730	0.010	0.013	0.018												
	B0 → COUTB	(HL)		0.893	1.474	2.900	0.015	0.020	0.030												
		(LH)		0.839	1.404	2.756	0.011	0.015	0.021												
	B0 → X	(HH)		0.311	0.508	0.927	0.011	0.015	0.022												
		(LL)		0.315	0.535	1.068	0.026	0.037	0.062												
	B0 → Y	(HH)		0.827	1.367	2.669	0.011	0.016	0.023												
		(LL)		0.805	1.345	2.627	0.010	0.013	0.017												
	A1 → F1	(HH)		0.488	0.942	1.792	0.011	0.015	0.022												
		(HL)		0.536	0.959	1.820	0.010	0.013	0.018												
		(LH)		0.546	0.968	1.816	0.011	0.015	0.022												
		(LL)		0.514	1.017	1.936	0.010	0.013	0.018												
A1 → F2	(HH)		0.516	0.895	1.879	0.011	0.015	0.021													
	(HL)		0.542	0.932	1.911	0.010	0.013	0.018													
	(LH)		0.496	0.821	1.614	0.011	0.015	0.022													
	(LL)		0.513	0.861	1.681	0.010	0.013	0.018													
A1 → F3	(HH)		0.698	1.195	2.459	0.011	0.015	0.021													
	(HL)		0.724	1.232	2.483	0.010	0.013	0.018													
	(LH)		0.676	1.110	2.130	0.011	0.015	0.022													
	(LL)		0.693	1.150	2.194	0.010	0.013	0.018													

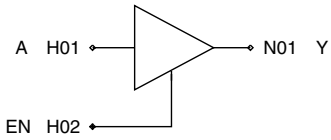
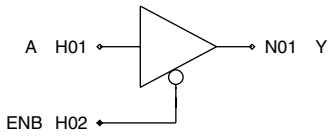
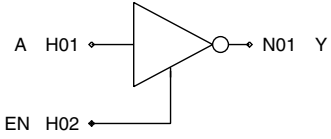
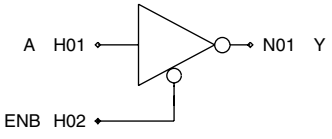
Chapter 2 Function Block

Block type	Switching speed								Input		Output	
	Path		t LDO (ns)			t 1						
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	A1 → COUTB	(HL)	0.840	1.409	2.802	0.015	0.020	0.030				
		(LH)	0.772	1.272	2.429	0.011	0.015	0.021				
	A1 → X	(HH)	0.329	0.512	0.947	0.011	0.015	0.022				
		(LL)	0.326	0.535	1.074	0.026	0.037	0.061				
	A1 → Y	(HH)	0.777	1.302	2.575	0.011	0.016	0.023				
		(LL)	0.736	1.211	2.300	0.010	0.013	0.017				
	B1 → F1	(HH)	0.498	0.944	1.793	0.011	0.015	0.022				
		(HL)	0.542	0.978	1.858	0.010	0.013	0.018				
		(LH)	0.522	0.995	1.883	0.011	0.015	0.022				
		(LL)	0.522	1.003	1.932	0.010	0.013	0.018				
	B1 → F2	(HH)	0.532	0.915	1.919	0.011	0.015	0.021				
		(HL)	0.557	0.952	1.950	0.010	0.013	0.018				
		(LH)	0.482	0.817	1.674	0.011	0.015	0.022				
		(LL)	0.498	0.857	1.741	0.010	0.013	0.018				
	B1 → F3	(HH)	0.714	1.215	2.498	0.011	0.015	0.021				
		(HL)	0.740	1.253	2.521	0.010	0.013	0.017				
		(LH)	0.662	1.105	2.191	0.011	0.015	0.022				
		(LL)	0.679	1.145	2.253	0.010	0.013	0.018				
	B1 → COUTB	(HL)	0.856	1.429	2.841	0.015	0.020	0.030				
		(LH)	0.758	1.268	2.489	0.011	0.015	0.021				
	B1 → X	(HH)	0.328	0.511	0.942	0.011	0.015	0.022				
		(LL)	0.326	0.535	1.074	0.026	0.037	0.061				
	B1 → Y	(HH)	0.793	1.322	2.612	0.011	0.016	0.023				
		(LL)	0.722	1.207	2.359	0.010	0.013	0.017				
	A2 → F2	(HH)	0.458	0.892	1.719	0.011	0.015	0.022				
		(HL)	0.516	0.907	1.734	0.010	0.013	0.018				
		(LH)	0.516	0.922	1.738	0.011	0.015	0.022				
		(LL)	0.491	0.963	1.856	0.010	0.013	0.018				
	A2 → F3	(HH)	0.545	0.949	2.057	0.011	0.015	0.021				
		(HL)	0.571	0.989	2.082	0.010	0.013	0.018				
		(LH)	0.494	0.815	1.597	0.011	0.015	0.022				
		(LL)	0.514	0.859	1.668	0.010	0.013	0.018				
	A2 → COUTB	(HL)	0.774	1.307	2.683	0.015	0.020	0.030				
		(LH)	0.665	1.082	2.025	0.011	0.015	0.021				
	A2 → X	(HH)	0.327	0.510	0.943	0.011	0.015	0.022				
		(LL)	0.321	0.528	1.064	0.026	0.037	0.061				
	A2 → Y	(HH)	0.711	1.200	2.451	0.011	0.016	0.023				
		(LL)	0.627	1.018	1.894	0.010	0.013	0.017				
	B2 → F2	(HH)	0.468	0.895	1.718	0.011	0.015	0.022				
		(HL)	0.523	0.926	1.772	0.010	0.013	0.018				
		(LH)	0.493	0.948	1.805	0.011	0.015	0.022				
		(LL)	0.499	0.951	1.852	0.010	0.013	0.018				
	B2 → F3	(HH)	0.561	0.969	2.095	0.011	0.015	0.021				
		(HL)	0.587	1.009	2.121	0.010	0.013	0.018				
		(LH)	0.481	0.812	1.657	0.011	0.015	0.022				
		(LL)	0.500	0.855	1.728	0.010	0.013	0.018				
	B2 → COUTB	(HL)	0.790	1.327	2.721	0.015	0.020	0.030				
		(LH)	0.651	1.079	2.085	0.011	0.015	0.021				
	B2 → X	(HH)	0.327	0.509	0.939	0.011	0.015	0.022				
		(LL)	0.321	0.528	1.064	0.026	0.037	0.061				
	B2 → Y	(HH)	0.727	1.220	2.490	0.011	0.016	0.023				
		(LL)	0.613	1.014	1.954	0.010	0.013	0.017				
	A3 → F3	(HH)	0.425	0.804	1.563	0.011	0.015	0.022				
		(HL)	0.459	0.848	1.636	0.010	0.013	0.018				
		(LH)	0.453	0.868	1.653	0.011	0.015	0.022				
		(LL)	0.461	0.866	1.693	0.010	0.013	0.018				

Chapter 2 Function Block

Block type	Switching speed								Input		Output	
	Path		t LDO (ns)			t 1						
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	A3 → COUTB	(HL)	0.590	1.012	2.186	0.015	0.020	0.030				
		(LH)	0.466	0.757	1.424	0.011	0.015	0.021				
	A3 → X	(HH)	0.279	0.436	0.812	0.011	0.015	0.021				
		(LL)	0.277	0.464	0.972	0.026	0.037	0.061				
	A3 → Y	(HH)	0.526	0.903	1.954	0.011	0.016	0.023				
		(LL)	0.430	0.692	1.292	0.010	0.013	0.017				
	B3 → F3	(HH)	0.434	0.807	1.562	0.011	0.015	0.022				
		(HL)	0.464	0.866	1.672	0.010	0.013	0.018				
		(LH)	0.427	0.895	1.720	0.011	0.015	0.022				
		(LL)	0.468	0.857	1.691	0.010	0.013	0.018				
	B3 → COUTB	(HL)	0.605	1.032	2.221	0.015	0.020	0.030				
		(LH)	0.452	0.753	1.485	0.011	0.015	0.021				
	B3 → X	(HH)	0.278	0.435	0.811	0.011	0.015	0.021				
		(LL)	0.277	0.465	0.971	0.026	0.037	0.061				
	B3 → Y	(HH)	0.542	0.923	1.993	0.011	0.016	0.023				
		(LL)	0.416	0.688	1.352	0.010	0.013	0.017				
	CINB → F0	(HH)	0.382	0.611	1.119	0.011	0.015	0.022				
		(HL)	0.413	0.667	1.203	0.010	0.013	0.018				
		(LH)	0.353	0.567	1.058	0.011	0.015	0.021				
		(LL)	0.361	0.577	1.047	0.010	0.013	0.017				
	CINB → F1	(HH)	0.554	0.893	1.646	0.011	0.015	0.022				
		(HL)	0.571	0.930	1.714	0.010	0.013	0.018				
		(LH)	0.531	0.867	1.635	0.011	0.015	0.021				
		(LL)	0.546	0.890	1.644	0.010	0.013	0.018				
	CINB → F2	(HH)	0.676	1.123	2.165	0.011	0.015	0.022				
		(HL)	0.696	1.164	2.228	0.010	0.013	0.018				
		(LH)	0.643	1.077	2.128	0.011	0.015	0.021				
		(LL)	0.666	1.115	2.157	0.010	0.013	0.018				
	CINB → F3	(HH)	0.743	1.235	2.389	0.011	0.015	0.022				
		(HL)	0.766	1.275	2.448	0.010	0.013	0.018				
		(LH)	0.717	1.205	2.402	0.011	0.015	0.021				
		(LL)	0.742	1.244	2.427	0.010	0.013	0.018				
	CINB → COUTB	(HH)	0.625	1.068	2.233	0.011	0.015	0.023				
		(LL)	0.437	0.693	1.242	0.015	0.020	0.031				

## Chapter 2 Function Block

Function	3-State Buffer									
Block type	Buffer type					Inverter type				
	with EN		with ENB			with EN		with ENB		
Drivability	Name	cells	Name	cells		Name	cells	Name	cells	
Low Power	L531	4	L532	4						
x1	F531	5	F532	5		F541	6	F542	6	
x2	F533	7	F534	7		F543	8	F544	8	
x4	F53F	11	F53G	11		F54F	12	F54G	12	
x8										
Logic Diagram for "Buffer with EN"					Logic Diagram for "Buffer with ENB"					
										
Logic Diagram for "Inverter with EN"					Logic Diagram for "Inverter with ENB"					
										
Truth Table										
With EN					With ENB					
A	EN	Y	Y*							
0	1	0	1							
1	1	1	0							
X	0	Z	Z	A	ENB	Y	Y*			
				0	0	0	1			
				1	0	1	0			
				X	1	Z	Z			
X:Irrelevant Z:High Impedance *:Inverter type										

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L531	A → Y	(HH)		0.164	0.255	0.463	0.022	0.030	0.042	A	2.1	Y	17
		(LL)		0.176	0.273	0.492	0.020	0.025	0.035		EN		
	EN → Y	(HZ)		0.346	0.500	0.832				Y	0.5		
		(LZ)		0.221	0.339	0.608							
		(ZH)		0.291	0.465	0.858	0.022	0.030	0.042				
		(ZL)		0.254	0.416	0.775	0.020	0.025	0.035				
F531	A → Y	(HH)		0.143	0.222	0.437	0.011	0.015	0.022	A	2.1	Y	34
		(LL)		0.164	0.249	0.397	0.010	0.013	0.017		EN		
	EN → Y	(HZ)		0.337	0.499	0.875				Y	0.5		
		(LZ)		0.231	0.349	0.589							
		(ZH)		0.271	0.432	0.837	0.011	0.015	0.022				
		(ZL)		0.244	0.392	0.671	0.010	0.013	0.018				
F533	A → Y	(HH)		0.173	0.263	0.538	0.006	0.008	0.011	A	2.1	Y	67
		(LL)		0.194	0.295	0.453	0.005	0.007	0.009		EN		
	EN → Y	(HZ)		0.402	0.583	1.044				Y	1.0		
		(LZ)		0.260	0.389	0.627							
		(ZH)		0.289	0.469	0.940	0.006	0.008	0.011				
		(ZL)		0.265	0.429	0.702	0.005	0.007	0.009				
F53F	A → Y	(HH)		0.230	0.343	0.738	0.003	0.004	0.006	A	2.1	Y	125
		(LL)		0.262	0.404	0.599	0.003	0.004	0.005		EN		
	EN → Y	(HZ)		0.532	0.754	1.380				Y	2.7		
		(LZ)		0.329	0.478	0.721							
		(ZH)		0.328	0.541	1.140	0.003	0.004	0.006				
		(ZL)		0.320	0.522	0.801	0.003	0.004	0.005				
L532	A → Y	(HH)		0.157	0.245	0.446	0.022	0.030	0.042	A	2.1	Y	17
		(LL)		0.185	0.287	0.513	0.020	0.025	0.035		ENB		
	ENB → Y	(HZ)		0.284	0.395	0.610				Y	0.5		
		(LZ)		0.293	0.445	0.783							
		(ZH)		0.215	0.351	0.664	0.022	0.030	0.042				
		(ZL)		0.315	0.529	1.010	0.020	0.025	0.035				
F532	A → Y	(HH)		0.141	0.218	0.430	0.011	0.015	0.022	A	2.1	Y	34
		(LL)		0.167	0.254	0.404	0.010	0.013	0.017		ENB		
	ENB → Y	(HZ)		0.286	0.402	0.667				Y	0.5		
		(LZ)		0.301	0.452	0.761							
		(ZH)		0.196	0.324	0.652	0.011	0.015	0.022				
		(ZL)		0.297	0.497	0.894	0.010	0.013	0.018				
F534	A → Y	(HH)		0.170	0.256	0.524	0.006	0.008	0.011	A	2.1	Y	67
		(LL)		0.200	0.304	0.467	0.005	0.007	0.009		ENB		
	ENB → Y	(HZ)		0.336	0.471	0.819				Y	1.0		
		(LZ)		0.335	0.497	0.810							
		(ZH)		0.209	0.350	0.742	0.006	0.008	0.011				
		(ZL)		0.322	0.539	0.934	0.005	0.007	0.009				
F53G	A → Y	(HH)		0.225	0.334	0.713	0.003	0.004	0.006	A	2.1	Y	126
		(LL)		0.271	0.420	0.628	0.003	0.004	0.005		ENB		
	ENB → Y	(HZ)		0.444	0.620	1.133				Y	2.7		
		(LZ)		0.414	0.596	0.914							
		(ZH)		0.242	0.413	0.931	0.003	0.004	0.006				
		(ZL)		0.388	0.652	1.053	0.003	0.004	0.005				
F541	A → Y	(HL)		0.252	0.390	0.643	0.010	0.013	0.017	A	1.0	Y	34
		(LH)		0.213	0.351	0.723	0.011	0.015	0.022		EN		
	EN → Y	(HZ)		0.347	0.509	0.888				Y	0.5		
		(LZ)		0.233	0.352	0.594							
		(ZH)		0.278	0.443	0.852	0.011	0.015	0.022				
		(ZL)		0.246	0.395	0.678	0.010	0.013	0.018				

Chapter 2 Function Block

Block type	Switching speed									Input		Output				
	Path			t LDO (ns)			t 1									
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout			
F543	A	→	Y	(HL)	0.284	0.442	0.708	0.005	0.007	0.009	A	1.0	Y	67		
				(LH)	0.236	0.387	0.822	0.006	0.008	0.011		EN			1.0	
	EN	→	Y	(HZ)	0.398	0.582	1.046	0.006	0.008	0.011	Y	1.0				
				(LZ)	0.272	0.404	0.648									
				(ZH)	0.293	0.474	0.945									
				(ZL)	0.275	0.443	0.724						0.005		0.007	0.009
F54F	A	→	Y	(HL)	0.355	0.556	0.864	0.003	0.004	0.005	A	1.0	Y	125		
				(LH)	0.285	0.466	1.020	0.003	0.004	0.006		EN			1.0	
	EN	→	Y	(HZ)	0.507	0.732	1.364	0.003	0.004	0.006	Y	2.6				
				(LZ)	0.347	0.500	0.753									
				(ZH)	0.326	0.538	1.133						0.003		0.004	0.006
				(ZL)	0.334	0.543	0.833						0.003		0.004	0.005
F542	A	→	Y	(HL)	0.252	0.390	0.643	0.010	0.013	0.017	A	1.0	Y	34		
				(LH)	0.213	0.351	0.723	0.011	0.015	0.022		ENB			1.0	
	ENB	→	Y	(HZ)	0.295	0.410	0.675	0.011	0.015	0.022	Y	0.5				
				(LZ)	0.303	0.456	0.767									
				(ZH)	0.202	0.330	0.663						0.011		0.015	0.022
				(ZL)	0.299	0.498	0.899						0.010		0.013	0.018
F544	A	→	Y	(HL)	0.284	0.442	0.708	0.005	0.007	0.009	A	1.0	Y	67		
				(LH)	0.236	0.387	0.822	0.006	0.008	0.011		ENB			1.0	
	ENB	→	Y	(HZ)	0.347	0.483	0.832	0.006	0.008	0.011	Y	1.0				
				(LZ)	0.340	0.504	0.819									
				(ZH)	0.216	0.360	0.758						0.006		0.008	0.011
				(ZL)	0.327	0.547	0.945						0.005		0.007	0.009
F54G	A	→	Y	(HL)	0.355	0.556	0.863	0.003	0.004	0.005	A	1.0	Y	125		
				(LH)	0.285	0.466	1.020	0.003	0.004	0.006		ENB			1.0	
	ENB	→	Y	(HZ)	0.457	0.631	1.146	0.003	0.004	0.006	Y	2.6				
				(LZ)	0.414	0.597	0.915									
				(ZH)	0.249	0.424	0.949						0.003		0.004	0.006
				(ZL)	0.391	0.650	1.055						0.003		0.004	0.005

[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	2 to 4 Decoder											
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L560	6					L561	6				
x1	F560	10					F561	10				
x2												
x4												

Logic Diagram

for "Positive output type"                      for "Positive output with ENB"                      for "Positive output with EN"

A H01 ←                      → N01 Y0  
 B H02 ←                      → N02 Y1  
    → N03 Y2  
    → N04 Y3

for "Negative output type"                      for "Negative output with ENB"                      for "Negative output with EN"

A H01 ←                      ○→ N01 Y0B  
 B H02 ←                      ○→ N02 Y1B  
    ○→ N03 Y2B  
    ○→ N04 Y3B

Truth Table

A	B	ENB	Y0	Y1	Y2	Y3	Y0B	Y1B	Y2B	Y3B
0	0	0	1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	1	0	1	1
0	1	0	0	0	1	0	1	1	0	1
1	1	0	0	0	0	1	1	1	1	0
X	X	1	0	0	0	0	1	1	1	1

X: Irrelevant

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LdO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L560	A → Y0	(HL)		0.273	0.419	0.730	0.020	0.025	0.033	A	1.0	Y0	8
		(LH)		0.261	0.420	0.771	0.038	0.053	0.077				
	A → Y1	(HH)		0.193	0.288	0.488	0.038	0.053	0.077	B	1.0	Y1	8
		(LL)		0.182	0.285	0.507	0.020	0.025	0.034				
	A → Y2	(HL)		0.275	0.421	0.733	0.020	0.025	0.033			Y2	8
		(LH)		0.264	0.424	0.777	0.038	0.053	0.077				
	A → Y3	(HH)		0.193	0.288	0.488	0.038	0.053	0.077			Y3	8
		(LL)		0.182	0.285	0.507	0.020	0.025	0.034				
	B → Y0	(HL)		0.291	0.444	0.781	0.020	0.025	0.034				
		(LH)		0.268	0.437	0.834	0.038	0.053	0.077				
	B → Y1	(HL)		0.291	0.444	0.781	0.020	0.025	0.034				
		(LH)		0.268	0.437	0.834	0.038	0.053	0.077				
	B → Y2	(HH)		0.196	0.302	0.550	0.038	0.053	0.077				
		(LL)		0.198	0.309	0.556	0.020	0.025	0.034				
	B → Y3	(HH)		0.193	0.298	0.544	0.038	0.053	0.077				
		(LL)		0.196	0.307	0.552	0.020	0.025	0.034				
F560	A → Y0	(HL)		0.258	0.392	0.685	0.010	0.012	0.017	A	1.0	Y0	34
		(LH)		0.276	0.450	0.876	0.011	0.015	0.022				
	A → Y1	(HH)		0.372	0.590	1.111	0.011	0.016	0.022	B	1.0	Y1	34
		(LL)		0.334	0.537	0.990	0.010	0.012	0.017				
	A → Y2	(HL)		0.263	0.399	0.694	0.010	0.012	0.017			Y2	34
		(LH)		0.281	0.457	0.887	0.011	0.015	0.022				
	A → Y3	(HH)		0.368	0.585	1.102	0.011	0.015	0.022			Y3	34
		(LL)		0.330	0.532	0.984	0.010	0.012	0.017				
	B → Y0	(HL)		0.291	0.432	0.725	0.010	0.012	0.017				
		(LH)		0.280	0.441	0.817	0.011	0.015	0.022				
	B → Y1	(HL)		0.294	0.436	0.731	0.010	0.013	0.017				
		(LH)		0.283	0.446	0.825	0.011	0.016	0.022				
	B → Y2	(HH)		0.375	0.576	1.046	0.011	0.015	0.022				
		(LL)		0.364	0.575	1.028	0.010	0.013	0.017				
	B → Y3	(HH)		0.370	0.569	1.035	0.011	0.015	0.022				
		(LL)		0.359	0.569	1.019	0.010	0.012	0.017				
L561	A → Y0B	(HH)		0.175	0.257	0.431	0.022	0.030	0.042	A	1.0	Y0B	13
		(LL)		0.194	0.311	0.585	0.030	0.041	0.062				
	A → Y1B	(HL)		0.283	0.441	0.809	0.030	0.041	0.062	B	1.0	Y1B	13
		(LH)		0.244	0.392	0.721	0.022	0.030	0.042				
	A → Y2B	(HH)		0.175	0.257	0.431	0.022	0.030	0.042			Y2B	13
		(LL)		0.194	0.310	0.585	0.030	0.041	0.062				
	A → Y3B	(HL)		0.280	0.437	0.805	0.030	0.041	0.062			Y3B	13
		(LH)		0.242	0.389	0.718	0.022	0.030	0.042				
	B → Y0B	(HH)		0.192	0.279	0.452	0.022	0.030	0.042				
		(LL)		0.186	0.285	0.509	0.029	0.040	0.062				
	B → Y1B	(HH)		0.194	0.281	0.455	0.022	0.030	0.042				
		(LL)		0.188	0.289	0.514	0.029	0.040	0.061				
	B → Y2B	(HL)		0.283	0.425	0.744	0.029	0.040	0.061				
		(LH)		0.266	0.419	0.749	0.022	0.029	0.042				
	B → Y3B	(HL)		0.282	0.426	0.744	0.029	0.040	0.061				
		(LH)		0.265	0.418	0.749	0.022	0.029	0.042				
F561	A → Y0B	(HH)		0.332	0.514	0.919	0.011	0.015	0.021	A	1.0	Y0B	35
		(LL)		0.391	0.634	1.171	0.010	0.013	0.018				
	A → Y1B	(HL)		0.320	0.496	0.882	0.010	0.013	0.018	B	1.0	Y1B	35
		(LH)		0.238	0.378	0.692	0.011	0.015	0.021				
	A → Y2B	(HH)		0.332	0.514	0.919	0.011	0.015	0.021			Y2B	35
		(LL)		0.391	0.634	1.171	0.010	0.013	0.018				
	A → Y3B	(HL)		0.320	0.496	0.882	0.010	0.013	0.018			Y3B	35
		(LH)		0.237	0.378	0.692	0.011	0.015	0.021				

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B → Y0B	(HH)		0.361	0.558	1.002	0.011	0.015	0.021				
			(LL)	0.405	0.662	1.249	0.010	0.013	0.018				
	B → Y1B	(HH)		0.361	0.558	1.002	0.011	0.015	0.021				
			(LL)	0.405	0.661	1.250	0.010	0.013	0.018				
	B → Y2B	(HL)		0.322	0.508	0.943	0.010	0.013	0.018				
			(LH)	0.259	0.413	0.760	0.011	0.015	0.021				
	B → Y3B	(HL)		0.322	0.508	0.943	0.010	0.013	0.018				
			(LH)	0.259	0.412	0.759	0.011	0.015	0.021				

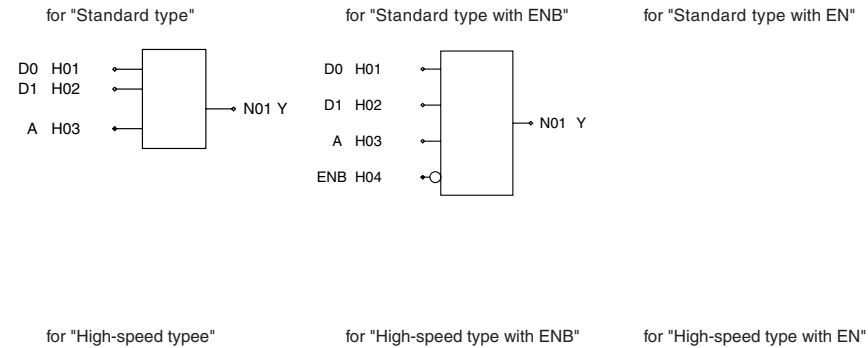
[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	2 to 1 Multiplexer (Positive Out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L565	3	L571	4								
x1	F565	4	F571	6								
x2												
x4												

Logic Diagram



Truth Table

D0	D1	A	ENB	Y	YB
X	X	X	1	0	1
A	X	0	0	A	AB
X	B	1	0	B	BB

X:Irrelevant

Chapter 2 Function Block

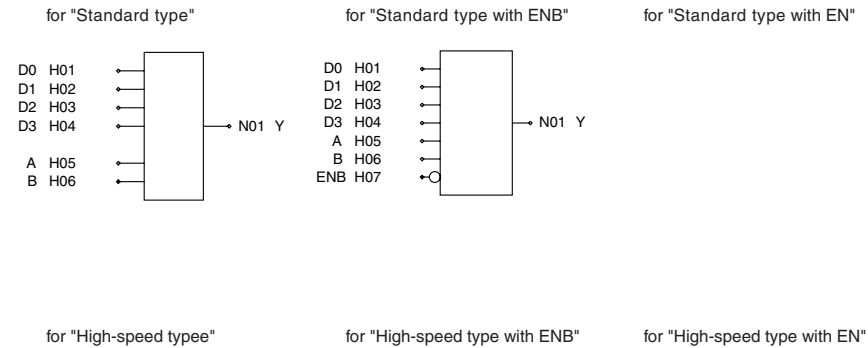
Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L565	D0 → Y	(HH)		0.222	0.340	0.616	0.022	0.030	0.042	D0	1.0	Y	16
		(LL)		0.230	0.377	0.707	0.020	0.026	0.035		D1		
	D1 → Y	(HH)		0.221	0.337	0.608	0.022	0.030	0.042	A	2.1		
		(LL)		0.223	0.372	0.701	0.020	0.026	0.035				
	A → Y	(HH)		0.159	0.248	0.428	0.022	0.030	0.042				
		(HL)		0.217	0.329	0.581	0.020	0.026	0.035				
	(LH)		0.184	0.297	0.555	0.022	0.030	0.042					
	(LL)		0.181	0.275	0.482	0.020	0.026	0.035					
F565	D0 → Y	(HH)		0.227	0.345	0.631	0.011	0.015	0.022	D0	1.0	Y	34
		(LL)		0.233	0.385	0.729	0.010	0.013	0.019		D1		
	D1 → Y	(HH)		0.225	0.342	0.627	0.011	0.015	0.022	A	1.0		
		(LL)		0.231	0.383	0.724	0.010	0.013	0.019				
	A → Y	(HH)		0.270	0.436	0.813	0.011	0.015	0.022				
		(HL)		0.277	0.441	0.786	0.010	0.013	0.018				
	(LH)		0.244	0.395	0.747	0.011	0.015	0.022					
	(LL)		0.276	0.460	0.877	0.010	0.013	0.019					
L571	D0 → Y	(HH)		0.226	0.354	0.651	0.038	0.053	0.077	D0	1.0	Y	8
		(LL)		0.216	0.363	0.690	0.020	0.026	0.036		D1		
	D1 → Y	(HH)		0.231	0.360	0.659	0.038	0.053	0.077	A	1.0		
		(LL)		0.219	0.369	0.700	0.020	0.026	0.036		ENB	1.0	
	A → Y	(HH)		0.271	0.447	0.836	0.038	0.053	0.077				
		(HL)		0.261	0.405	0.716	0.020	0.026	0.035				
	(LH)		0.242	0.398	0.751	0.038	0.053	0.078					
	(LL)		0.265	0.445	0.846	0.020	0.026	0.035					
ENB → Y	(HL)		0.093	0.128	0.195	0.020	0.024	0.033					
	(LH)		0.065	0.114	0.263	0.037	0.053	0.077					
F571	D0 → Y	(HH)		0.375	0.607	1.181	0.011	0.015	0.022	D0	1.0	Y	34
		(LL)		0.344	0.578	1.110	0.010	0.012	0.017		D1		
	D1 → Y	(HH)		0.373	0.604	1.176	0.011	0.015	0.022	A	1.0		
		(LL)		0.343	0.575	1.106	0.010	0.012	0.017		ENB	1.0	
	A → Y	(HH)		0.414	0.693	1.356	0.011	0.015	0.022				
		(HL)		0.386	0.619	1.129	0.010	0.012	0.017				
	(LH)		0.385	0.645	1.274	0.011	0.015	0.022					
	(LL)		0.387	0.653	1.254	0.010	0.012	0.017					
ENB → Y	(HL)		0.227	0.354	0.604	0.010	0.012	0.017					
	(LH)		0.218	0.355	0.678	0.011	0.015	0.022					



Chapter 2 Function Block

Function	4 to 1 Multiplexer (Positive Out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F564	8	F570	10								
x2												
x4												

Logic Diagram



Truth Table

D0	D1	D2	D3	A	B	ENB	Y	YB
X	X	X	X	X	X	1	0	1
A	X	X	X	0	0	0	A	AB
X	B	X	X	1	0	0	B	BB
X	X	C	X	0	1	0	C	CB
X	X	X	D	1	1	0	D	DB

X: Irrelevant

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F564	D0 → Y	(HH)		0.332	0.534	1.046	0.011	0.016	0.023	D0	1.0	Y	32		
		(LL)		0.338	0.584	1.161	0.011	0.015	0.021		D1			1.0	
	(HH)		0.331	0.531	1.043	0.011	0.016	0.023	D2		1.0				
	(LL)		0.335	0.579	1.151	0.011	0.015	0.021	D3		1.0				
	D1 → Y	(HH)		0.331	0.530	1.044	0.011	0.016	0.023	A	1.0	B	1.0		
		(LL)		0.336	0.581	1.158	0.011	0.015	0.021						
	D2 → Y	(HH)		0.326	0.525	1.034	0.011	0.016	0.023		B			1.0	1.0
		(LL)		0.330	0.572	1.143	0.011	0.015	0.021						
	A → Y	(HH)		0.404	0.673	1.313	0.011	0.016	0.023	A		1.0	1.0		
		(HL)		0.403	0.686	1.320	0.011	0.015	0.021						
	B → Y	(LH)		0.370	0.631	1.259	0.011	0.016	0.023		B	1.0		1.0	
		(LL)		0.398	0.697	1.391	0.011	0.015	0.021						
	ENB → Y	(HH)		0.291	0.473	0.897	0.011	0.016	0.023	ENB		1.0	1.0		
		(HL)		0.284	0.460	0.833	0.011	0.014	0.020						
ENB → Y	(LH)		0.262	0.425	0.812	0.011	0.016	0.023	ENB		1.0	1.0			
	(LL)		0.283	0.483	0.921	0.011	0.015	0.021							
F570	D0 → Y	(HH)		0.480	0.789	1.580	0.011	0.015		0.022	D0		1.0	Y	34
		(LL)		0.442	0.766	1.532	0.010	0.012		0.017			D1		
	(HH)		0.479	0.786	1.577	0.011	0.015	0.022	D2	1.0					
	(LL)		0.440	0.764	1.529	0.010	0.012	0.017	D3	1.0					
	D1 → Y	(HH)		0.475	0.779	1.566	0.011	0.015	0.022	A	1.0	B	1.0		
		(LL)		0.437	0.758	1.520	0.010	0.012	0.017						
	D2 → Y	(HH)		0.476	0.782	1.572	0.011	0.015	0.022		B			1.0	1.0
		(LL)		0.439	0.761	1.526	0.010	0.012	0.017						
	A → Y	(HH)		0.550	0.927	1.847	0.011	0.015	0.022	ENB		1.0	1.0		
		(HL)		0.510	0.873	1.691	0.010	0.012	0.017						
	B → Y	(LH)		0.516	0.884	1.787	0.011	0.015	0.022		ENB	1.0		1.0	
		(LL)		0.506	0.885	1.771	0.010	0.012	0.017						
	ENB → Y	(HH)		0.440	0.733	1.440	0.011	0.015	0.022	ENB		1.0	1.0		
		(HL)		0.399	0.647	1.177	0.010	0.012	0.017						
ENB → Y	(LH)		0.406	0.678	1.341	0.011	0.015	0.022	ENB		1.0	1.0			
	(LL)		0.398	0.680	1.309	0.010	0.012	0.017							
ENB → Y	(HL)		0.227	0.353	0.603	0.010	0.012	0.017		ENB	1.0		1.0		
	(LH)		0.218	0.355	0.677	0.011	0.015	0.022							

Chapter 2 Function Block

Function	8 to 1 Multiplexer (Positive Out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F563	18	F569	18								
x2												
x4												

Logic Diagram

for "Standard type"

for "Standard type with ENB"

for "Standard type with EN"

for "High-speed type"

for "High-speed type with ENB"

for "High-speed type with EN"

Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	A	B	C	ENB	Y	YB
X	X	X	X	X	X	X	X	X	X	X	1	0	1
A	X	X	X	X	X	X	X	0	0	0	0	A	AB
X	B	X	X	X	X	X	X	1	0	0	0	B	BB
X	X	C	X	X	X	X	X	0	1	0	0	C	CB
X	X	X	D	X	X	X	X	1	1	0	0	D	DB
X	X	X	X	E	X	X	X	0	0	1	0	E	EB
X	X	X	X	X	F	X	X	1	0	1	0	F	FB
X	X	X	X	X	X	G	X	0	1	1	0	G	GB
X	X	X	X	X	X	X	H	1	1	1	0	H	HB

X: Irrelevant

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F563	D0 → Y	(HH)		0.479	0.780	1.536	0.011	0.015	0.021	D0	1.0	Y	35	
		(LL)		0.522	0.920	1.862	0.010	0.012	0.017					
	D1 → Y	(HH)		0.476	0.777	1.533	0.011	0.015	0.021	D1	1.0			
		(LL)		0.520	0.919	1.852	0.010	0.012	0.017					
	D2 → Y	(HH)		0.477	0.778	1.536	0.011	0.015	0.021	D2	1.0			
		(LL)		0.521	0.917	1.856	0.010	0.012	0.017					
	D3 → Y	(HH)		0.472	0.771	1.525	0.011	0.015	0.021	D3	1.0			
		(LL)		0.516	0.908	1.841	0.010	0.012	0.017					
	D4 → Y	(HH)		0.475	0.776	1.530	0.011	0.015	0.021	D4	1.0			
		(LL)		0.520	0.915	1.847	0.010	0.012	0.017					
	D5 → Y	(HH)		0.471	0.770	1.521	0.011	0.015	0.021	D5	1.0			
		(LL)		0.515	0.905	1.833	0.010	0.012	0.017					
	D6 → Y	(HH)		0.472	0.771	1.523	0.011	0.015	0.021	D6	1.0			
		(LL)		0.516	0.909	1.838	0.010	0.012	0.017					
	D7 → Y	(HH)		0.467	0.763	1.513	0.011	0.015	0.021	D7	1.0			
		(LL)		0.511	0.899	1.822	0.010	0.012	0.017					
	A → Y	(HH)		0.610	1.023	1.997	0.011	0.015	0.021	A	1.0			
		(HL)		0.645	1.110	2.122	0.010	0.012	0.017					
	B → Y	(LH)		0.557	0.963	1.913	0.011	0.015	0.021	B	1.0			
		(LL)		0.643	1.146	2.304	0.010	0.012	0.017					
	C → Y	(HH)		0.459	0.762	1.479	0.011	0.015	0.021	C	1.0			
		(HL)		0.472	0.760	1.433	0.010	0.012	0.017					
			(LH)		0.418	0.697	1.359	0.011	0.015	0.021				
			(LL)		0.477	0.836	1.642	0.010	0.012	0.017				
		(HH)		0.320	0.509	0.926	0.011	0.015	0.021					
		(HL)		0.393	0.627	1.153	0.010	0.012	0.017					
		(LH)		0.371	0.610	1.144	0.011	0.015	0.021					
		(LL)		0.314	0.513	0.958	0.010	0.012	0.017					
F569	D0 → Y	(HH)		0.603	1.012	2.032	0.011	0.015	0.022	D0	1.0	Y	34	
		(LL)		0.562	0.977	1.950	0.010	0.012	0.017					
	D1 → Y	(HH)		0.601	1.013	2.032	0.011	0.015	0.022	D1	1.0			
		(LL)		0.562	0.976	1.948	0.010	0.012	0.017					
	D2 → Y	(HH)		0.596	1.003	2.018	0.011	0.015	0.022	D2	1.0			
		(LL)		0.556	0.967	1.934	0.010	0.012	0.017					
	D3 → Y	(HH)		0.597	1.005	2.020	0.011	0.015	0.022	D3	1.0			
		(LL)		0.557	0.969	1.937	0.010	0.012	0.017					
	D4 → Y	(HH)		0.588	0.992	2.000	0.011	0.015	0.022	D4	1.0			
		(LL)		0.551	0.960	1.920	0.010	0.012	0.017					
	D5 → Y	(HH)		0.587	0.991	2.000	0.011	0.015	0.022	D5	1.0			
		(LL)		0.548	0.958	1.918	0.010	0.012	0.017					
	D6 → Y	(HH)		0.586	0.990	1.997	0.011	0.015	0.022	D6	1.0			
		(LL)		0.545	0.951	1.907	0.010	0.012	0.017					
	D7 → Y	(HH)		0.586	0.990	1.997	0.011	0.015	0.022	D7	1.0			
		(LL)		0.546	0.954	1.911	0.010	0.012	0.017					
	A → Y	(HH)		0.749	1.265	2.504	0.011	0.015	0.022	A	1.0			
		(HL)		0.702	1.175	2.221	0.010	0.012	0.017					
	B → Y	(LH)		0.699	1.199	2.415	0.011	0.015	0.022	B	1.0			
		(LL)		0.698	1.214	2.408	0.010	0.012	0.017					
	C → Y	(HH)		0.593	1.006	1.984	0.011	0.015	0.022	C	1.0			
		(HL)		0.540	0.878	1.620	0.010	0.012	0.017					
			(LH)		0.553	0.942	1.870	0.011	0.015	0.022				
			(LL)		0.539	0.931	1.802	0.010	0.012	0.017				
		(HH)		0.352	0.572	1.090	0.011	0.015	0.022					
		(HL)		0.338	0.553	1.033	0.010	0.012	0.017					
		(LH)		0.355	0.610	1.220	0.011	0.015	0.022					
		(LL)		0.310	0.506	0.952	0.010	0.012	0.017					

Chapter 2 Function Block

Block type	Switching speed								Input		Output	
	Path	t LDo (ns)			t 1							
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
	ENB → Y	(HL) 0.221	0.348	0.597	0.010	0.012	0.017					
	(LH)	0.209	0.347	0.663	0.011	0.015	0.022					

[MEMO]

Chapter 2 Function Block

### Chapter 2 Function Block

Function	Quad 2 to 1 Multiplexer (Negative Out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power			L572	15								
x1			F572	17								
x2												
x4												

Logic Diagram

for "Standard type"

for "Standard type with ENB"

for "Standard type with EN"

for "High-speed type"

for "High-speed type with ENB"

for "High-speed type with EN"

Truth Table

Da	Da+1	A	ENB	Yn	YnB
A	X	0	0	A	AB
X	B	1	0	B	BB
X	X	X	1	0	1

X: Irrelevant  
a=2\*n(n=0 to 3)

### Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L572	D0	→	Y0B (HL)	0.328	0.524	0.978	0.020	0.025	0.034	D0	1.0	Y0B	16
			(LH)	0.253	0.434	0.846	0.021	0.029	0.042	D1	1.0	Y1B	16
	D1	→	Y0B (HL)	0.332	0.529	0.985	0.020	0.025	0.034	D2	1.0	Y2B	16
			(LH)	0.256	0.439	0.853	0.021	0.029	0.042	D3	1.0	Y3B	16
	D2	→	Y1B (HL)	0.328	0.524	0.980	0.020	0.025	0.034	D4	1.0		
			(LH)	0.254	0.435	0.848	0.022	0.030	0.042	D5	1.0		
	D3	→	Y1B (HL)	0.334	0.531	0.987	0.020	0.025	0.034	D6	1.0		
			(LH)	0.257	0.442	0.860	0.021	0.029	0.042	D7	1.0		
	D4	→	Y2B (HL)	0.328	0.524	0.979	0.020	0.025	0.034	A	1.0		
			(LH)	0.254	0.435	0.847	0.021	0.029	0.042	ENB	4.7		
	D5	→	Y2B (HL)	0.334	0.530	0.990	0.020	0.025	0.034				
			(LH)	0.257	0.442	0.858	0.022	0.030	0.042				
	D6	→	Y3B (HL)	0.327	0.524	0.978	0.020	0.025	0.034				
			(LH)	0.253	0.433	0.846	0.021	0.029	0.042				
	D7	→	Y3B (HL)	0.331	0.529	0.984	0.020	0.025	0.034				
			(LH)	0.257	0.438	0.852	0.021	0.029	0.042				
	A	→	Y0B (HH)	0.388	0.590	1.052	0.023	0.032	0.044				
			(HL)	0.493	0.805	1.520	0.020	0.026	0.035				
			(LH)	0.415	0.706	1.350	0.023	0.032	0.044				
			(LL)	0.427	0.706	1.343	0.020	0.026	0.035				
	A	→	Y1B (HH)	0.392	0.596	1.062	0.023	0.032	0.044				
			(HL)	0.494	0.807	1.523	0.020	0.025	0.035				
			(LH)	0.416	0.708	1.354	0.023	0.032	0.044				
			(LL)	0.430	0.711	1.350	0.020	0.025	0.035				
	A	→	Y2B (HH)	0.391	0.595	1.060	0.023	0.032	0.044				
			(HL)	0.494	0.807	1.522	0.020	0.025	0.035				
			(LH)	0.416	0.708	1.354	0.023	0.032	0.044				
			(LL)	0.429	0.710	1.349	0.020	0.025	0.035				
	A	→	Y3B (HH)	0.388	0.590	1.052	0.023	0.032	0.044				
			(HL)	0.493	0.805	1.520	0.020	0.026	0.035				
			(LH)	0.415	0.706	1.350	0.023	0.032	0.044				
			(LL)	0.427	0.706	1.343	0.020	0.026	0.035				
	ENB	→	Y0B (HH)	0.137	0.219	0.380	0.023	0.032	0.044				
			(LL)	0.172	0.285	0.587	0.020	0.025	0.035				
ENB	→	Y1B (HH)	0.135	0.217	0.379	0.023	0.032	0.044					
		(LL)	0.169	0.281	0.582	0.020	0.025	0.035					
ENB	→	Y2B (HH)	0.136	0.217	0.379	0.023	0.032	0.044					
		(LL)	0.170	0.282	0.583	0.020	0.025	0.035					
ENB	→	Y3B (HH)	0.137	0.219	0.380	0.023	0.032	0.044					
		(LL)	0.172	0.285	0.587	0.020	0.025	0.035					
F572	D0	→	Y0B (HL)	0.354	0.565	1.050	0.010	0.013	0.018	D0	1.0	Y0B	34
			(LH)	0.266	0.454	0.878	0.011	0.015	0.021	D1	1.0	Y1B	34
	D1	→	Y0B (HL)	0.358	0.568	1.058	0.010	0.013	0.018	D2	1.0	Y2B	34
			(LH)	0.270	0.458	0.886	0.011	0.015	0.021	D3	1.0	Y3B	34
	D2	→	Y1B (HL)	0.357	0.568	1.053	0.010	0.013	0.018	D4	1.0		
			(LH)	0.269	0.456	0.883	0.011	0.015	0.021	D5	1.0		
	D3	→	Y1B (HL)	0.363	0.575	1.065	0.010	0.013	0.018	D6	1.0		
			(LH)	0.273	0.465	0.897	0.011	0.015	0.021	D7	1.0		
	D4	→	Y2B (HL)	0.355	0.565	1.050	0.010	0.013	0.018	A	1.0		
			(LH)	0.266	0.454	0.878	0.011	0.015	0.021	ENB	4.7		
	D5	→	Y2B (HL)	0.358	0.569	1.058	0.010	0.013	0.018				
			(LH)	0.270	0.459	0.886	0.011	0.015	0.021				
	D6	→	Y3B (HL)	0.357	0.568	1.053	0.010	0.013	0.018				
			(LH)	0.269	0.456	0.883	0.011	0.015	0.021				
D7	→	Y3B (HL)	0.361	0.572	1.059	0.010	0.013	0.018					
		(LH)	0.273	0.461	0.890	0.011	0.015	0.021					

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDo (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	A → Y0B	(HH)		0.401	0.605	1.079	0.011	0.015	0.021				
		(HL)		0.525	0.853	1.601	0.010	0.013	0.018				
		(LH)		0.433	0.730	1.389	0.011	0.015	0.021				
		(LL)		0.457	0.752	1.419	0.010	0.013	0.018				
	A → Y1B	(HH)		0.404	0.609	1.085	0.011	0.015	0.021				
		(HL)		0.528	0.856	1.606	0.010	0.013	0.018				
		(LH)		0.434	0.733	1.393	0.011	0.015	0.021				
		(LL)		0.461	0.757	1.426	0.010	0.013	0.018				
	A → Y2B	(HH)		0.401	0.605	1.079	0.011	0.015	0.021				
		(HL)		0.526	0.853	1.602	0.010	0.013	0.018				
		(LH)		0.433	0.730	1.389	0.011	0.015	0.021				
		(LL)		0.458	0.753	1.419	0.010	0.013	0.018				
	A → Y3B	(HH)		0.404	0.610	1.086	0.011	0.015	0.021				
		(HL)		0.528	0.856	1.606	0.010	0.013	0.018				
		(LH)		0.435	0.733	1.393	0.011	0.015	0.021				
		(LL)		0.461	0.757	1.426	0.010	0.013	0.018				
	ENB → Y0B	(HH)		0.149	0.226	0.385	0.011	0.015	0.021				
		(LL)		0.196	0.323	0.654	0.010	0.013	0.018				
	ENB → Y1B	(HH)		0.149	0.226	0.385	0.011	0.015	0.021				
		(LL)		0.196	0.323	0.654	0.010	0.013	0.018				
	ENB → Y2B	(HH)		0.149	0.226	0.385	0.011	0.015	0.021				
		(LL)		0.196	0.323	0.654	0.010	0.013	0.018				
	ENB → Y3B	(HH)		0.149	0.226	0.385	0.011	0.015	0.021				
		(LL)		0.196	0.323	0.654	0.010	0.013	0.018				

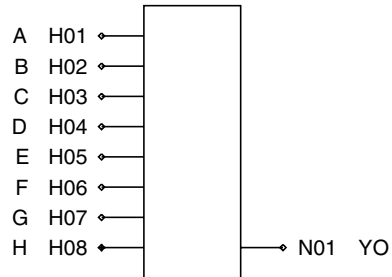
[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	8-Bit Odd Parity Generator									
Block type	Standard type									
	Normal					High speed				
Drivability	Name	cells	Name	cells						
Low Power										
x1	F581	19								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	D	E	F	G	H	YO
Σ of 1's at A through H is Odd								1
Σ of 1's at A through H is Even								0

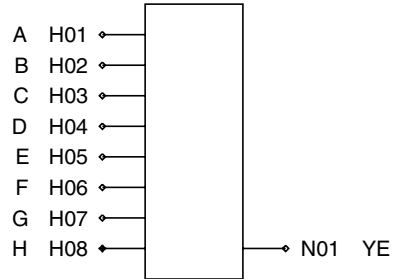
Chapter 2 Function Block

Block type	Switching speed								Input		Output				
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F581	A → YO	(HH)		0.568	0.974	2.017	0.011	0.015	0.022	A	1.7	YO	33		
		(HL)		0.560	0.935	1.849	0.010	0.012	0.017						
		(LH)		0.626	1.110	2.373	0.011	0.015	0.022						
	(LL)		0.606	0.992	1.838	0.010	0.012	0.017							
	B → YO	(HH)		0.601	1.035	2.203	0.011	0.015	0.022					B	2.0
		(HL)		0.544	0.914	1.823	0.010	0.012	0.017						
		(LH)		0.623	1.077	2.246	0.011	0.015	0.022						
	(LL)		0.599	1.035	2.017	0.010	0.012	0.017							
	C → YO	(HH)		0.554	0.935	1.881	0.011	0.015	0.022	C	1.7				
		(HL)		0.561	0.930	1.810	0.010	0.012	0.017						
		(LH)		0.616	1.076	2.251	0.011	0.015	0.022						
	(LL)		0.593	0.958	1.748	0.010	0.012	0.017							
	D → YO	(HH)		0.588	1.002	2.071	0.011	0.015	0.022			D	2.0		
		(HL)		0.544	0.908	1.783	0.010	0.012	0.017						
		(LH)		0.611	1.041	2.111	0.011	0.015	0.022						
	(LL)		0.585	0.998	1.926	0.010	0.012	0.017							
	E → YO	(HH)		0.561	0.945	1.894	0.011	0.015	0.022	E	1.7				
		(HL)		0.565	0.934	1.817	0.010	0.012	0.017						
		(LH)		0.618	1.080	2.252	0.011	0.015	0.022						
	(LL)		0.606	0.983	1.792	0.010	0.012	0.017							
	F → YO	(HH)		0.592	1.008	2.078	0.011	0.015	0.022			F	2.0		
		(HL)		0.549	0.912	1.790	0.010	0.012	0.017						
		(LH)		0.616	1.048	2.120	0.011	0.015	0.022						
	(LL)		0.599	1.023	1.973	0.010	0.012	0.017							
	G → YO	(HH)		0.556	0.919	1.773	0.011	0.015	0.022	G	1.7				
		(HL)		0.577	0.942	1.797	0.010	0.012	0.017						
		(LH)		0.618	1.058	2.141	0.011	0.015	0.022						
	(LL)		0.614	0.979	1.747	0.010	0.012	0.017							
	H → YO	(HH)		0.592	0.985	1.968	0.011	0.015	0.022			H	2.0		
		(HL)		0.561	0.920	1.770	0.010	0.012	0.017						
		(LH)		0.612	1.023	1.999	0.011	0.015	0.022						
	(LL)		0.607	1.021	1.926	0.010	0.012	0.017							

Chapter 2 Function Block

Function	8-Bit Even Parity Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power										
x1	F582	19								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	D	E	F	G	H	YE
Σ of 1's at A through H is Odd								0
Σ of 1's at A through H is Even								1

Chapter 2 Function Block

Block type	Switching speed								Input		Output				
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F582	A → YE	(HH)		0.538	0.913	1.875	0.011	0.015	0.022	A	1.7	YE	33		
		(HL)		0.533	0.913	1.859	0.010	0.013	0.018						
		(LH)		0.584	0.969	1.864	0.011	0.015	0.022						
	(LL)		0.591	1.049	2.213	0.010	0.013	0.018							
	B → YE	(HH)		0.522	0.891	1.847	0.011	0.015	0.022					B	2.0
		(HL)		0.566	0.975	2.046	0.010	0.013	0.018						
		(LH)		0.578	1.013	2.043	0.011	0.015	0.022						
	(LL)		0.588	1.017	2.086	0.010	0.013	0.018							
	C → YE	(HH)		0.540	0.907	1.835	0.011	0.015	0.022	C	1.7				
		(HL)		0.524	0.886	1.743	0.010	0.013	0.018						
		(LH)		0.571	0.935	1.774	0.011	0.015	0.022						
	(LL)		0.586	1.026	2.115	0.010	0.013	0.018							
	D → YE	(HH)		0.523	0.885	1.809	0.011	0.015	0.022			D	2.0		
		(HL)		0.559	0.952	1.934	0.010	0.013	0.018						
		(LH)		0.563	0.976	1.950	0.011	0.015	0.022						
	(LL)		0.582	0.992	1.975	0.010	0.013	0.018							
	E → YE	(HH)		0.553	0.923	1.841	0.011	0.015	0.022	E	1.7				
		(HL)		0.622	1.038	1.985	0.011	0.013	0.019						
		(LH)		0.595	0.972	1.816	0.011	0.015	0.022						
	(LL)		0.681	1.175	2.348	0.011	0.013	0.019							
	F → YE	(HH)		0.537	0.901	1.812	0.011	0.015	0.022			F	2.0		
		(HL)		0.655	1.102	2.164	0.011	0.013	0.019						
		(LH)		0.589	1.013	1.995	0.011	0.015	0.022						
	(LL)		0.678	1.141	2.214	0.011	0.013	0.019							
	G → YE	(HH)		0.564	0.929	1.816	0.011	0.015	0.022	G	1.7				
		(HL)		0.622	1.023	1.885	0.011	0.013	0.019						
		(LH)		0.601	0.965	1.766	0.011	0.015	0.022						
	(LL)		0.683	1.162	2.254	0.011	0.013	0.019							
	H → YE	(HH)		0.548	0.907	1.788	0.011	0.015	0.022			H	2.0		
		(HL)		0.659	1.089	2.081	0.011	0.013	0.019						
		(LH)		0.595	1.007	1.945	0.011	0.015	0.022						
	(LL)		0.678	1.127	2.112	0.011	0.013	0.019							

[MEMO]

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[MEMO]

## 2.9 RS-Latch, RS-F/F

### Chapter 2 Function Block

Function	RS-Latch									
Block type	Standard type									
	Normal			High speed						
Drivability	Name	cells	Name	cells						
Low Power										
x1	F595	5								
x2										
x4										

Logic Diagram

Truth Table

S	R	G	Q	QB
0	0	1	Latch	
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
1	1	1->0	Undefined	
X	X	0	Latch	

X:Irrelevant

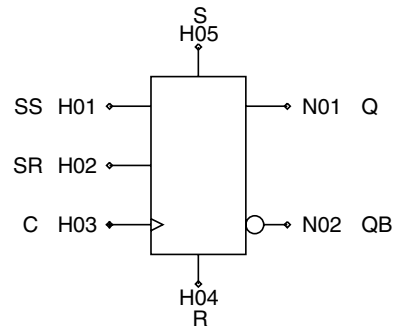
### Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F595	S → Q	(HH)		0.234	0.379	0.785	0.011	0.015	0.022	S	1.0	Q	34
			(LL)	0.305	0.516	0.944	0.011	0.014	0.019				
	S → QB	(HL)		0.529	0.853	1.587	0.011	0.014	0.019	R	1.0	QB	34
			(LL)	0.233	0.379	0.783	0.011	0.015	0.022				
	R → Q	(HL)		0.529	0.853	1.580	0.011	0.014	0.019	G	1.7		
			(LL)	0.305	0.515	0.946	0.011	0.014	0.019				
	R → QB	(HH)		0.233	0.379	0.783	0.011	0.015	0.022				
			(LL)	0.305	0.515	0.946	0.011	0.014	0.019				
	G → Q	(HH)		0.251	0.393	0.794	0.011	0.015	0.022				
			(HL)	0.539	0.864	1.593	0.011	0.014	0.019				
	G → QB	(HH)		0.251	0.394	0.796	0.011	0.015	0.022				
			(HL)	0.540	0.863	1.591	0.011	0.014	0.019				
	Set up time	S		0.900		1.460							
	Set up time	R		0.910		1.480							
Hold time	S		0.000		0.000								
Hold time	R		0.000		0.000								
Min Pulse	G		0.833		2.158								

## Chapter 2 Function Block

Function	RS-F/F with R, S											
Block type	Standard type											
	Normal				High speed							
Drivability	Name	cells	Name	cells								
Low Power												
x1	F596	11										
x2												
x4												

Logic Diagram



Truth Table

SS	SR	C	R	S	Q	QB
0	0	/	0	0	Hold	
1	0	/	0	0	1	0
X	1	/	0	0	0	1
X	X	\	0	0	Hold	
X	X	X	0	1	1	0
X	X	X	1	0	0	1
X	X	X	1	1	1	1

← Prohibition

X: Irrelevant

## Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F596	C → Q	(HH)		0.374	0.575	1.039	0.011	0.015	0.022	SS	1.0	Q	35
			(HL)	0.476	0.779	1.454	0.010	0.013	0.019	SR	1.0	QB	34
	C → QB	(HH)		0.607	1.009	1.933	0.011	0.015	0.021	C	1.0		
			(HL)	0.639	1.021	1.868	0.011	0.014	0.020	R	2.1		
	R → Q	(HL)		0.418	0.759	1.430	0.010	0.013	0.018	S	2.3		
	R → QB	(HH)		0.215	0.374	0.647	0.011	0.015	0.022				
	S → Q	(HH)		0.171	0.253	0.428	0.011	0.015	0.022				
	S → QB	(HL)		0.436	0.867	1.587	0.011	0.015	0.021				
	Set up time	SS		0.640		1.940							
	Set up time	SR		0.680		2.170							
	Hold time	SS		0.180		0.020							
	Hold time	SR		0.320		0.090							
	Release time	R		0.380		1.220							
	Release time	S		0.110		0.000							
	Removal time	R		0.430		0.310							
	Removal time	S		0.750		1.220							
	Min Pulse	C		0.841		2.303							
Min Pulse	R		0.749		1.943								
Min Pulse	S		0.670		1.959								

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## 2.10 D-Latch

[MEMO]

Chapter 2 Function Block

Function	D-Latch																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power									L601	4																		
x1	F601	6	F601NQ	5	F601NB	5																						
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	Q	QB	0	1	0	1	1	1	1	0	X	0	Latch	
D	G	Q	QB																									
0	1	0	1																									
1	1	1	0																									
X	0	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	Q	0	1	0	1	1	1	X	0	Latch				
D	G	Q																										
0	1	0																										
1	1	1																										
X	0	Latch																										
Logic Diagram for "QB output"				Truth Table for "QB output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	QB	0	1	1	1	1	0	X	0	Latch				
D	G	QB																										
0	1	1																										
1	1	0																										
X	0	Latch																										

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F601	D → Q	(HH)		0.432	0.699	1.319	0.012	0.016	0.022	D	1.0	Q	32	
				0.436	0.738	1.415	0.010	0.013	0.017					
				0.310	0.521	0.995	0.012	0.016	0.022					
	D → QB	(HL)		0.340	0.536	0.987	0.010	0.013	0.017	G	1.0	QB	32	
				0.476	0.790	1.505	0.012	0.016	0.022					
				0.480	0.774	1.427	0.010	0.013	0.017					
	G → Q	(HH)		0.476	0.790	1.505	0.012	0.016	0.022					
				0.354	0.558	1.009	0.012	0.016	0.022					
				0.385	0.629	1.174	0.010	0.013	0.017					
	Set up time	D		0.600		1.000								
Hold time			D		0.250		0.010							
				Min Pulse	G		0.639		1.836					
L601	D → Q	(HH)		0.251	0.383	0.696	0.022	0.030	0.043	D	1.0	Q	16	
				0.260	0.430	0.816	0.021	0.027	0.037					
				0.288	0.467	0.870	0.022	0.030	0.043					
	G → Q	(HH)		0.288	0.467	0.870	0.022	0.030	0.043	G	1.0			
				0.295	0.478	0.862	0.021	0.027	0.037					
				0.600		1.010								
	Set up time	D		0.600		1.010								
			Hold time	D		0.270		0.100						
					Min Pulse	G		0.450						1.195
	F601NQ	D → Q	(HH)		0.271	0.416	0.765	0.012	0.016	0.023	D	1.0	Q	31
				0.280	0.470	0.901	0.011	0.014	0.019					
				0.313	0.508	0.949	0.012	0.016	0.023					
G → Q		(HH)		0.313	0.508	0.949	0.012	0.016	0.023	G	1.0			
				0.323	0.529	0.978	0.011	0.014	0.019					
				0.610		1.080								
Set up time		D		0.610		1.080								
			Hold time	D		0.260		0.050						
					Min Pulse	G		0.480						1.316
F601NB		D → QB	(HL)		0.337	0.534	0.984	0.010	0.013	0.017	D	1.0	QB	32
				0.306	0.517	0.990	0.012	0.016	0.022					
				0.353	0.558	1.012	0.012	0.016	0.022					
	G → QB	(HH)		0.353	0.558	1.012	0.012	0.016	0.022	G	1.0			
				0.383	0.628	1.172	0.010	0.013	0.017					
				0.590		0.970								
	Set up time	D		0.590		0.970								
			Hold time	D		0.280		0.070						
					Min Pulse	G		0.516						1.501

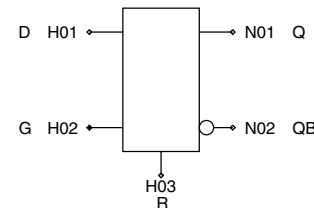
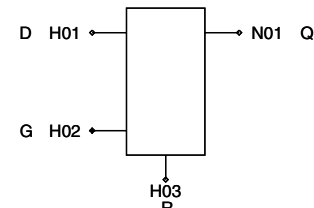
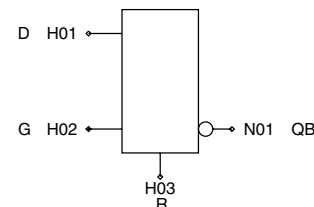
Chapter 2 Function Block

Function	D-Latch, High Speed																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power																												
x1	F6R1	6																										
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
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D	G	Q	QB																									
0	1	0	1																									
1	1	1	0																									
X	0	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F6R1	D	→	Q (HH)	0.258	0.391	0.715	0.011	0.015	0.022	D	1.0	Q	34
			(LL)	0.266	0.438	0.828	0.011	0.014	0.020				
	D	→	QB (HL)	0.384	0.601	1.120	0.010	0.013	0.017	G	1.0	QB	35
			(LH)	0.361	0.610	1.193	0.011	0.015	0.021				
	G	→	Q (HH)	0.298	0.480	0.895	0.011	0.015	0.022				
			(HL)	0.305	0.495	0.903	0.011	0.014	0.020				
	G	→	QB (HH)	0.399	0.664	1.263	0.011	0.015	0.021				
			(HL)	0.424	0.690	1.300	0.010	0.013	0.017				
	Set up time		D	0.650		1.210							
	Hold time		D	0.260		0.070							
Min Pulse		G	0.556		1.630								

Chapter 2 Function Block

Function	D-Latch with R																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power									L602	5																											
x1	F602	6	F602NQ	6	F602NB	5																															
x2																																					
x4																																					
Logic Diagram for "Normal"			Truth Table for "Normal"																																		
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D	G	R	Q	QB																																	
1	1	0	1	0																																	
0	1	0	0	1																																	
X	0	0	Latch																																		
X	X	1	0	1																																	
Logic Diagram for "Q output"			Truth Table for "Q output"																																		
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D	G	R	Q																																		
1	1	0	1																																		
0	1	0	0																																		
X	0	0	Latch																																		
X	X	1	0																																		
Logic Diagram for "QB output"			Truth Table for "QB output"																																		
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D	G	R	QB																																		
1	1	0	0																																		
0	1	0	1																																		
X	0	0	Latch																																		
X	X	1	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F602	D → Q	(HH)		0.514	0.840	1.600	0.011	0.015	0.021	D	1.0	Q	35
			(LL)	0.428	0.724	1.379	0.010	0.013	0.017				
	D → QB	(HL)		0.402	0.641	1.181	0.010	0.013	0.019	G	1.0	QB	35
			(LH)	0.292	0.494	0.947	0.011	0.015	0.021				
	G → Q	(HH)		0.557	0.930	1.783	0.011	0.015	0.021				
			(HL)	0.473	0.758	1.389	0.010	0.013	0.017				
	G → QB	(HH)		0.338	0.530	0.961	0.011	0.015	0.021				
			(HL)	0.445	0.732	1.364	0.010	0.013	0.019				
	R → Q	(HL)		0.310	0.578	1.039	0.010	0.013	0.018				
			(LH)	0.354	0.598	1.207	0.011	0.015	0.021				
	R → QB	(HH)		0.178	0.259	0.439	0.011	0.015	0.022				
			(LL)	0.242	0.398	0.789	0.010	0.013	0.019				
	Set up time	D		0.650		1.110							
	Hold time	D		0.210		0.000							
Release time	R		0.470		0.620								
Removal time	R		0.340		0.190								
Min Pulse	G		0.690		2.112								
Min Pulse	R		0.627		1.428								
L602	D → Q	(HH)		0.414	0.672	1.274	0.021	0.029	0.042	D	1.0	Q	17
			(LL)	0.369	0.633	1.218	0.020	0.025	0.034				
	G → Q	(HH)		0.446	0.752	1.444	0.021	0.029	0.042	G	1.0		
			(HL)	0.411	0.672	1.233	0.020	0.025	0.034				
	R → Q	(HL)		0.241	0.507	0.915	0.020	0.026	0.036				
			(LH)	0.251	0.425	0.870	0.021	0.029	0.042				
	Set up time	D		0.570		0.930							
	Hold time	D		0.250		0.000							
	Release time	R		0.390		0.340							
	Removal time	R		0.420		0.470							
Min Pulse	G		0.574		1.769								
Min Pulse	R		0.472		1.188								
F602NQ	D → Q	(HH)		0.379	0.606	1.255	0.012	0.017	0.025	D	1.0	Q	29
			(LL)	0.281	0.480	0.942	0.011	0.014	0.021				
	G → Q	(HH)		0.376	0.614	1.214	0.012	0.017	0.025	G	1.0		
			(HL)	0.330	0.542	1.030	0.011	0.014	0.021				
	R → Q	(HL)		0.333	0.591	1.019	0.010	0.014	0.020	R	1.0		
			(LH)	0.398	0.682	1.409	0.012	0.017	0.025				
	Set up time	D		0.750		1.490							
	Hold time	D		0.240		0.000							
	Release time	R		0.680		1.580							
	Removal time	R		0.190		0.000							
Min Pulse	G		0.514		1.545								
Min Pulse	R		0.519		1.620								
F602NB	D → QB	(HL)		0.402	0.643	1.186	0.010	0.013	0.019	D	1.0	QB	35
			(LH)	0.293	0.495	0.949	0.011	0.015	0.021				
	G → QB	(HH)		0.338	0.531	0.963	0.011	0.015	0.021	G	1.0		
			(HL)	0.445	0.733	1.369	0.010	0.013	0.019				
	R → QB	(HH)		0.178	0.259	0.440	0.011	0.015	0.022	R	1.0		
			(LL)	0.243	0.401	0.794	0.010	0.013	0.019				
	Set up time	D		0.610		1.000							
	Hold time	D		0.220		0.000							
	Release time	R		0.440		0.520							
	Removal time	R		0.370		0.300							
Min Pulse	G		0.579		1.697								
Min Pulse	R		0.503		1.005								



Chapter 2 Function Block

Function	D-Latch with R, High Speed																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F6R2	7																																			
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	G	R	Q	QB																																	
1	1	0	1	0																																	
0	1	0	0	1																																	
X	0	0	Latch																																		
X	X	1	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F6R2	D	→	Q	(HH)	0.371	0.598	1.239	0.012	0.017	0.025	D	1.0	Q	29
				(LL)	0.279	0.476	0.933	0.011	0.014	0.021	G	1.0	QB	34
	D	→	QB	(HL)	0.515	0.839	1.717	0.010	0.013	0.017	R	1.0		
				(LH)	0.392	0.675	1.349	0.011	0.015	0.021				
	G	→	Q	(HH)	0.356	0.589	1.174	0.012	0.017	0.025				
				(HL)	0.316	0.522	1.000	0.011	0.014	0.021				
	G	→	QB	(HH)	0.428	0.719	1.412	0.011	0.015	0.021				
				(HL)	0.500	0.828	1.652	0.010	0.013	0.017				
	R	→	Q	(HL)	0.332	0.586	1.012	0.010	0.014	0.020				
				(LH)	0.388	0.670	1.387	0.012	0.017	0.025				
	R	→	QB	(HH)	0.447	0.788	1.405	0.011	0.015	0.021				
				(LL)	0.532	0.910	1.865	0.010	0.013	0.017				
	Set up time	D			0.810		1.670							
	Hold time	D			0.230		0.000							
	Release time	R			0.740		1.750							
	Removal time	R			0.180		0.000							
Min Pulse	G			0.626		1.971								
Min Pulse	R			0.654		2.076								

Chapter 2 Function Block

Function	D-Latch with RB																																		
Block type	Standard type					Low Gate type																													
	Normal		Q output		QB output	Normal		Q output		QB output																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power							L603	5																											
x1	F603	7	F603NQ	5	F603NB	6																													
x2																																			
x4																																			
Logic Diagram for "Normal"		Truth Table for "Normal"																																	
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D	G	RB	Q	QB																															
1	1	1	1	0																															
0	1	1	0	1																															
X	0	1	Latch																																
X	X	0	0	1																															
Logic Diagram for "Q output"		Truth Table for "Q output"																																	
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D	G	R	Q																																
1	1	1	1																																
0	1	1	0																																
X	0	1	Latch																																
X	X	0	0																																
Logic Diagram for "QB output"		Truth Table for "QB output"																																	
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D	G	R	QB																																
1	1	1	0																																
0	1	1	1																																
X	0	1	Latch																																
X	X	0	1																																

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F603	D → Q	(HH)		0.519	0.847	1.611	0.011	0.015	0.021	D	1.0	Q	35
			(LL)	0.433	0.729	1.387	0.010	0.013	0.017				
	D → QB	(HL)		0.404	0.644	1.186	0.010	0.013	0.019	G	1.0	QB	35
			(LH)	0.294	0.496	0.950	0.011	0.015	0.021				
	G → Q	(HH)		0.562	0.938	1.793	0.011	0.015	0.021	RB	1.0		
			(HL)	0.477	0.764	1.397	0.010	0.013	0.017				
	G → QB	(HH)		0.339	0.532	0.963	0.011	0.015	0.021				
			(HL)	0.448	0.735	1.369	0.010	0.013	0.019				
	RB → Q	(HH)		0.439	0.736	1.424	0.011	0.015	0.021				
			(LL)	0.353	0.672	1.252	0.010	0.013	0.018				
	RB → QB	(HL)		0.324	0.533	1.000	0.010	0.013	0.019				
			(LH)	0.217	0.349	0.649	0.011	0.015	0.022				
	Set up time	D		0.650		1.120							
	Hold time	D		0.210		0.000							
Release time	RB		0.540		0.900								
Removal time	RB		0.270		0.000								
Min Pulse	G		0.695		2.122								
Min Pulse	RB		0.561		1.669								
L603	D → Q	(HH)		0.413	0.680	1.324	0.022	0.030	0.042	D	1.0	Q	17
			(LL)	0.385	0.660	1.277	0.020	0.025	0.034				
	G → Q	(HH)		0.449	0.762	1.498	0.022	0.030	0.042	G	1.0		
			(HL)	0.424	0.695	1.288	0.020	0.025	0.034				
	RB → Q	(HH)		0.324	0.536	1.002	0.022	0.029	0.042	RB	1.0		
			(LL)	0.283	0.574	1.042	0.020	0.026	0.036				
	Set up time	D		0.580		0.960							
	Hold time	D		0.250		0.000							
	Release time	RB		0.430		0.460							
	Removal time	RB		0.380		0.360							
Min Pulse	G		0.578		1.823								
Min Pulse	RB		0.476		1.295								
F603NQ	D → Q	(HH)		0.378	0.604	1.251	0.013	0.018	0.026	D	1.0	Q	28
			(LL)	0.276	0.472	0.931	0.011	0.014	0.021				
	G → Q	(HH)		0.373	0.609	1.207	0.013	0.018	0.026	G	1.0		
			(HL)	0.323	0.531	1.014	0.011	0.014	0.021				
	RB → Q	(HH)		0.356	0.591	1.235	0.013	0.018	0.026	RB	1.0		
			(LL)	0.254	0.470	0.810	0.010	0.014	0.020				
	Set up time	D		0.740		1.480							
	Hold time	D		0.240		0.000							
	Release time	RB		0.660		1.370							
	Removal time	RB		0.190		0.000							
Min Pulse	G		0.508		1.534								
Min Pulse	RB		0.642		1.514								
F603NB	D → QB	(HL)		0.405	0.646	1.191	0.010	0.013	0.019	D	1.0	QB	35
			(LH)	0.295	0.497	0.952	0.011	0.015	0.021				
	G → QB	(HH)		0.340	0.533	0.965	0.011	0.015	0.021	G	1.0		
			(HL)	0.448	0.736	1.373	0.010	0.013	0.019				
	RB → QB	(HL)		0.325	0.536	1.006	0.010	0.013	0.019	RB	1.0		
			(LH)	0.217	0.349	0.650	0.011	0.015	0.022				
	Set up time	D		0.610		1.010							
	Hold time	D		0.220		0.000							
	Release time	RB		0.500		0.800							
	Removal time	RB		0.310		0.030							
Min Pulse	G		0.581		1.702								
Min Pulse	RB		0.447		1.250								

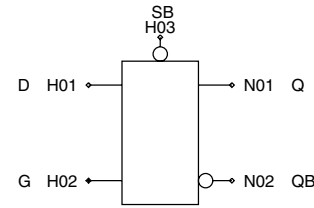
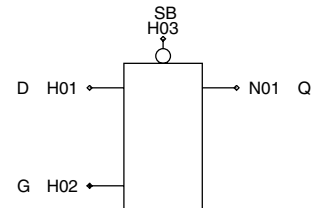
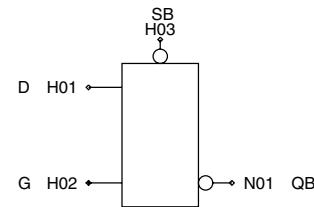
Chapter 2 Function Block

Function	D-Latch with RB, High Speed																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F6R5	6																																			
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	G	RB	Q	QB																																	
1	1	1	1	0																																	
0	1	1	0	1																																	
X	0	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F6R5	D	→	Q	(HH)	0.370	0.596	1.235	0.012	0.017	0.025	D	1.0	Q	29
				(LL)	0.278	0.474	0.929	0.011	0.014	0.021	G	1.0	QB	34
	D	→	QB	(HL)	0.501	0.818	1.686	0.010	0.013	0.017	RB	1.0		
				(LH)	0.379	0.657	1.323	0.011	0.015	0.021				
	G	→	Q	(HH)	0.356	0.587	1.172	0.012	0.017	0.025				
				(HL)	0.314	0.520	0.997	0.011	0.014	0.021				
	G	→	QB	(HH)	0.415	0.702	1.387	0.011	0.015	0.021				
				(HL)	0.485	0.809	1.622	0.010	0.013	0.017				
	RB	→	Q	(HH)	0.342	0.575	1.208	0.012	0.017	0.025				
				(LL)	0.256	0.471	0.811	0.010	0.014	0.020				
	RB	→	QB	(HL)	0.472	0.797	1.659	0.010	0.013	0.017				
				(LH)	0.348	0.639	1.159	0.011	0.015	0.021				
	Set up time	D			0.790		1.640							
	Hold time	D			0.230		0.000							
Release time	RB			0.720		1.530								
Removal time	RB			0.190		0.000								
Min Pulse	G			0.612		1.942								
Min Pulse	RB			0.761		1.938								

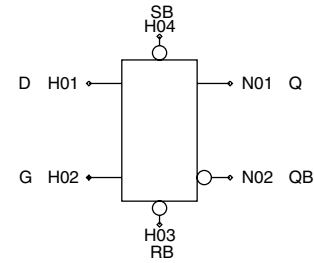
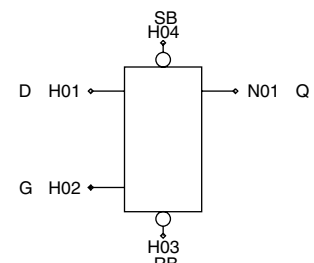
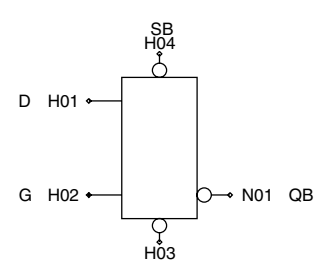
Chapter 2 Function Block

Function	D-Latch with SB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F60K	7	F60KNQ	6	F60KNB	5																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	G	SB	Q	QB																																	
0	1	1	0	1																																	
1	1	1	1	0																																	
X	0	1	Latch																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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D	G	SB	Q																																		
0	1	1	0																																		
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Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	G	SB	QB																																		
0	1	1	1																																		
1	1	1	0																																		
X	0	1	Latch																																		
X	X	0	0																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F60K	D → Q	(HH)		0.271	0.415	0.739	0.011	0.016	0.022	D	1.0	Q	32
			(LL)	0.445	0.713	1.271	0.013	0.017	0.025				
	D → QB	(HL)		0.407	0.641	1.166	0.010	0.013	0.017	G	1.0	QB	34
			(LH)	0.566	0.931	1.747	0.011	0.015	0.021				
	G → Q	(HH)		0.314	0.504	0.915	0.011	0.016	0.022	SB	1.0		
			(HL)	0.370	0.577	1.012	0.013	0.017	0.025				
	G → QB	(HH)		0.489	0.792	1.469	0.011	0.015	0.021				
			(HL)	0.450	0.728	1.340	0.010	0.013	0.017				
	SB → Q	(HL)		0.527	0.882	1.646	0.013	0.017	0.025				
			(LH)	0.276	0.437	0.765	0.011	0.016	0.023				
	SB → QB	(HH)		0.647	1.101	2.122	0.011	0.015	0.021				
			(LL)	0.417	0.672	1.234	0.010	0.013	0.017				
	Set up time	D		0.910		1.850							
	Hold time	D		0.270		0.050							
Release time	SB		0.920		2.230								
Removal time	SB		0.010		0.000								
Min Pulse	G		0.648		1.812								
Min Pulse	SB		0.730		2.359								
F60KNQ	D → Q	(HH)		0.272	0.417	0.742	0.011	0.016	0.022	D	1.0	Q	32
			(LL)	0.453	0.723	1.291	0.013	0.017	0.026				
	G → Q	(HH)		0.312	0.502	0.914	0.011	0.015	0.022	G	1.0		
			(HL)	0.375	0.584	1.026	0.013	0.017	0.025				
	SB → Q	(HL)		0.534	0.893	1.665	0.013	0.017	0.026	SB	1.0		
			(LH)	0.275	0.439	0.768	0.011	0.016	0.023				
	Set up time	D		0.860		1.700							
	Hold time	D		0.270		0.050							
	Release time	SB		0.870		2.070							
	Removal time	SB		0.010		0.000							
Min Pulse	G		0.530		1.368								
Min Pulse	SB		0.616		1.904								
F60KNB	D → QB	(HL)		0.323	0.510	0.935	0.010	0.013	0.017	D	1.0	QB	34
			(LH)	0.348	0.596	1.191	0.011	0.015	0.022				
	G → QB	(HH)		0.390	0.629	1.201	0.011	0.015	0.022	G	1.0		
			(HL)	0.371	0.605	1.121	0.010	0.013	0.017				
	SB → QB	(HH)		0.201	0.306	0.580	0.011	0.015	0.022	SB	1.0		
			(LL)	0.183	0.285	0.480	0.010	0.013	0.017				
	Set up time	D		0.630		1.130							
	Hold time	D		0.280		0.080							
	Release time	SB		0.420		0.410							
	Removal time	SB		0.390		0.410							
Min Pulse	G		0.550		1.538								
Min Pulse	SB		0.406		0.879								

Chapter 2 Function Block

Function	D-Latch with RB, SB																																																					
Block type	Standard type					Low Gate type																																																
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F60J	7	F60JNQ	6	F60JNB	6																																																
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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D	G	RB	SB	Q	QB																																																	
0	1	1	1	0	1																																																	
1	1	1	1	1	0																																																	
X	0	1	1	Latch																																																		
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D	G	RB	SB	Q																																																		
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X	0	1	1	Latch																																																		
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Logic Diagram for "QB output"				Truth Table for "QB output"																																																		
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D	G	RB	SB	QB																																																		
0	1	1	1	1																																																		
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X	X	0	1	1																																																		
X	X	1	0	0																																																		
X	X	0	0	1																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F60J	D → Q	(HH)		0.383	0.622	1.258	0.012	0.017	0.025	D	1.0	Q	25	
		(LL)		0.460	0.763	1.426	0.013	0.018	0.027					
	D → QB	(HL)		0.531	0.869	1.741	0.010	0.013	0.017	G	1.0	QB	33	
		(LH)		0.588	0.994	1.931	0.011	0.015	0.021					
	G → Q	(HH)		0.373	0.613	1.189	0.012	0.017	0.025	RB	1.0			
		(HL)		0.378	0.606	1.124	0.013	0.018	0.026					
	G → QB	(HH)		0.505	0.835	1.618	0.011	0.015	0.021	SB	1.0			
		(HL)		0.521	0.858	1.671	0.010	0.013	0.017					
	RB → Q	(HH)		0.355	0.597	1.219	0.012	0.017	0.025					
		(LL)		0.271	0.489	0.821	0.010	0.014	0.020					
	RB → QB	(HL)		0.504	0.843	1.702	0.010	0.013	0.017					
		(LH)		0.384	0.690	1.211	0.011	0.015	0.021					
	SB → Q	(HL)		0.555	0.943	1.807	0.013	0.018	0.027					
		(LH)		0.415	0.717	1.458	0.011	0.017	0.026					
	SB → QB	(HH)		0.683	1.174	2.312	0.011	0.015	0.021					
(LL)			0.571	0.976	2.015	0.010	0.013	0.017						
	Set up time	D		0.900		1.990								
	Hold time	D		0.130		0.000								
	Release time	RB		0.730		1.540								
	Release time	SB		0.950		2.380								
	Removal time	RB		0.180		0.000								
	Removal time	SB		0.000		0.000								
	Min Pulse	G		0.650		1.990								
	Min Pulse	RB		0.813		1.986								
	Min Pulse	SB		0.756		2.553								
F60JNQ	D → Q	(HH)		0.390	0.630	1.274	0.012	0.017	0.025	D	1.0	Q	25	
		(LL)		0.468	0.773	1.445	0.013	0.018	0.027					
	G → Q	(HH)		0.378	0.619	1.203	0.012	0.017	0.025	G	1.0			
		(HL)		0.386	0.615	1.142	0.013	0.018	0.027					
	RB → Q	(HH)		0.362	0.605	1.235	0.012	0.017	0.025	RB	1.0			
		(LL)		0.269	0.490	0.824	0.010	0.014	0.020					
	SB → Q	(HL)		0.562	0.953	1.826	0.013	0.018	0.027	SB	1.0			
		(LH)		0.414	0.726	1.477	0.011	0.017	0.026					
		Set up time	D		0.840		1.820							
		Hold time	D		0.120		0.000							
		Release time	RB		0.690		1.400							
		Release time	SB		0.890		2.220							
		Removal time	RB		0.180		0.000							
		Removal time	SB		0.000		0.000							
		Min Pulse	G		0.533		1.523							
	Min Pulse	RB		0.663		1.518								
	Min Pulse	SB		0.640		2.064								
F60JNB	D → QB	(HL)		0.424	0.690	1.407	0.010	0.013	0.018	D	1.0	QB	34	
		(LH)		0.375	0.657	1.363	0.011	0.015	0.022					
	G → QB	(HH)		0.425	0.713	1.426	0.011	0.015	0.022	G	1.0			
		(HL)		0.427	0.704	1.381	0.010	0.013	0.018					
	RB → QB	(HL)		0.401	0.674	1.386	0.010	0.013	0.018	RB	1.0			
		(LH)		0.367	0.678	1.274	0.011	0.015	0.022					
	SB → QB	(HH)		0.200	0.305	0.576	0.011	0.015	0.022	SB	1.0			
		(LL)		0.182	0.281	0.473	0.010	0.013	0.017					
		Set up time	D		0.690		1.290							
		Hold time	D		0.200		0.000							
		Release time	RB		0.630		1.190							
		Release time	SB		0.390		0.320							
		Removal time	RB		0.190		0.000							
		Removal time	SB		0.430		0.560							

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDo (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Min Pulse		G	0.583		1.761							
	Min Pulse		RB	0.655		1.661							
	Min Pulse		SB	0.407		0.879							

[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	D-Latch (GB)																										
Block type	Standard type						Low Gate type																				
	Normal		Q output		QB output		Normal		Q output		QB output																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells															
Low Power									L604	4																	
x1	F604	6	F604NQ	5	F604NB	5																					
x2																											
x4																											
Logic Diagram for "Normal"				Truth Table for "Normal"																							
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								D	GB	Q	QB	1	0	1	0	0	0	0	1	X	1	Latch	
D	GB	Q	QB																								
1	0	1	0																								
0	0	0	1																								
X	1	Latch																									
Logic Diagram for "Q output"				Truth Table for "Q output"																							
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								D	GB	Q	1	0	1	0	0	0	X	1	Latch				
D	GB	Q																									
1	0	1																									
0	0	0																									
X	1	Latch																									
Logic Diagram for "QB output"				Truth Table for "QB output"																							
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								D	GB	QB	1	0	0	0	0	1	X	1	Latch				
D	GB	QB																									
1	0	0																									
0	0	1																									
X	1	Latch																									

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F604	D → Q	(HH)		0.417	0.674	1.276	0.011	0.015	0.021	D	1.0	Q	35
				0.421	0.711	1.360	0.010	0.013	0.017				
	D → QB	(HL)		0.324	0.508	0.929	0.010	0.013	0.017	GB	1.0	QB	35
				0.295	0.495	0.948	0.011	0.015	0.021				
	GB → Q	(LH)		0.430	0.717	1.378	0.011	0.015	0.021				
				0.467	0.788	1.506	0.010	0.013	0.017				
	GB → QB	(LH)		0.342	0.573	1.094	0.011	0.015	0.021				
				0.337	0.551	1.028	0.010	0.013	0.017				
		Set up time	D		0.610		0.960						
		Hold time	D		0.280		0.000						
	Min Pulse	GB		0.644		1.802							
L604	D → Q	(HH)		0.253	0.385	0.699	0.022	0.030	0.043	D	1.0	Q	16
				0.262	0.433	0.820	0.021	0.027	0.038				
	GB → Q	(LH)		0.264	0.427	0.805	0.022	0.030	0.043	GB	1.0	QB	16
				0.296	0.497	0.949	0.021	0.027	0.037				
		Set up time	D		0.630		0.940						
		Hold time	D		0.270		0.000						
	Min Pulse	GB		0.475		1.247							
F604NQ	D → Q	(HH)		0.271	0.416	0.765	0.012	0.016	0.023	D	1.0	Q	31
				0.280	0.469	0.901	0.011	0.014	0.019				
	GB → Q	(LH)		0.288	0.470	0.889	0.012	0.016	0.023	GB	1.0	QB	31
				0.322	0.542	1.041	0.011	0.014	0.019				
		Set up time	D		0.640		1.000						
	Min Pulse	GB		0.508		1.345							
F604NB	D → QB	(HL)		0.337	0.534	0.984	0.010	0.013	0.017	D	1.0	QB	32
				0.306	0.517	0.990	0.012	0.016	0.022				
	GB → QB	(LH)		0.356	0.598	1.143	0.012	0.016	0.022	GB	1.0	QB	32
				0.354	0.579	1.088	0.010	0.013	0.017				
		Set up time	D		0.590		0.910						
	Min Pulse	GB		0.534		1.440							

## Chapter 2 Function Block

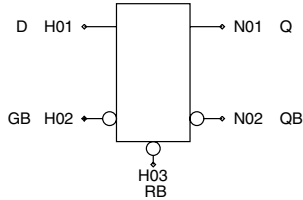
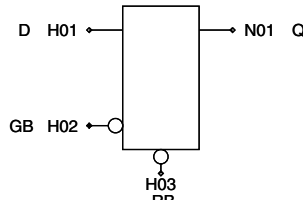
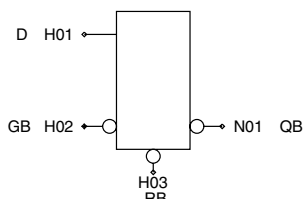
Function	D-Latch (GB), High Speed																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power																												
x1	F6R8	6																										
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	Q	QB	1	0	1	0	0	0	0	1	X	1	Latch	
D	GB	Q	QB																									
1	0	1	0																									
0	0	0	1																									
X	1	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

## Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F6R8	D	→	Q (HH)	0.261	0.394	0.719	0.011	0.015	0.022	D	1.0	Q	34
			(LL)	0.267	0.443	0.835	0.011	0.014	0.020				
	D	→	QB (HL)	0.387	0.605	1.125	0.010	0.013	0.017	GB	1.0	QB	35
			(LH)	0.362	0.615	1.201	0.011	0.015	0.021				
	GB	→	Q (LH)	0.273	0.443	0.837	0.011	0.015	0.022				
			(LL)	0.302	0.506	0.963	0.011	0.014	0.020				
	GB	→	QB (LH)	0.397	0.677	1.325	0.011	0.015	0.021				
			(LL)	0.399	0.653	1.242	0.010	0.013	0.017				
	Set up time		D	0.670		1.100							
	Hold time		D	0.260		0.000							
Min Pulse		GB	0.587		1.627								



Chapter 2 Function Block

Function	D-Latch (GB) with RB																																				
Block type	Standard type					Low Gate type																															
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power								L605	5																												
x1	F605	7	F605NQ	5	F605NB	6																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	QB	1	0	1	1	0	0	0	1	0	1	X	1	1	Latch		X	X	0	0	1
D	GB	RB	Q	QB																																	
1	0	1	1	0																																	
0	0	1	0	1																																	
X	1	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td>Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	1	0	1	1	0	0	1	0	X	1	1	Latch	X	X	0	0					
D	GB	RB	Q																																		
1	0	1	1																																		
0	0	1	0																																		
X	1	1	Latch																																		
X	X	0	0																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td>Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	QB	1	0	1	0	0	0	1	1	X	1	1	Latch	X	X	0	1					
D	GB	RB	QB																																		
1	0	1	0																																		
0	0	1	1																																		
X	1	1	Latch																																		
X	X	0	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F605	D → Q	(HH)		0.519	0.847	1.611	0.011	0.015	0.021	D	1.0	Q	35
		(LL)		0.432	0.729	1.386	0.010	0.013	0.017				
	D → QB	(HL)		0.404	0.643	1.186	0.010	0.013	0.019	GB	1.0	QB	35
		(LH)		0.294	0.496	0.950	0.011	0.015	0.021				
	GB → Q	(LH)		0.532	0.889	1.709	0.011	0.015	0.021				
		(LL)		0.481	0.808	1.535	0.010	0.013	0.017				
	GB → QB	(LH)		0.343	0.576	1.100	0.011	0.015	0.021				
		(LL)		0.417	0.685	1.283	0.010	0.013	0.019				
	RB → Q	(HH)		0.439	0.736	1.424	0.011	0.015	0.021				
		(LL)		0.353	0.672	1.252	0.010	0.013	0.018				
	RB → QB	(HL)		0.324	0.534	1.000	0.010	0.013	0.019				
		(LH)		0.217	0.349	0.649	0.011	0.015	0.022				
	Set up time	D		0.670		1.190							
	Hold time	D		0.280		0.000							
Release time	RB		0.540		0.960								
Removal time	RB		0.270		0.000								
Min Pulse	GB		0.707		2.012								
Min Pulse	RB		0.561		1.669								
L605	D → Q	(HH)		0.411	0.677	1.319	0.022	0.030	0.042	D	1.0	Q	17
		(LL)		0.383	0.658	1.274	0.020	0.025	0.034				
	GB → Q	(LH)		0.421	0.717	1.419	0.022	0.030	0.042	GB	1.0		
		(LL)		0.424	0.726	1.408	0.020	0.025	0.034				
	RB → Q	(HH)		0.321	0.532	0.998	0.022	0.029	0.042				
		(LL)		0.281	0.571	1.038	0.020	0.026	0.036				
	Set up time	D		0.610		0.970							
	Hold time	D		0.300		0.040							
	Release time	RB		0.430		0.540							
	Removal time	RB		0.380		0.280							
Min Pulse	GB		0.596		1.716								
Min Pulse	RB		0.472		1.289								
F605NQ	D → Q	(HH)		0.371	0.595	1.237	0.012	0.017	0.025	D	1.0	Q	29
		(LL)		0.276	0.472	0.931	0.011	0.014	0.021				
	GB → Q	(LH)		0.338	0.560	1.136	0.012	0.017	0.025	GB	1.0		
		(LL)		0.317	0.536	1.052	0.011	0.014	0.021				
	RB → Q	(HH)		0.348	0.582	1.221	0.012	0.017	0.025				
		(LL)		0.254	0.472	0.810	0.010	0.014	0.020				
	Set up time	D		0.810		1.630							
	Hold time	D		0.290		0.000							
	Release time	RB		0.730		1.530							
	Removal time	RB		0.110		0.000							
Min Pulse	GB		0.529		1.444								
Min Pulse	RB		0.626		1.499								
F605NB	D → QB	(HL)		0.404	0.646	1.191	0.010	0.013	0.019	D	1.0	QB	35
		(LH)		0.295	0.497	0.951	0.011	0.015	0.021				
	GB → QB	(LH)		0.344	0.575	1.100	0.011	0.015	0.021	GB	1.0		
		(LL)		0.417	0.687	1.289	0.010	0.013	0.019				
	RB → QB	(HL)		0.325	0.536	1.006	0.010	0.013	0.019	RB	1.0		
		(LH)		0.217	0.349	0.650	0.011	0.015	0.022				
	Set up time	D		0.650		1.110							
	Hold time	D		0.290		0.020							
	Release time	RB		0.510		0.860							
	Removal time	RB		0.310		0.000							
Min Pulse	GB		0.593		1.588								
Min Pulse	RB		0.447		1.249								

Chapter 2 Function Block

Function	D-Latch (GB) with RB, High Speed																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F6R9	6																																			
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	QB	1	0	1	1	0	0	0	1	0	1	X	1	1	Latch		X	X	0	0	1
D	GB	RB	Q	QB																																	
1	0	1	1	0																																	
0	0	1	0	1																																	
X	1	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F6R9	D → Q	(HH)		0.370	0.596	1.235	0.012	0.017	0.025	D	1.0	Q	29
		(LL)		0.278	0.474	0.930	0.011	0.014	0.021				
	D → QB	(HL)		0.500	0.818	1.686	0.010	0.013	0.017	GB	1.0	QB	34
		(LH)		0.379	0.657	1.324	0.011	0.015	0.021				
	GB → Q	(LH)		0.331	0.549	1.115	0.012	0.017	0.025	RB	1.0		
		(LL)		0.310	0.525	1.035	0.011	0.014	0.021				
	GB → QB	(LH)		0.412	0.707	1.425	0.011	0.015	0.021				
		(LL)		0.460	0.771	1.566	0.010	0.013	0.017				
	RB → Q	(HH)		0.342	0.575	1.207	0.012	0.017	0.025				
		(LL)		0.256	0.471	0.810	0.010	0.014	0.020				
	RB → QB	(HL)		0.472	0.797	1.658	0.010	0.013	0.017				
		(LH)		0.348	0.639	1.159	0.011	0.015	0.021				
	Set up time	D		0.850		1.770							
	Hold time	D		0.280		0.000							
Release time	RB		0.770		1.660								
Removal time	RB		0.110		0.000								
Min Pulse	GB		0.646		1.870								
Min Pulse	RB		0.760		1.938								

[MEMO]

[MEMO]

## 2.11 D-F/F

[MEMO]

## Chapter 2 Function Block

Function	D-F/F																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power									L641	6																		
x1	F641	8	F641NQ	7	F641NB	7																						
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↗</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	Q	QB	0	↗	0	1	1	↗	1	0	X	↘	Hold	
D	C	Q	QB																									
0	↗	0	1																									
1	↗	1	0																									
X	↘	Hold																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>0</td> </tr> <tr> <td>1</td> <td>↗</td> <td>1</td> </tr> <tr> <td>X</td> <td>↘</td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	Q	0	↗	0	1	↗	1	X	↘	Hold				
D	C	Q																										
0	↗	0																										
1	↗	1																										
X	↘	Hold																										
Logic Diagram for "QB output"				Truth Table for "QB output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>1</td> </tr> <tr> <td>1</td> <td>↗</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	QB	0	↗	1	1	↗	0	X	↘	Hold				
D	C	QB																										
0	↗	1																										
1	↗	0																										
X	↘	Hold																										

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F641	C → Q	(HH)		0.358	0.551	0.994	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.401	0.652	1.211	0.010	0.013	0.017			QB	35
		(HL)		0.481	0.762	1.397	0.010	0.013	0.017				
		Set up time	D		0.570								
		Hold time	D		0.370								
		Min Pulse	C		0.669		1.924						
L641	C → Q	(HH)		0.358	0.551	0.992	0.022	0.030	0.042	D	1.0	Q	17
		(HL)		0.401	0.651	1.212	0.020	0.025	0.034			C	1.0
		Set up time	D		0.560		0.860						
		Hold time	D		0.350		0.140						
		Min Pulse	C		0.567		1.584						
F641NQ	C → Q	(HH)		0.358	0.550	0.993	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.400	0.650	1.211	0.010	0.013	0.017			C	1.0
		Set up time	D		0.570		1.100						
		Hold time	D		0.370		0.310						
	Min Pulse	C		0.566		1.584							
F641NB	C → QB	(HH)		0.329	0.529	0.989	0.011	0.015	0.022	D	1.0	QB	34
		(HL)		0.338	0.537	0.953	0.011	0.014	0.020			C	1.0
		Set up time	D		0.570		1.040						
		Hold time	D		0.370		0.310						
	Min Pulse	C		0.528		1.362							

Chapter 2 Function Block

Function	D-F/F with R																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F642	9	F642NQ	8	F642NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	C	R	Q	QB																																	
0	/	0	0	1																																	
1	/	0	1	0																																	
X	\	0	Hold																																		
X	X	1	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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D	C	R	QB																																		
0	/	0	1																																		
1	/	0	0																																		
X	\	0	Hold																																		
X	X	1	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F642	C → Q	(HH)		0.374	0.570	1.029	0.011	0.015	0.022	D	1.0	Q	35
				0.404	0.655	1.214	0.010	0.013	0.017	C	1.0	QB	34
				0.583	0.933	1.718	0.010	0.013	0.019				
	C → QB	(HH)		0.498	0.823	1.568	0.011	0.015	0.021	R	2.2		
				0.357	0.602	1.126	0.010	0.013	0.017				
				0.184	0.334	0.579	0.011	0.015	0.022				
	Set up time	D		0.610		1.720							
	Hold time	D		0.380		0.310							
	Release time	R		0.400		1.230							
	Removal time	R		0.410		0.290							
	Min Pulse	C		0.788		2.113							
	Min Pulse	R		0.585		1.597							
	F642NQ	C → Q	(HH)	0.373	0.570	1.029	0.011	0.015	0.022	D	1.0	Q	35
(HL)			0.401	0.652	1.213	0.010	0.013	0.017	C	1.0			
R → Q		(HL)	0.335	0.561	1.046	0.010	0.013	0.017	R	2.2			
Set up time		D		0.610		1.720							
Hold time		D		0.380		0.310							
Release time		R		0.400		1.230							
Removal time		R		0.410		0.290							
Min Pulse		C		0.578		1.586							
Min Pulse		R		0.529		1.491							
F642NB	C → QB	(HH)	0.331	0.532	0.993	0.011	0.015	0.022	D	1.0	QB	34	
		(HL)	0.361	0.576	1.039	0.011	0.015	0.022	C	1.0			
	R → QB	(HH)	0.264	0.434	0.817	0.011	0.015	0.022	R	2.2			
	Set up time	D		0.610		1.590							
	Hold time	D		0.390		0.310							
	Release time	R		0.410		1.120							
	Removal time	R		0.390		0.250							
Min Pulse	C		0.558		1.429								
Min Pulse	R		0.500		1.298								

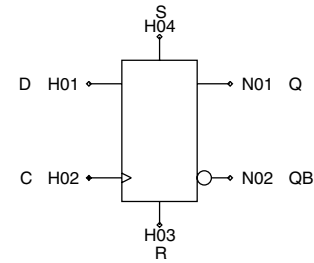
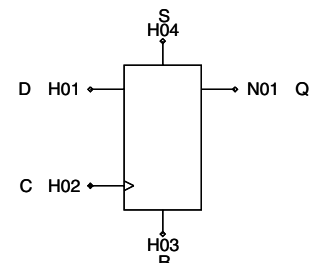
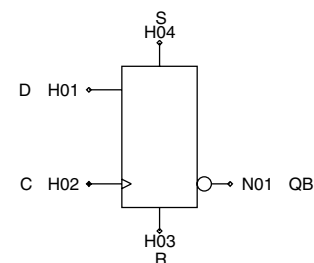
Chapter 2 Function Block

Function	D-F/F with S																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F643	9	F643NQ	8	F643NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	C	S	Q	QB																																	
0	/	0	0	1																																	
1	/	0	1	0																																	
X	\	0	Hold																																		
X	X	1	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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D	C	S	QB																																		
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1	/	0	0																																		
X	\	0	Hold																																		
X	X	1	0																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F643	C → Q	(HH)		0.365	0.562	1.011	0.011	0.015	0.021	D	1.0	Q	35
				0.486	0.794	1.476	0.010	0.013	0.019	C	1.0	QB	35
	C → QB	(HH)		0.596	0.989	1.890	0.011	0.015	0.021	S	2.2		
				0.498	0.788	1.435	0.010	0.013	0.017				
	S → Q	(HH)		0.177	0.259	0.438	0.011	0.015	0.022				
				0.317	0.580	1.040	0.010	0.013	0.018				
	Set up time	D		0.570		1.120							
	Hold time	D		0.360		0.300							
	Release time	S		0.110		0.000							
	Removal time	S		0.740		1.180							
	Min Pulse	C		0.763		2.265							
	Min Pulse	S		0.493		1.427							
	F643NQ	C → Q	(HH)		0.365	0.562	1.012	0.011	0.015	0.021	D	1.0	Q
				0.486	0.795	1.479	0.010	0.013	0.019	C	1.0		
S → Q		(HH)		0.178	0.260	0.441	0.011	0.015	0.022	S	2.2		
				0.570		1.130							
Set up time		D		0.570		1.130							
Hold time		D		0.360		0.300							
Release time		S		0.110		0.000							
Removal time		S		0.740		1.190							
Min Pulse		C		0.654		1.853							
Min Pulse		S		0.296		0.831							
F643NB	C → QB	(HH)		0.331	0.531	0.986	0.011	0.015	0.022	D	1.0	QB	34
				0.343	0.541	0.955	0.011	0.014	0.020	C	1.0		
	S → QB	(HL)		0.342	0.757	1.454	0.011	0.014	0.019	S	2.2		
				0.570		1.090							
	Set up time	D		0.570		1.090							
	Hold time	D		0.370		0.310							
	Release time	S		0.110		0.000							
Removal time	S		0.690		1.130								
Min Pulse	C		0.536		1.362								
Min Pulse	S		0.602		1.856								

Chapter 2 Function Block

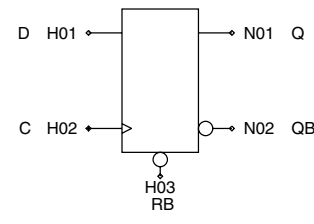
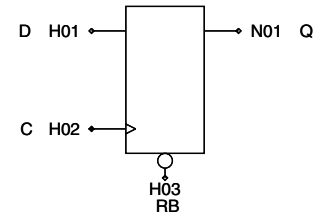
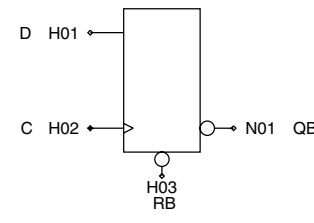
Function	D-F/F with R, S																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power									L644	8																																												
x1	F644	10	F644NQ	9	F644NB	9																																																
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D	C	R	S	Q	QB																																																	
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D	C	R	S	QB																																																		
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F644	C → Q	(HH)		0.383	0.587	1.057	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.482	0.787	1.467	0.010	0.013	0.019	C	1.0	QB	34
	C → QB	(HH)		0.577	0.966	1.860	0.011	0.015	0.021	R	2.1		
		(HL)		0.591	0.947	1.744	0.010	0.013	0.019	S	2.3		
	R → Q	(HL)		0.419	0.723	1.368	0.010	0.013	0.018				
	R → QB	(HH)		0.184	0.337	0.582	0.011	0.015	0.022				
	S → Q	(HH)		0.173	0.255	0.431	0.011	0.015	0.022				
	S → QB	(HL)		0.381	0.788	1.451	0.010	0.014	0.021				
	Set up time	D		0.600		1.710							
	Hold time	D		0.380		0.310							
	Release time	R		0.380		1.220							
	Release time	S		0.100		0.000							
	Removal time	R		0.430		0.320							
	Removal time	S		0.760		1.220							
	Min Pulse	C		0.794		2.232							
	Min Pulse	R		0.688		1.849							
	Min Pulse	S		0.628		1.826							
L644	C → Q	(HH)		0.383	0.587	1.052	0.022	0.030	0.042	D	1.0	Q	17
		(HL)		0.480	0.781	1.452	0.020	0.026	0.036	C	1.0		
	R → Q	(HL)		0.403	0.662	1.239	0.020	0.026	0.036	R	2.1		
	S → Q	(HH)		0.174	0.260	0.440	0.021	0.030	0.042	S	2.3		
	Set up time	D		0.590		1.690							
	Hold time	D		0.380		0.310							
	Release time	R		0.380		1.200							
	Release time	S		0.100		0.000							
	Removal time	R		0.430		0.320							
	Removal time	S		0.760		1.220							
	Min Pulse	C		0.647		1.826							
	Min Pulse	R		0.607		1.687							
	Min Pulse	S		0.272		0.789							
F644NQ	C → Q	(HH)		0.382	0.586	1.055	0.011	0.015	0.022	D	1.0	Q	35
		(HL)		0.482	0.789	1.472	0.010	0.013	0.019	C	1.0		
	R → Q	(HL)		0.406	0.671	1.265	0.010	0.013	0.019	R	2.1		
	S → Q	(HH)		0.173	0.254	0.430	0.011	0.015	0.022	S	2.3		
	Set up time	D		0.590		1.710							
	Hold time	D		0.380		0.320							
Release time	R		0.380		1.220								
Release time	S		0.110		0.000								
Removal time	R		0.430		0.320								
Removal time	S		0.760		1.220								
Min Pulse	C		0.650		1.845								
Min Pulse	R		0.612		1.711								
Min Pulse	S		0.284		0.812								
F644NB	C → QB	(HH)		0.335	0.536	0.993	0.011	0.015	0.022	D	1.0	QB	33
		(HL)		0.368	0.587	1.060	0.011	0.015	0.022	C	1.0		
	R → QB	(HH)		0.266	0.432	0.808	0.011	0.015	0.022	R	2.1		
	S → QB	(HL)		0.453	0.955	1.858	0.011	0.015	0.022	S	2.3		
	Set up time	D		0.600		1.590							
	Hold time	D		0.390		0.320							
	Release time	R		0.390		1.100							
	Release time	S		0.100		0.000							
	Removal time	R		0.420		0.300							
	Removal time	S		0.700		1.150							
Min Pulse	C		0.567		1.451								
Min Pulse	R		0.500		1.286								
Min Pulse	S		0.724		2.250								



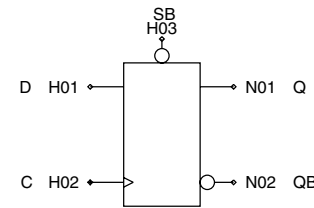
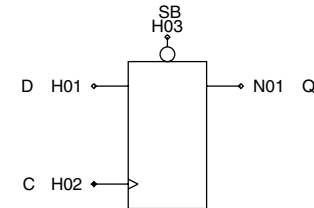
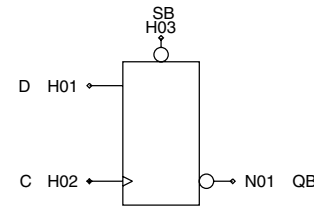
Chapter 2 Function Block

Function	D-F/F with RB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power							L645	7																													
x1	F615	9	F615NQ	8	F615NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	C	RB	Q	QB																																	
0	/	1	0	1																																	
1	/	1	1	0																																	
X	\	1	Hold																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>/</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>/</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>\</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	RB	Q	0	/	1	0	1	/	1	1	X	\	1	Hold	X	X	0	0					
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0	/	1	0																																		
1	/	1	1																																		
X	\	1	Hold																																		
X	X	0	0																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	C	RB	QB																																		
0	/	1	1																																		
1	/	1	0																																		
X	\	1	Hold																																		
X	X	0	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F615	C → Q	(HH)		0.425	0.675	1.282	0.012	0.016	0.023	D	1.0	Q	31
				0.424	0.688	1.278	0.010	0.013	0.017				
				0.559	0.905	1.728	0.010	0.013	0.017				
	C → QB	(HH)		0.523	0.860	1.624	0.012	0.016	0.022	C	1.0	QB	31
				0.199	0.311	0.535	0.010	0.013	0.017				
	RB → Q	(LL)		0.199	0.311	0.535	0.010	0.013	0.017	RB	2.2		
				0.305	0.567	1.029	0.012	0.016	0.022				
	Set up time	D		0.580		1.140							
	Hold time	D		0.380		0.310							
	Release time	RB		0.190		0.000							
	Removal time	RB		0.670		1.010							
	Min Pulse	C		0.751		2.111							
	Min Pulse	RB		0.547		1.338							
L645	C → Q	(HH)		0.404	0.638	1.202	0.022	0.030	0.043	D	1.0	Q	16
				0.406	0.656	1.218	0.020	0.025	0.034				
	RB → Q	(LL)		0.183	0.285	0.480	0.020	0.025	0.034	C	1.0	QB	16
				0.199	0.315	0.540	0.010	0.013	0.017				
	Set up time	D		0.580		1.130							
	Hold time	D		0.380		0.310							
	Release time	RB		0.190		0.000							
	Removal time	RB		0.670		1.010							
	Min Pulse	C		0.596		1.594							
	Min Pulse	RB		0.358		0.760							
F615NQ	C → Q	(HH)		0.427	0.678	1.290	0.012	0.016	0.023	D	1.0	Q	31
				0.425	0.689	1.282	0.010	0.013	0.017				
	RB → Q	(LL)		0.199	0.315	0.540	0.010	0.013	0.017	C	1.0	QB	31
				0.580		1.140							
	Set up time	D		0.580		1.140							
	Hold time	D		0.380		0.310							
	Release time	RB		0.190		0.000							
Removal time	RB		0.670		1.010								
Min Pulse	C		0.619		1.671								
Min Pulse	RB		0.386		0.841								
F615NB	C → QB	(HH)		0.353	0.567	1.055	0.012	0.016	0.023	D	1.0	QB	31
				0.359	0.570	1.012	0.011	0.014	0.020				
	RB → QB	(LH)		0.327	0.750	1.447	0.012	0.016	0.023	C	1.0	QB	31
				0.580		1.120							
	Set up time	D		0.580		1.120							
	Hold time	D		0.380		0.310							
	Release time	RB		0.170		0.000							
	Removal time	RB		0.630		0.960							
	Min Pulse	C		0.552		1.432							
Min Pulse	RB		0.628		1.747								

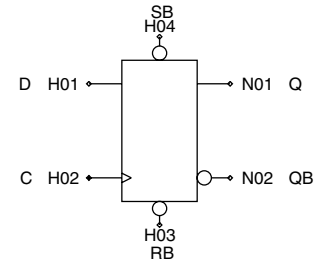
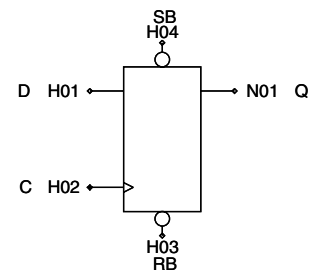
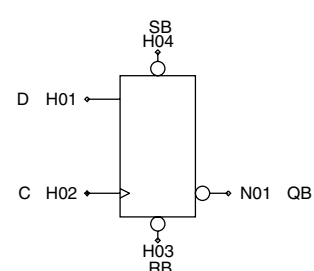
## Chapter 2 Function Block

Function	D-F/F with SB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F616	9	F616NQ	8	F616NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	C	SB	Q	QB																																	
0	/	1	0	1																																	
1	/	1	1	0																																	
X	\	1	Hold																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	C	SB	QB																																		
0	/	1	1																																		
1	/	1	0																																		
X	\	1	Hold																																		
X	X	0	0																																		

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F616	C → Q	(HH)		0.360	0.553	0.996	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.422	0.686	1.294	0.010	0.013	0.017	C	1.0	QB	34
	C → QB	(HH)		0.575	0.968	1.923	0.011	0.015	0.021	SB	2.2		
		(HL)		0.489	0.774	1.411	0.010	0.013	0.017				
	SB → Q	(LH)		0.335	0.619	1.170	0.011	0.015	0.021				
	SB → QB	(LL)		0.190	0.386	0.660	0.010	0.013	0.018				
	Set up time	D		0.590		1.200							
	Hold time	D		0.350		0.290							
	Release time	SB		0.450		0.560							
	Removal time	SB		0.360		0.370							
	Min Pulse	C		0.740		2.295							
	Min Pulse	SB		0.579		1.505							
F616NQ	C → Q	(HH)		0.360	0.554	0.998	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.420	0.684	1.291	0.010	0.013	0.017	C	1.0	QB	34
	SB → Q	(LH)		0.313	0.564	1.057	0.011	0.015	0.021	SB	2.2		
	Set up time	D		0.590		1.210							
	Hold time	D		0.350		0.280							
	Release time	SB		0.450		0.570							
	Removal time	SB		0.360		0.370							
	Min Pulse	C		0.588		1.667							
	Min Pulse	SB		0.541		1.381							
	F616NB	C → QB	(HH)		0.366	0.592	1.121	0.011	0.016	0.023	D	1.0	QB
		(HL)		0.340	0.541	0.960	0.011	0.014	0.020	C	1.0		
SB → QB		(LL)		0.279	0.507	0.938	0.010	0.014	0.019	SB	2.2		
Set up time		D		0.610		1.230							
Hold time		D		0.350		0.290							
Release time		SB		0.460		0.590							
Removal time	SB		0.340		0.330								
Min Pulse	C		0.533		1.495								
Min Pulse	SB		0.524		1.276								

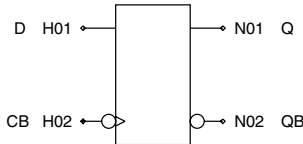
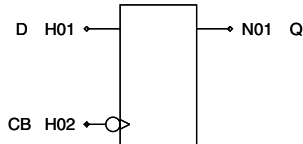
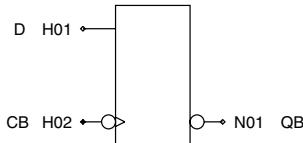
Chapter 2 Function Block

Function	D-F/F with RB, SB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power									L647	8																																												
x1	F647	10	F647NQ	9	F647NB	9																																																
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Logic Diagram for "Normal"			Truth Table for "Normal"																																																			
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D	C	RB	SB	Q	QB																																																	
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Logic Diagram for "Q output"			Truth Table for "Q output"																																																			
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D	C	RB	SB	QB																																																		
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1	/	1	1	0																																																		
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X	X	1	0	0																																																		
X	X	0	0	0																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F647	C → Q	(HH)		0.412	0.653	1.237	0.011	0.015	0.022	D	1.0	Q	34	
		(HL)		0.427	0.694	1.302	0.010	0.013	0.017	C	1.0	QB	32	
	C → QB	(HH)		0.575	0.968	1.920	0.011	0.015	0.021	RB	2.3			
		(HL)		0.540	0.874	1.662	0.010	0.013	0.017	SB	2.1			
	RB → Q	(LL)		0.176	0.273	0.463	0.010	0.013	0.017					
	RB → QB	(LH)		0.329	0.677	1.334	0.011	0.015	0.022					
	SB → Q	(LH)		0.382	0.727	1.423	0.011	0.015	0.022					
	SB → QB	(LL)		0.187	0.385	0.654	0.010	0.013	0.018					
	Set up time	D		0.570		1.160								
	Hold time	D		0.360		0.300								
	Release time	RB		0.180		0.000								
	Release time	SB		0.420		0.510								
	Removal time	RB		0.690		1.080								
	Removal time	SB		0.390		0.440								
	Min Pulse	C		0.743		2.296								
	Min Pulse	RB		0.603		1.640								
Min Pulse	SB		0.658		1.769									
L647	C → Q	(HH)		0.413	0.652	1.223	0.022	0.030	0.043	D	1.0	Q	16	
		(HL)		0.427	0.693	1.299	0.020	0.025	0.034	C	1.0			
	RB → Q	(LL)		0.183	0.284	0.477	0.020	0.025	0.034	RB	2.3			
	SB → Q	(LH)		0.359	0.654	1.267	0.022	0.030	0.042	SB	2.2			
	Set up time	D		0.580		1.180								
	Hold time	D		0.360		0.290								
	Release time	RB		0.180		0.000								
	Release time	SB		0.420		0.530								
	Removal time	RB		0.700		1.090								
	Removal time	SB		0.390		0.440								
	Min Pulse	C		0.596		1.677								
	Min Pulse	RB		0.357		0.754								
	Min Pulse	SB		0.608		1.600								
	F647NQ	C → Q	(HH)		0.409	0.651	1.236	0.011	0.015	0.022	D	1.0	Q	34
			(HL)		0.422	0.687	1.295	0.010	0.013	0.017	C	1.0		
		RB → Q	(LL)		0.178	0.276	0.467	0.010	0.013	0.017	RB	2.3		
SB → Q		(LH)		0.358	0.654	1.285	0.011	0.015	0.022	SB	2.2			
Set up time		D		0.580		1.170								
Hold time		D		0.360		0.290								
Release time		RB		0.180		0.000								
Release time		SB		0.420		0.530								
Removal time		RB		0.700		1.090								
Removal time		SB		0.390		0.440								
Min Pulse		C		0.591		1.673								
Min Pulse		RB		0.354		0.757								
Min Pulse		SB		0.608		1.618								
F647NB		C → QB	(HH)		0.373	0.601	1.135	0.011	0.016	0.023	D	1.0	QB	32
			(HL)		0.342	0.543	0.958	0.011	0.014	0.020	C	1.0		
		RB → QB	(LH)		0.374	0.889	1.808	0.011	0.016	0.023	RB	2.3		
	SB → QB	(LL)		0.274	0.499	0.920	0.011	0.014	0.020	SB	2.2			
	Set up time	D		0.590		1.210								
	Hold time	D		0.360		0.290								
	Release time	RB		0.150		0.000								
	Release time	SB		0.440		0.560								
	Removal time	RB		0.650		1.010								
	Removal time	SB		0.380		0.400								
	Min Pulse	C		0.541		1.510								
	Min Pulse	RB		0.713		2.114								
	Min Pulse	SB		0.520		1.254								

## Chapter 2 Function Block

Function	D-F/F (CB)																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power									L661	6																		
x1	F661	8	F661NQ	7	F661NB	7																						
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↘</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↘</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↗</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	Q	QB	0	↘	0	1	1	↘	1	0	X	↗	Hold	
D	CB	Q	QB																									
0	↘	0	1																									
1	↘	1	0																									
X	↗	Hold																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↘</td> <td>0</td> </tr> <tr> <td>1</td> <td>↘</td> <td>1</td> </tr> <tr> <td>X</td> <td>↗</td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	Q	0	↘	0	1	↘	1	X	↗	Hold				
D	CB	Q																										
0	↘	0																										
1	↘	1																										
X	↗	Hold																										
Logic Diagram for "QB output"				Truth Table for "QB output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↘</td> <td>1</td> </tr> <tr> <td>1</td> <td>↘</td> <td>0</td> </tr> <tr> <td>X</td> <td>↗</td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	QB	0	↘	1	1	↘	0	X	↗	Hold				
D	CB	QB																										
0	↘	1																										
1	↘	0																										
X	↗	Hold																										

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F661	CB → Q	(LH)		0.376	0.629	1.199	0.011	0.015	0.021	D	1.0	Q	35
		(LL)		0.354	0.579	1.085	0.010	0.013	0.017				
		(LH)		0.447	0.745	1.434	0.011	0.015	0.021	CB	1.0	QB	35
	(LL)		0.502	0.844	1.610	0.010	0.013	0.017					
	Set up time	D			0.560								
Hold time	D			0.370									
Min Pulse	CB			0.706		1.933							
L661	CB → Q	(LH)		0.374	0.628	1.195	0.022	0.030	0.042	D	1.0	Q	17
		(LL)		0.353	0.580	1.087	0.020	0.025	0.034				
	Set up time	D			0.570								
	Hold time	D			0.370								
Min Pulse	CB			0.579		1.518							
F661NQ	CB → Q	(LH)		0.375	0.628	1.197	0.011	0.015	0.021	D	1.0	Q	35
		(LL)		0.353	0.580	1.087	0.010	0.013	0.017				
	Set up time	D			0.560								
	Hold time	D			0.370								
Min Pulse	CB			0.580		1.521							
F661NB	CB → QB	(LH)		0.293	0.480	0.909	0.011	0.016	0.022	D	1.0	QB	34
		(LL)		0.335	0.561	1.069	0.011	0.014	0.020				
	Set up time	D			0.570								
	Hold time	D			0.370								
Min Pulse	CB			0.549		1.399							

Chapter 2 Function Block

Function	D-F/F (CB) with RB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F665	9	F665NQ	8	F665NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	RB	Q	QB	0	\	1	0	1	1	\	1	1	0	X	/	1	Hold		X	X	0	0	1
D	CB	RB	Q	QB																																	
0	\	1	0	1																																	
1	\	1	1	0																																	
X	/	1	Hold																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	RB	Q	0	\	1	0	1	\	1	1	X	/	1	Hold	X	X	0	0					
D	CB	RB	Q																																		
0	\	1	0																																		
1	\	1	1																																		
X	/	1	Hold																																		
X	X	0	0																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>RB</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	RB	QB	0	\	1	1	1	\	1	0	X	/	1	Hold	X	X	0	1					
D	CB	RB	QB																																		
0	\	1	1																																		
1	\	1	0																																		
X	/	1	Hold																																		
X	X	0	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F665	CB → Q	(LH)		0.447	0.759	1.496	0.012	0.016	0.023	D	1.0	Q	31
		(LL)		0.376	0.616	1.154	0.010	0.013	0.017				
	CB → QB	(LH)		0.476	0.789	1.504	0.012	0.016	0.022	CB	1.0	QB	31
		(LL)		0.582	0.988	1.942	0.010	0.013	0.017				
	RB → Q	(LL)		0.199	0.310	0.533	0.010	0.013	0.017	RB	2.2		
		(LH)		0.304	0.566	1.026	0.012	0.016	0.022				
	Set up time	D		0.570		1.020							
	Hold time	D		0.360		0.370							
	Release time	RB		0.180		0.000							
	Removal time	RB		0.670		1.140							
	Min Pulse	CB		0.789		2.264							
	Min Pulse	RB		0.546		1.335							
	F665NQ	CB → Q	(LH)		0.449	0.761	1.501	0.012	0.016	0.023	D	1.0	Q
(LL)				0.377	0.618	1.160	0.010	0.013	0.017				
RB → Q		(LL)		0.199	0.313	0.537	0.010	0.013	0.017	CB	1.0	RB	2.3
		(LH)		0.325	0.574	1.010	0.012	0.016	0.023				
Set up time		D		0.570		1.020							
Hold time		D		0.360		0.370							
Release time		RB		0.180		0.000							
Removal time		RB		0.670		1.140							
Min Pulse		CB		0.656		1.824							
Min Pulse		RB		0.384		0.837							
F665NB	CB → QB	(LH)		0.317	0.518	0.975	0.012	0.016	0.023	D	1.0	QB	31
		(LL)		0.358	0.601	1.143	0.011	0.014	0.020				
	RB → QB	(LH)		0.325	0.754	1.454	0.012	0.016	0.023	CB	1.0	RB	2.3
		(LL)		0.580	0.975	1.010	0.012	0.016	0.023				
	Set up time	D		0.580		1.010							
	Hold time	D		0.370		0.390							
	Release time	RB		0.170		0.000							
	Removal time	RB		0.630		1.070							
Min Pulse	CB		0.575		1.474								
Min Pulse	RB		0.633		1.754								

Chapter 2 Function Block

Function	D-F/F (CB) with SB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F666	9	F666NQ	8	F666NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	SB	Q	QB	0	\	1	0	1	1	\	1	1	0	X	/	1	Hold		X	X	0	1	0
D	CB	SB	Q	QB																																	
0	\	1	0	1																																	
1	\	1	1	0																																	
X	/	1	Hold																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>SB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	SB	Q	0	\	1	0	1	\	1	1	X	/	1	Hold	X	X	0	1					
D	CB	SB	Q																																		
0	\	1	0																																		
1	\	1	1																																		
X	/	1	Hold																																		
X	X	0	1																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	CB	SB	QB																																		
0	\	1	1																																		
1	\	1	0																																		
X	/	1	Hold																																		
X	X	0	0																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F666	CB → Q	(LH)		0.374	0.624	1.189	0.011	0.015	0.021	D	1.0	Q	35	
				0.366	0.605	1.145	0.010	0.013	0.017	CB	1.0	QB	34	
	CB → QB	(LH)		0.518	0.885	1.774	0.011	0.015	0.021					
				0.501	0.841	1.598	0.010	0.013	0.017					
	SB → Q	(LH)		0.334	0.659	1.230	0.011	0.015	0.021					
				0.212	0.423	0.712	0.010	0.013	0.018					
	Set up time	D		0.610		1.310								
	Hold time	D		0.380		0.390								
	Release time	SB		0.420		0.730								
	Removal time	SB		0.400		0.430								
	Min Pulse	CB		0.724		2.107								
	Min Pulse	SB		0.671		1.574								
F666NQ	CB → Q	(LH)		0.373	0.623	1.187	0.011	0.015	0.021	D	1.0	Q	35	
				0.366	0.604	1.147	0.010	0.013	0.017	CB	1.0			
	SB → Q	(LH)		0.312	0.558	1.048	0.011	0.015	0.021	SB	2.2			
	Set up time	D		0.610		1.310								
	Hold time	D		0.380		0.390								
	Release time	SB		0.420		0.730								
	Removal time	SB		0.400		0.430								
	Min Pulse	CB		0.574		1.509								
	Min Pulse	SB		0.536		1.372								
	F666NB	CB → QB	(LH)		0.323	0.532	1.022	0.011	0.016	0.023	D	1.0	QB	32
					0.333	0.558	1.061	0.011	0.014	0.020	CB	1.0		
SB → QB		(LL)		0.279	0.502	0.929	0.010	0.014	0.019	SB	2.2			
Set up time		D		0.620		1.300								
Hold time		D		0.390		0.390								
Release time		SB		0.430		0.710								
Removal time		SB		0.380		0.410								
Min Pulse		CB		0.545		1.391								
Min Pulse		SB		0.520		1.267								

Chapter 2 Function Block

Function	D-F/F (CB) with RB, SB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power								L667	8																																													
x1	F667	10	F667NQ	9	F667NB	9																																																
x2																																																						
x4																																																						
Logic Diagram for "Normal"			Truth Table for "Normal"																																																			
			<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>										D	CB	RB	SB	Q	QB	0	\	1	1	0	1	1	\	1	1	1	0	X	/	1	1	Hold		X	X	0	1	0	1	X	X	1	0	1	0	X	X	0	0	0	0
D	CB	RB	SB	Q	QB																																																	
0	\	1	1	0	1																																																	
1	\	1	1	1	0																																																	
X	/	1	1	Hold																																																		
X	X	0	1	0	1																																																	
X	X	1	0	1	0																																																	
X	X	0	0	0	0																																																	
Logic Diagram for "Q output"			Truth Table for "Q output"																																																			
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F667	CB → Q	(LH)		0.426	0.723	1.429	0.011	0.015	0.022	D	1.0	Q	34
		(LL)		0.375	0.615	1.160	0.010	0.013	0.017	CB	1.0	QB	32
		(LH)		0.524	0.890	1.782	0.011	0.015	0.021	RB	2.3		
	CB → QB	(LL)		0.553	0.943	1.855	0.010	0.013	0.017	SB	2.2		
		(LL)		0.178	0.275	0.466	0.010	0.013	0.017				
		(LH)		0.331	0.680	1.338	0.011	0.015	0.022				
	RB → Q	(LL)		0.178	0.275	0.466	0.010	0.013	0.017				
		(LH)		0.331	0.680	1.338	0.011	0.015	0.022				
	SB → Q	(LH)		0.385	0.724	1.421	0.011	0.015	0.022				
		(LL)		0.187	0.384	0.655	0.010	0.013	0.018				
	Set up time	D		0.600		1.300							
	Hold time	D		0.370		0.380							
	Release time	RB		0.170		0.000							
	Release time	SB		0.400		0.730							
	Removal time	RB		0.690		1.220							
Removal time	SB		0.420		0.480								
Min Pulse	CB		0.755		2.176								
Min Pulse	RB		0.613		1.646								
Min Pulse	SB		0.656		1.768								
L667	CB → Q	(LH)		0.427	0.721	1.412	0.022	0.030	0.043	D	1.0	Q	16
		(LL)		0.377	0.619	1.165	0.020	0.025	0.034	CB	1.0		
		(LH)		0.182	0.282	0.476	0.020	0.025	0.034	RB	2.3		
	RB → Q	(LL)		0.359	0.651	1.264	0.022	0.030	0.042	SB	2.1		
		(LL)		0.600		1.310							
		(LH)		0.370		0.380							
	Set up time	D		0.600		1.310							
	Hold time	D		0.370		0.380							
	Release time	RB		0.170		0.000							
	Release time	SB		0.400		0.720							
	Removal time	RB		0.690		1.220							
	Removal time	SB		0.420		0.480							
	Min Pulse	CB		0.629		1.733							
	Min Pulse	RB		0.356		0.752							
	Min Pulse	SB		0.607		1.598							
F667NQ	CB → Q	(LH)		0.425	0.722	1.428	0.011	0.015	0.022	D	1.0	Q	34
		(LL)		0.374	0.614	1.161	0.010	0.013	0.017	CB	1.0		
		(LH)		0.178	0.276	0.466	0.010	0.013	0.017	RB	2.3		
	RB → Q	(LH)		0.358	0.654	1.286	0.011	0.015	0.022	SB	2.2		
		(LL)		0.600		1.320							
		(LH)		0.370		0.380							
Set up time	D		0.600		1.320								
Hold time	D		0.370		0.380								
Release time	RB		0.170		0.000								
Release time	SB		0.400		0.730								
Removal time	RB		0.690		1.220								
Removal time	SB		0.420		0.480								
Min Pulse	CB		0.627		1.751								
Min Pulse	RB		0.354		0.757								
Min Pulse	SB		0.608		1.618								
F667NB	CB → QB	(LH)		0.330	0.542	1.037	0.011	0.016	0.023	D	1.0	QB	32
		(LL)		0.335	0.560	1.059	0.011	0.014	0.020	CB	1.0		
		(LH)		0.373	0.888	1.807	0.011	0.016	0.023	RB	2.3		
	RB → QB	(LL)		0.275	0.498	0.919	0.011	0.014	0.020	SB	2.2		
		(LL)		0.610		1.310							
		(LH)		0.380		0.400							
Set up time	D		0.610		1.310								
Hold time	D		0.380		0.400								
Release time	RB		0.160		0.000								
Release time	SB		0.410		0.700								
Removal time	RB		0.640		1.120								
Removal time	SB		0.410		0.460								
Min Pulse	CB		0.547		1.389								
Min Pulse	RB		0.713		2.112								
Min Pulse	SB		0.520		1.253								

Chapter 2 Function Block

Function	D-F/F with 2 to 1 Selector																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F641S	10	F641SQ	9	F641SB	9																																																
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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D0	D1	C	A	Q	QB																																																	
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D0	D1	C	A	QB																																																		
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X	X	\	0	Hold																																																		
X	X	\	1	Hold																																																		

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t Ld0 (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F641S	C → Q	(HH)		0.363	0.555	1.000	0.011	0.015	0.021	D0	1.0	Q	35	
		(HL)		0.410	0.663	1.226	0.010	0.013	0.017	D1	1.0	QB	35	
	C → QB	(HH)		0.502	0.828	1.572	0.011	0.015	0.021	C	1.0			
		(HL)		0.489	0.771	1.409	0.010	0.013	0.017	A	1.0			
	Set up time	D0		0.680		1.500								
	Set up time	D1		0.680		1.500								
	Set up time	A		0.680		1.660								
	Hold time	D0		0.270		0.000								
	Hold time	D1		0.270		0.000								
	Hold time	A		0.250		0.000								
	Min Pulse	C		0.684		1.951								
F641SQ	C → Q	(HH)		0.363	0.556	1.001	0.011	0.015	0.021	D0	1.0	Q	35	
		(HL)		0.409	0.663	1.227	0.010	0.013	0.017	D1	1.0	QB	35	
	Set up time	D0		0.680		1.500				C	1.0			
	Set up time	D1		0.680		1.500				A	1.0			
	Set up time	A		0.680		1.650								
	Hold time	D0		0.270		0.000								
	Hold time	D1		0.270		0.000								
	Hold time	A		0.250		0.000								
	Min Pulse	C		0.583		1.607								
	F641SB	C → QB	(HH)		0.339	0.542	1.005	0.011	0.015	0.022	D0	1.0	QB	34
			(HL)		0.346	0.545	0.960	0.011	0.014	0.020	D1	1.0		
Set up time		D0		0.680		1.470				C	1.0			
Set up time		D1		0.680		1.470				A	1.0			
Set up time		A		0.680		1.630								
Hold time		D0		0.270		0.010								
Hold time		D1		0.280		0.010								
Hold time		A		0.260		0.000								
Min Pulse		C		0.544		1.385								



Chapter 2 Function Block

Function	D-F/F with R, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F642S	11	F642SQ	10	F642SB	10																																																														
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F642S	C → Q	(HH)		0.377	0.574	1.034	0.011	0.015	0.022	D0	1.0	Q	35
		(HL)		0.408	0.659	1.222	0.010	0.013	0.017	D1	1.0	QB	34
	C → QB	(HH)		0.498	0.824	1.571	0.011	0.015	0.021	C	1.0		
		(HL)		0.580	0.928	1.711	0.010	0.013	0.019	R	2.2		
	R → Q	(HL)		0.361	0.604	1.129	0.010	0.013	0.017	A	1.0		
	R → QB	(HH)		0.180	0.329	0.573	0.011	0.015	0.022				
	Set up time		D0	0.730		2.140							
	Set up time		D1	0.730		2.130							
	Set up time		A	0.730		2.290							
	Hold time		D0	0.280		0.000							
	Hold time		D1	0.280		0.010							
	Hold time		A	0.260		0.000							
	Release time		R	0.410		1.240							
	Removal time		R	0.400		0.270							
	Min Pulse		C	0.795		2.107							
	Min Pulse		R	0.582		1.596							
	F642SQ	C → Q	(HH)		0.372	0.570	1.029	0.011	0.015	0.022	D0	1.0	Q
		(HL)		0.401	0.653	1.214	0.010	0.013	0.017	D1	1.0		
R → Q		(HL)		0.337	0.564	1.050	0.010	0.013	0.017	C	1.0		
Set up time			D0	0.740		2.150				R	2.2		
Set up time			D1	0.740		2.140				A	1.0		
Set up time			A	0.740		2.300							
Hold time			D0	0.270		0.000							
Hold time			D1	0.280		0.000							
Hold time			A	0.260		0.000							
Release time			R	0.410		1.250							
Removal time			R	0.400		0.270							
Min Pulse			C	0.577		1.585							
Min Pulse			R	0.533		1.495							
F642SB	C → QB	(HH)		0.329	0.528	0.987	0.011	0.015	0.022	D0	1.0	QB	34
		(HL)		0.358	0.572	1.034	0.011	0.015	0.022	D1	1.0		
	R → QB	(HH)		0.262	0.434	0.817	0.011	0.015	0.022	C	1.0		
	Set up time		D0	0.750		2.020				R	2.2		
	Set up time		D1	0.740		2.000				A	1.0		
	Set up time		A	0.740		2.160							
	Hold time		D0	0.280		0.000							
	Hold time		D1	0.290		0.000							
	Hold time		A	0.270		0.000							
	Release time		R	0.420		1.110							
	Removal time		R	0.390		0.240							
	Min Pulse		C	0.564		1.426							
	Min Pulse		R	0.500		1.298							

Chapter 2 Function Block

Function	D-F/F with S, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F643S	11	F643SQ	10	F643SB	10																																																														
x2																																																																				
x4																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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D0	D1	C	S	A	Q	QB																																																														
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X	1	/	0	1	1	0																																																														
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X	X	X	1	X	0																																																															
				X:Irrelevant																																																																

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F643S	C → Q	(HH)		0.369	0.566	1.017	0.011	0.015	0.021	D0	1.0	Q	35	
			(HL)	0.494	0.803	1.490	0.010	0.013	0.019	D1	1.0	QB	35	
	C → QB	(HH)		0.604	0.999	1.904	0.011	0.015	0.021	C	1.0			
			(HL)	0.502	0.792	1.440	0.010	0.013	0.017	S	2.2			
	S → Q	(HH)		0.178	0.260	0.439	0.011	0.015	0.022	A	1.0			
			(HL)	0.318	0.580	1.042	0.010	0.013	0.018					
	Set up time	D0		0.680		1.540								
	Set up time	D1		0.690		1.540								
	Set up time	A		0.690		1.700								
	Hold time	D0		0.260		0.000								
	Hold time	D1		0.260		0.000								
	Hold time	A		0.240		0.000								
	Release time	S		0.110		0.000								
	Removal time	S		0.730		1.190								
	Min Pulse	C		0.778		2.283								
	Min Pulse	S		0.496		1.429								
F643SQ	C → Q	(HH)		0.369	0.566	1.018	0.011	0.015	0.021	D0	1.0	Q	35	
			(HL)	0.493	0.803	1.492	0.010	0.013	0.019	D1	1.0			
	S → Q	(HH)		0.178	0.260	0.440	0.011	0.015	0.022	C	1.0			
			(HL)	0.318	0.580	1.042	0.010	0.013	0.018	S	2.2			
	Set up time	D0		0.680		1.540								
	Set up time	D1		0.690		1.540								
	Set up time	A		0.690		1.700								
	Hold time	D0		0.260		0.000								
	Hold time	D1		0.260		0.000								
	Hold time	A		0.240		0.000								
	Release time	S		0.110		0.000								
	Removal time	S		0.730		1.190								
	Min Pulse	C		0.668		1.870								
	Min Pulse	S		0.295		0.830								
	F643SB	C → QB	(HH)		0.340	0.542	1.000	0.011	0.015	0.022	D0	1.0	QB	34
				(HL)	0.350	0.548	0.961	0.011	0.014	0.020	D1	1.0		
S → QB		(HL)		0.343	0.757	1.454	0.011	0.014	0.019	C	1.0			
			(HL)	0.343	0.757	1.454	0.011	0.014	0.019	S	2.2			
Set up time		D0		0.690		1.530								
Set up time		D1		0.690		1.520								
Set up time		A		0.690		1.680								
Hold time		D0		0.260		0.000								
Hold time		D1		0.260		0.010								
Hold time		A		0.240		0.000								
Release time		S		0.110		0.000								
Removal time		S		0.690		1.130								
Min Pulse		C		0.548		1.380								
Min Pulse		S		0.602		1.855								

Chapter 2 Function Block

Function	D-F/F with R, S, 2 to 1 Selector																																																																																											
Block type	Standard type						Low Gate type																																																																																					
	Normal		Q output		QB output		Normal		Q output		QB output																																																																																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																
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D0	D1	C	R	S	A	Q	QB																																																																																					
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F644S	C → Q	(HH)		0.379	0.581	1.047	0.011	0.015	0.022	D0	1.0	Q	35
		(HL)		0.478	0.781	1.458	0.010	0.013	0.019	D1	1.0	QB	34
	C → QB	(HH)		0.574	0.962	1.854	0.011	0.015	0.021	C	1.0		
		(HL)		0.588	0.942	1.735	0.010	0.013	0.019	R	2.1		
	R → Q	(HL)		0.415	0.720	1.361	0.010	0.013	0.018	S	2.3		
	R → QB	(HH)		0.185	0.337	0.584	0.011	0.015	0.022	A	1.0		
	S → Q	(HH)		0.173	0.254	0.429	0.011	0.015	0.022				
	S → QB	(HL)		0.380	0.782	1.443	0.010	0.014	0.021				
	Set up time	D0		0.730		2.120							
	Set up time	D1		0.730		2.130							
	Set up time	A		0.720		2.270							
	Hold time	D0		0.270		0.000							
	Hold time	D1		0.270		0.000							
	Hold time	A		0.260		0.000							
	Release time	R		0.380		1.210							
	Release time	S		0.110		0.000							
	Removal time	R		0.430		0.320							
	Removal time	S		0.750		1.210							
	Min Pulse	C		0.791		2.225							
	Min Pulse	R		0.690		1.845							
Min Pulse	S		0.622		1.817								
F644SQ	C → Q	(HH)		0.379	0.581	1.048	0.011	0.015	0.022	D0	1.0	Q	35
		(HL)		0.479	0.783	1.464	0.010	0.013	0.019	D1	1.0		
	R → Q	(HL)		0.404	0.667	1.260	0.010	0.013	0.019	C	1.0		
	S → Q	(HH)		0.173	0.254	0.430	0.011	0.015	0.022	R	2.1		
	Set up time	D0		0.730		2.130				S	2.3		
	Set up time	D1		0.730		2.130				A	1.0		
	Set up time	A		0.720		2.280							
	Hold time	D0		0.270		0.000							
	Hold time	D1		0.270		0.000							
	Hold time	A		0.260		0.000							
	Release time	R		0.380		1.220							
	Release time	S		0.110		0.000							
	Removal time	R		0.430		0.320							
Removal time	S		0.750		1.210								
Min Pulse	C		0.645		1.836								
Min Pulse	R		0.606		1.702								
Min Pulse	S		0.284		0.811								
F644SB	C → QB	(HH)		0.330	0.530	0.984	0.011	0.015	0.022	D0	1.0	QB	33
		(HL)		0.363	0.579	1.048	0.011	0.015	0.022	D1	1.0		
	R → QB	(HH)		0.264	0.427	0.801	0.011	0.015	0.022	C	1.0		
	S → QB	(HL)		0.449	0.949	1.850	0.011	0.015	0.022	R	2.1		
	Set up time	D0		0.730		2.010				S	2.3		
	Set up time	D1		0.740		2.020				A	1.0		
	Set up time	A		0.730		2.170							
	Hold time	D0		0.280		0.000							
	Hold time	D1		0.280		0.000							
	Hold time	A		0.260		0.000							
	Release time	R		0.400		1.110							
	Release time	S		0.110		0.000							
	Removal time	R		0.420		0.290							
Removal time	S		0.690		1.140								
Min Pulse	C		0.562		1.439								
Min Pulse	R		0.492		1.277								
Min Pulse	S		0.721		2.241								

Chapter 2 Function Block

Function	D-F/F with RB, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F615S	11	F615SQ	10	F615SB	10																																																														
x2																																																																				
x4																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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D0	D1	C	RB	A	Q	QB																																																														
0	X	/	1	0	0	1																																																														
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X	X	\	1	0	Hold																																																															
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D0	D1	C	RB	A	Q																																																															
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F615S	C → Q	(HH)		0.423	0.673	1.278	0.012	0.016	0.023	D0	1.0	Q	31
		(HL)		0.422	0.685	1.274	0.010	0.013	0.017	D1	1.0	QB	31
	C → QB	(HH)		0.521	0.856	1.620	0.012	0.016	0.022	C	1.0		
		(HL)		0.556	0.902	1.723	0.010	0.013	0.017	RB	2.2		
	RB → Q	(LL)		0.199	0.311	0.535	0.010	0.013	0.017	A	1.0		
	RB → QB	(LH)		0.305	0.567	1.028	0.012	0.016	0.022				
	Set up time	D0		0.700		1.560							
	Set up time	D1		0.700		1.570							
	Set up time	A		0.700		1.720							
	Hold time	D0		0.270		0.000							
	Hold time	D1		0.270		0.000							
	Hold time	A		0.250		0.000							
	Release time	RB		0.190		0.000							
	Removal time	RB		0.670		1.010							
	Min Pulse	C		0.747		2.104							
	Min Pulse	RB		0.547		1.337							
	F615SQ	C → Q	(HH)		0.423	0.674	1.282	0.012	0.016	0.023	D0	1.0	Q
		(HL)		0.422	0.684	1.276	0.010	0.013	0.017	D1	1.0		
RB → Q		(LL)		0.199	0.312	0.537	0.010	0.013	0.017	C	1.0		
Set up time		D0		0.700		1.570				RB	2.3		
Set up time		D1		0.700		1.570				A	1.0		
Set up time		A		0.700		1.720							
Hold time		D0		0.260		0.000							
Hold time		D1		0.270		0.000							
Hold time		A		0.250		0.000							
Release time		RB		0.190		0.000							
Removal time		RB		0.670		1.010							
Min Pulse		C		0.614		1.664							
Min Pulse		RB		0.384		0.837							
F615SB	C → QB	(HH)		0.351	0.564	1.051	0.012	0.016	0.023	D0	1.0	QB	31
		(HL)		0.356	0.567	1.010	0.011	0.014	0.020	D1	1.0		
	RB → QB	(LH)		0.327	0.748	1.443	0.012	0.016	0.023	C	1.0		
	Set up time	D0		0.710		1.550				RB	2.3		
	Set up time	D1		0.710		1.550				A	1.0		
	Set up time	A		0.700		1.700							
	Hold time	D0		0.270		0.000							
	Hold time	D1		0.270		0.000							
	Hold time	A		0.250		0.000							
	Release time	RB		0.170		0.000							
	Removal time	RB		0.630		0.960							
	Min Pulse	C		0.548		1.426							
	Min Pulse	RB		0.626		1.743							

Chapter 2 Function Block

Function	D-F/F with SB, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F616S	11	F616SQ	10	F616SB	10																																																														
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D0	D1	C	SB	A	Q	QB																																																														
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D0	D1	C	SB	A	Q																																																															
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D0	D1	C	SB	A	QB																																																															
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Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F616S	C → Q	(HH)		0.365	0.560	1.005	0.011	0.015	0.021	D0	1.0	Q	35	
		(HL)		0.431	0.699	1.310	0.010	0.013	0.017	D1	1.0	QB	34	
	C → QB	(HH)		0.582	0.978	1.936	0.011	0.015	0.021	C	1.0			
		(HL)		0.493	0.779	1.416	0.010	0.013	0.017	SB	2.2			
	SB → Q	(LH)		0.335	0.620	1.172	0.011	0.015	0.021	A	1.0			
	SB → QB	(LL)		0.189	0.385	0.658	0.010	0.013	0.018					
	Set up time	D0		0.720		1.740								
	Set up time	D1		0.720		1.740								
	Set up time	A		0.740		1.860								
	Hold time	D0		0.240		0.000								
	Hold time	D1		0.240		0.000								
	Hold time	A		0.230		0.000								
	Release time	SB		0.440		0.550								
	Removal time	SB		0.370		0.380								
	Min Pulse	C		0.755		2.313								
	Min Pulse	SB		0.577		1.506								
F616SQ	C → Q	(HH)		0.366	0.561	1.007	0.011	0.015	0.021	D0	1.0	Q	35	
		(HL)		0.429	0.695	1.309	0.010	0.013	0.017	D1	1.0			
	SB → Q	(LH)		0.316	0.559	1.051	0.011	0.015	0.021	C	1.0			
	Set up time	D0		0.720		1.740				SB	2.2			
	Set up time	D1		0.720		1.730				A	1.0			
	Set up time	A		0.730		1.860								
	Hold time	D0		0.240		0.000								
	Hold time	D1		0.240		0.000								
	Hold time	A		0.230		0.000								
	Release time	SB		0.440		0.550								
	Removal time	SB		0.370		0.380								
	Min Pulse	C		0.603		1.688								
	Min Pulse	SB		0.535		1.374								
	F616SB	C → QB	(HH)		0.376	0.604	1.137	0.011	0.016	0.023	D0	1.0	QB	32
			(HL)		0.350	0.553	0.976	0.011	0.014	0.020	D1	1.0		
		SB → QB	(LL)		0.282	0.501	0.929	0.010	0.014	0.019	C	1.0		
Set up time		D0		0.730		1.750				SB	2.2			
Set up time		D1		0.730		1.750				A	1.0			
Set up time		A		0.750		1.880								
Hold time		D0		0.250		0.000								
Hold time		D1		0.250		0.000								
Hold time		A		0.230		0.000								
Release time		SB		0.450		0.570								
Removal time		SB		0.350		0.340								
Min Pulse		C		0.549		1.517								
Min Pulse		SB		0.521		1.267								

Chapter 2 Function Block

Function	D-F/F with RB, SB, 2 to 1 Selector																																																																																											
Block type	Standard type						Low Gate type																																																																																					
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F647S	C → Q	(HH)		0.415	0.655	1.239	0.011	0.015	0.022	D0	1.0	Q	34
		(HL)		0.434	0.701	1.314	0.010	0.013	0.017	D1	1.0	QB	32
	C → QB	(HH)		0.584	0.976	1.934	0.011	0.015	0.021	C	1.0		
		(HL)		0.544	0.877	1.666	0.010	0.013	0.017	RB	2.3		
	RB → Q	(LL)		0.178	0.275	0.466	0.010	0.013	0.017	SB	2.2		
	RB → QB	(LH)		0.332	0.681	1.340	0.011	0.015	0.022	A	1.0		
	SB → Q	(LH)		0.386	0.725	1.422	0.011	0.015	0.022				
	SB → QB	(LL)		0.187	0.385	0.656	0.010	0.013	0.018				
	Set up time	D0		0.710		1.720							
	Set up time	D1		0.710		1.720							
	Set up time	A		0.730		1.850							
	Hold time	D0		0.250		0.000							
	Hold time	D1		0.260		0.000							
	Hold time	A		0.240		0.000							
	Release time	RB		0.170		0.000							
	Release time	SB		0.420		0.530							
	Removal time	RB		0.700		1.100							
	Removal time	SB		0.390		0.440							
Min Pulse	C		0.758		2.315								
Min Pulse	RB		0.614		1.649								
Min Pulse	SB		0.657		1.769								
F647SQ	C → Q	(HH)		0.414	0.656	1.243	0.011	0.015	0.022	D0	1.0	Q	34
		(HL)		0.432	0.697	1.313	0.010	0.013	0.017	D1	1.0		
	RB → Q	(LL)		0.178	0.276	0.466	0.010	0.013	0.017	C	1.0		
	SB → Q	(LH)		0.358	0.655	1.286	0.011	0.015	0.022	RB	2.3		
	Set up time	D0		0.710		1.720				SB	2.2		
	Set up time	D1		0.710		1.720				A	1.0		
	Set up time	A		0.730		1.850							
	Hold time	D0		0.260		0.000							
	Hold time	D1		0.260		0.000							
	Hold time	A		0.240		0.000							
	Release time	RB		0.170		0.000							
	Release time	SB		0.420		0.520							
Removal time	RB		0.710		1.100								
Removal time	SB		0.390		0.440								
Min Pulse	C		0.608		1.695								
Min Pulse	RB		0.354		0.757								
Min Pulse	SB		0.608		1.618								
F647SB	C → QB	(HH)		0.382	0.613	1.152	0.011	0.016	0.023	D0	1.0	QB	32
		(HL)		0.351	0.551	0.965	0.011	0.014	0.020	D1	1.0		
	RB → QB	(LH)		0.374	0.888	1.808	0.011	0.016	0.023	C	1.0		
	SB → QB	(LL)		0.275	0.499	0.921	0.011	0.014	0.020	RB	2.3		
	Set up time	D0		0.720		1.750				SB	2.2		
	Set up time	D1		0.720		1.750				A	1.0		
	Set up time	A		0.740		1.880							
	Hold time	D0		0.250		0.000							
	Hold time	D1		0.260		0.000							
	Hold time	A		0.240		0.000							
	Release time	RB		0.140		0.000							
	Release time	SB		0.430		0.560							
Removal time	RB		0.660		1.020								
Removal time	SB		0.380		0.400								
Min Pulse	C		0.558		1.533								
Min Pulse	RB		0.714		2.114								
Min Pulse	SB		0.520		1.254								

Chapter 2 Function Block

Function	D-F/F (CB) with 2 to 1 Selector																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F661S	10	F661SQ	9	F661SB	9																																																
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F661S	CB → Q	(LH)		0.387	0.641	1.217	0.011	0.015	0.021	D0	1.0	Q	35
				0.360	0.586	1.095	0.010	0.013	0.017	D1	1.0	QB	35
				0.512	0.857	1.627	0.010	0.013	0.017	A	1.0		
	CB → QB	(LH)		0.453	0.752	1.444	0.011	0.015	0.021	D0	1.0		
										D1	1.0		
										A	1.0		
	Set up time	D0		0.670		1.450							
				0.670		1.450							
				0.700		1.580							
				0.270		0.060							
				0.270		0.060							
			0.290		0.000								
			0.290		0.000								
			0.720		1.954								
F661SQ	CB → Q	(LH)		0.387	0.641	1.217	0.011	0.015	0.021	D0	1.0	Q	35
				0.359	0.587	1.097	0.010	0.013	0.017	D1	1.0	QB	35
				0.670		1.450				A	1.0		
	Set up time	D0		0.670		1.450							
				0.670		1.450							
				0.700		1.590							
	Hold time	D0		0.270		0.050							
				0.270		0.050							
				0.290		0.000							
	Min Pulse	CB		0.595		1.543							
F661SB	CB → QB	(LH)		0.301	0.489	0.921	0.011	0.015	0.022	D0	1.0	QB	34
				0.346	0.575	1.087	0.011	0.014	0.020	D1	1.0		
				0.680		1.450				CB	1.0		
	Set up time	D0		0.680		1.440				A	1.0		
				0.700		1.580							
				0.280		0.060							
	Hold time	D0		0.280		0.060							
				0.280		0.060							
				0.290		0.000							
	Min Pulse	CB		0.563		1.421							

Chapter 2 Function Block

Function	D-F/F (CB) with RB, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
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Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F665S	CB → Q	(LH)		0.447	0.755	1.491	0.012	0.016	0.023	D0	1.0	Q	31	
		(LL)		0.375	0.614	1.151	0.010	0.013	0.017					
	CB → QB	(LH)		0.475	0.787	1.501	0.012	0.016	0.022	D1	1.0	QB	31	
		(LL)		0.582	0.985	1.939	0.010	0.013	0.017					
	RB → Q	(LL)		0.199	0.310	0.533	0.010	0.013	0.017	RB	2.2	A	1.0	
		(LH)		0.304	0.566	1.027	0.012	0.016	0.022					
	Set up time	D0		0.710		1.500								
	Set up time	D1		0.700		1.490								
	Set up time	A		0.710		1.620								
	Hold time	D0		0.250		0.020								
	Hold time	D1		0.250		0.030								
	Hold time	A		0.280		0.000								
	Release time	RB		0.190		0.000								
	Removal time	RB		0.650		1.110								
	Min Pulse	CB		0.784		2.260								
	Min Pulse	RB		0.546		1.336								
F665SQ	CB → Q	(LH)		0.446	0.756	1.493	0.012	0.016	0.023	D0	1.0	Q	31	
		(LL)		0.375	0.613	1.155	0.010	0.013	0.017					
	RB → Q	(LL)		0.199	0.312	0.535	0.010	0.013	0.017	D1	1.0	CB	1.0	
		(LH)		0.329	0.577	1.143	0.011	0.014	0.020					
	Set up time	D0		0.710		1.500				RB	2.3	A	1.0	
	Set up time	D1		0.700		1.490								
	Set up time	A		0.710		1.620								
	Hold time	D0		0.250		0.020								
	Hold time	D1		0.250		0.030								
	Hold time	A		0.280		0.000								
	Release time	RB		0.190		0.000								
	Removal time	RB		0.650		1.110								
	Min Pulse	CB		0.650		1.815								
	Min Pulse	RB		0.383		0.835								
	F665SB	CB → QB	(LH)		0.319	0.519	0.978	0.012	0.016	0.023	D0	1.0	QB	31
			(LL)		0.359	0.601	1.143	0.011	0.014	0.020				
RB → QB		(LH)		0.329	0.757	1.458	0.012	0.016	0.023	D1	1.0	CB	1.0	
		(LL)		0.359	0.601	1.143	0.011	0.014	0.020					
Set up time		D0		0.720		1.490				RB	2.3	A	1.0	
Set up time		D1		0.710		1.490								
Set up time		A		0.710		1.610								
Hold time		D0		0.260		0.030								
Hold time		D1		0.260		0.040								
Hold time		A		0.280		0.000								
Release time		RB		0.190		0.000								
Removal time		RB		0.610		1.040								
Min Pulse		CB		0.573		1.473								
Min Pulse		RB		0.635		1.759								



Chapter 2 Function Block

Function	D-F/F (CB) with SB, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F666S	11	F666SQ	10	F666SB	10																																																														
x2																																																																				
x4																																																																				
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F666S	CB → Q	(LH)		0.385	0.636	1.206	0.011	0.015	0.021	D0	1.0	Q	35
		(LL)		0.377	0.615	1.160	0.010	0.013	0.017	D1	1.0	QB	34
	CB → QB	(LH)		0.529	0.895	1.790	0.011	0.015	0.021	CB	1.0		
		(LL)		0.511	0.853	1.618	0.010	0.013	0.017	SB	2.2		
	SB → Q	(LH)		0.330	0.618	1.169	0.011	0.015	0.021	A	1.0		
		(LL)		0.189	0.383	0.656	0.010	0.013	0.018				
	Set up time	D0		0.720		1.820							
	Set up time	D1		0.720		1.810							
	Set up time	A		0.750		1.950							
	Hold time	D0		0.290		0.080							
	Hold time	D1		0.290		0.080							
	Hold time	A		0.300		0.000							
	Release time	SB		0.410		0.720							
	Removal time	SB		0.410		0.460							
	Min Pulse	CB		0.735		2.125							
	Min Pulse	SB		0.576		1.502							
	F666SQ	CB → Q	(LH)		0.384	0.635	1.205	0.011	0.015	0.021	D0	1.0	Q
(LL)				0.376	0.614	1.162	0.010	0.013	0.017	D1	1.0		
SB → Q		(LH)		0.314	0.553	1.042	0.011	0.015	0.021	CB	1.0		
		(LL)		0.314	0.553	1.042	0.011	0.015	0.021	SB	2.2		
Set up time		D0		0.720		1.820				A	1.0		
Set up time		D1		0.720		1.820							
Set up time		A		0.750		1.940							
Hold time		D0		0.290		0.080							
Hold time		D1		0.290		0.080							
Hold time		A		0.300		0.000							
Release time		SB		0.410		0.720							
Removal time		SB		0.410		0.460							
Min Pulse		CB		0.589		1.530							
Min Pulse	SB		0.527		1.364								
F666SB	CB → QB	(LH)		0.335	0.545	1.041	0.011	0.016	0.023	D0	1.0	QB	32
		(LL)		0.343	0.572	1.081	0.011	0.014	0.020	D1	1.0		
	SB → QB	(LH)		0.281	0.496	0.921	0.010	0.014	0.019	CB	1.0		
		(LL)		0.281	0.496	0.921	0.010	0.014	0.019	SB	2.2		
	Set up time	D0		0.730		1.790				A	1.0		
	Set up time	D1		0.730		1.790							
	Set up time	A		0.750		1.920							
	Hold time	D0		0.290		0.080							
	Hold time	D1		0.290		0.080							
	Hold time	A		0.300		0.000							
	Release time	SB		0.420		0.680							
	Removal time	SB		0.390		0.430							
	Min Pulse	CB		0.559		1.414							
Min Pulse	SB		0.514		1.257								

Chapter 2 Function Block

Function	D-F/F (CB) with RB, SB, 2 to 1 Selector																																																																																									
Block type	Standard type					Low Gate type																																																																																				
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Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																
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D0	D1	CB	RB	SB	A	QB																																																																																				
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F667S	CB → Q	(LH)		0.437	0.736	1.446	0.011	0.015	0.022	D0	1.0	Q	34
		(LL)		0.382	0.622	1.171	0.010	0.013	0.017	D1	1.0	QB	32
	CB → QB	(LH)		0.531	0.898	1.793	0.011	0.015	0.021	CB	1.0		
		(LL)		0.564	0.956	1.872	0.010	0.013	0.017	RB	2.3		
	RB → Q	(LL)		0.179	0.275	0.466	0.010	0.013	0.017	SB	2.2		
		(LH)		0.331	0.680	1.338	0.011	0.015	0.022	A	1.0		
	SB → Q	(LH)		0.385	0.724	1.422	0.011	0.015	0.022				
		(LL)		0.187	0.384	0.656	0.010	0.013	0.018				
	Set up time	D0		0.720		1.830							
	Set up time	D1		0.720		1.830							
	Set up time	A		0.750		1.960							
	Hold time	D0		0.280		0.070							
	Hold time	D1		0.280		0.070							
	Hold time	A		0.290		0.000							
	Release time	RB		0.170		0.000							
	Release time	SB		0.390		0.720							
	Removal time	RB		0.680		1.220							
Removal time	SB		0.430		0.490								
Min Pulse	CB		0.769		2.196								
Min Pulse	RB		0.614		1.646								
Min Pulse	SB		0.656		1.768								
F667SQ	CB → Q	(LH)		0.435	0.734	1.445	0.011	0.015	0.022	D0	1.0	Q	34
		(LL)		0.381	0.621	1.172	0.010	0.013	0.017	D1	1.0		
	RB → Q	(LL)		0.178	0.276	0.466	0.010	0.013	0.017	CB	1.0		
		(LH)		0.358	0.655	1.286	0.011	0.015	0.022	RB	2.3		
	SB → Q	(LH)		0.358	0.655	1.286	0.011	0.015	0.022	SB	2.2		
		(LL)		0.178	0.276	0.466	0.010	0.013	0.017	A	1.0		
	Set up time	D0		0.720		1.830							
	Set up time	D1		0.720		1.830							
	Set up time	A		0.750		1.970							
	Hold time	D0		0.280		0.070							
	Hold time	D1		0.280		0.070							
	Hold time	A		0.290		0.000							
	Release time	RB		0.170		0.000							
	Release time	SB		0.390		0.720							
	Removal time	RB		0.690		1.220							
	Removal time	SB		0.430		0.490							
	Min Pulse	CB		0.641		1.771							
Min Pulse	RB		0.354		0.757								
Min Pulse	SB		0.608		1.617								
F667SB	CB → QB	(LH)		0.340	0.552	1.051	0.011	0.016	0.023	D0	1.0	QB	32
		(LL)		0.345	0.572	1.077	0.011	0.014	0.020	D1	1.0		
	RB → QB	(LH)		0.374	0.887	1.807	0.011	0.016	0.023	CB	1.0		
		(LL)		0.274	0.499	0.919	0.011	0.014	0.020	RB	2.3		
	SB → QB	(LH)		0.274	0.499	0.919	0.011	0.014	0.020	SB	2.2		
		(LL)		0.730		1.820				A	1.0		
	Set up time	D0		0.730		1.820							
	Set up time	D1		0.720		1.820							
	Set up time	A		0.750		1.950							
	Hold time	D0		0.290		0.080							
	Hold time	D1		0.290		0.080							
	Hold time	A		0.300		0.000							
	Release time	RB		0.160		0.000							
	Release time	SB		0.410		0.690							
	Removal time	RB		0.640		1.120							
	Removal time	SB		0.420		0.470							
	Min Pulse	CB		0.561		1.411							
Min Pulse	RB		0.713		2.112								
Min Pulse	SB		0.520		1.253								

Chapter 2 Function Block

Function	D-F/F with Hold																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F641H	10	F641HQ	9	F641HB	9																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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0	/	0	1																																		
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Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F641H	C → Q	(HH)		0.362	0.554	0.998	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.409	0.661	1.224	0.010	0.013	0.017	C	1.0	QB	35
	C → QB	(HH)		0.528	0.866	1.639	0.011	0.015	0.021	H	1.0		
		(HL)		0.521	0.821	1.492	0.010	0.013	0.018				
	Set up time	D		0.680		1.500							
	Set up time	H		0.670		1.590							
	Hold time	D		0.270		0.000							
Hold time	H		0.250		0.000								
Min Pulse	C		0.714		2.015								
F641HQ	C → Q	(HH)		0.361	0.554	0.998	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.409	0.660	1.223	0.010	0.013	0.017	C	1.0		
	Set up time	D		0.680		1.500				H	1.0		
	Set up time	H		0.670		1.600							
	Hold time	D		0.270		0.000							
	Hold time	H		0.250		0.000							
F641HB	C → QB	(HH)		0.338	0.540	1.002	0.011	0.015	0.022	D	1.0	QB	34
		(HL)		0.345	0.543	0.958	0.011	0.014	0.020	C	1.0		
	Set up time	D		0.680		1.470				H	1.0		
	Set up time	H		0.670		1.560							
	Hold time	D		0.270		0.010							
	Hold time	H		0.250		0.000							
Min Pulse	C		0.541		1.382								

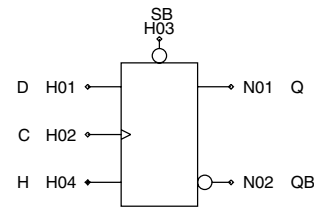
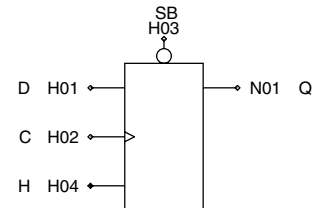
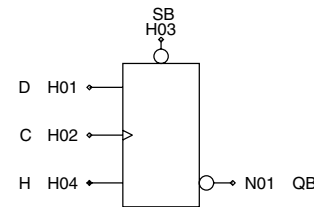
Chapter 2 Function Block

Function	D-F/F with RB, Hold																																															
Block type	Standard type						Low Gate type																																									
	Normal		Q output		QB output		Normal		Q output		QB output																																					
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																				
Low Power																																																
x1	F615H	11	F615HQ	10	F615HB	10																																										
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Logic Diagram for "Normal"				Truth Table for "Normal"																																												
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D	C	RB	H	Q	QB																																											
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Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F615H	C → Q	(HH)		0.432	0.682	1.289	0.012	0.016	0.023	D	1.0	Q	31	
		(HL)		0.436	0.702	1.297	0.010	0.013	0.017	C	1.0	QB	31	
	C → QB	(HH)		0.562	0.913	1.713	0.012	0.016	0.022	RB	2.3			
		(HL)		0.602	0.966	1.829	0.010	0.013	0.018	H	1.0			
	RB → Q	(LL)		0.199	0.311	0.534	0.010	0.013	0.017					
	RB → QB	(LH)		0.333	0.607	1.097	0.012	0.016	0.022					
	Set up time	D		0.690		1.540								
	Set up time	H		0.680		1.630								
	Hold time	D		0.290		0.010								
	Hold time	H		0.270		0.000								
	Release time	RB		0.170		0.000								
	Removal time	RB		0.680		1.030								
	Min Pulse	C		0.802		2.224								
	Min Pulse	RB		0.576		1.407								
F615HQ	C → Q	(HH)		0.432	0.682	1.291	0.012	0.016	0.023	D	1.0	Q	31	
		(HL)		0.435	0.701	1.298	0.010	0.013	0.017	C	1.0	QB	31	
	RB → Q	(LL)		0.199	0.312	0.535	0.010	0.013	0.017	RB	2.3			
	Set up time	D		0.690		1.540				H	1.0			
	Set up time	H		0.680		1.630								
	Hold time	D		0.290		0.010								
	Hold time	H		0.270		0.000								
	Release time	RB		0.170		0.000								
	Removal time	RB		0.680		1.030								
	Min Pulse	C		0.633		1.685								
	Min Pulse	RB		0.384		0.834								
	F615HB	C → QB	(HH)		0.366	0.583	1.077	0.012	0.016	0.023	D	1.0	QB	31
			(HL)		0.371	0.579	1.022	0.011	0.014	0.020	C	1.0		
		RB → QB	(LH)		0.350	0.752	1.450	0.012	0.016	0.023	RB	2.3		
Set up time		D		0.690		1.540				H	1.0			
Set up time		H		0.680		1.630								
Hold time		D		0.290		0.020								
Hold time		H		0.260		0.000								
Release time		RB		0.160		0.000								
Removal time		RB		0.640		0.980								
Min Pulse		C		0.572		1.462								
Min Pulse		RB		0.629		1.748								

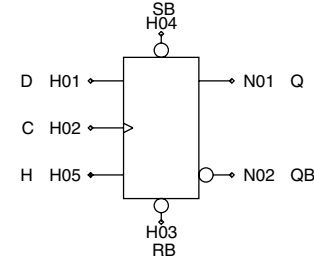
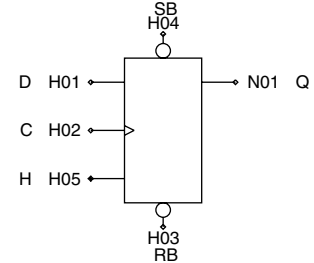
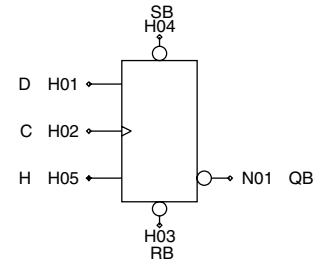
## Chapter 2 Function Block

Function	D-F/F with SB, Hold																																															
Block type	Standard type						Low Gate type																																									
	Normal		Q output		QB output		Normal		Q output		QB output																																					
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																				
Low Power																																																
x1	F616H	11	F616HQ	10	F616HB	10																																										
x2																																																
x4																																																
Logic Diagram for "Normal"				Truth Table for "Normal"																																												
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>SB</th> <th>H</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>/</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>\</td> <td>1</td> <td>0</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>X</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	SB	H	Q	QB	0	/	1	0	0	1	1	/	1	0	1	0	X	\	1	0	Hold		X	X	1	1	Hold		X	X	0	X	1	0
D	C	SB	H	Q	QB																																											
0	/	1	0	0	1																																											
1	/	1	0	1	0																																											
X	\	1	0	Hold																																												
X	X	1	1	Hold																																												
X	X	0	X	1	0																																											
Logic Diagram for "Q output"				Truth Table for "Q output"																																												
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D	C	SB	H	Q																																												
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X	X	0	X	1																																												
Logic Diagram for "QB output"				Truth Table for "QB output"																																												
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D	C	SB	H	QB																																												
0	/	1	0	1																																												
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X	\	1	0	Hold																																												
X	X	1	1	Hold																																												
X	X	0	X	0																																												

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F616H	C → Q	(HH)		0.365	0.559	1.004	0.011	0.015	0.021	D	1.0	Q	35
			(HL)	0.431	0.698	1.309	0.010	0.013	0.017	C	1.0	QB	33
			(LH)	0.530	0.834	1.507	0.010	0.013	0.018	H	1.0		
	C → QB	(HH)	0.624	1.042	2.055	0.011	0.015	0.022	SB	2.2			
		(LH)	0.334	0.675	1.273	0.011	0.015	0.021					
	SB → Q	(LH)	0.334	0.675	1.273	0.011	0.015	0.021					
		(LL)	0.223	0.436	0.747	0.010	0.013	0.019					
	Set up time	D		0.720		1.740							
	Set up time	H		0.740		1.860							
	Hold time	D		0.240		0.000							
	Hold time	H		0.230		0.000							
	Release time	SB		0.440		0.560							
	Removal time	SB		0.370		0.380							
	Min Pulse	C		0.796		2.435							
Min Pulse	SB		0.629		1.614								
F616HQ	C → Q	(HH)		0.366	0.561	1.007	0.011	0.015	0.021	D	1.0	Q	35
			(HL)	0.430	0.697	1.307	0.010	0.013	0.017	C	1.0	QB	33
			(LH)	0.336	0.583	1.090	0.011	0.015	0.021	SB	2.2		
	SB → Q	(LH)	0.336	0.583	1.090	0.011	0.015	0.021	H	1.0			
	Set up time	D		0.720		1.740							
	Set up time	H		0.730		1.860							
	Hold time	D		0.240		0.000							
	Hold time	H		0.230		0.000							
	Release time	SB		0.440		0.560							
	Removal time	SB		0.370		0.380							
	Min Pulse	C		0.604		1.689							
	Min Pulse	SB		0.551		1.420							
	F616HB	C → QB	(HH)		0.378	0.607	1.143	0.011	0.016	0.023	D	1.0	QB
(HL)				0.350	0.553	0.977	0.011	0.014	0.020	C	1.0		
(LH)				0.301	0.523	0.970	0.011	0.014	0.019	SB	2.2		
SB → QB		(LH)	0.301	0.523	0.970	0.011	0.014	0.019	H	1.0			
Set up time		D		0.730		1.750							
Set up time		H		0.750		1.880							
Hold time		D		0.250		0.000							
Hold time		H		0.230		0.000							
Release time		SB		0.450		0.570							
Removal time		SB		0.350		0.340							
Min Pulse		C		0.552		1.522							
Min Pulse		SB		0.537		1.310							

Chapter 2 Function Block

Function	D-F/F with RB, SB, Hold																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F647H	12	F647HQ	11	F647HB	11																																																														
x2																																																																				
x4																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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D	C	RB	SB	H	Q	QB																																																														
0	/	1	1	0	0	1																																																														
1	/	1	1	0	1	0																																																														
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X	X	0	0	X	0	0																																																														
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																
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D	C	RB	SB	H	Q																																																															
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Logic Diagram for "QB output"				Truth Table for "QB output"																																																																
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D	C	RB	SB	H	QB																																																															
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X	X	1	0	X	0																																																															
X	X	0	0	X	0																																																															

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F647H	C → Q	(HH)		0.416	0.657	1.240	0.011	0.015	0.022	D	1.0	Q	34	
		(HL)		0.435	0.702	1.315	0.010	0.013	0.017	C	1.0	QB	31	
	C → QB	(HH)		0.627	1.044	2.059	0.011	0.015	0.022	RB	2.4			
		(HL)		0.584	0.940	1.769	0.010	0.013	0.018	SB	2.1			
	RB → Q	(LL)		0.179	0.275	0.466	0.010	0.013	0.017	H	1.0			
	RB → QB	(LH)		0.376	0.749	1.465	0.011	0.016	0.023					
	SB → Q	(LH)		0.387	0.793	1.545	0.011	0.015	0.022					
	SB → QB	(LL)		0.223	0.440	0.748	0.010	0.013	0.019					
	Set up time	D		0.710		1.720								
	Set up time	H		0.730		1.850								
	Hold time	D		0.250		0.000								
	Hold time	H		0.240		0.000								
	Release time	RB		0.170		0.000								
	Release time	SB		0.420		0.530								
	Removal time	RB		0.700		1.100								
	Removal time	SB		0.390		0.440								
	Min Pulse	C		0.801		2.440								
Min Pulse	RB		0.660		1.775									
Min Pulse	SB		0.717		1.902									
F647HQ	C → Q	(HH)		0.414	0.655	1.239	0.011	0.015	0.022	D	1.0	Q	34	
		(HL)		0.433	0.700	1.311	0.010	0.013	0.017	C	1.0			
	RB → Q	(LL)		0.178	0.275	0.466	0.010	0.013	0.017	RB	2.3			
	SB → Q	(LH)		0.386	0.683	1.331	0.011	0.015	0.022	SB	2.2			
	Set up time	D		0.710		1.720								
	Set up time	H		0.730		1.850								
	Hold time	D		0.250		0.000								
	Hold time	H		0.240		0.000								
	Release time	RB		0.170		0.000								
	Release time	SB		0.420		0.530								
	Removal time	RB		0.700		1.100								
	Removal time	SB		0.390		0.440								
	Min Pulse	C		0.607		1.693								
	Min Pulse	RB		0.353		0.756								
	Min Pulse	SB		0.627		1.672								
	F647HB	C → QB	(HH)		0.383	0.613	1.152	0.011	0.016	0.023	D	1.0	QB	31
			(HL)		0.350	0.550	0.964	0.011	0.014	0.020	C	1.0		
RB → QB		(LH)		0.416	0.892	1.812	0.011	0.016	0.023	RB	2.3			
SB → QB		(LL)		0.302	0.516	0.954	0.011	0.014	0.020	SB	2.2			
Set up time		D		0.730		1.760								
Set up time		H		0.740		1.890								
Hold time		D		0.250		0.000								
Hold time		H		0.240		0.000								
Release time		RB		0.140		0.000								
Release time		SB		0.430		0.560								
Removal time		RB		0.660		1.020								
Removal time		SB		0.380		0.400								
Min Pulse		C		0.558		1.533								
Min Pulse		RB		0.713		2.113								
Min Pulse		SB		0.536		1.293								

Chapter 2 Function Block

Function	D-F/F (CB) with 2 to 1 Selector(2 CTRL), RB																																																																																			
Block type	Standard type					Low Gate type																																																																														
	Normal		Q output		QB output		Normal		Q output		QB output																																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																								
Low Power																																																																																				
x1	F673	11																																																																																		
x2																																																																																				
x4																																																																																				
Logic Diagram for "Normal"			Truth Table for "Normal"																																																																																	
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D0	D1	S0	S1	CB	RB	Q	QB																																																																													
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Logic Diagram for "Q output"			Truth Table for "Q output"																																																																																	
Logic Diagram for "QB output"			Truth Table for "QB output"																																																																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F673	CB	→	Q (LH)	0.464	0.780	1.542	0.011	0.016	0.022	D0	1.0	Q	33
			(LL)	0.383	0.625	1.166	0.010	0.013	0.018	D1	1.0	QB	35
	CB	→	QB (LH)	0.453	0.749	1.423	0.011	0.015	0.021	CB	1.0		
			(LL)	0.571	0.957	1.885	0.010	0.012	0.017	RB	2.2		
	RB	→	Q (LL)	0.207	0.323	0.549	0.010	0.013	0.018	S0	1.0		
	RB	→	QB (LH)	0.280	0.447	0.806	0.011	0.015	0.021	S1	1.0		
	Set up time		D0	0.670		1.340							
	Set up time		D1	0.760		1.690							
	Set up time		S0	0.690		1.260							
	Set up time		S1	0.690		1.590							
	Hold time		D0	0.280		0.120							
	Hold time		D1	0.270		0.000							
	Hold time		S0	0.350		0.220							
	Hold time		S1	0.270		0.000							
	Release time		RB	0.180		0.000							
	Removal time		RB	0.660		1.120							
	Min Pulse		CB	0.776		2.210							
Min Pulse		RB	0.484		1.134								

Chapter 2 Function Block

Function	D-F/F (CB) with Hold, 2 to 1 Selector(2 CTRL), RB																																																																																																																							
Block type	Standard type						Low Gate type																																																																																																																	
	Normal		Q output		QB output		Normal		Q output		QB output																																																																																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																																												
Low Power																																																																																																																								
x1	F674	12																																																																																																																						
x2																																																																																																																								
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Logic Diagram for "Normal"							<p>Truth Table for "Normal"</p> <table border="1"> <thead> <tr> <th>D0</th> <th>D1</th> <th>S0</th> <th>S1</th> <th>CB</th> <th>RB</th> <th>H</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr><td>0</td><td>X</td><td>1</td><td>0</td><td>\</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>X</td><td>1</td><td>0</td><td>\</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>X</td><td>X</td><td>1</td><td>0</td><td>\</td><td>1</td><td>1</td><td>X</td><td>X</td></tr> <tr><td>X</td><td>0</td><td>0</td><td>1</td><td>\</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>X</td><td>1</td><td>0</td><td>1</td><td>\</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>X</td><td>X</td><td>0</td><td>1</td><td>\</td><td>1</td><td>1</td><td>X</td><td>X</td></tr> <tr><td>X</td><td>X</td><td>0</td><td>0</td><td>\</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>X</td><td>X</td><td>0</td><td>0</td><td>\</td><td>1</td><td>1</td><td>Hold</td><td></td></tr> <tr><td>X</td><td>X</td><td>1</td><td>1</td><td>\</td><td>1</td><td>X</td><td>X</td><td>X</td></tr> <tr><td>X</td><td>X</td><td>X</td><td>X</td><td>/</td><td>1</td><td>X</td><td>Hold</td><td></td></tr> <tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>X</td><td>0</td><td>1</td></tr> </tbody> </table> <p>X: Irrelevant</p>						D0	D1	S0	S1	CB	RB	H	Q	QB	0	X	1	0	\	1	0	0	1	1	X	1	0	\	1	0	1	0	X	X	1	0	\	1	1	X	X	X	0	0	1	\	1	0	0	1	X	1	0	1	\	1	0	1	0	X	X	0	1	\	1	1	X	X	X	X	0	0	\	1	0	0	1	X	X	0	0	\	1	1	Hold		X	X	1	1	\	1	X	X	X	X	X	X	X	/	1	X	Hold		X	X	X	X	X	0	X	0	1
D0	D1	S0	S1	CB	RB	H	Q	QB																																																																																																																
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Logic Diagram for "Q output"							<p>Truth Table for "Q output"</p>																																																																																																																	
Logic Diagram for "QB output"							<p>Truth Table for "QB output"</p>																																																																																																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F674	CB	→	Q (LH)	0.466	0.785	1.548	0.011	0.015	0.022	D0	1.0	Q	33
			(LL)	0.384	0.626	1.168	0.010	0.013	0.018	D1	1.0	QB	35
	CB	→	QB (LH)	0.496	0.808	1.521	0.011	0.015	0.021	CB	1.0		
			(LL)	0.619	1.032	2.010	0.010	0.013	0.017	RB	2.1		
	RB	→	Q (LL)	0.202	0.316	0.539	0.010	0.013	0.018	S0	1.0		
	RB	→	QB (LH)	0.316	0.498	0.891	0.011	0.015	0.021	S1	1.0		
	Set up time		D0	0.830		1.780				H	1.0		
	Set up time		D1	0.840		2.090							
	Set up time		S0	0.870		1.830							
	Set up time		S1	0.880		2.140							
	Set up time		H	0.750		2.080							
	Hold time		D0	0.260		0.000							
	Hold time		D1	0.200		0.000							
	Hold time		S0	0.330		0.070							
	Hold time		S1	0.280		0.000							
	Hold time		H	0.140		0.000							
	Release time		RB	0.190		0.000							
	Removal time		RB	0.650		1.110							
Min Pulse		CB	0.827		2.335								
Min Pulse		RB	0.515		1.218								



[MEMO]

[MEMO]

## 2.12 T-F/F, JK-F/F

[MEMO]

Chapter 2 Function Block

Function	T-F/F with R, S																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power									L744	7																																
x1	F744	9	F744NQ	8																																						
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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T	R	S	Q	QB																																						
/	0	0	Invert																																							
\	0	0	Hold																																							
X	1	0	0	1																																						
X	0	1	1	0																																						
X	1	1	1	1																																						
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
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T	R	S	Q																																							
/	0	0	Invert																																							
\	0	0	Hold																																							
X	1	0	0																																							
X	0	1	1																																							
X	1	1	1																																							
Logic Diagram for "QB output"				Truth Table for "QB output"																																						

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F744	T → Q	(HH)		0.379	0.582	1.050	0.011	0.015	0.021	T	1.0	Q	35
		(HL)		0.477	0.780	1.457	0.010	0.013	0.019	R	2.1	QB	33
	T → QB	(HH)		0.608	1.020	1.977	0.011	0.015	0.021	S	2.3		
		(HL)		0.639	1.036	1.903	0.011	0.014	0.020				
	R → Q	(HL)		0.416	0.830	1.574	0.010	0.013	0.018				
	R → QB	(HH)		0.213	0.442	0.782	0.011	0.015	0.022				
	S → Q	(HH)		0.170	0.251	0.426	0.011	0.015	0.022				
	S → QB	(HL)		0.428	1.026	1.892	0.011	0.016	0.023				
	Release time	R		0.380		1.170							
	Release time	S		0.110		0.000							
	Removal time	R		0.440		0.330							
	Removal time	S		0.740		1.200							
	Min Pulse	T		0.839		2.348							
	Min Pulse	R		0.844		2.135							
Min Pulse	S		0.751		2.254								
L744	T → Q	(HH)		0.342	0.556	1.037	0.038	0.053	0.078	T	1.0	Q	7
		(HL)		0.330	0.493	0.861	0.021	0.027	0.038	R	2.3		
	R → Q	(HL)		0.140	0.156	0.233	0.014	0.024	0.033	S	2.1		
	S → Q	(HH)		0.283	0.540	1.024	0.038	0.054	0.079				
	Release time	R		0.110		0.000							
	Release time	S		0.380		1.150							
	Removal time	R		0.740		1.200							
	Removal time	S		0.440		0.330							
	Min Pulse	T		0.530		1.409							
	Min Pulse	R		0.228		0.594							
Min Pulse	S		0.609		1.557								
F744NQ	T → Q	(HH)		0.379	0.584	1.052	0.011	0.015	0.021	T	1.0	Q	35
		(HL)		0.477	0.780	1.459	0.010	0.013	0.019	R	2.1		
	R → Q	(HL)		0.412	0.757	1.438	0.010	0.013	0.018	S	2.3		
	S → Q	(HH)		0.170	0.251	0.426	0.011	0.015	0.022				
	Release time	R		0.380		1.170							
Release time	S		0.110		0.000								
Removal time	R		0.440		0.330								
Removal time	S		0.740		1.200								
Min Pulse	T		0.641		1.831								
Min Pulse	R		0.744		1.968								
Min Pulse	S		0.278		0.804								

Chapter 2 Function Block

Function	T-F/F with RB																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power																												
x1	F745	8	F745NQ	7																								
x2																												
x4																												
Logic Diagram for "Normal"					Truth Table for "Normal"																							
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T	RB	Q	QB																									
/	1	Invert																										
\	1	Hold																										
X	0	0	1																									
Logic Diagram for "Q output"					Truth Table for "Q output"																							
					<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>/</td> <td>1</td> <td>Invert</td> </tr> <tr> <td>\</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								T	RB	Q	/	1	Invert	\	1	Hold	X	0	0				
T	RB	Q																										
/	1	Invert																										
\	1	Hold																										
X	0	0																										
Logic Diagram for "QB output"					Truth Table for "QB output"																							

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F745	T	→	Q (HH)	0.406	0.642	1.223	0.011	0.015	0.022	T	1.0	Q	34
			(HL)	0.404	0.654	1.215	0.010	0.013	0.017				
	T	→	QB (HH)	0.532	0.878	1.677	0.011	0.015	0.021	RB	2.2	QB	33
			(HL)	0.572	0.931	1.775	0.010	0.013	0.018				
	RB	→	Q (LL)	0.183	0.284	0.479	0.010	0.013	0.017				
	RB	→	QB (LH)	0.316	0.651	1.189	0.011	0.015	0.022				
	Release time		RB	0.190		0.000							
	Removal time		RB	0.660		1.010							
	Min Pulse		T	0.761		2.160							
	Min Pulse		RB	0.605		1.503							
F745NQ	T	→	Q (HH)	0.405	0.643	1.223	0.011	0.015	0.022	T	1.0	Q	34
			(HL)	0.403	0.653	1.214	0.010	0.013	0.017				
	RB	→	Q (LL)	0.182	0.284	0.478	0.010	0.013	0.017	RB	2.2		
	Release time		RB	0.190		0.000							
	Removal time		RB	0.660		1.010							
	Min Pulse		T	0.594		1.606							
Min Pulse		RB	0.364		0.773								

Chapter 2 Function Block

Function	T-F/F with RB, SB																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power									L747	7																																
x1	F747	9	F747NQ	8																																						
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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T	RB	SB	Q	QB																																						
/	1	1	Invert																																							
\	1	1	Hold																																							
X	0	1	0	1																																						
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X	0	0	0	0																																						
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
				<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>SB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>/</td> <td>1</td> <td>1</td> <td>Invert</td> </tr> <tr> <td>\</td> <td>1</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>									T	RB	SB	Q	/	1	1	Invert	\	1	1	Hold	X	0	1	0	X	1	0	1	X	0	0	0						
T	RB	SB	Q																																							
/	1	1	Invert																																							
\	1	1	Hold																																							
X	0	1	0																																							
X	1	0	1																																							
X	0	0	0																																							
Logic Diagram for "QB output"				Truth Table for "QB output"																																						

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F747	T	→	Q (HH)	0.412	0.651	1.232	0.011	0.015	0.022	T	1.0	Q	34	
			(HL)	0.424	0.689	1.298	0.010	0.013	0.017					
	T	→	QB (HH)	0.614	1.040	2.089	0.011	0.015	0.022					
			(HL)	0.574	0.934	1.769	0.010	0.013	0.018	RB	2.3	QB	30	
	RB	→	Q (LL)	0.176	0.273	0.463	0.010	0.013	0.017					
	RB	→	QB (LH)	0.369	0.863	1.723	0.011	0.016	0.023					
	SB	→	Q (LH)	0.374	0.876	1.712	0.011	0.015	0.022	SB	2.1			
	SB	→	QB (LL)	0.217	0.516	0.897	0.010	0.014	0.020					
	Release time	RB		0.170		0.000								
	Release time	SB		0.410		0.480								
	Removal time	RB		0.690		1.080								
	Removal time	SB		0.400		0.460								
	Min Pulse	T		0.780		2.466								
	Min Pulse	RB		0.720		2.033								
Min Pulse	SB		0.770		2.079									
L747	T	→	Q (HH)	0.339	0.546	1.023	0.022	0.030	0.044	T	1.0	Q	11	
			(HL)	0.334	0.515	0.944	0.030	0.041	0.063					
	RB	→	Q (LL)	0.298	0.630	1.207	0.030	0.042	0.065					RB
	SB	→	Q (LH)	0.117	0.126	0.200	0.014	0.029	0.042					
	Release time	RB		0.410		0.470								
	Release time	SB		0.170		0.000								
	Removal time	RB		0.400		0.460								
	Removal time	SB		0.690		1.080								
	Min Pulse	T		0.517		1.400								
	Min Pulse	RB		0.611		1.565								
	Min Pulse	SB		0.234		0.450								
F747NQ	T	→	Q (HH)	0.412	0.653	1.237	0.011	0.015	0.022	T	1.0	Q	34	
			(HL)	0.424	0.689	1.298	0.010	0.013	0.017					
	RB	→	Q (LL)	0.176	0.273	0.463	0.010	0.013	0.017					RB
	SB	→	Q (LH)	0.375	0.769	1.504	0.011	0.015	0.022					
	Release time	RB		0.170		0.000				SB	2.1			
	Release time	SB		0.410		0.480								
	Removal time	RB		0.690		1.080								
Removal time	SB		0.400		0.460									
Min Pulse	T		0.595		1.675									
Min Pulse	RB		0.351		0.752									
Min Pulse	SB		0.688		1.866									

Chapter 2 Function Block

Function	T-F/F with Data-Hold R, S																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F791	12																																																				
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>T</th> <th>TE</th> <th>R</th> <th>S</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td></td> <td>Invert</td> </tr> <tr> <td>\</td> <td>1</td> <td>0</td> <td>0</td> <td></td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td></td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									T	TE	R	S	Q	QB	/	1	0	0		Invert	\	1	0	0		Hold	X	0	0	0		Hold	X	X	1	0	0	1	X	X	0	1	1	0	X	X	1	1	1	1
T	TE	R	S	Q	QB																																																	
/	1	0	0		Invert																																																	
\	1	0	0		Hold																																																	
X	0	0	0		Hold																																																	
X	X	1	0	0	1																																																	
X	X	0	1	1	0																																																	
X	X	1	1	1	1																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F791	T	→	Q	(HH)	0.429	0.656	1.180	0.011	0.015	0.022	T	1.0	Q	34
				(HL)	0.563	0.915	1.691	0.011	0.014	0.020	TE	1.7	QB	34
	T	→	QB	(HH)	0.665	1.109	2.116	0.011	0.015	0.021	R	2.1		
				(HL)	0.651	1.036	1.899	0.010	0.014	0.019	S	2.2		
	R	→	Q	(HL)	0.503	0.860	1.607	0.011	0.014	0.020				
	R	→	QB	(HH)	0.189	0.340	0.590	0.011	0.015	0.022				
	S	→	Q	(HH)	0.219	0.314	0.532	0.011	0.015	0.022				
	S	→	QB	(HL)	0.439	0.856	1.569	0.010	0.014	0.021				
	Set up time		TE		0.770		2.310							
	Hold time		TE		0.310		0.000							
	Release time		R		0.390		1.240							
	Release time		S		0.110		0.000							
	Removal time		R		0.430		0.320							
	Removal time		S		0.750		1.210							
Min Pulse		T		0.853		2.485								
Min Pulse		R		0.777		2.086								
Min Pulse		S		0.739		2.022								

## Chapter 2 Function Block

Function	T-F/F (TB) with RB																										
Block type	Standard type						Low Gate type																				
	Normal		Q output		QB output		Normal		Q output		QB output																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells															
Low Power																											
x1	F765	8	F765NQ	7																							
x2																											
x4																											
Logic Diagram for "Normal"						Truth Table for "Normal"																					
						<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>↘</td> <td>1</td> <td colspan="2">Invert</td> </tr> <tr> <td>↙</td> <td>1</td> <td colspan="2">Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>						T	RB	Q	QB	↘	1	Invert		↙	1	Hold		X	0	0	1
T	RB	Q	QB																								
↘	1	Invert																									
↙	1	Hold																									
X	0	0	1																								
Logic Diagram for "Q output"						Truth Table for "Q output"																					
						<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>↘</td> <td>1</td> <td>Invert</td> </tr> <tr> <td>↙</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>						T	RB	Q	↘	1	Invert	↙	1	Hold	X	0	0				
T	RB	Q																									
↘	1	Invert																									
↙	1	Hold																									
X	0	0																									
Logic Diagram for "QB output"						Truth Table for "QB output"																					

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F765	TB → Q	(LH)		0.428	0.724	1.433	0.011	0.015	0.022	TB	1.0	Q	34
		(LL)		0.357	0.582	1.089	0.010	0.013	0.017			QB	33
	TB → QB	(LH)		0.486	0.807	1.559	0.011	0.015	0.021	RB	2.2		
		(LL)		0.596	1.014	1.989	0.010	0.013	0.018				
	RB → Q	(LL)		0.183	0.285	0.479	0.010	0.013	0.017				
		(LH)		0.317	0.651	1.188	0.011	0.015	0.022				
	Release time	RB		0.180		0.000							
	Removal time	RB		0.650		1.110							
	Min Pulse	TB		0.794		2.308							
	Min Pulse	RB		0.605		1.502							
F765NQ	TB → Q	(LH)		0.428	0.723	1.432	0.011	0.015	0.022	TB	1.0	Q	34
		(LL)		0.356	0.582	1.091	0.010	0.013	0.017			RB	2.2
	RB → Q	(LL)		0.183	0.284	0.478	0.010	0.013	0.017				
				0.180		0.000							
	Release time	RB		0.650		1.110							
	Min Pulse	TB		0.627		1.752							
	Min Pulse	RB		0.364		0.773							

Chapter 2 Function Block

Function	T-F/F (TB) with RB, SB																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power									L767	7																																
x1	F767	9	F767NQ	8																																						
x2																																										
x4																																										
Logic Diagram for "Normal"			Truth Table for "Normal"																																							
			<table border="1"> <thead> <tr> <th>TB</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>\</td> <td>1</td> <td>1</td> <td>Invert</td> <td></td> </tr> <tr> <td>/</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>										TB	RB	SB	Q	QB	\	1	1	Invert		/	1	1	Hold		X	0	1	0	1	X	1	0	1	0	X	0	0	0	0
TB	RB	SB	Q	QB																																						
\	1	1	Invert																																							
/	1	1	Hold																																							
X	0	1	0	1																																						
X	1	0	1	0																																						
X	0	0	0	0																																						
Logic Diagram for "Q output"			Truth Table for "Q output"																																							
			<table border="1"> <thead> <tr> <th>TB</th> <th>RB</th> <th>SB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>\</td> <td>1</td> <td>1</td> <td>Invert</td> </tr> <tr> <td>/</td> <td>1</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>										TB	RB	SB	Q	\	1	1	Invert	/	1	1	Hold	X	0	1	0	X	1	0	1	X	0	0	0						
TB	RB	SB	Q																																							
\	1	1	Invert																																							
/	1	1	Hold																																							
X	0	1	0																																							
X	1	0	1																																							
X	0	0	0																																							
Logic Diagram for "QB output"			Truth Table for "QB output"																																							

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F767	TB	→	Q (LH)	0.426	0.723	1.425	0.011	0.015	0.022	TB	1.0	Q	34	
			(LL)	0.376	0.614	1.162	0.010	0.013	0.017					
	TB	→	QB (LH)	0.567	0.967	1.962	0.011	0.015	0.022					
			(LL)	0.587	1.005	1.965	0.010	0.013	0.018	RB	2.3	QB	30	
	RB	→	Q (LL)	0.176	0.273	0.462	0.010	0.013	0.017					
	RB	→	QB (LH)	0.369	0.863	1.723	0.011	0.016	0.023					
	SB	→	Q (LH)	0.374	0.876	1.712	0.011	0.015	0.022	SB	2.1			
	SB	→	QB (LL)	0.217	0.517	0.897	0.010	0.014	0.020					
	Release time	RB		0.180		0.000								
	Release time	SB		0.390		0.650								
	Removal time	RB		0.670		1.180								
	Removal time	SB		0.430		0.500								
	Min Pulse	TB		0.787		2.296								
	Min Pulse	RB		0.720		2.033								
Min Pulse	SB		0.770		2.079									
L767	TB	→	Q (LH)	0.291	0.473	0.893	0.022	0.030	0.044	TB	1.0	Q	11	
			(LL)	0.348	0.585	1.130	0.030	0.041	0.063					
	RB	→	Q (LL)	0.298	0.630	1.207	0.030	0.042	0.065					RB
	SB	→	Q (LH)	0.117	0.126	0.200	0.014	0.029	0.042					
	Release time	RB		0.390		0.640								
	Release time	SB		0.170		0.000								
	Removal time	RB		0.430		0.500								
	Removal time	SB		0.660		1.180								
	Min Pulse	TB		0.547		1.453								
	Min Pulse	RB		0.611		1.566								
	Min Pulse	SB		0.234		0.450								
	F767NQ	TB	→	Q (LH)	0.426	0.723	1.425	0.011	0.015	0.022	TB	1.0	Q	34
				(LL)	0.376	0.615	1.165	0.010	0.013	0.017				
		RB	→	Q (LL)	0.176	0.273	0.463	0.010	0.013	0.017				
SB		→	Q (LH)	0.375	0.769	1.505	0.011	0.015	0.022					
Release time		RB		0.180		0.000								
Release time		SB		0.390		0.650								
Removal time		RB		0.660		1.180								
Removal time		SB		0.430		0.500								
Min Pulse		TB		0.626		1.747								
Min Pulse		RB		0.351		0.752								
Min Pulse		SB		0.688		1.866								



Chapter 2 Function Block

Function	T-F/F (TB) with Data-Hold RB, SB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F792	12																																																				
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>TB</th> <th>TEB</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>↘</td> <td>0</td> <td>1</td> <td>1</td> <td colspan="2">Invert</td> </tr> <tr> <td>↗</td> <td>0</td> <td>1</td> <td>1</td> <td colspan="2">Hold</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td>1</td> <td colspan="2">Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>									TB	TEB	RB	SB	Q	QB	↘	0	1	1	Invert		↗	0	1	1	Hold		X	1	1	1	Hold		X	X	0	1	0	1	X	X	1	0	1	0	X	X	0	0	0	0
TB	TEB	RB	SB	Q	QB																																																	
↘	0	1	1	Invert																																																		
↗	0	1	1	Hold																																																		
X	1	1	1	Hold																																																		
X	X	0	1	0	1																																																	
X	X	1	0	1	0																																																	
X	X	0	0	0	0																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F792	TB	→	Q (LH)	0.492	0.826	1.629	0.011	0.015	0.022	TB	1.0	Q	33
			(LL)	0.432	0.702	1.309	0.010	0.013	0.018	TEB	1.7	QB	32
	TB	→	QB (LH)	0.599	1.006	1.984	0.011	0.015	0.021	RB	2.3		
			(LL)	0.626	1.057	2.075	0.010	0.013	0.017	SB	2.1		
	RB	→	Q (LL)	0.230	0.356	0.603	0.010	0.013	0.018				
	RB	→	QB (LH)	0.399	0.788	1.524	0.011	0.015	0.022				
	SB	→	Q (LH)	0.449	0.845	1.639	0.011	0.015	0.022				
	SB	→	QB (LL)	0.193	0.391	0.664	0.010	0.013	0.019				
	Set up time		TEB	0.850		1.850							
	Hold time		TEB	0.350		0.190							
	Release time		RB	0.180		0.000							
	Release time		SB	0.400		0.710							
	Removal time		RB	0.670		1.190							
	Removal time		SB	0.430		0.490							
Min Pulse		TB	0.824		2.395								
Min Pulse		RB	0.716		1.870								
Min Pulse		SB	0.739		1.985								

Chapter 2 Function Block

Function	JK-F/F																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F771	10	F771NQ	9	F771NB	9																																				
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F771	C → Q	(HH)		0.357	0.550	0.991	0.011	0.015	0.021	J	1.0	Q	35
		(HL)		0.398	0.647	1.202	0.010	0.013	0.017	K	1.0	QB	34
	C → QB	(HH)		0.534	0.876	1.663	0.011	0.015	0.021	C	1.0		
		(HL)		0.534	0.845	1.535	0.010	0.013	0.018				
	Set up time	J		0.680		1.360							
	Set up time	K		0.660		1.480							
	Hold time	J		0.200		0.000							
Hold time	K		0.250		0.000								
Min Pulse	C		0.719		2.032								
F771NQ	C → Q	(HH)		0.326	0.525	0.980	0.011	0.015	0.022	J	1.0	Q	33
		(HL)		0.332	0.530	0.944	0.011	0.014	0.020	K	1.0		
	Set up time	J		0.690		1.470				C	1.0		
	Set up time	K		0.660		1.300							
	Hold time	J		0.180		0.000							
Hold time	K		0.200		0.000								
Min Pulse	C		0.518		1.352								
F771NB	C → QB	(HH)		0.326	0.525	0.980	0.011	0.015	0.022	J	1.0	QB	33
		(HL)		0.332	0.530	0.944	0.011	0.014	0.020	K	1.0		
	Set up time	J		0.660		1.300				C	1.0		
	Set up time	K		0.660		1.470							
	Hold time	J		0.200		0.000							
Hold time	K		0.250		0.000								
Min Pulse	C		0.518		1.352								

Chapter 2 Function Block

Function	JK-F/F, High Speed																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F7D1	10																																								
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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Logic Diagram for "Q output"				Truth Table for "Q output"																																						
Logic Diagram for "QB output"				Truth Table for "QB output"																																						

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F7D1	C → Q	(HH)		0.333	0.534	0.993	0.011	0.015	0.022	J	1.0	Q	34
		(HL)		0.340	0.541	0.963	0.011	0.014	0.020	K	1.0	QB	35
	C → QB	(HH)		0.433	0.711	1.321	0.011	0.015	0.021	C	1.0		
		(HL)		0.458	0.743	1.396	0.010	0.013	0.017				
	Set up time	J		0.690		1.470							
	Set up time	K		0.660		1.290							
	Hold time	J		0.180		0.000							
Hold time	K		0.200		0.000								
Min Pulse	C		0.621		1.766								

Chapter 2 Function Block

Function	JK-F/F with R, S																																																																										
Block type	Standard type					Low Gate type																																																																					
	Normal		Q output		QB output		Normal		Q output		QB output																																																																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																															
Low Power																																																																											
x1	F774	12	F774NQ	11	F774NB	11																																																																					
x2																																																																											
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Logic Diagram for "Normal"			Truth Table for "Normal"																																																																								
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F774	C → Q	(HH)		0.374	0.575	1.040	0.011	0.015	0.021	J	1.0	Q	34
		(HL)		0.475	0.777	1.451	0.010	0.013	0.019	K	1.0	QB	34
	C → QB	(HH)		0.620	1.030	1.975	0.011	0.015	0.021	C	1.0		
		(HL)		0.662	1.059	1.944	0.011	0.014	0.020	R	2.1		
	R → Q	(HL)		0.417	0.776	1.463	0.010	0.013	0.018	S	2.2		
	R → QB	(HH)		0.227	0.393	0.683	0.011	0.015	0.022				
	S → Q	(HH)		0.170	0.251	0.426	0.011	0.015	0.022				
	S → QB	(HL)		0.457	0.904	1.664	0.011	0.015	0.022				
	Set up time	J		0.660		1.970							
	Set up time	K		0.660		1.600							
	Hold time	J		0.160		0.000							
	Hold time	K		0.230		0.000							
	Release time	R		0.380		1.210							
	Release time	S		0.110		0.000							
	Removal time	R		0.430		0.320							
	Removal time	S		0.760		1.220							
Min Pulse	C		0.861		2.344								
Min Pulse	R		0.779		1.990								
Min Pulse	S		0.689		2.031								
F774NQ	C → Q	(HH)		0.374	0.576	1.041	0.011	0.015	0.021	J	1.0	Q	35
		(HL)		0.473	0.777	1.451	0.010	0.013	0.019	K	1.0		
	R → Q	(HL)		0.414	0.712	1.338	0.010	0.013	0.018	C	1.0		
	S → Q	(HH)		0.170	0.251	0.426	0.011	0.015	0.022	R	2.1		
	Set up time	J		0.660		1.970				S	2.2		
	Set up time	K		0.660		1.600							
	Hold time	J		0.160		0.000							
	Hold time	K		0.230		0.000							
	Release time	R		0.380		1.210							
	Release time	S		0.110		0.000							
	Removal time	R		0.430		0.320							
	Removal time	S		0.760		1.220							
	Min Pulse	C		0.637		1.821							
	Min Pulse	R		0.687		1.826							
	Min Pulse	S		0.277		0.804							
	F774NB	C → QB	(HH)		0.328	0.527	0.981	0.011	0.015	0.022	J	1.0	QB
		(HL)		0.359	0.573	1.038	0.011	0.015	0.022	K	1.0		
R → QB		(HH)		0.276	0.466	0.866	0.011	0.015	0.022	C	1.0		
S → QB		(HL)		0.534	0.944	1.851	0.012	0.016	0.023	R	2.1		
Set up time		J		0.650		1.860				S	2.2		
Set up time		K		0.660		1.580							
Hold time		J		0.160		0.000							
Hold time		K		0.240		0.000							
Release time		R		0.400		1.110							
Release time		S		0.100		0.000							
Removal time		R		0.420		0.290							
Removal time		S		0.700		1.150							
Min Pulse		C		0.554		1.428							
Min Pulse		R		0.557		1.376							
Min Pulse		S		0.710		2.228							

Chapter 2 Function Block

Function	JK-F/F with RB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F775	11	F775NQ	10	F775NB	10																																																
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F775	C → Q	(HH)		0.401	0.636	1.214	0.011	0.015	0.022	J	1.0	Q	34
			(HL)	0.403	0.652	1.209	0.010	0.013	0.017	K	1.0	QB	34
			(LL)	0.587	0.945	1.798	0.010	0.013	0.018				
	C → QB	(HH)	0.544	0.888	1.678	0.011	0.015	0.021					
		(HL)	0.185	0.285	0.479	0.010	0.013	0.017	RB	2.2			
	RB → Q	(LL)	0.334	0.598	1.083	0.011	0.015	0.022					
		(LH)											
	Set up time	J		0.660		1.390							
	Set up time	K		0.660		1.540							
	Hold time	J		0.180		0.000							
	Hold time	K		0.240		0.000							
	Release time	RB		0.190		0.000							
	Removal time	RB		0.670		1.010							
	Min Pulse	C		0.774		2.181							
Min Pulse	RB		0.574		1.397								
F775NQ	C → Q	(HH)		0.401	0.637	1.216	0.011	0.015	0.022	J	1.0	Q	34
			(HL)	0.402	0.652	1.209	0.010	0.013	0.017	K	1.0		
			(LL)	0.185	0.285	0.480	0.010	0.013	0.017	C	1.0		
	RB → Q	(LL)	0.185	0.285	0.480	0.010	0.013	0.017					
		(LH)							RB	2.2			
	Set up time	J		0.660		1.390							
	Set up time	K		0.650		1.540							
	Hold time	J		0.180		0.000							
	Hold time	K		0.240		0.000							
	Release time	RB		0.190		0.000							
	Removal time	RB		0.670		1.010							
	Min Pulse	C		0.589		1.598							
	Min Pulse	RB		0.365		0.775							
	F775NB	C → QB	(HH)		0.330	0.529	0.987	0.011	0.015	0.022	J	1.0	QB
(HL)				0.334	0.526	0.928	0.011	0.014	0.020	K	1.0		
(LH)				0.348	0.711	1.374	0.011	0.015	0.022	C	1.0		
RB → QB		(LH)	0.348	0.711	1.374	0.011	0.015	0.022					
		(LL)							RB	2.2			
Set up time		J		0.650		1.360							
Set up time		K		0.660		1.530							
Hold time		J		0.180		0.000							
Hold time		K		0.240		0.000							
Release time		RB		0.180		0.000							
Removal time		RB		0.620		0.960							
Min Pulse		C		0.525		1.362							
Min Pulse		RB		0.602		1.674							

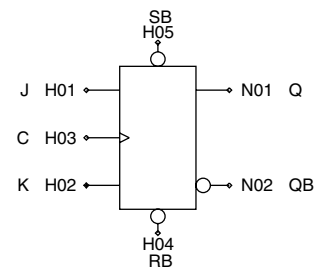
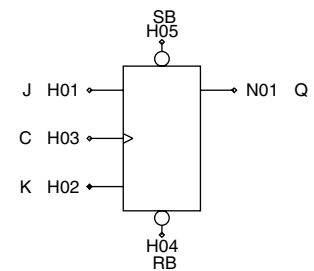
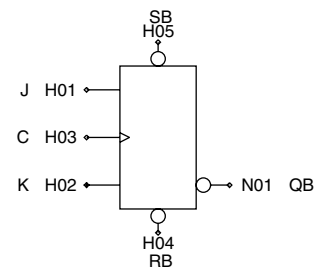
Chapter 2 Function Block

Function	JK-F/F with SB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F776	11	F776NQ	10	F776NB	10																																																
x2																																																						
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F776	C → Q	(HH)		0.375	0.579	1.044	0.011	0.015	0.021	J	1.0	Q	34
			(HL)	0.439	0.715	1.351	0.010	0.013	0.017	K	1.0	QB	33
			(LH)	0.634	1.060	2.100	0.011	0.015	0.022	C	1.0		
	SB → Q	(LH)		0.341	0.711	1.342	0.011	0.015	0.021	SB	2.1		
			(LL)	0.233	0.457	0.785	0.010	0.013	0.019				
	Set up time	J		0.730		1.340							
	Set up time	K		0.720		1.580							
	Hold time	J		0.200		0.000							
	Hold time	K		0.260		0.000							
	Release time	SB		0.430		0.540							
	Removal time	SB		0.370		0.390							
	Min Pulse	C		0.798		2.474							
	Min Pulse	SB		0.655		1.686							
	F776NQ	C → Q	(HH)		0.375	0.580	1.045	0.011	0.015	0.021	J	1.0	Q
(HL)				0.438	0.714	1.349	0.010	0.013	0.017	K	1.0		
(LH)				0.344	0.623	1.166	0.011	0.015	0.021	C	1.0		
SB → Q		(LH)		0.344	0.623	1.166	0.011	0.015	0.021	SB	2.1		
			(LL)	0.233	0.457	0.785	0.010	0.013	0.019				
Set up time		J		0.730		1.350							
Set up time		K		0.720		1.580							
Hold time		J		0.200		0.000							
Hold time		K		0.260		0.000							
Release time		SB		0.430		0.540							
Removal time		SB		0.370		0.390							
Min Pulse		C		0.603		1.723							
Min Pulse		SB		0.584		1.503							
F776NB		C → QB	(HH)		0.385	0.623	1.181	0.011	0.015	0.023	J	1.0	QB
	(HL)			0.357	0.572	1.026	0.011	0.014	0.019	K	1.0		
	(LH)			0.316	0.574	1.078	0.010	0.013	0.019	C	1.0		
	SB → QB	(LL)		0.316	0.574	1.078	0.010	0.013	0.019	SB	2.1		
			(LL)	0.233	0.457	0.785	0.010	0.013	0.019				
	Set up time	J		0.700		1.310							
	Set up time	K		0.730		1.600							
	Hold time	J		0.200		0.000							
	Hold time	K		0.260		0.000							
	Release time	SB		0.450		0.560							
	Removal time	SB		0.360		0.350							
	Min Pulse	C		0.551		1.556							
	Min Pulse	SB		0.565		1.424							

Chapter 2 Function Block

Function	JK-F/F with RB, SB																																																																										
Block type	Standard type					Low Gate type																																																																					
	Normal		Q output		QB output		Normal		Q output		QB output																																																																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																															
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F777	C → Q	(HH)		0.406	0.644	1.223	0.011	0.015	0.022	J	1.0	Q	34
		(HL)		0.422	0.686	1.291	0.010	0.013	0.017	K	1.0	QB	31
	C → QB	(HH)		0.631	1.057	2.095	0.011	0.015	0.022	C	1.0		
		(HL)		0.587	0.946	1.794	0.010	0.013	0.018	RB	2.3		
	RB → Q	(LL)		0.177	0.273	0.463	0.010	0.013	0.017	SB	2.1		
	RB → QB	(LH)		0.391	0.772	1.521	0.011	0.016	0.023				
	SB → Q	(LH)		0.378	0.809	1.571	0.011	0.015	0.022				
	SB → QB	(LL)		0.235	0.458	0.782	0.010	0.013	0.019				
	Set up time	J		0.720		1.380							
	Set up time	K		0.710		1.560							
	Hold time	J		0.190		0.000							
	Hold time	K		0.250		0.000							
	Release time	RB		0.180		0.000							
	Release time	SB		0.420		0.520							
	Removal time	RB		0.690		1.080							
	Removal time	SB		0.390		0.440							
Min Pulse	C		0.795		2.469								
Min Pulse	RB		0.672		1.830								
Min Pulse	SB		0.732		1.932								
F777NQ	C → Q	(HH)		0.406	0.644	1.224	0.011	0.015	0.022	J	1.0	Q	34
		(HL)		0.421	0.685	1.289	0.010	0.013	0.017	K	1.0		
	RB → Q	(LL)		0.177	0.273	0.463	0.010	0.013	0.017	C	1.0		
	SB → Q	(LH)		0.379	0.708	1.374	0.011	0.015	0.022	RB	2.3		
	Set up time	J		0.710		1.380				SB	2.1		
	Set up time	K		0.710		1.560							
	Hold time	J		0.190		0.000							
	Hold time	K		0.250		0.000							
	Release time	RB		0.180		0.000							
	Release time	SB		0.420		0.520							
	Removal time	RB		0.690		1.080							
	Removal time	SB		0.390		0.440							
	Min Pulse	C		0.587		1.665							
	Min Pulse	RB		0.351		0.752							
	Min Pulse	SB		0.655		1.723							
	F777NB	C → QB	(HH)		0.367	0.593	1.125	0.011	0.016	0.023	J	1.0	QB
		(HL)		0.336	0.533	0.943	0.011	0.014	0.020	K	1.0		
RB → QB		(LH)		0.432	0.869	1.774	0.011	0.016	0.023	C	1.0		
SB → QB		(LL)		0.293	0.536	0.991	0.011	0.014	0.020	RB	2.3		
Set up time		J		0.690		1.330				SB	2.1		
Set up time		K		0.720		1.590							
Hold time		J		0.190		0.000							
Hold time		K		0.260		0.000							
Release time		RB		0.160		0.000							
Release time		SB		0.430		0.550							
Removal time		RB		0.640		1.010							
Removal time		SB		0.380		0.400							
Min Pulse		C		0.533		1.500							
Min Pulse		RB		0.695		2.075							
Min Pulse		SB		0.553		1.336							

Chapter 2 Function Block

Function	JK-F/F (CB)																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F781	10	F781NQ	9	F781NB	9																																				
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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J	K	CB	Q	QB																																						
0	0	\	Hold																																							
0	1	\	0	1																																						
1	0	\	1	0																																						
1	1	\	Invert																																							
X	X	/	Hold																																							
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
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J	K	CB	Q																																							
0	0	\	Hold																																							
0	1	\	0																																							
1	0	\	1																																							
1	1	\	Invert																																							
X	X	/	Hold																																							
Logic Diagram for "QB output"				Truth Table for "QB output"																																						
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J	K	CB	QB																																							
0	0	\	Hold																																							
0	1	\	1																																							
1	0	\	0																																							
1	1	\	Invert																																							
X	X	/	Hold																																							

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F781	CB → Q	(LH)		0.372	0.622	1.190	0.011	0.015	0.021	J	1.0	Q	35
		(LL)		0.351	0.574	1.076	0.010	0.013	0.017	K	1.0	QB	34
		(LL)		0.549	0.916	1.737	0.010	0.013	0.018	CB	1.0		
	CB → QB	(LH)		0.489	0.807	1.543	0.011	0.015	0.021				
		(LL)		0.549	0.916	1.737	0.010	0.013	0.018				
			J		0.700		1.290						
			K		0.710		1.380						
	J		0.200		0.000								
	K		0.370		0.100								
	CB		0.748		2.056								
F781NQ	CB → Q	(LH)		0.290	0.473	0.897	0.011	0.015	0.022	J	1.0	Q	34
		(LL)		0.330	0.553	1.057	0.011	0.014	0.020	K	1.0	QB	34
	Set up time	J		0.720		1.470				CB	1.0		
		K		0.690		1.280							
	Hold time	J		0.310		0.000							
		K		0.190		0.000							
Min Pulse	CB		0.538		1.384								
F781NB	CB → QB	(LH)		0.290	0.473	0.897	0.011	0.015	0.022	J	1.0	QB	34
		(LL)		0.330	0.553	1.057	0.011	0.014	0.020	K	1.0	QB	34
	Set up time	J		0.690		1.280				CB	1.0		
		K		0.710		1.380							
	Hold time	J		0.190		0.000							
		K		0.370		0.110							
Min Pulse	CB		0.538		1.384								



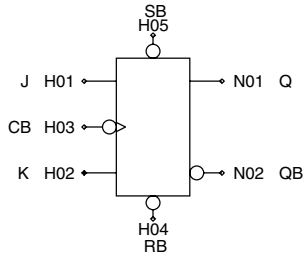
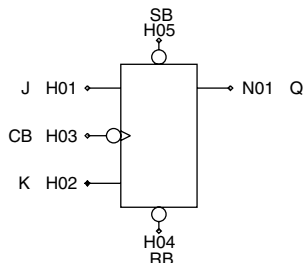
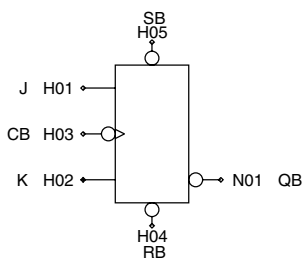
Chapter 2 Function Block

Function	JK-F/F (CB), High Speed																																									
Block type	Standard type					Low Gate type																																				
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F7E1	10																																								
x2																																										
x4																																										
Logic Diagram for "Normal"			Truth Table for "Normal"																																							
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J	K	CB	Q	QB																																						
0	0	\	Hold																																							
0	1	\	0	1																																						
1	0	\	1	0																																						
1	1	\	Invert																																							
X	X	/	Hold																																							
Logic Diagram for "Q output"			Truth Table for "Q output"																																							
Logic Diagram for "QB output"			Truth Table for "QB output"																																							

Chapter 2 Function Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F7E1	CB	→	Q (LH)	0.298	0.484	0.913	0.011	0.015	0.022	J	1.0	Q	34
			(LL)	0.337	0.561	1.067	0.011	0.014	0.020	K	1.0	QB	35
	CB	→	QB (LH)	0.431	0.732	1.428	0.011	0.015	0.021	CB	1.0		
			(LL)	0.423	0.693	1.315	0.010	0.013	0.017				
	Set up time		J	0.730		1.470							
	Set up time		K	0.690		1.270							
	Hold time		J	0.310		0.000							
Hold time		K	0.190		0.000								
Min Pulse		CB	0.642		1.754								

Chapter 2 Function Block

Function	JK-F/F (CB) with RB, SB																																																																										
Block type	Standard type					Low Gate type																																																																					
	Normal		Q output		QB output		Normal		Q output		QB output																																																																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																															
Low Power																																																																											
x1	F787	12	F787NQ	11	F787NB	11																																																																					
x2																																																																											
x4																																																																											
Logic Diagram for "Normal"			Truth Table for "Normal"																																																																								
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J	K	CB	RB	SB	Q	QB																																																																					
0	0	\	1	1	Hold																																																																						
0	1	\	1	1	0	1																																																																					
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Logic Diagram for "Q output"			Truth Table for "Q output"																																																																								
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Logic Diagram for "QB output"			Truth Table for "QB output"																																																																								
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F787	CB → Q	(LH)		0.421	0.716	1.419	0.011	0.015	0.022	J	1.0	Q	34
		(LL)		0.373	0.609	1.150	0.010	0.013	0.017	K	1.0	QB	31
	CB → QB	(LH)		0.584	0.983	1.962	0.011	0.015	0.022	CB	1.0		
		(LL)		0.600	1.016	1.986	0.010	0.013	0.018	RB	2.3		
	RB → Q	(LL)		0.177	0.273	0.463	0.010	0.013	0.017	SB	2.1		
		(LH)		0.391	0.772	1.520	0.011	0.016	0.023				
	SB → Q	(LH)		0.377	0.808	1.570	0.011	0.015	0.022				
		(LL)		0.235	0.458	0.783	0.010	0.013	0.019				
	Set up time	J		0.750		1.460							
	Set up time	K		0.740		1.680							
	Hold time	J		0.200		0.000							
	Hold time	K		0.370		0.110							
	Release time	RB		0.180		0.000							
	Release time	SB		0.390		0.700							
	Removal time	RB		0.670		1.180							
Removal time	SB		0.430		0.490								
Min Pulse	CB		0.798		2.307								
Min Pulse	RB		0.672		1.830								
Min Pulse	SB		0.732		1.932								
F787NQ	CB → Q	(LH)		0.420	0.716	1.417	0.011	0.015	0.022	J	1.0	Q	34
		(LL)		0.372	0.609	1.151	0.010	0.013	0.017	K	1.0		
	RB → Q	(LL)		0.177	0.273	0.463	0.010	0.013	0.017	CB	1.0		
		(LH)		0.379	0.709	1.374	0.011	0.015	0.022	RB	2.3		
	SB → Q	(LH)		0.379	0.709	1.374	0.011	0.015	0.022	SB	2.1		
		(LL)		0.235	0.458	0.783	0.010	0.013	0.019				
	Set up time	J		0.750		1.460							
	Set up time	K		0.740		1.680							
	Hold time	J		0.200		0.000							
	Hold time	K		0.370		0.110							
	Release time	RB		0.180		0.000							
	Release time	SB		0.390		0.700							
	Removal time	RB		0.670		1.190							
	Removal time	SB		0.430		0.490							
	Min Pulse	CB		0.620		1.737							
Min Pulse	RB		0.351		0.752								
Min Pulse	SB		0.655		1.724								
F787NB	CB → QB	(LH)		0.326	0.532	1.022	0.011	0.016	0.023	J	1.0	QB	31
		(LL)		0.331	0.553	1.051	0.011	0.014	0.020	K	1.0		
	RB → QB	(LH)		0.432	0.869	1.774	0.011	0.016	0.023	CB	1.0		
		(LL)		0.293	0.536	0.992	0.011	0.014	0.020	RB	2.3		
	SB → QB	(LH)		0.293	0.536	0.992	0.011	0.014	0.020	SB	2.1		
		(LL)		0.235	0.458	0.783	0.010	0.013	0.019				
	Set up time	J		0.730		1.440							
	Set up time	K		0.740		1.680							
	Hold time	J		0.190		0.000							
	Hold time	K		0.370		0.120							
	Release time	RB		0.170		0.000							
	Release time	SB		0.410		0.680							
	Removal time	RB		0.630		1.090							
	Removal time	SB		0.420		0.470							
	Min Pulse	CB		0.539		1.380							
Min Pulse	RB		0.695		2.074								
Min Pulse	SB		0.553		1.336								

# **Chapter 3**

## **Scan Path Block**

[MEMO]

### 3.1 Standard Type

Chapter 3 Scan Path Block

Function	Scan D-F/F with R, S, 2 to 1 Selector																																																																			
Block type	Standard type																																																																			
	Normal				Q output				QB output																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
x1	s000	12																																																																		
x2																																																																				
x4																																																																				
x8																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>S</th> <th>R</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>X</td> <td>0</td> <td>1</td> </tr> <tr> <td>A</td> <td>/</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>X</td> <td>\</td> <td>X</td> <td>0</td> <td>0</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>X</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									SIN	SCK	SMC	S	R	D	Q	QB	X	X	X	1	0	X	1	0	X	X	X	0	1	X	0	1	A	/	0	0	0	X	A	AB	X	/	1	0	0	B	B	BB	X	\	X	0	0	X	Hold		X	X	X	1	1	X	1	1
SIN	SCK	SMC	S	R	D	Q	QB																																																													
X	X	X	1	0	X	1	0																																																													
X	X	X	0	1	X	0	1																																																													
A	/	0	0	0	X	A	AB																																																													
X	/	1	0	0	B	B	BB																																																													
X	\	X	0	0	X	Hold																																																														
X	X	X	1	1	X	1	1																																																													
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S000	SCK	→	Q	(HH)	0.375	0.577	1.042	0.011	0.015	0.021	SIN	1.0	Q	35
				(HL)	0.476	0.780	1.456	0.010	0.013	0.019	SCK	1.0	QB	34
	SCK	→	QB	(HH)	0.570	0.956	1.848	0.011	0.015	0.021	SMC	1.0		
				(HL)	0.581	0.936	1.726	0.010	0.013	0.019	S	2.2		
	S	→	Q	(HH)	0.172	0.253	0.429	0.011	0.015	0.022	R	2.2		
				(HL)	0.378	0.780	1.439	0.010	0.014	0.021	D	1.0		
	R	→	Q	(HL)	0.418	0.717	1.357	0.010	0.013	0.018				
			QB	(HH)	0.183	0.334	0.581	0.011	0.015	0.022				
	Set up time		SIN		0.740		2.150							
	Set up time		SMC		0.730		2.300							
	Set up time		D		0.740		2.160							
	Hold time		SIN		0.260		0.000							
	Hold time		SMC		0.250		0.000							
	Hold time		D		0.260		0.000							
	Release time		S		0.110		0.000							
	Release time		R		0.380		1.230							
	Removal time		S		0.760		1.220							
	Removal time		R		0.430		0.320							
Min Pulse		SCK		0.783		2.217								
Min Pulse		S		0.613		1.811								
Min Pulse		R		0.679		1.841								

### Chapter 3 Scan Path Block

Function	Scan D-F/F with 2 to 1 Selector																																		
Block type	Standard type																																		
	Normal				Q output				QB output																										
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																							
Drivability																																			
x1	S002	10																																	
x2																																			
x4																																			
x8																																			
Logic Diagram for "Normal"				Truth Table for "Normal"																															
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>↗</td> <td>1</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>A</td> <td>↗</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>↘</td> <td>X</td> <td>X</td> <td></td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								SIN	SCK	SMC	D	Q	QB	X	↗	1	B	B	BB	A	↗	0	X	A	AB	X	↘	X	X		Hold
SIN	SCK	SMC	D	Q	QB																														
X	↗	1	B	B	BB																														
A	↗	0	X	A	AB																														
X	↘	X	X		Hold																														
Logic Diagram for "Q output"				Truth Table for "Q output"																															
Logic Diagram for "QB output"				Truth Table for "QB output"																															

### Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S002	SCK	→	Q (HH)	0.356	0.550	0.992	0.011	0.015	0.021	SIN	1.0	Q	35
			(HL)	0.399	0.648	1.205	0.010	0.013	0.017	SCK	1.0	QB	35
	SCK	→	QB (HH)	0.491	0.812	1.551	0.011	0.015	0.021	SMC	1.0		
			(HL)	0.482	0.765	1.400	0.010	0.013	0.017	D	1.0		
	Set up time		SIN	0.690		1.520							
	Set up time		SMC	0.690		1.660							
	Set up time		D	0.700		1.530							
	Hold time		SIN	0.250		0.000							
	Hold time		SMC	0.240		0.000							
	Hold time		D	0.250		0.000							
	Min Pulse		SCK	0.668		1.920							

Chapter 3 Scan Path Block

Function	Scan D-F/F with 2 to 1 Selector, High Speed																																		
Block type	Standard type																																		
	Normal				Q output				QB output																										
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																							
Drivability																																			
x1	S003	11																																	
x2																																			
x4																																			
x8																																			
Logic Diagram for "Normal"				Truth Table for "Normal"																															
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>↗</td> <td>1</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>A</td> <td>↗</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>↘</td> <td>X</td> <td>X</td> <td></td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								SIN	SCK	SMC	D	Q	QB	X	↗	1	B	B	BB	A	↗	0	X	A	AB	X	↘	X	X		Hold
SIN	SCK	SMC	D	Q	QB																														
X	↗	1	B	B	BB																														
A	↗	0	X	A	AB																														
X	↘	X	X		Hold																														
Logic Diagram for "Q output"				Truth Table for "Q output"																															
Logic Diagram for "QB output"				Truth Table for "QB output"																															

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S003	SCK	→	Q (HH)	0.325	0.525	0.980	0.011	0.015	0.022	SIN	1.0	Q	34
			(HL)	0.334	0.532	0.946	0.011	0.014	0.020	SCK	1.0	QB	35
	SCK	→	QB (HH)	0.428	0.702	1.304	0.011	0.015	0.021	SMC	1.0		
			(HL)	0.451	0.735	1.385	0.010	0.013	0.017	D	1.0		
	Set up time		SIN	0.720		1.590							
	Set up time		SMC	0.740		1.730							
	Set up time		D	0.710		1.570							
	Hold time		SIN	0.190		0.000							
	Hold time		SMC	0.200		0.000							
	Hold time		D	0.200		0.000							
Min Pulse		SCK	0.615		1.754								

Chapter 3 Scan Path Block

Function	Scan D-F/F with R, S, Hold, 2 to 1 Selector																																																																																			
Block type	Standard type																																																																																			
	Normal				Q output				QB output																																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																								
x1	S050	16																																																																																		
x2																																																																																				
x4																																																																																				
x8																																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																																
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>SDH</th> <th>S</th> <th>R</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>/</td> <td>X</td> <td>1</td> <td>0</td> <td>0</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>A</td> <td>/</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>X</td> <td>\</td> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>X</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>X</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									SIN	SCK	SMC	SDH	S	R	D	Q	QB	X	/	X	1	0	0	X	Hold		A	/	0	0	0	0	X	A	AB	X	/	1	0	0	0	B	B	BB	X	\	X	X	0	0	X	Hold		X	X	X	X	0	1	X	0	1	X	X	X	X	1	0	X	1	0	X	X	X	X	1	1	X	1	1
SIN	SCK	SMC	SDH	S	R	D	Q	QB																																																																												
X	/	X	1	0	0	X	Hold																																																																													
A	/	0	0	0	0	X	A	AB																																																																												
X	/	1	0	0	0	B	B	BB																																																																												
X	\	X	X	0	0	X	Hold																																																																													
X	X	X	X	0	1	X	0	1																																																																												
X	X	X	X	1	0	X	1	0																																																																												
X	X	X	X	1	1	X	1	1																																																																												
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDo (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S050	SCK → Q	(HH)		0.413	0.632	1.135	0.011	0.015	0.022	SIN	1.0	Q	34
		(HL)		0.542	0.880	1.626	0.011	0.014	0.020	SCK	1.0	QB	34
	SCK → QB	(HH)		0.636	1.063	2.036	0.011	0.015	0.021	SMC	1.0		
		(HL)		0.623	0.996	1.834	0.010	0.013	0.019	SDH	1.0		
	R → Q	(HL)		0.484	0.820	1.531	0.011	0.014	0.020	R	2.2		
		(HH)		0.183	0.334	0.581	0.011	0.015	0.022	S	2.4		
	S → Q	(HH)		0.207	0.297	0.499	0.011	0.015	0.022	D	1.0		
		(HL)		0.416	0.826	1.517	0.010	0.014	0.021				
	Set up time		SIN		0.900								
	Set up time		SMC		0.910								
	Set up time		SDH		0.760								
	Set up time		D		0.900								
	Hold time		SIN		0.070								
	Hold time		SMC		0.050								
	Hold time		SDH		0.180								
	Hold time		D		0.080								
	Release time		R		0.390								
	Release time		S		0.110								
	Removal time		R		0.430								
	Removal time		S		0.760								
Min Pulse		SCK		0.824									
Min Pulse		R		0.745									
Min Pulse		S		0.702									



Chapter 3 Scan Path Block

Function	Scan D-F/F with Hold, 2 to 1 Selector																																														
Block type	Standard type																																														
	Normal				Q output				QB output																																						
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																			
x1	S052	14																																													
x2																																															
x4																																															
x8																																															
Logic Diagram for "Normal"				Truth Table for "Normal"																																											
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>SDH</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>↗</td> <td>X</td> <td>1</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>A</td> <td>↗</td> <td>0</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>↗</td> <td>1</td> <td>0</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>X</td> <td>↘</td> <td>X</td> <td>X</td> <td>X</td> <td>Hold</td> <td></td> </tr> </tbody> </table> <p>X:Irrelevant</p>									SIN	SCK	SMC	SDH	D	Q	QB	X	↗	X	1	X	Hold		A	↗	0	0	X	A	AB	X	↗	1	0	B	B	BB	X	↘	X	X	X	Hold	
SIN	SCK	SMC	SDH	D	Q	QB																																									
X	↗	X	1	X	Hold																																										
A	↗	0	0	X	A	AB																																									
X	↗	1	0	B	B	BB																																									
X	↘	X	X	X	Hold																																										
Logic Diagram for "Q output"				Truth Table for "Q output"																																											
Logic Diagram for "QB output"				Truth Table for "QB output"																																											

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S052	SCK	→	Q (HH)	0.390	0.598	1.074	0.011	0.015	0.022	SIN	1.0	Q	35
			(HL)	0.438	0.709	1.306	0.010	0.013	0.018	SCK	1.0	QB	35
	SCK	→	QB (HH)	0.531	0.877	1.664	0.011	0.015	0.021	SMC	1.0		
			(HL)	0.516	0.815	1.489	0.010	0.013	0.017	SDH	1.0		
	Set up time		SIN	0.880		2.180				D	1.0		
	Set up time		SMC	0.880		2.330							
	Set up time		SDH	0.730		1.790							
	Set up time		D	0.870		2.170							
	Hold time		SIN	0.070		0.000							
	Hold time		SMC	0.040		0.000							
	Hold time		SDH	0.180		0.000							
	Hold time		D	0.070		0.000							
	Min Pulse		SCK	0.702		2.033							

Chapter 3 Scan Path Block

Function	Scan JK-F/F with R, S, D-F/F Function																																																																																																			
Block type	Standard type																																																																																																			
	Normal				Q output				QB output																																																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																								
x1	S100	14																																																																																																		
x2																																																																																																				
x4																																																																																																				
x8																																																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																																																
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SIN	SCK	SMC	S	R	J	K	Qn	QBn	Qn+1	QBn+1																																																																																										
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Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S100	SCK	→	Q	(HH)	0.375	0.576	1.041	0.011	0.015	0.021	SIN	1.0	Q	34
				(HL)	0.478	0.780	1.457	0.010	0.013	0.019	SCK	1.0	QB	33
	SCK	→	QB	(HH)	0.636	1.051	2.006	0.011	0.015	0.021	SMC	1.0		
				(HL)	0.686	1.094	1.993	0.011	0.014	0.021	S	2.2		
	S	→	Q	(HH)	0.172	0.253	0.429	0.011	0.015	0.022	R	2.2		
				(HL)	0.482	0.938	1.712	0.011	0.015	0.022	J	1.0		
	R	→	Q	(HL)	0.423	0.797	1.492	0.010	0.013	0.018	K	1.0		
				(HH)	0.239	0.407	0.703	0.011	0.015	0.022				
	Set up time		SIN		0.730		2.140							
	Set up time		SMC		0.790		2.550							
	Set up time		J		0.780		2.540							
	Set up time		K		0.790		2.160							
	Hold time		SIN		0.270		0.000							
	Hold time		SMC		0.250		0.000							
	Hold time		J		0.040		0.000							
	Hold time		K		0.040		0.000							
	Release time		S		0.110		0.000							
	Release time		R		0.380		1.220							
Removal time		S		0.750		1.210								
Removal time		R		0.430		0.320								
Min Pulse		SCK		0.886		2.387								
Min Pulse		S		0.715		2.078								
Min Pulse		R		0.806		2.027								

Chapter 3 Scan Path Block

Function	Scan JK-F/F with D-F/F Function																																																								
Block type	Standard type																																																								
	Normal				Q output				QB output																																																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																													
x1	S102	12																																																							
x2																																																									
x4																																																									
x8																																																									
Logic Diagram for "Normal"				Truth Table for "Normal"																																																					
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SIN	SCK	SMC	J	K	Qn	QBn	Qn+1	QBn+1																																																	
A	/	0	X	X	X	X	A	AB																																																	
X	/	1	B	X	0	1	B	BB																																																	
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Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S102	SCK	→	Q (HH)	0.358	0.550	0.992	0.011	0.015	0.021	SIN	1.0	Q	35
			(HL)	0.401	0.650	1.207	0.010	0.013	0.017	SCK	1.0	QB	34
	SCK	→	QB (HH)	0.540	0.883	1.673	0.011	0.015	0.021	SMC	1.0		
			(HL)	0.539	0.851	1.544	0.010	0.013	0.018	J	1.0		
	Set up time		SIN	0.700		1.530				K	1.0		
	Set up time		SMC	0.740		1.930							
	Set up time		J	0.810		1.920							
	Set up time		K	0.810		2.020							
	Hold time		SIN	0.250		0.000							
	Hold time		SMC	0.240		0.000							
	Hold time		J	0.060		0.000							
	Hold time		K	0.050		0.000							
	Min Pulse		SCK	0.724		2.042							

Chapter 3 Scan Path Block

Function	Scan JK-F/F with R, S, Hold, D-F/F Function																																																																																																																							
Block type	Standard type																																																																																																																							
	Normal				Q output				QB output																																																																																																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																																												
x1	S150	18																																																																																																																						
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SIN	SCK	SMC	SDH	S	R	J	K	Qn	QBn	Qn+1	QBn+1																																																																																																													
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Logic Diagram for "QB output"				Truth Table for "QB output"																																																																																																																				

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S150	SCK → Q	(HH)		0.376	0.577	1.041	0.011	0.015	0.021	SIN	1.0	Q	35
		(HL)		0.480	0.783	1.459	0.010	0.013	0.019	SCK	1.0	QB	33
	SCK → QB	(HH)		0.662	1.090	2.075	0.011	0.015	0.021	SMC	1.0		
		(HL)		0.732	1.165	2.119	0.011	0.015	0.021	SDH	1.0		
	R → Q	(HL)		0.425	0.832	1.556	0.010	0.013	0.019	R	2.2		
		(HH)		0.259	0.438	0.757	0.011	0.015	0.022	S	2.3		
	S → Q	(HH)		0.172	0.253	0.429	0.011	0.015	0.022	J	1.0		
		(HL)		0.527	1.009	1.842	0.011	0.016	0.023	K	1.0		
	Set up time		SIN		0.900								
	Set up time		SMC		0.930								
	Set up time		SDH		0.710								
	Set up time		J		0.940								
	Set up time		K		0.980								
	Hold time		SIN		0.070								
	Hold time		SMC		0.040								
	Hold time		SDH		0.240								
	Hold time		J		0.000								
	Hold time		K		0.000								
	Release time		R		0.380								
	Release time		S		0.110								
Removal time		R		0.430									
Removal time		S		0.740									
Min Pulse		SCK		0.931									
Min Pulse		R		0.854									
Min Pulse		S		0.759									

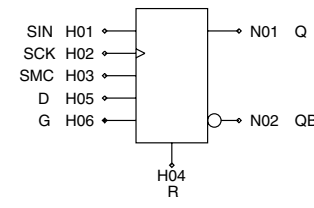
Chapter 3 Scan Path Block

Function	Scan JK-F/F with Hold, D-F/F Function																																																																							
Block type	Standard type																																																																							
	Normal				Q output				QB output																																																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																												
x1	S152	16																																																																						
x2																																																																								
x4																																																																								
x8																																																																								
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																				
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SIN	SCK	SMC	SDH	J	K	Qn	QBn	Qn+1	QBn+1																																																															
X	/	X	1	X	X	X	X	A	Hold																																																															
A	/	0	0	X	X	X	X	B	AB																																																															
X	/	1	0	B	X	0	1	B	BB																																																															
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X	\	X	X	X	X	X	X	X	Hold																																																															
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																				
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																				

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S152	SCK	→	Q (HH)	0.357	0.550	0.991	0.011	0.015	0.021	SIN	1.0	Q	35
			(HL)	0.402	0.652	1.210	0.010	0.013	0.017	SCK	1.0	QB	34
			(LL)	0.571	0.899	1.624	0.010	0.013	0.019	SDH	1.0		
	Set up time		SIN	0.870		2.190				J	1.0		
	Set up time		SMC	0.900		2.430				K	1.0		
	Set up time		SDH	0.680		1.610							
	Set up time		J	0.950		2.410							
	Set up time		K	0.990		2.560							
	Hold time		SIN	0.060		0.000							
	Hold time		SMC	0.030		0.000							
	Hold time		SDH	0.230		0.000							
	Hold time		J	0.000		0.000							
	Hold time		K	0.000		0.000							
	Min Pulse		SCK	0.758		2.109							

Chapter 3 Scan Path Block

Function	Scan D-Latch with R, D-F/F Function																																																																			
Block type	Standard type																																																																			
	Normal				Q output				QB output																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
x1	S201	13																																																																		
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SIN	SCK	SMC	R	D	G	Q	QB																																																													
X	X	X	1	X	X	0	1																																																													
A	/	0	0	X	X	A	AB																																																													
X	\	0	0	X	X		Hold																																																													
X	X	1	0	B	1	B	BB																																																													
X	X	1	0	X	0		Latch																																																													
X	1	Down	0	1	1	X	X																																																													
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S201	SCK → Q	(HH)		0.726	1.200	2.338	0.011	0.015	0.021	SIN	1.0	Q	35
		(HL)		0.619	0.988	1.848	0.010	0.013	0.017	SCK	1.0	QB	34
	SCK → QB	(HH)		0.490	0.767	1.432	0.011	0.015	0.021	SMC	1.0		
		(HL)		0.619	1.006	1.926	0.010	0.013	0.019	R	2.1		
	R → Q	(HL)		0.366	0.578	1.038	0.010	0.013	0.018	D	1.0		
		(HH)		0.177	0.259	0.437	0.011	0.015	0.021	G	1.0		
	R → QB	(HH)		0.631	1.035	2.028	0.011	0.015	0.021				
		(LL)		0.533	0.924	1.827	0.010	0.013	0.017				
	D → Q	(HL)		0.522	0.841	1.615	0.010	0.013	0.019				
		(LH)		0.403	0.702	1.404	0.011	0.015	0.021				
	D → QB	(HH)		0.720	1.194	2.334	0.011	0.015	0.021				
		(HL)		0.616	0.986	1.851	0.010	0.013	0.017				
	G → Q	(HH)		0.486	0.765	1.435	0.011	0.015	0.021				
		(HL)		0.612	1.001	1.922	0.010	0.013	0.019				
	Set up time	SIN		0.540		2.080							
	Set up time	SMC		0.950		1.860							
	Set up time	D		0.640		1.210							
	Hold time	SIN		0.440		0.460							
	Hold time	SMC		0.000		0.000							
	Hold time	D		0.200		0.000							
Release time	R		0.350		0.690								
Removal time	R		0.550		0.730								
Min Pulse	SCK		0.995		2.805								
Min Pulse	R		0.485		1.420								
Min Pulse	G		0.981		2.796								

Chapter 3 Scan Path Block

Function	Scan D-Latch with D-F/F Function																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	S202	12																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>D</th> <th>G</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>/</td> <td>0</td> <td>X</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>\</td> <td>0</td> <td>X</td> <td>X</td> <td></td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>B</td> <td>1</td> <td>B</td> <td>BB</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>X</td> <td>0</td> <td></td> <td>Latch</td> </tr> <tr> <td>X</td> <td>1</td> <td>Down</td> <td>1</td> <td>1</td> <td>X</td> <td>X</td> </tr> </tbody> </table> <p>X:Irrelevant ← Prohibition</p>									SIN	SCK	SMC	D	G	Q	QB	A	/	0	X	X	A	AB	X	\	0	X	X		Hold	X	X	1	B	1	B	BB	X	X	1	X	0		Latch	X	1	Down	1	1	X	X
SIN	SCK	SMC	D	G	Q	QB																																																
A	/	0	X	X	A	AB																																																
X	\	0	X	X		Hold																																																
X	X	1	B	1	B	BB																																																
X	X	1	X	0		Latch																																																
X	1	Down	1	1	X	X																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output						
	Path			t LDO (ns)			t 1										
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout				
S202	SCK	→	Q	(HH)	0.625	1.029	2.007	0.011	0.015	0.021	SIN	1.0	Q	35			
				(HL)	0.607	0.964	1.810	0.010	0.013	0.017		SCK		1.0	QB	34	
	SCK	→	QB	(HH)	0.484	0.752	1.405	0.011	0.015	0.021	SMC	1.0	D	1.0			
				(HL)	0.535	0.866	1.663	0.010	0.013	0.017		D		1.0			
	D	→	Q	(HH)	0.522	0.857	1.678	0.011	0.015	0.021	G	1.0	G	1.0			
				(LL)	0.530	0.921	1.822	0.010	0.013	0.017							
	D	→	QB	(HL)	0.430	0.692	1.331	0.010	0.013	0.017	(LH)	0.405	0.705	1.410	0.011	0.015	0.021
				(HH)	0.618	1.023	2.002	0.011	0.015	0.021							
	G	→	Q	(HL)	0.610	0.968	1.821	0.010	0.013	0.017	(HH)	0.487	0.755	1.415	0.011	0.015	0.021
				(HL)	0.527	0.860	1.658	0.010	0.013	0.017							
	Set up time		SIN		0.470		2.050										
	Set up time		SMC		0.960		1.860										
	Set up time		D		0.620		1.220										
	Hold time		SIN		0.460		0.480										
	Hold time		SMC		0.000		0.000										
	Hold time		D		0.270		0.090										
Min Pulse		SCK		0.912		2.474											
Min Pulse		G		0.912		2.466											

Chapter 3 Scan Path Block

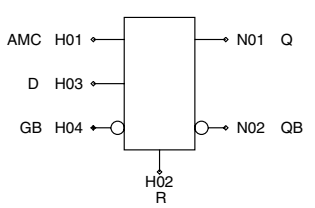
Function	Scan D-Latch with D-F/F Function, High Speed																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	S204	12																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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SIN	SCK	SMC	D	G	Q	QB																																																
A	/	0	X	X	A	AB																																																
X	\	0	X	X		Hold																																																
X	X	1	B	1	B	BB																																																
X	X	1	X	0		Latch																																																
X	1	Down	1	1	X	X																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S204	SCK	→	Q	(HH)	0.477	0.767	1.485	0.011	0.016	0.023	SIN	1.0	Q	31
				(HL)	0.464	0.757	1.423	0.012	0.015	0.022	SCK	1.0	QB	34
	SCK	→	QB	(HH)	0.562	0.942	1.828	0.011	0.015	0.020	SMC	1.0	D	1.0
				(HL)	0.611	0.991	1.924	0.010	0.012	0.017				
	D	→	Q	(HH)	0.371	0.595	1.163	0.011	0.016	0.023	G	1.0		
				(LL)	0.378	0.652	1.304	0.012	0.016	0.023				
	D	→	QB	(HL)	0.506	0.821	1.608	0.010	0.012	0.017				
				(LH)	0.480	0.848	1.742	0.011	0.015	0.020				
	G	→	Q	(HH)	0.470	0.762	1.480	0.011	0.016	0.023				
				(HL)	0.466	0.762	1.438	0.012	0.015	0.022				
	G	→	QB	(HH)	0.565	0.948	1.846	0.011	0.015	0.020				
				(HL)	0.604	0.985	1.919	0.010	0.012	0.017				
		Set up time		SIN	0.470		1.890							
		Set up time		SMC	0.970		2.100							
		Set up time		D	0.670		1.480							
		Hold time		SIN	0.460		0.490							
	Hold time		SMC	0.000		0.000								
	Hold time		D	0.280		0.030								
	Min Pulse		SCK	0.882		2.392								
	Min Pulse		G	0.869		2.382								



Chapter 3 Scan Path Block

Function	Scan D-Latch with R, Special Function, R																																																																	
Block type	Standard type																																																																	
	Normal				Q output				QB output																																																									
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																						
Drivability																																																																		
x1	S301	8																																																																
x2																																																																		
x4																																																																		
x8																																																																		
Logic Diagram for "Normal"				Truth Table for "Normal"																																																														
				<table border="1"> <thead> <tr> <th>AMC</th> <th>R</th> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>1</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									AMC	R	D	GB	Q	QB	1	0	0	0	0	1	1	0	1	0	1	0	1	0	X	1	Latch		X	1	X	X	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0	1	1	1	0
AMC	R	D	GB	Q	QB																																																													
1	0	0	0	0	1																																																													
1	0	1	0	1	0																																																													
1	0	X	1	Latch																																																														
X	1	X	X	0	1																																																													
0	0	0	0	0	1																																																													
0	0	0	1	0	1																																																													
0	0	1	0	0	1																																																													
0	0	1	1	1	0																																																													
Logic Diagram for "Q output"				Truth Table for "Q output"																																																														
Logic Diagram for "QB output"				Truth Table for "QB output"																																																														

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S301	AMC → Q	(HH)		0.555	0.937	1.857	0.011	0.015	0.021	AMC	1.8	Q	35	
		(LH)		0.553	0.944	1.884	0.011	0.015	0.021					
	AMC → QB	(HL)		0.445	0.740	1.440	0.010	0.013	0.019	R	1.0	QB	34	
		(LH)		0.447	0.742	1.339	0.011	0.015	0.021					
	R → Q	(HL)		0.442	0.747	1.466	0.010	0.013	0.019	D	1.0			
		(LH)		0.307	0.479	0.860	0.010	0.013	0.017					
	R → QB	(HH)		0.349	0.590	1.199	0.011	0.015	0.021	GB	2.0			
		(LL)		0.176	0.257	0.436	0.011	0.015	0.022					
	D → Q	(HH)		0.239	0.394	0.785	0.010	0.013	0.019					
		(LL)		0.573	0.945	1.872	0.011	0.015	0.021					
	D → QB	(HL)		0.414	0.709	1.364	0.010	0.013	0.017					
		(LH)		0.462	0.748	1.456	0.010	0.013	0.019					
	GB → Q	(HH)		0.283	0.487	0.943	0.011	0.015	0.021					
		(LH)		0.598	1.018	2.091	0.011	0.015	0.021					
	GB → QB	(HH)		0.561	0.937	1.797	0.011	0.015	0.021					
		(LL)		0.443	1.057	1.961	0.010	0.013	0.017					
	Set up time	D			0.710		1.390							
					0.340		0.100							
	Hold time	D			0.440		0.580							
					0.370		0.240							
Release time	R			0.622		1.417								
				0.799		2.360								
Min Pulse	GB													

Chapter 3 Scan Path Block

Function	Scan D-Latch with Special Function																																																			
Block type	Standard type																																																			
	Normal				Q output				QB output																																											
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																								
Drivability																																																				
x1	S302	7																																																		
x2																																																				
x4																																																				
x8																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																
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AMC	D	GB	Q	QB																																																
1	0	0	0	1																																																
1	1	0	1	0																																																
1	X	1	Latch																																																	
0	0	0	0	1																																																
0	0	1	0	1																																																
0	1	0	0	1																																																
0	1	1	1	0																																																
				X:Irrelevant																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output										
	Path			t LDO (ns)			t 1															
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout									
S302	AMC → Q	(HH)		0.456	0.767	1.527	0.011	0.015	0.021	AMC	1.8	Q	35									
		(LH)		0.455	0.774	1.553	0.011	0.015	0.021													
	AMC → QB	(HL)		0.360	0.597	1.174	0.010	0.013	0.017					D	1.0	QB	34					
		(LH)		0.456	0.750	1.346	0.011	0.015	0.021													
	D → Q	(LL)		0.359	0.604	1.197	0.010	0.013	0.017									GB	2.0			
		(HH)		0.474	0.776	1.540	0.011	0.015	0.021													
	D → QB	(LL)		0.410	0.702	1.351	0.010	0.013	0.017													
		(HL)		0.378	0.606	1.187	0.010	0.013	0.017													
	GB → Q	(HH)		0.283	0.483	0.934	0.011	0.015	0.021													
		(LH)		0.496	0.845	1.753	0.011	0.015	0.021													
	GB → QB	(LL)		0.464	0.769	1.472	0.011	0.015	0.021													
		(HL)		0.438	1.063	1.966	0.010	0.013	0.017													
			(HL)		0.400	0.675	1.398	0.010	0.013	0.017												
			(LH)		0.311	0.839	1.542	0.011	0.015	0.021												
			(LL)		0.369	0.600	1.116	0.010	0.013	0.017												
		Set up time	D		0.650		1.150															
		Hold time	D		0.340		0.090															
		Min Pulse	GB		0.832		2.238															

Chapter 3 Scan Path Block

Function	Scan D-Latch with Special Function, High Speed																																																			
Block type	Standard type																																																			
	Normal				Q output				QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																								
x1	S303	7																																																		
x2																																																				
x4																																																				
x8																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																
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AMC	D	GB	Q	QB																																																
1	0	0	0	1																																																
1	1	0	1	0																																																
1	X	1	Latch																																																	
0	0	0	0	1																																																
0	0	1	0	1																																																
0	1	0	0	1																																																
0	1	1	1	0																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output								
	Path			t LDO (ns)			t 1												
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout						
S303	AMC	→ Q	(HH)	0.306	0.507	1.018	0.011	0.016	0.023	AMC	1.8	Q	31						
			(LH)	0.309	0.522	1.058	0.011	0.016	0.023										
		(LL)	0.453	0.732	1.290	0.012	0.016	0.023											
	AMC	→ QB	(HL)	0.437	0.727	1.452	0.010	0.012	0.017			D		1.0	QB	34			
			(LH)	0.559	0.928	1.720	0.011	0.015	0.020										
		(LL)	0.441	0.744	1.497	0.010	0.012	0.017											
	D	→ Q	(HH)	0.324	0.513	1.028	0.011	0.016	0.023	GB	2.0								
			(LL)	0.253	0.426	0.814	0.011	0.014	0.020										
	D	→ QB	(HL)	0.456	0.735	1.463	0.010	0.012	0.017				D				1.0		
			(LH)	0.347	0.597	1.178	0.011	0.015	0.021										
	GB	→ Q	(HH)	0.347	0.586	1.252	0.011	0.016	0.023			GB		2.0					
			(LH)	0.317	0.514	0.971	0.011	0.016	0.023										
	GB	→ QB	(LL)	0.295	0.799	1.473	0.011	0.015	0.022	GB	2.0								
			(HL)	0.481	0.811	1.697	0.010	0.012	0.017										
	GB	→ QB	(LH)	0.366	1.020	1.921	0.011	0.015	0.021				GB		2.0				
			(LL)	0.449	0.734	1.404	0.010	0.012	0.017										
	Set up time		D	0.720	1.380														
	Hold time		D	0.320	0.080														
Min Pulse		GB	0.809	2.198															

[MEMO]

[MEMO]

[MEMO]

## 3.2 NEC Scan

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch																											
Block type	Standard type																											
	Normal				Q output				QB output																			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Drivability																												
x1	SE601	13																										
x2																												
x4																												
x8																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	Q	QB	0	1	0	1	1	1	1	0	X	0	Latch	
D	G	Q	QB																									
0	1	0	1																									
1	1	1	0																									
X	0	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SE601	D	→	Q (HH)	0.589	0.972	1.872	0.011	0.015	0.021	D	1.0	Q	34	
			(LL)	0.575	0.962	1.860	0.010	0.013	0.017					
	D	→	QB (HL)	0.460	0.747	1.410	0.011	0.014	0.020	G	2.0	QB	34	
			(LH)	0.420	0.705	1.369	0.011	0.015	0.022					
	G	→	Q (HH)	0.466	0.770	1.492	0.011	0.015	0.021					
			(HL)	0.488	0.793	1.525	0.010	0.013	0.017					
	G	→	QB (HH)	0.334	0.539	1.038	0.011	0.015	0.022					
			(HL)	0.342	0.555	1.052	0.011	0.014	0.020					
	Set up time		D		0.930		1.930							
	Hold time		D		0.010		0.000							
Min Pulse		G		0.848		2.151								

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch with R																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
x1	SE602	14																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>R</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	R	Q	QB	1	1	0	1	0	0	1	0	0	1	X	0	0	Latch		X	X	1	0	1
D	G	R	Q	QB																																	
1	1	0	1	0																																	
0	1	0	0	1																																	
X	0	0	Latch																																		
X	X	1	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output				
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
SE602	D	→	Q	(HH)	0.725	1.215	2.371	0.011	0.015	0.020	D	1.0	Q	34	
				(LL)	0.571	0.959	1.860	0.010	0.013	0.017					
	D	→	QB	(HL)	0.590	0.972	1.846	0.012	0.016	0.023	G	1.9	QB	34	
				(LH)	0.416	0.702	1.370	0.011	0.015	0.022					
	G	→	Q	(HH)	0.485	0.808	1.595	0.011	0.015	0.021	R	2.5			
				(HL)	0.485	0.790	1.520	0.010	0.013	0.017					
	G	→	QB	(HH)	0.332	0.536	1.034	0.011	0.015	0.022					
				(HL)	0.359	0.581	1.113	0.012	0.015	0.022					
	R	→	Q	(HL)	0.413	0.690	1.304	0.010	0.013	0.017					
				(LH)	0.553	0.965	1.965	0.011	0.015	0.020					
	R	→	QB	(HH)	0.266	0.446	0.831	0.011	0.015	0.022					
				(LL)	0.419	0.723	1.441	0.012	0.016	0.023					
	Set up time	D			1.080		2.490								
	Hold time	D			0.020		0.000								
	Release time	R			0.890		1.980								
	Removal time	R			0.000		0.000								
Min Pulse	G			0.862		2.197									
Min Pulse	R			0.865		2.225									

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch with RB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Drivability																																					
x1	SE603	14																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	RB	Q	QB	1	1	1	1	0	0	1	1	0	1	X	0	1	Latch		X	X	0	0	1
D	G	RB	Q	QB																																	
1	1	1	1	0																																	
0	1	1	0	1																																	
X	0	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE603	D → Q	(HH)		0.572	0.953	1.871	0.011	0.015	0.022	D	1.0	Q	33
				0.512	0.858	1.650	0.010	0.013	0.018				
	D → QB	(HL)		0.717	1.201	2.347	0.011	0.013	0.018	G	1.9	QB	35
				0.619	1.044	2.033	0.011	0.015	0.021				
	G → Q	(HH)		0.451	0.727	1.430	0.011	0.015	0.022	RB	2.5		
				0.429	0.698	1.330	0.010	0.013	0.018				
	G → QB	(HH)		0.535	0.883	1.710	0.011	0.015	0.021				
				0.596	0.975	1.905	0.011	0.013	0.018				
	RB → Q	(HH)		0.221	0.345	0.689	0.011	0.015	0.022				
				0.203	0.315	0.536	0.010	0.013	0.018				
	RB → QB	(HL)		0.366	0.592	1.163	0.011	0.013	0.018				
				0.311	0.584	1.064	0.011	0.015	0.021				
	Set up time	D		0.930		1.920							
	Hold time	D		0.050		0.000							
Release time	RB		0.520		0.580								
Removal time	RB		0.310		0.290								
Min Pulse	G		0.958		2.443								
Min Pulse	RB		0.613		1.451								



Chapter 3 Scan Path Block

Function	NEC Scan D-Latch(GB)																											
Block type	Standard type																											
	Normal				Q output				QB output																			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Drivability																												
x1	SE604	13																										
x2																												
x4																												
x8																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	Q	QB	1	0	1	0	0	0	0	1	X	1	Latch	
D	GB	Q	QB																									
1	0	1	0																									
0	0	0	1																									
X	1	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
SE604	D	→	Q	(HH)	0.587	0.968	1.865	0.011	0.015	0.021	D	1.0	Q	34	
				(LL)	0.576	0.965	1.867	0.010	0.013	0.017			GB	2.0	QB
	D	→	QB	(HL)	0.459	0.745	1.404	0.011	0.014	0.020					
				(LH)	0.421	0.708	1.376	0.011	0.015	0.022					
	GB	→	Q	(LH)	0.497	0.838	1.623	0.011	0.015	0.021					
				(LL)	0.496	0.811	1.561	0.010	0.013	0.017					
	GB	→	QB	(LH)	0.342	0.556	1.071	0.011	0.015	0.022					
				(LL)	0.371	0.619	1.183	0.011	0.014	0.020					
	Set up time		D		0.870		1.780								
	Hold time		D		0.000		0.000								
Min Pulse		GB		0.902		2.122									

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch(GB) with RB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
x1	SE605	14																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	QB	1	0	1	1	0	0	0	1	0	1	X	1	1	Latch		X	X	0	0	1
D	GB	RB	Q	QB																																	
1	0	1	1	0																																	
0	0	1	0	1																																	
X	1	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output				
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
SE605	D	→	Q	(HH)	0.571	0.952	1.869	0.011	0.015	0.022	D	1.0	Q	33	
				(LL)	0.512	0.859	1.654	0.010	0.013	0.018					
	D	→	QB	(HL)	0.716	1.199	2.346	0.011	0.013	0.018	GB	2.0	QB	33	
				(LH)	0.619	1.045	2.035	0.011	0.015	0.021					
	GB	→	Q	(LH)	0.487	0.816	1.624	0.011	0.015	0.022	RB	2.5			
				(LL)	0.431	0.702	1.328	0.010	0.013	0.018					
	GB	→	QB	(LH)	0.536	0.886	1.710	0.011	0.015	0.021					
				(LL)	0.632	1.062	2.099	0.011	0.013	0.018					
	RB	→	Q	(HH)	0.221	0.345	0.689	0.011	0.015	0.022					
				(LL)	0.203	0.315	0.536	0.010	0.013	0.018					
	RB	→	QB	(HL)	0.366	0.592	1.164	0.011	0.013	0.018					
				(LH)	0.311	0.584	1.064	0.011	0.015	0.021					
	Set up time		D		0.850		1.780								
	Hold time		D		0.010		0.000								
Release time		RB		0.480		0.480									
Removal time		RB		0.340		0.370									
Min Pulse		GB		0.999		2.517									
Min Pulse		RB		0.613		1.451									

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F																											
Block type	Standard type																											
	Normal				Q output				QB output																			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
x1	SE611	11																										
x2																												
x4																												
x8																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↘</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	Q	QB	0	↗	0	1	1	↘	1	0	X	↘	Hold	
D	C	Q	QB																									
0	↗	0	1																									
1	↘	1	0																									
X	↘	Hold																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SE611	C → Q	(HH)		0.382	0.600	1.120	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.411	0.666	1.272	0.010	0.013	0.017	C	2.4	QB	35
	C → QB	(HH)		0.522	0.860	1.671	0.011	0.015	0.021				
		(HL)		0.531	0.852	1.596	0.010	0.013	0.018				
	Set up time		D		0.620		1.200						
	Hold time		D		0.280		0.210						
Min Pulse		C		0.924		2.263							

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with R, S																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Drivability																																																						
x1	SE614	13																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>R</th> <th>S</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>/</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>/</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>\</td> <td>0</td> <td>0</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>									D	C	R	S	Q	QB	0	/	0	0	0	1	1	/	0	0	1	0	X	\	0	0	Hold		X	X	0	1	1	0	X	X	1	0	0	1	X	X	1	1	1	1
D	C	R	S	Q	QB																																																	
0	/	0	0	0	1																																																	
1	/	0	0	1	0																																																	
X	\	0	0	Hold																																																		
X	X	0	1	1	0																																																	
X	X	1	0	0	1																																																	
X	X	1	1	1	1																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE614	C → Q	(HH)		0.387	0.616	1.158	0.011	0.015	0.021	D	1.0	Q	35
		(HL)		0.483	0.792	1.512	0.010	0.013	0.019	C	2.5	QB	34
	C → QB	(HH)		0.602	1.008	1.972	0.011	0.015	0.021	R	2.2		
		(HL)		0.634	1.039	1.960	0.011	0.014	0.019	S	2.4		
	R → Q	(HL)		0.424	0.751	1.420	0.010	0.013	0.018				
	R → QB	(HH)		0.203	0.361	0.629	0.011	0.015	0.022				
	S → Q	(HH)		0.173	0.254	0.429	0.011	0.015	0.022				
	S → QB	(HL)		0.418	0.844	1.558	0.011	0.015	0.021				
	Set up time		D		0.670		1.790						
	Hold time		D		0.300		0.230						
	Release time		R		0.470		1.280						
	Release time		S		0.200		0.130						
	Removal time		R		0.350		0.110						
	Removal time		S		0.630		0.980						
Min Pulse		C		1.041		2.653							
Min Pulse		R		0.726		1.923							
Min Pulse		S		0.706		2.098							

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with RB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Drivability																																					
x1	SE615	12																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↗</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	RB	Q	QB	0	↗	1	0	1	1	↗	1	1	0	X	↘	1	Hold		X	X	0	0	1
D	C	RB	Q	QB																																	
0	↗	1	0	1																																	
1	↗	1	1	0																																	
X	↘	1	Hold																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE615	C → Q	(HH)		0.439	0.705	1.369	0.011	0.015	0.022	D	1.0	Q	34
		(HL)		0.419	0.677	1.288	0.010	0.013	0.017	C	2.5	QB	34
	C → QB	(HH)		0.534	0.875	1.694	0.011	0.015	0.021	RB	2.6		
		(HL)		0.591	0.966	1.874	0.010	0.013	0.017				
	RB → Q	(LL)		0.181	0.281	0.474	0.010	0.013	0.017				
	RB → QB	(LH)		0.300	0.565	1.025	0.011	0.015	0.021				
	Set up time		D	0.630		1.360							
	Hold time		D	0.300		0.230							
	Release time		RB	0.320		0.350							
	Removal time		RB	0.510		0.710							
	Min Pulse		C	0.977		2.498							
	Min Pulse		RB	0.562		1.401							

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with SB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Drivability																																					
x1	SE616	12																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↗</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X: Irrelevant</p>									D	C	SB	Q	QB	0	↗	1	0	1	1	↗	1	1	0	X	↘	1	Hold		X	X	0	1	0
D	C	SB	Q	QB																																	
0	↗	1	0	1																																	
1	↗	1	1	0																																	
X	↘	1	Hold																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.					MAX.
SE616	C → Q	(HH)		0.385	0.604	1.126	0.011	0.015	0.022	D	1.0	Q	34
		(HL)		0.430	0.702	1.354	0.011	0.013	0.018	C	2.5	QB	33
	C → QB	(HH)		0.607	1.023	2.062	0.011	0.015	0.022	SB	2.3		
		(HL)		0.533	0.855	1.599	0.010	0.013	0.017				
	SB → Q	(LH)		0.341	0.661	1.254	0.011	0.015	0.022				
	SB → QB	(LL)		0.207	0.415	0.713	0.010	0.013	0.018				
	Set up time		D	0.640		1.390							
	Hold time		D	0.250		0.180							
	Release time		SB	0.470		0.720							
	Removal time		SB	0.340		0.290							
	Min Pulse		C	0.964		2.672							
	Min Pulse		SB	0.611		1.590							

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with RB, SB																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	SE617	13																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>/</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>/</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>\</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									D	C	RB	SB	Q	QB	0	/	1	1	0	1	1	/	1	1	1	0	X	\	1	1	Hold		X	X	0	1	0	1	X	X	1	0	1	0	X	X	0	0	0	0
D	C	RB	SB	Q	QB																																																	
0	/	1	1	0	1																																																	
1	/	1	1	1	0																																																	
X	\	1	1	Hold																																																		
X	X	0	1	0	1																																																	
X	X	1	0	1	0																																																	
X	X	0	0	0	0																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
SE617	C → Q	(HH)		0.424	0.686	1.340	0.011	0.015	0.022	D	1.0	Q	34	
		(HL)		0.423	0.693	1.337	0.010	0.013	0.017	C	2.5	QB	32	
	C → QB	(HH)		0.599	1.011	2.044	0.011	0.015	0.022	RB	2.4			
		(HL)		0.576	0.946	1.840	0.010	0.013	0.017	SB	2.2			
	RB → Q	(LL)		0.176	0.274	0.463	0.010	0.013	0.017					
	RB → QB	(LH)		0.356	0.721	1.421	0.011	0.015	0.022					
	SB → Q	(LH)		0.382	0.766	1.506	0.011	0.015	0.022					
	SB → QB	(LL)		0.210	0.417	0.717	0.010	0.013	0.019					
	Set up time		D		0.630		1.350							
	Hold time		D		0.260		0.180							
	Release time		RB		0.280		0.290							
	Release time		SB		0.450		0.680							
	Removal time		RB		0.560		0.840							
	Removal time		SB		0.360		0.330							
Min Pulse		C		0.957		2.651								
Min Pulse		RB		0.660		1.824								
Min Pulse		SB		0.691		1.857								

### Chapter 3 Scan Path Block

Function	NEC Scan D-F/F (CB)																										
Block type	Standard type																										
	Normal				Q output				QB output																		
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells															
Drivability																											
x1	SE631	11																									
x2																											
x4																											
x8																											
Logic Diagram for "Normal"				Truth Table for "Normal"																							
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								D	CB	Q	QB	0	\	0	1	1	\	1	0	X	/	Hold	
D	CB	Q	QB																								
0	\	0	1																								
1	\	1	0																								
X	/	Hold																									
Logic Diagram for "Q output"				Truth Table for "Q output"																							
Logic Diagram for "QB output"				Truth Table for "QB output"																							

### Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SE631	CB	→	Q (LH)	0.412	0.681	1.304	0.011	0.015	0.021	D	1.0	Q	35
			(LL)	0.405	0.659	1.254	0.010	0.013	0.017			CB	2.3
	CB	→	QB (LH)	0.516	0.854	1.655	0.011	0.015	0.021				
			(LL)	0.561	0.933	1.780	0.010	0.013	0.018				
	Set up time		D	0.610		1.150							
Hold time		D	0.270		0.250								
Min Pulse		CB	0.958		2.297								



Chapter 3 Scan Path Block

Function	NEC Scan D-F/F (CB) with RB, SB																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	SE637	13																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									D	CB	RB	SB	Q	QB	0	\	1	1	0	1	1	\	1	1	1	0	X	/	1	1	Hold		X	X	0	1	0	1	X	X	1	0	1	0	X	X	0	0	0	0
D	CB	RB	SB	Q	QB																																																	
0	\	1	1	0	1																																																	
1	\	1	1	1	0																																																	
X	/	1	1	Hold																																																		
X	X	0	1	0	1																																																	
X	X	1	0	1	0																																																	
X	X	0	0	0	0																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE637	CB → Q	(LH)		0.453	0.762	1.513	0.011	0.015	0.022	D	1.0	Q	34
		(LL)		0.418	0.684	1.313	0.010	0.013	0.017	CB	2.5	QB	32
	CB → QB	(LH)		0.593	1.002	2.023	0.011	0.015	0.022	RB	2.4		
		(LL)		0.604	1.021	2.011	0.010	0.013	0.017	SB	2.2		
	RB → Q	(LH)		0.176	0.274	0.463	0.010	0.013	0.017				
		(LL)		0.176	0.274	0.463	0.010	0.013	0.017				
	RB → QB	(LH)		0.356	0.720	1.419	0.011	0.015	0.022				
		(LL)		0.356	0.720	1.419	0.011	0.015	0.022				
	SB → Q	(LH)		0.381	0.766	1.506	0.011	0.015	0.022				
		(LL)		0.381	0.766	1.506	0.011	0.015	0.022				
	SB → QB	(LH)		0.210	0.417	0.717	0.010	0.013	0.019				
		(LL)		0.210	0.417	0.717	0.010	0.013	0.019				
	Set up time		D		0.650		1.440						
	Hold time		D		0.290		0.260						
Release time		RB		0.280		0.240							
Release time		SB		0.450		0.760							
Removal time		RB		0.550		0.920							
Removal time		SB		0.370		0.330							
Min Pulse		CB		0.994		2.534							
Min Pulse		RB		0.660		1.823							
Min Pulse		SB		0.692		1.858							

[MEMO]

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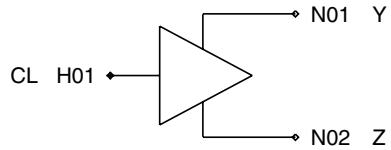
[MEMO]

### 3.3 Scan Controller

### Chapter 3 Scan Path Block

Function	Clock Distributor											
Block type	Standard type											
	Normal			High speed								
Drivability	Name	cells	Name	cells								
x1	SCD1	8										
x2												
x4												
x8												

Logic Diagram



Truth Table

CL	Y	Z
1	1	1
0	0	0

Y: Must be connected to the clock of Negative edge triggered F/F or the gate of Low enable Latch  
 Z: Must be connected to the clock of Positive edge triggered F/F or the gate of High enable Latch

### Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SCD1	CL	→	Y (HH)	0.215	0.327	0.590	0.011	0.015	0.022	CL	2.1	Y	34
			(LL)	0.224	0.365	0.684	0.010	0.013	0.019			Z	34
	CL	→	Z (HH)	0.214	0.326	0.589	0.011	0.015	0.022				
			(LL)	0.223	0.364	0.683	0.010	0.013	0.019				

### Chapter 3 Scan Path Block

Function	Clock Distributor with Test (Positive Clock)									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SCDC	2								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    CL_H01[CL H01] --> Buffer[ ]
    Buffer --> N01_Y[N01 Y]
  
```

Truth Table

CL	Y
1	1
0	0

### Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SCDC	CL	→ Y	(HH) 0.133	(LL) 0.208	0.204 0.320	0.345 0.579	0.011 0.010	0.015 0.013	0.021 0.018	CL	1.0	Y	35

Chapter 3 Scan Path Block

Function	Clock Distributor with Test (Negative Clock)									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SCDD	2								
x2										
x4										
x8										

Logic Diagram

```

    graph LR
      CL_H01[CL H01] --> Buffer[ ]
      Buffer --> N01_Y[N01 Y]
  
```

Truth Table

CL	Y
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output	
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SCDD	CL	→ Y	(HH) 0.184	(HH) 0.274	(HH) 0.499	(LL) 0.011	(LL) 0.015	(LL) 0.022	CL	1.0	Y	34

Chapter 3 Scan Path Block

Function	I/F Control (AMC) with EN									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SFEH	3								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    D_H01[D H01] --> Inverter[ ]
    Inverter --> N01_EN[N01 EN]
  
```

Truth Table

D	EN
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SFEH	D	→ EN	(HH) (LL)	0.184 0.133	0.274 0.212	0.498 0.380	0.011 0.010	0.015 0.012	0.022 0.017	D	1.0	EN	34

Chapter 3 Scan Path Block

Function	I/F Control (AMC) with ENB																
Block type	Standard type																
	Normal		High speed														
Drivability	Name	cells	Name	cells													
x1	SFEL	2															
x2																	
x4																	
x8																	
<p>Logic Diagram</p> <pre> graph LR     D_H01[D H01] --&gt; Inverter[ ]     Inverter --&gt; N01_ENB[N01 ENB]     </pre>																	
<p>Truth Table</p> <table border="1"> <thead> <tr> <th>D</th> <th>ENB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>												D	ENB	1	1	0	0
D	ENB																
1	1																
0	0																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output	
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SFEL	D → ENB (HH) (LL)		0.133	0.204	0.345	0.011	0.015	0.021	D	1.0	ENB	35



Chapter 3 Scan Path Block

Function	I/F Control (SMC) with EN									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SOEH	3								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    D_H01[D H01] --> Inverter[ ]
    Inverter --> N01_EN[N01 EN]
  
```

Truth Table

D	EN
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SOEH	D	→ EN	(HH) 0.184	(LL) 0.133	0.274 0.212	0.498 0.380	0.011 0.010	0.015 0.012	0.022 0.017	D	1.0	EN	34

Chapter 3 Scan Path Block

Function	I/F Control (SMC) with ENB									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SOEL	2								
x2										
x4										
x8										

Logic Diagram

```

    graph LR
      D_H01[D H01] --> Buffer[ ]
      Buffer --> N01_ENB[N01 ENB]
  
```

Truth Table

D	ENB
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SOEL	D → ENB		(HH)	0.133	0.204	0.345	0.011	0.015	0.021	D	1.0	ENB	35
			(LL)	0.208	0.320	0.579	0.010	0.013	0.018				

Chapter 3 Scan Path Block

Function	Mega Macro Skip									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SMS1	4								
x2										
x4										
x8										

Logic Diagram

```

    graph LR
      A[A H01] --> Block[ ]
      B[B H02] --> Block
      Block --> Y[N01 Y]
  
```

Truth Table

A	Y
1	1
0	0

Note:H02 is a pin of scan

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SMS1	A → Y												
			(HH)	0.229	0.347	0.633	0.011	0.015	0.022	A	1.0	Y	34
			(LL)	0.234	0.389	0.733	0.010	0.013	0.019	B	1.0		

Chapter 3 Scan Path Block

Function	Set/Reset Control									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SRH1	2								
x2										
x4										
x8										

Logic Diagram

```

    graph LR
      A[SET H01] --> B[ ]
      B --> C[N01 S]
  
```

Truth Table

SET	S
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output		
	Path			t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	SET	1.0	S	34	
SRH1	SET	→	S	(HH) 0.184	(LL) 0.132	0.274 0.213	0.499 0.380	0.011 0.010	0.015 0.012	0.022 0.017	SET	1.0	S	34

Chapter 3 Scan Path Block

Function	Set-B/Reset-B Control									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SRL1	2								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    A[SETB H01] --> B[ ]
    B --> C[N01 S]
    style B fill:none,stroke:none
  
```

Truth Table

SETB	S
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output		
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	SETB	1.0	S	35	
SRL1	SETB	→	S	(HH) 0.133	(LL) 0.208	0.204 0.320	0.345 0.579	0.011 0.010	0.015 0.013	0.021 0.018				

Chapter 3 Scan Path Block

Function	Loop Cut										
Block type	Standard type										
	Normal		High speed								
Drivability	Name	cells	Name	cells							
x1	SRPD	12									
x2											
x4											
x8											

Logic Diagram

```

    graph LR
      RIN_H01[RIN H01] --> Inverter[ ]
      Inverter --> N01_ROUT[N01 ROUT]
  
```

Truth Table

RIN	ROUT
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed							Input		Output		
	Path		t LDo (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SRPD	RIN	→ ROUT (HH) (LL)	0.312	0.471	0.864	0.011	0.015	0.022	RIN	1.0	ROUT	33

### Chapter 3 Scan Path Block

Function	Clock Generator												
Block type	Standard type												
	Normal		High speed										
Drivability	Name	cells	Name	cells									
x1	SCKG	16											
x2													
x4													
x8													

Logic Diagram

```

graph LR
    CL_H01[CL H01] --> Block[ ]
    Block --> N01_SC[N01 SC]
  
```

Truth Table

CL	SC
1	1
0	0

### Chapter 3 Scan Path Block

Block type	Switching speed							Input		Output			
	Path			t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	CL	2.1	SC	34
SCKG													

Chapter 3 Scan Path Block

Function	Common Input									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	sci1	2								
x2										
x4										
x8										

Logic Diagram

Truth Table

A	Y
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SCI1	A	→ Y	(HH) (LL)	0.143 0.143	0.208 0.219	0.343 0.385	0.011 0.010	0.015 0.012	0.021 0.017	A	1.0	Y	35



Chapter 3 Scan Path Block

Function	Common Output											
Block type	Standard type											
	Normal			High speed								
Drivability	Name	cells	Name	cells								
x1	SCO1	4										
x2												
x4												
x8												

Logic Diagram

```

graph LR
    A[A H01] --> Buffer[ ]
    Buffer --> Y[N01 Y]
  
```

Truth Table

A	Y
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SCO1	A	→ Y	(HH) (LL)	0.228 0.234	0.346 0.388	0.633 0.732	0.011 0.010	0.015 0.013	0.022 0.019	A	1.0	Y	34

Chapter 3 Scan Path Block

Function	GND										
Block type	Standard type										
	Normal		High speed								
Drivability	Name	cells	Name	cells							
x1	SGND	2									
x2											
x4											
x8											

Logic Diagram

Truth Table

Y
0

Chapter 3 Scan Path Block

Block type	Switching speed							Input		Output		
	Path		t LDo (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			Y	35
SGND												

# **Chapter 4**

## **Boundary Scan Block**

[MEMO]

## 4.1 TAP Macro

### Chapter 4 Boundary Scan Block

Function	BScan TAP Macro										
Block type	Standard type										
	-	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells							
	-	SBCJ	262								

Logic Diagram

Equivalent Circuit

### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output	
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBCJ												

### Chapter 4 Boundary Scan Block

Function	BScan TAP Macro with NEC Scan									
Block type	Standard type									
Drivability	Name	cells	Name	cells						
-	SBCL	315								

Logic Diagram

Equivalent Circuit

### Chapter 4 Boundary Scan Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBCL													

[MEMO]

[MEMO]

[MEMO]

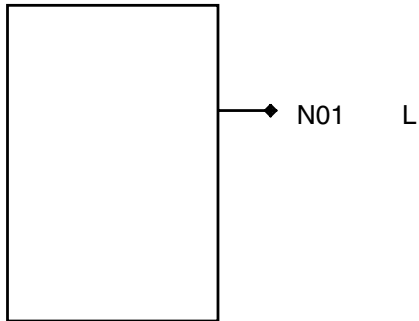
## 4.2 Level Generator



Chapter 4 Boundary Scan Block

Function	BScan Level Generator (CLANP)										
Block type	Standard type										
	-	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells							
-	SBZ1	1									
-											

Logic Diagram



Truth Table

L
0

Chapter 4 Boundary Scan Block

Block type	Switching speed							Input		Output		
	Path		t LDo (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			L	152
SBZ1												

[MEMO]

[MEMO]

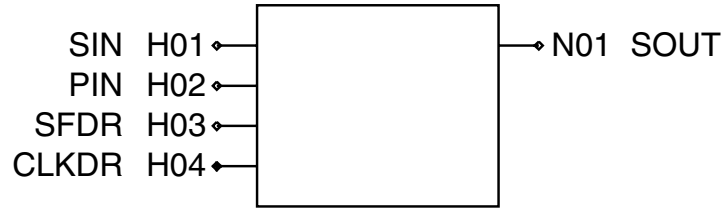
[MEMO]

### 4.3 Data Register

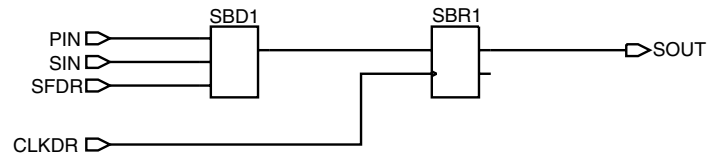
Chapter 4 Boundary Scan Block

Function	BScan Data Register for Input												
Block type	Standard type												
	-	-	-	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells									
-	SVRN12	12											
-													

Logic Diagram



Equivalent Circuit



Chapter 4 Boundary Scan Block

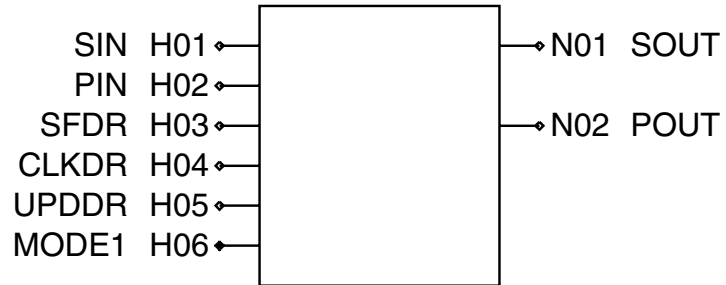
Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				

SVRN12

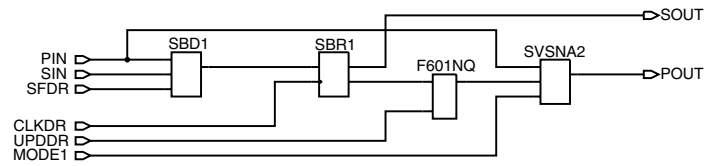
### Chapter 4 Boundary Scan Block

Function	BScan Data Register for Output									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SVRN22	24								
-										

Logic Diagram



Equivalent Circuit



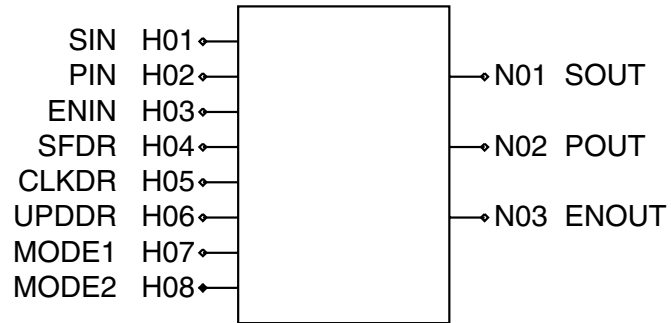
### Chapter 4 Boundary Scan Block

Block type	Switching speed						Input		Output			
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SVRN22												

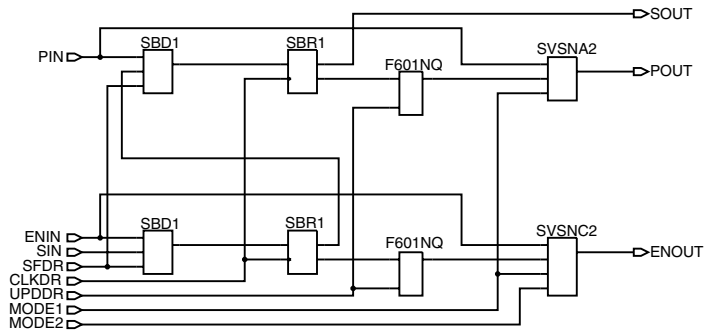
### Chapter 4 Boundary Scan Block

Function	BScan Data Register for 3-state									
Block type	Standard type									
	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells						
	-	SVRN32	50							

Logic Diagram



Equivalent Circuit



### Chapter 4 Boundary Scan Block

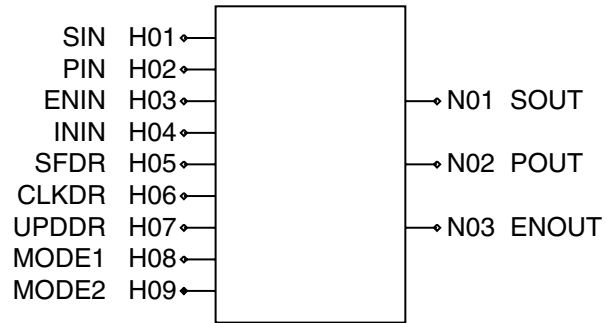
Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				

SVRN32

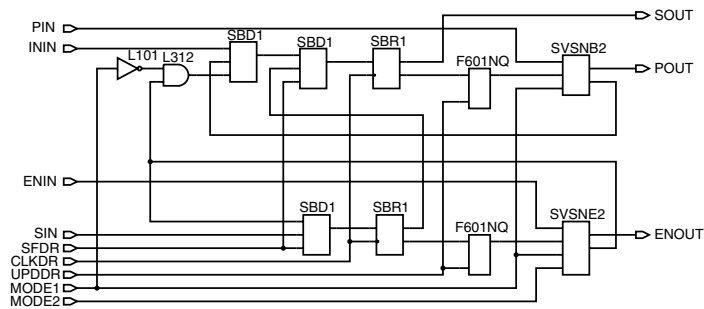
### Chapter 4 Boundary Scan Block

Function	BScan Data Register for Bid									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SVRNB2	57								
-										

Logic Diagram



Equivalent Circuit



### Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SVRNB2													

[MEMO]

[MEMO]



[MEMO]

#### 4.4 D-latch, Selector, Shift Register

### Chapter 4 Boundary Scan Block

Function	BScan D-Latch with SB Q Out, Low Power									
Block type	Standard type									
Drivability	Name	cells	Name	cells						
-	L606	5								

Logic Diagram

Truth Table

D	C	SB	Q
1	0	1	1
0	0	1	0
X	1	1	Latch
X	X	0	1

X:Irrelevant

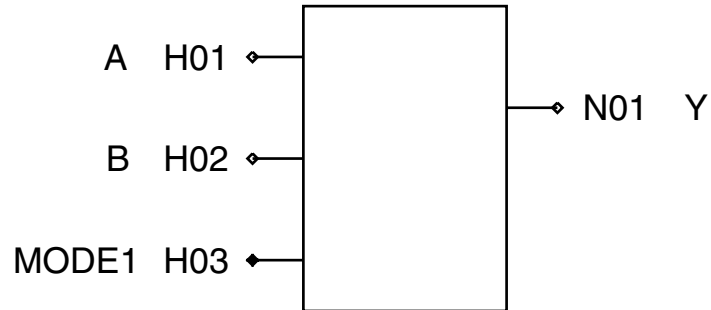
### Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L606	D	→	Q	(HH)	0.193	0.314	0.581	0.022	0.030	0.042	D	3.9	Q	16
				(LL)	0.240	0.409	0.834	0.020	0.026	0.036	C	1.0		
	C	→	Q	(HH)	0.304	0.480	0.870	0.022	0.030	0.042	SB	1.0		
				(HL)	0.394	0.658	1.256	0.020	0.026	0.036				
	SB	→	Q	(HL)	0.289	0.468	0.852	0.020	0.026	0.036				
				(LH)	0.205	0.331	0.603	0.022	0.030	0.043				
	Set up time		D		0.460		0.610							
	Hold time		D		0.370		0.400							
	Release time		SB		0.430		0.540							
	Removal time		SB		0.380		0.340							
	Min Pulse		C		0.527		1.581							
	Min Pulse		SB		0.433		1.135							

Chapter 4 Boundary Scan Block

Function	BScan Selector									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SBD1	4								
-										

Logic Diagram



Truth Table

A	B	MODE1	Y
A	X	0	A
X	B	1	B

X : Irrelevant

Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBD1	A	→	Y (HH)	0.218	0.335	0.606	0.021	0.029	0.042	A	1.0	Y	16
				0.232	0.384	0.724	0.020	0.025	0.034				
	B	→	Y (HH)	0.222	0.340	0.614	0.021	0.029	0.042	B	1.0		
				0.237	0.390	0.733	0.020	0.025	0.034				
	MODE1	→	Y (HH)	0.258	0.420	0.784	0.021	0.029	0.042	MODE1	1.0		
				0.267	0.416	0.734	0.020	0.025	0.034				
				0.231	0.374	0.700	0.021	0.029	0.042				
				0.271	0.454	0.863	0.020	0.025	0.034				

Chapter 4 Boundary Scan Block

Function	BScan Shift Register									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SBR1	8								
Logic Diagram										
Truth Table										
D	C	Q	U							
A	/	A	Hold							
B	\	Hold	B							
X : Irrelevant										

Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBR1	C	→	Q (LH)	0.345	0.586	1.126	0.020	0.028	0.038	D	3.8	Q	15
			(LL)	0.317	0.521	0.993	0.019	0.023	0.031	C	1.0	U	13
	C	→	U (HH)	0.503	0.824	1.549	0.022	0.030	0.042				
			(HL)	0.494	0.785	1.440	0.020	0.025	0.035				
	Set up time		D	0.270		0.160							
Hold time		D	0.650		1.200								
Min Pulse		C	0.672		1.900								

Chapter 4 Boundary Scan Block

Function	BScan Data Selector for Output																					
Block type	Standard type																					
	-		-																			
Drivability	Name	cells	Name	cells																		
-	SVSNA2	7																				
Logic Diagram																						
Truth Table																						
<table border="1"> <thead> <tr> <th>PIN</th> <th>BSCAN</th> <th>MODE1</th> <th>POUT</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>X</td> <td>0</td> <td>A</td> </tr> <tr> <td>X</td> <td>B</td> <td>1</td> <td>B</td> </tr> </tbody> </table>											PIN	BSCAN	MODE1	POUT	A	X	0	A	X	B	1	B
PIN	BSCAN	MODE1	POUT																			
A	X	0	A																			
X	B	1	B																			
X : Irrelevant																						

Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SVSNA2	PIN → POUT	(HH)		0.169	0.270	0.496	0.006	0.008	0.011	PIN	4.1	POUT	65
		(LL)		0.170	0.286	0.558	0.005	0.007	0.009				
	BSCAN → POUT	(HH)		0.290	0.438	0.802	0.006	0.008	0.011	BSCAN	1.0		
		(LL)		0.296	0.487	0.926	0.006	0.007	0.010				
		(HL)		0.318	0.513	0.962	0.006	0.008	0.011				
	MODE1 → POUT	(HH)		0.318	0.513	0.962	0.006	0.008	0.011	MODE1	1.0		
		(HL)		0.318	0.519	0.972	0.006	0.007	0.010				
		(LH)		0.260	0.414	0.768	0.006	0.008	0.011				
		(LL)		0.276	0.459	0.876	0.005	0.007	0.009				

Chapter 4 Boundary Scan Block

Function	BScan Data Selector for Bid																								
Block type	Standard type																								
	-		-																						
Drivability	Name	cells	Name	cells																					
-	SVSNB2	7																							
Logic Diagram																									
Truth Table																									
<table border="1"> <thead> <tr> <th>PIN</th> <th>BSCAN</th> <th>MODE1</th> <th>POUT</th> <th>Z1</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>X</td> <td>0</td> <td>A</td> <td>A</td> </tr> <tr> <td>X</td> <td>B</td> <td>1</td> <td>B</td> <td>B</td> </tr> </tbody> </table>											PIN	BSCAN	MODE1	POUT	Z1	A	X	0	A	A	X	B	1	B	B
PIN	BSCAN	MODE1	POUT	Z1																					
A	X	0	A	A																					
X	B	1	B	B																					
X : Irrelevant																									

Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SVSNB2	PIN	→	POUT (HH)	0.185	0.294	0.540	0.006	0.008	0.011	PIN	4.1	POUT	64
				0.184	0.310	0.606	0.005	0.007	0.009				
	PIN	→	Z1 (HH)	0.205	0.334	0.631	0.021	0.029	0.042	BSCAN	1.0	Z1	15
				0.226	0.392	0.782	0.020	0.025	0.033				
	BSCAN	→	POUT (HH)	0.311	0.473	0.870	0.006	0.008	0.011	MODE1	1.0		
				0.320	0.527	1.005	0.006	0.007	0.011				
	BSCAN	→	Z1 (HH)	0.332	0.522	0.992	0.021	0.030	0.042				
				0.374	0.637	1.242	0.020	0.025	0.034				
	MODE1	→	POUT (HH)	0.339	0.546	1.028	0.006	0.008	0.011				
				0.339	0.556	1.051	0.006	0.007	0.011				
	MODE1	→	Z1 (HL)	0.276	0.439	0.816	0.006	0.008	0.011				
				0.290	0.483	0.922	0.005	0.007	0.009				
	MODE1	→	Z1 (HL)	0.361	0.597	1.150	0.022	0.030	0.042				
				0.398	0.671	1.294	0.020	0.025	0.034				
	MODE1	→	Z1 (LH)	0.295	0.479	0.906	0.021	0.029	0.042				
0.332				0.565	1.098	0.020	0.025	0.033					

Chapter 4 Boundary Scan Block

Function	BScan Data Enable Selector for 3-state																													
Block type	Standard type																													
	-		-																											
Drivability	Name	cells	Name	cells																										
-	SVSNC2	9																												
Logic Diagram																														
Truth Table																														
<table border="1"> <thead> <tr> <th>ENIN</th> <th>BSCAN</th> <th>MODE1</th> <th>MODE2</th> <th>ENOUT</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>X</td> <td>0</td> <td>0</td> <td>A</td> </tr> <tr> <td>X</td> <td>B</td> <td>1</td> <td>0</td> <td>B</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> </tr> </tbody> </table>											ENIN	BSCAN	MODE1	MODE2	ENOUT	A	X	0	0	A	X	B	1	0	B	X	X	X	1	0
ENIN	BSCAN	MODE1	MODE2	ENOUT																										
A	X	0	0	A																										
X	B	1	0	B																										
X	X	X	1	0																										
X : Irrelevant																														

Chapter 4 Boundary Scan Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SVSNC2	ENIN	→	ENOUT (HH)	0.201	0.329	0.625	0.009	0.013	0.020	ENIN	4.1	ENOUT	33
			(LL)	0.188	0.322	0.634	0.005	0.007	0.010				
	BSCAN	→	ENOUT (HH)	0.325	0.499	0.934	0.009	0.013	0.020	MODE1	1.0		
			(LL)	0.309	0.518	0.999	0.006	0.008	0.011				
	MODE1	→	ENOUT (HH)	0.353	0.574	1.094	0.009	0.013	0.020	MODE2	4.2		
			(HL)	0.334	0.553	1.050	0.006	0.008	0.011				
			(LH)	0.291	0.472	0.896	0.009	0.013	0.019				
			(LL)	0.294	0.495	0.950	0.005	0.007	0.010				
	MODE2	→	ENOUT (HL)	0.083	0.120	0.180	0.005	0.006	0.008				
			(LH)	0.081	0.122	0.235	0.009	0.013	0.020				

Chapter 4 Boundary Scan Block

Function	BScan Data Enable Selector for Bid									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SVSNE2	9								

Logic Diagram

Truth Table

ENIN	BSCAN	MODE1	MODE2	ENOUT	Z2
A	X	0	0	A	A
X	B	1	0	B	B
A	X	0	1	0	A
X	B	1	1	0	B

X : Irrelevant

Chapter 4 Boundary Scan Block

Block type	Switching speed							Input		Output				
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
SVSNE2	ENIN	→	ENOUT (HH)	0.217	0.353	0.671	0.009	0.013	0.019	ENIN	4.1	ENOUT	32	
				0.201	0.345	0.685	0.006	0.007	0.010					
	ENIN	→	Z2 (HH)	0.198	0.326	0.603	0.021	0.030	0.042	MODE1	1.0	Z2	15	
				0.206	0.380	0.738	0.020	0.025	0.034					
	BSCAN	→	ENOUT (HH)	0.349	0.537	1.010	0.009	0.013	0.019	MODE2	4.2			
				0.333	0.557	1.080	0.006	0.008	0.012					
	BSCAN	→	Z2 (HH)	0.322	0.510	0.948	0.022	0.030	0.043					
				0.341	0.616	1.174	0.020	0.026	0.037					
	MODE1	→	ENOUT (HH)	0.376	0.610	1.167	0.009	0.013	0.019					
				(HL)	0.354	0.589	1.129	0.006	0.008					0.012
				(LH)	0.308	0.498	0.946	0.009	0.013					0.019
	MODE1	→	Z2 (HH)	0.350	0.584	1.105	0.022	0.030	0.043					
				(HL)	0.365	0.649	1.224	0.020	0.026					0.037
				(LH)	0.288	0.471	0.878	0.021	0.030					0.042
	MODE2	→	ENOUT (HL)	0.313	0.553	1.054	0.020	0.025	0.034					
				(HL)	0.083	0.120	0.180	0.005	0.006					0.008
				(LH)	0.081	0.122	0.234	0.009	0.013					0.020



[MEMO]

[MEMO]

[MEMO]

## 4.5 Soft Macro

### Chapter 4 Boundary Scan Block

Function	BScan TAP Controller									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SBCK	392								

Logic Diagram

Equivalent Circuit

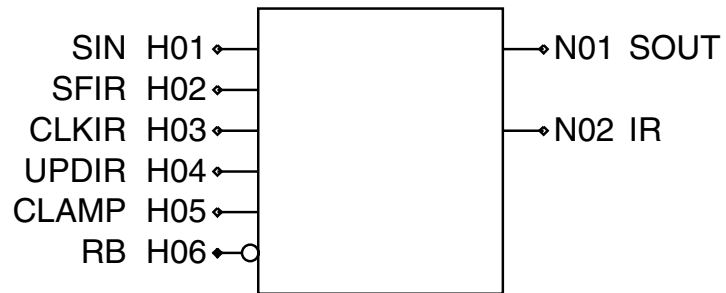
### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBCK													

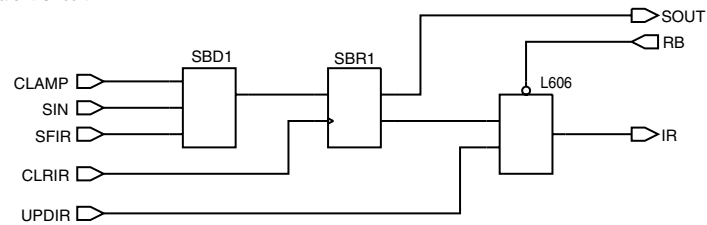
### Chapter 4 Boundary Scan Block

Function	BScan Instruction Register (Internal Circuit)									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SBM4	46								
-										

Logic Diagram



Equivalent Circuit



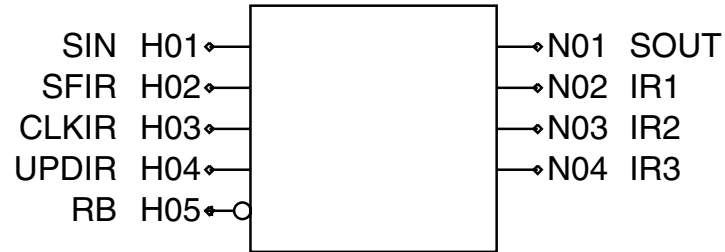
### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBM4													

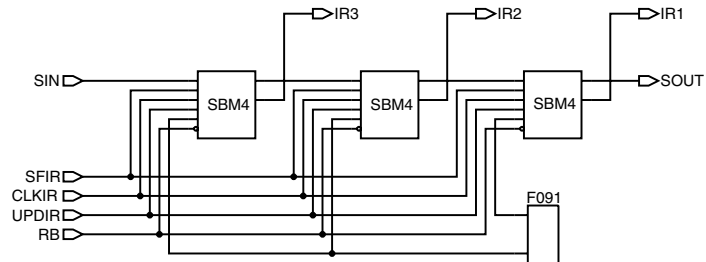
Chapter 4 Boundary Scan Block

Function	BScan Instruction Register									
Block type	Standard type									
	Name	cells	Name	cells						
-	SBM5	140								
-										

Logic Diagram



Equivalent Circuit



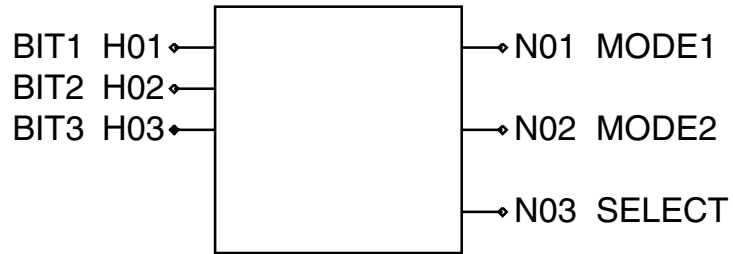
Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBM5													

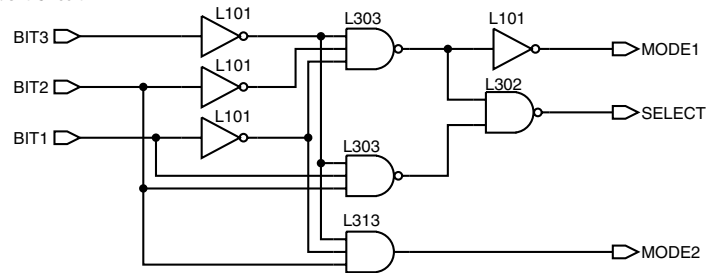
Chapter 4 Boundary Scan Block

Function	BScan Instruction Decoder											
Block type	Standard type											
Drivability	Name	cells	Name	cells								
-	SBM6	24										

Logic Diagram



Equivalent Circuit



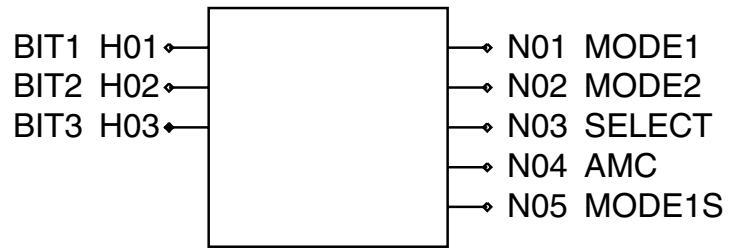
Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBM6													

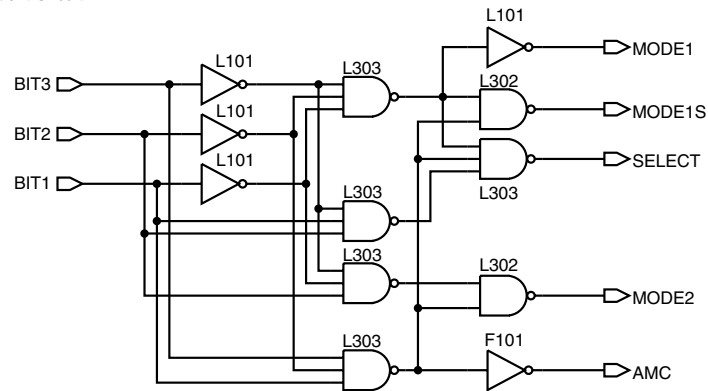
### Chapter 4 Boundary Scan Block

Function	BScan Instruction Decoder with NEC Scan									
Block type	Standard type									
Drivability	Name	cells	Name	cells						
-	SBMC	37								

Logic Diagram



Equivalent Circuit



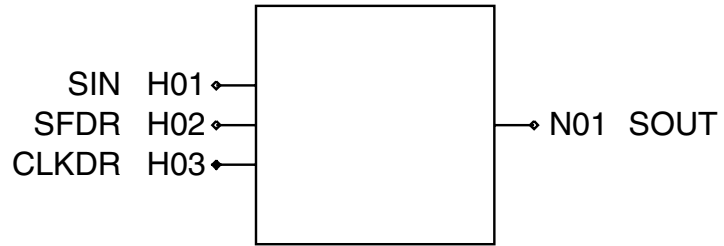
### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBMC													

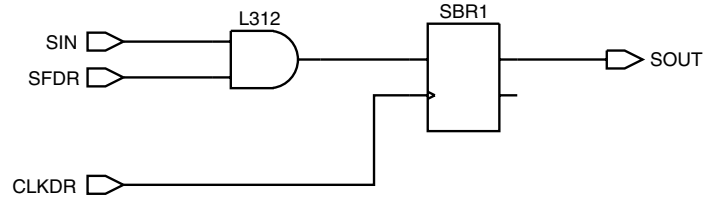
Chapter 4 Boundary Scan Block

Function	BScan Bypass Register												
Block type	Standard type												
	-	-	-	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells									
	-	SBS3	26										
-													

Logic Diagram



Equivalent Circuit



Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				

SBS3



# Index

Block	Function	Cells (I/O)	Page
B001	I/O Buffer 12mA	20 (1)	1-28
B002	I/O Buffer 12mA	20 (1)	1-72
B003	I/O Buffer 9mA	10 (1)	1-28
B004	I/O Buffer 9mA	10 (1)	1-72
B005	I/O Buffer 18mA	20 (1)	1-28
B006	I/O Buffer 18mA	20 (1)	1-72
B007	3-State Buffer 12mA	17 (1)	1-16
B008	3-State Buffer 9mA	7 (1)	1-16
B009	3-State Buffer 18mA	17 (1)	1-16
B00C	I/O Buffer 6mA	10 (1)	1-28
B00D	I/O Buffer 6mA	10 (1)	1-72
B00E	3-State Buffer 6mA	7 (1)	1-16
B00F	I/O Buffer 24mA	20 (1)	1-28
B00G	I/O Buffer 24mA	20 (1)	1-72
B00H	3-State Buffer 24mA	17 (1)	1-16
B00T	3-State Buffer 3mA	7 (1)	1-16
B00U	I/O Buffer 3mA	10 (1)	1-28
B00V	I/O Buffer 3mA	10 (1)	1-72
B0D1	I/O Buffer 12mA 50kΩ Pull-down	20 (1)	1-28
B0D2	I/O Buffer 12mA 50kΩ Pull-down	20 (1)	1-72
B0D3	I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-28
B0D4	I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-72
B0D5	I/O Buffer 18mA 50kΩ Pull-down	20 (1)	1-28
B0D6	I/O Buffer 18mA 50kΩ Pull-down	20 (1)	1-72
B0D7	3-State Buffer 12mA 50kΩ Pull-down	17 (1)	1-16
B0D8	3-State Buffer 9mA 50kΩ Pull-down	7 (1)	1-16
B0D9	3-State Buffer 18mA 50kΩ Pull-down	17 (1)	1-16
B0DC	I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-28
B0DD	I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-72
B0DE	3-State Buffer 6mA 50kΩ Pull-down	7 (1)	1-16
B0DF	I/O Buffer 24mA 50kΩ Pull-down	20 (1)	1-28
B0DG	I/O Buffer 24mA 50kΩ Pull-down	20 (1)	1-72
B0DH	3-State Buffer 24mA 50kΩ Pull-down	17 (1)	1-16
B0DT	3-State Buffer 3mA 50kΩ Pull-down	7 (1)	1-16
B0DU	I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-28
B0DV	I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-72
B0U1	I/O Buffer 12mA 50kΩ Pull-up	20 (1)	1-28
B0U2	I/O Buffer 12mA 50kΩ Pull-up	20 (1)	1-72
B0U3	I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-28
B0U4	I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-72
B0U5	I/O Buffer 18mA 50kΩ Pull-up	20 (1)	1-28

Block	Function	Cells (I/O)	Page
B0U6	I/O Buffer 18mA 50kΩ Pull-up	20 (1)	1-72
B0U7	3-State Buffer 12mA 50kΩ Pull-up	17 (1)	1-16
B0U8	3-State Buffer 9mA 50kΩ Pull-up	7 (1)	1-16
B0U9	3-State Buffer 18mA 50kΩ Pull-up	17 (1)	1-16
B0UC	I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-28
B0UD	I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-72
B0UE	3-State Buffer 6mA 50kΩ Pull-up	7 (1)	1-16
B0UF	I/O Buffer 24mA 50kΩ Pull-up	20 (1)	1-28
B0UG	I/O Buffer 24mA 50kΩ Pull-up	20 (1)	1-72
B0UH	3-State Buffer 24mA 50kΩ Pull-up	17 (1)	1-16
B0UT	3-State Buffer 3mA 50kΩ Pull-up	7 (1)	1-16
B0UU	I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-28
B0UV	I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-72
B0W1	I/O Buffer 12mA 5kΩ Pull-up	20 (1)	1-28
B0W2	I/O Buffer 12mA 5kΩ Pull-up	20 (1)	1-72
B0W3	I/O Buffer 9mA 5kΩ Pull-up	10 (1)	1-28
B0W4	I/O Buffer 9mA 5kΩ Pull-up	10 (1)	1-72
B0W5	I/O Buffer 18mA 5kΩ Pull-up	20 (1)	1-28
B0W6	I/O Buffer 18mA 5kΩ Pull-up	20 (1)	1-72
B0W7	3-State Buffer 12mA 5kΩ Pull-up	17 (1)	1-16
B0W8	3-State Buffer 9mA 5kΩ Pull-up	7 (1)	1-16
B0W9	3-State Buffer 18mA 5kΩ Pull-up	17 (1)	1-16
B0WC	I/O Buffer 6mA 5kΩ Pull-up	10 (1)	1-28
B0WD	I/O Buffer 6mA 5kΩ Pull-up	10 (1)	1-72
B0WE	3-State Buffer 6mA 5kΩ Pull-up	7 (1)	1-16
B0WF	I/O Buffer 24mA 5kΩ Pull-up	20 (1)	1-28
B0WG	I/O Buffer 24mA 5kΩ Pull-up	20 (1)	1-72
B0WH	3-State Buffer 24mA 5kΩ Pull-up	17 (1)	1-16
B0WT	3-State Buffer 3mA 5kΩ Pull-up	7 (1)	1-16
B0WU	I/O Buffer 3mA 5kΩ Pull-up	10 (1)	1-28
B0WV	I/O Buffer 3mA 5kΩ Pull-up	10 (1)	1-72
BE01	Low-noise I/O Buffer 12mA	10 (1)	1-34
BE02	Low-noise I/O Buffer 12mA	10 (1)	1-78
BE03	Low-noise I/O Buffer 9mA	10 (1)	1-34
BE04	Low-noise I/O Buffer 9mA	10 (1)	1-78
BE05	Low-noise I/O Buffer 18mA	10 (1)	1-34
BE06	Low-noise I/O Buffer 18mA	10 (1)	1-78
BE07	Low-noise 3-State Buffer 12mA	7 (1)	1-20
BE08	Low-noise 3-State Buffer 9mA	7 (1)	1-20
BE09	Low-noise 3-State Buffer 18mA	7 (1)	1-20
BE0C	Low-noise I/O Buffer 6mA	10 (1)	1-34
BE0D	Low-noise I/O Buffer 6mA	10 (1)	1-78
BE0E	Low-noise 3-State Buffer 6mA	7 (1)	1-20

Block	Function	Cells (I/O)	Page
BE0F	Low-noise I/O Buffer 24mA	10 (1)	1-34
BE0G	Low-noise I/O Buffer 24mA	10 (1)	1-78
BE0H	Low-noise 3-State Buffer 24mA	7 (1)	1-20
BE0T	Low-noise 3-State Buffer 3mA	7 (1)	1-20
BE0U	Low-noise I/O Buffer 3mA	10 (1)	1-34
BE0V	Low-noise I/O Buffer 3mA	10 (1)	1-78
BED1	Low-noise I/O Buffer 12mA 50kΩ Pull-down	10 (1)	1-34
BED2	Low-noise I/O Buffer 12mA 50kΩ Pull-down	10 (1)	1-78
BED3	Low-noise I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-34
BED4	Low-noise I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-78
BED5	Low-noise I/O Buffer 18mA 50kΩ Pull-down	10 (1)	1-34
BED6	Low-noise I/O Buffer 18mA 50kΩ Pull-down	10 (1)	1-78
BED7	Low-noise 3-State Buffer 12mA 50kΩ Pull-down	7 (1)	1-20
BED8	Low-noise 3-State Buffer 9mA 50kΩ Pull-down	7 (1)	1-20
BED9	Low-noise 3-State Buffer 18mA 50kΩ Pull-down	7 (1)	1-20
BEDC	Low-noise I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-34
BEDD	Low-noise I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-78
BEDE	Low-noise 3-State Buffer 6mA 50kΩ Pull-down	7 (1)	1-20
BEDF	Low-noise I/O Buffer 24mA 50kΩ Pull-down	10 (1)	1-34
BEDG	Low-noise I/O Buffer 24mA 50kΩ Pull-down	10 (1)	1-78
BEDH	Low-noise 3-State Buffer 24mA 50kΩ Pull-down	7 (1)	1-20
BEDT	Low-noise 3-State Buffer 3mA 50kΩ Pull-down	7 (1)	1-20
BEDU	Low-noise I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-34
BEDV	Low-noise I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-78
BEU1	Low-noise I/O Buffer 12mA 50kΩ Pull-up	10 (1)	1-34
BEU2	Low-noise I/O Buffer 12mA 50kΩ Pull-up	10 (1)	1-78
BEU3	Low-noise I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-34
BEU4	Low-noise I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-78
BEU5	Low-noise I/O Buffer 18mA 50kΩ Pull-up	10 (1)	1-34
BEU6	Low-noise I/O Buffer 18mA 50kΩ Pull-up	10 (1)	1-78
BEU7	Low-noise 3-State Buffer 12mA 50kΩ Pull-up	7 (1)	1-20
BEU8	Low-noise 3-State Buffer 9mA 50kΩ Pull-up	7 (1)	1-20
BEU9	Low-noise 3-State Buffer 18mA 50kΩ Pull-up	7 (1)	1-20
BEUC	Low-noise I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-34
BEUD	Low-noise I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-78
BEUE	Low-noise 3-State Buffer 6mA 50kΩ Pull-up	7 (1)	1-20
BEUF	Low-noise I/O Buffer 24mA 50kΩ Pull-up	10 (1)	1-34
BEUG	Low-noise I/O Buffer 24mA 50kΩ Pull-up	10 (1)	1-78
BEUH	Low-noise 3-State Buffer 24mA 50kΩ Pull-up	7 (1)	1-20
BEUT	Low-noise 3-State Buffer 3mA 50kΩ Pull-up	7 (1)	1-20
BEUU	Low-noise I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-34
BEUV	Low-noise I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-78
BEW1	Low-noise I/O Buffer 12mA 5kΩ Pull-up	10 (1)	1-34

Block	Function	Cells (I/O)	Page
BEW2	Low-noise I/O Buffer 12mA 5k $\Omega$ Pull-up	10 (1)	1-78
BEW3	Low-noise I/O Buffer 9mA 5k $\Omega$ Pull-up	10 (1)	1-34
BEW4	Low-noise I/O Buffer 9mA 5k $\Omega$ Pull-up	10 (1)	1-78
BEW5	Low-noise I/O Buffer 18mA 5k $\Omega$ Pull-up	10 (1)	1-34
BEW6	Low-noise I/O Buffer 18mA 5k $\Omega$ Pull-up	10 (1)	1-78
BEW7	Low-noise 3-State Buffer 12mA 5k $\Omega$ Pull-up	7 (1)	1-20
BEW8	Low-noise 3-State Buffer 9mA 5k $\Omega$ Pull-up	7 (1)	1-20
BEW9	Low-noise 3-State Buffer 18mA 5k $\Omega$ Pull-up	7 (1)	1-20
BEWC	Low-noise I/O Buffer 6mA 5k $\Omega$ Pull-up	10 (1)	1-34
BEWD	Low-noise I/O Buffer 6mA 5k $\Omega$ Pull-up	10 (1)	1-78
BEWE	Low-noise 3-State Buffer 6mA 5k $\Omega$ Pull-up	7 (1)	1-20
BEWF	Low-noise I/O Buffer 24mA 5k $\Omega$ Pull-up	10 (1)	1-34
BEWG	Low-noise I/O Buffer 24mA 5k $\Omega$ Pull-up	10 (1)	1-78
BEWH	Low-noise 3-State Buffer 24mA 5k $\Omega$ Pull-up	7 (1)	1-20
BEWT	Low-noise 3-State Buffer 3mA 5k $\Omega$ Pull-up	7 (1)	1-20
BEWU	Low-noise I/O Buffer 3mA 5k $\Omega$ Pull-up	10 (1)	1-34
BEWV	Low-noise I/O Buffer 3mA 5k $\Omega$ Pull-up	10 (1)	1-78
BFD1W	Low-noise Schmitt I/O Buffer 12mA 50k $\Omega$ Pull-down	13 (1)	1-46
BFD2W	Low-noise Schmitt I/O Buffer 12mA 50k $\Omega$ Pull-down	13 (1)	1-90
BFD3W	Low-noise Schmitt I/O Buffer 9mA 50k $\Omega$ Pull-down	13 (1)	1-46
BFD4W	Low-noise Schmitt I/O Buffer 9mA 50k $\Omega$ Pull-down	13 (1)	1-90
BFD5W	Low-noise Schmitt I/O Buffer 18mA 50k $\Omega$ Pull-down	13 (1)	1-46
BFD6W	Low-noise Schmitt I/O Buffer 18mA 50k $\Omega$ Pull-down	13 (1)	1-90
BFDCW	Low-noise Schmitt I/O Buffer 6mA 50k $\Omega$ Pull-down	13 (1)	1-46
BFDDW	Low-noise Schmitt I/O Buffer 6mA 50k $\Omega$ Pull-down	13 (1)	1-90
BFDFW	Low-noise Schmitt I/O Buffer 24mA 50k $\Omega$ Pull-down	13 (1)	1-46
BFDGW	Low-noise Schmitt I/O Buffer 24mA 50k $\Omega$ Pull-down	13 (1)	1-90
BFDUW	Low-noise Schmitt I/O Buffer 3mA 50k $\Omega$ Pull-down	13 (1)	1-46
BFDVW	Low-noise Schmitt I/O Buffer 3mA 50k $\Omega$ Pull-down	13 (1)	1-90
BFI1W	Low-noise Schmitt I/O Buffer 12mA	13 (1)	1-46
BFI2W	Low-noise Schmitt I/O Buffer 12mA	13 (1)	1-90
BFI3W	Low-noise Schmitt I/O Buffer 9mA	13 (1)	1-46
BFI4W	Low-noise Schmitt I/O Buffer 9mA	13 (1)	1-90
BFI5W	Low-noise Schmitt I/O Buffer 18mA	13 (1)	1-46
BFI6W	Low-noise Schmitt I/O Buffer 18mA	13 (1)	1-90
BFICW	Low-noise Schmitt I/O Buffer 6mA	13 (1)	1-46
BFIDW	Low-noise Schmitt I/O Buffer 6mA	13 (1)	1-90
BFIFW	Low-noise Schmitt I/O Buffer 24mA	13 (1)	1-46
BFIGW	Low-noise Schmitt I/O Buffer 24mA	13 (1)	1-90
BFIUW	Low-noise Schmitt I/O Buffer 3mA	13 (1)	1-46
BFIVW	Low-noise Schmitt I/O Buffer 3mA	13 (1)	1-90
BFU1W	Low-noise Schmitt I/O Buffer 12mA 50k $\Omega$ Pull-up	13 (1)	1-46
BFU2W	Low-noise Schmitt I/O Buffer 12mA 50k $\Omega$ Pull-up	13 (1)	1-90

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BFU4W	Low-noise Schmitt I/O Buffer 9mA 50kΩ Pull-up	13 (1)	1-90
BFU5W	Low-noise Schmitt I/O Buffer 18mA 50kΩ Pull-up	13 (1)	1-46
BFU6W	Low-noise Schmitt I/O Buffer 18mA 50kΩ Pull-up	13 (1)	1-90
BFUCW	Low-noise Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-46
BFUDW	Low-noise Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-90
BFUFW	Low-noise Schmitt I/O Buffer 24mA 50kΩ Pull-up	13 (1)	1-46
BFUGW	Low-noise Schmitt I/O Buffer 24mA 50kΩ Pull-up	13 (1)	1-90
BFUJW	Low-noise Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-46
BFUVW	Low-noise Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-90
BFW1W	Low-noise Schmitt I/O Buffer 12mA 5kΩ Pull-up	13 (1)	1-46
BFW2W	Low-noise Schmitt I/O Buffer 12mA 5kΩ Pull-up	13 (1)	1-90
BFW3W	Low-noise Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-46
BFW4W	Low-noise Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-90
BFW5W	Low-noise Schmitt I/O Buffer 18mA 5kΩ Pull-up	13 (1)	1-46
BFW6W	Low-noise Schmitt I/O Buffer 18mA 5kΩ Pull-up	13 (1)	1-90
BFWCW	Low-noise Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-46
BFWDW	Low-noise Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-90
BFWFW	Low-noise Schmitt I/O Buffer 24mA 5kΩ Pull-up	13 (1)	1-46
BFWGW	Low-noise Schmitt I/O Buffer 24mA 5kΩ Pull-up	13 (1)	1-90
BFWJW	Low-noise Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-46
BFWVW	Low-noise Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-90
BN21	I/O Buffer with EN(AND) 12mA	23 (1)	1-52
BN22	I/O Buffer with EN(AND) 12mA	24 (1)	1-96
BN23	I/O Buffer with EN(AND) 9mA	13 (1)	1-52
BN24	I/O Buffer with EN(AND) 9mA	14 (1)	1-96
BN25	I/O Buffer with EN(AND) 18mA	23 (1)	1-52
BN26	I/O Buffer with EN(AND) 18mA	24 (1)	1-96
BN2C	I/O Buffer with EN(AND) 6mA	13 (1)	1-52
BN2D	I/O Buffer with EN(AND) 6mA	14 (1)	1-96
BN2F	I/O Buffer with EN(AND) 24mA	23 (1)	1-52
BN2G	I/O Buffer with EN(AND) 24mA	24 (1)	1-96
BN2U	I/O Buffer with EN(AND) 3mA	13 (1)	1-52
BN2V	I/O Buffer with EN(AND) 3mA	14 (1)	1-96
BN31	I/O Buffer with EN(OR) 12mA	21 (1)	1-56
BN32	I/O Buffer with EN(OR) 12mA	21 (1)	1-100
BN33	I/O Buffer with EN(OR) 9mA	11 (1)	1-56
BN34	I/O Buffer with EN(OR) 9mA	11 (1)	1-100
BN35	I/O Buffer with EN(OR) 18mA	21 (1)	1-56
BN36	I/O Buffer with EN(OR) 18mA	21 (1)	1-100
BN3C	I/O Buffer with EN(OR) 6mA	11 (1)	1-56
BN3D	I/O Buffer with EN(OR) 6mA	11 (1)	1-100
BN3F	I/O Buffer with EN(OR) 24mA	21 (1)	1-56

Block	Function	Cells (I/O)	Page
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BN3U	I/O Buffer with EN(OR) 3mA	11 (1)	1-56
BN3V	I/O Buffer with EN(OR) 3mA	11 (1)	1-100
BN41	I/O Buffer with EN(AND) 12mA 50kΩ Pull-down	23 (1)	1-52
BN42	I/O Buffer with EN(AND) 12mA 50kΩ Pull-down	24 (1)	1-96
BN43	I/O Buffer with EN(AND) 9mA 50kΩ Pull-down	13 (1)	1-52
BN44	I/O Buffer with EN(AND) 9mA 50kΩ Pull-down	14 (1)	1-96
BN45	I/O Buffer with EN(AND) 18mA 50kΩ Pull-down	23 (1)	1-52
BN46	I/O Buffer with EN(AND) 18mA 50kΩ Pull-down	24 (1)	1-96
BN4C	I/O Buffer with EN(AND) 6mA 50kΩ Pull-down	13 (1)	1-52
BN4D	I/O Buffer with EN(AND) 6mA 50kΩ Pull-down	14 (1)	1-96
BN4F	I/O Buffer with EN(AND) 24mA 50kΩ Pull-down	23 (1)	1-52
BN4G	I/O Buffer with EN(AND) 24mA 50kΩ Pull-down	24 (1)	1-96
BN4U	I/O Buffer with EN(AND) 3mA 50kΩ Pull-down	13 (1)	1-52
BN4V	I/O Buffer with EN(AND) 3mA 50kΩ Pull-down	14 (1)	1-96
BN51	I/O Buffer with EN(OR) 12mA 50kΩ Pull-down	21 (1)	1-56
BN52	I/O Buffer with EN(OR) 12mA 50kΩ Pull-down	21 (1)	1-100
BN53	I/O Buffer with EN(OR) 9mA 50kΩ Pull-down	11 (1)	1-56
BN54	I/O Buffer with EN(OR) 9mA 50kΩ Pull-down	11 (1)	1-100
BN55	I/O Buffer with EN(OR) 18mA 50kΩ Pull-down	21 (1)	1-56
BN56	I/O Buffer with EN(OR) 18mA 50kΩ Pull-down	21 (1)	1-100
BN5C	I/O Buffer with EN(OR) 6mA 50kΩ Pull-down	11 (1)	1-56
BN5D	I/O Buffer with EN(OR) 6mA 50kΩ Pull-down	11 (1)	1-100
BN5F	I/O Buffer with EN(OR) 24mA 50kΩ Pull-down	21 (1)	1-56
BN5G	I/O Buffer with EN(OR) 24mA 50kΩ Pull-down	21 (1)	1-100
BN5U	I/O Buffer with EN(OR) 3mA 50kΩ Pull-down	11 (1)	1-56
BN5V	I/O Buffer with EN(OR) 3mA 50kΩ Pull-down	11 (1)	1-100
BSD1W	Schmitt I/O Buffer 12mA 50kΩ Pull-down	23 (1)	1-40
BSD2W	Schmitt I/O Buffer 12mA 50kΩ Pull-down	23 (1)	1-84
BSD3W	Schmitt I/O Buffer 9mA 50kΩ Pull-down	13 (1)	1-40
BSD4W	Schmitt I/O Buffer 9mA 50kΩ Pull-down	13 (1)	1-84
BSD5W	Schmitt I/O Buffer 18mA 50kΩ Pull-down	23 (1)	1-40
BSD6W	Schmitt I/O Buffer 18mA 50kΩ Pull-down	23 (1)	1-84
BSDCW	Schmitt I/O Buffer 6mA 50kΩ Pull-down	13 (1)	1-40
BSDDW	Schmitt I/O Buffer 6mA 50kΩ Pull-down	13 (1)	1-84
BSDFW	Schmitt I/O Buffer 24mA 50kΩ Pull-down	23 (1)	1-40
BSDGW	Schmitt I/O Buffer 24mA 50kΩ Pull-down	23 (1)	1-84
BSDUW	Schmitt I/O Buffer 3mA 50kΩ Pull-down	13 (1)	1-40
BSDVW	Schmitt I/O Buffer 3mA 50kΩ Pull-down	13 (1)	1-84
BSI1W	Schmitt I/O Buffer 12mA	23 (1)	1-40
BSI2W	Schmitt I/O Buffer 12mA	23 (1)	1-84
BSI3W	Schmitt I/O Buffer 9mA	13 (1)	1-40
BSI4W	Schmitt I/O Buffer 9mA	13 (1)	1-84

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BSI5W	Schmitt I/O Buffer 18mA	23 (1)	1-40
BSI6W	Schmitt I/O Buffer 18mA	23 (1)	1-84
BSICW	Schmitt I/O Buffer 6mA	13 (1)	1-40
BSIDW	Schmitt I/O Buffer 6mA	13 (1)	1-84
BSIFW	Schmitt I/O Buffer 24mA	23 (1)	1-40
BSIGW	Schmitt I/O Buffer 24mA	23 (1)	1-84
BSIUW	Schmitt I/O Buffer 3mA	13 (1)	1-40
BSIVW	Schmitt I/O Buffer 3mA	13 (1)	1-84
BSU1W	Schmitt I/O Buffer 12mA 50kΩ Pull-up	23 (1)	1-40
BSU2W	Schmitt I/O Buffer 12mA 50kΩ Pull-up	23 (1)	1-84
BSU3W	Schmitt I/O Buffer 9mA 50kΩ Pull-up	13 (1)	1-40
BSU4W	Schmitt I/O Buffer 9mA 50kΩ Pull-up	13 (1)	1-84
BSU5W	Schmitt I/O Buffer 18mA 50kΩ Pull-up	23 (1)	1-40
BSU6W	Schmitt I/O Buffer 18mA 50kΩ Pull-up	23 (1)	1-84
BSUCW	Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-40
BSUDW	Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-84
BSUFW	Schmitt I/O Buffer 24mA 50kΩ Pull-up	23 (1)	1-40
BSUGW	Schmitt I/O Buffer 24mA 50kΩ Pull-up	23 (1)	1-84
BSUUW	Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-40
BSUVW	Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-84
BSW1W	Schmitt I/O Buffer 12mA 5kΩ Pull-up	23 (1)	1-40
BSW2W	Schmitt I/O Buffer 12mA 5kΩ Pull-up	23 (1)	1-84
BSW3W	Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-40
BSW4W	Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-84
BSW5W	Schmitt I/O Buffer 18mA 5kΩ Pull-up	23 (1)	1-40
BSW6W	Schmitt I/O Buffer 18mA 5kΩ Pull-up	23 (1)	1-84
BSWCW	Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-40
BSWDW	Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-84
BSWFW	Schmitt I/O Buffer 24mA 5kΩ Pull-up	23 (1)	1-40
BSWGW	Schmitt I/O Buffer 24mA 5kΩ Pull-up	23 (1)	1-84
BSWUW	Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-40
BSWVW	Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-84
EXO1	N-ch open drain Buffer with failsafe 9mA	4 (1)	1-26
EXO5	N-ch open drain Buffer with failsafe 18mA	4 (1)	1-26
EXO9	N-ch open drain Buffer with failsafe 12mA	4 (1)	1-26
EXOD	N-ch open drain Buffer with failsafe 24mA	4 (1)	1-26
EXT1	N-ch open drain Buffer 9mA	4 (1)	1-24
EXT3	N-ch open drain Buffer 9mA 50kΩ Pull-up	4 (1)	1-24
EXT5	N-ch open drain Buffer 18mA	4 (1)	1-24
EXT7	N-ch open drain Buffer 18mA 50kΩ Pull-up	4 (1)	1-24
EXT9	N-ch open drain Buffer 12mA	4 (1)	1-24
EXTB	N-ch open drain Buffer 12mA 50kΩ Pull-up	4 (1)	1-24
EXTD	N-ch open drain Buffer 24mA	4 (1)	1-24

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EXTF	N-ch open drain Buffer 24mA 50kΩ Pull-up	4 (1)	1-24
EXW3	N-ch open drain Buffer 9mA 5kΩ Pull-up	4 (1)	1-24
EXW7	N-ch open drain Buffer 18mA 5kΩ Pull-up	4 (1)	1-24
EXWB	N-ch open drain Buffer 12mA 5kΩ Pull-up	4 (1)	1-24
EXWF	N-ch open drain Buffer 24mA 5kΩ Pull-up	4 (1)	1-24
F091	H, L Level Generator	1 (-)	2-4
F101	Inverter Single Out	1 (-)	2-10
F102	Inverter Single Out, x2-drive	2 (-)	2-10
F111	Buffer Single Out	2 (-)	2-12
F112	Buffer Single Out, x2-drive	3 (-)	2-12
F131	Delay Gate	6 (-)	2-16
F132	Delay Gate	10 (-)	2-16
F143	Inverter Single Out, x3-drive	3 (-)	2-10
F144	Inverter Single Out, x4-drive	4 (-)	2-10
F145	Inverter Single Out, x5-drive	5 (-)	2-10
F146	Inverter Single Out, x6-drive	6 (-)	2-10
F148	Inverter Single Out, x8-drive	12 (-)	2-10
F153	Buffer Single Out, x3-drive	4 (-)	2-12
F154	Buffer Single Out, x4-drive	5 (-)	2-12
F158	Buffer Single Out, x8-drive	11 (-)	2-12
F202	2-Input NOR	2 (-)	2-22
F203	3-Input NOR	3 (-)	2-24
F204	4-Input NOR	4 (-)	2-26
F205	5-Input NOR	5 (-)	2-28
F206	6-Input NOR	5 (-)	2-30
F208	8-Input NOR	7 (-)	2-32
F212	2-Input OR	2 (-)	2-34
F213	3-Input OR	3 (-)	2-36
F214	4-Input OR	3 (-)	2-38
F215	5-Input OR	5 (-)	2-40
F216	6-Input OR	5 (-)	2-42
F218	8-Input OR	8 (-)	2-44
F222	2-Input NOR x2-drive	4 (-)	2-22
F223	3-Input NOR x2-drive	6 (-)	2-24
F225	5-Input NOR x2-drive	6 (-)	2-28
F226	6-Input NOR x2-drive	6 (-)	2-30
F228	8-Input NOR x2-drive	8 (-)	2-32
F232	2-Input OR x2-drive	3 (-)	2-34
F233	3-Input OR x2-drive	4 (-)	2-36
F234	4-Input OR x2-drive	4 (-)	2-38
F235	5-Input OR x2-drive	7 (-)	2-40
F236	6-Input OR x2-drive	7 (-)	2-42
F238	8-Input OR x2-drive	9 (-)	2-44



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F282	2-Input NOR x4-drive	6 (-)	2-22
F302	2-Input NAND	2 (-)	2-50
F303	3-Input NAND	3 (-)	2-52
F304	4-Input NAND	4 (-)	2-54
F305	5-Input NAND	5 (-)	2-56
F306	6-Input NAND	5 (-)	2-58
F308	8-Input NAND	6 (-)	2-60
F312	2-Input AND	2 (-)	2-62
F313	3-Input AND	3 (-)	2-64
F314	4-Input AND	3 (-)	2-66
F315	5-Input AND	5 (-)	2-68
F316	6-Input AND	5 (-)	2-70
F318	8-Input AND	6 (-)	2-72
F322	2-Input NAND x2-drive	4 (-)	2-50
F323	3-Input NAND x2-drive	6 (-)	2-52
F324	4-Input NAND x2-drive	8 (-)	2-54
F325	5-Input NAND x2-drive	6 (-)	2-56
F326	6-Input NAND x2-drive	6 (-)	2-58
F328	8-Input NAND x2-drive	7 (-)	2-60
F332	2-Input AND x2-drive	3 (-)	2-62
F333	3-Input AND x2-drive	4 (-)	2-64
F334	4-Input AND x2-drive	4 (-)	2-66
F335	5-Input AND x2-drive	7 (-)	2-68
F336	6-Input AND x2-drive	7 (-)	2-70
F338	8-Input AND x2-drive	8 (-)	2-72
F352	2-Input AND x4-drive	6 (-)	2-62
F382	2-Input NAND x4-drive	6 (-)	2-50
F421	1-2-Input AND-NOR	3 (-)	2-78
F422	1-1-2-Input AND-NOR	4 (-)	2-80
F423	1-3-Input AND-NOR	4 (-)	2-82
F424	2-2-Input AND-NOR	4 (-)	2-84
F425	2-2-2-Input AND-NOR	6 (-)	2-86
F427	2-3-Input AND-NOR	5 (-)	2-88
F428	1-2-2-Input AND-NOR	5 (-)	2-90
F429	2-2-2-2-Input AND-NOR	6 (-)	2-92
F430	1-4-Input OR-NAND	5 (-)	2-124
F431	1-2-Input OR-NAND	3 (-)	2-126
F432	1-1-2-Input OR-NAND	4 (-)	2-128
F433	1-3-Input OR-NAND	4 (-)	2-130
F434	2-2-Input OR-NAND	4 (-)	2-132
F435	2-3-Input OR-NAND	5 (-)	2-134
F436	3-3-Input OR-NAND	6 (-)	2-136

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F439	1-5-Input OR-NAND	6 (-)	2-142
F440	1-4-Input AND-NOR	5 (-)	2-94
F441	1-5-Input AND-NOR	7 (-)	2-96
F444	4-4-4-Input AND-NOR	8 (-)	2-98
F446	1-1-1-2-Input AND-NOR	5 (-)	2-100
F447	1-1-1-3-Input AND-NOR	5 (-)	2-102
F448	1-1-2-2-Input AND-NOR	5 (-)	2-104
F449	3-3-3-3-Input AND-NOR	8 (-)	2-106
F450	2-4-Input OR-NAND	6 (-)	2-144
F451	4-4-Input OR-NAND	8 (-)	2-146
F452	1-1-3-Input OR-NAND	5 (-)	2-148
F453	1-1-4-Input OR-NAND	6 (-)	2-150
F457	4-4-4-Input OR-NAND	10 (-)	2-152
F458	1-1-1-2-Input OR-NAND	5 (-)	2-154
F459	1-1-1-3-Input OR-NAND	5 (-)	2-156
F460	3-3-3-Input AND-NOR	7 (-)	2-108
F462	1-2-3-Input AND-NOR	6 (-)	2-110
F463	1-1-3-Input AND-NOR	5 (-)	2-112
F464	1-1-4-Input AND-NOR	5 (-)	2-114
F465	1-1-1-1-2-Input AND-NOR	5 (-)	2-116
F466	4-4-4-4-Input AND-NOR	10 (-)	2-118
F490	1-1-1-1-2-Input OR-NAND	5 (-)	2-158
F491	1-2-3-Input OR-NAND	5 (-)	2-160
F493	3-3-3-Input OR-NAND	7 (-)	2-162
F495	1-1-2-2-Input OR-NAND	6 (-)	2-164
F496	3-3-3-3-Input OR-NAND	8 (-)	2-166
F498	4-4-4-4-Input OR-NAND	14 (-)	2-168
F511	2-Input Exclusive OR	4 (-)	2-174
F512	2-Input Exclusive NOR	4 (-)	2-178
F516	3-Input Exclusive OR	7 (-)	2-176
F517	3-Input Exclusive NOR	7 (-)	2-180
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F531	3-State Buffer with EN	5 (-)	2-198
F532	3-State Buffer with ENB	5 (-)	2-198
F533	3-State Buffer with EN, x2-drive	7 (-)	2-198
F534	3-State Buffer with ENB, x2-drive	7 (-)	2-198
F53F	3-State Buffer with EN, x4-drive	11 (-)	2-198
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F543	3-State Buffer Inverter with EN, x2-drive	8 (-)	2-198
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F565	2 to 1 Multiplexer (Positive Out)	4 (-)	2-206
F569	8 to 1 Multiplexer (Positive Out) with ENB	18 (-)	2-210
F570	4 to 1 Multiplexer (Positive Out) with ENB	10 (-)	2-208
F571	2 to 1 Multiplexer (Positive Out) with ENB	6 (-)	2-206
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F595	RS-Latch	5 (-)	2-226
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F601	D-Latch	6 (-)	2-234
F601NB	D-Latch QB Out	5 (-)	2-234
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F602	D-Latch with R	6 (-)	2-238
F602NB	D-Latch with R QB Out	5 (-)	2-238
F602NQ	D-Latch with R Q Out	6 (-)	2-238
F603	D-Latch with RB	7 (-)	2-242
F603NB	D-Latch with RB QB Out	6 (-)	2-242
F603NQ	D-Latch with RB Q Out	5 (-)	2-242
F604	D-Latch (GB)	6 (-)	2-252
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F605	D-Latch (GB) with RB	7 (-)	2-256
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F60KNB	D-Latch with SB QB Out	5 (-)	2-246
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F615	D-F/F with RB	9 (-)	2-272
F615H	D-F/F with RB, Hold	11 (-)	2-310
F615HB	D-F/F with RB, Hold QB Out	10 (-)	2-310

Block	Function	Cells (I/O)	Page
F615HQ	D-F/F with RB, Hold Q Out	10 (-)	2-310
F615NB	D-F/F with RB QB Out	8 (-)	2-272
F615NQ	D-F/F with RB Q Out	8 (-)	2-272
F615S	D-F/F with RB, 2 to 1 Selector	11 (-)	2-294
F615SB	D-F/F with RB, 2 to 1 Selector QB Out	10 (-)	2-294
F615SQ	D-F/F with RB, 2 to 1 Selector Q Out	10 (-)	2-294
F616	D-F/F with SB	9 (-)	2-274
F616H	D-F/F with SB, Hold	11 (-)	2-312
F616HB	D-F/F with SB, Hold QB Out	10 (-)	2-312
F616HQ	D-F/F with SB, Hold Q Out	10 (-)	2-312
F616NB	D-F/F with SB QB Out	8 (-)	2-274
F616NQ	D-F/F with SB Q Out	8 (-)	2-274
F616S	D-F/F with SB, 2 to 1 Selector	11 (-)	2-296
F616SB	D-F/F with SB, 2 to 1 Selector QB Out	10 (-)	2-296
F616SQ	D-F/F with SB, 2 to 1 Selector Q Out	10 (-)	2-296
F641	D-F/F	8 (-)	2-264
F641H	D-F/F with Hold	10 (-)	2-308
F641HB	D-F/F with Hold QB Out	9 (-)	2-308
F641HQ	D-F/F with Hold Q Out	9 (-)	2-308
F641NB	D-F/F QB Out	7 (-)	2-264
F641NQ	D-F/F Q Out	7 (-)	2-264
F641S	D-F/F with 2 to 1 Selector	10 (-)	2-286
F641SB	D-F/F with 2 to 1 Selector QB Out	9 (-)	2-286
F641SQ	D-F/F with 2 to 1 Selector Q Out	9 (-)	2-286
F642	D-F/F with R	9 (-)	2-266
F642NB	D-F/F with R QB Out	8 (-)	2-266
F642NQ	D-F/F with R Q Out	8 (-)	2-266
F642S	D-F/F with R, 2 to 1 Selector	11 (-)	2-288
F642SB	D-F/F with R, 2 to 1 Selector QB Out	10 (-)	2-288
F642SQ	D-F/F with R, 2 to 1 Selector Q Out	10 (-)	2-288
F643	D-F/F with S	9 (-)	2-268
F643NB	D-F/F with S QB Out	8 (-)	2-268
F643NQ	D-F/F with S Q Out	8 (-)	2-268
F643S	D-F/F with S, 2 to 1 Selector	11 (-)	2-290
F643SB	D-F/F with S, 2 to 1 Selector QB Out	10 (-)	2-290
F643SQ	D-F/F with S, 2 to 1 Selector Q Out	10 (-)	2-290
F644	D-F/F with R, S	10 (-)	2-270
F644NB	D-F/F with R, S QB Out	9 (-)	2-270
F644NQ	D-F/F with R, S Q Out	9 (-)	2-270
F644S	D-F/F with R, S, 2 to 1 Selector	12 (-)	2-292
F644SB	D-F/F with R, S, 2 to 1 Selector QB Out	11 (-)	2-292
F644SQ	D-F/F with R, S, 2 to 1 Selector Q Out	11 (-)	2-292
F647	D-F/F with RB, SB	10 (-)	2-276

Block	Function	Cells (I/O)	Page
F647H	D-F/F with RB, SB, Hold	12 (-)	2-314
F647HB	D-F/F with RB, SB, Hold QB Out	11 (-)	2-314
F647HQ	D-F/F with RB, SB, Hold Q Out	11 (-)	2-314
F647NB	D-F/F with RB, SB QB Out	9 (-)	2-276
F647NQ	D-F/F with RB, SB Q Out	9 (-)	2-276
F647S	D-F/F with RB, SB, 2 to 1 Selector	12 (-)	2-298
F647SB	D-F/F with RB, SB, 2 to 1 Selector QB Out	11 (-)	2-298
F647SQ	D-F/F with RB, SB, 2 to 1 Selector Q Out	11 (-)	2-298
F661	D-F/F (CB)	8 (-)	2-278
F661NB	D-F/F (CB) QB Out	7 (-)	2-278
F661NQ	D-F/F (CB) Q Out	7 (-)	2-278
F661S	D-F/F (CB) with 2 to 1 Selector	10 (-)	2-300
F661SB	D-F/F (CB) with 2 to 1 Selector QB Out	9 (-)	2-300
F661SQ	D-F/F (CB) with 2 to 1 Selector Q Out	9 (-)	2-300
F665	D-F/F (CB) with RB	9 (-)	2-280
F665NB	D-F/F (CB) with RB QB Out	8 (-)	2-280
F665NQ	D-F/F (CB) with RB Q Out	8 (-)	2-280
F665S	D-F/F (CB) with RB, 2 to 1 Selector	11 (-)	2-302
F665SB	D-F/F (CB) with RB, 2 to 1 Selector QB Out	10 (-)	2-302
F665SQ	D-F/F (CB) with RB, 2 to 1 Selector Q Out	10 (-)	2-302
F666	D-F/F (CB) with SB	9 (-)	2-282
F666NB	D-F/F (CB) with SB QB Out	8 (-)	2-282
F666NQ	D-F/F (CB) with SB Q Out	8 (-)	2-282
F666S	D-F/F (CB) with SB, 2 to 1 Selector	11 (-)	2-304
F666SB	D-F/F (CB) with SB, 2 to 1 Selector QB Out	10 (-)	2-304
F666SQ	D-F/F (CB) with SB, 2 to 1 Selector Q Out	10 (-)	2-304
F667	D-F/F (CB) with RB, SB	10 (-)	2-284
F667NB	D-F/F (CB) with RB, SB QB Out	9 (-)	2-284
F667NQ	D-F/F (CB) with RB, SB Q Out	9 (-)	2-284
F667S	D-F/F (CB) with RB, SB, 2 to 1 Selector	12 (-)	2-306
F667SB	D-F/F (CB) with RB, SB, 2 to 1 Selector QB Out	11 (-)	2-306
F667SQ	D-F/F (CB) with RB, SB, 2 to 1 Selector Q Out	11 (-)	2-306
F673	D-F/F (CB) with 2 to 1 Selector(2 CTRL), RB	11 (-)	2-316
F674	D-F/F (CB) with Hold, 2 to 1 Selector(2 CTRL), RB	12 (-)	2-318
F6R1	D-Latch, High Speed	6 (-)	2-236
F6R2	D-Latch with R, High Speed	7 (-)	2-240
F6R5	D-Latch with RB, High Speed	6 (-)	2-244
F6R8	D-Latch (GB), High Speed	6 (-)	2-254
F6R9	D-Latch (GB) with RB, High Speed	6 (-)	2-258
F744	T-F/F with R, S	9 (-)	2-324
F744NQ	T-F/F with R, S Q Out	8 (-)	2-324
F745	T-F/F with RB	8 (-)	2-326
F745NQ	T-F/F with RB Q Out	7 (-)	2-326

Block	Function	Cells (I/O)	Page
F747	T-F/F with RB, SB	9 (-)	2-328
F747NQ	T-F/F with RB, SB Q Out	8 (-)	2-328
F765	T-F/F (TB) with RB	8 (-)	2-332
F765NQ	T-F/F (TB) with RB Q Out	7 (-)	2-332
F767	T-F/F (TB) with RB, SB	9 (-)	2-334
F767NQ	T-F/F (TB) with RB, SB Q Out	8 (-)	2-334
F771	JK-F/F	10 (-)	2-338
F771NB	JK-F/F QB Out	9 (-)	2-338
F771NQ	JK-F/F Q Out	9 (-)	2-338
F774	JK-F/F with R, S	12 (-)	2-342
F774NB	JK-F/F with R, S QB Out	11 (-)	2-342
F774NQ	JK-F/F with R, S Q Out	11 (-)	2-342
F775	JK-F/F with RB	11 (-)	2-344
F775NB	JK-F/F with RB QB Out	10 (-)	2-344
F775NQ	JK-F/F with RB Q Out	10 (-)	2-344
F776	JK-F/F with SB	11 (-)	2-346
F776NB	JK-F/F with SB QB Out	10 (-)	2-346
F776NQ	JK-F/F with SB Q Out	10 (-)	2-346
F777	JK-F/F with RB, SB	12 (-)	2-348
F777NB	JK-F/F with RB, SB QB Out	11 (-)	2-348
F777NQ	JK-F/F with RB, SB Q Out	11 (-)	2-348
F781	JK-F/F (CB)	10 (-)	2-350
F781NB	JK-F/F (CB) QB Out	9 (-)	2-350
F781NQ	JK-F/F (CB) Q Out	9 (-)	2-350
F787	JK-F/F (CB) with RB, SB	12 (-)	2-354
F787NB	JK-F/F (CB) with RB, SB QB Out	11 (-)	2-354
F787NQ	JK-F/F (CB) with RB, SB Q Out	11 (-)	2-354
F791	T-F/F with Data-Hold R, S	12 (-)	2-330
F792	T-F/F (TB) with Data-Hold RB, SB	12 (-)	2-336
F7D1	JK-F/F, High Speed	10 (-)	2-340
F7E1	JK-F/F (CB), High Speed	10 (-)	2-352
FC42	CTS Driver (Inverter Type) Single type	132 (-)	2-14
FC44	CTS Driver (Inverter Type) Double type	340 (-)	2-14
FC82	CTS Driver (Inverter Type) Single type, x2-drive	396 (-)	2-14
FC84	CTS Driver (Inverter Type) Double type, x2-drive	1020 (-)	2-14
FDA1	Input Buffer with failsafe 50kΩ Pull-down	3 (1)	1-6
FDA2	Input Buffer with failsafe 50kΩ Pull-down	3 (1)	1-66
FDE1W	Input Buffer with failsafe Schmitt 50kΩ Pull-down	6 (1)	1-6
FDE2W	Input Buffer with failsafe Schmitt 50kΩ Pull-down	6 (1)	1-66
FDS1W	Input Buffer Schmitt 50kΩ Pull-down	6 (1)	1-4
FDS2W	Input Buffer Schmitt 50kΩ Pull-down	6 (1)	1-64
FE01	Low-noise Output Buffer 9mA	5 (1)	1-14
FE02	Low-noise Output Buffer 12mA	5 (1)	1-14

Block	Function	Cells (I/O)	Page
FE03	Low-noise Output Buffer 18mA	5 (1)	1-14
FE04	Low-noise Output Buffer 6mA	5 (1)	1-14
FE06	Low-noise Output Buffer 24mA	5 (1)	1-14
FE09	Low-noise Output Buffer 3mA	5 (1)	1-14
FI01	Input Buffer	3 (1)	1-4
FI02	Input Buffer	3 (1)	1-64
FIA1	Input Buffer with failsafe	3 (1)	1-6
FIA2	Input Buffer with failsafe	3 (1)	1-66
FID1	Input Buffer 50k $\Omega$ Pull-down	3 (1)	1-4
FID2	Input Buffer 50k $\Omega$ Pull-down	3 (1)	1-64
FIE1W	Input Buffer with failsafe Schmitt	6 (1)	1-6
FIE2W	Input Buffer with failsafe Schmitt	6 (1)	1-66
FIS1W	Input Buffer Schmitt	6 (1)	1-4
FIS2W	Input Buffer Schmitt	6 (1)	1-64
FIU1	Input Buffer 50k $\Omega$ Pull-up	3 (1)	1-4
FIU2	Input Buffer 50k $\Omega$ Pull-up	3 (1)	1-64
FIW1	Input Buffer 5k $\Omega$ Pull-up	3 (1)	1-4
FIW2	Input Buffer 5k $\Omega$ Pull-up	3 (1)	1-64
FN11	Input Buffer with EN(AND)	6 (1)	1-8
FN12	Input Buffer with EN(AND)	7 (1)	1-68
FN13	Input Buffer with EN(OR)	4 (1)	1-10
FN14	Input Buffer with EN(OR)	4 (1)	1-70
FN21	Input Buffer with EN(AND) 50k $\Omega$ Pull-down	6 (1)	1-8
FN22	Input Buffer with EN(AND) 50k $\Omega$ Pull-down	7 (1)	1-68
FN23	Input Buffer with EN(OR) 50k $\Omega$ Pull-down	4 (1)	1-10
FN24	Input Buffer with EN(OR) 50k $\Omega$ Pull-down	4 (1)	1-70
FO01	Output Buffer 9mA	4 (1)	1-12
FO02	Output Buffer 12mA	12 (1)	1-12
FO03	Output Buffer 18mA	12 (1)	1-12
FO04	Output Buffer 6mA	4 (1)	1-12
FO06	Output Buffer 24mA	12 (1)	1-12
FO09	Output Buffer 3mA	4 (1)	1-12
FUS1W	Input Buffer Schmitt 50k $\Omega$ Pull-up	6 (1)	1-4
FUS2W	Input Buffer Schmitt 50k $\Omega$ Pull-up	6 (1)	1-64
FWS1W	Input Buffer Schmitt 5k $\Omega$ Pull-up	6 (1)	1-4
FWS2W	Input Buffer Schmitt 5k $\Omega$ Pull-up	6 (1)	1-64
L101	Inverter Single Out, Low Power	1 (-)	2-10
L111	Buffer Single Out, Low Power	1 (-)	2-12
L202	2-Input NOR Low Power	1 (-)	2-22
L203	3-Input NOR Low Power	2 (-)	2-24
L204	4-Input NOR Low Power	2 (-)	2-26
L205	5-Input NOR Low Power	4 (-)	2-28
L208	8-Input NOR Low Power	7 (-)	2-32

Block	Function	Cells (I/O)	Page
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L213	3-Input OR Low Power	2 (-)	2-36
L214	4-Input OR Low Power	3 (-)	2-38
L215	5-Input OR Low Power	4 (-)	2-40
L216	6-Input OR Low Power	4 (-)	2-42
L218	8-Input OR Low Power	6 (-)	2-44
L302	2-Input NAND Low Power	1 (-)	2-50
L303	3-Input NAND Low Power	2 (-)	2-52
L304	4-Input NAND Low Power	2 (-)	2-54
L312	2-Input AND Low Power	2 (-)	2-62
L313	3-Input AND Low Power	2 (-)	2-64
L314	4-Input AND Low Power	3 (-)	2-66
L315	5-Input AND Low Power	4 (-)	2-68
L316	6-Input AND Low Power	4 (-)	2-70
L318	8-Input AND Low Power	5 (-)	2-72
L421	1-2-Input AND-NOR Low Power	2 (-)	2-78
L422	1-1-2-Input AND-NOR Low Power	2 (-)	2-80
L423	1-3-Input AND-NOR Low Power	2 (-)	2-82
L424	2-2-Input AND-NOR Low Power	2 (-)	2-84
L425	2-2-2-Input AND-NOR Low Power	3 (-)	2-86
L427	2-3-Input AND-NOR Low Power	3 (-)	2-88
L428	1-2-2-Input AND-NOR Low Power	3 (-)	2-90
L429	2-2-2-2-Input AND-NOR Low Power	6 (-)	2-92
L430	1-4-Input OR-NAND Low Power	4 (-)	2-124
L431	1-2-Input OR-NAND Low Power	2 (-)	2-126
L432	1-1-2-Input OR-NAND Low Power	2 (-)	2-128
L433	1-3-Input OR-NAND Low Power	2 (-)	2-130
L434	2-2-Input OR-NAND Low Power	2 (-)	2-132
L436	3-3-Input OR-NAND Low Power	3 (-)	2-136
L439	1-5-Input OR-NAND Low Power	5 (-)	2-142
L440	1-4-Input AND-NOR Low Power	3 (-)	2-94
L441	1-5-Input AND-NOR Low Power	5 (-)	2-96
L444	4-4-4-Input AND-NOR Low Power	8 (-)	2-98
L446	1-1-1-2-Input AND-NOR Low Power	4 (-)	2-100
L447	1-1-1-3-Input AND-NOR Low Power	5 (-)	2-102
L448	1-1-2-2-Input AND-NOR Low Power	5 (-)	2-104
L450	2-4-Input OR-NAND Low Power	5 (-)	2-144
L451	4-4-Input OR-NAND Low Power	7 (-)	2-146
L452	1-1-3-Input OR-NAND Low Power	4 (-)	2-148
L453	1-1-4-Input OR-NAND Low Power	5 (-)	2-150
L458	1-1-1-2-Input OR-NAND Low Power	3 (-)	2-154
L459	1-1-1-3-Input OR-NAND Low Power	5 (-)	2-156
L460	3-3-3-Input AND-NOR Low Power	6 (-)	2-108



Block	Function	Cells (I/O)	Page
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L491	1-2-3-Input OR-NAND Low Power	5 (-)	2-160
L493	3-3-3-Input OR-NAND Low Power	6 (-)	2-162
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L517	3-Input Exclusive NOR Low Power	7 (-)	2-180
L531	3-State Buffer with EN, Low Power	4 (-)	2-198
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L601	D-Latch Q Out, Low Power	4 (-)	2-234
L602	D-Latch with R Q Out, Low Power	5 (-)	2-238
L603	D-Latch with RB Q Out, Low Power	5 (-)	2-242
L604	D-Latch (GB) Q Out, Low Power	4 (-)	2-252
L605	D-Latch (GB) with RB Q Out, Low Power	5 (-)	2-256
L606	BScan D-Latch with SB Q Out, Low Power	5 (-)	4-30
L641	D-F/F Q Out, Low Power	6 (-)	2-264
L644	D-F/F with R, S Q Out, Low Power	8 (-)	2-270
L645	D-F/F with RB Q Out, Low Power	7 (-)	2-272
L647	D-F/F with RB, SB Q Out, Low Power	8 (-)	2-276
L661	D-F/F (CB) Q Out, Low Power	6 (-)	2-278
L667	D-F/F (CB) with RB, SB Q Out, Low Power	8 (-)	2-284
L744	T-F/F with R, S Q Out, Low Power	7 (-)	2-324
L747	T-F/F with RB, SB Q Out, Low Power	7 (-)	2-328
L767	T-F/F (TB) with RB, SB Q Out, Low Power	7 (-)	2-334
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OSI2	Oscillator Input Buffer for Enable	0 (1)	1-110
OSI4	Oscillator Input Buffer for OSO9	0 (1)	1-112
OSO1	Oscillator Output Buffer (Internal Feedback Resistor)	0 (1)	1-114
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S000	Scan D-F/F with R, S, 2 to 1 Selector	12 (-)	3-4
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S003	Scan D-F/F with 2 to 1 Selector, High Speed	11 (-)	3-8
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S052	Scan D-F/F with Hold, 2 to 1 Selector	14 (-)	3-12
S100	Scan JK-F/F with R, S, D-F/F Function	14 (-)	3-14
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Block	Function	Cells (I/O)	Page
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S202	Scan D-Latch with D-F/F Function	12 (-)	3-24
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SBM5	BScan Instruction Register	140 (-)	4-52
SBM6	BScan Instruction Decoder	24 (-)	4-54
SBMC	BScan Instruction Decoder with NEC Scan	37 (-)	4-56
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SCD1	Clock Distributor	8 (-)	3-66
SCDC	Clock Distributor with Test (Positive Clock)	2 (-)	3-68
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SCI1	Common Input	2 (-)	3-90
SCKG	Clock Generator	16 (-)	3-88
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SE602	NEC Scan D-Latch with R	14 (-)	3-40
SE603	NEC Scan D-Latch with RB	14 (-)	3-42
SE604	NEC Scan D-Latch(GB)	13 (-)	3-44
SE605	NEC Scan D-Latch(GB) with RB	14 (-)	3-46
SE611	NEC Scan D-F/F	11 (-)	3-48
SE614	NEC Scan D-F/F with R, S	13 (-)	3-50
SE615	NEC Scan D-F/F with RB	12 (-)	3-52
SE616	NEC Scan D-F/F with SB	12 (-)	3-54
SE617	NEC Scan D-F/F with RB, SB	13 (-)	3-56
SE631	NEC Scan D-F/F (CB)	11 (-)	3-58
SE637	NEC Scan D-F/F (CB) with RB, SB	13 (-)	3-60
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SFEL	I/F Control (AMC) with ENB	2 (-)	3-74
SGND	GND	2 (-)	3-94
SMS1	Mega Macro Skip	4 (-)	3-80
SOEH	I/F Control (SMC) with EN	3 (-)	3-76
SOEL	I/F Control (SMC) with ENB	2 (-)	3-78

Block	Function	Cells (I/O)	Page
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SRL1	Set-B/Reset-B Control	2 (-)	3-84
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SVRN32	BScan Data Register for 3-state	50 (-)	4-22
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SVRNI2	BScan Data Register for Input	12 (-)	4-18
SVSNA2	BScan Data Selector for Output	7 (-)	4-36
SVSNB2	BScan Data Selector for Bid	7 (-)	4-38
SVSNC2	BScan Data Enable Selector for 3-state	9 (-)	4-40
SVSNE2	BScan Data Enable Selector for Bid	9 (-)	4-42

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