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## カタログ等資料中の旧社名の扱いについて

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ルネサスエレクトロニクス ホームページ (<http://www.renesas.com>)

2010年4月1日  
ルネサスエレクトロニクス株式会社

【発行】ルネサスエレクトロニクス株式会社 (<http://www.renesas.com>)

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高品質水準： 輸送機器（自動車、電車、船舶等）、交通用信号機器、防災・防犯装置、各種安全装置、生命維持を目的として設計されていない医療機器（厚生労働省定義の管理医療機器に相当）  
特定水準： 航空機器、航空宇宙機器、海底中継機器、原子力制御システム、生命維持のための医療機器（生命維持装置、人体に埋め込み使用するもの、治療行為（患部切り出し等）を行うもの、その他直接人命に影響を与えるもの）（厚生労働省定義の高度管理医療機器に相当）またはシステム等
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**Block Library**

# **CMOS-N5 Family**

**CMOS Gate Array**

**(3.3 V) Ver.1.0**

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[MEMO]

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    - 特別水準：輸送機器（自動車、列車、船舶等）、交通信号機器、防災／防犯装置、各種安全装置、生命維持を直接の目的としない医療機器
    - 特定水準：航空機器、航空宇宙機器、海底中継機器、原子力制御システム、生命維持のための医療機器、生命維持のための装置またはシステム等
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巻末にアンケート・コーナーを設けております。このドキュメントに対するご意見をお気軽にお寄せください。

# はじめに

このマニュアルはCMOS-N5ファミリの3.3 Vのブロックについて記載しています。5.0 VのブロックについてはCMOS-N5 Family (5.0 V) Block Library (A13872J) を参照してください。

回路設計を行う際には必ず先にCMOS-N5ファミリ **設計マニュアル** (A13826J) を読んでください。

またマニュアルに記載された事項(一般事項, 注意事項, 制限事項)は必ずお守りください。お守りいただけない場合, LSI製品の品質や性能の低下, および動作の異常が生じることがあります。



# 1. 構 成

このマニュアルは次のような構成になっています。

## (1) はじめに

このマニュアルを活用されるにあたっての注意事項，用語，定義などを説明しています。

## (2) Contents

目次としてブロックを機能別にまとめてあります。

## (3) Chapter 1 Interface Block

## (4) Chapter 2 Function Block

## (5) Chapter 3 Scan Path Block

## (6) Chapter 4 Boundary Scan Block

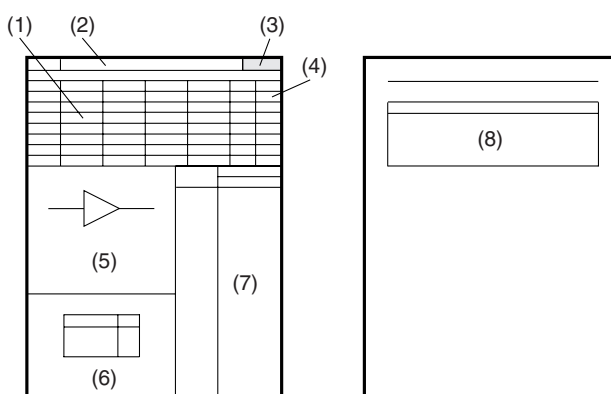
Chapter 1～4は，それぞれのブロックを機能順に並べてあります。各ページには，論理シンボル，真理値表，入出力データ，スイッチング・スピード（伝達遅延時間）などを2. **ブロック・ライブラリ記載内容の説明**に添って記載してあります。

## (7) Index

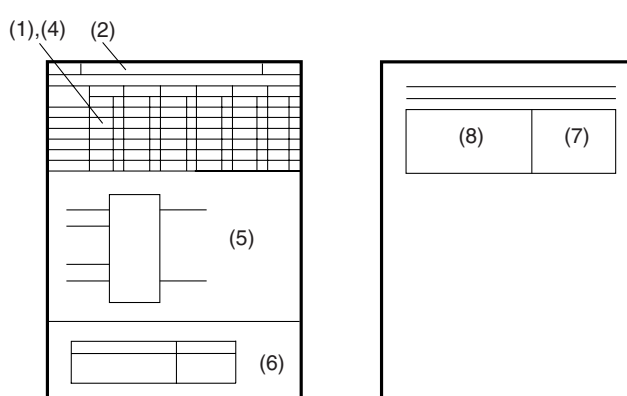
索引としてブロックをアルファベット順にまとめてあります。

## 2. ブロック・ライブラリ記載内容の説明

(a) インタフェース・ブロック

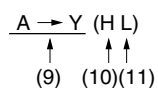


(b) ファンクション・ブロック



- |                       |  |
|-----------------------|--|
| (1) Block type        | : 機能ブロックの名称                                      |
| (2) Function          | : そのブロックの機能名                                     |
| (3) Interface level   | : そのブロックのインタフェース・レベル                             |
| (4) No. of int. cells | : 使用セル数 (内部セル数)                                  |
| (5) Logic Diagram     | : そのブロックの論理シンボル (論理図)                            |
| (6) Truth Table       | : そのブロックの真理値表                                    |
| (7) Input, Output     | : Input (入力端子名, Fan-in), Output (出力端子名, Fan-out) |
| (8) Switching speed   | : そのブロックの伝達遅延時間など                                |

なお、スイッチング・スピードの記号は次のとおりです。



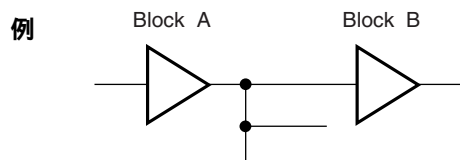
- |              |                                       |
|--------------|---------------------------------------|
| (9) 信号のパス名   | (入力 出力)                               |
| (10) 入力信号の状態 | (H: ハイ・レベル, L: ロウ・レベル, Z: ハイ・インピーダンス) |
| (11) 出力信号の状態 | (H: ハイ・レベル, L: ロウ・レベル, Z: ハイ・インピーダンス) |

Setup time, Hold time, Release time, Removal time, Minimum pulse widthはMIN.条件での最小値をMIN.の欄に, またMAX.条件での最小値をMAX.の欄に記載しています。

### 3. 伝達遅延時間 (t<sub>PD</sub>)

ここで示す計算式は、簡易的に計算するための概略計算式です。この計算式では特に負荷が次の条件を満足する範囲での算出結果が比較的精度よく求められるようになっていました。負荷容量が大きいほど誤差が大きくなり、シミュレータの結果より小さい値を算出します。あらかじめ、ご承知のうえ目安としてご利用ください。

**条件** 遅延計算対象ブロックの前段F/Iの合計が、前段の駆動ブロックF/O制限の15%以内である。



ブロックBが遅延計算対象のブロックとするとブロックAの出力に接続されるF/Iの合計がブロックAのF/O制限15%以内のとき、簡易計算式の精度が高い。

#### 3.1 伝達遅延時間の概算式

##### 3.1.1 入力バッファと内部ファンクション・ブロックの遅延時間

入力バッファと内部ファンクション・ブロックの遅延時間は、メモリ・ブロックを含み、そのブロックに接続されている負荷（ファンアウト数）とその配線長（配線容量）から概算できます。

$$t_{PD} = t_{LD0} + (\Sigma F/O + L) \times t_1 \quad (\text{ns})$$

- $t_{LD0}$  : F/O = 0, L = 0におけるブロック自身の遅延時間  
 $\Sigma F/O$  : 該当出力端子のファンアウト数  
L : 該当出力端子の配線容量 (3.1.3 予測配線容量参照)  
 $t_1$  : 該当出力端子の遅延係数

##### 3.1.2 出力バッファの遅延時間

出力バッファの遅延時間は、その出力端子に接続されている負荷容量によって大きく変わります。また、遅延時間の負荷容量依存性はそのバッファ駆動能力によっても変わります。

出力バッファの遅延時間 (t<sub>PD</sub>) は、負荷容量 (C<sub>L</sub>) に対して次の公式で概算できます。

$$t_{PD} = t_{LD0} + T \times C_L \quad (\text{ns})$$

- $t_{LD0}$  : 基準遅延時間 (ns)  
T : 遅延係数  
C<sub>L</sub> : 負荷容量 (pF) (ただし, C<sub>L</sub> 15 pF)

なお、入出力バッファの遅延時間は、次の条件下で求められています。

CMOSレベル・インタフェース : スレッシユホールド電圧 = 1/2 V<sub>DD</sub>

### 3.1.3 予測配線容量

CMOS-N5ファミリの予測配線容量は次のようになります。

#### 予測配線容量（配線長をFan-in値に換算）

(1/2)

品名	ピン・ペア数					
	1	2	3	4	5	6
μ PD65880	1.621	3.266	4.911	6.556	8.200	9.845
μ PD65881	1.641	3.356	5.070	6.785	8.500	10.214
μ PD65882	1.684	3.552	5.421	7.289	9.158	11.027
μ PD65883	1.730	3.767	5.803	7.840	9.876	11.913
μ PD65884	1.757	3.892	6.026	8.161	10.295	12.430
μ PD65885	1.780	3.997	6.213	8.430	10.647	12.863
μ PD65887	1.819	4.175	6.532	8.889	11.245	13.602
μ PD65889	1.861	4.372	6.883	9.393	11.904	14.414
μ PD65890	1.904	4.569	7.233	9.897	12.562	15.226
μ PD65893	1.943	4.747	7.552	10.356	13.160	15.965

(2/2)

品名	ピン・ペア数					
	7	8	9	10	11 to 15	16 to 20
μ PD65880	11.490	13.135	14.779	16.424	24.648	32.871
μ PD65881	11.929	13.644	15.358	17.073	25.647	34.220
μ PD65882	12.895	14.764	16.632	18.501	27.844	37.187
μ PD65883	13.949	15.986	18.022	20.059	30.241	40.424
μ PD65884	14.564	16.699	18.833	20.967	31.640	42.312
μ PD65885	15.080	17.297	19.513	21.730	32.813	43.897
μ PD65887	15.958	18.315	20.672	23.028	34.811	46.594
μ PD65889	16.925	19.435	21.946	24.456	37.009	49.561
μ PD65890	17.891	20.555	23.220	25.884	39.206	52.528
μ PD65893	18.769	21.574	24.378	27.182	41.204	55.226

## 4. 入力インタフェース・レベル

次の4種類の入力インタフェース・レベルを用意してあります。用途に合わせて最適なものを選択してください。

- (1) CMOS レベル入力
- (2) TTL レベル入力
- (3) CMOS シュミット入力
- (4) TTL シュミット入力

## 5. 出力駆動能力

次のような出力駆動能力が異なるバッファを多数用意していますので、用途にあわせて最適なものを選択してください。

CMOS レベル出力 (6 種類) : 3.0 mA, 6.0 mA, 9.0 mA, 12.0 mA, 18.0 mA, 24.0 mA

## 6. 高性能バッファ

### 6.1 プルアップ/プルダウン抵抗付きバッファ

入力/出力/双方向バッファに次のようなプルアップ抵抗付き,プルダウン抵抗付きのものを用意しています。用途にあわせて最適なものを選択してください。

- (1) プルアップ抵抗 : 50 k $\Omega$  (TYP)
- (2) プルダウン抵抗 : 50 k $\Omega$  (TYP)
- (3) プルアップ抵抗 : 5 k $\Omega$  (TYP)

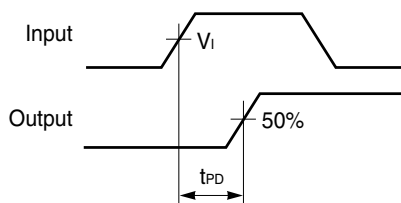
### 6.2 ロウ・スルーレート・バッファ

スルーレートを低くし,ロウ・ノイズ化を図った出力/双方向バッファを用意しており,ロウ・スルーレート・バッファと呼びます。なお,このマニュアルではLow-noiseと表示します。

## 7. 伝達遅延時間の定義

入力/出力バッファの伝達遅延時間は、次の定義による値を記載しています。

### (1) 入力バッファ

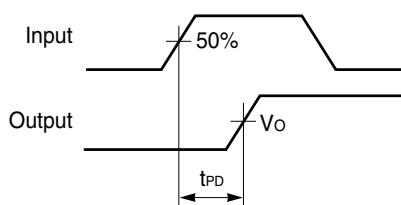


$V_i = 2.5 \text{ V}$  (CMOSレベル)

$V_i = 1.5 \text{ V}$  (TTLレベル)

(内部電圧幅)  $\times 50\%$

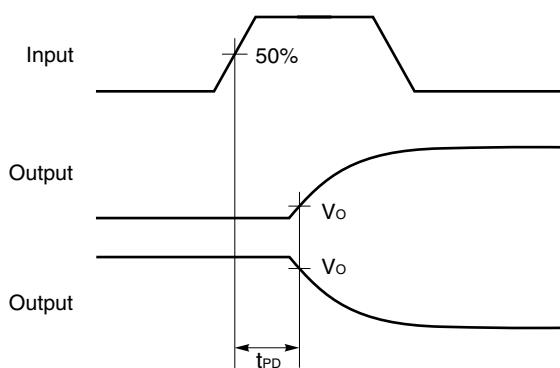
### (2) 出力バッファ (L H, H L, Z H (初期 $V_o = \text{“L”}$ レベル), Z L (初期 $V_o = \text{“H”}$ レベル))



(内部電圧幅)  $\times 50\%$

$V_o = 2.5 \text{ V}$  (CMOSレベル)

### (3) 出力バッファ (L Z, H Z)



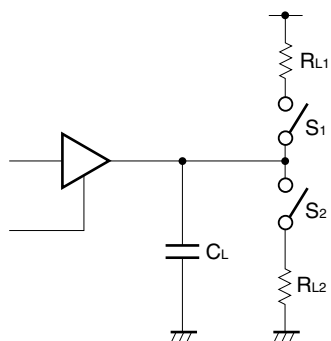
(内部電圧幅)  $\times 50\%$

$V_o = 0.1 \times V_{DD}$  (L Z)

$V_o = 1.2 \times V_{DD}$  (H Z)

## 8. 測定負荷条件

### CMOS レベル出力バッファ



#### (a) 通常出力バッファ

$R_{L1}, R_{L2} = \infty, C_L = 15 \text{ pF}$

(  $S_1, S_2$  : OFF )

#### (b) 3ステート出力バッファ

$R_{L1} = 2 \text{ k}\Omega, R_{L2} = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$

$t_{P(HH)}, t_{P(LL)}$  :  $S_1 = \text{OFF}, S_2 = \text{OFF}$

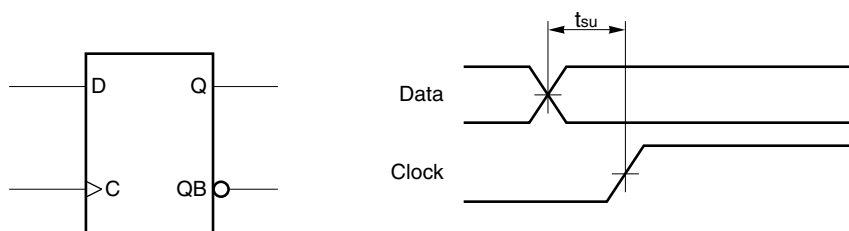
$t_{P(ZL)}, t_{P(LZ)}$  :  $S_1 = \text{ON}, S_2 = \text{OFF}$

$t_{P(ZH)}, t_{P(HZ)}$  :  $S_1 = \text{OFF}, S_2 = \text{ON}$

## 9. タイミング

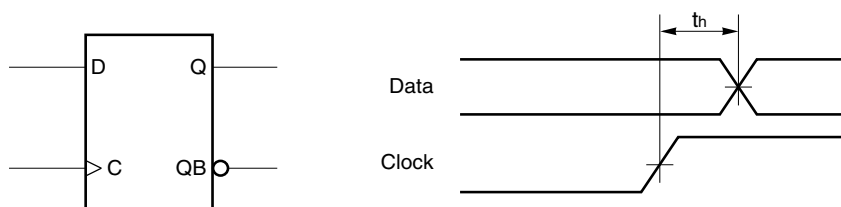
### (1) セットアップ・タイム ( $t_{su}$ )

D-F/Fなどで、クロックが変化する前にデータ信号が確定していなければならない時間。



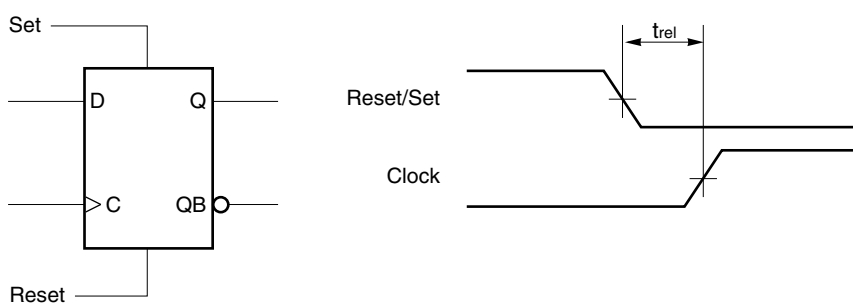
### (2) ホールド・タイム ( $t_h$ )

D-F/Fなどで、クロックが変化したあとにデータ信号を保持していなければならない時間。



### (3) リリース・タイム ( $t_{rel}$ )

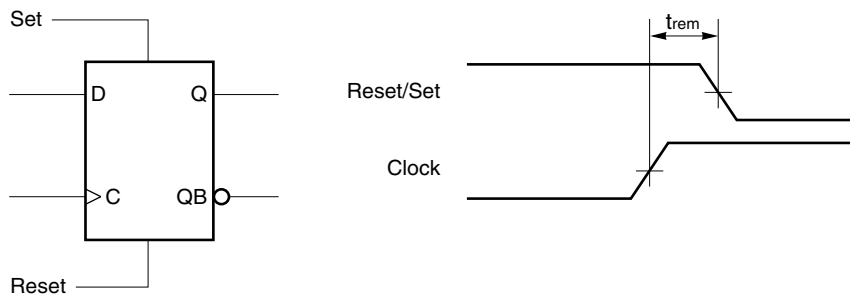
D-F/Fなどで、リセットかセットが解除になってからクロックが有効になるまでの時間。





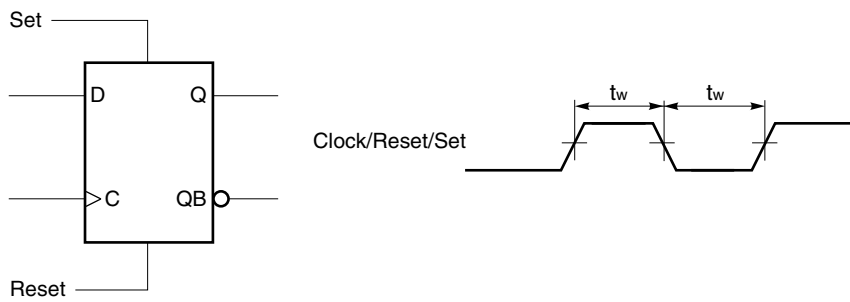
#### (4) リムーバル・タイム ( $t_{rem}$ )

D-F/Fなどで、クロックを無効にするまでのセットまたはリセットの保持時間。



#### (5) 最小パルス幅 ( $t_w$ )

D-F/Fなどで、データを正常に読み込むために必要となるクロック、リセット、セットのパルス幅の最小時間。



## 関連資料

関連資料は暫定版の場合もありますが、この資料では [ 暫定 ] の表示をしておりません。あらかじめご了承ください。

CMOS-N5 ファミリ 設計マニュアル	: A13826J
CMOS-N5 ファミリ 設計マニュアル メガマクロ編	: A14759J
CMOS-N5 Family ( 5.0 V ) Block Library	: A13872J
CMOS-N5 Family ( 3.3 V ) Block Library	: このマニュアル
CMOS-N5 Family Memory Block Library	: A14683J
テスト容易化設計 ユーザーズ・マニュアル	: A14357J
半導体総合セレクション・ガイド -製品・パッケージ情報-	: X13769J

設計する際は最新の資料を使用させていただくため、NEC販売担当または  
特約店にご確認ください。

# Contents

## Chapter 1 Interface Block

### 1.1 CMOS Level

Function	Block	Description	Cells (I/O)	Page
Input Buffer	FI01	-	3 (1)	1-4
	FID1	50k $\Omega$ Pull-down	3 (1)	
	FIU1	50k $\Omega$ Pull-up	3 (1)	
	FIW1	5k $\Omega$ Pull-up	3 (1)	
	FIS1W	Schmitt	6 (1)	
	FDS1W	Schmitt 50k $\Omega$ Pull-down	6 (1)	
	FUS1W	Schmitt 50k $\Omega$ Pull-up	6 (1)	
	FWS1W	Schmitt 5k $\Omega$ Pull-up	6 (1)	
Input Buffer with failsafe	FIA1	-	3 (1)	1-6
	FDA1	50k $\Omega$ Pull-down	3 (1)	
	FIE1W	Schmitt	6 (1)	
	FDE1W	Schmitt 50k $\Omega$ Pull-down	6 (1)	
Input Buffer with EN(AND)	FN11	-	6 (1)	1-8
	FN21	50k $\Omega$ Pull-down	6 (1)	
Input Buffer with EN(OR)	FN13	-	4 (1)	1-10
	FN23	50k $\Omega$ Pull-down	4 (1)	
Output Buffer	FO09	3mA	4 (1)	1-12
	FO04	6mA	4 (1)	
	FO01	9mA	4 (1)	
	FO02	12mA	12 (1)	
	FO03	18mA	12 (1)	
	FO06	24mA	12 (1)	
Low-noise Output Buffer	FE09	3mA	5 (1)	1-14
	FE04	6mA	5 (1)	
	FE01	9mA	5 (1)	
	FE02	12mA	5 (1)	
	FE03	18mA	5 (1)	
	FE06	24mA	5 (1)	

Function	Block	Description	Cells (I/O)	Page
3-State Buffer	B00T	3mA	7 (1)	1-16
	B0DT	3mA 50kΩ Pull-down	7 (1)	
	B0UT	3mA 50kΩ Pull-up	7 (1)	
	B0WT	3mA 5kΩ Pull-up	7 (1)	
	B00E	6mA	7 (1)	
	B0DE	6mA 50kΩ Pull-down	7 (1)	
	B0UE	6mA 50kΩ Pull-up	7 (1)	
	B0WE	6mA 5kΩ Pull-up	7 (1)	
	B008	9mA	7 (1)	
	B0D8	9mA 50kΩ Pull-down	7 (1)	
	B0U8	9mA 50kΩ Pull-up	7 (1)	
	B0W8	9mA 5kΩ Pull-up	7 (1)	
	B007	12mA	17 (1)	
	B0D7	12mA 50kΩ Pull-down	17 (1)	
	B0U7	12mA 50kΩ Pull-up	17 (1)	
	B0W7	12mA 5kΩ Pull-up	17 (1)	
	B009	18mA	17 (1)	
	B0D9	18mA 50kΩ Pull-down	17 (1)	
	B0U9	18mA 50kΩ Pull-up	17 (1)	
	B0W9	18mA 5kΩ Pull-up	17 (1)	
	B00H	24mA	17 (1)	
	B0DH	24mA 50kΩ Pull-down	17 (1)	
	B0UH	24mA 50kΩ Pull-up	17 (1)	
	B0WH	24mA 5kΩ Pull-up	17 (1)	

Function	Block	Description	Cells (I/O)	Page
Low-noise 3-State Buffer	BE0T	3mA	7 (1)	1-20
	BEDT	3mA 50kΩ Pull-down	7 (1)	
	BEUT	3mA 50kΩ Pull-up	7 (1)	
	BEWT	3mA 5kΩ Pull-up	7 (1)	
	BE0E	6mA	7 (1)	
	BEDE	6mA 50kΩ Pull-down	7 (1)	
	BEUE	6mA 50kΩ Pull-up	7 (1)	
	BEWE	6mA 5kΩ Pull-up	7 (1)	
	BE08	9mA	7 (1)	
	BED8	9mA 50kΩ Pull-down	7 (1)	
	BEU8	9mA 50kΩ Pull-up	7 (1)	
	BEW8	9mA 5kΩ Pull-up	7 (1)	
	BE07	12mA	7 (1)	
	BED7	12mA 50kΩ Pull-down	7 (1)	
	BEU7	12mA 50kΩ Pull-up	7 (1)	
	BEW7	12mA 5kΩ Pull-up	7 (1)	
	BE09	18mA	7 (1)	
	BED9	18mA 50kΩ Pull-down	7 (1)	
	BEU9	18mA 50kΩ Pull-up	7 (1)	
	BEW9	18mA 5kΩ Pull-up	7 (1)	
	BE0H	24mA	7 (1)	
	BEDH	24mA 50kΩ Pull-down	7 (1)	
	BEUH	24mA 50kΩ Pull-up	7 (1)	
	BEWH	24mA 5kΩ Pull-up	7 (1)	
N-ch open drain Buffer	EXT1	9mA	4 (1)	1-24
	EXT3	9mA 50kΩ Pull-up	4 (1)	
	EXW3	9mA 5kΩ Pull-up	4 (1)	
	EXT9	12mA	4 (1)	
	EXTB	12mA 50kΩ Pull-up	4 (1)	
	EXWB	12mA 5kΩ Pull-up	4 (1)	
	EXT5	18mA	4 (1)	
	EXT7	18mA 50kΩ Pull-up	4 (1)	
	EXW7	18mA 5kΩ Pull-up	4 (1)	
	EXTD	24mA	4 (1)	
	EXTF	24mA 50kΩ Pull-up	4 (1)	
	EXWF	24mA 5kΩ Pull-up	4 (1)	
	N-ch open drain Buffer with failsafe	EXO1	9mA	
EXO9		12mA	4 (1)	
EXO5		18mA	4 (1)	
EXOD		24mA	4 (1)	

Function	Block	Description	Cells (I/O)	Page
N-ch open drain I/O Buffer with failsafe	EBA1	9mA	7 (1)	1-28
	EBA9	12mA	7 (1)	
	EBA5	18mA	7 (1)	
	EBAD	24mA	7 (1)	
N-ch open drain Schmitt I/O Buffer with failsafe	EBE1W	9mA	10 (1)	1-30
	EBE9W	12mA	10 (1)	
	EBE5W	18mA	10 (1)	
	EBEDW	24mA	10 (1)	
I/O Buffer	B00U	3mA	10 (1)	1-32
	B0DU	3mA 50k $\Omega$ Pull-down	10 (1)	
	B0UU	3mA 50k $\Omega$ Pull-up	10 (1)	
	B0WU	3mA 5k $\Omega$ Pull-up	10 (1)	
	B00C	6mA	10 (1)	
	B0DC	6mA 50k $\Omega$ Pull-down	10 (1)	
	B0UC	6mA 50k $\Omega$ Pull-up	10 (1)	
	B0WC	6mA 5k $\Omega$ Pull-up	10 (1)	
	B003	9mA	10 (1)	
	B0D3	9mA 50k $\Omega$ Pull-down	10 (1)	
	B0U3	9mA 50k $\Omega$ Pull-up	10 (1)	
	B0W3	9mA 5k $\Omega$ Pull-up	10 (1)	
	B001	12mA	20 (1)	
	B0D1	12mA 50k $\Omega$ Pull-down	20 (1)	
	B0U1	12mA 50k $\Omega$ Pull-up	20 (1)	
	B0W1	12mA 5k $\Omega$ Pull-up	20 (1)	
	B005	18mA	20 (1)	
	B0D5	18mA 50k $\Omega$ Pull-down	20 (1)	
	B0U5	18mA 50k $\Omega$ Pull-up	20 (1)	
	B0W5	18mA 5k $\Omega$ Pull-up	20 (1)	
B00F	24mA	20 (1)		
B0DF	24mA 50k $\Omega$ Pull-down	20 (1)		
B0UF	24mA 50k $\Omega$ Pull-up	20 (1)		
B0WF	24mA 5k $\Omega$ Pull-up	20 (1)		

Function	Block	Description	Cells (I/O)	Page
Low-noise I/O Buffer	BE0U	3mA	10 (1)	1-38
	BEDU	3mA 50k $\Omega$ Pull-down	10 (1)	
	BEUU	3mA 50k $\Omega$ Pull-up	10 (1)	
	BEWU	3mA 5k $\Omega$ Pull-up	10 (1)	
	BE0C	6mA	10 (1)	
	BEDC	6mA 50k $\Omega$ Pull-down	10 (1)	
	BEUC	6mA 50k $\Omega$ Pull-up	10 (1)	
	BEWC	6mA 5k $\Omega$ Pull-up	10 (1)	
	BE03	9mA	10 (1)	
	BED3	9mA 50k $\Omega$ Pull-down	10 (1)	
	BEU3	9mA 50k $\Omega$ Pull-up	10 (1)	
	BEW3	9mA 5k $\Omega$ Pull-up	10 (1)	
	BE01	12mA	10 (1)	
	BED1	12mA 50k $\Omega$ Pull-down	10 (1)	
	BEU1	12mA 50k $\Omega$ Pull-up	10 (1)	
	BEW1	12mA 5k $\Omega$ Pull-up	10 (1)	
	BE05	18mA	10 (1)	
	BED5	18mA 50k $\Omega$ Pull-down	10 (1)	
	BEU5	18mA 50k $\Omega$ Pull-up	10 (1)	
	BEW5	18mA 5k $\Omega$ Pull-up	10 (1)	
	BE0F	24mA	10 (1)	
	BEDF	24mA 50k $\Omega$ Pull-down	10 (1)	
	BEUF	24mA 50k $\Omega$ Pull-up	10 (1)	
	BEWF	24mA 5k $\Omega$ Pull-up	10 (1)	

Function	Block	Description	Cells (I/O)	Page
Schmitt I/O Buffer	BSIUW	3mA	13 (1)	1-44
	BSDUW	3mA 50k $\Omega$ Pull-down	13 (1)	
	BSUUW	3mA 50k $\Omega$ Pull-up	13 (1)	
	BSWUW	3mA 5k $\Omega$ Pull-up	13 (1)	
	BSICW	6mA	13 (1)	
	BSDCW	6mA 50k $\Omega$ Pull-down	13 (1)	
	BSUCW	6mA 50k $\Omega$ Pull-up	13 (1)	
	BSWCW	6mA 5k $\Omega$ Pull-up	13 (1)	
	BSI3W	9mA	13 (1)	
	BSD3W	9mA 50k $\Omega$ Pull-down	13 (1)	
	BSU3W	9mA 50k $\Omega$ Pull-up	13 (1)	
	BSW3W	9mA 5k $\Omega$ Pull-up	13 (1)	
	BSI1W	12mA	23 (1)	
	BSD1W	12mA 50k $\Omega$ Pull-down	23 (1)	
	BSU1W	12mA 50k $\Omega$ Pull-up	23 (1)	
	BSW1W	12mA 5k $\Omega$ Pull-up	23 (1)	
	BSI5W	18mA	23 (1)	
	BSD5W	18mA 50k $\Omega$ Pull-down	23 (1)	
	BSU5W	18mA 50k $\Omega$ Pull-up	23 (1)	
	BSW5W	18mA 5k $\Omega$ Pull-up	23 (1)	
	BSIFW	24mA	23 (1)	
	BSDFW	24mA 50k $\Omega$ Pull-down	23 (1)	
	BSUFW	24mA 50k $\Omega$ Pull-up	23 (1)	
	BSWFW	24mA 5k $\Omega$ Pull-up	23 (1)	



Function	Block	Description	Cells (I/O)	Page
Low-noise Schmitt I/O Buffer	BFIUW	3mA	13 (1)	1-50
	BFDUW	3mA 50kΩ Pull-down	13 (1)	
	BFUUW	3mA 50kΩ Pull-up	13 (1)	
	BFWUW	3mA 5kΩ Pull-up	13 (1)	
	BFICW	6mA	13 (1)	
	BFDCW	6mA 50kΩ Pull-down	13 (1)	
	BFUCW	6mA 50kΩ Pull-up	13 (1)	
	BFWCW	6mA 5kΩ Pull-up	13 (1)	
	BFI3W	9mA	13 (1)	
	BFD3W	9mA 50kΩ Pull-down	13 (1)	
	BFU3W	9mA 50kΩ Pull-up	13 (1)	
	BFW3W	9mA 5kΩ Pull-up	13 (1)	
	BF11W	12mA	13 (1)	
	BFD1W	12mA 50kΩ Pull-down	13 (1)	
	BFU1W	12mA 50kΩ Pull-up	13 (1)	
	BFW1W	12mA 5kΩ Pull-up	13 (1)	
	BF15W	18mA	13 (1)	
	BFD5W	18mA 50kΩ Pull-down	13 (1)	
	BFU5W	18mA 50kΩ Pull-up	13 (1)	
	BFW5W	18mA 5kΩ Pull-up	13 (1)	
	BF1FW	24mA	13 (1)	
	BFDFW	24mA 50kΩ Pull-down	13 (1)	
	BFUFW	24mA 50kΩ Pull-up	13 (1)	
	BFWFW	24mA 5kΩ Pull-up	13 (1)	
I/O Buffer with EN(AND)	BN2U	3mA	13 (1)	1-56
	BN4U	3mA 50kΩ Pull-down	13 (1)	
	BN2C	6mA	13 (1)	
	BN4C	6mA 50kΩ Pull-down	13 (1)	
	BN23	9mA	13 (1)	
	BN43	9mA 50kΩ Pull-down	13 (1)	
	BN21	12mA	23 (1)	
	BN41	12mA 50kΩ Pull-down	23 (1)	
	BN25	18mA	23 (1)	
	BN45	18mA 50kΩ Pull-down	23 (1)	
	BN2F	24mA	23 (1)	
	BN4F	24mA 50kΩ Pull-down	23 (1)	

Function	Block	Description	Cells (I/O)	Page
I/O Buffer with EN(OR)	BN3U	3mA	11 (1)	1-60
	BN5U	3mA 50kΩ Pull-down	11 (1)	
	BN3C	6mA	11 (1)	
	BN5C	6mA 50kΩ Pull-down	11 (1)	
	BN33	9mA	11 (1)	
	BN53	9mA 50kΩ Pull-down	11 (1)	
	BN31	12mA	21 (1)	
	BN51	12mA 50kΩ Pull-down	21 (1)	
	BN35	18mA	21 (1)	
	BN55	18mA 50kΩ Pull-down	21 (1)	
	BN3F	24mA	21 (1)	
	BN5F	24mA 50kΩ Pull-down	21 (1)	

## 1.2 TTL Level

Function	Block	Description	Cells (I/O)	Page
Input Buffer	FI02	-	3 (1)	1-68
	FID2	50kΩ Pull-down	3 (1)	
	FIU2	50kΩ Pull-up	3 (1)	
	FIW2	5kΩ Pull-up	3 (1)	
	FIS2W	Schmitt	6 (1)	
	FDS2W	Schmitt 50kΩ Pull-down	6 (1)	
	FUS2W	Schmitt 50kΩ Pull-up	6 (1)	
	FWS2W	Schmitt 5kΩ Pull-up	6 (1)	
Input Buffer with failsafe	FIA2	-	3 (1)	1-70
	FDA2	50kΩ Pull-down	3 (1)	
	FIE2W	Schmitt	6 (1)	
	FDE2W	Schmitt 50kΩ Pull-down	6 (1)	
Input Buffer with EN(AND)	FN12	-	7 (1)	1-72
	FN22	50kΩ Pull-down	7 (1)	
Input Buffer with EN(OR)	FN14	-	4 (1)	1-74
	FN24	50kΩ Pull-down	4 (1)	
N-ch open drain I/O Buffer with failsafe	EBA2	9mA	7 (1)	1-76
	EBAA	12mA	7 (1)	
	EBA6	18mA	7 (1)	
	EBAE	24mA	7 (1)	
N-ch open drain Schmitt I/O Buffer with failsafe	EBE2W	9mA	10 (1)	1-78
	EBEAW	12mA	10 (1)	
	EBE6W	18mA	10 (1)	
	EBEEW	24mA	10 (1)	

Function	Block	Description	Cells (I/O)	Page
I/O Buffer	B00V	3mA	10 (1)	1-80
	B0DV	3mA 50k $\Omega$ Pull-down	10 (1)	
	B0UV	3mA 50k $\Omega$ Pull-up	10 (1)	
	B0WV	3mA 5k $\Omega$ Pull-up	10 (1)	
	B00D	6mA	10 (1)	
	B0DD	6mA 50k $\Omega$ Pull-down	10 (1)	
	B0UD	6mA 50k $\Omega$ Pull-up	10 (1)	
	B0WD	6mA 5k $\Omega$ Pull-up	10 (1)	
	B004	9mA	10 (1)	
	B0D4	9mA 50k $\Omega$ Pull-down	10 (1)	
	B0U4	9mA 50k $\Omega$ Pull-up	10 (1)	
	B0W4	9mA 5k $\Omega$ Pull-up	10 (1)	
	B002	12mA	20 (1)	
	B0D2	12mA 50k $\Omega$ Pull-down	20 (1)	
	B0U2	12mA 50k $\Omega$ Pull-up	20 (1)	
	B0W2	12mA 5k $\Omega$ Pull-up	20 (1)	
	B006	18mA	20 (1)	
	B0D6	18mA 50k $\Omega$ Pull-down	20 (1)	
	B0U6	18mA 50k $\Omega$ Pull-up	20 (1)	
	B0W6	18mA 5k $\Omega$ Pull-up	20 (1)	
	B00G	24mA	20 (1)	
	B0DG	24mA 50k $\Omega$ Pull-down	20 (1)	
	B0UG	24mA 50k $\Omega$ Pull-up	20 (1)	
	B0WG	24mA 5k $\Omega$ Pull-up	20 (1)	

Function	Block	Description	Cells (I/O)	Page
Low-noise I/O Buffer	BE0V	3mA	10 (1)	1-86
	BEDV	3mA 50k $\Omega$ Pull-down	10 (1)	
	BEUV	3mA 50k $\Omega$ Pull-up	10 (1)	
	BEWV	3mA 5k $\Omega$ Pull-up	10 (1)	
	BE0D	6mA	10 (1)	
	BEDD	6mA 50k $\Omega$ Pull-down	10 (1)	
	BEUD	6mA 50k $\Omega$ Pull-up	10 (1)	
	BEWD	6mA 5k $\Omega$ Pull-up	10 (1)	
	BE04	9mA	10 (1)	
	BED4	9mA 50k $\Omega$ Pull-down	10 (1)	
	BEU4	9mA 50k $\Omega$ Pull-up	10 (1)	
	BEW4	9mA 5k $\Omega$ Pull-up	10 (1)	
	BE02	12mA	10 (1)	
	BED2	12mA 50k $\Omega$ Pull-down	10 (1)	
	BEU2	12mA 50k $\Omega$ Pull-up	10 (1)	
	BEW2	12mA 5k $\Omega$ Pull-up	10 (1)	
	BE06	18mA	10 (1)	
	BED6	18mA 50k $\Omega$ Pull-down	10 (1)	
	BEU6	18mA 50k $\Omega$ Pull-up	10 (1)	
	BEW6	18mA 5k $\Omega$ Pull-up	10 (1)	
	BE0G	24mA	10 (1)	
	BEDG	24mA 50k $\Omega$ Pull-down	10 (1)	
	BEUG	24mA 50k $\Omega$ Pull-up	10 (1)	
	BEWG	24mA 5k $\Omega$ Pull-up	10 (1)	

Function	Block	Description	Cells (I/O)	Page
Schmitt I/O Buffer	BSIVW	3mA	13 (1)	1-92
	BSDVW	3mA 50k $\Omega$ Pull-down	13 (1)	
	BSUVW	3mA 50k $\Omega$ Pull-up	13 (1)	
	BSWVW	3mA 5k $\Omega$ Pull-up	13 (1)	
	BSIDW	6mA	13 (1)	
	BSDDW	6mA 50k $\Omega$ Pull-down	13 (1)	
	BSUDW	6mA 50k $\Omega$ Pull-up	13 (1)	
	BSWDW	6mA 5k $\Omega$ Pull-up	13 (1)	
	BSI4W	9mA	13 (1)	
	BSD4W	9mA 50k $\Omega$ Pull-down	13 (1)	
	BSU4W	9mA 50k $\Omega$ Pull-up	13 (1)	
	BSW4W	9mA 5k $\Omega$ Pull-up	13 (1)	
	BSI2W	12mA	23 (1)	
	BSD2W	12mA 50k $\Omega$ Pull-down	23 (1)	
	BSU2W	12mA 50k $\Omega$ Pull-up	23 (1)	
	BSW2W	12mA 5k $\Omega$ Pull-up	23 (1)	
	BSI6W	18mA	23 (1)	
	BSD6W	18mA 50k $\Omega$ Pull-down	23 (1)	
	BSU6W	18mA 50k $\Omega$ Pull-up	23 (1)	
	BSW6W	18mA 5k $\Omega$ Pull-up	23 (1)	
	BSIGW	24mA	23 (1)	
	BSDGW	24mA 50k $\Omega$ Pull-down	23 (1)	
	BSUGW	24mA 50k $\Omega$ Pull-up	23 (1)	
	BSWGW	24mA 5k $\Omega$ Pull-up	23 (1)	

Function	Block	Description	Cells (I/O)	Page
Low-noise Schmitt I/O Buffer	BFIVW	3mA	13 (1)	1-98
	BFDVW	3mA 50kΩ Pull-down	13 (1)	
	BFUVW	3mA 50kΩ Pull-up	13 (1)	
	BFVWV	3mA 5kΩ Pull-up	13 (1)	
	BFIDW	6mA	13 (1)	
	BFDDW	6mA 50kΩ Pull-down	13 (1)	
	BFUDW	6mA 50kΩ Pull-up	13 (1)	
	BFWDW	6mA 5kΩ Pull-up	13 (1)	
	BFI4W	9mA	13 (1)	
	BFD4W	9mA 50kΩ Pull-down	13 (1)	
	BFU4W	9mA 50kΩ Pull-up	13 (1)	
	BFW4W	9mA 5kΩ Pull-up	13 (1)	
	BFI2W	12mA	13 (1)	
	BFD2W	12mA 50kΩ Pull-down	13 (1)	
	BFU2W	12mA 50kΩ Pull-up	13 (1)	
	BFW2W	12mA 5kΩ Pull-up	13 (1)	
	BFI6W	18mA	13 (1)	
	BFD6W	18mA 50kΩ Pull-down	13 (1)	
	BFU6W	18mA 50kΩ Pull-up	13 (1)	
	BFW6W	18mA 5kΩ Pull-up	13 (1)	
	BFIGW	24mA	13 (1)	
	BFDGW	24mA 50kΩ Pull-down	13 (1)	
	BFUGW	24mA 50kΩ Pull-up	13 (1)	
BFWGW	24mA 5kΩ Pull-up	13 (1)		
I/O Buffer with EN(AND)	BN2V	3mA	14 (1)	1-104
	BN4V	3mA 50kΩ Pull-down	14 (1)	
	BN2D	6mA	14 (1)	
	BN4D	6mA 50kΩ Pull-down	14 (1)	
	BN24	9mA	14 (1)	
	BN44	9mA 50kΩ Pull-down	14 (1)	
	BN22	12mA	24 (1)	
	BN42	12mA 50kΩ Pull-down	24 (1)	
	BN26	18mA	24 (1)	
	BN46	18mA 50kΩ Pull-down	24 (1)	
	BN2G	24mA	24 (1)	
	BN4G	24mA 50kΩ Pull-down	24 (1)	

Function	Block	Description	Cells (I/O)	Page
I/O Buffer with EN(OR)	BN3V	3mA	11 (1)	1-108
	BN5V	3mA 50k $\Omega$ Pull-down	11 (1)	
	BN3D	6mA	11 (1)	
	BN5D	6mA 50k $\Omega$ Pull-down	11 (1)	
	BN34	9mA	11 (1)	
	BN54	9mA 50k $\Omega$ Pull-down	11 (1)	
	BN32	12mA	21 (1)	
	BN52	12mA 50k $\Omega$ Pull-down	21 (1)	
	BN36	18mA	21 (1)	
	BN56	18mA 50k $\Omega$ Pull-down	21 (1)	
	BN3G	24mA	21 (1)	
	BN5G	24mA 50k $\Omega$ Pull-down	21 (1)	

### 1.3 Oscillator

Function	Block	Description	Cells (I/O)	Page
Oscillator Input Buffer	OSI1	-	0 (1)	1-116
Oscillator Input Buffer for Enable	OSI2	-	0 (1)	1-118
Oscillator Input Buffer for OSO9	OSI4	-	0 (1)	1-120
Oscillator Output Buffer (Internal Feedback Resistor)	OSO1	-	0 (1)	1-122
Oscillator Output Buffer (for Enable Type)	OSO7	-	0 (1)	1-124
Oscillator Output Buffer (External Feedback Resistor)	OSO9	-	0 (1)	1-126

## Chapter 2 Function Block

### 2.1 Level Generator

Function	Block	Description	Cells (I/O)	Page
H, L Level Generator	F091	-	1 (-)	2-4

### 2.2 Inverter, Buffer, CTS Driver, Delay Gate

Function	Block	Description	Cells (I/O)	Page
Inverter	L101	Single Out, Low Power	1 (-)	2-10
	F101	Single Out	1 (-)	
	F102	Single Out, x2-drive	2 (-)	
	F143	Single Out, x3-drive	3 (-)	
	F144	Single Out, x4-drive	4 (-)	
	F145	Single Out, x5-drive	5 (-)	
	F146	Single Out, x6-drive	6 (-)	
	F148	Single Out, x8-drive	12 (-)	
Buffer	L111	Single Out, Low Power	1 (-)	2-12
	F111	Single Out	2 (-)	
	F112	Single Out, x2-drive	3 (-)	
	F153	Single Out, x3-drive	4 (-)	
	F154	Single Out, x4-drive	5 (-)	
	F158	Single Out, x8-drive	11 (-)	
CTS Driver (Inverter Type)	FC42	Single type	80 (-)	2-14
	FC82	Single type, x2-drive	396 (-)	
	FC44	Double type	340 (-)	
	FC84	Double type, x2-drive	1020 (-)	
Delay Gate	F131	-	6 (-)	2-16
	F132	-	10 (-)	



## 2.3 OR(NOR)

Function	Block	Description	Cells (I/O)	Page
2-Input NOR	L202	Low Power	1 (-)	2-22
	F202	-	2 (-)	
	F222	x2-drive	4 (-)	
	F282	x4-drive	6 (-)	
3-Input NOR	F203	-	3 (-)	2-24
	F223	x2-drive	6 (-)	
4-Input NOR	F204	-	4 (-)	2-26
5-Input NOR	L205	Low Power	4 (-)	2-28
	F205	-	5 (-)	
	F225	x2-drive	6 (-)	
6-Input NOR	F206	-	5 (-)	2-30
	F226	x2-drive	6 (-)	
8-Input NOR	L208	Low Power	7 (-)	2-32
	F208	-	7 (-)	
	F228	x2-drive	8 (-)	
2-Input OR	L212	Low Power	2 (-)	2-34
	F212	-	2 (-)	
	F232	x2-drive	3 (-)	
	F252	x4-drive	6 (-)	
3-Input OR	L213	Low Power	2 (-)	2-36
	F213	-	3 (-)	
	F233	x2-drive	4 (-)	
4-Input OR	L214	Low Power	3 (-)	2-38
	F214	-	3 (-)	
	F234	x2-drive	4 (-)	
5-Input OR	L215	Low Power	4 (-)	2-40
	F215	-	5 (-)	
	F235	x2-drive	7 (-)	
6-Input OR	L216	Low Power	4 (-)	2-42
	F216	-	5 (-)	
	F236	x2-drive	7 (-)	
8-Input OR	L218	Low Power	6 (-)	2-44
	F218	-	8 (-)	
	F238	x2-drive	9 (-)	

## 2.4 AND(NAND)

Function	Block	Description	Cells (I/O)	Page
2-Input NAND	L302	Low Power	1 (-)	2-50
	F302	-	2 (-)	
	F322	x2-drive	4 (-)	
	F382	x4-drive	6 (-)	
3-Input NAND	L303	Low Power	2 (-)	2-52
	F303	-	3 (-)	
	F323	x2-drive	6 (-)	
4-Input NAND	L304	Low Power	2 (-)	2-54
	F304	-	4 (-)	
	F324	x2-drive	8 (-)	
5-Input NAND	F305	-	5 (-)	2-56
	F325	x2-drive	6 (-)	
6-Input NAND	F306	-	5 (-)	2-58
	F326	x2-drive	6 (-)	
8-Input NAND	F308	-	6 (-)	2-60
	F328	x2-drive	7 (-)	
2-Input AND	L312	Low Power	2 (-)	2-62
	F312	-	2 (-)	
	F332	x2-drive	3 (-)	
	F352	x4-drive	6 (-)	
3-Input AND	L313	Low Power	2 (-)	2-64
	F313	-	3 (-)	
	F333	x2-drive	4 (-)	
4-Input AND	L314	Low Power	3 (-)	2-66
	F314	-	3 (-)	
	F334	x2-drive	4 (-)	
5-Input AND	L315	Low Power	4 (-)	2-68
	F315	-	5 (-)	
	F335	x2-drive	7 (-)	
6-Input AND	L316	Low Power	4 (-)	2-70
	F316	-	5 (-)	
	F336	x2-drive	7 (-)	
8-Input AND	L318	Low Power	5 (-)	2-72
	F318	-	6 (-)	
	F338	x2-drive	8 (-)	

## 2.5 AND-NOR

Function	Block	Description	Cells (I/O)	Page
1-2-Input AND-NOR	L421	Low Power	2 (-)	2-78
	F421	-	3 (-)	
1-1-2-Input AND-NOR	F422	-	4 (-)	2-80
1-3-Input AND-NOR	L423	Low Power	2 (-)	2-82
	F423	-	4 (-)	
2-2-Input AND-NOR	L424	Low Power	2 (-)	2-84
	F424	-	4 (-)	
2-3-Input AND-NOR	F427	-	5 (-)	2-86
1-2-2-Input AND-NOR	F428	-	5 (-)	2-88
2-2-2-Input AND-NOR	L429	Low Power	6 (-)	2-90
	F429	-	6 (-)	
1-4-Input AND-NOR	F440	-	5 (-)	2-92
1-5-Input AND-NOR	L441	Low Power	5 (-)	2-94
	F441	-	7 (-)	
4-4-4-Input AND-NOR	L444	Low Power	8 (-)	2-96
	F444	-	8 (-)	
1-1-1-2-Input AND-NOR	L446	Low Power	4 (-)	2-98
	F446	-	5 (-)	
1-1-1-3-Input AND-NOR	L447	Low Power	5 (-)	2-100
	F447	-	5 (-)	
1-1-2-2-Input AND-NOR	L448	Low Power	5 (-)	2-102
	F448	-	5 (-)	
3-3-3-3-Input AND-NOR	F449	-	8 (-)	2-104
3-3-3-Input AND-NOR	L460	Low Power	6 (-)	2-106
	F460	-	7 (-)	
1-1-4-Input AND-NOR	L464	Low Power	5 (-)	2-108
	F464	-	5 (-)	
1-1-1-1-2-Input AND-NOR	F465	-	5 (-)	2-110
4-4-4-4-Input AND-NOR	F466	-	10 (-)	2-112

## 2.6 OR-NAND

Function	Block	Description	Cells (I/O)	Page
1-4-Input OR-NAND	L430	Low Power	4 (-)	2-118
	F430	-	5 (-)	
1-2-Input OR-NAND	L431	Low Power	2 (-)	2-120
	F431	-	3 (-)	
1-1-2-Input OR-NAND	L432	Low Power	2 (-)	2-122
	F432	-	4 (-)	
1-3-Input OR-NAND	F433	-	4 (-)	2-124
2-2-Input OR-NAND	F434	-	4 (-)	2-126
1-5-Input OR-NAND	L439	Low Power	5 (-)	2-128
	F439	-	6 (-)	
2-4-Input OR-NAND	L450	Low Power	5 (-)	2-130
	F450	-	6 (-)	
4-4-Input OR-NAND	L451	Low Power	7 (-)	2-132
	F451	-	8 (-)	
1-1-3-Input OR-NAND	L452	Low Power	4 (-)	2-134
	F452	-	5 (-)	
1-1-4-Input OR-NAND	L453	Low Power	5 (-)	2-136
	F453	-	6 (-)	
4-4-4-Input OR-NAND	F457	-	10 (-)	2-138
1-1-1-2-Input OR-NAND	F458	-	5 (-)	2-140
1-1-1-3-Input OR-NAND	L459	Low Power	5 (-)	2-142
	F459	-	5 (-)	
1-1-1-1-2-Input OR-NAND	F490	-	5 (-)	2-144
1-2-3-Input OR-NAND	L491	Low Power	5 (-)	2-146
	F491	-	5 (-)	
3-3-3-Input OR-NAND	L493	Low Power	6 (-)	2-148
	F493	-	7 (-)	
3-3-3-3-Input OR-NAND	F496	-	8 (-)	2-150
4-4-4-4-Input OR-NAND	F498	-	14 (-)	2-152

## 2.7 Exclusive OR, Exclusive NOR

Function	Block	Description	Cells (I/O)	Page
2-Input Exclusive OR	L511	Low Power	3 (-)	2-158
	F511	-	4 (-)	
3-Input Exclusive OR	L516	Low Power	6 (-)	2-160
	F516	-	7 (-)	
2-Input Exclusive NOR	L512	Low Power	3 (-)	2-162
	F512	-	4 (-)	
3-Input Exclusive NOR	L517	Low Power	7 (-)	2-164
	F517	-	7 (-)	

## 2.8 Adder, 3-State Buffer, Decoder, Multiplexer, Generator

Function	Block	Description	Cells (I/O)	Page
1-Bit Full Adder	F521	-	9 (-)	2-170
4-Bit Full Adder	F523	-	32 (-)	2-172
4-Bit Look Ahead Carry Generator	F526	-	34 (-)	2-176
4-Bit Carry Look Ahead Adder	F527	-	69 (-)	2-178
3-State Buffer	L531	with EN, Low Power	4 (-)	2-182
	F531	with EN	5 (-)	
	F533	with EN, x2-drive	7 (-)	
	F53F	with EN, x4-drive	11 (-)	
	L532	with ENB, Low Power	4 (-)	
	F532	with ENB	5 (-)	
	F534	with ENB, x2-drive	7 (-)	
	F53G	with ENB, x4-drive	11 (-)	
	F541	Inverter with EN	6 (-)	
	F543	Inverter with EN, x2-drive	8 (-)	
	F54F	Inverter with EN, x4-drive	12 (-)	
	F542	Inverter with ENB	6 (-)	
	F544	Inverter with ENB, x2-drive	8 (-)	
	F54G	Inverter with ENB, x4-drive	12 (-)	
2 to 4 Decoder	L560	Positive Out, Low Power	6 (-)	2-186
	F560	Positive Out	10 (-)	
	L561	Negative Out, Low Power	6 (-)	
	F561	Negative Out	10 (-)	
2 to 1 Multiplexer (Positive Out)	L565	Low Power	3 (-)	2-190
	F565	-	4 (-)	
	L571	with ENB, Low Power	4 (-)	
	F571	with ENB	6 (-)	
4 to 1 Multiplexer (Positive Out)	F564	-	8 (-)	2-192
	F570	with ENB	10 (-)	
8 to 1 Multiplexer (Positive Out)	F563	-	18 (-)	2-194
	F569	with ENB	18 (-)	
Quad 2 to 1 Multiplexer (Negative Out)	L572	with ENB, Low Power	15 (-)	2-198
	F572	with ENB	17 (-)	
8-Bit Odd Parity Generator	F581	-	19 (-)	2-202
8-Bit Even Parity Generator	F582	-	19 (-)	2-204

## 2.9 RS-Latch, RS-F/F

Function	Block	Description	Cells (I/O)	Page
RS-Latch	F595	-	5 (-)	2-210
RS-F/F with R, S	F596	-	11 (-)	2-212

## 2.10 D-Latch

Function	Block	Description	Cells (I/O)	Page
D-Latch	F601	-	6 (-)	2-218
	L601	Q Out, Low Power	4 (-)	
	F601NQ	Q Out	5 (-)	
	F601NB	QB Out	5 (-)	
D-Latch, High Speed	F6R1	-	6 (-)	2-220
D-Latch with R	F602	-	6 (-)	2-222
	L602	Q Out, Low Power	5 (-)	
	F602NQ	Q Out	6 (-)	
	F602NB	QB Out	5 (-)	
D-Latch with R, High Speed	F6R2	-	7 (-)	2-224
D-Latch with RB	F603	-	7 (-)	2-226
	L603	Q Out, Low Power	5 (-)	
	F603NQ	Q Out	5 (-)	
	F603NB	QB Out	6 (-)	
D-Latch with RB, High Speed	F6R5	-	6 (-)	2-228
D-Latch with SB	F60K	-	7 (-)	2-230
	F60KNQ	Q Out	6 (-)	
	F60KNB	QB Out	5 (-)	
D-Latch with RB, SB	F60J	-	7 (-)	2-232
	F60JNQ	Q Out	6 (-)	
	F60JNB	QB Out	6 (-)	
D-Latch (GB)	F604	-	6 (-)	2-236
	L604	Q Out, Low Power	4 (-)	
	F604NQ	Q Out	5 (-)	
	F604NB	QB Out	5 (-)	
D-Latch (GB), High Speed	F6R8	-	6 (-)	2-238
D-Latch (GB) with RB	F605	-	7 (-)	2-240
	L605	Q Out, Low Power	5 (-)	
	F605NQ	Q Out	5 (-)	
	F605NB	QB Out	6 (-)	
D-Latch (GB) with RB, High Speed	F6R9	-	6 (-)	2-242

## 2.11 D-F/F

Function	Block	Description	Cells (I/O)	Page
D-F/F	F641	-	8 (-)	2-248
	L641	Q Out, Low Power	6 (-)	
	F641NQ	Q Out	7 (-)	
	F641NB	QB Out	7 (-)	
D-F/F with R	F642	-	9 (-)	2-250
	F642NQ	Q Out	8 (-)	
	F642NB	QB Out	8 (-)	
D-F/F with S	F643	-	9 (-)	2-252
	F643NQ	Q Out	8 (-)	
	F643NB	QB Out	8 (-)	
D-F/F with R, S	F644	-	10 (-)	2-254
	L644	Q Out, Low Power	8 (-)	
	F644NQ	Q Out	9 (-)	
	F644NB	QB Out	9 (-)	
D-F/F with RB	F615	-	9 (-)	2-256
	L645	Q Out, Low Power	7 (-)	
	F615NQ	Q Out	8 (-)	
	F615NB	QB Out	8 (-)	
D-F/F with SB	F616	-	9 (-)	2-258
	F616NQ	Q Out	8 (-)	
	F616NB	QB Out	8 (-)	
D-F/F with RB, SB	F647	-	10 (-)	2-260
	L647	Q Out, Low Power	8 (-)	
	F647NQ	Q Out	9 (-)	
	F647NB	QB Out	9 (-)	
D-F/F (CB)	F661	-	8 (-)	2-262
	L661	Q Out, Low Power	6 (-)	
	F661NQ	Q Out	7 (-)	
	F661NB	QB Out	7 (-)	
D-F/F (CB) with RB	F665	-	9 (-)	2-264
	F665NQ	Q Out	8 (-)	
	F665NB	QB Out	8 (-)	
D-F/F (CB) with SB	F666	-	9 (-)	2-266
	F666NQ	Q Out	8 (-)	
	F666NB	QB Out	8 (-)	
D-F/F (CB) with RB, SB	F667	-	10 (-)	2-268
	L667	Q Out, Low Power	8 (-)	
	F667NQ	Q Out	9 (-)	
	F667NB	QB Out	9 (-)	
D-F/F with 2 to 1 Selector	F641S	-	10 (-)	2-270
	F641SQ	Q Out	9 (-)	
	F641SB	QB Out	9 (-)	

Function	Block	Description	Cells (I/O)	Page
D-F/F with R, 2 to 1 Selector	F642S	-	11 (-)	2-272
	F642SQ	Q Out	10 (-)	
	F642SB	QB Out	10 (-)	
D-F/F with S, 2 to 1 Selector	F643S	-	11 (-)	2-274
	F643SQ	Q Out	10 (-)	
	F643SB	QB Out	10 (-)	
D-F/F with R, S, 2 to 1 Selector	F644S	-	12 (-)	2-276
	F644SQ	Q Out	11 (-)	
	F644SB	QB Out	11 (-)	
D-F/F with RB, 2 to 1 Selector	F615S	-	11 (-)	2-278
	F615SQ	Q Out	10 (-)	
	F615SB	QB Out	10 (-)	
D-F/F with SB, 2 to 1 Selector	F616S	-	11 (-)	2-280
	F616SQ	Q Out	10 (-)	
	F616SB	QB Out	10 (-)	
D-F/F with RB, SB, 2 to 1 Selector	F647S	-	12 (-)	2-282
	F647SQ	Q Out	11 (-)	
	F647SB	QB Out	11 (-)	
D-F/F (CB) with 2 to 1 Selector	F661S	-	10 (-)	2-284
	F661SQ	Q Out	9 (-)	
	F661SB	QB Out	9 (-)	
D-F/F (CB) with RB, 2 to 1 Selector	F665S	-	11 (-)	2-286
	F665SQ	Q Out	10 (-)	
	F665SB	QB Out	10 (-)	
D-F/F (CB) with SB, 2 to 1 Selector	F666S	-	11 (-)	2-288
	F666SQ	Q Out	10 (-)	
	F666SB	QB Out	10 (-)	
D-F/F (CB) with RB, SB, 2 to 1 Selector	F667S	-	12 (-)	2-290
	F667SQ	Q Out	11 (-)	
	F667SB	QB Out	11 (-)	
D-F/F with Hold	F641H	-	10 (-)	2-292
	F641HQ	Q Out	9 (-)	
	F641HB	QB Out	9 (-)	
D-F/F with RB, Hold	F615H	-	11 (-)	2-294
	F615HQ	Q Out	10 (-)	
	F615HB	QB Out	10 (-)	
D-F/F with SB, Hold	F616H	-	11 (-)	2-296
	F616HQ	Q Out	10 (-)	
	F616HB	QB Out	10 (-)	
D-F/F with RB, SB, Hold	F647H	-	12 (-)	2-298
	F647HQ	Q Out	11 (-)	
	F647HB	QB Out	11 (-)	
D-F/F (CB) with 2 to 1 Selector(2 CTRL), RB	F673	-	11 (-)	2-300
D-F/F (CB) with Hold, 2 to 1 Selector(2 CTRL), RB	F674	-	12 (-)	2-302



## 2.12 T-F/F, JK-F/F

Function	Block	Description	Cells (I/O)	Page
T-F/F with R, S	F744	-	9 (-)	2-308
	L744	Q Out, Low Power	7 (-)	
	F744NQ	Q Out	8 (-)	
T-F/F with RB	F745	-	8 (-)	2-310
	F745NQ	Q Out	7 (-)	
T-F/F with RB, SB	F747	-	9 (-)	2-312
	L747	Q Out, Low Power	7 (-)	
	F747NQ	Q Out	8 (-)	
T-F/F with Data-Hold R, S	F791	-	12 (-)	2-314
T-F/F (TB) with RB	F765	-	8 (-)	2-316
	F765NQ	Q Out	7 (-)	
T-F/F (TB) with RB, SB	F767	-	9 (-)	2-318
	L767	Q Out, Low Power	7 (-)	
	F767NQ	Q Out	8 (-)	
T-F/F (TB) with Data-Hold RB, SB	F792	-	12 (-)	2-320
JK-F/F	F771	-	10 (-)	2-322
	F771NQ	Q Out	9 (-)	
	F771NB	QB Out	9 (-)	
JK-F/F, High Speed	F7D1	-	10 (-)	2-324
JK-F/F with R, S	F774	-	12 (-)	2-326
	F774NQ	Q Out	11 (-)	
	F774NB	QB Out	11 (-)	
JK-F/F with RB	F775	-	11 (-)	2-328
	F775NQ	Q Out	10 (-)	
	F775NB	QB Out	10 (-)	
JK-F/F with SB	F776	-	11 (-)	2-330
	F776NQ	Q Out	10 (-)	
	F776NB	QB Out	10 (-)	
JK-F/F with RB, SB	F777	-	12 (-)	2-332
	F777NQ	Q Out	11 (-)	
	F777NB	QB Out	11 (-)	
JK-F/F (CB)	F781	-	10 (-)	2-334
	F781NQ	Q Out	9 (-)	
	F781NB	QB Out	9 (-)	
JK-F/F (CB), High Speed	F7E1	-	10 (-)	2-336
JK-F/F (CB) with RB, SB	F787	-	12 (-)	2-338
	F787NQ	Q Out	11 (-)	
	F787NB	QB Out	11 (-)	

## Chapter 3 Scan Path Block

### 3.1 Standard Type

Function	Block	Description	Cells (I/O)	Page
Scan D-F/F with R, S, 2 to 1 Selector	S000	-	12 (-)	3-4
Scan D-F/F with 2 to 1 Selector	S002	-	10 (-)	3-6
Scan D-F/F with 2 to 1 Selector, High Speed	S003	-	11 (-)	3-8
Scan D-F/F with R, S, Hold, 2 to 1 Selector	S050	-	16 (-)	3-10
Scan D-F/F with Hold, 2 to 1 Selector	S052	-	14 (-)	3-12
Scan JK-F/F with R, S, D-F/F Function	S100	-	14 (-)	3-14
Scan JK-F/F with D-F/F Function	S102	-	12 (-)	3-16
Scan JK-F/F with R, S, Hold, D-F/F Function	S150	-	18 (-)	3-18
Scan JK-F/F with Hold, D-F/F Function	S152	-	16 (-)	3-20
Scan D-Latch with R, D-F/F Function	S201	-	13 (-)	3-22
Scan D-Latch with D-F/F Function	S202	-	12 (-)	3-24
Scan D-Latch with D-F/F Function, High Speed	S204	-	12 (-)	3-26
Scan D-Latch with R, Special Function	S301	-	8 (-)	3-28
Scan D-Latch with Special Function	S302	-	7 (-)	3-30
Scan D-Latch with Special Function, High Speed	S303	-	7 (-)	3-32

### 3.2 NEC Scan

Function	Block	Description	Cells (I/O)	Page
NEC Scan D-Latch	SE601	-	13 (-)	3-38
NEC Scan D-Latch with R	SE602	-	14 (-)	3-40
NEC Scan D-Latch with RB	SE603	-	14 (-)	3-42
NEC Scan D-Latch(GB)	SE604	-	13 (-)	3-44
NEC Scan D-Latch(GB) with RB	SE605	-	14 (-)	3-46
NEC Scan D-F/F	SE611	-	11 (-)	3-48
NEC Scan D-F/F with R, S	SE614	-	13 (-)	3-50
NEC Scan D-F/F with RB	SE615	-	12 (-)	3-52
NEC Scan D-F/F with SB	SE616	-	12 (-)	3-54
NEC Scan D-F/F with RB, SB	SE617	-	13 (-)	3-56
NEC Scan D-F/F (CB)	SE631	-	11 (-)	3-58
NEC Scan D-F/F (CB) with RB, SB	SE637	-	13 (-)	3-60

### 3.3 Scan Controller

Function	Block	Description	Cells (I/O)	Page
Clock Distributor	SCD1	-	8 (-)	3-66
Clock Distributor with Test (Positive Clock)	SCDC	-	2 (-)	3-68
Clock Distributor with Test (Negative Clock)	SCDD	-	2 (-)	3-70
I/F Control (AMC) with EN	SFEH	-	3 (-)	3-72
I/F Control (AMC) with ENB	SFEL	-	2 (-)	3-74
I/F Control (SMC) with EN	SOEH	-	3 (-)	3-76
I/F Control (SMC) with ENB	SOEL	-	2 (-)	3-78
Mega Macro Skip	SMS1	-	4 (-)	3-80
Set/Reset Control	SRH1	-	2 (-)	3-82
Set-B/Reset-B Control	SRL1	-	2 (-)	3-84
Loop Cut	SRPD	-	12 (-)	3-86
Clock Generator	SCKG	-	16 (-)	3-88
Common Input	SCI1	-	2 (-)	3-90
Common Output	SCO1	-	4 (-)	3-92
GND	SGND	-	2 (-)	3-94

## Chapter 4 Boundary Scan Block

### 4.1 TAP Macro

Function	Block	Description	Cells (I/O)	Page
BScan TAP Macro	SBCJ	-	262 (-)	4-4
BScan TAP Macro with NEC Scan	SBCL	-	315 (-)	4-6

### 4.2 Level Generator

Function	Block	Description	Cells (I/O)	Page
BScan Level Generator (CLANP)	SBZ1	-	1 (-)	4-12

### 4.3 Data Register

Function	Block	Description	Cells (I/O)	Page
BScan Data Register for Input	SVRNI2	-	12 (-)	4-18
BScan Data Register for Output	SVRN22	-	24 (-)	4-20
BScan Data Register for 3-state	SVRN32	-	50 (-)	4-22
BScan Data Register for Bid	SVRNB2	-	57 (-)	4-24

### 4.4 D-latch, Selector, Shift Register

Function	Block	Description	Cells (I/O)	Page
BScan D-Latch with SB Q Out, Low Power	L606	-	5 (-)	4-30
BScan Selector	SBD1	-	4 (-)	4-32
BScan Shift Register	SBR1	-	8 (-)	4-34
BScan Data Selector for Output	SVSNA2	-	7 (-)	4-36
BScan Data Selector for Bid	SVSNB2	-	7 (-)	4-38
BScan Data Enable Selector for 3-state	SVSNC2	-	9 (-)	4-40
BScan Data Enable Selector for Bid	SVSNE2	-	9 (-)	4-42

### 4.5 Soft Macro

Function	Block	Description	Cells (I/O)	Page
BScan TAP Controller	SBCK	-	392 (-)	4-48
BScan Instruction Register (Internal Circuit)	SBM4	-	46 (-)	4-50
BScan Instruction Register	SBM5	-	140 (-)	4-52
BScan Instruction Decoder	SBM6	-	24 (-)	4-54
BScan Instruction Decoder with NEC Scan	SBMC	-	37 (-)	4-56
BScan Bypass Register	SBS3	-	26 (-)	4-58

# **Chapter 1**

## **Interface Block**

## 1.1 CMOS Level

[MEMO]

### Chapter 1 Interface Block

Function	Input Buffer					3.3 V	
Block type							
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
Normal	FI01	FID1	FIU1	FIW1	1	3	
Schmitt	FIS1W	FDS1W	FUS1W	FWS1W	1	6	
Clock							

Logic Diagram for "Normal"	Truth Table																			
	<table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>	A	Y	1	1	0	0													
A	Y																			
1	1																			
0	0																			
Logic Diagram for "Schmitt"	Block type																			
	<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FI01 to FIW1</td> <td>A</td> <td>-</td> <td>Y</td> <td>33</td> </tr> <tr> <td>FIS1W to FWS1W</td> <td>A</td> <td>-</td> <td>Y</td> <td>24</td> </tr> </tbody> </table>	Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FI01 to FIW1	A	-	Y	33	FIS1W to FWS1W	A	-	Y	24
Block type	Input		Output																	
	Symbol	Fan-In	Symbol	Fan-Out																
FI01 to FIW1	A	-	Y	33																
FIS1W to FWS1W	A	-	Y	24																
Logic Diagram for "Clock"																				

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FI01	A → Y	(HH)	0.188	0.308	0.601	0.010	0.014	0.021			
		(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
FID1	A → Y	(HH)	0.188	0.308	0.601	0.010	0.014	0.021			
		(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
FIU1	A → Y	(HH)	0.188	0.308	0.601	0.010	0.014	0.021			
		(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
FIW1	A → Y	(HH)	0.188	0.308	0.601	0.010	0.014	0.021			
		(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
FIS1W	A → Y	(HH)	0.780	1.214	2.365	0.011	0.017	0.025			
		(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
FDS1W	A → Y	(HH)	0.780	1.214	2.365	0.011	0.017	0.025			
		(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
FUS1W	A → Y	(HH)	0.780	1.214	2.365	0.011	0.017	0.025			
		(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
FWS1W	A → Y	(HH)	0.780	1.214	2.365	0.011	0.017	0.025			
		(LL)	1.187	1.883	3.417	0.010	0.015	0.022			

### Chapter 1 Interface Block

Function	Input Buffer with failsafe					3.3 V	
Block type							
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
Normal	FIA1	FDA1			1	3	
Schmitt	FIE1W	FDE1W			1	6	
Clock							

Logic Diagram for "Normal"	Truth Table																			
	<table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>	A	Y	1	1	0	0													
A	Y																			
1	1																			
0	0																			
Logic Diagram for "Schmitt"	Block type																			
	<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FIA1 to FDA1</td> <td>A</td> <td>-</td> <td>Y</td> <td>33</td> </tr> <tr> <td>FIE1W to FDE1W</td> <td>A</td> <td>-</td> <td>Y</td> <td>24</td> </tr> </tbody> </table>	Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FIA1 to FDA1	A	-	Y	33	FIE1W to FDE1W	A	-	Y	24
Block type	Input		Output																	
	Symbol	Fan-In	Symbol	Fan-Out																
FIA1 to FDA1	A	-	Y	33																
FIE1W to FDE1W	A	-	Y	24																
Logic Diagram for "Clock"																				

### Chapter 1 Interface Block

Block type	Switching speed									
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.
FIA1	A → Y	(HH) (LL)	0.188 0.145	0.308 0.239	0.601 0.444	0.010 0.011	0.014 0.014	0.021 0.021		
FDA1	A → Y	(HH) (LL)	0.188 0.145	0.308 0.239	0.601 0.444	0.010 0.011	0.014 0.014	0.021 0.021		
FIE1W	A → Y	(HH) (LL)	0.780 1.187	1.213 1.883	2.369 3.417	0.011 0.010	0.017 0.015	0.025 0.022		
FDE1W	A → Y	(HH) (LL)	0.780 1.187	1.213 1.883	2.369 3.417	0.011 0.010	0.017 0.015	0.025 0.022		



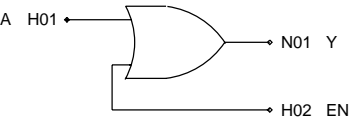
Chapter 1 Interface Block

Function	Input Buffer with EN(AND)					3.3 V																				
Block type																										
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells																				
Normal	FN11	FN21			1	6																				
Schmitt																										
Clock																										
Logic Diagram for "Normal"				Truth Table																						
				<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	0	1	0	0	1	1	1				
A	EN	Y																								
0	0	0																								
0	1	0																								
1	0	0																								
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Logic Diagram for "Schmitt"				<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FN11 to FN21</td> <td>A</td> <td>-</td> <td>Y</td> <td>34</td> </tr> <tr> <td></td> <td>EN</td> <td>3.0</td> <td></td> <td></td> </tr> </tbody> </table>				Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FN11 to FN21	A	-	Y	34		EN	3.0		
Block type	Input		Output																							
	Symbol	Fan-In	Symbol	Fan-Out																						
FN11 to FN21	A	-	Y	34																						
	EN	3.0																								
Logic Diagram for "Clock"																										

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FN11	A → Y	(HH)	0.109	0.219	0.462	0.010	0.014	0.021			
		(LL)	0.253	0.371	0.715	0.011	0.015	0.021			
	EN → Y	(HH)	0.158	0.244	0.510	0.010	0.014	0.021			
		(LL)	0.342	0.488	0.939	0.011	0.015	0.021			
FN21	A → Y	(HH)	0.109	0.219	0.462	0.010	0.014	0.021			
		(LL)	0.253	0.371	0.715	0.011	0.015	0.021			
	EN → Y	(HH)	0.158	0.244	0.510	0.010	0.014	0.021			
		(LL)	0.342	0.488	0.939	0.011	0.015	0.021			

### Chapter 1 Interface Block

Function	Input Buffer with EN(OR)					3.3 V																				
Block type																										
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells																				
Normal	FN13	FN23			1	4																				
Schmitt																										
Clock																										
Logic Diagram for "Normal" 				Truth Table <table border="1" data-bbox="616 470 761 614"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	1	1	0	1	1	1	1				
A	EN	Y																								
0	0	0																								
0	1	1																								
1	0	1																								
1	1	1																								
Logic Diagram for "Schmitt"				<table border="1" data-bbox="582 702 1008 813"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FN13 to FN23</td> <td>A</td> <td>-</td> <td>Y</td> <td>34</td> </tr> <tr> <td></td> <td>EN</td> <td>3.0</td> <td></td> <td></td> </tr> </tbody> </table>				Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FN13 to FN23	A	-	Y	34		EN	3.0		
Block type	Input		Output																							
	Symbol	Fan-In	Symbol	Fan-Out																						
FN13 to FN23	A	-	Y	34																						
	EN	3.0																								
Logic Diagram for "Clock"																										

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FN13	A → Y	(HH)	0.130	0.233	0.450	0.010	0.014	0.021			
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023			
	EN → Y	(HH)	0.138	0.225	0.411	0.010	0.014	0.021			
		(LL)	0.309	0.534	1.127	0.011	0.015	0.023			
FN23	A → Y	(HH)	0.130	0.233	0.450	0.010	0.014	0.021			
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023			
	EN → Y	(HH)	0.138	0.225	0.411	0.010	0.014	0.021			
		(LL)	0.309	0.534	1.127	0.011	0.015	0.023			

Chapter 1 Interface Block

Function	Output Buffer						CMOS 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	FO09				1	4	
6mA	FO04				1	4	
9mA	FO01				1	4	
12mA	FO02				1	12	
18mA	FO03				1	12	
24mA	FO06				1	12	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
<p>A H01 <math>\rightarrow</math> <math>\triangle</math> <math>\rightarrow</math> N01 Y</p>	FO09	A	6.1	Y	-
	FO04	A	6.1	Y	-
	FO01	A	6.1	Y	-
	FO02	A	18.4	Y	-
	FO03	A	18.4	Y	-
	FO06	A	18.4	Y	-

Truth Table	
A	Y
1	1
0	0

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	$\rightarrow$	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
FO09	A	$\rightarrow$	Y	(HH)	0.628	0.992	2.011				0.055	0.078	0.113
				(LL)	0.785	1.363	2.737				0.090	0.131	0.193
FO04	A	$\rightarrow$	Y	(HH)	0.620	1.001	2.053				0.037	0.052	0.076
				(LL)	0.644	1.115	2.214				0.045	0.066	0.097
FO01	A	$\rightarrow$	Y	(HH)	0.660	1.111	2.334				0.023	0.032	0.048
				(LL)	0.688	1.196	2.356				0.030	0.045	0.066
FO02	A	$\rightarrow$	Y	(HH)	0.466	0.785	1.646				0.019	0.027	0.039
				(LL)	0.427	0.784	1.634				0.023	0.033	0.049
FO03	A	$\rightarrow$	Y	(HH)	0.541	0.936	1.987				0.013	0.019	0.030
				(LL)	0.486	0.912	1.925				0.016	0.023	0.034
FO06	A	$\rightarrow$	Y	(HH)	0.612	1.074	2.300				0.011	0.016	0.026
				(LL)	0.560	1.072	2.277				0.012	0.018	0.027

Chapter 1 Interface Block

Function	Low-noise Output Buffer						CMOS 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	FE09				1	5	
6mA	FE04				1	5	
9mA	FE01				1	5	
12mA	FE02				1	5	
18mA	FE03				1	5	
24mA	FE06				1	5	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	FE09	A	9.4	Y	-
	FE04	A	9.4	Y	-
	FE01	A	9.4	Y	-
	FE02	A	9.4	Y	-
	FE03	A	9.4	Y	-
	FE06	A	9.4	Y	-

Truth Table	
A	Y
1	1
0	0

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FE09	A → Y	(HH)	1.277	2.373	5.611				0.057	0.081	0.120
		(LL)	1.556	2.640	5.338				0.091	0.133	0.196
FE04	A → Y	(HH)	1.330	2.554	6.113				0.040	0.058	0.089
		(LL)	1.462	2.543	5.121				0.049	0.071	0.106
FE01	A → Y	(HH)	1.433	2.890	7.130				0.028	0.042	0.070
		(LL)	1.481	2.634	5.334				0.036	0.053	0.079
FE02	A → Y	(HH)	1.489	3.061	7.646				0.026	0.039	0.066
		(LL)	1.521	2.760	5.639				0.030	0.044	0.068
FE03	A → Y	(HH)	1.659	3.562	9.177				0.023	0.036	0.064
		(LL)	1.687	3.110	6.401				0.024	0.037	0.058
FE06	A → Y	(HH)	1.824	4.045	10.666				0.022	0.035	0.064
		(LL)	1.904	3.537	7.289				0.021	0.033	0.053

Chapter 1 Interface Block

Function	3-State Buffer						CMOS 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	B00T	B0DT	B0UT	B0WT	1	7	
6mA	B00E	B0DE	B0UE	B0WE	1	7	
9mA	B008	B0D8	B0U8	B0W8	1	7	
12mA	B007	B0D7	B0U7	B0W7	1	17	
18mA	B009	B0D9	B0U9	B0W9	1	17	
24mA	B00H	B0DH	B0UH	B0WH	1	17	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	B00T to B0WT	A	6.3	Y	-
		EN	1.0		
	B00E to B0WE	A	6.3	Y	-
		EN	1.0		
	B008 to B0W8	A	6.3	Y	-
		EN	1.0		
	B007 to B0W7	A	16.9	Y	-
		EN	1.0		
	B009 to B0W9	A	16.9	Y	-
		EN	1.0		
	B00H to B0WH	A	16.9	Y	-
		EN	1.0		

Truth Table		
A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B00T	A → Y	(HH)		0.839	1.469	3.318				0.056	0.078	0.114
		(LL)		0.963	1.638	3.333				0.089	0.131	0.192
	EN → Y	(HZ)		1.259	1.846	3.271						
		(LZ)		0.469	0.771	1.492				0.056	0.078	0.114
		(ZH)		1.149	2.002	4.411				0.090	0.131	0.193
		(ZL)		1.074	1.852	3.792						
B0DT	A → Y	(HH)		0.839	1.469	3.318				0.056	0.078	0.114
		(LL)		0.963	1.638	3.333				0.089	0.131	0.192
	EN → Y	(HZ)		1.259	1.846	3.271						
		(LZ)		0.469	0.771	1.492				0.056	0.078	0.114
		(ZH)		1.149	2.002	4.411				0.090	0.131	0.193
		(ZL)		1.074	1.852	3.792						
B0UT	A → Y	(HH)		0.839	1.469	3.318				0.056	0.078	0.114
		(LL)		0.963	1.638	3.333				0.089	0.131	0.192
	EN → Y	(HZ)		1.259	1.846	3.271						
		(LZ)		0.469	0.771	1.492				0.056	0.078	0.114
		(ZH)		1.149	2.002	4.411				0.090	0.131	0.193
		(ZL)		1.074	1.852	3.792						
B0WT	A → Y	(HH)		0.839	1.469	3.318				0.056	0.078	0.114
		(LL)		0.963	1.638	3.333				0.089	0.131	0.192
	EN → Y	(HZ)		1.259	1.846	3.271						
		(LZ)		0.469	0.771	1.492				0.056	0.078	0.114
		(ZH)		1.149	2.002	4.411				0.090	0.131	0.193
		(ZL)		1.074	1.852	3.792						
B00E	A → Y	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
	EN → Y	(HZ)		1.602	2.366	4.209						
		(LZ)		0.547	0.906	1.819				0.038	0.053	0.080
		(ZH)		1.164	2.076	4.626				0.045	0.066	0.098
		(ZL)		0.931	1.622	3.317						
B0DE	A → Y	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
	EN → Y	(HZ)		1.602	2.366	4.209						
		(LZ)		0.547	0.906	1.819				0.038	0.053	0.080
		(ZH)		1.164	2.076	4.626				0.045	0.066	0.098
		(ZL)		0.931	1.622	3.317						
B0UE	A → Y	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
	EN → Y	(HZ)		1.602	2.366	4.209						
		(LZ)		0.547	0.906	1.819				0.038	0.053	0.080
		(ZH)		1.164	2.076	4.626				0.045	0.066	0.098
		(ZL)		0.931	1.622	3.317						
B0WE	A → Y	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
	EN → Y	(HZ)		1.602	2.366	4.209						
		(LZ)		0.547	0.906	1.819				0.038	0.053	0.080
		(ZH)		1.164	2.076	4.626				0.045	0.066	0.098
		(ZL)		0.931	1.622	3.317						
B008	A → Y	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005				0.024	0.035	0.056
		(ZH)		1.232	2.276	5.174				0.031	0.045	0.067
		(ZL)		0.913	1.619	3.323						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0D8	A → Y	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
		(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
B0U8	A → Y	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
		(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
B0W8	A → Y	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
		(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
B007	A → Y	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
B0D7	A → Y	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
B0U7	A → Y	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
B0W7	A → Y	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
B009	A → Y	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
B0D9	A → Y	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0U9	A → Y	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
B0W9	A → Y	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
B00H	A → Y	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
B0DH	A → Y	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
B0UH	A → Y	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
B0WH	A → Y	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031

Chapter 1 Interface Block

Function	Low-noise 3-State Buffer						CMOS 3.3 V	
Block type								
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells		
1mA								
2mA								
3mA	BE0T	BEDT	BEUT	BEWT	1	7		
6mA	BE0E	BEDE	BEUE	BEWE	1	7		
9mA	BE08	BED8	BEU8	BEW8	1	7		
12mA	BE07	BED7	BEU7	BEW7	1	7		
18mA	BE09	BED9	BEU9	BEW9	1	7		
24mA	BE0H	BEDH	BEUH	BEWH	1	7		
Logic Diagram		Block type		Input		Output		
		Symbol	Fan-in	Symbol	Fan-out			
		BE0T to BEWT	A	6.1	Y	-		
			EN	4.0				
		BE0E to BEWE	A	6.1	Y	-		
			EN	4.0				
		BE08 to BEW8	A	6.1	Y	-		
	EN	4.0						
BE07 to BEW7	A	6.1	Y	-				
	EN	4.0						
BE09 to BEW9	A	6.1	Y	-				
	EN	4.0						
BE0H to BEWH	A	6.1	Y	-				
	EN	4.0						
Truth Table								
A	EN	Y						
0	1	0						
1	1	1						
X	0	Z						
X:Irrelevant								
Z:High Impedance								

Chapter 1 Interface Block

Block type	Switching speed										
	Path		tLDO (ns)			t1			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BE0T	A → Y	(HH)	1.275	2.384	5.623				0.057	0.081	0.121
		(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y	(HZ)	0.785	1.011	1.593						
		(LZ)	0.745	1.089	2.013				0.057	0.081	0.121
		(ZH)	1.340	2.445	5.805				0.090	0.131	0.194
	(ZL)	1.365	2.279	4.559							
BEDT	A → Y	(HH)	1.275	2.384	5.623				0.057	0.081	0.121
		(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y	(HZ)	0.785	1.011	1.593						
		(LZ)	0.745	1.089	2.013				0.057	0.081	0.121
		(ZH)	1.340	2.445	5.805				0.090	0.131	0.194
	(ZL)	1.365	2.279	4.559							
BEUT	A → Y	(HH)	1.275	2.384	5.623				0.057	0.081	0.121
		(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y	(HZ)	0.785	1.011	1.593						
		(LZ)	0.745	1.089	2.013				0.057	0.081	0.121
		(ZH)	1.340	2.445	5.805				0.090	0.131	0.194
	(ZL)	1.365	2.279	4.559							
BEWT	A → Y	(HH)	1.275	2.384	5.623				0.057	0.081	0.121
		(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y	(HZ)	0.785	1.011	1.593						
		(LZ)	0.745	1.089	2.013				0.057	0.081	0.121
		(ZH)	1.340	2.445	5.805				0.090	0.131	0.194
	(ZL)	1.365	2.279	4.559							
BE0E	A → Y	(HH)	1.326	2.555	6.105				0.040	0.058	0.090
		(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y	(HZ)	1.054	1.423	2.365						
		(LZ)	0.927	1.364	2.581				0.040	0.058	0.090
		(ZH)	1.388	2.613	6.285				0.047	0.068	0.101
	(ZL)	1.265	2.149	4.276							
BEDE	A → Y	(HH)	1.326	2.555	6.105				0.040	0.058	0.090
		(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y	(HZ)	1.054	1.423	2.365						
		(LZ)	0.927	1.364	2.581				0.040	0.058	0.090
		(ZH)	1.388	2.613	6.285				0.047	0.068	0.101
	(ZL)	1.265	2.149	4.276							
BEUE	A → Y	(HH)	1.326	2.555	6.105				0.040	0.058	0.090
		(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y	(HZ)	1.054	1.423	2.365						
		(LZ)	0.927	1.364	2.581				0.040	0.058	0.090
		(ZH)	1.388	2.613	6.285				0.047	0.068	0.101
	(ZL)	1.265	2.149	4.276							
BEWE	A → Y	(HH)	1.326	2.555	6.105				0.040	0.058	0.090
		(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y	(HZ)	1.054	1.423	2.365						
		(LZ)	0.927	1.364	2.581				0.040	0.058	0.090
		(ZH)	1.388	2.613	6.285				0.047	0.068	0.101
	(ZL)	1.265	2.149	4.276							
BE08	A → Y	(HH)	1.429	2.884	7.106				0.028	0.042	0.070
		(LL)	1.311	2.202	4.323				0.032	0.047	0.070
	EN → Y	(HZ)	1.476	2.066	3.447						
		(LZ)	1.086	1.602	3.023				0.028	0.042	0.070
		(ZH)	1.485	2.941	7.290				0.033	0.049	0.073
	(ZL)	1.268	2.209	4.413							

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BED8	A → Y	(HH)		1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
	EN → Y	(HZ)	1.476	2.066	3.447							
		(LZ)	1.086	1.602	3.023							
		(ZH)	1.485	2.941	7.290				0.028	0.042	0.070	
		(ZL)	1.268	2.209	4.413				0.033	0.049	0.073	
BEU8	A → Y	(HH)		1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
	EN → Y	(HZ)	1.476	2.066	3.447							
		(LZ)	1.086	1.602	3.023							
		(ZH)	1.485	2.941	7.290				0.028	0.042	0.070	
		(ZL)	1.268	2.209	4.413				0.033	0.049	0.073	
BEW8	A → Y	(HH)		1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
	EN → Y	(HZ)	1.476	2.066	3.447							
		(LZ)	1.086	1.602	3.023							
		(ZH)	1.485	2.941	7.290				0.028	0.042	0.070	
		(ZL)	1.268	2.209	4.413				0.033	0.049	0.073	
BE07	A → Y	(HH)		1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
	EN → Y	(HZ)	1.692	2.390	3.993							
		(LZ)	1.242	1.836	3.457							
		(ZH)	1.539	3.109	7.803				0.026	0.039	0.067	
		(ZL)	1.288	2.293	4.624				0.027	0.040	0.061	
BED7	A → Y	(HH)		1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
	EN → Y	(HZ)	1.692	2.390	3.993							
		(LZ)	1.242	1.836	3.457							
		(ZH)	1.539	3.109	7.803				0.026	0.039	0.067	
		(ZL)	1.288	2.293	4.624				0.027	0.040	0.061	
BEU7	A → Y	(HH)		1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
	EN → Y	(HZ)	1.692	2.390	3.993							
		(LZ)	1.242	1.836	3.457							
		(ZH)	1.539	3.109	7.803				0.026	0.039	0.067	
		(ZL)	1.288	2.293	4.624				0.027	0.040	0.061	
BEW7	A → Y	(HH)		1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
	EN → Y	(HZ)	1.692	2.390	3.993							
		(LZ)	1.242	1.836	3.457							
		(ZH)	1.539	3.109	7.803				0.026	0.039	0.067	
		(ZL)	1.288	2.293	4.624				0.027	0.040	0.061	
BE09	A → Y	(HH)		1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
	EN → Y	(HZ)	2.348	3.377	5.634							
		(LZ)	1.559	2.307	4.328							
		(ZH)	1.706	3.606	9.328				0.023	0.036	0.064	
		(ZL)	1.353	2.504	5.120				0.022	0.033	0.051	
BED9	A → Y	(HH)		1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
	EN → Y	(HZ)	2.348	3.377	5.634							
		(LZ)	1.559	2.307	4.328							
		(ZH)	1.706	3.606	9.328				0.023	0.036	0.064	
		(ZL)	1.353	2.504	5.120				0.022	0.033	0.051	

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEU9	A → Y	(HH)		1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
	EN → Y	(HZ)	2.348	3.377	5.634							
		(LZ)	1.559	2.307	4.328							
		(ZH)	1.706	3.606	9.328				0.023	0.036	0.064	
		(ZL)	1.353	2.504	5.120				0.022	0.033	0.051	
BEW9	A → Y	(HH)		1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
	EN → Y	(HZ)	2.348	3.377	5.634							
		(LZ)	1.559	2.307	4.328							
		(ZH)	1.706	3.606	9.328				0.023	0.036	0.064	
		(ZL)	1.353	2.504	5.120				0.022	0.033	0.051	
BE0H	A → Y	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
			(LL)	1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y	(HZ)	3.006	4.371	7.283							
		(LZ)	1.877	2.777	5.195							
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064	
		(ZL)	1.424	2.718	5.634				0.020	0.030	0.047	
BEDH	A → Y	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
			(LL)	1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y	(HZ)	3.006	4.371	7.283							
		(LZ)	1.877	2.777	5.195							
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064	
		(ZL)	1.424	2.718	5.634				0.020	0.030	0.047	
BEUH	A → Y	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
			(LL)	1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y	(HZ)	3.006	4.371	7.283							
		(LZ)	1.877	2.777	5.195							
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064	
		(ZL)	1.424	2.718	5.634				0.020	0.030	0.047	
BEWH	A → Y	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
			(LL)	1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y	(HZ)	3.006	4.371	7.283							
		(LZ)	1.877	2.777	5.195							
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064	
		(ZL)	1.424	2.718	5.634				0.020	0.030	0.047	



Chapter 1 Interface Block

Function	N-ch open drain Buffer						CMOS 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA							
6mA							
9mA	EXT1		EXT3	EXW3	1	4	
12mA	EXT9		EXTB	EXWB	1	4	
18mA	EXT5		EXT7	EXW7	1	4	
24mA	EXTD		EXTF	EXWF	1	4	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	EXT1 to EXW3	A	6.1	Y	-
	EXT9 to EXWB	A	6.1	Y	-
	EXT5 to EXW7	A	6.1	Y	-
	EXTD to EXWF	A	6.1	Y	-

Truth Table	
A	Y
1	Z
0	0

Z:High Impedance  
Connect a pull-up resistor to get a high level

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EXT1	A → Y	(LZ) (ZL)	0.377 0.391	0.530 0.712	0.967 1.453				0.030	0.044	0.065
EXT3	A → Y	(LZ) (ZL)	0.377 0.391	0.530 0.712	0.967 1.453				0.030	0.044	0.065
EXW3	A → Y	(LZ) (ZL)	0.377 0.391	0.530 0.712	0.967 1.453				0.030	0.044	0.065
EXT9	A → Y	(LZ) (ZL)	0.438 0.386	0.625 0.719	1.146 1.478				0.023	0.033	0.050
EXTB	A → Y	(LZ) (ZL)	0.438 0.386	0.625 0.719	1.146 1.478				0.023	0.033	0.050
EXWB	A → Y	(LZ) (ZL)	0.438 0.386	0.625 0.719	1.146 1.478				0.023	0.033	0.050
EXT5	A → Y	(LZ) (ZL)	0.562 0.399	0.813 0.768	1.502 1.598				0.016	0.024	0.036
EXT7	A → Y	(LZ) (ZL)	0.562 0.399	0.813 0.768	1.502 1.598				0.016	0.024	0.036
EXW7	A → Y	(LZ) (ZL)	0.562 0.399	0.813 0.768	1.502 1.598				0.016	0.024	0.036
EXTD	A → Y	(LZ) (ZL)	0.684 0.414	1.000 0.817	1.854 1.721				0.013	0.020	0.030
EXTF	A → Y	(LZ) (ZL)	0.684 0.414	1.000 0.817	1.854 1.721				0.013	0.020	0.030
EXWF	A → Y	(LZ) (ZL)	0.684 0.414	1.000 0.817	1.854 1.721				0.013	0.020	0.030

### Chapter 1 Interface Block

Function	N-ch open drain Buffer with failsafe						CMOS 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA							
6mA							
9mA	EXO1				1	4	
12mA	EXO9				1	4	
18mA	EXO5				1	4	
24mA	EXOD				1	4	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		EXO1	A	6.1	Y
EXO9	A	6.1	Y	-	
EXO5	A	6.1	Y	-	
EXOD	A	6.1	Y	-	

Truth Table	
A	Y
1	Z
0	0

Z:High Impedance  
Connect a pull-up resistor to get a high level

### Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EXO1	A	→	Y	(LZ) 0.377 (ZL) 0.391	0.530 0.712	0.967 1.453				0.030	0.044	0.065
EXO9	A	→	Y	(LZ) 0.438 (ZL) 0.386	0.625 0.719	1.146 1.478				0.023	0.033	0.050
EXO5	A	→	Y	(LZ) 0.562 (ZL) 0.399	0.813 0.768	1.502 1.598				0.016	0.024	0.036
EXOD	A	→	Y	(LZ) 0.684 (ZL) 0.414	1.000 0.817	1.854 1.721				0.013	0.020	0.030

### Chapter 1 Interface Block

Function	N-ch open drain I/O Buffer with failsafe					CMOS 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA							
6mA							
9mA	EBA1				1	7	
12mA	EBA9				1	7	
18mA	EBA5				1	7	
24mA	EBAD				1	7	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		EBA1	A	6.1	Y1
EBA9	A	6.1	Y1	33	
EBA5	A	6.1	Y1	33	
EBAD	A	6.1	Y1	33	

Truth Table	
A	Y0
1	Z
0	0

Z:High Impedance  
Connect a pull-up resistor to get a high level

Y0	Y1
0	0
1	1

### Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
EBA1	A	→	Y0	(LZ)	0.377	0.530	0.967						
				(ZL)	0.391	0.712	1.453						
	Y0	→	Y1	(HH)	0.188	0.308	0.601	0.010	0.014	0.021	0.030	0.044	0.065
EBA9	A	→	Y0	(LZ)	0.438	0.625	1.146						
				(ZL)	0.386	0.719	1.478						
	Y0	→	Y1	(HH)	0.188	0.308	0.601	0.010	0.014	0.021	0.023	0.033	0.050
EBA5	A	→	Y0	(LZ)	0.562	0.813	1.502						
				(ZL)	0.399	0.768	1.598						
	Y0	→	Y1	(HH)	0.188	0.308	0.601	0.010	0.014	0.021	0.016	0.024	0.036
EBAD	A	→	Y0	(LZ)	0.684	1.000	1.854						
				(ZL)	0.414	0.817	1.721						
	Y0	→	Y1	(HH)	0.188	0.308	0.601	0.010	0.014	0.021	0.013	0.020	0.030
			(LL)	0.145	0.239	0.444	0.011	0.014	0.021				

### Chapter 1 Interface Block

Function	N-ch open drain Schmitt I/O Buffer with failsafe						CMOS 3.3 V	
Block type								
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells		
1mA								
2mA								
3mA								
6mA								
9mA	EBE1W				1	10		
12mA	EBE9W				1	10		
18mA	EBE5W				1	10		
24mA	EBEDW				1	10		
Logic Diagram		Block type		Input		Output		
		Symbol	Fan-in	Symbol	Fan-out			
		EBE1W	A	6.1	Y1	24		
		EBE9W	A	6.1	Y1	24		
		EBE5W	A	6.1	Y1	24		
		EBEDW	A	6.1	Y1	24		
Truth Table								
A	Y0							
1	Z							
0	0							
Z:High Impedance Connect a pull-up resistor to get a high level								
Y0	Y1							
0	0							
1	1							

### Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
EBE1W	A	→	Y0	(LZ)	0.377	0.530	0.967				0.030	0.044	0.065
				(ZL)	0.391	0.712	1.453						
	Y0	→	Y1	(HH)	0.780	1.213	2.369	0.011	0.017	0.025			
EBE9W	A	→	Y0	(LZ)	0.438	0.625	1.146				0.023	0.033	0.050
				(ZL)	0.386	0.719	1.478						
	Y0	→	Y1	(HH)	0.780	1.213	2.369	0.011	0.017	0.025			
EBE5W	A	→	Y0	(LZ)	0.562	0.813	1.502				0.016	0.024	0.036
				(ZL)	0.399	0.768	1.598						
	Y0	→	Y1	(HH)	0.780	1.213	2.369	0.011	0.017	0.025			
EBEDW	A	→	Y0	(LZ)	0.684	1.000	1.854				0.013	0.020	0.030
				(ZL)	0.414	0.817	1.721						
	Y0	→	Y1	(HH)	0.780	1.213	2.369	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022				

Chapter 1 Interface Block

Function	I/O Buffer					CMOS 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	B00U	B0DU	B0UU	B0WU	1	10	
6mA	B00C	B0DC	B0UC	B0WC	1	10	
9mA	B003	B0D3	B0U3	B0W3	1	10	
12mA	B001	B0D1	B0U1	B0W1	1	20	
18mA	B005	B0D5	B0U5	B0W5	1	20	
24mA	B00F	B0DF	B0UF	B0WF	1	20	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		B00U to B0WU	A	6.3	Y1
B00C to B0WC	A	6.3	Y1	33	
B003 to B0W3	A	6.3	Y1	33	
B001 to B0W1	A	16.9	Y1	33	
B005 to B0W5	A	16.9	Y1	33	
B00F to B0WF	A	16.9	Y1	33	

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X: Irrelevant  
Z: High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
B00U	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
B0DU	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
B0UU	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
B0WU	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
B00C	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.010	0.014	0.021	0.045	0.066
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
B0DC	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.010	0.014	0.021	0.045	0.066
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
B0UC	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.010	0.014	0.021	0.045	0.066
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0WC	A → Y0	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
	EN → Y0	(HZ)		1.602	2.366	4.209						
		(LZ)		0.547	0.906	1.819						
		(ZH)		1.164	2.076	4.626				0.038	0.053	0.080
	Y0 → Y1	(ZL)		0.931	1.622	3.317				0.045	0.066	0.098
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B003	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0D3	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0U3	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0W3	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B001	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0D1	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0U1	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0W1	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B005	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0D5	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0U5	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B0W5	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					
B00F	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
(HH)			0.188	0.308	0.601	0.010	0.014	0.021				
(LL)		0.145	0.239	0.443	0.011	0.014	0.021					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BODF	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
		(HH)		0.188	0.308	0.601	0.010	0.014	0.021			
		(LL)		0.145	0.239	0.443	0.011	0.014	0.021			
	BOUF	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021
(LL)				0.881	1.569	3.211				0.012	0.018	0.027
EN → Y0		(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
Y0 → Y1		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
		(HH)		0.188	0.308	0.601	0.010	0.014	0.021			
		(LL)		0.145	0.239	0.443	0.011	0.014	0.021			
BOWF		A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021
	(LL)			0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
		(HH)		0.188	0.308	0.601	0.010	0.014	0.021			
		(LL)		0.145	0.239	0.443	0.011	0.014	0.021			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise I/O Buffer					CMOS 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BE0U	BEDU	BEUU	BEWU	1	10	
6mA	BE0C	BEDC	BEUC	BEWC	1	10	
9mA	BE03	BED3	BEU3	BEW3	1	10	
12mA	BE01	BED1	BEU1	BEW1	1	10	
18mA	BE05	BED5	BEU5	BEW5	1	10	
24mA	BE0F	BEDF	BEUF	BEWF	1	10	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		BE0U to BEWU	A	6.1	Y1
	EN	4.0			
BE0C to BEWC	A	6.1	Y1	33	
	EN	4.0			
BE03 to BEW3	A	6.1	Y1	33	
	EN	4.0			
BE01 to BEW1	A	6.1	Y1	33	
	EN	4.0			
BE05 to BEW5	A	6.1	Y1	33	
	EN	4.0			
BE0F to BEWF	A	6.1	Y1	33	
	EN	4.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BE0U	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121	
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194	
	EN → Y0	(HZ)	0.785	1.011	1.593								
		(LZ)	0.745	1.089	2.013								
		(ZH)	1.340	2.445	5.805				0.057	0.081	0.121		
	Y0 → Y1	(ZL)	1.365	2.279	4.559				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
BEDU	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121	
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194	
	EN → Y0	(HZ)	0.785	1.011	1.593								
		(LZ)	0.745	1.089	2.013								
		(ZH)	1.340	2.445	5.805				0.057	0.081	0.121		
	Y0 → Y1	(ZL)	1.365	2.279	4.559				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
BEUU	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121	
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194	
	EN → Y0	(HZ)	0.785	1.011	1.593								
		(LZ)	0.745	1.089	2.013								
		(ZH)	1.340	2.445	5.805				0.057	0.081	0.121		
	Y0 → Y1	(ZL)	1.365	2.279	4.559				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
BEWU	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121	
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194	
	EN → Y0	(HZ)	0.785	1.011	1.593								
		(LZ)	0.745	1.089	2.013								
		(ZH)	1.340	2.445	5.805				0.057	0.081	0.121		
	Y0 → Y1	(ZL)	1.365	2.279	4.559				0.010	0.014	0.021	0.090	0.131
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
BE0C	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090	
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101	
	EN → Y0	(HZ)	1.054	1.423	2.365								
		(LZ)	0.927	1.364	2.581								
		(ZH)	1.388	2.613	6.285				0.040	0.058	0.090		
	Y0 → Y1	(ZL)	1.265	2.149	4.276				0.010	0.014	0.021	0.047	0.068
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
BEDC	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090	
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101	
	EN → Y0	(HZ)	1.054	1.423	2.365								
		(LZ)	0.927	1.364	2.581								
		(ZH)	1.388	2.613	6.285				0.040	0.058	0.090		
	Y0 → Y1	(ZL)	1.265	2.149	4.276				0.010	0.014	0.021	0.047	0.068
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						
BEUC	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090	
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101	
	EN → Y0	(HZ)	1.054	1.423	2.365								
		(LZ)	0.927	1.364	2.581								
		(ZH)	1.388	2.613	6.285				0.040	0.058	0.090		
	Y0 → Y1	(ZL)	1.265	2.149	4.276				0.010	0.014	0.021	0.047	0.068
(HH)		0.188	0.308	0.601	0.010	0.014	0.021						
(LL)		0.145	0.239	0.443	0.011	0.014	0.021						



Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEWC	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
		(HZ)	1.054	1.423	2.365							
	EN → Y0	(LZ)	(ZH)	0.927	1.364	2.581				0.040	0.058	0.090
			(ZL)	1.388	2.613	6.285				0.047	0.068	0.101
		(ZH)	1.265	2.149	4.276							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BE03	A → Y0	(HH)	(LL)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
		(HZ)	1.476	2.066	3.447							
	EN → Y0	(LZ)	(ZH)	1.086	1.602	3.023				0.028	0.042	0.070
			(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
		(ZH)	1.268	2.209	4.413							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BED3	A → Y0	(HH)	(LL)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
		(HZ)	1.476	2.066	3.447							
	EN → Y0	(LZ)	(ZH)	1.086	1.602	3.023				0.028	0.042	0.070
			(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
		(ZH)	1.268	2.209	4.413							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BEU3	A → Y0	(HH)	(LL)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
		(HZ)	1.476	2.066	3.447							
	EN → Y0	(LZ)	(ZH)	1.086	1.602	3.023				0.028	0.042	0.070
			(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
		(ZH)	1.268	2.209	4.413							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BEW3	A → Y0	(HH)	(LL)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
		(HZ)	1.476	2.066	3.447							
	EN → Y0	(LZ)	(ZH)	1.086	1.602	3.023				0.028	0.042	0.070
			(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
		(ZH)	1.268	2.209	4.413							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BE01	A → Y0	(HH)	(LL)	1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
		(HZ)	1.692	2.390	3.993							
	EN → Y0	(LZ)	(ZH)	1.242	1.836	3.457				0.026	0.039	0.067
			(ZL)	1.539	3.109	7.803				0.027	0.040	0.061
		(ZH)	1.288	2.293	4.624							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BED1	A → Y0	(HH)	(LL)	1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
		(HZ)	1.692	2.390	3.993							
	EN → Y0	(LZ)	(ZH)	1.242	1.836	3.457				0.026	0.039	0.067
			(ZL)	1.539	3.109	7.803				0.027	0.040	0.061
		(ZH)	1.288	2.293	4.624							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEU1	A → Y0	(HH)	(LL)	1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
		(HZ)	1.692	2.390	3.993							
	EN → Y0	(LZ)	(ZH)	1.242	1.836	3.457				0.026	0.039	0.067
			(ZL)	1.539	3.109	7.803				0.027	0.040	0.061
		(ZH)	1.288	2.293	4.624							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BEW1	A → Y0	(HH)	(LL)	1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
		(HZ)	1.692	2.390	3.993							
	EN → Y0	(LZ)	(ZH)	1.242	1.836	3.457				0.026	0.039	0.067
			(ZL)	1.539	3.109	7.803				0.027	0.040	0.061
		(ZH)	1.288	2.293	4.624							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BE05	A → Y0	(HH)	(LL)	1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
		(HZ)	2.348	3.377	5.634							
	EN → Y0	(LZ)	(ZH)	1.559	2.307	4.328				0.023	0.036	0.064
			(ZL)	1.706	3.606	9.328				0.022	0.033	0.051
		(ZH)	1.353	2.504	5.120							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BED5	A → Y0	(HH)	(LL)	1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
		(HZ)	2.348	3.377	5.634							
	EN → Y0	(LZ)	(ZH)	1.559	2.307	4.328				0.023	0.036	0.064
			(ZL)	1.706	3.606	9.328				0.022	0.033	0.051
		(ZH)	1.353	2.504	5.120							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BEU5	A → Y0	(HH)	(LL)	1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
		(HZ)	2.348	3.377	5.634							
	EN → Y0	(LZ)	(ZH)	1.559	2.307	4.328				0.023	0.036	0.064
			(ZL)	1.706	3.606	9.328				0.022	0.033	0.051
		(ZH)	1.353	2.504	5.120							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
BEW5	A → Y0	(HH)	(LL)	1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
		(HZ)	2.348	3.377	5.634							
	EN → Y0	(LZ)	(ZH)	1.559	2.307	4.328				0.023	0.036	0.064
			(ZL)	1.706	3.606	9.328				0.022	0.033	0.051
		(ZH)	1.353	2.504	5.120							
	Y0 → Y1	(HH)	(LL)	0.188	0.308	0.601	0.010	0.014	0.021			
			(LL)	0.145	0.239	0.443	0.011	0.014	0.021			
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEDF	A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
			(LL)	1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)	3.006	4.371	7.283							
		(LZ)	1.877	2.777	5.195							
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064	
	Y0 → Y1	(ZL)	1.424	2.718	5.634				0.020	0.030	0.047	
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
		(LL)	0.145	0.239	0.443	0.011	0.014	0.021				
	BEUF	A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035
(LL)				1.997	3.484	7.016				0.015	0.023	0.035
EN → Y0		(HZ)	3.006	4.371	7.283							
		(LZ)	1.877	2.777	5.195							
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064	
Y0 → Y1		(ZL)	1.424	2.718	5.634				0.020	0.030	0.047	
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
		(LL)	0.145	0.239	0.443	0.011	0.014	0.021				
BEWF		A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035
	(LL)			1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)	3.006	4.371	7.283							
		(LZ)	1.877	2.777	5.195							
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064	
	Y0 → Y1	(ZL)	1.424	2.718	5.634				0.020	0.030	0.047	
		(HH)	0.188	0.308	0.601	0.010	0.014	0.021				
		(LL)	0.145	0.239	0.443	0.011	0.014	0.021				

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Schmitt I/O Buffer					CMOS 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BSIUW	BSDUW	BSUWU	BSWUW	1	13	
6mA	BSICW	BSDCW	BSUCW	BSWCW	1	13	
9mA	BSI3W	BSD3W	BSU3W	BSW3W	1	13	
12mA	BSI1W	BSD1W	BSU1W	BSW1W	1	23	
18mA	BSI5W	BSD5W	BSU5W	BSW5W	1	23	
24mA	BSIFW	BSDFW	BSUFW	BSWFW	1	23	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		BSIUW to BSUWU	A	6.3	Y1
BSICW to BSWCW	A	6.3	Y1	24	
	EN	1.0			
BSI3W to BSW3W	A	6.3	Y1	24	
	EN	1.0			
BSI1W to BSW1W	A	16.9	Y1	24	
	EN	1.0			
BSI5W to BSW5W	A	16.9	Y1	24	
	EN	1.0			
BSIFW to BSWFW	A	16.9	Y1	24	
	EN	1.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X: Irrelevant  
Z: High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BSIUW	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.011	0.017	0.025	0.090	0.131
(HH)		0.780	1.214	2.365	0.010	0.015	0.022						
(LL)		1.187	1.883	3.417									
BSDUW	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.011	0.017	0.025	0.090	0.131
(HH)		0.780	1.214	2.365	0.010	0.015	0.022						
(LL)		1.187	1.883	3.417									
BSUWU	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.011	0.017	0.025	0.090	0.131
(HH)		0.780	1.214	2.365	0.010	0.015	0.022						
(LL)		1.187	1.883	3.417									
BSWUW	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.011	0.017	0.025	0.090	0.131
(HH)		0.780	1.214	2.365	0.010	0.015	0.022						
(LL)		1.187	1.883	3.417									
BSICW	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.011	0.017	0.025	0.045	0.066
(HH)		0.780	1.214	2.365	0.010	0.015	0.022						
(LL)		1.187	1.883	3.417									
BSDCW	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.011	0.017	0.025	0.045	0.066
(HH)		0.780	1.214	2.365	0.010	0.015	0.022						
(LL)		1.187	1.883	3.417									
BSUCW	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.011	0.017	0.025	0.045	0.066
(HH)		0.780	1.214	2.365	0.010	0.015	0.022						
(LL)		1.187	1.883	3.417									

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSWCW	A → Y0	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
	EN → Y0	(HZ)		1.602	2.366	4.209						
		(LZ)		0.547	0.906	1.819						
		(ZH)		1.164	2.076	4.626				0.038	0.053	0.080
	Y0 → Y1	(ZL)		0.931	1.622	3.317				0.045	0.066	0.098
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSI3W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSD3W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSU3W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSW3W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSI1W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSD1W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSU1W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSW1W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSI5W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSD5W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSU5W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSW5W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSIFW	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSDFW	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSUFW	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				
BSWFW	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
(HH)			0.780	1.214	2.365	0.011	0.017	0.025				
	(LL)		1.187	1.883	3.417	0.010	0.015	0.022				

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise Schmitt I/O Buffer					CMOS 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BFIUW	BFDUW	BFUWU	BFWUW	1	13	
6mA	BFICW	BFDCW	BFUCW	BFWCW	1	13	
9mA	BF13W	BFD3W	BFU3W	BFW3W	1	13	
12mA	BF11W	BFD1W	BFU1W	BFW1W	1	13	
18mA	BF15W	BFD5W	BFU5W	BFW5W	1	13	
24mA	BF1FW	BFD5W	BFU5W	BFW5W	1	13	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		BFIUW to BFWUW	A	6.1	Y1
BFICW to BFWCW	A	6.1	Y1	24	
BF13W to BFW3W	A	6.1	Y1	24	
BF11W to BFW1W	A	6.1	Y1	24	
BF15W to BFW5W	A	6.1	Y1	24	
BF1FW to BFWFW	A	6.1	Y1	24	

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFIUW	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013						
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.057	0.081	0.121
			(LL)	1.365	2.279	4.559	0.011	0.017	0.025	0.090	0.131	0.194
BFDUW	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013						
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.057	0.081	0.121
			(LL)	1.365	2.279	4.559	0.011	0.017	0.025	0.090	0.131	0.194
BFUWU	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013						
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.057	0.081	0.121
			(LL)	1.365	2.279	4.559	0.011	0.017	0.025	0.090	0.131	0.194
BFWUW	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013						
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.057	0.081	0.121
			(LL)	1.365	2.279	4.559	0.011	0.017	0.025	0.090	0.131	0.194
BFICW	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y0	(HZ)	(LZ)	1.054	1.423	2.365						
			(ZH)	0.927	1.364	2.581						
	Y0 → Y1	(HH)	(ZL)	1.388	2.613	6.285				0.040	0.058	0.090
			(LL)	1.265	2.149	4.276	0.011	0.017	0.025	0.047	0.068	0.101
BFDCW	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y0	(HZ)	(LZ)	1.054	1.423	2.365						
			(ZH)	0.927	1.364	2.581						
	Y0 → Y1	(HH)	(ZL)	1.388	2.613	6.285				0.040	0.058	0.090
			(LL)	1.265	2.149	4.276	0.011	0.017	0.025	0.047	0.068	0.101
BFUCW	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y0	(HZ)	(LZ)	1.054	1.423	2.365						
			(ZH)	0.927	1.364	2.581						
	Y0 → Y1	(HH)	(ZL)	1.388	2.613	6.285				0.040	0.058	0.090
			(LL)	1.265	2.149	4.276	0.011	0.017	0.025	0.047	0.068	0.101

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFWCW	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
		(HZ)	1.054	1.423	2.365							
	EN → Y0	(LZ)	(ZH)	0.927	1.364	2.581				0.040	0.058	0.090
			(ZL)	1.388	2.613	6.285				0.047	0.068	0.101
		(ZH)	1.265	2.149	4.276							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.429	2.884	7.106				0.028	0.042	0.070	
BFI3W	A → Y0	(LL)	(LL)	1.311	2.202	4.323				0.032	0.047	0.070
			(HZ)	1.476	2.066	3.447						
		(LZ)	1.086	1.602	3.023				0.028	0.042	0.070	
	EN → Y0	(ZH)	(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
			(ZL)	1.268	2.209	4.413						
		(HH)	0.780	1.214	2.365	0.011	0.017	0.025				
	Y0 → Y1	(LL)	(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
			(HH)	1.429	2.884	7.106				0.028	0.042	0.070
		BFD3W	A → Y0	(LL)	(LL)	1.311	2.202	4.323				0.032
(HZ)	1.476				2.066	3.447						
(LZ)	1.086			1.602	3.023				0.028	0.042	0.070	
EN → Y0	(ZH)		(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
			(ZL)	1.268	2.209	4.413						
	(HH)		0.780	1.214	2.365	0.011	0.017	0.025				
Y0 → Y1	(LL)		(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
			(HH)	1.429	2.884	7.106				0.028	0.042	0.070
	BFU3W		A → Y0	(LL)	(LL)	1.311	2.202	4.323				0.032
(HZ)		1.476			2.066	3.447						
(LZ)		1.086		1.602	3.023				0.028	0.042	0.070	
EN → Y0		(ZH)	(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
			(ZL)	1.268	2.209	4.413						
		(HH)	0.780	1.214	2.365	0.011	0.017	0.025				
Y0 → Y1		(LL)	(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
			(HH)	1.429	2.884	7.106				0.028	0.042	0.070
		BFW3W	A → Y0	(LL)	(LL)	1.311	2.202	4.323				0.032
(HZ)	1.476				2.066	3.447						
(LZ)	1.086			1.602	3.023				0.028	0.042	0.070	
EN → Y0	(ZH)		(ZL)	1.485	2.941	7.290				0.033	0.049	0.073
			(ZL)	1.268	2.209	4.413						
	(HH)		0.780	1.214	2.365	0.011	0.017	0.025				
Y0 → Y1	(LL)		(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
			(HH)	1.429	2.884	7.106				0.028	0.042	0.070
	BFI1W		A → Y0	(LL)	(LL)	1.390	2.366	4.674				0.026
(HZ)		1.692			2.390	3.993				0.025	0.037	0.056
(LZ)		1.242		1.836	3.457							
EN → Y0		(ZH)	(ZL)	1.539	3.109	7.803				0.026	0.039	0.067
			(ZL)	1.288	2.293	4.624				0.027	0.040	0.061
		(ZH)	1.288	2.293	4.624							
Y0 → Y1		(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.492	3.051	7.617				0.026	0.039	0.067	
BFD1W	A → Y0	(LL)	(LL)	1.390	2.366	4.674				0.025	0.037	0.056
			(HZ)	1.692	2.390	3.993						
		(LZ)	1.242	1.836	3.457				0.026	0.039	0.067	
	EN → Y0	(ZH)	(ZL)	1.539	3.109	7.803				0.027	0.040	0.061
			(ZL)	1.288	2.293	4.624						
		(ZH)	1.288	2.293	4.624							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.492	3.051	7.617				0.026	0.039	0.067	

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFU1W	A → Y0	(HH)	(LL)	1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
		(HZ)	1.692	2.390	3.993							
	EN → Y0	(LZ)	(ZH)	1.242	1.836	3.457				0.026	0.039	0.067
			(ZH)	1.539	3.109	7.803				0.027	0.040	0.061
		(ZL)	1.288	2.293	4.624							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.492	3.051	7.617				0.026	0.039	0.067	
BFW1W	A → Y0	(LL)	(LL)	1.390	2.366	4.674				0.025	0.037	0.056
			(HZ)	1.692	2.390	3.993						
		(LZ)	1.242	1.836	3.457				0.026	0.039	0.067	
	EN → Y0	(ZH)	(ZL)	1.539	3.109	7.803				0.027	0.040	0.061
			(ZL)	1.288	2.293	4.624						
		(ZH)	1.288	2.293	4.624							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.492	3.051	7.617				0.026	0.039	0.067	
BFI5W	A → Y0	(LL)	(LL)	1.684	3.547	9.136				0.022	0.036	0.064
			(LL)	1.687	2.913	5.814				0.018	0.028	0.042
		(HZ)	2.348	3.377	5.634							
	EN → Y0	(LZ)	(ZH)	1.559	2.307	4.328				0.023	0.036	0.064
			(ZH)	1.706	3.606	9.328				0.022	0.033	0.051
		(ZL)	1.353	2.504	5.120							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.684	3.547	9.136				0.022	0.036	0.064	
BFD5W	A → Y0	(LL)	(LL)	1.687	2.913	5.814				0.018	0.028	0.042
			(HZ)	2.348	3.377	5.634						
		(LZ)	1.559	2.307	4.328				0.023	0.036	0.064	
	EN → Y0	(ZH)	(ZL)	1.706	3.606	9.328				0.022	0.033	0.051
			(ZL)	1.353	2.504	5.120						
		(ZH)	1.706	3.606	9.328							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.684	3.547	9.136				0.022	0.036	0.064	
BFU5W	A → Y0	(LL)	(LL)	1.687	2.913	5.814				0.018	0.028	0.042
			(HZ)	2.348	3.377	5.634						
		(LZ)	1.559	2.307	4.328				0.023	0.036	0.064	
	EN → Y0	(ZH)	(ZL)	1.706	3.606	9.328				0.022	0.033	0.051
			(ZL)	1.353	2.504	5.120						
		(ZH)	1.706	3.606	9.328							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.684	3.547	9.136				0.022	0.036	0.064	
BFW5W	A → Y0	(LL)	(LL)	1.687	2.913	5.814				0.018	0.028	0.042
			(HZ)	2.348	3.377	5.634						
		(LZ)	1.559	2.307	4.328				0.023	0.036	0.064	
	EN → Y0	(ZH)	(ZL)	1.706	3.606	9.328				0.022	0.033	0.051
			(ZL)	1.353	2.504	5.120						
		(ZH)	1.706	3.606	9.328							
	Y0 → Y1	(HH)	(LL)	0.780	1.214	2.365	0.011	0.017	0.025			
			(LL)	1.187	1.883	3.417	0.010	0.015	0.022			
		(HH)	1.684	3.547	9.136				0.022	0.036	0.064	
BFIFW	A → Y0	(LL)	(LL)	1.997	3.484	7.016				0.021	0.035	0.065
			(HZ)	3.006	4.371	7.283				0.015	0.023	0.035
		(LZ)	1.877	2.777	5.195							
	EN → Y0	(ZH)	(ZL)	1.867	4.086	10.808				0.022	0.035	0.064
			(ZL)	1.424								

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFDFW	A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
				1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)		3.006	4.371	7.283						
				1.877	2.777	5.195						
				1.867	4.086	10.808				0.022	0.035	0.064
	Y0 → Y1	(ZH)		1.424	2.718	5.634				0.020	0.030	0.047
				0.780	1.214	2.365	0.011	0.017	0.025			
				1.187	1.883	3.417	0.010	0.015	0.022			
BFUFW	A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
				1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)		3.006	4.371	7.283						
				1.877	2.777	5.195						
				1.867	4.086	10.808				0.022	0.035	0.064
	Y0 → Y1	(ZH)		1.424	2.718	5.634				0.020	0.030	0.047
				0.780	1.214	2.365	0.011	0.017	0.025			
				1.187	1.883	3.417	0.010	0.015	0.022			
BFWFW	A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
				1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)		3.006	4.371	7.283						
				1.877	2.777	5.195						
				1.867	4.086	10.808				0.022	0.035	0.064
	Y0 → Y1	(ZH)		1.424	2.718	5.634				0.020	0.030	0.047
				0.780	1.214	2.365	0.011	0.017	0.025			
				1.187	1.883	3.417	0.010	0.015	0.022			

[MEMO]

Chapter 1 Interface Block



Chapter 1 Interface Block

Function	I/O Buffer with EN(AND)						CMOS 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN2U	BN4U			1	13	
6mA	BN2C	BN4C			1	13	
9mA	BN23	BN43			1	13	
12mA	BN21	BN41			1	23	
18mA	BN25	BN45			1	23	
24mA	BN2F	BN4F			1	23	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	BN2U to BN4U	A	6.3	Y1	34
		EN	1.0		
		ENI	3.0		
	BN2C to BN4C	A	6.3	Y1	34
		EN	1.0		
		ENI	3.0		
	BN23 to BN43	A	6.3	Y1	34
		EN	1.0		
		ENI	3.0		
	BN21 to BN41	A	16.9	Y1	34
		EN	1.0		
		ENI	3.0		
BN25 to BN45	A	16.9	Y1	34	
	EN	1.0			
	ENI	3.0			
BN2F to BN4F	A	16.9	Y1	34	
	EN	1.0			
	ENI	3.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	0
1	0	0
1	1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN2U	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(LZ)	(ZH)	0.469	0.771	1.492				0.056	0.078	0.114
			(ZH)	1.149	2.002	4.411				0.090	0.131	0.193
			(ZL)	1.074	1.852	3.792						
	ENI → Y1	(HH)	(LL)	0.158	0.244	0.510	0.010	0.014	0.021			
			(LL)	0.342	0.488	0.939	0.011	0.015	0.021			
			(LL)	0.109	0.219	0.462	0.010	0.014	0.021			
	Y0 → Y1	(HH)	(LL)	0.253	0.371	0.715	0.011	0.015	0.021			
(LL)			0.839	1.469	3.318				0.056	0.078	0.114	
(LL)			0.963	1.638	3.333				0.089	0.131	0.192	
BN4U	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(LZ)	(ZH)	0.469	0.771	1.492				0.056	0.078	0.114
			(ZH)	1.149	2.002	4.411				0.090	0.131	0.193
			(ZL)	1.074	1.852	3.792						
	ENI → Y1	(HH)	(LL)	0.158	0.244	0.510	0.010	0.014	0.021			
			(LL)	0.342	0.488	0.939	0.011	0.015	0.021			
			(LL)	0.109	0.219	0.462	0.010	0.014	0.021			
	Y0 → Y1	(HH)	(LL)	0.253	0.371	0.715	0.011	0.015	0.021			
(LL)			0.839	1.469	3.318				0.056	0.078	0.114	
(LL)			0.963	1.638	3.333				0.089	0.131	0.192	
BN2C	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(LZ)	(ZH)	0.547	0.906	1.819				0.038	0.053	0.080
			(ZH)	1.164	2.076	4.626				0.045	0.066	0.098
			(ZL)	0.931	1.622	3.317						
	ENI → Y1	(HH)	(LL)	0.158	0.244	0.510	0.010	0.014	0.021			
			(LL)	0.342	0.488	0.939	0.011	0.015	0.021			
			(LL)	0.109	0.219	0.462	0.010	0.014	0.021			
	Y0 → Y1	(HH)	(LL)	0.253	0.371	0.715	0.011	0.015	0.021			
(LL)			0.857	1.549	3.541				0.038	0.053	0.080	
(LL)			0.857	1.450	2.908				0.044	0.065	0.097	
BN4C	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(LZ)	(ZH)	0.547	0.906	1.819				0.038	0.053	0.080
			(ZH)	1.164	2.076	4.626				0.045	0.066	0.098
			(ZL)	0.931	1.622	3.317						
	ENI → Y1	(HH)	(LL)	0.158	0.244	0.510	0.010	0.014	0.021			
			(LL)	0.342	0.488	0.939	0.011	0.015	0.021			
			(LL)	0.109	0.219	0.462	0.010	0.014	0.021			
	Y0 → Y1	(HH)	(LL)	0.253	0.371	0.715	0.011	0.015	0.021			
(LL)			0.927	1.751	4.088				0.024	0.036	0.056	
(LL)			0.979	1.652	3.277				0.029	0.043	0.064	
BN23	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(LZ)	(ZH)	0.607	1.003	2.005				0.024	0.035	0.056
			(ZH)	1.232	2.276	5.174				0.031	0.045	0.067
			(ZL)	0.913	1.619	3.323						
	ENI → Y1	(HH)	(LL)	0.158	0.244	0.510	0.010	0.014	0.021			
			(LL)	0.342	0.488	0.939	0.011	0.015	0.021			
			(LL)	0.109	0.219	0.462	0.010	0.014	0.021			
	Y0 → Y1	(HH)	(LL)	0.253	0.371	0.715	0.011	0.015	0.021			
(LL)			0.927	1.751	4.088				0.024	0.036	0.056	
(LL)			0.979	1.652	3.277				0.029	0.043	0.064	
BN43	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(LZ)	(ZH)	0.607	1.003	2.005				0.024	0.035	0.056
			(ZH)	1.232	2.276	5.174				0.031	0.045	0.067
			(ZL)	0.913	1.619	3.323						

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BN21	ENI → Y1	(HH)		0.158	0.244	0.510	0.010	0.014	0.021				
		(LL)		0.342	0.488	0.939	0.011	0.015	0.021				
	Y0 → Y1	(HH)		0.109	0.219	0.462	0.010	0.014	0.021				
		(LL)		0.253	0.371	0.715	0.011	0.015	0.021				
	BN41	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
			(LL)		0.644	1.115	2.283				0.022	0.032	0.048
EN → Y0		(HZ)		1.929	3.060	5.656							
		(LZ)		0.770	1.362	2.783							
ENI → Y1		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045	
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050	
BN25	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039	
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033	
	EN → Y0	(HZ)		2.463	3.879	7.031							
		(LZ)		0.858	1.497	3.031							
	ENI → Y1	(ZH)		1.317	2.435	5.418				0.015	0.023	0.038	
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037	
BN45	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039	
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033	
	EN → Y0	(HZ)		2.463	3.879	7.031							
		(LZ)		0.858	1.497	3.031							
	ENI → Y1	(ZH)		1.317	2.435	5.418				0.015	0.023	0.038	
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037	
BN2F	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037	
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027	
	EN → Y0	(HZ)		3.004	4.704	8.420							
		(LZ)		0.945	1.629	3.274							
	ENI → Y1	(ZH)		1.377	2.588	5.829				0.013	0.021	0.037	
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031	
Y0 → Y1	(HH)		0.158	0.244	0.510	0.010	0.014	0.021					
	(LL)		0.342	0.488	0.939	0.011	0.015	0.021					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN4F	A → Y0	(HH)		0.819	1.598	3.790						
		(LL)		0.881	1.569	3.211						
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
	ENI → Y1	(ZH)		1.377	2.588	5.829				0.010	0.014	0.021
		(ZL)		0.847	1.572	3.332				0.010	0.015	0.021
Y0 → Y1	(HH)		0.109	0.219	0.462	0.010	0.014	0.021				
	(LL)		0.253	0.371	0.715	0.011	0.015	0.021				

Chapter 1 Interface Block

Function	I/O Buffer with EN(OR)						CMOS 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN3U	BN5U			1	11	
6mA	BN3C	BN5C			1	11	
9mA	BN33	BN53			1	11	
12mA	BN31	BN51			1	21	
18mA	BN35	BN55			1	21	
24mA	BN3F	BN5F			1	21	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	BN3U to BN5U	A	6.3	Y1	34
		EN	1.0		
		ENI	3.0		
	BN3C to BN5C	A	6.3	Y1	34
		EN	1.0		
		ENI	3.0		
	BN33 to BN53	A	6.3	Y1	34
		EN	1.0		
		ENI	3.0		
	BN31 to BN51	A	16.9	Y1	34
		EN	1.0		
		ENI	3.0		
BN35 to BN55	A	16.9	Y1	34	
	EN	1.0			
	ENI	3.0			
BN3F to BN5F	A	16.9	Y1	34	
	EN	1.0			
	ENI	3.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	1
1	0	1
1	1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN3U	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(HZ)	(LZ)	0.469	0.771	1.492				0.056	0.078	0.114
			(ZH)	1.149	2.002	4.411				0.090	0.131	0.193
			(ZL)	1.074	1.852	3.792						
	ENI → Y1	(HH)	(LL)	0.138	0.225	0.411	0.010	0.014	0.021			
			(LL)	0.309	0.534	1.127	0.011	0.015	0.023			
			(HH)	0.130	0.233	0.450	0.010	0.014	0.021			
Y0 → Y1	(HH)	(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
BN5U	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(HZ)	(LZ)	0.469	0.771	1.492				0.056	0.078	0.114
			(ZH)	1.149	2.002	4.411				0.090	0.131	0.193
			(ZL)	1.074	1.852	3.792						
	ENI → Y1	(HH)	(LL)	0.138	0.225	0.411	0.010	0.014	0.021			
			(LL)	0.309	0.534	1.127	0.011	0.015	0.023			
			(HH)	0.130	0.233	0.450	0.010	0.014	0.021			
Y0 → Y1	(HH)	(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
BN3C	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(HZ)	(LZ)	0.547	0.906	1.819				0.038	0.053	0.080
			(ZH)	1.164	2.076	4.626				0.045	0.066	0.098
			(ZL)	0.931	1.622	3.317						
	ENI → Y1	(HH)	(LL)	0.138	0.225	0.411	0.010	0.014	0.021			
			(LL)	0.309	0.534	1.127	0.011	0.015	0.023			
			(HH)	0.130	0.233	0.450	0.010	0.014	0.021			
Y0 → Y1	(HH)	(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
BN5C	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(HZ)	(LZ)	0.547	0.906	1.819				0.038	0.053	0.080
			(ZH)	1.164	2.076	4.626				0.045	0.066	0.098
			(ZL)	0.931	1.622	3.317						
	ENI → Y1	(HH)	(LL)	0.138	0.225	0.411	0.010	0.014	0.021			
			(LL)	0.309	0.534	1.127	0.011	0.015	0.023			
			(HH)	0.130	0.233	0.450	0.010	0.014	0.021			
Y0 → Y1	(HH)	(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
BN33	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(HZ)	(LZ)	0.607	1.003	2.005				0.024	0.035	0.056
			(ZH)	1.232	2.276	5.174				0.031	0.045	0.067
			(ZL)	0.913	1.619	3.323						
	ENI → Y1	(HH)	(LL)	0.138	0.225	0.411	0.010	0.014	0.021			
			(LL)	0.309	0.534	1.127	0.011	0.015	0.023			
			(HH)	0.130	0.233	0.450	0.010	0.014	0.021			
Y0 → Y1	(HH)	(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
		(LL)	0.333	0.505	1.014	0.011	0.015	0.023				
BN53	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(HZ)	(LZ)	0.607	1.003	2.005				0.024	0.035	0.056
			(ZH)	1.232	2.276	5.174				0.031	0.045	0.067
			(ZL)	0.913	1.619	3.323						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN31	ENI → Y1	(HH)		0.138	0.225	0.411	0.010	0.014	0.021			
		(LL)		0.309	0.534	1.127	0.011	0.015	0.023			
	Y0 → Y1	(HH)		0.130	0.233	0.450	0.010	0.014	0.021			
		(LL)		0.333	0.505	1.014	0.011	0.015	0.023			
	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
(HZ)			1.929	3.060	5.656							
(LZ)			0.770	1.362	2.783							
EN → Y0	(ZH)		1.247	2.257	4.957				0.020	0.029	0.045	
	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050	
ENI → Y1	(HH)		0.138	0.225	0.411	0.010	0.014	0.021				
	(LL)		0.309	0.534	1.127	0.011	0.015	0.023				
Y0 → Y1	(HH)		0.130	0.233	0.450	0.010	0.014	0.021				
	(LL)		0.333	0.505	1.014	0.011	0.015	0.023				
BN51	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
	(ZH)		1.247	2.257	4.957				0.020	0.029	0.045	
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
ENI → Y1	(HH)		0.138	0.225	0.411	0.010	0.014	0.021				
	(LL)		0.309	0.534	1.127	0.011	0.015	0.023				
Y0 → Y1	(HH)		0.130	0.233	0.450	0.010	0.014	0.021				
	(LL)		0.333	0.505	1.014	0.011	0.015	0.023				
BN35	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
	(ZH)		1.317	2.435	5.418				0.015	0.023	0.038	
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
ENI → Y1	(HH)		0.138	0.225	0.411	0.010	0.014	0.021				
	(LL)		0.309	0.534	1.127	0.011	0.015	0.023				
Y0 → Y1	(HH)		0.130	0.233	0.450	0.010	0.014	0.021				
	(LL)		0.333	0.505	1.014	0.011	0.015	0.023				
BN55	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
	(ZH)		1.317	2.435	5.418				0.015	0.023	0.038	
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
ENI → Y1	(HH)		0.138	0.225	0.411	0.010	0.014	0.021				
	(LL)		0.309	0.534	1.127	0.011	0.015	0.023				
Y0 → Y1	(HH)		0.130	0.233	0.450	0.010	0.014	0.021				
	(LL)		0.333	0.505	1.014	0.011	0.015	0.023				
BN3F	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
	(ZH)		1.377	2.588	5.829				0.013	0.021	0.037	
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
ENI → Y1	(HH)		0.138	0.225	0.411	0.010	0.014	0.021				
	(LL)		0.309	0.534	1.127	0.011	0.015	0.023				
Y0 → Y1	(HH)		0.130	0.233	0.450	0.010	0.014	0.021				
	(LL)		0.333	0.505	1.014	0.011	0.015	0.023				

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN5F	A → Y0	(HH)		0.819	1.598	3.790						
		(LL)		0.881	1.569	3.211						
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
	(ZH)		1.377	2.588	5.829				0.013	0.021	0.037	
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
ENI → Y1	(HH)		0.138	0.225	0.411	0.010	0.014	0.021				
	(LL)		0.309	0.534	1.127	0.011	0.015	0.023				
Y0 → Y1	(HH)		0.130	0.233	0.450	0.010	0.014	0.021				
	(LL)		0.333	0.505	1.014	0.011	0.015	0.023				

[MEMO]

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## 1.2 TTL Level

### Chapter 1 Interface Block

Function	Input Buffer					3.3 V	
Block type							
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
Normal	FI02	FID2	FIU2	FIW2	1	3	
Schmitt	FIS2W	FDS2W	FUS2W	FWS2W	1	6	
Clock							

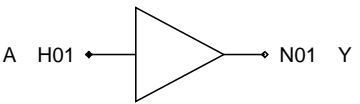
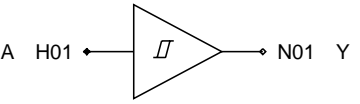
  

Logic Diagram for "Normal"	Truth Table																			
	<table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>	A	Y	1	1	0	0													
A	Y																			
1	1																			
0	0																			
Logic Diagram for "Schmitt"	Block type																			
	<table border="1"> <thead> <tr> <th rowspan="2">Block type</th> <th colspan="2">Input</th> <th colspan="2">Output</th> </tr> <tr> <th>Symbol</th> <th>Fan-In</th> <th>Symbol</th> <th>Fan-Out</th> </tr> </thead> <tbody> <tr> <td>FI02 to FIW2</td> <td>A</td> <td>-</td> <td>Y</td> <td>22</td> </tr> <tr> <td>FIS2W to FWS2W</td> <td>A</td> <td>-</td> <td>Y</td> <td>19</td> </tr> </tbody> </table>	Block type	Input		Output		Symbol	Fan-In	Symbol	Fan-Out	FI02 to FIW2	A	-	Y	22	FIS2W to FWS2W	A	-	Y	19
Block type	Input		Output																	
	Symbol	Fan-In	Symbol	Fan-Out																
FI02 to FIW2	A	-	Y	22																
FIS2W to FWS2W	A	-	Y	19																
Logic Diagram for "Clock"																				

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FI02	A → Y	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
FID2	A → Y	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
FIU2	A → Y	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
FIW2	A → Y	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
FIS2W	A → Y	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
FDS2W	A → Y	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
FUS2W	A → Y	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
FWS2W	A → Y	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)	3.005	4.875	8.847	0.014	0.020	0.030			

### Chapter 1 Interface Block

Function	Input Buffer with failsafe					3.3 V							
Block type													
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells							
Normal	FIA2	FDA2			1	3							
Schmitt	FIE2W	FDE2W			1	6							
Clock													
Logic Diagram for "Normal"				Truth Table									
				<table border="1"> <thead> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>				A	Y	1	1	0	0
A	Y												
1	1												
0	0												
Logic Diagram for "Schmitt"				Block type									
				Input		Output							
				Symbol	Fan-In	Symbol	Fan-Out						
				FIA2 to FDA2	A -	Y	22						
				FIE2W to FDE2W	A -	Y	19						
Logic Diagram for "Clock"													

### Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIA2	A → Y	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
FDA2	A → Y	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
FIE2W	A → Y	(HH)	0.672	1.030	1.867	0.010	0.016	0.024			
		(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
FDE2W	A → Y	(HH)	0.672	1.030	1.867	0.010	0.016	0.024			
		(LL)	3.005	4.875	8.847	0.014	0.020	0.030			



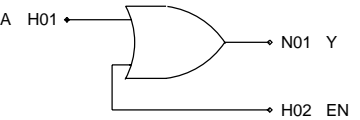
Chapter 1 Interface Block

Function	Input Buffer with EN(AND)					3.3 V																
Block type																						
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells																
Normal	FN12	FN22			1	7																
Schmitt																						
Clock																						
Logic Diagram for "Normal"				Truth Table																		
				<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	0	1	0	0	1	1	1
A	EN	Y																				
0	0	0																				
0	1	0																				
1	0	0																				
1	1	1																				
Logic Diagram for "Schmitt"				Block type																		
				Input		Output																
				Symbol	Fan-In	Symbol	Fan-Out															
				FN12 to FN22	A EN	- 4.0	Y 22															
Logic Diagram for "Clock"																						

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FN12	A → Y	(HH)	0.129	0.245	0.511	0.015	0.021	0.031			
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015			
	EN → Y	(HH)	0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)	0.241	0.353	0.667	0.008	0.010	0.015			
FN22	A → Y	(HH)	0.129	0.245	0.511	0.015	0.021	0.031			
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015			
	EN → Y	(HH)	0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)	0.241	0.353	0.667	0.008	0.010	0.015			

Chapter 1 Interface Block

Function	Input Buffer with EN(OR)					3.3 V																
Block type																						
Function	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells																
Normal	FN14	FN24			1	4																
Schmitt																						
Clock																						
Logic Diagram for "Normal"				Truth Table																		
				<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>				A	EN	Y	0	0	0	0	1	1	1	0	1	1	1	1
A	EN	Y																				
0	0	0																				
0	1	1																				
1	0	1																				
1	1	1																				
Logic Diagram for "Schmitt"				Block type																		
				Input		Output																
				Symbol	Fan-In	Symbol	Fan-Out															
				FN14 to FN24	-	Y	21															
Logic Diagram for "Clock"																						

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP. MAX.	
FN14	A → Y	(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
		(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
	EN → Y	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
		(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
FN24	A → Y	(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
		(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
	EN → Y	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
		(LL)	0.302	0.519	1.097	0.008	0.011	0.017			

### Chapter 1 Interface Block

Function	N-ch open drain I/O Buffer with failsafe					TTL 3.3 V
Block type						
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells
1mA						
2mA						
3mA						
6mA						
9mA	EBA2				1	7
12mA	EBAA				1	7
18mA	EBA6				1	7
24mA	EBAE				1	7

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		EBA2	A	6.1	Y1
EBAA	A	6.1	Y1	22	
EBA6	A	6.1	Y1	22	
EBAE	A	6.1	Y1	22	

Truth Table	
A	Y0
1	Z
0	0

Z:High Impedance  
Connect a pull-up resistor to get a high level

Y0	Y1
0	0
1	1

### Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
EBA2	A	→	Y0	(LZ)	0.377	0.530	0.967				0.030	0.044	0.065
				(ZL)	0.391	0.712	1.453						
	Y0	→	Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
EBAA	A	→	Y0	(LZ)	0.438	0.625	1.146				0.023	0.033	0.050
				(ZL)	0.386	0.719	1.478						
	Y0	→	Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
EBA6	A	→	Y0	(LZ)	0.562	0.813	1.502				0.016	0.024	0.036
				(ZL)	0.399	0.768	1.598						
	Y0	→	Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
EBAE	A	→	Y0	(LZ)	0.684	1.000	1.854				0.013	0.020	0.030
				(ZL)	0.414	0.817	1.721						
	Y0	→	Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031			

### Chapter 1 Interface Block

Function	N-ch open drain Schmitt I/O Buffer with failsafe					TTL 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA							
6mA							
9mA	EBE2W				1	10	
12mA	EBEAW				1	10	
18mA	EBE6W				1	10	
24mA	EBEEW				1	10	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
		EBE2W	A	6.1	Y1
EBEAW	A	6.1	Y1	19	
EBE6W	A	6.1	Y1	19	
EBEEW	A	6.1	Y1	19	

Truth Table	
A	Y0
1	Z
0	0

Z:High Impedance  
Connect a pull-up resistor to get a high level

Y0	Y1
0	0
1	1

### Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
EBE2W	A	→	Y0	(LZ)	0.377	0.530	0.967				0.030	0.044	0.065
				(ZL)	0.391	0.712	1.453						
	Y0	→	Y1	(HH)	0.672	1.030	1.867	0.010	0.016	0.024			
EBEAW				(LL)	3.005	4.875	8.847	0.014	0.020	0.030	0.023	0.033	0.050
	A	→	Y0	(LZ)	0.438	0.625	1.146						
				(ZL)	0.386	0.719	1.478						
EBE6W	Y0	→	Y1	(HH)	0.672	1.030	1.867	0.010	0.016	0.024	0.016	0.024	0.036
				(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
	A	→	Y0	(LZ)	0.562	0.813	1.502						
EBEEW				(ZL)	0.399	0.768	1.598				0.013	0.020	0.030
	A	→	Y0	(LZ)	0.684	1.000	1.854						
				(ZL)	0.414	0.817	1.721						
			(HH)	0.672	1.030	1.867	0.010	0.016	0.024	0.013	0.020	0.030	
Y0	→	Y1	(LL)	3.005	4.875	8.847	0.014	0.020	0.030				
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030				

Chapter 1 Interface Block

Function	I/O Buffer					TTL 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	B00V	B0DV	B0UV	B0WV	1	10	
6mA	B00D	B0DD	B0UD	B0WD	1	10	
9mA	B004	B0D4	B0U4	B0W4	1	10	
12mA	B002	B0D2	B0U2	B0W2	1	20	
18mA	B006	B0D6	B0U6	B0W6	1	20	
24mA	B00G	B0DG	B0UG	B0WG	1	20	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			B00V to B0WV	A	6.3
	EN	1.0			
	B00D to B0WD	A	6.3	Y1	22
		EN	1.0		
	B004 to B0W4	A	6.3	Y1	22
		EN	1.0		
	B002 to B0W2	A	16.9	Y1	22
		EN	1.0		
	B006 to B0W6	A	16.9	Y1	22
		EN	1.0		
	B00G to B0WG	A	16.9	Y1	22
		EN	1.0		

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			tLDo (ns)			t1			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
B00V	A → Y0	(HH)		0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.015	0.021	0.031	0.090	0.131
(HH)		0.115	0.215	0.422	0.015	0.021	0.031						
(LL)		0.240	0.366	0.699	0.008	0.010	0.015						
B0DV	A → Y0	(HH)		0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.015	0.021	0.031	0.090	0.131
(HH)		0.115	0.215	0.422	0.015	0.021	0.031						
(LL)		0.240	0.366	0.699	0.008	0.010	0.015						
B0UV	A → Y0	(HH)		0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.015	0.021	0.031	0.090	0.131
(HH)		0.115	0.215	0.422	0.015	0.021	0.031						
(LL)		0.240	0.366	0.699	0.008	0.010	0.015						
B0WV	A → Y0	(HH)		0.839	1.469	3.318				0.056	0.078	0.114	
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	1.259	1.846	3.271								
		(LZ)	0.469	0.771	1.492								
		(ZH)	1.149	2.002	4.411				0.056	0.078	0.114		
	Y0 → Y1	(ZL)	1.074	1.852	3.792				0.015	0.021	0.031	0.090	0.131
(HH)		0.115	0.215	0.422	0.015	0.021	0.031						
(LL)		0.240	0.366	0.699	0.008	0.010	0.015						
B00D	A → Y0	(HH)		0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.015	0.021	0.031	0.045	0.066
(HH)		0.115	0.215	0.422	0.015	0.021	0.031						
(LL)		0.240	0.366	0.699	0.008	0.010	0.015						
B0DD	A → Y0	(HH)		0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.015	0.021	0.031	0.045	0.066
(HH)		0.115	0.215	0.422	0.015	0.021	0.031						
(LL)		0.240	0.366	0.699	0.008	0.010	0.015						
B0UD	A → Y0	(HH)		0.857	1.549	3.541				0.038	0.053	0.080	
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	1.602	2.366	4.209								
		(LZ)	0.547	0.906	1.819								
		(ZH)	1.164	2.076	4.626				0.038	0.053	0.080		
	Y0 → Y1	(ZL)	0.931	1.622	3.317				0.015	0.021	0.031	0.045	0.066
(HH)		0.115	0.215	0.422	0.015	0.021	0.031						
(LL)		0.240	0.366	0.699	0.008	0.010	0.015						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0WD	A → Y0	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
	EN → Y0	(HZ)		1.602	2.366	4.209						
		(LZ)		0.547	0.906	1.819						
		(ZH)		1.164	2.076	4.626				0.038	0.053	0.080
	Y0 → Y1	(ZL)		0.931	1.622	3.317				0.045	0.066	0.098
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B004	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0D4	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0U4	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0W4	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
	EN → Y0	(HZ)		2.160	3.204	5.612						
		(LZ)		0.607	1.003	2.005						
		(ZH)		1.232	2.276	5.174				0.024	0.035	0.056
	Y0 → Y1	(ZL)		0.913	1.619	3.323				0.031	0.045	0.067
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B002	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0D2	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B0U2	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0W2	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
	Y0 → Y1	(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B006	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0D6	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0U6	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B0W6	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
	Y0 → Y1	(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					
B00G	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
(HH)			0.115	0.215	0.422	0.015	0.021	0.031				
(LL)		0.240	0.366	0.699	0.008	0.010	0.015					

Chapter 1 Interface Block

Block type	Switching speed										
	Path		tLDO (ns)			t 1			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BODG	A → Y0	(HH)	0.819	1.598	3.790				0.013	0.021	0.037
		(LL)	0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)	3.004	4.704	8.420						
		(LZ)	0.945	1.629	3.274						
		(ZH)	1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)	0.847	1.572	3.332				0.013	0.020	0.031
		(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
	BOUG	A → Y0	(HH)	0.819	1.598	3.790				0.013	0.021
(LL)			0.881	1.569	3.211				0.012	0.018	0.027
EN → Y0		(HZ)	3.004	4.704	8.420						
		(LZ)	0.945	1.629	3.274						
		(ZH)	1.377	2.588	5.829				0.013	0.021	0.037
Y0 → Y1		(ZL)	0.847	1.572	3.332				0.013	0.020	0.031
		(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
BOWG		A → Y0	(HH)	0.819	1.598	3.790				0.013	0.021
	(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)	3.004	4.704	8.420						
		(LZ)	0.945	1.629	3.274						
		(ZH)	1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)	0.847	1.572	3.332				0.013	0.020	0.031
		(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise I/O Buffer						TTL 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BE0V	BEDV	BEUV	BEWV	1	10	
6mA	BE0D	BEDD	BEUD	BEWD	1	10	
9mA	BE04	BED4	BEU4	BEW4	1	10	
12mA	BE02	BED2	BEU2	BEW2	1	10	
18mA	BE06	BED6	BEU6	BEW6	1	10	
24mA	BE0G	BEDG	BEUG	BEWG	1	10	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	BE0V to BEWV	A	6.1	Y1	22
	EN	4.0			
	BE0D to BEWD	A	6.1	Y1	22
	EN	4.0			
	BE04 to BEW4	A	6.1	Y1	22
	EN	4.0			
	BE02 to BEW2	A	6.1	Y1	22
	EN	4.0			
	BE06 to BEW6	A	6.1	Y1	22
	EN	4.0			
BE0G to BEWG	A	6.1	Y1	22	
EN	4.0				

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BE0V	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013				0.057	0.081	0.121
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.090	0.131	0.194
			(LL)	1.365	2.279	4.559	0.015	0.021	0.031	0.057	0.081	0.121
BEDV	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013				0.057	0.081	0.121
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.090	0.131	0.194
			(LL)	1.365	2.279	4.559	0.015	0.021	0.031	0.057	0.081	0.121
BEUV	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013				0.057	0.081	0.121
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.090	0.131	0.194
			(LL)	1.365	2.279	4.559	0.015	0.021	0.031	0.057	0.081	0.121
BEWV	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	(LZ)	0.785	1.011	1.593						
			(ZH)	0.745	1.089	2.013				0.057	0.081	0.121
	Y0 → Y1	(HH)	(ZL)	1.340	2.445	5.805				0.090	0.131	0.194
			(LL)	1.365	2.279	4.559	0.015	0.021	0.031	0.057	0.081	0.121
BE0D	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y0	(HZ)	(LZ)	1.054	1.423	2.365						
			(ZH)	0.927	1.364	2.581				0.040	0.058	0.090
	Y0 → Y1	(HH)	(ZL)	1.388	2.613	6.285				0.040	0.058	0.090
			(LL)	1.265	2.149	4.276	0.015	0.021	0.031	0.047	0.068	0.101
BEDD	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y0	(HZ)	(LZ)	1.054	1.423	2.365						
			(ZH)	0.927	1.364	2.581				0.040	0.058	0.090
	Y0 → Y1	(HH)	(ZL)	1.388	2.613	6.285				0.040	0.058	0.090
			(LL)	1.265	2.149	4.276	0.015	0.021	0.031	0.047	0.068	0.101
BEUD	A → Y0	(HH)	(LL)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
	EN → Y0	(HZ)	(LZ)	1.054	1.423	2.365						
			(ZH)	0.927	1.364	2.581				0.040	0.058	0.090
	Y0 → Y1	(HH)	(ZL)	1.388	2.613	6.285				0.040	0.058	0.090
			(LL)	1.265	2.149	4.276	0.015	0.021	0.031	0.047	0.068	0.101



Chapter 1 Interface Block

Block type	Switching speed														
	Path			tLD0 (ns)			t 1			T					
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
BEWD	A → Y0	(HH)	1.326	2.555	6.105				0.040	0.058	0.090				
			(LL)	1.185	1.984							3.930	0.046	0.068	0.101
			(HZ)	1.054	1.423							2.365			
	EN → Y0	(LZ)	0.927	1.364	2.581				0.040	0.058	0.090				
			(ZH)	1.388	2.613							6.285	0.047	0.068	0.101
			(ZL)	1.265	2.149							4.276			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BE04	A → Y0	(HH)	1.429	2.884	7.106				0.028	0.042	0.070				
			(LL)	1.311	2.202							4.323	0.032	0.047	0.070
			(HZ)	1.476	2.066							3.447			
	EN → Y0	(LZ)	1.086	1.602	3.023				0.028	0.042	0.070				
			(ZH)	1.485	2.941							7.290	0.033	0.049	0.073
			(ZL)	1.268	2.209							4.413			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BED4	A → Y0	(HH)	1.429	2.884	7.106				0.028	0.042	0.070				
			(LL)	1.311	2.202							4.323	0.032	0.047	0.070
			(HZ)	1.476	2.066							3.447			
	EN → Y0	(LZ)	1.086	1.602	3.023				0.028	0.042	0.070				
			(ZH)	1.485	2.941							7.290	0.033	0.049	0.073
			(ZL)	1.268	2.209							4.413			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BEU4	A → Y0	(HH)	1.429	2.884	7.106				0.028	0.042	0.070				
			(LL)	1.311	2.202							4.323	0.032	0.047	0.070
			(HZ)	1.476	2.066							3.447			
	EN → Y0	(LZ)	1.086	1.602	3.023				0.028	0.042	0.070				
			(ZH)	1.485	2.941							7.290	0.033	0.049	0.073
			(ZL)	1.268	2.209							4.413			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BEW4	A → Y0	(HH)	1.429	2.884	7.106				0.028	0.042	0.070				
			(LL)	1.311	2.202							4.323	0.032	0.047	0.070
			(HZ)	1.476	2.066							3.447			
	EN → Y0	(LZ)	1.086	1.602	3.023				0.028	0.042	0.070				
			(ZH)	1.485	2.941							7.290	0.033	0.049	0.073
			(ZL)	1.268	2.209							4.413			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BE02	A → Y0	(HH)	1.492	3.051	7.617				0.026	0.039	0.067				
			(LL)	1.390	2.366							4.674	0.025	0.037	0.056
			(HZ)	1.692	2.390							3.993			
	EN → Y0	(LZ)	1.242	1.836	3.457				0.026	0.039	0.067				
			(ZH)	1.539	3.109							7.803	0.027	0.040	0.061
			(ZL)	1.288	2.293							4.624			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BED2	A → Y0	(HH)	1.492	3.051	7.617				0.026	0.039	0.067				
			(LL)	1.390	2.366							4.674	0.025	0.037	0.056
			(HZ)	1.692	2.390							3.993			
	EN → Y0	(LZ)	1.242	1.836	3.457				0.026	0.039	0.067				
			(ZH)	1.539	3.109							7.803	0.027	0.040	0.061
			(ZL)	1.288	2.293							4.624			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			

Chapter 1 Interface Block

Block type	Switching speed														
	Path			tLD0 (ns)			t 1			T					
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
BEU2	A → Y0	(HH)	1.492	3.051	7.617				0.026	0.039	0.067				
			(LL)	1.390	2.366							4.674	0.025	0.037	0.056
			(HZ)	1.692	2.390							3.993			
	EN → Y0	(LZ)	1.242	1.836	3.457				0.026	0.039	0.067				
			(ZH)	1.539	3.109							7.803	0.027	0.040	0.061
			(ZL)	1.288	2.293							4.624			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BEW2	A → Y0	(HH)	1.492	3.051	7.617				0.026	0.039	0.067				
			(LL)	1.390	2.366							4.674	0.025	0.037	0.056
			(HZ)	1.692	2.390							3.993			
	EN → Y0	(LZ)	1.242	1.836	3.457				0.026	0.039	0.067				
			(ZH)	1.539	3.109							7.803	0.027	0.040	0.061
			(ZL)	1.288	2.293							4.624			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BE06	A → Y0	(HH)	1.684	3.547	9.136				0.022	0.036	0.064				
			(LL)	1.687	2.913							5.814	0.018	0.028	0.042
			(HZ)	2.348	3.377							5.634			
	EN → Y0	(LZ)	1.559	2.307	4.328				0.023	0.036	0.064				
			(ZH)	1.706	3.606							9.328	0.022	0.033	0.051
			(ZL)	1.353	2.504							5.120			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BED6	A → Y0	(HH)	1.684	3.547	9.136				0.022	0.036	0.064				
			(LL)	1.687	2.913							5.814	0.018	0.028	0.042
			(HZ)	2.348	3.377							5.634			
	EN → Y0	(LZ)	1.559	2.307	4.328				0.023	0.036	0.064				
			(ZH)	1.706	3.606							9.328	0.022	0.033	0.051
			(ZL)	1.353	2.504							5.120			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BEU6	A → Y0	(HH)	1.684	3.547	9.136				0.022	0.036	0.064				
			(LL)	1.687	2.913							5.814	0.018	0.028	0.042
			(HZ)	2.348	3.377							5.634			
	EN → Y0	(LZ)	1.559	2.307	4.328				0.023	0.036	0.064				
			(ZH)	1.706	3.606							9.328	0.022	0.033	0.051
			(ZL)	1.353	2.504							5.120			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BEW6	A → Y0	(HH)	1.684	3.547	9.136				0.022	0.036	0.064				
			(LL)	1.687	2.913							5.814	0.018	0.028	0.042
			(HZ)	2.348	3.377							5.634			
	EN → Y0	(LZ)	1.559	2.307	4.328				0.023	0.036	0.064				
			(ZH)	1.706	3.606							9.328	0.022	0.033	0.051
			(ZL)	1.353	2.504							5.120			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			
BE0G	A → Y0	(HH)	1.883	4.029	10.615				0.021	0.035	0.065				
			(LL)	1.997	3.484							7.016	0.015	0.023	0.035
			(HZ)	3.006	4.371							7.283			
	EN → Y0	(LZ)	1.877	2.777	5.195				0.022	0.035	0.064				
			(ZH)	1.867	4.086							10.808	0.020	0.030	0.047
			(ZL)	1.424	2.718							5.634			
	Y0 → Y1	(HH)	0.115	0.215	0.422	0.015	0.021	0.031							
			(LL)	0.240	0.366	0.699	0.008	0.010				0.015			
			(LZ)	0.240	0.366	0.699	0.008	0.010				0.015			

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BEDG	A → Y0	(HH)	1.883	4.029	10.615				0.021	0.035	0.065
		(LL)	1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)	3.006	4.371	7.283						
		(LZ)	1.877	2.777	5.195						
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064
	Y0 → Y1	(ZL)	1.424	2.718	5.634				0.020	0.030	0.047
		(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
	BEUG	A → Y0	(HH)	1.883	4.029	10.615				0.021	0.035
(LL)			1.997	3.484	7.016				0.015	0.023	0.035
EN → Y0		(HZ)	3.006	4.371	7.283						
		(LZ)	1.877	2.777	5.195						
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064
Y0 → Y1		(ZL)	1.424	2.718	5.634				0.020	0.030	0.047
		(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			
BEWG		A → Y0	(HH)	1.883	4.029	10.615				0.021	0.035
	(LL)		1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)	3.006	4.371	7.283						
		(LZ)	1.877	2.777	5.195						
		(ZH)	1.867	4.086	10.808				0.022	0.035	0.064
	Y0 → Y1	(ZL)	1.424	2.718	5.634				0.020	0.030	0.047
		(HH)	0.115	0.215	0.422	0.015	0.021	0.031			
		(LL)	0.240	0.366	0.699	0.008	0.010	0.015			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Schmitt I/O Buffer					TTL 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BSIVW	BSDVW	BSUVW	BSWVW	1	13	
6mA	BSIDW	BSDDW	BSUDW	BSWDW	1	13	
9mA	BSI4W	BSD4W	BSU4W	BSW4W	1	13	
12mA	BSI2W	BSD2W	BSU2W	BSW2W	1	23	
18mA	BSI6W	BSD6W	BSU6W	BSW6W	1	23	
24mA	BSIGW	BSDGW	BSUGW	BSWGW	1	23	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			BSIVW to BSWVW	A	6.3
BSIDW to BSWDW	A	6.3	Y1	19	
BSI4W to BSW4W	A	6.3	Y1	19	
BSI2W to BSW2W	A	16.9	Y1	19	
BSI6W to BSW6W	A	16.9	Y1	19	
BSIGW to BSWGW	A	16.9	Y1	19	

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X: Irrelevant  
Z: High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BSIVW	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
				0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	(LZ)	1.259	1.846	3.271				0.056	0.078	0.114	
				0.469	0.771	1.492							0.090
	Y0 → Y1	(ZH)	(ZL)	1.149	2.002	4.411	0.010	0.016	0.024	0.010	0.016	0.024	0.030
				1.074	1.852	3.792							
BSDVW	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
				0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	(LZ)	1.259	1.846	3.271				0.056	0.078	0.114	
				0.469	0.771	1.492							0.090
	Y0 → Y1	(ZH)	(ZL)	1.149	2.002	4.411	0.010	0.016	0.024	0.010	0.016	0.024	0.030
				1.074	1.852	3.792							
BSUVW	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
				0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	(LZ)	1.259	1.846	3.271				0.056	0.078	0.114	
				0.469	0.771	1.492							0.090
	Y0 → Y1	(ZH)	(ZL)	1.149	2.002	4.411	0.010	0.016	0.024	0.010	0.016	0.024	0.030
				1.074	1.852	3.792							
BSWVW	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114	
				0.963	1.638	3.333				0.089	0.131	0.192	
	EN → Y0	(HZ)	(LZ)	1.259	1.846	3.271				0.056	0.078	0.114	
				0.469	0.771	1.492							0.090
	Y0 → Y1	(ZH)	(ZL)	1.149	2.002	4.411	0.010	0.016	0.024	0.010	0.016	0.024	0.030
				1.074	1.852	3.792							
BSIDW	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
				0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	(LZ)	1.602	2.366	4.209				0.038	0.053	0.080	
				0.547	0.906	1.819							0.045
	Y0 → Y1	(ZH)	(ZL)	1.164	2.076	4.626	0.010	0.016	0.024	0.010	0.016	0.024	0.030
				0.931	1.622	3.317							
BSDDW	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
				0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	(LZ)	1.602	2.366	4.209				0.038	0.053	0.080	
				0.547	0.906	1.819							0.045
	Y0 → Y1	(ZH)	(ZL)	1.164	2.076	4.626	0.010	0.016	0.024	0.010	0.016	0.024	0.030
				0.931	1.622	3.317							
BSUDW	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080	
				0.857	1.450	2.908				0.044	0.065	0.097	
	EN → Y0	(HZ)	(LZ)	1.602	2.366	4.209				0.038	0.053	0.080	
				0.547	0.906	1.819							0.045
	Y0 → Y1	(ZH)	(ZL)	1.164	2.076	4.626	0.010	0.016	0.024	0.010	0.016	0.024	0.030
				0.931	1.622	3.317							

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSWDW	A → Y0	(HH)		0.857	1.549	3.541				0.038	0.053	0.080
		(LL)		0.857	1.450	2.908				0.044	0.065	0.097
		(LZ)		0.547	0.906	1.819						
	EN → Y0	(HZ)		1.602	2.366	4.209				0.038	0.053	0.080
		(ZH)		1.164	2.076	4.626				0.045	0.066	0.098
		(ZL)		0.931	1.622	3.317						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.607	1.003	2.005						
BSI4W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
		(LZ)		0.607	1.003	2.005						
	EN → Y0	(HZ)		2.160	3.204	5.612				0.024	0.035	0.056
		(ZH)		1.232	2.276	5.174				0.031	0.045	0.067
		(ZL)		0.913	1.619	3.323						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.607	1.003	2.005						
BSD4W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
		(LZ)		0.607	1.003	2.005						
	EN → Y0	(HZ)		2.160	3.204	5.612				0.024	0.035	0.056
		(ZH)		1.232	2.276	5.174				0.031	0.045	0.067
		(ZL)		0.913	1.619	3.323						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.607	1.003	2.005						
BSU4W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
		(LZ)		0.607	1.003	2.005						
	EN → Y0	(HZ)		2.160	3.204	5.612				0.024	0.035	0.056
		(ZH)		1.232	2.276	5.174				0.031	0.045	0.067
		(ZL)		0.913	1.619	3.323						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.607	1.003	2.005						
BSW4W	A → Y0	(HH)		0.927	1.751	4.088				0.024	0.036	0.056
		(LL)		0.979	1.652	3.277				0.029	0.043	0.064
		(LZ)		0.607	1.003	2.005						
	EN → Y0	(HZ)		2.160	3.204	5.612				0.024	0.035	0.056
		(ZH)		1.232	2.276	5.174				0.031	0.045	0.067
		(ZL)		0.913	1.619	3.323						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.607	1.003	2.005						
BSI2W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
		(LZ)		0.770	1.362	2.783						
	EN → Y0	(HZ)		1.929	3.060	5.656				0.020	0.029	0.045
		(ZH)		1.247	2.257	4.957				0.023	0.034	0.050
		(ZL)		0.831	1.483	3.091						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.770	1.362	2.783						
BSD2W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
		(LZ)		0.770	1.362	2.783						
	EN → Y0	(HZ)		1.929	3.060	5.656				0.020	0.029	0.045
		(ZH)		1.247	2.257	4.957				0.023	0.034	0.050
		(ZL)		0.831	1.483	3.091						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.770	1.362	2.783						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSU2W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
		(LZ)		0.770	1.362	2.783						
	EN → Y0	(HZ)		1.929	3.060	5.656				0.020	0.029	0.045
		(ZH)		1.247	2.257	4.957				0.023	0.034	0.050
		(ZL)		0.831	1.483	3.091						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.770	1.362	2.783						
BSW2W	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
		(LZ)		0.770	1.362	2.783						
	EN → Y0	(HZ)		1.929	3.060	5.656				0.020	0.029	0.045
		(ZH)		1.247	2.257	4.957				0.023	0.034	0.050
		(ZL)		0.831	1.483	3.091						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.770	1.362	2.783						
BSI6W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
		(LZ)		0.858	1.497	3.031						
	EN → Y0	(HZ)		2.463	3.879	7.031				0.015	0.023	0.038
		(ZH)		1.317	2.435	5.418				0.017	0.025	0.037
		(ZL)		0.837	1.526	3.208						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.858	1.497	3.031						
BSD6W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
		(LZ)		0.858	1.497	3.031						
	EN → Y0	(HZ)		2.463	3.879	7.031				0.015	0.023	0.038
		(ZH)		1.317	2.435	5.418				0.017	0.025	0.037
		(ZL)		0.837	1.526	3.208						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.858	1.497	3.031						
BSU6W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
		(LZ)		0.858	1.497	3.031						
	EN → Y0	(HZ)		2.463	3.879	7.031				0.015	0.023	0.038
		(ZH)		1.317	2.435	5.418				0.017	0.025	0.037
		(ZL)		0.837	1.526	3.208						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.858	1.497	3.031						
BSW6W	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
		(LZ)		0.858	1.497	3.031						
	EN → Y0	(HZ)		2.463	3.879	7.031				0.015	0.023	0.038
		(ZH)		1.317	2.435	5.418				0.017	0.025	0.037
		(ZL)		0.837	1.526	3.208						
	Y0 → Y1	(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
		(LZ)		0.858	1.497	3.031						
BSIGW	A → Y0	(HH										

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSDGW	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
		(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
	BSUGW	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021
(LL)				0.881	1.569	3.211				0.012	0.018	0.027
EN → Y0		(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
Y0 → Y1		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
		(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
BSWGW		A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021
	(LL)			0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
	Y0 → Y1	(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
		(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			

[MEMO]

Chapter 1 Interface Block

Chapter 1 Interface Block

Function	Low-noise Schmitt I/O Buffer					TTL 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BF1VW	BFDVW	BFUVW	BFVWW	1	13	
6mA	BF1DW	BFDDW	BFUDW	BFVDW	1	13	
9mA	BF14W	BF44W	BFU4W	BFV4W	1	13	
12mA	BF12W	BF22W	BFU2W	BFV2W	1	13	
18mA	BF16W	BF66W	BFU6W	BFV6W	1	13	
24mA	BF1GW	BF6GW	BFUGW	BFV6GW	1	13	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			BF1VW to BFVWW	A	6.1
EN	4.0				
	BF1DW to BFVDW	A	6.1	Y1	19
	EN	4.0			
	BF14W to BFV4W	A	6.1	Y1	19
	EN	4.0			
	BF12W to BFV2W	A	6.1	Y1	19
	EN	4.0			
	BF16W to BFV6W	A	6.1	Y1	19
	EN	4.0			
	BF1GW to BFV6GW	A	6.1	Y1	19
	EN	4.0			

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X: Irrelevant  
Z: High Impedance

Y0	Y1
0	0
1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BF1VW	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFDDW	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFU4W	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFV4W	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFU2W	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFU6W	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFV2W	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFV6W	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030
BFV6GW	A → Y0	(HH)	(LL)	1.275	2.384	5.623				0.057	0.081	0.121
			(LL)	1.260	2.099	4.212				0.090	0.131	0.194
	EN → Y0	(HZ)	0.785	1.011	1.593							
		(LZ)	0.745	1.089	2.013							
	Y0 → Y1	(ZH)	1.340	2.445	5.805					0.057	0.081	0.121
		(ZL)	1.365	2.279	4.559				0.010	0.016	0.024	0.030

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLD0 (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFWDW	A → Y0	(HH)	(HH)	1.326	2.555	6.105				0.040	0.058	0.090
			(LL)	1.185	1.984	3.930				0.046	0.068	0.101
			(LZ)	0.927	1.364	2.581						
	EN → Y0	(HZ)	(HZ)	1.054	1.423	2.365						
			(ZH)	1.388	2.613	6.285				0.040	0.058	0.090
			(ZL)	1.265	2.149	4.276				0.047	0.068	0.101
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
			(LZ)	0.927	1.364	2.581						
BFI4W	A → Y0	(HH)	(HH)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
			(LZ)	1.086	1.602	3.023						
	EN → Y0	(HZ)	(HZ)	1.476	2.066	3.447						
			(ZH)	1.485	2.941	7.290				0.028	0.042	0.070
			(ZL)	1.268	2.209	4.413				0.033	0.049	0.073
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
			(LZ)	0.927	1.364	2.581						
BFD4W	A → Y0	(HH)	(HH)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
			(LZ)	1.086	1.602	3.023						
	EN → Y0	(HZ)	(HZ)	1.476	2.066	3.447						
			(ZH)	1.485	2.941	7.290				0.028	0.042	0.070
			(ZL)	1.268	2.209	4.413				0.033	0.049	0.073
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
			(LZ)	0.927	1.364	2.581						
BFU4W	A → Y0	(HH)	(HH)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
			(LZ)	1.086	1.602	3.023						
	EN → Y0	(HZ)	(HZ)	1.476	2.066	3.447						
			(ZH)	1.485	2.941	7.290				0.028	0.042	0.070
			(ZL)	1.268	2.209	4.413				0.033	0.049	0.073
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
			(LZ)	0.927	1.364	2.581						
BFW4W	A → Y0	(HH)	(HH)	1.429	2.884	7.106				0.028	0.042	0.070
			(LL)	1.311	2.202	4.323				0.032	0.047	0.070
			(LZ)	1.086	1.602	3.023						
	EN → Y0	(HZ)	(HZ)	1.476	2.066	3.447						
			(ZH)	1.485	2.941	7.290				0.028	0.042	0.070
			(ZL)	1.268	2.209	4.413				0.033	0.049	0.073
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
			(LZ)	0.927	1.364	2.581						
BFI2W	A → Y0	(HH)	(HH)	1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
			(LZ)	1.242	1.836	3.457						
	EN → Y0	(HZ)	(HZ)	1.692	2.390	3.993						
			(ZH)	1.539	3.109	7.803				0.026	0.039	0.067
			(ZL)	1.288	2.293	4.624				0.027	0.040	0.061
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
			(LZ)	0.927	1.364	2.581						
BFD2W	A → Y0	(HH)	(HH)	1.492	3.051	7.617				0.026	0.039	0.067
			(LL)	1.390	2.366	4.674				0.025	0.037	0.056
			(LZ)	1.242	1.836	3.457						
	EN → Y0	(HZ)	(HZ)	1.692	2.390	3.993						
			(ZH)	1.539	3.109	7.803				0.026	0.039	0.067
			(ZL)	1.288	2.293	4.624				0.027	0.040	0.061
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024			
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030			
			(LZ)	0.927	1.364	2.581						

Chapter 1 Interface Block

Block type	Switching speed														
	Path			tLD0 (ns)			t 1			T					
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
BFU2W	A → Y0	(HH)	(HH)	1.492	3.051	7.617						0.026	0.039	0.067	
			(LL)	1.390	2.366	4.674						0.025	0.037	0.056	
			(LZ)	1.242	1.836	3.457									
	EN → Y0	(HZ)	(HZ)	1.692	2.390	3.993							0.026	0.039	0.067
			(ZH)	1.539	3.109	7.803							0.027	0.040	0.061
			(ZL)	1.288	2.293	4.624									
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024						
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030						
			(LZ)	0.927	1.364	2.581									
BFW2W	A → Y0	(HH)	(HH)	1.492	3.051	7.617						0.026	0.039	0.067	
			(LL)	1.390	2.366	4.674						0.025	0.037	0.056	
			(LZ)	1.242	1.836	3.457									
	EN → Y0	(HZ)	(HZ)	1.692	2.390	3.993							0.026	0.039	0.067
			(ZH)	1.539	3.109	7.803							0.027	0.040	0.061
			(ZL)	1.288	2.293	4.624									
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024						
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030						
			(LZ)	0.927	1.364	2.581									
BFI6W	A → Y0	(HH)	(HH)	1.684	3.547	9.136						0.022	0.036	0.064	
			(LL)	1.687	2.913	5.814						0.018	0.028	0.042	
			(LZ)	1.559	2.307	4.328									
	EN → Y0	(HZ)	(HZ)	2.348	3.377	5.634							0.023	0.036	0.064
			(ZH)	1.706	3.606	9.328						0.022	0.033	0.051	
			(ZL)	1.353	2.504	5.120									
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024						
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030						
			(LZ)	0.927	1.364	2.581									
BFD6W	A → Y0	(HH)	(HH)	1.684	3.547	9.136						0.022	0.036	0.064	
			(LL)	1.687	2.913	5.814						0.018	0.028	0.042	
			(LZ)	1.559	2.307	4.328									
	EN → Y0	(HZ)	(HZ)	2.348	3.377	5.634							0.023	0.036	0.064
			(ZH)	1.706	3.606	9.328						0.022	0.033	0.051	
			(ZL)	1.353	2.504	5.120									
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024						
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030						
			(LZ)	0.927	1.364	2.581									
BFU6W	A → Y0	(HH)	(HH)	1.684	3.547	9.136						0.022	0.036	0.064	
			(LL)	1.687	2.913	5.814						0.018	0.028	0.042	
			(LZ)	1.559	2.307	4.328									
	EN → Y0	(HZ)	(HZ)	2.348	3.377	5.634							0.023	0.036	0.064
			(ZH)	1.706	3.606	9.328						0.022	0.033	0.051	
			(ZL)	1.353	2.504	5.120									
	Y0 → Y1	(HH)	(HH)	0.673	1.029	1.867	0.010	0.016	0.024						
			(LL)	3.005	4.875	8.847	0.014	0.020	0.030						
			(LZ)	0.927	1.364	2.581									
BFW6W	A → Y0	(HH)	(HH)	1.684	3.547	9.136						0.022	0.036	0.064	
			(LL)	1.687	2.913	5.814						0.018	0.028	0.042	
			(LZ)	1.559	2.307	4.328									
	EN → Y0	(HZ)	(HZ)	2.348	3.377	5.634							0.023	0.036	0.064
			(ZH)	1.706	3.606	9.328						0.022			

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t 1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFDGW	A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035	0.065
		(LL)		1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)		3.006	4.371	7.283						
		(LZ)		1.877	2.777	5.195						
		(ZH)		1.867	4.086	10.808				0.022	0.035	0.064
	Y0 → Y1	(ZL)		1.424	2.718	5.634				0.020	0.030	0.047
		(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
	BFUGW	A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035
(LL)				1.997	3.484	7.016				0.015	0.023	0.035
EN → Y0		(HZ)		3.006	4.371	7.283						
		(LZ)		1.877	2.777	5.195						
		(ZH)		1.867	4.086	10.808				0.022	0.035	0.064
Y0 → Y1		(ZL)		1.424	2.718	5.634				0.020	0.030	0.047
		(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			
BFWGW		A → Y0	(HH)		1.883	4.029	10.615				0.021	0.035
	(LL)			1.997	3.484	7.016				0.015	0.023	0.035
	EN → Y0	(HZ)		3.006	4.371	7.283						
		(LZ)		1.877	2.777	5.195						
		(ZH)		1.867	4.086	10.808				0.022	0.035	0.064
	Y0 → Y1	(ZL)		1.424	2.718	5.634				0.020	0.030	0.047
		(HH)		0.673	1.029	1.867	0.010	0.016	0.024			
		(LL)		3.005	4.875	8.847	0.014	0.020	0.030			

[MEMO]

Chapter 1 Interface Block



Chapter 1 Interface Block

Function	I/O Buffer with EN(AND)						TTL 3.3 V
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN2V	BN4V			1	14	
6mA	BN2D	BN4D			1	14	
9mA	BN24	BN44			1	14	
12mA	BN22	BN42			1	24	
18mA	BN26	BN46			1	24	
24mA	BN2G	BN4G			1	24	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
	BN2V to BN4V	A	6.3	Y1	22
	EN	1.0			
	ENI	4.0			
	BN2D to BN4D	A	6.3	Y1	22
	EN	1.0			
	ENI	4.0			
	BN24 to BN44	A	6.3	Y1	22
	EN	1.0			
	ENI	4.0			
	BN22 to BN42	A	16.9	Y1	22
	EN	1.0			
	ENI	4.0			
BN26 to BN46	A	16.9	Y1	22	
EN	1.0				
ENI	4.0				
BN2G to BN4G	A	16.9	Y1	22	
EN	1.0				
ENI	4.0				

Truth Table		
A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	0
1	0	0
1	1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDo (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN2V	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(LZ)	(ZH)	0.469	0.771	1.492				0.056	0.078	0.114
			(ZH)	1.149	2.002	4.411				0.090	0.131	0.193
			(ZL)	1.074	1.852	3.792						
	ENI → Y1	(HH)	(LL)	0.169	0.261	0.554	0.015	0.021	0.031			
			(LL)	0.241	0.353	0.667	0.008	0.010	0.015			
			(LL)	0.129	0.245	0.511	0.015	0.021	0.031			
Y0 → Y1	(HH)	(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
BN4V	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(LZ)	(ZH)	0.469	0.771	1.492				0.056	0.078	0.114
			(ZH)	1.149	2.002	4.411				0.090	0.131	0.193
			(ZL)	1.074	1.852	3.792						
	ENI → Y1	(HH)	(LL)	0.169	0.261	0.554	0.015	0.021	0.031			
			(LL)	0.241	0.353	0.667	0.008	0.010	0.015			
			(LL)	0.129	0.245	0.511	0.015	0.021	0.031			
Y0 → Y1	(HH)	(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
BN2D	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(LZ)	(ZH)	0.547	0.906	1.819				0.038	0.053	0.080
			(ZH)	1.164	2.076	4.626				0.045	0.066	0.098
			(ZL)	0.931	1.622	3.317						
	ENI → Y1	(HH)	(LL)	0.169	0.261	0.554	0.015	0.021	0.031			
			(LL)	0.241	0.353	0.667	0.008	0.010	0.015			
			(LL)	0.129	0.245	0.511	0.015	0.021	0.031			
Y0 → Y1	(HH)	(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
BN4D	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(LZ)	(ZH)	0.547	0.906	1.819				0.038	0.053	0.080
			(ZH)	1.164	2.076	4.626				0.045	0.066	0.098
			(ZL)	0.931	1.622	3.317						
	ENI → Y1	(HH)	(LL)	0.169	0.261	0.554	0.015	0.021	0.031			
			(LL)	0.241	0.353	0.667	0.008	0.010	0.015			
			(LL)	0.129	0.245	0.511	0.015	0.021	0.031			
Y0 → Y1	(HH)	(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
BN24	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(LZ)	(ZH)	0.607	1.003	2.005				0.024	0.035	0.056
			(ZH)	1.232	2.276	5.174				0.031	0.045	0.067
			(ZL)	0.913	1.619	3.323						
	ENI → Y1	(HH)	(LL)	0.169	0.261	0.554	0.015	0.021	0.031			
			(LL)	0.241	0.353	0.667	0.008	0.010	0.015			
			(LL)	0.129	0.245	0.511	0.015	0.021	0.031			
Y0 → Y1	(HH)	(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
		(LL)	0.234	0.347	0.666	0.007	0.010	0.015				
BN44	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(LZ)	(ZH)	0.607	1.003	2.005				0.024	0.035	0.056
			(ZH)	1.232	2.276	5.174				0.031	0.045	0.067
			(ZL)	0.913	1.619	3.323						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
	ENI → Y1	(HH)		0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)		0.241	0.353	0.667	0.008	0.010	0.015			
	Y0 → Y1	(HH)		0.129	0.245	0.511	0.015	0.021	0.031			
BN22	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
	ENI → Y1	(HH)		0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)		0.241	0.353	0.667	0.008	0.010	0.015			
	Y0 → Y1	(HH)		0.129	0.245	0.511	0.015	0.021	0.031			
BN42	A → Y0	(HH)		0.681	1.265	2.923				0.020	0.029	0.045
		(LL)		0.644	1.115	2.283				0.022	0.032	0.048
	EN → Y0	(HZ)		1.929	3.060	5.656						
		(LZ)		0.770	1.362	2.783						
		(ZH)		1.247	2.257	4.957				0.020	0.029	0.045
		(ZL)		0.831	1.483	3.091				0.023	0.034	0.050
	ENI → Y1	(HH)		0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)		0.241	0.353	0.667	0.008	0.010	0.015			
	Y0 → Y1	(HH)		0.129	0.245	0.511	0.015	0.021	0.031			
BN26	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
	ENI → Y1	(HH)		0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)		0.241	0.353	0.667	0.008	0.010	0.015			
	Y0 → Y1	(HH)		0.129	0.245	0.511	0.015	0.021	0.031			
BN46	A → Y0	(HH)		0.754	1.442	3.379				0.015	0.023	0.039
		(LL)		0.761	1.339	2.741				0.015	0.022	0.033
	EN → Y0	(HZ)		2.463	3.879	7.031						
		(LZ)		0.858	1.497	3.031						
		(ZH)		1.317	2.435	5.418				0.015	0.023	0.038
		(ZL)		0.837	1.526	3.208				0.017	0.025	0.037
	ENI → Y1	(HH)		0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)		0.241	0.353	0.667	0.008	0.010	0.015			
	Y0 → Y1	(HH)		0.129	0.245	0.511	0.015	0.021	0.031			
BN2G	A → Y0	(HH)		0.819	1.598	3.790				0.013	0.021	0.037
		(LL)		0.881	1.569	3.211				0.012	0.018	0.027
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
	ENI → Y1	(HH)		0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)		0.241	0.353	0.667	0.008	0.010	0.015			
	Y0 → Y1	(HH)		0.129	0.245	0.511	0.015	0.021	0.031			
		(LL)		0.234	0.347	0.666	0.007	0.010	0.015			

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN4G	A → Y0	(HH)		0.819	1.598	3.790						
		(LL)		0.881	1.569	3.211						
	EN → Y0	(HZ)		3.004	4.704	8.420						
		(LZ)		0.945	1.629	3.274						
		(ZH)		1.377	2.588	5.829				0.013	0.021	0.037
		(ZL)		0.847	1.572	3.332				0.013	0.020	0.031
	ENI → Y1	(HH)		0.169	0.261	0.554	0.015	0.021	0.031			
		(LL)		0.241	0.353	0.667	0.008	0.010	0.015			
	Y0 → Y1	(HH)		0.129	0.245	0.511	0.015	0.021	0.031			
		(LL)		0.234	0.347	0.666	0.007	0.010	0.015			

Chapter 1 Interface Block

Function	I/O Buffer with EN(OR)					TTL 3.3 V	
Block type							
Drivability	no resistor	with 50 K $\Omega$ P/D	with 50 K $\Omega$ P/U	with 5 K $\Omega$ P/U	I/O cells	int. Cells	
1mA							
2mA							
3mA	BN3V	BN5V			1	11	
6mA	BN3D	BN5D			1	11	
9mA	BN34	BN54			1	11	
12mA	BN32	BN52			1	21	
18mA	BN36	BN56			1	21	
24mA	BN3G	BN5G			1	21	

Logic Diagram	Block type	Input		Output	
		Symbol	Fan-in	Symbol	Fan-out
			BN3V to BN5V	A	6.3
	EN	1.0			
		ENI	2.0		
	BN3D to BN5D	A	6.3	Y1	21
		EN	1.0		
		ENI	2.0		
	BN34 to BN54	A	6.3	Y1	21
		EN	1.0		
		ENI	2.0		
	BN32 to BN52	A	16.9	Y1	21
		EN	1.0		
		ENI	2.0		
	BN36 to BN56	A	16.9	Y1	21
		EN	1.0		
		ENI	2.0		
	BN3G to BN5G	A	16.9	Y1	21
		EN	1.0		
		ENI	2.0		

A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant  
Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	1
1	0	1
1	1	1

Chapter 1 Interface Block

Block type	Switching speed											
	Path			tLDO (ns)			t1			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN3V	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(HZ)	(LZ)	0.469	0.771	1.492						
			(ZH)	1.149	2.002	4.411				0.056	0.078	0.114
			(ZL)	1.074	1.852	3.792				0.090	0.131	0.193
	ENI → Y1	(HH)	(LL)	0.215	0.314	0.598	0.015	0.021	0.031			
			(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
			(LL)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0 → Y1	(HH)	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
(LL)			0.839	1.469	3.318				0.056	0.078	0.114	
(LL)			0.963	1.638	3.333				0.089	0.131	0.192	
BN5V	A → Y0	(HH)	(LL)	0.839	1.469	3.318				0.056	0.078	0.114
			(LL)	0.963	1.638	3.333				0.089	0.131	0.192
			(HZ)	1.259	1.846	3.271						
	EN → Y0	(HZ)	(LZ)	0.469	0.771	1.492						
			(ZH)	1.149	2.002	4.411				0.056	0.078	0.114
			(ZL)	1.074	1.852	3.792				0.090	0.131	0.193
	ENI → Y1	(HH)	(LL)	0.215	0.314	0.598	0.015	0.021	0.031			
			(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
			(LL)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0 → Y1	(HH)	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
(LL)			0.839	1.469	3.318				0.056	0.078	0.114	
(LL)			0.963	1.638	3.333				0.089	0.131	0.192	
BN3D	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(HZ)	(LZ)	0.547	0.906	1.819						
			(ZH)	1.164	2.076	4.626				0.038	0.053	0.080
			(ZL)	0.931	1.622	3.317				0.045	0.066	0.098
	ENI → Y1	(HH)	(LL)	0.215	0.314	0.598	0.015	0.021	0.031			
			(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
			(LL)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0 → Y1	(HH)	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
(LL)			0.857	1.549	3.541				0.038	0.053	0.080	
(LL)			0.857	1.450	2.908				0.044	0.065	0.097	
BN5D	A → Y0	(HH)	(LL)	0.857	1.549	3.541				0.038	0.053	0.080
			(LL)	0.857	1.450	2.908				0.044	0.065	0.097
			(HZ)	1.602	2.366	4.209						
	EN → Y0	(HZ)	(LZ)	0.547	0.906	1.819						
			(ZH)	1.164	2.076	4.626				0.038	0.053	0.080
			(ZL)	0.931	1.622	3.317				0.045	0.066	0.098
	ENI → Y1	(HH)	(LL)	0.215	0.314	0.598	0.015	0.021	0.031			
			(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
			(LL)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0 → Y1	(HH)	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
(LL)			0.857	1.549	3.541				0.038	0.053	0.080	
(LL)			0.857	1.450	2.908				0.044	0.065	0.097	
BN34	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(HZ)	(LZ)	0.607	1.003	2.005						
			(ZH)	1.232	2.276	5.174				0.024	0.035	0.056
			(ZL)	0.913	1.619	3.323				0.031	0.045	0.067
	ENI → Y1	(HH)	(LL)	0.215	0.314	0.598	0.015	0.021	0.031			
			(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
			(LL)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0 → Y1	(HH)	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
(LL)			0.927	1.751	4.088				0.024	0.036	0.056	
(LL)			0.979	1.652	3.277				0.029	0.043	0.064	
BN54	A → Y0	(HH)	(LL)	0.927	1.751	4.088				0.024	0.036	0.056
			(LL)	0.979	1.652	3.277				0.029	0.043	0.064
			(HZ)	2.160	3.204	5.612						
	EN → Y0	(HZ)	(LZ)	0.607	1.003	2.005						
			(ZH)	1.232	2.276	5.174				0.024	0.035	0.056
			(ZL)	0.913	1.619	3.323				0.031	0.045	0.067

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	ENI	→	Y1	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
				(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
	Y0	→	Y1	(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
BN32	A	→	Y0	(HH)	0.681	1.265	2.923				0.020	0.029	0.045
				(LL)	0.644	1.115	2.283				0.022	0.032	0.048
				(HZ)	1.929	3.060	5.656						
	EN	→	Y0	(LZ)	0.770	1.362	2.783						
				(ZH)	1.247	2.257	4.957				0.020	0.029	0.045
				(ZL)	0.831	1.483	3.091				0.023	0.034	0.050
	ENI	→	Y1	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
				(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
				(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0	→	Y1	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
BN52	A	→	Y0	(HH)	0.681	1.265	2.923				0.020	0.029	0.045
				(LL)	0.644	1.115	2.283				0.022	0.032	0.048
				(HZ)	1.929	3.060	5.656						
	EN	→	Y0	(LZ)	0.770	1.362	2.783						
				(ZH)	1.247	2.257	4.957				0.020	0.029	0.045
				(ZL)	0.831	1.483	3.091				0.023	0.034	0.050
	ENI	→	Y1	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
				(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
				(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0	→	Y1	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
BN36	A	→	Y0	(HH)	0.754	1.442	3.379				0.015	0.023	0.039
				(LL)	0.761	1.339	2.741				0.015	0.022	0.033
				(HZ)	2.463	3.879	7.031						
	EN	→	Y0	(LZ)	0.858	1.497	3.031						
				(ZH)	1.317	2.435	5.418				0.015	0.023	0.038
				(ZL)	0.837	1.526	3.208				0.017	0.025	0.037
	ENI	→	Y1	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
				(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
				(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0	→	Y1	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
BN56	A	→	Y0	(HH)	0.754	1.442	3.379				0.015	0.023	0.039
				(LL)	0.761	1.339	2.741				0.015	0.022	0.033
				(HZ)	2.463	3.879	7.031						
	EN	→	Y0	(LZ)	0.858	1.497	3.031						
				(ZH)	1.317	2.435	5.418				0.015	0.023	0.038
				(ZL)	0.837	1.526	3.208				0.017	0.025	0.037
	ENI	→	Y1	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
				(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
				(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0	→	Y1	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			
BN3G	A	→	Y0	(HH)	0.819	1.598	3.790				0.013	0.021	0.037
				(LL)	0.881	1.569	3.211				0.012	0.018	0.027
				(HZ)	3.004	4.704	8.420						
	EN	→	Y0	(LZ)	0.945	1.629	3.274						
				(ZH)	1.377	2.588	5.829				0.013	0.021	0.037
				(ZL)	0.847	1.572	3.332				0.013	0.020	0.031
	ENI	→	Y1	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
				(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
				(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0	→	Y1	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BN5G	A	→	Y0	(HH)	0.819	1.598	3.790						
				(LL)	0.881	1.569	3.211						
				(HZ)	3.004	4.704	8.420						
	EN	→	Y0	(LZ)	0.945	1.629	3.274						
				(ZH)	1.377	2.588	5.829				0.013	0.021	0.037
				(ZL)	0.847	1.572	3.332				0.013	0.020	0.031
	ENI	→	Y1	(HH)	0.215	0.314	0.598	0.015	0.021	0.031			
				(LL)	0.302	0.519	1.097	0.008	0.011	0.017			
				(HH)	0.124	0.218	0.433	0.015	0.021	0.031			
	Y0	→	Y1	(LL)	0.322	0.468	0.960	0.008	0.011	0.017			

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## 1.3 Oscillator

Chapter 1 Interface Block

Function	Oscillator Input Buffer										
Block type											
Function				I/O cells	int. cells						
Normal	OSI1			1	0						
Oscillation stop function											
-											
Logic Diagram		Input		Output							
		Block type	Symbol	Fan-in	Symbol	Fan-out					
		OSI1	XT1	-	O	10					
Truth Table											
<table border="1"> <thead> <tr> <th>XT1</th> <th>O</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </tbody> </table>						XT1	O	0	0	1	1
XT1	O										
0	0										
1	1										

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI1	XT1 → O	(HH) (LL)	0.010 0.010	0.010 0.010	0.010 0.010	0.001 0.001	0.001 0.001	0.001 0.001			

Chapter 1 Interface Block

Function	Oscillator Input Buffer for Enable					
Block type						
Function				I/O cells	int. cells	
Normal						
Oscillation stop function	OSI2			1	0	
-						
Logic Diagram		Block type	Input		Output	
		OSI2	Symbol	Fan-in	Symbol	Fan-out
		XT1	-	O	10	
		EN	3.0			
Truth Table						
	XT1	EN	O			
	0	0	0			
	1	0	1			
	1	1	1			
	0	1	X	← Prohibition		
X:Irrelevant						

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI2	XT1 → O	(HH) (LL)	0.010 0.010	0.010 0.010	0.010 0.010	0.001 0.001	0.001 0.001	0.001 0.001			



Chapter 1 Interface Block

Function	Oscillator Input Buffer for OSO9										
Block type											
Function				I/O cells	int. cells						
Normal	OSI4			1	0						
Oscillation stop function											
-											
Logic Diagram	Block type		Input		Output						
			Symbol	Fan-in	Symbol	Fan-out					
	OSI4		XT1	-	O	10					
Truth Table											
<table border="1"> <tr> <td>XT1</td> <td>O</td> </tr> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </table>						XT1	O	0	0	1	1
XT1	O										
0	0										
1	1										

Chapter 1 Interface Block

Block type	Switching speed										
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI4	XT1 → O	(HH) (LL)	0.010 0.010	0.010 0.010	0.010 0.010	0.001 0.001	0.001 0.001	0.001 0.001			

Chapter 1 Interface Block

Function	Oscillator Output Buffer (Internal Feedback Resistor)													
Block type														
Function	MHz range	kHz range		I/O cells	int. cells									
External feedback Resistor														
Internal feedback Resistor	oso1			1	0									
Internal feedback Resistor Oscillation stop function														
Logic Diagram		Input		Output										
		Block type	Symbol	Fan-in	Symbol	Fan-out								
		OSO1	I1	1.0	XT2 O2	- 33								
		Truth Table												
<table border="1"> <thead> <tr> <th>I1</th> <th>XT2</th> <th>O2</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> </tbody> </table>						I1	XT2	O2	0	1	1	1	0	0
I1	XT2	O2												
0	1	1												
1	0	0												

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
OSO1	I1	→	XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
				(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1	→	O2	(HL)	9.737	21.997	21.997	0.010	0.022	0.022			
				(LH)	6.164	13.299	13.299	0.011	0.020	0.020			

Chapter 1 Interface Block

Function	Oscillator Output Buffer (for Enable Type)																								
Block type																									
Function	MHz range	kHz range		I/O cells	int. cells																				
External feedback Resistor																									
Internal feedback Resistor																									
Internal feedback Resistor Oscillation stop function	OSO7			1	0																				
Logic Diagram	Block type		Input		Output																				
			Symbol	Fan-in	Symbol	Fan-out																			
	OSO7		I1	1.0	XT2	-																			
		EN	3.0	O2	33																				
Truth Table																									
<table border="1"> <thead> <tr> <th>I1</th> <th>EN</th> <th>XT2</th> <th>O2</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>X</td> <td>X</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>						I1	EN	XT2	O2	0	0	1	1	1	0	0	0	1	1	0	0	0	1	X	X
I1	EN	XT2	O2																						
0	0	1	1																						
1	0	0	0																						
1	1	0	0																						
0	1	X	X																						

Chapter 1 Interface Block

Block type	Switching speed											
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSO7	I1	→	XT2 (HL)	0.010	0.010	0.010				0.001	0.001	0.001
			(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1	→	O2 (HL)	9.737	21.997	21.997	0.010	0.022	0.022			
			(LH)	6.164	13.299	13.299	0.011	0.020	0.020			

Chapter 1 Interface Block

Function	Oscillator Output Buffer (External Feedback Resistor)					
Block type						
Function	MHz range	kHz range		I/O cells	int. cells	
External feedback Resistor	OSO9			1	0	
Internal feedback Resistor						
Internal feedback Resistor Oscillation stop function						
Logic Diagram		Input		Output		
		Block type				
		Symbol	Fan-in	Symbol	Fan-out	
		OSO9	I1 1.0	XT2 O2	- 33	
Truth Table						
I1	XT2	O2				
0	1	1				
1	0	0				

Chapter 1 Interface Block

Block type	Switching speed												
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			T			
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
OSO9	I1	→	XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
				(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1	→	O2	(HL)	9.737	21.997	21.997	0.010	0.022	0.022			
				(LH)	6.164	13.299	13.299	0.011	0.020	0.020			

# **Chapter 2**

## **Function Block**

[MEMO]

## 2.1 Level Generator

Chapter 2 Function Block

Function	H, L Level Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
-	F091	1								
-										
-										
-										

Logic Diagram

```

graph LR
    subgraph Block
        direction TB
        N01[N01 H]
        N02[N02 L]
    end
  
```

Truth Table

H	L
1	0

Chapter 2 Function Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			H	142
F091												L	142

[MEMO]

[MEMO]



## 2.2 Inverter, Buffer, CTS Driver, Delay Gate

[MEMO]

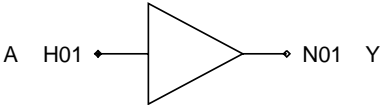
Chapter 2 Function Block

Function	Inverter											
Block type	Single output type						Multi output type					
	Name	cells					Name	cells				
Low Power	L101	1										
x1	F101	1										
x2	F102	2										
x3	F143	3										
x4	F144	4										
x5	F145	5										
x6	F146	6										
x8	F148	12										
x12												
Logic Diagram for "Single output type"												
Logic Diagram for "Multi output type 1"												
Logic Diagram for "Multi output type 2"												

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L101	A	→	Y	(HL) 0.105 (LH) 0.088	0.133 0.130	0.204 0.226	0.022 0.028	0.029 0.042	0.041 0.061	A	1.0	Y	10
F101	A	→	Y	(HL) 0.077 (LH) 0.061	0.101 0.095	0.155 0.166	0.011 0.015	0.015 0.021	0.021 0.031	A	2.1	Y	22
F102	A	→	Y	(HL) 0.074 (LH) 0.060	0.099 0.093	0.154 0.164	0.006 0.007	0.007 0.010	0.010 0.015	A	4.1	Y	45
F143	A	→	Y	(HL) 0.077 (LH) 0.062	0.102 0.096	0.157 0.168	0.004 0.005	0.005 0.007	0.007 0.010	A	6.2	Y	68
F144	A	→	Y	(HL) 0.075 (LH) 0.062	0.100 0.095	0.156 0.167	0.003 0.004	0.004 0.005	0.005 0.008	A	8.2	Y	92
F145	A	→	Y	(HL) 0.077 (LH) 0.062	0.101 0.096	0.157 0.169	0.002 0.003	0.003 0.004	0.004 0.006	A	10.3	Y	113
F146	A	→	Y	(HL) 0.075 (LH) 0.062	0.100 0.095	0.156 0.168	0.002 0.002	0.002 0.004	0.003 0.005	A	12.4	Y	137
F148	A	→	Y	(HL) 0.274 (LH) 0.239	0.485 0.426	0.979 0.872	0.002 0.002	0.002 0.003	0.003 0.004	A	4.1	Y	178

Chapter 2 Function Block

Function	Buffer											
Block type	Single output type						Multi output type					
	Name	cells					Name	cells				
Low Power	L111	1										
x1	F111	2										
x2	F112	3										
x3	F153	4										
x4	F154	5										
x5												
x6												
x8	F158	11										
x12												
Logic Diagram for "Single output type"												
 <pre> graph LR     A[H01] --&gt; B[ ]     B --&gt; N01[Y]     style B fill:none,stroke:none             </pre>												
Logic Diagram for "Multi output type 1"												
Logic Diagram for "Multi output type 2"												

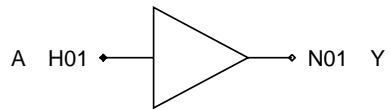
Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L111	A	→	Y	(HH) 0.172	(LL) 0.178	0.261 0.284	0.489 0.550	0.029 0.022	0.042 0.029	0.061 0.043	A	1.0	Y	10
F111	A	→	Y	(HH) 0.120	(LL) 0.126	0.194 0.215	0.363 0.412	0.015 0.011	0.021 0.015	0.031 0.021	A	2.1	Y	23
F112	A	→	Y	(HH) 0.151	(LL) 0.163	0.240 0.278	0.442 0.537	0.007 0.006	0.011 0.008	0.016 0.011	A	2.1	Y	45
F153	A	→	Y	(HH) 0.179	(LL) 0.197	0.282 0.339	0.523 0.665	0.005 0.004	0.007 0.005	0.011 0.008	A	2.1	Y	67
F154	A	→	Y	(HH) 0.203	(LL) 0.226	0.317 0.392	0.593 0.776	0.004 0.003	0.005 0.004	0.008 0.006	A	2.1	Y	89
F158	A	→	Y	(HH) 0.175	(LL) 0.188	0.272 0.320	0.498 0.621	0.002 0.001	0.003 0.002	0.004 0.003	A	6.2	Y	181

Chapter 2 Function Block

Function	CTS Driver (Inverter Type)										
Block type	Single type (Small scale circuit)			Standard type (Middle scale circuit)			Double type (Large scale circuit)				
	Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
x1	FC42	80				FC44	340				
x2	FC82	396				FC84	1020				
x3											
x4											
x5											
-											
-											
-											

Logic Diagram



Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
FC42	A	→	Y	(HH)	0.584	0.947	1.832	0.000	0.001	0.001	A	8.2	Y	1109
				(LL)	0.745	1.372	2.735	0.001	0.001	0.001				
FC82	A	→	Y	(HH)	0.769	1.369	2.822	0.000	0.000	0.000	A	4.1	Y	5230
				(LL)	0.843	1.545	3.189	0.000	0.000	0.000				
FC44	A	→	Y	(HH)	0.594	1.010	2.004	0.000	0.000	0.000	A	8.3	Y	4782
				(LL)	0.611	1.090	2.203	0.000	0.000	0.000				
FC84	A	→	Y	(HH)	1.048	1.947	4.162	0.000	0.000	0.000	A	4.1	Y	10353
				(LL)	1.046	1.956	4.195	0.000	0.000	0.000				

Chapter 2 Function Block

Function	Delay Gate									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
-	F131	6								
-	F132	10								
-										
-										

Logic Diagram



Truth Table

A	Y
0	0
1	1

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F131	A	→	Y	(HH) 1.285	(LL) 2.397	5.345	0.016	0.024	0.037	A	1.0	Y	18
F132	A	→	Y	(HH) 2.547	(LL) 4.809	10.970	0.016	0.024	0.037	A	1.0	Y	18

[MEMO]

[MEMO]

## 2.3 OR(NOR)

[MEMO]

Chapter 2 Function Block

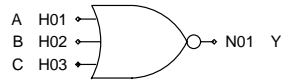
Function	2-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L202	1									
x1	F202	2									
x2	F222	4									
x4	F282	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L202	A	→	Y (HL)	0.098	0.134	0.209	0.022	0.029	0.041	A	1.0	Y	5
			(LH)	0.108	0.170	0.340	0.051	0.078	0.116				
	B	→	Y (HL)	0.112	0.152	0.235	0.022	0.029	0.041	B	1.0		
			(LH)	0.096	0.182	0.398	0.052	0.078	0.116				
F202	A	→	Y (HL)	0.104	0.143	0.223	0.011	0.014	0.021	A	2.1	Y	10
			(LH)	0.104	0.180	0.375	0.026	0.039	0.058				
	B	→	Y (HL)	0.104	0.143	0.223	0.011	0.014	0.021	B	2.1		
			(LH)	0.104	0.180	0.375	0.026	0.039	0.058				
F222	A	→	Y (HL)	0.103	0.145	0.226	0.006	0.007	0.010	A	4.2	Y	20
			(LH)	0.111	0.188	0.384	0.013	0.020	0.029				
	B	→	Y (HL)	0.103	0.145	0.226	0.006	0.007	0.010	B	4.2		
			(LH)	0.111	0.188	0.384	0.013	0.020	0.029				
F282	A	→	Y (HL)	0.327	0.569	1.140	0.003	0.004	0.006	A	1.0	Y	88
			(LH)	0.392	0.713	1.537	0.004	0.005	0.008				
	B	→	Y (HL)	0.342	0.588	1.179	0.003	0.004	0.006	B	1.0		
			(LH)	0.379	0.725	1.595	0.004	0.005	0.008				



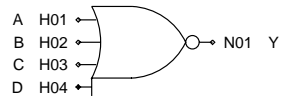
Chapter 2 Function Block

Function	3-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F203	3									
x2	F223	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F203	A	→	Y	(HL)	0.105	0.143	0.220	0.012	0.015	0.022	A B C	2.1 2.1 2.1	Y	5
				(LH)	0.151	0.254	0.558	0.040	0.060	0.089				
	B	→	Y	(HL)	0.117	0.160	0.246	0.012	0.015	0.022				
				(LH)	0.174	0.320	0.701	0.040	0.060	0.089				
	C	→	Y	(HL)	0.105	0.143	0.220	0.012	0.015	0.022				
				(LH)	0.152	0.256	0.560	0.040	0.060	0.090				
F223	A	→	Y	(HL)	0.125	0.166	0.262	0.006	0.007	0.011	A B C	4.3 4.2 4.3	Y	7
				(LH)	0.218	0.355	0.768	0.021	0.031	0.046				
	B	→	Y	(HL)	0.129	0.173	0.277	0.006	0.007	0.010				
				(LH)	0.207	0.341	0.772	0.021	0.031	0.045				
	C	→	Y	(HL)	0.125	0.166	0.262	0.006	0.007	0.011				
				(LH)	0.218	0.355	0.768	0.021	0.031	0.046				

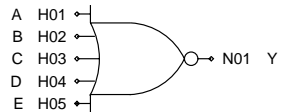
Chapter 2 Function Block

Function	4-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F204	4									
x2											
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F204	A	→	Y	(HL)	0.266	0.451	0.904	0.011	0.015	0.023	A	1.0	Y	21
				(LH)	0.356	0.642	1.442	0.015	0.022	0.033	B	1.0		
	B	→	Y	(HL)	0.282	0.472	0.940	0.011	0.015	0.023	C	1.0		
				(LH)	0.344	0.653	1.501	0.015	0.022	0.033	D	1.0		
	C	→	Y	(HL)	0.295	0.489	0.972	0.011	0.015	0.023				
				(LH)	0.346	0.611	1.370	0.015	0.022	0.033				
	D	→	Y	(HL)	0.311	0.510	1.009	0.011	0.015	0.023				
				(LH)	0.333	0.622	1.429	0.015	0.022	0.033				

Chapter 2 Function Block

5-Input NOR											
Function											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L205	4									
x1	F205	5									
x2	F225	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L205	A → Y	(HL)		0.251	0.417	0.834	0.022	0.029	0.043	A	1.0	Y	10
		(LH)		0.339	0.595	1.336	0.029	0.043	0.063				
	B → Y	(HL)		0.268	0.437	0.870	0.022	0.029	0.043	B	1.0		
		(LH)		0.326	0.606	1.395	0.029	0.043	0.063				
	C → Y	(HL)		0.308	0.480	0.953	0.022	0.029	0.043	C	1.0		
		(LH)		0.468	0.765	1.729	0.029	0.043	0.063				
	D → Y	(HL)		0.323	0.501	0.993	0.022	0.029	0.043	D	1.0		
		(LH)		0.484	0.830	1.890	0.029	0.043	0.063				
	E → Y	(HL)		0.337	0.520	1.033	0.022	0.029	0.043	E	1.0		
		(LH)		0.516	0.918	2.037	0.029	0.043	0.063				
F205	A → Y	(HL)		0.268	0.455	0.909	0.011	0.015	0.023	A	1.0	Y	21
		(LH)		0.355	0.640	1.440	0.015	0.022	0.033				
	B → Y	(HL)		0.284	0.476	0.945	0.011	0.015	0.023	B	1.0		
		(LH)		0.343	0.651	1.499	0.015	0.022	0.033				
	C → Y	(HL)		0.321	0.516	1.025	0.011	0.015	0.023	C	1.0		
		(LH)		0.480	0.802	1.823	0.015	0.022	0.033				
	D → Y	(HL)		0.336	0.537	1.066	0.011	0.015	0.023	D	1.0		
		(LH)		0.495	0.867	1.984	0.015	0.022	0.033				
	E → Y	(HL)		0.349	0.557	1.110	0.011	0.015	0.023	E	1.0		
		(LH)		0.526	0.954	2.130	0.015	0.022	0.033				
F225	A → Y	(HL)		0.321	0.561	1.131	0.006	0.008	0.012	A	1.0	Y	40
		(LH)		0.418	0.767	1.736	0.007	0.011	0.017				
	B → Y	(HL)		0.337	0.581	1.169	0.006	0.008	0.012	B	1.0		
		(LH)		0.405	0.778	1.795	0.007	0.011	0.017				
	C → Y	(HL)		0.372	0.618	1.246	0.006	0.008	0.012	C	1.0		
		(LH)		0.541	0.928	2.124	0.007	0.011	0.017				
	D → Y	(HL)		0.387	0.640	1.288	0.006	0.008	0.012	D	1.0		
		(LH)		0.556	0.992	2.285	0.007	0.011	0.017				
	E → Y	(HL)		0.402	0.662	1.337	0.006	0.008	0.012	E	1.0		
		(LH)		0.588	1.080	2.430	0.007	0.011	0.017				

Chapter 2 Function Block

Function	6-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F206	5									
x2	F226	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
F206	A → Y	(HL)		0.290	0.476	0.956	0.011	0.015	0.023	A	1.0	Y	21		
		(LH)		0.503	0.860	1.971	0.015	0.022	0.033						
	B → Y	(HL)		0.305	0.498	0.996	0.011	0.015	0.023					B	1.0
		(LH)		0.519	0.925	2.131	0.015	0.022	0.033						
	C → Y	(HL)		0.319	0.515	1.036	0.011	0.015	0.023					C	1.0
		(LH)		0.551	1.013	2.277	0.015	0.022	0.033						
	D → Y	(HL)		0.320	0.513	1.021	0.011	0.015	0.023	D	1.0				
		(LH)		0.486	0.814	1.840	0.015	0.022	0.033						
	E → Y	(HL)		0.335	0.534	1.062	0.011	0.015	0.023	E	1.0				
		(LH)		0.502	0.878	2.000	0.015	0.022	0.033						
	F → Y	(HL)		0.348	0.554	1.106	0.011	0.015	0.023	F	1.0				
		(LH)		0.536	0.968	2.150	0.015	0.022	0.033						
F226	A → Y	(HL)		0.355	0.599	1.206	0.006	0.008	0.012	A	1.0	Y	40		
		(LH)		0.582	1.016	2.325	0.007	0.011	0.017						
	B → Y	(HL)		0.370	0.620	1.245	0.006	0.008	0.012					B	1.0
		(LH)		0.598	1.080	2.486	0.007	0.011	0.017						
	C → Y	(HL)		0.385	0.642	1.295	0.006	0.008	0.012					C	1.0
		(LH)		0.630	1.168	2.632	0.007	0.011	0.017						
	D → Y	(HL)		0.380	0.629	1.262	0.006	0.008	0.012	D	1.0				
		(LH)		0.543	0.932	2.135	0.007	0.011	0.017						
	E → Y	(HL)		0.394	0.651	1.304	0.006	0.008	0.012	E	1.0				
		(LH)		0.559	0.998	2.296	0.007	0.011	0.017						
	F → Y	(HL)		0.409	0.674	1.355	0.006	0.008	0.012	F	1.0				
		(LH)		0.593	1.088	2.447	0.007	0.011	0.017						

Chapter 2 Function Block

Function	8-Input NOR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L208	7									
x1	F208	7									
x2	F228	8									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L208	A → Y	(HL)		0.278	0.470	0.939	0.022	0.030	0.044	A	1.0	Y	9
		(LH)		0.439	0.815	1.906	0.030	0.045	0.071				
	B → Y	(HL)		0.295	0.491	0.976	0.022	0.030	0.044	B	1.0		
		(LH)		0.427	0.828	1.965	0.030	0.045	0.071				
	C → Y	(HL)		0.309	0.507	1.006	0.022	0.030	0.044	C	1.0		
		(LH)		0.457	0.833	1.959	0.030	0.046	0.071				
	D → Y	(HL)		0.325	0.528	1.044	0.022	0.030	0.044	D	1.0		
		(LH)		0.445	0.845	2.019	0.030	0.046	0.071				
	E → Y	(HL)		0.358	0.562	1.106	0.023	0.030	0.045	E	1.0		
		(LH)		0.508	0.883	2.089	0.030	0.046	0.071				
	F → Y	(HL)		0.374	0.582	1.143	0.023	0.030	0.045	F	1.0		
		(LH)		0.495	0.896	2.148	0.030	0.046	0.071				
	G → Y	(HL)		0.375	0.582	1.135	0.023	0.031	0.046	G	1.0		
		(LH)		0.518	0.891	2.093	0.030	0.046	0.071				
	H → Y	(HL)		0.391	0.603	1.173	0.023	0.031	0.046	H	1.0		
		(LH)		0.506	0.904	2.152	0.030	0.046	0.071				
F208	A → Y	(HL)		0.281	0.488	0.982	0.011	0.015	0.023	A	1.0	Y	19
		(LH)		0.452	0.868	2.066	0.016	0.024	0.037				
	B → Y	(HL)		0.297	0.509	1.019	0.011	0.015	0.023	B	1.0		
		(LH)		0.440	0.879	2.125	0.016	0.024	0.037				
	C → Y	(HL)		0.310	0.525	1.049	0.011	0.015	0.023	C	1.0		
		(LH)		0.471	0.888	2.125	0.016	0.024	0.037				
	D → Y	(HL)		0.326	0.546	1.087	0.011	0.015	0.023	D	1.0		
		(LH)		0.459	0.899	2.185	0.016	0.024	0.037				
	E → Y	(HL)		0.358	0.581	1.151	0.012	0.016	0.024	E	1.0		
		(LH)		0.524	0.940	2.257	0.016	0.024	0.037				
	F → Y	(HL)		0.374	0.602	1.189	0.012	0.016	0.024	F	1.0		
		(LH)		0.511	0.952	2.316	0.016	0.024	0.037				
	G → Y	(HL)		0.374	0.600	1.180	0.012	0.016	0.024	G	1.0		
		(LH)		0.533	0.946	2.257	0.016	0.024	0.037				
	H → Y	(HL)		0.389	0.621	1.218	0.012	0.016	0.024	H	1.0		
		(LH)		0.520	0.957	2.317	0.016	0.024	0.037				
F228	A → Y	(HL)		0.342	0.600	1.212	0.006	0.008	0.013	A	1.0	Y	32
		(LH)		0.566	1.101	2.644	0.008	0.012	0.020				
	B → Y	(HL)		0.358	0.621	1.251	0.006	0.008	0.013	B	1.0		
		(LH)		0.554	1.113	2.703	0.008	0.012	0.020				
	C → Y	(HL)		0.366	0.631	1.272	0.006	0.008	0.013	C	1.0		
		(LH)		0.575	1.106	2.682	0.008	0.012	0.020				
	D → Y	(HL)		0.381	0.652	1.312	0.006	0.008	0.013	D	1.0		
		(LH)		0.562	1.118	2.742	0.008	0.012	0.020				
	E → Y	(HL)		0.418	0.693	1.386	0.006	0.008	0.013	E	1.0		
		(LH)		0.633	1.167	2.826	0.008	0.012	0.020				
	F → Y	(HL)		0.433	0.714	1.424	0.006	0.008	0.013	F	1.0		
		(LH)		0.619	1.179	2.886	0.008	0.012	0.020				
	G → Y	(HL)		0.434	0.715	1.420	0.006	0.008	0.013	G	1.0		
		(LH)		0.639	1.169	2.821	0.008	0.012	0.020				
	H → Y	(HL)		0.449	0.736	1.459	0.006	0.008	0.013	H	1.0		
		(LH)		0.626	1.180	2.881	0.008	0.012	0.020				

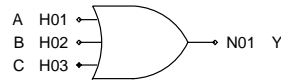
Chapter 2 Function Block

Function	2-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L212	2									
x1	F212	2									
x2	F232	3									
x4	F252	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L212	A	→	Y (HH)	0.164	0.263	0.496	0.029	0.042	0.061	A	1.0	Y	10
			(LL)	0.239	0.398	0.825	0.023	0.031	0.047				
	B	→	Y (HH)	0.181	0.283	0.531	0.028	0.042	0.061	B	1.0		
F212			(LL)	0.227	0.410	0.884	0.023	0.031	0.047				
	A	→	Y (HH)	0.170	0.270	0.504	0.015	0.022	0.031	A	1.0	Y	22
			(LL)	0.264	0.462	0.968	0.012	0.017	0.025				
F232	B	→	Y (HH)	0.185	0.289	0.540	0.015	0.022	0.031	B	1.0		
			(LL)	0.252	0.474	1.026	0.012	0.017	0.025				
	A	→	Y (HH)	0.219	0.343	0.651	0.007	0.011	0.016	A	1.0	Y	44
		(LL)	0.359	0.655	1.391	0.006	0.009	0.014					
F252	B	→	Y (HH)	0.231	0.362	0.688	0.007	0.011	0.016	B	1.0		
			(LL)	0.348	0.670	1.447	0.006	0.009	0.014				
	A	→	Y (HH)	0.228	0.355	0.672	0.004	0.006	0.008	A	2.0	Y	88
		(LL)	0.353	0.662	1.416	0.003	0.005	0.008					
F252	B	→	Y (HH)	0.228	0.355	0.672	0.004	0.006	0.008	B	2.1		
			(LL)	0.353	0.662	1.416	0.003	0.005	0.008				

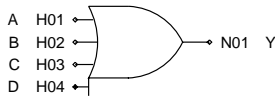
Chapter 2 Function Block

Function	3-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L213	2									
x1	F213	3									
x2	F233	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout				
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.								
L213	A → Y	(HH)		0.188	0.287	0.544	0.029	0.042	0.061	A	1.0	Y	10				
		(LL)		0.361	0.573	1.253	0.026	0.035	0.055								
	B → Y	(HH)		0.204	0.308	0.583	0.029	0.042	0.062					B	1.0		
		(LL)		0.376	0.637	1.414	0.025	0.035	0.055								
	C → Y	(HH)		0.215	0.322	0.611	0.029	0.043	0.063							C	1.0
		(LL)		0.407	0.724	1.560	0.025	0.035	0.055								
F213	A → Y	(HH)		0.192	0.293	0.551	0.015	0.022	0.032	A	1.0	Y	22				
		(LL)		0.407	0.684	1.494	0.014	0.019	0.030								
	B → Y	(HH)		0.206	0.313	0.591	0.015	0.022	0.032					B	1.0		
		(LL)		0.423	0.749	1.652	0.014	0.019	0.030								
	C → Y	(HH)		0.219	0.330	0.623	0.015	0.022	0.032							C	1.0
		(LL)		0.458	0.839	1.801	0.014	0.019	0.030								
F233	A → Y	(HH)		0.236	0.361	0.692	0.007	0.011	0.016	A	1.0	Y	43				
		(LL)		0.543	0.966	2.115	0.007	0.011	0.017								
	B → Y	(HH)		0.248	0.382	0.733	0.007	0.011	0.016					B	1.0		
		(LL)		0.562	1.034	2.269	0.007	0.011	0.017								
	C → Y	(HH)		0.262	0.402	0.776	0.007	0.011	0.017							C	1.0
		(LL)		0.597	1.121	2.415	0.007	0.011	0.017								

Chapter 2 Function Block

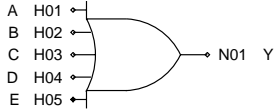
Function	4-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L214	3									
x1	F214	3									
x2	F234	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L214	A → Y	(HH)		0.184	0.287	0.547	0.029	0.042	0.061	A	1.0	Y	10		
		(LL)		0.389	0.638	1.442	0.027	0.039	0.061						
	B → Y	(HH)		0.200	0.309	0.586	0.029	0.042	0.061					B	1.0
		(LL)		0.422	0.741	1.691	0.027	0.039	0.061						
	C → Y	(HH)		0.213	0.326	0.621	0.029	0.043	0.063	C	1.0				
		(LL)		0.497	0.916	2.001	0.027	0.039	0.061						
	D → Y	(HH)		0.213	0.325	0.617	0.029	0.043	0.064	D	1.0				
		(LL)		0.503	0.938	2.047	0.027	0.039	0.061						
F214	A → Y	(HH)		0.187	0.291	0.550	0.015	0.022	0.032	A	1.0	Y	22		
		(LL)		0.440	0.768	1.742	0.014	0.021	0.033						
	B → Y	(HH)		0.201	0.312	0.590	0.015	0.022	0.032					B	1.0
		(LL)		0.476	0.875	1.990	0.014	0.021	0.033						
	C → Y	(HH)		0.215	0.330	0.627	0.015	0.022	0.032	C	1.0				
		(LL)		0.556	1.055	2.307	0.014	0.021	0.033						
	D → Y	(HH)		0.215	0.329	0.623	0.015	0.022	0.033	D	1.0				
		(LL)		0.562	1.076	2.352	0.014	0.021	0.033						
F234	A → Y	(HH)		0.232	0.360	0.692	0.007	0.011	0.016	A	1.0	Y	38		
		(LL)		0.615	1.135	2.554	0.008	0.012	0.019						
	B → Y	(HH)		0.245	0.381	0.734	0.007	0.011	0.016					B	1.0
		(LL)		0.653	1.245	2.799	0.008	0.012	0.019						
	C → Y	(HH)		0.259	0.403	0.781	0.007	0.011	0.017	C	1.0				
		(LL)		0.734	1.420	3.109	0.008	0.012	0.019						
	D → Y	(HH)		0.260	0.403	0.780	0.007	0.011	0.017	D	1.0				
		(LL)		0.741	1.441	3.155	0.008	0.012	0.019						



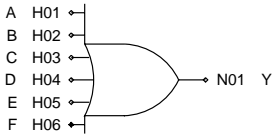
Chapter 2 Function Block

Function	5-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L215	4									
x1	F215	5									
x2	F235	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L215	A → Y	(HH)		0.163	0.262	0.501	0.029	0.042	0.061	A	1.0	Y	8		
		(LL)		0.250	0.428	0.930	0.034	0.051	0.085						
	B → Y	(HH)		0.179	0.282	0.536	0.029	0.042	0.061					B	1.0
		(LL)		0.238	0.440	0.989	0.034	0.051	0.085					C	1.0
	C → Y	(HH)		0.206	0.312	0.603	0.029	0.042	0.061					D	1.0
		(LL)		0.365	0.578	1.290	0.035	0.052	0.087	E	1.0				
	D → Y	(HH)		0.221	0.333	0.642	0.029	0.042	0.062						
		(LL)		0.380	0.642	1.450	0.035	0.052	0.087						
	E → Y	(HH)		0.235	0.351	0.677	0.029	0.043	0.063						
		(LL)		0.411	0.729	1.596	0.035	0.052	0.087						
F215	A → Y	(HH)		0.202	0.317	0.608	0.014	0.021	0.031	A	1.0	Y	15		
		(LL)		0.299	0.520	1.120	0.017	0.026	0.043						
	B → Y	(HH)		0.216	0.336	0.644	0.014	0.021	0.031					B	1.0
		(LL)		0.287	0.532	1.178	0.017	0.026	0.043					C	1.0
	C → Y	(HH)		0.223	0.338	0.655	0.014	0.021	0.031					D	1.0
		(LL)		0.451	0.752	1.667	0.018	0.027	0.046	E	1.0				
	D → Y	(HH)		0.237	0.359	0.695	0.014	0.021	0.031						
		(LL)		0.468	0.818	1.825	0.018	0.027	0.046						
	E → Y	(HH)		0.250	0.377	0.732	0.014	0.022	0.032						
		(LL)		0.501	0.906	1.972	0.018	0.027	0.046						
F235	A → Y	(HH)		0.336	0.591	1.226	0.007	0.011	0.016	A	1.0	Y	45		
		(LL)		0.455	0.833	1.867	0.006	0.008	0.011						
	B → Y	(HH)		0.352	0.611	1.262	0.007	0.011	0.016					B	1.0
		(LL)		0.443	0.845	1.926	0.006	0.008	0.011					C	1.0
	C → Y	(HH)		0.387	0.649	1.338	0.007	0.011	0.016					D	1.0
		(LL)		0.573	0.985	2.236	0.006	0.008	0.011	E	1.0				
	D → Y	(HH)		0.402	0.670	1.378	0.007	0.011	0.016						
		(LL)		0.588	1.050	2.396	0.006	0.008	0.011						
	E → Y	(HH)		0.416	0.690	1.423	0.007	0.011	0.016						
		(LL)		0.622	1.140	2.546	0.006	0.008	0.011						

Chapter 2 Function Block

6-Input OR											
Function											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L216	4									
x1	F216	5									
x2	F236	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L216	A → Y	(HH)		0.195	0.297	0.566	0.030	0.044	0.063	A	1.0	Y	7		
		(LL)		0.407	0.655	1.450	0.037	0.056	0.094						
	B → Y	(HH)		0.210	0.317	0.605	0.030	0.044	0.063					B	1.0
		(LL)		0.422	0.720	1.611	0.037	0.056	0.094						
	C → Y	(HH)		0.222	0.333	0.636	0.030	0.044	0.064					C	1.0
		(LL)		0.455	0.808	1.757	0.037	0.056	0.094						
	D → Y	(HH)		0.213	0.320	0.615	0.030	0.044	0.063	D	1.0				
		(LL)		0.373	0.590	1.310	0.036	0.053	0.089						
	E → Y	(HH)		0.228	0.342	0.655	0.030	0.044	0.063	E	1.0				
		(LL)		0.389	0.655	1.471	0.036	0.053	0.089						
	F → Y	(HH)		0.241	0.359	0.690	0.030	0.044	0.064	F	1.0				
		(LL)		0.422	0.745	1.620	0.036	0.053	0.089						
F216	A → Y	(HH)		0.233	0.359	0.687	0.015	0.022	0.031	A	1.0	Y	14		
		(LL)		0.466	0.786	1.729	0.019	0.028	0.047						
	B → Y	(HH)		0.247	0.379	0.727	0.015	0.022	0.031					B	1.0
		(LL)		0.482	0.851	1.887	0.019	0.028	0.047						
	C → Y	(HH)		0.259	0.397	0.765	0.015	0.022	0.032					C	1.0
		(LL)		0.515	0.939	2.034	0.019	0.028	0.047						
	D → Y	(HH)		0.235	0.361	0.690	0.014	0.021	0.031	D	1.0				
		(LL)		0.477	0.801	1.752	0.019	0.028	0.047						
	E → Y	(HH)		0.249	0.381	0.730	0.014	0.021	0.031	E	1.0				
		(LL)		0.493	0.867	1.910	0.019	0.028	0.047						
	F → Y	(HH)		0.261	0.400	0.769	0.015	0.022	0.032	F	1.0				
		(LL)		0.529	0.957	2.060	0.019	0.028	0.047						
F236	A → Y	(HH)		0.365	0.623	1.290	0.007	0.011	0.016	A	1.0	Y	45		
		(LL)		0.599	1.047	2.392	0.006	0.008	0.011						
	B → Y	(HH)		0.380	0.644	1.330	0.007	0.011	0.016					B	1.0
		(LL)		0.615	1.112	2.552	0.006	0.008	0.011						
	C → Y	(HH)		0.393	0.662	1.372	0.007	0.011	0.016					C	1.0
		(LL)		0.648	1.202	2.701	0.006	0.008	0.011						
	D → Y	(HH)		0.395	0.659	1.355	0.007	0.011	0.016	D	1.0				
		(LL)		0.578	0.994	2.251	0.006	0.008	0.011						
	E → Y	(HH)		0.410	0.681	1.396	0.007	0.011	0.016	E	1.0				
		(LL)		0.594	1.058	2.412	0.006	0.008	0.011						
	F → Y	(HH)		0.424	0.701	1.440	0.007	0.011	0.016	F	1.0				
		(LL)		0.626	1.147	2.558	0.006	0.008	0.011						

Chapter 2 Function Block

Function	8-Input OR										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L218	6									
x1	F218	8									
x2	F238	9									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L218	A → Y	(HH)		0.180	0.296	0.570	0.029	0.042	0.061	A	1.0	Y	2
		(LL)		0.293	0.542	1.252	0.060	0.094	0.167				
	B → Y	(HH)		0.196	0.317	0.607	0.029	0.042	0.061	B	1.0		
		(LL)		0.281	0.554	1.311	0.060	0.094	0.167				
	C → Y	(HH)		0.200	0.324	0.625	0.029	0.042	0.061	C	1.0		
		(LL)		0.306	0.555	1.299	0.060	0.094	0.168				
	D → Y	(HH)		0.216	0.345	0.663	0.029	0.042	0.061	D	1.0		
		(LL)		0.294	0.567	1.359	0.060	0.094	0.168				
	E → Y	(HH)		0.235	0.365	0.700	0.029	0.043	0.062	E	1.0		
		(LL)		0.357	0.605	1.429	0.061	0.094	0.168				
	F → Y	(HH)		0.250	0.385	0.737	0.029	0.043	0.063	F	1.0		
		(LL)		0.344	0.618	1.488	0.061	0.094	0.168				
	G → Y	(HH)		0.242	0.374	0.709	0.030	0.043	0.064	G	1.0		
		(LL)		0.363	0.606	1.422	0.061	0.094	0.168				
	H → Y	(HH)		0.257	0.395	0.747	0.030	0.043	0.064	H	1.0		
		(LL)		0.349	0.617	1.481	0.061	0.094	0.168				
F218	A → Y	(HH)		0.328	0.582	1.209	0.015	0.021	0.031	A	1.0	Y	23
		(LL)		0.519	0.998	2.378	0.011	0.015	0.022				
	B → Y	(HH)		0.344	0.603	1.246	0.015	0.021	0.031	B	1.0		
		(LL)		0.507	1.009	2.437	0.011	0.015	0.022				
	C → Y	(HH)		0.353	0.616	1.272	0.015	0.021	0.031	C	1.0		
		(LL)		0.533	1.009	2.425	0.011	0.015	0.022				
	D → Y	(HH)		0.369	0.637	1.310	0.015	0.021	0.031	D	1.0		
		(LL)		0.521	1.021	2.484	0.011	0.015	0.022				
	E → Y	(HH)		0.408	0.682	1.389	0.015	0.021	0.031	E	1.0		
		(LL)		0.599	1.080	2.586	0.011	0.015	0.022				
	F → Y	(HH)		0.424	0.703	1.427	0.015	0.021	0.031	F	1.0		
		(LL)		0.586	1.092	2.645	0.011	0.015	0.022				
	G → Y	(HH)		0.419	0.697	1.413	0.015	0.021	0.031	G	1.0		
		(LL)		0.601	1.075	2.570	0.011	0.015	0.022				
	H → Y	(HH)		0.435	0.718	1.451	0.015	0.021	0.031	H	1.0		
		(LL)		0.588	1.088	2.629	0.011	0.015	0.022				
F238	A → Y	(HH)		0.357	0.637	1.322	0.007	0.011	0.016	A	1.0	Y	45
		(LL)		0.565	1.086	2.570	0.006	0.008	0.011				
	B → Y	(HH)		0.373	0.658	1.360	0.007	0.011	0.016	B	1.0		
		(LL)		0.553	1.097	2.629	0.006	0.008	0.011				
	C → Y	(HH)		0.384	0.672	1.386	0.007	0.011	0.016	C	1.0		
		(LL)		0.580	1.099	2.619	0.006	0.008	0.011				
	D → Y	(HH)		0.401	0.693	1.425	0.007	0.011	0.016	D	1.0		
		(LL)		0.567	1.111	2.678	0.006	0.008	0.011				
	E → Y	(HH)		0.452	0.753	1.527	0.007	0.011	0.016	E	1.0		
		(LL)		0.645	1.169	2.780	0.006	0.008	0.011				
	F → Y	(HH)		0.466	0.773	1.563	0.007	0.011	0.016	F	1.0		
		(LL)		0.632	1.182	2.838	0.006	0.008	0.011				
	G → Y	(HH)		0.457	0.760	1.539	0.007	0.011	0.016	G	1.0		
		(LL)		0.652	1.172	2.774	0.006	0.008	0.011				
	H → Y	(HH)		0.473	0.781	1.577	0.007	0.011	0.016	H	1.0		
		(LL)		0.638	1.183	2.834	0.006	0.008	0.011				

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## 2.4 AND(NAND)

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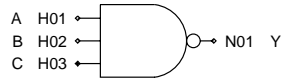
Chapter 2 Function Block

Function	2-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L302	1									
x1	F302	2									
x2	F322	4									
x4	F382	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L302	A	→	Y (HL)	0.119	0.158	0.287	0.034	0.049	0.082	A	1.0	Y	9
			(LH)	0.081	0.127	0.232	0.029	0.042	0.061				
	B	→	Y (HL)	0.103	0.143	0.294	0.034	0.049	0.081	B	1.0		
			(LH)	0.105	0.157	0.283	0.028	0.042	0.061				
F302	A	→	Y (HL)	0.111	0.152	0.293	0.017	0.025	0.041	A	2.1	Y	18
			(LH)	0.094	0.143	0.259	0.014	0.021	0.030				
	B	→	Y (HL)	0.110	0.152	0.293	0.017	0.025	0.041	B	2.1		
			(LH)	0.094	0.143	0.259	0.014	0.021	0.030				
F322	A	→	Y (HL)	0.115	0.158	0.303	0.008	0.012	0.020	A	4.1	Y	36
			(LH)	0.098	0.148	0.266	0.007	0.011	0.015				
	B	→	Y (HL)	0.115	0.158	0.303	0.008	0.012	0.020	B	4.1		
			(LH)	0.097	0.148	0.266	0.007	0.011	0.015				
F382	A	→	Y (HL)	0.383	0.666	1.431	0.003	0.004	0.006	A	1.0	Y	89
			(LH)	0.302	0.537	1.120	0.004	0.005	0.008				
	B	→	Y (HL)	0.366	0.650	1.436	0.003	0.004	0.006	B	1.0		
			(LH)	0.333	0.572	1.183	0.004	0.005	0.008				

Chapter 2 Function Block

Function	3-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L303	2									
x1	F303	3									
x2	F323	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L303	A → Y	(HL)		0.160	0.242	0.514	0.047	0.072	0.125	A	1.0	Y	4
		(LH)		0.098	0.162	0.297	0.029	0.042	0.061				
	B → Y	(HL)		0.160	0.253	0.576	0.047	0.072	0.125	B	1.0		
		(LH)		0.121	0.192	0.354	0.029	0.042	0.061				
	C → Y	(HL)		0.176	0.273	0.633	0.047	0.072	0.125	C	1.0		
		(LH)		0.154	0.229	0.419	0.029	0.042	0.062				
F303	A → Y	(HL)		0.134	0.204	0.439	0.024	0.036	0.063	A	2.1	Y	10
		(LH)		0.105	0.168	0.296	0.015	0.022	0.032				
	B → Y	(HL)		0.149	0.225	0.504	0.024	0.036	0.063	B	2.1		
		(LH)		0.123	0.187	0.339	0.014	0.021	0.031				
	C → Y	(HL)		0.134	0.205	0.440	0.024	0.036	0.063	C	2.1		
		(LH)		0.106	0.168	0.296	0.015	0.022	0.032				
F323	A → Y	(HL)		0.177	0.268	0.591	0.012	0.018	0.032	A	4.3	Y	17
		(LH)		0.128	0.199	0.358	0.007	0.011	0.016				
	B → Y	(HL)		0.166	0.263	0.594	0.012	0.018	0.031	B	4.2		
		(LH)		0.124	0.197	0.360	0.007	0.011	0.015				
	C → Y	(HL)		0.177	0.269	0.591	0.012	0.018	0.032	C	4.2		
		(LH)		0.128	0.199	0.358	0.007	0.011	0.016				

Chapter 2 Function Block

Function	4-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L304	2									
x1	F304	4									
x2	F324	8									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L304	A → Y	(HL)		0.158	0.249	0.574	0.060	0.094	0.167	A	1.0	Y	2		
		(LH)		0.094	0.159	0.295	0.029	0.042	0.061						
	B → Y	(HL)		0.169	0.281	0.689	0.060	0.094	0.166					B	1.0
		(LH)		0.118	0.190	0.354	0.029	0.042	0.061						
	C → Y	(HL)		0.211	0.335	0.829	0.060	0.094	0.166	C	1.0				
		(LH)		0.152	0.229	0.425	0.029	0.043	0.062						
	D → Y	(HL)		0.208	0.334	0.838	0.060	0.094	0.166	D	1.0				
		(LH)		0.160	0.239	0.435	0.029	0.043	0.064						
F304	A → Y	(HL)		0.195	0.308	0.734	0.030	0.047	0.084	A	2.1	Y	5		
		(LH)		0.129	0.201	0.363	0.015	0.022	0.032						
	B → Y	(HL)		0.201	0.324	0.787	0.030	0.047	0.084					B	2.1
		(LH)		0.139	0.214	0.395	0.015	0.021	0.031						
	C → Y	(HL)		0.201	0.324	0.787	0.030	0.047	0.084	C	2.1				
		(LH)		0.139	0.214	0.395	0.015	0.021	0.031						
	D → Y	(HL)		0.195	0.308	0.734	0.030	0.047	0.084	D	2.1				
		(LH)		0.129	0.201	0.363	0.015	0.022	0.032						
F324	A → Y	(HL)		0.196	0.310	0.737	0.015	0.024	0.042	A	4.3	Y	10		
		(LH)		0.129	0.202	0.364	0.007	0.011	0.016						
	B → Y	(HL)		0.202	0.326	0.790	0.015	0.024	0.042					B	4.3
		(LH)		0.139	0.215	0.396	0.007	0.011	0.016						
	C → Y	(HL)		0.202	0.326	0.790	0.015	0.024	0.042	C	4.3				
		(LH)		0.139	0.215	0.396	0.007	0.011	0.016						
	D → Y	(HL)		0.196	0.310	0.737	0.015	0.024	0.042	D	4.3				
		(LH)		0.129	0.202	0.364	0.007	0.011	0.016						



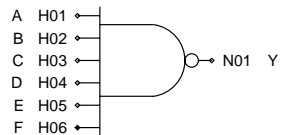
Chapter 2 Function Block

Function	5-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F305	5									
x2	F325	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
F305	A → Y	(HL)		0.388	0.674	1.449	0.012	0.017	0.026	A	1.0	Y	22		
		(LH)		0.244	0.428	0.888	0.015	0.022	0.031						
	B → Y	(HL)		0.374	0.658	1.456	0.012	0.017	0.026					B	1.0
		(LH)		0.276	0.463	0.950	0.015	0.022	0.031						
	C → Y	(HL)		0.458	0.818	1.824	0.012	0.017	0.026					D	1.0
		(LH)		0.278	0.498	1.030	0.015	0.022	0.031						
	D → Y	(HL)		0.456	0.828	1.888	0.012	0.017	0.026	E	1.0				
		(LH)		0.310	0.534	1.096	0.015	0.022	0.031						
	E → Y	(HL)		0.473	0.849	1.946	0.012	0.017	0.026						
		(LH)		0.355	0.585	1.192	0.015	0.022	0.031						
F325	A → Y	(HL)		0.480	0.862	1.860	0.006	0.009	0.014	A	1.0	Y	44		
		(LH)		0.282	0.497	1.036	0.007	0.011	0.016						
	B → Y	(HL)		0.466	0.845	1.867	0.006	0.009	0.014					C	1.0
		(LH)		0.315	0.533	1.099	0.007	0.011	0.016						
	C → Y	(HL)		0.553	1.011	2.246	0.006	0.009	0.014					D	1.0
		(LH)		0.322	0.576	1.194	0.007	0.011	0.016						
	D → Y	(HL)		0.552	1.021	2.309	0.006	0.009	0.014	E	1.0				
		(LH)		0.353	0.613	1.261	0.007	0.011	0.016						
	E → Y	(HL)		0.568	1.041	2.365	0.006	0.009	0.014						
		(LH)		0.401	0.665	1.359	0.007	0.011	0.016						

Chapter 2 Function Block

Function	6-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F306	5									
x2	F326	6									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F306	A → Y	(HL)		0.466	0.824	1.850	0.012	0.017	0.026	A	1.0	Y	22		
		(LH)		0.266	0.476	0.988	0.015	0.022	0.031						
	B → Y	(HL)		0.465	0.834	1.913	0.012	0.017	0.026					B	1.0
		(LH)		0.296	0.512	1.054	0.015	0.022	0.031					C	1.0
	C → Y	(HL)		0.481	0.853	1.970	0.012	0.017	0.026					D	1.0
		(LH)		0.341	0.562	1.147	0.015	0.022	0.031					E	1.0
	D → Y	(HL)		0.463	0.827	1.841	0.012	0.017	0.026	F	1.0				
		(LH)		0.282	0.503	1.038	0.015	0.022	0.031						
	E → Y	(HL)		0.462	0.838	1.905	0.012	0.017	0.026						
		(LH)		0.313	0.539	1.104	0.015	0.022	0.031						
	F → Y	(HL)		0.479	0.859	1.963	0.012	0.017	0.026						
		(LH)		0.360	0.592	1.202	0.015	0.022	0.031						
F326	A → Y	(HL)		0.562	1.017	2.276	0.006	0.009	0.014	A	1.0	Y	44		
		(LH)		0.307	0.552	1.148	0.007	0.011	0.016						
	B → Y	(HL)		0.562	1.028	2.339	0.006	0.009	0.014					B	1.0
		(LH)		0.339	0.589	1.215	0.007	0.011	0.016					C	1.0
	C → Y	(HL)		0.578	1.048	2.398	0.006	0.009	0.014					D	1.0
		(LH)		0.388	0.643	1.314	0.007	0.011	0.016					E	1.0
	D → Y	(HL)		0.560	1.024	2.269	0.006	0.009	0.014	F	1.0				
		(LH)		0.327	0.583	1.203	0.007	0.011	0.016						
	E → Y	(HL)		0.559	1.034	2.332	0.006	0.009	0.014						
		(LH)		0.358	0.620	1.270	0.007	0.011	0.016						
	F → Y	(HL)		0.575	1.052	2.389	0.006	0.009	0.014						
		(LH)		0.407	0.673	1.370	0.007	0.011	0.016						

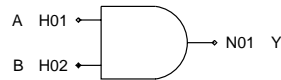
Chapter 2 Function Block

Function	8-Input NAND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1	F308	6									
x2	F328	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F308	A → Y	(HL)		0.486	0.878	2.040	0.012	0.017	0.026	A	1.0	Y	22
		(LH)		0.258	0.468	0.979	0.015	0.022	0.031	B	1.0		
	B → Y	(HL)		0.499	0.908	2.156	0.012	0.017	0.026	C	1.0	D	1.0
		(LH)		0.290	0.505	1.047	0.015	0.022	0.031	E	1.0		
	C → Y	(HL)		0.540	0.963	2.296	0.012	0.017	0.026	F	1.0	G	1.0
		(LH)		0.335	0.557	1.147	0.015	0.022	0.031	H	1.0		
	D → Y	(HL)		0.537	0.961	2.305	0.012	0.017	0.026				
		(LH)		0.349	0.575	1.175	0.015	0.022	0.031				
	E → Y	(HL)		0.475	0.863	1.987	0.012	0.017	0.026				
		(LH)		0.273	0.491	1.024	0.015	0.022	0.031				
	F → Y	(HL)		0.486	0.893	2.103	0.012	0.017	0.026				
		(LH)		0.304	0.529	1.093	0.015	0.022	0.031				
	G → Y	(HL)		0.526	0.948	2.243	0.012	0.017	0.026				
		(LH)		0.351	0.582	1.194	0.015	0.022	0.031				
	H → Y	(HL)		0.524	0.947	2.252	0.012	0.017	0.026				
		(LH)		0.365	0.601	1.225	0.015	0.022	0.031				
F328	A → Y	(HL)		0.588	1.080	2.488	0.006	0.009	0.014	A	1.0	Y	43
		(LH)		0.301	0.545	1.141	0.007	0.011	0.016	B	1.0		
	B → Y	(HL)		0.600	1.111	2.604	0.006	0.009	0.014	C	1.0	D	1.0
		(LH)		0.333	0.583	1.210	0.007	0.011	0.016	E	1.0		
	C → Y	(HL)		0.642	1.167	2.747	0.006	0.009	0.014	F	1.0	G	1.0
		(LH)		0.383	0.639	1.316	0.007	0.011	0.016	H	1.0		
	D → Y	(HL)		0.639	1.166	2.756	0.006	0.009	0.014				
		(LH)		0.398	0.659	1.348	0.007	0.011	0.016				
	E → Y	(HL)		0.576	1.066	2.431	0.006	0.009	0.014				
		(LH)		0.318	0.573	1.192	0.007	0.011	0.016				
	F → Y	(HL)		0.586	1.096	2.546	0.006	0.009	0.014				
		(LH)		0.350	0.611	1.261	0.007	0.011	0.016				
	G → Y	(HL)		0.628	1.153	2.689	0.006	0.009	0.014				
		(LH)		0.401	0.668	1.369	0.007	0.011	0.016				
	H → Y	(HL)		0.625	1.151	2.698	0.006	0.009	0.014				
		(LH)		0.417	0.689	1.403	0.007	0.011	0.016				

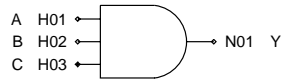
Chapter 2 Function Block

Function	2-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L312	2									
x1	F312	2									
x2	F332	3									
x4	F352	6									
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L312	A	→	Y (HH)	0.210	0.329	0.684	0.029	0.042	0.062	A	1.0	Y	10
			(LL)	0.171	0.282	0.558	0.022	0.029	0.043	B	1.0		
F312	A	→	Y (HH)	0.221	0.355	0.751	0.015	0.022	0.033	A	1.0	Y	22
			(LL)	0.184	0.312	0.621	0.011	0.015	0.022	B	1.0		
F332	A	→	Y (HH)	0.221	0.355	0.751	0.015	0.022	0.033	A	1.0	Y	22
			(LL)	0.184	0.312	0.621	0.011	0.015	0.022	B	1.0		
F352	A	→	Y (HH)	0.275	0.465	1.032	0.004	0.006	0.009	A	2.1	Y	82
			(LL)	0.256	0.439	0.879	0.003	0.004	0.006	B	2.1		

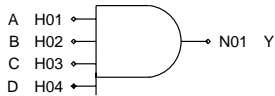
Chapter 2 Function Block

Function	3-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L313	2									
x1	F313	3									
x2	F333	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout				
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.								
L313	A → Y	(HH)		0.280	0.463	1.039	0.029	0.044	0.066	A	1.0	Y	10				
		(LL)		0.193	0.328	0.651	0.022	0.030	0.044								
	B → Y	(HH)		0.279	0.473	1.102	0.029	0.044	0.066					B	1.0		
		(LL)		0.225	0.364	0.716	0.022	0.030	0.044								
	C → Y	(HH)		0.295	0.493	1.158	0.029	0.044	0.066							C	1.0
		(LL)		0.264	0.407	0.796	0.023	0.030	0.045								
F313	A → Y	(HH)		0.298	0.512	1.168	0.015	0.023	0.035	A	1.0	Y	20				
		(LL)		0.205	0.356	0.708	0.011	0.016	0.023								
	B → Y	(HH)		0.296	0.522	1.231	0.015	0.023	0.035					B	1.0		
		(LL)		0.233	0.392	0.772	0.011	0.016	0.023								
	C → Y	(HH)		0.313	0.543	1.289	0.015	0.023	0.035							C	1.0
		(LL)		0.277	0.442	0.863	0.012	0.016	0.024								
F333	A → Y	(HH)		0.375	0.674	1.575	0.008	0.012	0.019	A	1.0	Y	36				
		(LL)		0.259	0.460	0.927	0.006	0.008	0.013								
	B → Y	(HH)		0.373	0.685	1.637	0.008	0.012	0.019					B	1.0		
		(LL)		0.286	0.495	0.991	0.006	0.008	0.013								
	C → Y	(HH)		0.390	0.704	1.693	0.008	0.012	0.019							C	1.0
		(LL)		0.329	0.546	1.088	0.006	0.008	0.013								

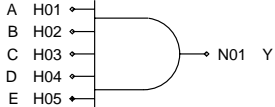
Chapter 2 Function Block

Function	4-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L314	3									
x1	F314	3									
x2	F334	4									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L314	A → Y	(HH)		0.305	0.519	1.215	0.030	0.045	0.070	A	1.0	Y	9		
		(LL)		0.192	0.329	0.655	0.022	0.030	0.044						
	B → Y	(HH)		0.317	0.551	1.331	0.030	0.045	0.070					B	1.0
		(LL)		0.223	0.366	0.722	0.022	0.030	0.044						
	C → Y	(HH)		0.357	0.605	1.470	0.030	0.045	0.070	C	1.0				
		(LL)		0.270	0.417	0.817	0.023	0.030	0.045						
	D → Y	(HH)		0.355	0.603	1.480	0.030	0.045	0.070	D	1.0				
		(LL)		0.283	0.434	0.842	0.023	0.031	0.046						
F314	A → Y	(HH)		0.321	0.576	1.383	0.016	0.024	0.037	A	1.0	Y	19		
		(LL)		0.199	0.350	0.702	0.011	0.015	0.023						
	B → Y	(HH)		0.333	0.607	1.497	0.016	0.024	0.037					B	1.0
		(LL)		0.228	0.387	0.769	0.011	0.015	0.023						
	C → Y	(HH)		0.375	0.664	1.640	0.016	0.024	0.037	C	1.0				
		(LL)		0.273	0.439	0.867	0.012	0.016	0.024						
	D → Y	(HH)		0.372	0.662	1.649	0.016	0.024	0.037	D	1.0				
		(LL)		0.286	0.456	0.894	0.012	0.016	0.024						
F334	A → Y	(HH)		0.418	0.786	1.929	0.008	0.012	0.020	A	1.0	Y	32		
		(LL)		0.255	0.456	0.924	0.006	0.008	0.013						
	B → Y	(HH)		0.431	0.819	2.041	0.008	0.012	0.020					B	1.0
		(LL)		0.282	0.493	0.990	0.006	0.008	0.013						
	C → Y	(HH)		0.473	0.874	2.181	0.008	0.012	0.020	C	1.0				
		(LL)		0.327	0.546	1.094	0.006	0.008	0.013						
	D → Y	(HH)		0.471	0.873	2.190	0.008	0.012	0.020	D	1.0				
		(LL)		0.342	0.567	1.128	0.006	0.008	0.013						

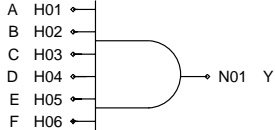
Chapter 2 Function Block

Function	5-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L315	4									
x1	F315	5									
x2	F335	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"			Logic Diagram for "with 2 inverter"					
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L315	A → Y	(HH)		0.229	0.375	0.803	0.052	0.078	0.117	A	1.0	Y	4
		(LL)		0.171	0.286	0.569	0.022	0.029	0.043				
	B → Y	(HH)		0.216	0.359	0.810	0.052	0.078	0.117	B	1.0		
		(LL)		0.203	0.322	0.631	0.022	0.029	0.043				
	C → Y	(HH)		0.300	0.518	1.170	0.052	0.079	0.118	C	1.0		
		(LL)		0.205	0.354	0.703	0.022	0.030	0.044				
	D → Y	(HH)		0.299	0.528	1.233	0.052	0.079	0.118	D	1.0		
		(LL)		0.237	0.390	0.769	0.022	0.030	0.044				
	E → Y	(HH)		0.315	0.548	1.290	0.052	0.079	0.118	E	1.0		
		(LL)		0.281	0.440	0.858	0.023	0.030	0.045				
F315	A → Y	(HH)		0.273	0.452	0.970	0.027	0.040	0.061	A	1.0	Y	8
		(LL)		0.213	0.359	0.714	0.012	0.016	0.024				
	B → Y	(HH)		0.255	0.435	0.976	0.027	0.040	0.061	B	1.0		
		(LL)		0.241	0.393	0.775	0.012	0.016	0.024				
	C → Y	(HH)		0.347	0.600	1.375	0.027	0.041	0.063	C	1.0		
		(LL)		0.229	0.398	0.796	0.012	0.017	0.025				
	D → Y	(HH)		0.345	0.610	1.437	0.027	0.041	0.063	D	1.0		
		(LL)		0.258	0.434	0.860	0.012	0.017	0.025				
	E → Y	(HH)		0.362	0.631	1.495	0.027	0.041	0.063	E	1.0		
		(LL)		0.300	0.484	0.953	0.013	0.017	0.026				
F335	A → Y	(HH)		0.461	0.824	1.808	0.007	0.011	0.016	A	1.0	Y	45
		(LL)		0.339	0.608	1.280	0.006	0.008	0.011				
	B → Y	(HH)		0.446	0.808	1.815	0.007	0.011	0.016	B	1.0		
		(LL)		0.371	0.644	1.343	0.006	0.008	0.011				
	C → Y	(HH)		0.531	0.969	2.184	0.007	0.011	0.016	C	1.0		
		(LL)		0.374	0.679	1.424	0.006	0.008	0.011				
	D → Y	(HH)		0.529	0.979	2.248	0.007	0.011	0.016	D	1.0		
		(LL)		0.405	0.716	1.491	0.006	0.008	0.011				
	E → Y	(HH)		0.546	1.000	2.306	0.007	0.011	0.016	E	1.0		
		(LL)		0.451	0.767	1.586	0.006	0.008	0.011				

Chapter 2 Function Block

Function	6-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L316	4									
x1	F316	5									
x2	F336	7									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
											
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout				
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.								
L316	A → Y	(HH)		0.308	0.521	1.187	0.052	0.079	0.119	A	1.0	Y	4				
		(LL)		0.195	0.337	0.668	0.022	0.030	0.044								
	B → Y	(HH)		0.308	0.532	1.251	0.052	0.079	0.119					B	1.0		
		(LL)		0.225	0.372	0.733	0.022	0.030	0.044								
	C → Y	(HH)		0.324	0.553	1.309	0.052	0.079	0.119							C	1.0
		(LL)		0.270	0.422	0.823	0.023	0.030	0.045								
	D → Y	(HH)		0.304	0.523	1.180	0.052	0.079	0.118	D	1.0						
		(LL)		0.208	0.358	0.708	0.022	0.030	0.044								
	E → Y	(HH)		0.303	0.534	1.243	0.052	0.079	0.118			E	1.0				
		(LL)		0.239	0.393	0.773	0.022	0.030	0.044								
	F → Y	(HH)		0.319	0.553	1.299	0.052	0.079	0.118					F	1.0		
		(LL)		0.284	0.444	0.864	0.023	0.030	0.045								
F316	A → Y	(HH)		0.353	0.612	1.401	0.026	0.040	0.060	A	1.0					Y	9
		(LL)		0.236	0.409	0.816	0.011	0.015	0.023								
	B → Y	(HH)		0.351	0.622	1.464	0.026	0.040	0.060			B	1.0				
		(LL)		0.264	0.445	0.880	0.011	0.015	0.023								
	C → Y	(HH)		0.366	0.642	1.520	0.026	0.040	0.060					C	1.0		
		(LL)		0.309	0.496	0.975	0.012	0.015	0.023								
	D → Y	(HH)		0.354	0.615	1.407	0.026	0.040	0.060	D	1.0						
		(LL)		0.238	0.412	0.820	0.011	0.015	0.023								
	E → Y	(HH)		0.352	0.625	1.469	0.026	0.040	0.060			E	1.0				
		(LL)		0.266	0.448	0.884	0.011	0.015	0.023								
	F → Y	(HH)		0.369	0.646	1.528	0.026	0.040	0.060					F	1.0		
		(LL)		0.312	0.500	0.980	0.012	0.015	0.023								
F336	A → Y	(HH)		0.538	0.975	2.210	0.007	0.011	0.016	A	1.0					Y	45
		(LL)		0.361	0.657	1.381	0.006	0.008	0.011								
	B → Y	(HH)		0.538	0.985	2.273	0.007	0.011	0.016			B	1.0				
		(LL)		0.391	0.693	1.447	0.006	0.008	0.011								
	C → Y	(HH)		0.554	1.004	2.330	0.007	0.011	0.016					C	1.0		
		(LL)		0.436	0.744	1.540	0.006	0.008	0.011								
	D → Y	(HH)		0.536	0.978	2.202	0.007	0.011	0.016	D	1.0						
		(LL)		0.378	0.685	1.433	0.006	0.008	0.011								
	E → Y	(HH)		0.535	0.989	2.265	0.007	0.011	0.016			E	1.0				
		(LL)		0.408	0.721	1.499	0.006	0.008	0.011								
	F → Y	(HH)		0.552	1.010	2.324	0.007	0.011	0.016					F	1.0		
		(LL)		0.456	0.774	1.596	0.006	0.008	0.011								



Chapter 2 Function Block

Function	8-Input AND										
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L318	5									
x1	F318	6									
x2	F338	8									
x4											
x8											
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter		-
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power											
x1											
x2											
x4											
x8											
Logic Diagram for "Normal"			Logic Diagram for "with 1 inverter"				Logic Diagram for "with 2 inverter"				
Logic Diagram for "with 3 inverter"			Logic Diagram for "with 4 inverter"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L318	A	→	Y	(HH)	0.330	0.574	1.361	0.053	0.080	0.122	A	1.0	Y	4
				(LL)	0.189	0.330	0.662	0.022	0.030	0.044	B	1.0		
	B	→	Y	(HH)	0.342	0.604	1.476	0.053	0.080	0.122	C	1.0		
				(LL)	0.220	0.367	0.729	0.022	0.030	0.044	D	1.0		
	C	→	Y	(HH)	0.384	0.660	1.619	0.052	0.080	0.122	E	1.0		
				(LL)	0.265	0.419	0.825	0.023	0.030	0.045	F	1.0		
	D	→	Y	(HH)	0.381	0.659	1.628	0.053	0.080	0.122	G	1.0		
				(LL)	0.278	0.435	0.849	0.023	0.031	0.046	H	1.0		
	E	→	Y	(HH)	0.321	0.565	1.329	0.052	0.079	0.120				
				(LL)	0.203	0.353	0.704	0.022	0.030	0.044				
	F	→	Y	(HH)	0.331	0.596	1.445	0.052	0.079	0.120				
				(LL)	0.234	0.390	0.772	0.022	0.030	0.044				
	G	→	Y	(HH)	0.373	0.652	1.588	0.052	0.079	0.120				
				(LL)	0.281	0.443	0.871	0.023	0.030	0.045				
	H	→	Y	(HH)	0.371	0.651	1.597	0.052	0.079	0.120				
				(LL)	0.295	0.461	0.896	0.023	0.031	0.045				
F318	A	→	Y	(HH)	0.379	0.674	1.609	0.027	0.042	0.065	A	1.0	Y	8
				(LL)	0.226	0.396	0.796	0.012	0.017	0.025	B	1.0		
	B	→	Y	(HH)	0.391	0.705	1.723	0.027	0.042	0.065	C	1.0		
				(LL)	0.255	0.433	0.862	0.012	0.017	0.025	D	1.0		
	C	→	Y	(HH)	0.432	0.760	1.863	0.027	0.042	0.065	E	1.0		
				(LL)	0.299	0.484	0.961	0.013	0.017	0.026	F	1.0		
	D	→	Y	(HH)	0.429	0.759	1.872	0.027	0.042	0.065	G	1.0		
				(LL)	0.312	0.502	0.989	0.013	0.017	0.026	H	1.0		
	E	→	Y	(HH)	0.380	0.675	1.612	0.027	0.042	0.065				
				(LL)	0.227	0.397	0.798	0.012	0.017	0.025				
	F	→	Y	(HH)	0.392	0.707	1.726	0.027	0.042	0.065				
				(LL)	0.256	0.434	0.864	0.012	0.017	0.025				
	G	→	Y	(HH)	0.433	0.762	1.866	0.027	0.042	0.065				
				(LL)	0.300	0.486	0.963	0.013	0.017	0.026				
	H	→	Y	(HH)	0.430	0.761	1.875	0.027	0.042	0.065				
				(LL)	0.313	0.504	0.991	0.013	0.017	0.026				
F338	A	→	Y	(HH)	0.562	1.033	2.409	0.007	0.011	0.016	A	1.0	Y	45
				(LL)	0.355	0.651	1.375	0.006	0.008	0.011	B	1.0		
	B	→	Y	(HH)	0.574	1.064	2.525	0.007	0.011	0.016	C	1.0		
				(LL)	0.386	0.688	1.443	0.006	0.008	0.011	D	1.0		
	C	→	Y	(HH)	0.616	1.118	2.665	0.007	0.011	0.016	E	1.0		
				(LL)	0.432	0.740	1.543	0.006	0.008	0.011	F	1.0		
	D	→	Y	(HH)	0.613	1.117	2.674	0.007	0.011	0.016	G	1.0		
				(LL)	0.445	0.759	1.572	0.006	0.008	0.011	H	1.0		
	E	→	Y	(HH)	0.559	1.031	2.380	0.007	0.011	0.016				
				(LL)	0.375	0.683	1.434	0.006	0.008	0.011				
	F	→	Y	(HH)	0.569	1.062	2.495	0.007	0.011	0.016				
				(LL)	0.406	0.721	1.502	0.006	0.008	0.011				
	G	→	Y	(HH)	0.610	1.116	2.635	0.007	0.011	0.016				
				(LL)	0.453	0.774	1.604	0.006	0.008	0.011				
	H	→	Y	(HH)	0.607	1.115	2.644	0.007	0.011	0.016				
				(LL)	0.468	0.794	1.635	0.006	0.008	0.011				

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## 2.5 AND-NOR

[MEMO]

Chapter 2 Function Block

Function	1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L421	2										
x1	F421	3										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L421	A → Y	(HL)		0.100	0.138	0.211	0.022	0.029	0.041	A	1.0	Y	3
		(LH)		0.097	0.291	0.576	0.040	0.084	0.123				
	B → Y	(HL)		0.154	0.227	0.436	0.035	0.052	0.085	B	1.0		
		(LH)		0.115	0.229	0.481	0.052	0.079	0.116				
	C → Y	(HL)		0.153	0.229	0.482	0.035	0.052	0.085	C	1.0		
		(LH)		0.209	0.347	0.714	0.057	0.084	0.123				
F421	A → Y	(HL)		0.092	0.123	0.196	0.012	0.015	0.021	A	2.1	Y	8
		(LH)		0.109	0.196	0.396	0.022	0.042	0.062				
	B → Y	(HL)		0.140	0.201	0.408	0.017	0.026	0.043	B	2.0		
		(LH)		0.150	0.260	0.555	0.029	0.043	0.062				
	C → Y	(HL)		0.140	0.201	0.408	0.017	0.026	0.043	C	2.0		
		(LH)		0.150	0.260	0.555	0.029	0.043	0.062				

Chapter 2 Function Block

Function	1-1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F422	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F422	A	→	Y	(HL)	0.100	0.134	0.214	0.012	0.015	0.021	A	2.1	Y	3
				(LH)	0.146	0.240	0.545	0.037	0.065	0.095				
	B	→	Y	(HL)	0.125	0.166	0.260	0.012	0.015	0.022	B	2.0		
				(LH)	0.192	0.420	0.913	0.038	0.065	0.095				
	C	→	Y	(HL)	0.157	0.227	0.482	0.018	0.027	0.045	C	2.0		
				(LH)	0.269	0.469	1.012	0.045	0.065	0.095				
	D	→	Y	(HL)	0.157	0.227	0.483	0.018	0.027	0.045	D	2.0		
				(LH)	0.269	0.469	1.012	0.045	0.065	0.095				

Chapter 2 Function Block

Function	1-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L423	2										
x1	F423	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L423	A → Y	(HL)		0.099	0.138	0.211	0.022	0.029	0.041	A	1.0	Y	3		
		(LH)		0.094	0.351	0.683	0.036	0.085	0.125						
	B → Y	(HL)		0.167	0.269	0.581	0.047	0.073	0.126					B	1.0
		(LH)		0.112	0.227	0.480	0.052	0.078	0.116						
	C → Y	(HL)		0.194	0.309	0.713	0.047	0.073	0.126	C	1.0				
		(LH)		0.207	0.350	0.729	0.057	0.084	0.123						
	D → Y	(HL)		0.187	0.305	0.722	0.047	0.073	0.126	D	1.0				
		(LH)		0.242	0.397	0.808	0.057	0.084	0.124						
F423	A → Y	(HL)		0.080	0.114	0.180	0.012	0.015	0.021	A	2.1	Y	8		
		(LH)		0.084	0.253	0.495	0.020	0.043	0.064						
	B → Y	(HL)		0.168	0.263	0.602	0.024	0.038	0.066					B	2.0
		(LH)		0.172	0.298	0.612	0.029	0.043	0.063						
	C → Y	(HL)		0.186	0.287	0.666	0.024	0.038	0.065	C	2.0				
		(LH)		0.203	0.336	0.695	0.029	0.043	0.063						
	D → Y	(HL)		0.168	0.264	0.604	0.024	0.038	0.066	D	2.0				
		(LH)		0.172	0.299	0.613	0.029	0.043	0.063						

Chapter 2 Function Block

Function	2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L424	2										
x1	F424	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L424	A → Y	(HL)		0.142	0.193	0.362	0.034	0.050	0.081	A	1.0	Y	2		
		(LH)		0.132	0.273	0.579	0.044	0.084	0.123						
	B → Y	(HL)		0.124	0.177	0.367	0.034	0.050	0.081					B	1.0
		(LH)		0.164	0.331	0.694	0.044	0.084	0.122						
	C → Y	(HL)		0.196	0.302	0.615	0.034	0.051	0.084	C	1.0				
		(LH)		0.151	0.384	0.812	0.044	0.084	0.123						
	D → Y	(HL)		0.176	0.286	0.619	0.034	0.051	0.084	D	1.0				
		(LH)		0.184	0.445	0.926	0.043	0.084	0.122						
F424	A → Y	(HL)		0.161	0.236	0.479	0.017	0.025	0.041	A	2.1	Y	4		
		(LH)		0.179	0.354	0.727	0.022	0.042	0.062						
	B → Y	(HL)		0.161	0.236	0.479	0.017	0.025	0.041					B	2.1
		(LH)		0.179	0.355	0.728	0.022	0.042	0.062						
	C → Y	(HL)		0.194	0.310	0.651	0.017	0.025	0.042	C	2.0				
		(LH)		0.182	0.412	0.864	0.022	0.042	0.061						
	D → Y	(HL)		0.194	0.310	0.651	0.017	0.025	0.042	D	2.0				
		(LH)		0.182	0.412	0.864	0.022	0.042	0.061						

Chapter 2 Function Block

Function	2-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F427	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F427	A → Y	(HL)		0.183	0.358	0.752	0.017	0.027	0.045	A	2.0	Y	5
		(LH)		0.160	0.503	1.032	0.020	0.043	0.063				
	B → Y	(HL)		0.183	0.358	0.752	0.017	0.027	0.045	B	2.0	C	2.1
		(LH)		0.160	0.503	1.032	0.020	0.043	0.063				
	C → Y	(HL)		0.159	0.242	0.537	0.024	0.036	0.063	C	2.1	D	2.1
		(LH)		0.164	0.304	0.632	0.022	0.042	0.063				
	D → Y	(HL)		0.175	0.262	0.600	0.024	0.036	0.063	D	2.1	E	2.1
		(LH)		0.187	0.337	0.708	0.022	0.042	0.062				
	E → Y	(HL)		0.158	0.241	0.536	0.024	0.036	0.063	E	2.1		
		(LH)		0.164	0.303	0.630	0.022	0.042	0.063				



Chapter 2 Function Block

Function	1-2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F428	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F428	A → Y	(HL)		0.113	0.145	0.230	0.012	0.015	0.021	A	2.1	Y	2
		(LH)		0.155	0.321	0.718	0.030	0.063	0.093				
	B → Y	(HL)		0.166	0.237	0.492	0.017	0.026	0.042	B	2.0		
		(LH)		0.243	0.485	1.071	0.037	0.063	0.093				
	C → Y	(HL)		0.166	0.237	0.492	0.017	0.026	0.042	C	2.0		
		(LH)		0.243	0.486	1.071	0.037	0.063	0.093				
	D → Y	(HL)		0.180	0.257	0.563	0.018	0.028	0.047	D	2.0		
		(LH)		0.312	0.622	1.309	0.037	0.064	0.093				
	E → Y	(HL)		0.180	0.257	0.563	0.018	0.028	0.047	E	2.0		
		(LH)		0.312	0.622	1.310	0.037	0.064	0.093				

Chapter 2 Function Block

Function	2-2-2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L429	6										
x1	F429	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t Ld0 (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L429	A → Y	(HL)		0.330	0.545	1.168	0.022	0.029	0.043	A	1.0	Y	10
		(LH)		0.365	0.758	1.677	0.029	0.043	0.063				
	B → Y	(HL)		0.314	0.529	1.174	0.022	0.029	0.043	B	1.0		
		(LH)		0.410	0.829	1.802	0.029	0.043	0.063				
	C → Y	(HL)		0.396	0.649	1.419	0.022	0.029	0.043	C	1.0		
		(LH)		0.387	0.868	1.907	0.029	0.043	0.063				
	D → Y	(HL)		0.376	0.633	1.423	0.022	0.029	0.043	D	1.0		
		(LH)		0.432	0.942	2.032	0.029	0.043	0.063				
	E → Y	(HL)		0.359	0.583	1.239	0.022	0.029	0.043	E	1.0		
		(LH)		0.355	0.716	1.578	0.029	0.043	0.063				
	F → Y	(HL)		0.343	0.566	1.244	0.022	0.029	0.043	F	1.0		
		(LH)		0.396	0.785	1.698	0.029	0.043	0.063				
	G → Y	(HL)		0.428	0.687	1.489	0.022	0.029	0.043	G	1.0		
		(LH)		0.373	0.827	1.808	0.029	0.043	0.063				
	H → Y	(HL)		0.407	0.671	1.493	0.022	0.029	0.043	H	1.0		
		(LH)		0.415	0.898	1.930	0.029	0.043	0.063				
F429	A → Y	(HL)		0.342	0.582	1.250	0.011	0.015	0.023	A	1.0	Y	21
		(LH)		0.376	0.799	1.777	0.015	0.022	0.033				
	B → Y	(HL)		0.326	0.566	1.256	0.011	0.015	0.023	B	1.0		
		(LH)		0.422	0.870	1.902	0.015	0.022	0.033				
	C → Y	(HL)		0.410	0.686	1.498	0.011	0.015	0.023	C	1.0		
		(LH)		0.400	0.909	2.007	0.015	0.022	0.033				
	D → Y	(HL)		0.390	0.669	1.502	0.011	0.015	0.023	D	1.0		
		(LH)		0.446	0.983	2.132	0.015	0.022	0.033				
	E → Y	(HL)		0.369	0.616	1.315	0.011	0.015	0.023	E	1.0		
		(LH)		0.361	0.747	1.660	0.015	0.022	0.033				
	F → Y	(HL)		0.352	0.599	1.320	0.011	0.015	0.023	F	1.0		
		(LH)		0.403	0.815	1.781	0.015	0.022	0.033				
	G → Y	(HL)		0.438	0.721	1.563	0.011	0.015	0.023	G	1.0		
		(LH)		0.380	0.858	1.891	0.015	0.022	0.033				
	H → Y	(HL)		0.417	0.704	1.567	0.011	0.015	0.023	H	1.0		
		(LH)		0.423	0.929	2.011	0.015	0.022	0.033				

Chapter 2 Function Block

Function	1-4-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F440	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F440	A → Y	(HL)		0.094	0.126	0.198	0.012	0.015	0.021	A	2.1	Y	3
		(LH)		0.101	0.274	0.539	0.019	0.044	0.065				
	B → Y	(HL)		0.238	0.387	0.953	0.031	0.049	0.087	B	2.1		
		(LH)		0.219	0.361	0.727	0.030	0.044	0.064				
	C → Y	(HL)		0.246	0.404	1.004	0.031	0.049	0.087	C	2.0		
		(LH)		0.232	0.382	0.780	0.029	0.043	0.063				
	D → Y	(HL)		0.246	0.404	1.004	0.031	0.049	0.087	D	2.0		
		(LH)		0.232	0.382	0.780	0.029	0.043	0.063				
	E → Y	(HL)		0.238	0.387	0.953	0.031	0.049	0.087	E	2.1		
		(LH)		0.218	0.361	0.728	0.030	0.044	0.064				

Chapter 2 Function Block

Function	1-5-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L441	5										
x1	F441	7										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L441	A → Y	(HL)		0.099	0.136	0.210	0.022	0.029	0.041	A	1.0	Y	3
		(LH)		0.096	0.287	0.569	0.040	0.084	0.124				
	B → Y	(HL)		0.343	0.585	1.278	0.035	0.052	0.085	B	1.0		
		(LH)		0.298	0.525	1.100	0.052	0.078	0.116	C	1.0		
	C → Y	(HL)		0.329	0.569	1.285	0.035	0.052	0.085	E	1.0		
		(LH)		0.330	0.561	1.161	0.052	0.078	0.116	F	1.0		
	D → Y	(HL)		0.434	0.732	1.667	0.035	0.052	0.085				
		(LH)		0.418	0.689	1.429	0.057	0.084	0.123				
	E → Y	(HL)		0.433	0.742	1.731	0.035	0.052	0.085				
		(LH)		0.449	0.726	1.494	0.057	0.084	0.123				
	F → Y	(HL)		0.448	0.761	1.787	0.035	0.052	0.085				
		(LH)		0.487	0.769	1.574	0.057	0.084	0.123				
F441	A → Y	(HL)		0.093	0.124	0.197	0.012	0.015	0.021	A	2.1	Y	8
		(LH)		0.111	0.197	0.398	0.022	0.042	0.062				
	B → Y	(HL)		0.376	0.629	1.375	0.018	0.026	0.044	B	1.0		
		(LH)		0.360	0.602	1.262	0.029	0.043	0.062	C	1.0		
	C → Y	(HL)		0.363	0.613	1.382	0.018	0.026	0.044	D	1.0		
		(LH)		0.392	0.638	1.324	0.029	0.043	0.062	E	1.0		
	D → Y	(HL)		0.457	0.784	1.781	0.018	0.026	0.044	F	1.0		
		(LH)		0.386	0.657	1.371	0.029	0.043	0.062				
	E → Y	(HL)		0.456	0.794	1.844	0.018	0.026	0.044				
		(LH)		0.417	0.692	1.437	0.029	0.043	0.062				
	F → Y	(HL)		0.472	0.814	1.902	0.018	0.026	0.044				
		(LH)		0.456	0.737	1.521	0.029	0.043	0.062				

Chapter 2 Function Block

Function	4-4-4-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L444	8										
x1	F444	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L444	A → Y	(HL)		0.394	0.683	1.592	0.022	0.030	0.044	A	1.0	Y	10
		(LH)		0.300	0.535	1.170	0.029	0.042	0.062	B	1.0		
	B → Y	(HL)		0.406	0.714	1.708	0.022	0.030	0.044	C	1.0	D	1.0
		(LH)		0.331	0.572	1.237	0.029	0.042	0.062	E	1.0		
	C → Y	(HL)		0.446	0.768	1.848	0.022	0.030	0.044	F	1.0	G	1.0
		(LH)		0.379	0.624	1.337	0.029	0.043	0.062	H	1.0		
	D → Y	(HL)		0.444	0.767	1.857	0.022	0.030	0.044	I	1.0	J	1.0
		(LH)		0.394	0.643	1.366	0.029	0.043	0.063	K	1.0		
	E → Y	(HL)		0.479	0.867	1.955	0.022	0.030	0.044	L	1.0	L	1.0
		(LH)		0.362	0.942	1.997	0.029	0.043	0.063				
	F → Y	(HL)		0.491	0.898	2.068	0.022	0.030	0.044				
		(LH)		0.398	1.017	2.138	0.029	0.043	0.063				
	G → Y	(HL)		0.533	0.952	2.208	0.022	0.030	0.044				
		(LH)		0.454	1.144	2.378	0.029	0.043	0.063				
	H → Y	(HL)		0.530	0.951	2.217	0.022	0.030	0.044				
		(LH)		0.475	1.197	2.469	0.029	0.043	0.063				
I → Y	(HL)		0.742	1.348	3.184	0.022	0.030	0.044					
	(LH)		0.424	1.188	2.487	0.029	0.043	0.063					
J → Y	(HL)		0.757	1.380	3.293	0.022	0.030	0.044					
	(LH)		0.461	1.265	2.627	0.029	0.043	0.063					
K → Y	(HL)		0.803	1.437	3.433	0.022	0.030	0.044					
	(LH)		0.521	1.392	2.865	0.029	0.043	0.063					
L → Y	(HL)		0.801	1.436	3.442	0.022	0.030	0.044					
	(LH)		0.544	1.446	2.956	0.029	0.043	0.063					
F444	A → Y	(HL)		0.406	0.722	1.686	0.011	0.015	0.023	A	1.0	Y	21
		(LH)		0.301	0.555	1.231	0.015	0.022	0.033	B	1.0		
	B → Y	(HL)		0.418	0.752	1.801	0.011	0.015	0.023	C	1.0	D	1.0
		(LH)		0.333	0.592	1.299	0.015	0.022	0.033	E	1.0		
	C → Y	(HL)		0.458	0.807	1.941	0.011	0.015	0.023	F	1.0	G	1.0
		(LH)		0.383	0.646	1.401	0.015	0.022	0.033	H	1.0		
	D → Y	(HL)		0.456	0.805	1.950	0.011	0.015	0.023	I	1.0	J	1.0
		(LH)		0.399	0.666	1.433	0.015	0.022	0.033	K	1.0		
	E → Y	(HL)		0.489	0.916	2.073	0.011	0.015	0.023	L	1.0	L	1.0
		(LH)		0.363	0.971	2.073	0.015	0.022	0.033				
	F → Y	(HL)		0.501	0.947	2.186	0.011	0.015	0.023				
		(LH)		0.399	1.045	2.214	0.015	0.022	0.033				
	G → Y	(HL)		0.543	1.000	2.326	0.011	0.015	0.023				
		(LH)		0.456	1.173	2.453	0.015	0.022	0.033				
	H → Y	(HL)		0.541	1.000	2.336	0.011	0.015	0.023				
		(LH)		0.478	1.227	2.545	0.015	0.022	0.033				
I → Y	(HL)		0.751	1.385	3.277	0.011	0.015	0.023					
	(LH)		0.426	1.213	2.559	0.015	0.022	0.033					
J → Y	(HL)		0.765	1.418	3.386	0.011	0.015	0.023					
	(LH)		0.464	1.290	2.699	0.015	0.022	0.033					
K → Y	(HL)		0.812	1.475	3.526	0.011	0.015	0.023					
	(LH)		0.525	1.418	2.937	0.015	0.022	0.033					
L → Y	(HL)		0.810	1.474	3.535	0.011	0.015	0.023					
	(LH)		0.548	1.474	3.028	0.015	0.022	0.033					

Chapter 2 Function Block

Function	1-1-1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L446	4										
x1	F446	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L446	A → Y	(HL)		0.255	0.422	0.842	0.022	0.029	0.043	A	1.0	Y	10		
		(LH)		0.343	0.602	1.346	0.029	0.043	0.063						
	B → Y	(HL)		0.271	0.442	0.877	0.022	0.029	0.043					B	1.0
		(LH)		0.331	0.613	1.406	0.029	0.043	0.063					C	1.0
	C → Y	(HL)		0.288	0.483	0.950	0.022	0.029	0.043					D	1.0
		(LH)		0.311	0.744	1.591	0.029	0.043	0.063	E	1.0				
	D → Y	(HL)		0.378	0.616	1.305	0.022	0.029	0.043						
		(LH)		0.349	0.646	1.446	0.029	0.043	0.063						
	E → Y	(HL)		0.379	0.618	1.350	0.022	0.029	0.043						
		(LH)		0.475	0.795	1.719	0.029	0.043	0.063						
F446	A → Y	(HL)		0.265	0.451	0.903	0.011	0.015	0.023	A	1.0	Y	21		
		(LH)		0.356	0.641	1.441	0.015	0.022	0.033						
	B → Y	(HL)		0.281	0.471	0.939	0.011	0.015	0.023					B	1.0
		(LH)		0.344	0.653	1.500	0.015	0.022	0.033					C	1.0
	C → Y	(HL)		0.295	0.511	1.013	0.011	0.015	0.023					D	1.0
		(LH)		0.316	0.773	1.668	0.015	0.022	0.033	E	1.0				
	D → Y	(HL)		0.387	0.649	1.378	0.011	0.015	0.023						
		(LH)		0.357	0.677	1.527	0.015	0.022	0.033						
	E → Y	(HL)		0.388	0.651	1.423	0.011	0.015	0.023						
		(LH)		0.481	0.823	1.796	0.015	0.022	0.033						

Chapter 2 Function Block

Function	1-1-1-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L447	5										
x1	F447	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout				
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.								
L447	A → Y	(HL)		0.262	0.430	0.856	0.022	0.029	0.043	A	1.0	Y	10				
		(LH)		0.349	0.612	1.362	0.030	0.044	0.064								
	B → Y	(HL)		0.278	0.451	0.891	0.022	0.029	0.043					B	1.0		
		(LH)		0.337	0.623	1.420	0.030	0.044	0.064								
	C → Y	(HL)		0.290	0.492	0.967	0.022	0.029	0.043							C	1.0
		(LH)		0.304	0.818	1.719	0.030	0.044	0.064								
	D → Y	(HL)		0.418	0.710	1.582	0.022	0.029	0.043	D	1.0						
		(LH)		0.349	0.649	1.454	0.030	0.044	0.064								
	E → Y	(HL)		0.446	0.749	1.713	0.022	0.029	0.043			E	1.0				
		(LH)		0.472	0.798	1.736	0.030	0.044	0.064								
	F → Y	(HL)		0.438	0.745	1.722	0.022	0.029	0.043					F	1.0		
		(LH)		0.518	0.855	1.831	0.030	0.044	0.064								
F447	A → Y	(HL)		0.264	0.450	0.903	0.011	0.015	0.023	A	1.0					Y	21
		(LH)		0.352	0.636	1.433	0.015	0.022	0.033								
	B → Y	(HL)		0.280	0.471	0.939	0.011	0.015	0.023			B	1.0				
		(LH)		0.340	0.647	1.493	0.015	0.022	0.033								
	C → Y	(HL)		0.301	0.527	1.040	0.011	0.015	0.023					C	1.0		
		(LH)		0.313	0.861	1.818	0.015	0.022	0.033								
	D → Y	(HL)		0.437	0.760	1.689	0.011	0.015	0.023	D	1.0						
		(LH)		0.364	0.690	1.549	0.015	0.022	0.033								
	E → Y	(HL)		0.466	0.801	1.823	0.011	0.015	0.023			E	1.0				
		(LH)		0.492	0.844	1.837	0.015	0.022	0.033								
	F → Y	(HL)		0.458	0.797	1.832	0.011	0.015	0.023					F	1.0		
		(LH)		0.538	0.902	1.932	0.015	0.022	0.033								

Chapter 2 Function Block

Function	1-1-2-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L448	5										
x1	F448	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L448	A → Y	(HL)		0.254	0.419	0.838	0.022	0.029	0.043	A	1.0	Y	10
		(LH)		0.343	0.602	1.346	0.029	0.043	0.063				
	B → Y	(HL)		0.270	0.440	0.873	0.022	0.029	0.043	B	1.0		
		(LH)		0.331	0.613	1.405	0.029	0.043	0.063				
	C → Y	(HL)		0.363	0.587	1.246	0.022	0.029	0.043	C	1.0		
		(LH)		0.359	0.723	1.590	0.029	0.043	0.063				
	D → Y	(HL)		0.346	0.571	1.252	0.022	0.029	0.043	D	1.0		
		(LH)		0.400	0.791	1.711	0.029	0.043	0.063				
	E → Y	(HL)		0.411	0.691	1.496	0.022	0.029	0.043	E	1.0		
		(LH)		0.377	0.834	1.820	0.029	0.043	0.063				
	F → Y	(HL)		0.391	0.675	1.500	0.022	0.029	0.043	F	1.0		
		(LH)		0.419	0.905	1.941	0.029	0.043	0.063				
F448	A → Y	(HL)		0.264	0.450	0.902	0.011	0.015	0.023	A	1.0	Y	21
		(LH)		0.352	0.635	1.432	0.015	0.022	0.033				
	B → Y	(HL)		0.280	0.470	0.938	0.011	0.015	0.023	B	1.0		
		(LH)		0.340	0.647	1.491	0.015	0.022	0.033				
	C → Y	(HL)		0.383	0.636	1.348	0.011	0.015	0.023	C	1.0		
		(LH)		0.379	0.779	1.707	0.015	0.022	0.033				
	D → Y	(HL)		0.365	0.620	1.353	0.011	0.015	0.023	D	1.0		
		(LH)		0.420	0.846	1.828	0.015	0.022	0.033				
	E → Y	(HL)		0.432	0.741	1.597	0.011	0.015	0.023	E	1.0		
		(LH)		0.398	0.890	1.939	0.015	0.022	0.033				
	F → Y	(HL)		0.411	0.724	1.601	0.011	0.015	0.023	F	1.0		
		(LH)		0.441	0.960	2.059	0.015	0.022	0.033				



Chapter 2 Function Block

Function	3-3-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F449	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-	-	-			
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F449	A	→	Y	(HL)	0.380	0.731	1.603	0.011	0.015	0.023	A	1.0	Y	21
				(LH)	0.335	0.952	2.044	0.015	0.022	0.033	B	1.0		
	B	→	Y	(HL)	0.408	0.771	1.738	0.011	0.015	0.023	C	1.0		
				(LH)	0.424	1.092	2.309	0.015	0.022	0.033	D	1.0		
	C	→	Y	(HL)	0.401	0.766	1.747	0.011	0.015	0.023	E	1.0		
				(LH)	0.455	1.155	2.420	0.015	0.022	0.033	F	1.0		
	D	→	Y	(HL)	0.461	0.944	2.149	0.011	0.015	0.023	G	1.0		
				(LH)	0.379	1.103	2.357	0.015	0.022	0.033	H	1.0		
	E	→	Y	(HL)	0.489	0.984	2.280	0.011	0.015	0.023	I	1.0		
				(LH)	0.468	1.245	2.616	0.015	0.022	0.033	J	1.0		
	F	→	Y	(HL)	0.481	0.980	2.289	0.011	0.015	0.023	K	1.0		
				(LH)	0.502	1.310	2.727	0.015	0.022	0.033	L	1.0		
	G	→	Y	(HL)	0.410	0.777	1.693	0.011	0.015	0.023				
				(LH)	0.328	0.889	1.898	0.015	0.022	0.033				
	H	→	Y	(HL)	0.439	0.817	1.828	0.011	0.015	0.023				
				(LH)	0.408	1.023	2.154	0.015	0.022	0.033				
I	→	Y	(HL)	0.431	0.813	1.837	0.011	0.015	0.023					
			(LH)	0.436	1.083	2.259	0.015	0.022	0.033					
J	→	Y	(HL)	0.494	0.986	2.230	0.011	0.015	0.023					
			(LH)	0.362	1.040	2.211	0.015	0.022	0.033					
K	→	Y	(HL)	0.521	1.027	2.361	0.011	0.015	0.023					
			(LH)	0.443	1.177	2.462	0.015	0.022	0.033					
L	→	Y	(HL)	0.514	1.023	2.370	0.011	0.015	0.023					
			(LH)	0.474	1.238	2.566	0.015	0.022	0.033					

Chapter 2 Function Block

Function	3-3-3-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L460	6										
x1	F460	7										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L460	A → Y	(HL)		0.373	0.629	1.412	0.022	0.029	0.043	A	1.0	Y	10
		(LH)		0.301	0.534	1.166	0.029	0.043	0.063				
	B → Y	(HL)		0.372	0.639	1.475	0.022	0.029	0.043	B	1.0		
		(LH)		0.333	0.571	1.231	0.029	0.043	0.063				
	C → Y	(HL)		0.388	0.658	1.532	0.022	0.029	0.043	C	1.0		
		(LH)		0.383	0.625	1.329	0.029	0.043	0.063				
	D → Y	(HL)		0.441	0.815	1.778	0.022	0.029	0.043	D	1.0		
		(LH)		0.350	0.957	2.008	0.029	0.043	0.063				
	E → Y	(HL)		0.469	0.855	1.913	0.022	0.029	0.043	E	1.0		
		(LH)		0.432	1.093	2.268	0.029	0.043	0.063				
	F → Y	(HL)		0.461	0.851	1.922	0.022	0.029	0.043	F	1.0		
		(LH)		0.461	1.152	2.372	0.029	0.043	0.063				
	G → Y	(HL)		0.545	0.970	2.189	0.022	0.029	0.044	G	1.0		
		(LH)		0.371	1.056	2.224	0.029	0.043	0.063				
	H → Y	(HL)		0.572	1.010	2.319	0.022	0.029	0.044	H	1.0		
		(LH)		0.452	1.191	2.476	0.029	0.043	0.063				
	I → Y	(HL)		0.565	1.006	2.328	0.022	0.029	0.043	I	1.0		
		(LH)		0.481	1.251	2.579	0.029	0.043	0.063				
F460	A → Y	(HL)		0.394	0.679	1.519	0.011	0.015	0.023	A	1.0	Y	21
		(LH)		0.313	0.569	1.250	0.015	0.022	0.033				
	B → Y	(HL)		0.392	0.689	1.582	0.011	0.015	0.023	B	1.0		
		(LH)		0.344	0.605	1.315	0.015	0.022	0.033				
	C → Y	(HL)		0.409	0.710	1.641	0.011	0.015	0.023	C	1.0		
		(LH)		0.393	0.658	1.411	0.015	0.022	0.033				
	D → Y	(HL)		0.450	0.858	1.883	0.011	0.015	0.023	D	1.0		
		(LH)		0.353	0.990	2.090	0.015	0.022	0.033				
	E → Y	(HL)		0.476	0.898	2.015	0.011	0.015	0.023	E	1.0		
		(LH)		0.435	1.123	2.344	0.015	0.022	0.033				
	F → Y	(HL)		0.469	0.893	2.024	0.011	0.015	0.023	F	1.0		
		(LH)		0.464	1.184	2.449	0.015	0.022	0.033				
	G → Y	(HL)		0.551	1.003	2.269	0.011	0.015	0.023	G	1.0		
		(LH)		0.373	1.080	2.295	0.015	0.022	0.033				
	H → Y	(HL)		0.580	1.045	2.403	0.011	0.015	0.023	H	1.0		
		(LH)		0.457	1.218	2.550	0.015	0.022	0.033				
	I → Y	(HL)		0.573	1.041	2.412	0.011	0.015	0.023	I	1.0		
		(LH)		0.486	1.279	2.655	0.015	0.022	0.033				

Chapter 2 Function Block

Function	1-1-4-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L464	5										
x1	F464	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L464	A → Y	(HL)		0.254	0.419	0.838	0.022	0.029	0.043	A	1.0	Y	10		
		(LH)		0.343	0.602	1.346	0.029	0.043	0.063						
	B → Y	(HL)		0.270	0.440	0.874	0.022	0.029	0.043					B	1.0
		(LH)		0.331	0.613	1.405	0.029	0.043	0.063					D	1.0
	C → Y	(HL)		0.424	0.721	1.670	0.022	0.029	0.043					E	1.0
		(LH)		0.292	0.515	1.131	0.029	0.043	0.063					F	1.0
	D → Y	(HL)		0.437	0.752	1.785	0.022	0.029	0.043						
		(LH)		0.322	0.550	1.195	0.029	0.043	0.063						
	E → Y	(HL)		0.477	0.806	1.925	0.022	0.029	0.043						
		(LH)		0.365	0.596	1.281	0.029	0.043	0.063						
	F → Y	(HL)		0.474	0.805	1.934	0.022	0.029	0.043						
		(LH)		0.377	0.611	1.302	0.029	0.043	0.063						
F464	A → Y	(HL)		0.266	0.452	0.905	0.011	0.015	0.023	A	1.0	Y	21		
		(LH)		0.358	0.644	1.446	0.015	0.022	0.033						
	B → Y	(HL)		0.282	0.473	0.941	0.011	0.015	0.023					B	1.0
		(LH)		0.346	0.656	1.505	0.015	0.022	0.033					C	1.0
	C → Y	(HL)		0.438	0.764	1.768	0.011	0.015	0.023					D	1.0
		(LH)		0.299	0.544	1.207	0.015	0.022	0.033					E	1.0
	D → Y	(HL)		0.450	0.794	1.883	0.011	0.015	0.023	F	1.0				
		(LH)		0.329	0.578	1.271	0.015	0.022	0.033						
	E → Y	(HL)		0.492	0.851	2.026	0.011	0.015	0.023						
		(LH)		0.373	0.626	1.360	0.015	0.022	0.033						
	F → Y	(HL)		0.489	0.849	2.035	0.011	0.015	0.023						
		(LH)		0.386	0.641	1.380	0.015	0.022	0.033						

Chapter 2 Function Block

Function	1-1-1-1-2-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F465	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F465	A → Y	(HL)		0.294	0.482	0.965	0.011	0.015	0.023	A	1.0	Y	21	
		(LH)		0.501	0.858	1.968	0.015	0.022	0.033		B			1.0
	B → Y	(HL)		0.309	0.503	1.005	0.011	0.015	0.023		C			1.0
		(LH)		0.517	0.922	2.128	0.015	0.022	0.033		D			1.0
	C → Y	(HL)		0.322	0.521	1.045	0.011	0.015	0.023		E			1.0
		(LH)		0.549	1.010	2.274	0.015	0.022	0.033		F			1.0
	D → Y	(HL)		0.295	0.511	1.013	0.011	0.015	0.023					
		(LH)		0.316	0.777	1.675	0.015	0.022	0.033					
	E → Y	(HL)		0.388	0.650	1.380	0.011	0.015	0.023					
		(LH)		0.359	0.679	1.530	0.015	0.022	0.033					
	F → Y	(HL)		0.390	0.653	1.427	0.011	0.015	0.023					
		(LH)		0.487	0.831	1.808	0.015	0.022	0.033					

Chapter 2 Function Block

Function	4-4-4-4-Input AND-NOR											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F466	10										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F466	A → Y	(HL)		0.473	0.889	2.017	0.011	0.015	0.023	A	1.0	Y	21
		(LH)		0.392	1.077	2.297	0.015	0.022	0.033	B	1.0		
	B → Y	(HL)		0.485	0.920	2.130	0.011	0.015	0.023	C	1.0		
		(LH)		0.430	1.154	2.440	0.015	0.022	0.033	D	1.0		
	C → Y	(HL)		0.527	0.975	2.270	0.011	0.015	0.023	E	1.0		
		(LH)		0.494	1.288	2.689	0.015	0.022	0.033	F	1.0		
	D → Y	(HL)		0.524	0.974	2.280	0.011	0.015	0.023	G	1.0		
		(LH)		0.518	1.346	2.787	0.015	0.022	0.033	H	1.0		
	E → Y	(HL)		0.727	1.358	3.222	0.011	0.015	0.023	I	1.0		
		(LH)		0.465	1.317	2.778	0.015	0.022	0.033	J	1.0		
	F → Y	(HL)		0.741	1.391	3.331	0.011	0.015	0.023	K	1.0		
		(LH)		0.505	1.396	2.921	0.015	0.022	0.033	L	1.0		
	G → Y	(HL)		0.787	1.447	3.471	0.011	0.015	0.023	M	1.0		
		(LH)		0.572	1.530	3.167	0.015	0.022	0.033	N	1.0		
	H → Y	(HL)		0.785	1.446	3.480	0.011	0.015	0.023	O	1.0		
		(LH)		0.598	1.589	3.266	0.015	0.022	0.033	P	1.0		
	I → Y	(HL)		0.504	0.940	2.115	0.011	0.015	0.023				
		(LH)		0.375	0.995	2.106	0.015	0.022	0.033				
	J → Y	(HL)		0.516	0.971	2.227	0.011	0.015	0.023				
		(LH)		0.411	1.069	2.246	0.015	0.022	0.033				
	K → Y	(HL)		0.558	1.025	2.367	0.011	0.015	0.023				
		(LH)		0.469	1.197	2.486	0.015	0.022	0.033				
	L → Y	(HL)		0.555	1.024	2.377	0.011	0.015	0.023				
		(LH)		0.490	1.251	2.578	0.015	0.022	0.033				
M → Y	(HL)		0.762	1.402	3.307	0.011	0.015	0.023					
	(LH)		0.443	1.247	2.608	0.015	0.022	0.033					
N → Y	(HL)		0.776	1.435	3.415	0.011	0.015	0.023					
	(LH)		0.481	1.324	2.751	0.015	0.022	0.033					
O → Y	(HL)		0.822	1.492	3.555	0.011	0.015	0.023					
	(LH)		0.544	1.456	2.990	0.015	0.022	0.033					
P → Y	(HL)		0.820	1.490	3.563	0.011	0.015	0.023					
	(LH)		0.557	1.493	3.055	0.015	0.022	0.033					

[MEMO]

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## 2.6 OR-NAND

[MEMO]

Chapter 2 Function Block

Function	1-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L430	4										
x1	F430	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L430	A → Y	(HL)		0.119	0.159	0.287	0.034	0.049	0.082	A	1.0	Y	9
		(LH)		0.081	0.127	0.231	0.029	0.042	0.061				
	B → Y	(HL)		0.264	0.436	0.906	0.034	0.050	0.082	B	1.0		
		(LH)		0.369	0.641	1.428	0.029	0.043	0.062				
	C → Y	(HL)		0.280	0.456	0.941	0.034	0.050	0.082	C	1.0		
		(LH)		0.356	0.653	1.487	0.029	0.043	0.062				
	D → Y	(HL)		0.286	0.464	0.958	0.034	0.050	0.082	D	1.0		
		(LH)		0.358	0.610	1.357	0.029	0.043	0.062				
	E → Y	(HL)		0.303	0.484	0.994	0.034	0.050	0.082	E	1.0		
		(LH)		0.345	0.622	1.417	0.029	0.043	0.062				
F430	A → Y	(HL)		0.111	0.154	0.300	0.017	0.025	0.041	A	2.1	Y	18
		(LH)		0.093	0.142	0.257	0.014	0.021	0.030				
	B → Y	(HL)		0.297	0.503	1.043	0.017	0.025	0.041	B	1.0		
		(LH)		0.394	0.699	1.570	0.014	0.021	0.032				
	C → Y	(HL)		0.313	0.523	1.079	0.017	0.025	0.041	C	1.0		
		(LH)		0.381	0.711	1.629	0.014	0.021	0.032				
	D → Y	(HL)		0.322	0.532	1.097	0.017	0.025	0.041	D	1.0		
		(LH)		0.383	0.667	1.496	0.014	0.021	0.032				
	E → Y	(HL)		0.338	0.554	1.134	0.017	0.025	0.041	E	1.0		
		(LH)		0.370	0.679	1.555	0.014	0.021	0.032				



Chapter 2 Function Block

Function	1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L431	2										
x1	F431	3										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L431	A → Y	(HL)		0.112	0.229	0.431	0.028	0.052	0.085	A	1.0	Y	3
		(LH)		0.083	0.131	0.236	0.029	0.043	0.061				
	B → Y	(HL)		0.119	0.165	0.337	0.034	0.050	0.081	B	1.0		
		(LH)		0.191	0.272	0.561	0.057	0.084	0.123				
	C → Y	(HL)		0.153	0.227	0.476	0.035	0.052	0.085	C	1.0		
		(LH)		0.207	0.344	0.713	0.057	0.084	0.123				
F431	A → Y	(HL)		0.107	0.189	0.342	0.015	0.026	0.042	A	2.1	Y	8
		(LH)		0.073	0.129	0.230	0.015	0.022	0.031				
	B → Y	(HL)		0.127	0.192	0.396	0.018	0.026	0.042	B	2.0		
		(LH)		0.172	0.283	0.587	0.026	0.039	0.059				
	C → Y	(HL)		0.127	0.192	0.396	0.018	0.026	0.042	C	2.0		
		(LH)		0.172	0.283	0.587	0.026	0.039	0.059				

Chapter 2 Function Block

Function	1-1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L432	2										
x1	F432	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
L432	A → Y	(HL)		0.153	0.300	0.651	0.041	0.072	0.125	A	1.0	Y	2		
		(LH)		0.097	0.163	0.297	0.029	0.042	0.061						
	B → Y	(HL)		0.144	0.310	0.714	0.041	0.072	0.125					B	1.0
		(LH)		0.120	0.193	0.355	0.028	0.042	0.061						
	C → Y	(HL)		0.174	0.278	0.649	0.047	0.072	0.125	C	1.0				
		(LH)		0.239	0.373	0.766	0.052	0.078	0.117						
	D → Y	(HL)		0.199	0.326	0.762	0.047	0.072	0.125	D	1.0				
		(LH)		0.230	0.388	0.816	0.052	0.078	0.117						
F432	A → Y	(HL)		0.147	0.272	0.605	0.020	0.036	0.063	A	2.1	Y	5		
		(LH)		0.107	0.175	0.322	0.014	0.021	0.031						
	B → Y	(HL)		0.146	0.272	0.605	0.020	0.036	0.063					B	2.1
		(LH)		0.107	0.175	0.322	0.014	0.021	0.031						
	C → Y	(HL)		0.187	0.301	0.703	0.024	0.036	0.063	C	2.0				
		(LH)		0.234	0.380	0.786	0.026	0.040	0.060						
	D → Y	(HL)		0.187	0.301	0.703	0.024	0.036	0.063	D	2.0				
		(LH)		0.234	0.380	0.786	0.026	0.040	0.060						

Chapter 2 Function Block

Function	1-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F433	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F433	A	→	Y	(HL)	0.089	0.204	0.368	0.014	0.027	0.045	A	2.1	Y	3
				(LH)	0.063	0.112	0.201	0.015	0.022	0.031				
	B	→	Y	(HL)	0.135	0.193	0.394	0.018	0.027	0.045	B	2.0		
				(LH)	0.277	0.432	0.926	0.040	0.060	0.091				
	C	→	Y	(HL)	0.152	0.224	0.468	0.018	0.027	0.044	C	2.0		
				(LH)	0.307	0.502	1.066	0.040	0.060	0.090				
	D	→	Y	(HL)	0.136	0.193	0.394	0.018	0.027	0.045	D	2.1		
				(LH)	0.279	0.433	0.929	0.040	0.060	0.091				

Chapter 2 Function Block

Function	2-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F434	4										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F434	A	→	Y	(HL)	0.137	0.245	0.472	0.014	0.026	0.042	A	2.1	Y	4
				(LH)	0.128	0.238	0.499	0.026	0.039	0.059				
	B	→	Y	(HL)	0.137	0.245	0.472	0.014	0.026	0.042	B	2.1		
				(LH)	0.128	0.238	0.499	0.026	0.039	0.059				
	C	→	Y	(HL)	0.153	0.269	0.559	0.013	0.026	0.042	C	2.0		
				(LH)	0.234	0.418	0.863	0.026	0.039	0.059				
	D	→	Y	(HL)	0.153	0.269	0.559	0.013	0.026	0.042	D	2.0		
				(LH)	0.234	0.418	0.863	0.026	0.039	0.059				

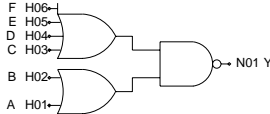
Chapter 2 Function Block

Function	1-5-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L439	5										
x1	F439	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L439	A → Y	(HL)		0.119	0.159	0.287	0.034	0.049	0.082	A	1.0	Y	9
		(LH)		0.081	0.127	0.231	0.029	0.042	0.061				
	B → Y	(HL)		0.264	0.437	0.908	0.034	0.050	0.082	B	1.0	C	1.0
		(LH)		0.366	0.637	1.422	0.029	0.043	0.062				
	C → Y	(HL)		0.280	0.457	0.942	0.034	0.050	0.082	C	1.0	D	1.0
		(LH)		0.353	0.648	1.481	0.029	0.043	0.062				
	D → Y	(HL)		0.319	0.500	1.027	0.034	0.050	0.082	D	1.0	E	1.0
		(LH)		0.488	0.797	1.802	0.029	0.043	0.063				
	E → Y	(HL)		0.334	0.521	1.067	0.034	0.050	0.082	E	1.0	F	1.0
		(LH)		0.503	0.862	1.963	0.029	0.043	0.063				
	F → Y	(HL)		0.347	0.538	1.104	0.034	0.050	0.082	F	1.0		
		(LH)		0.535	0.950	2.109	0.029	0.043	0.063				
F439	A → Y	(HL)		0.112	0.155	0.301	0.017	0.025	0.041	A	2.1	Y	18
		(LH)		0.093	0.142	0.257	0.014	0.021	0.030				
	B → Y	(HL)		0.293	0.498	1.038	0.017	0.025	0.041	B	1.0	C	1.0
		(LH)		0.386	0.688	1.551	0.014	0.021	0.032				
	C → Y	(HL)		0.309	0.519	1.074	0.017	0.025	0.041	C	1.0	D	1.0
		(LH)		0.374	0.699	1.610	0.014	0.021	0.032				
	D → Y	(HL)		0.350	0.563	1.157	0.017	0.025	0.041	D	1.0	E	1.0
		(LH)		0.518	0.863	1.955	0.014	0.022	0.032				
	E → Y	(HL)		0.365	0.584	1.198	0.017	0.025	0.041	E	1.0	F	1.0
		(LH)		0.534	0.927	2.115	0.014	0.022	0.032				
	F → Y	(HL)		0.379	0.603	1.241	0.017	0.025	0.041	F	1.0		
		(LH)		0.566	1.015	2.261	0.014	0.022	0.032				

Chapter 2 Function Block

Function	2-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L450	5										
x1	F450	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
												
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L450	A → Y	(HL)		0.152	0.233	0.494	0.035	0.052	0.085	A	1.0	Y	3
		(LH)		0.205	0.341	0.709	0.057	0.084	0.123				
	B → Y	(HL)		0.119	0.170	0.350	0.034	0.050	0.082	B	1.0	C	1.0
		(LH)		0.188	0.269	0.557	0.057	0.084	0.123				
	C → Y	(HL)		0.262	0.524	1.097	0.028	0.052	0.086	C	1.0	D	1.0
		(LH)		0.348	0.615	1.371	0.029	0.043	0.063				
	D → Y	(HL)		0.278	0.545	1.132	0.028	0.052	0.086	D	1.0	E	1.0
		(LH)		0.335	0.626	1.430	0.029	0.043	0.063				
	E → Y	(HL)		0.294	0.562	1.162	0.028	0.052	0.086	E	1.0	F	1.0
		(LH)		0.346	0.598	1.323	0.029	0.043	0.063				
	F → Y	(HL)		0.310	0.583	1.198	0.028	0.052	0.086	F	1.0		
		(LH)		0.334	0.610	1.383	0.029	0.043	0.063				
F450	A → Y	(HL)		0.128	0.205	0.428	0.018	0.026	0.043	A	2.0	Y	7
		(LH)		0.171	0.282	0.586	0.026	0.039	0.059				
	B → Y	(HL)		0.128	0.205	0.428	0.018	0.026	0.043	B	2.0	C	1.0
		(LH)		0.171	0.282	0.586	0.026	0.039	0.059				
	C → Y	(HL)		0.288	0.538	1.122	0.015	0.026	0.043	C	1.0	D	1.0
		(LH)		0.372	0.678	1.518	0.015	0.023	0.035				
	D → Y	(HL)		0.304	0.558	1.158	0.015	0.026	0.043	D	1.0	E	1.0
		(LH)		0.360	0.690	1.578	0.015	0.023	0.035				
	E → Y	(HL)		0.313	0.569	1.178	0.015	0.026	0.044	E	1.0	F	1.0
		(LH)		0.360	0.645	1.442	0.015	0.023	0.035				
	F → Y	(HL)		0.329	0.590	1.215	0.015	0.026	0.044	F	1.0		
		(LH)		0.348	0.657	1.501	0.015	0.023	0.035				

Chapter 2 Function Block

Function	4-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L451	7										
x1	F451	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L451	A → Y	(HL)		0.260	0.442	0.924	0.034	0.050	0.083	A	1.0	Y	9
		(LH)		0.341	0.599	1.347	0.029	0.043	0.063	B	1.0		
	B → Y	(HL)		0.277	0.462	0.960	0.034	0.050	0.083	C	1.0		
		(LH)		0.328	0.610	1.406	0.029	0.043	0.063	D	1.0		
	C → Y	(HL)		0.293	0.479	0.989	0.034	0.050	0.083	E	1.0		
		(LH)		0.340	0.584	1.301	0.029	0.043	0.063	F	1.0		
	D → Y	(HL)		0.309	0.500	1.025	0.034	0.050	0.083	G	1.0		
		(LH)		0.328	0.596	1.361	0.029	0.043	0.063	H	1.0		
	E → Y	(HL)		0.266	0.442	0.919	0.034	0.050	0.082				
		(LH)		0.367	0.639	1.426	0.029	0.043	0.063				
	F → Y	(HL)		0.282	0.462	0.954	0.034	0.050	0.082				
		(LH)		0.355	0.651	1.485	0.029	0.043	0.063				
	G → Y	(HL)		0.290	0.472	0.974	0.034	0.050	0.082				
		(LH)		0.361	0.614	1.365	0.029	0.043	0.063				
	H → Y	(HL)		0.306	0.492	1.010	0.034	0.050	0.082				
		(LH)		0.348	0.626	1.424	0.029	0.043	0.063				
F451	A → Y	(HL)		0.299	0.509	1.055	0.017	0.025	0.042	A	1.0	Y	17
		(LH)		0.395	0.702	1.573	0.015	0.022	0.032	B	1.0		
	B → Y	(HL)		0.315	0.529	1.091	0.017	0.025	0.042	C	1.0		
		(LH)		0.383	0.713	1.632	0.015	0.022	0.032	D	1.0		
	C → Y	(HL)		0.327	0.542	1.114	0.017	0.025	0.042	E	1.0		
		(LH)		0.390	0.678	1.514	0.015	0.022	0.032	F	1.0		
	D → Y	(HL)		0.344	0.565	1.154	0.017	0.025	0.042	G	1.0		
		(LH)		0.377	0.690	1.573	0.015	0.022	0.032	H	1.0		
	E → Y	(HL)		0.301	0.510	1.057	0.017	0.025	0.042				
		(LH)		0.397	0.704	1.579	0.014	0.022	0.032				
	F → Y	(HL)		0.317	0.530	1.093	0.017	0.025	0.042				
		(LH)		0.385	0.716	1.638	0.014	0.022	0.032				
	G → Y	(HL)		0.326	0.540	1.111	0.017	0.025	0.042				
		(LH)		0.386	0.672	1.504	0.014	0.022	0.032				
	H → Y	(HL)		0.342	0.561	1.148	0.017	0.025	0.042				
		(LH)		0.373	0.684	1.563	0.014	0.022	0.032				

Chapter 2 Function Block

Function	1-1-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L452	4										
x1	F452	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L452	A → Y	(HL)		0.320	0.536	1.101	0.023	0.031	0.047	A	1.0	Y	10
		(LH)		0.254	0.425	0.866	0.029	0.042	0.061				
	B → Y	(HL)		0.340	0.715	1.543	0.023	0.031	0.047	B	1.0		
		(LH)		0.254	0.468	0.968	0.029	0.042	0.061				
	C → Y	(HL)		0.363	0.631	1.382	0.023	0.031	0.047	C	1.0		
		(LH)		0.493	0.805	1.768	0.029	0.042	0.061				
	D → Y	(HL)		0.399	0.699	1.548	0.023	0.031	0.047	D	1.0		
		(LH)		0.552	0.964	2.087	0.029	0.042	0.061				
	E → Y	(HL)		0.405	0.709	1.578	0.023	0.031	0.047	E	1.0		
		(LH)		0.555	0.986	2.133	0.029	0.042	0.061				
F452	A → Y	(HL)		0.349	0.603	1.246	0.012	0.017	0.025	A	1.0	Y	22
		(LH)		0.255	0.435	0.889	0.015	0.022	0.031				
	B → Y	(HL)		0.365	0.779	1.686	0.012	0.017	0.025	B	1.0		
		(LH)		0.252	0.481	0.999	0.015	0.022	0.031				
	C → Y	(HL)		0.388	0.694	1.522	0.012	0.017	0.025	C	1.0		
		(LH)		0.502	0.828	1.815	0.015	0.022	0.031				
	D → Y	(HL)		0.424	0.762	1.688	0.012	0.017	0.025	D	1.0		
		(LH)		0.561	0.987	2.134	0.015	0.022	0.031				
	E → Y	(HL)		0.430	0.772	1.720	0.012	0.017	0.026	E	1.0		
		(LH)		0.564	1.009	2.180	0.015	0.022	0.031				



Chapter 2 Function Block

Function	1-1-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L453	5										
x1	F453	6										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L453	A → Y	(HL)		0.198	0.317	0.685	0.047	0.072	0.125	A	1.0	Y	3		
		(LH)		0.117	0.196	0.360	0.029	0.042	0.061						
	B → Y	(HL)		0.196	0.328	0.747	0.047	0.072	0.124					B	1.0
		(LH)		0.140	0.226	0.417	0.028	0.042	0.061					D	1.0
	C → Y	(HL)		0.384	0.648	1.420	0.047	0.072	0.125					E	1.0
		(LH)		0.443	0.761	1.657	0.029	0.043	0.063					F	1.0
	D → Y	(HL)		0.400	0.668	1.455	0.047	0.072	0.125						
		(LH)		0.431	0.772	1.716	0.029	0.043	0.063						
	E → Y	(HL)		0.404	0.673	1.469	0.047	0.072	0.125						
		(LH)		0.431	0.727	1.582	0.029	0.043	0.063						
	F → Y	(HL)		0.420	0.694	1.505	0.047	0.072	0.125						
		(LH)		0.418	0.739	1.642	0.029	0.043	0.063						
F453	A → Y	(HL)		0.130	0.200	0.434	0.024	0.036	0.063	A	2.1	Y	10		
		(LH)		0.103	0.165	0.292	0.015	0.022	0.032						
	B → Y	(HL)		0.144	0.220	0.498	0.024	0.036	0.063					B	2.1
		(LH)		0.121	0.183	0.334	0.015	0.022	0.032					C	1.0
	C → Y	(HL)		0.318	0.553	1.180	0.024	0.037	0.063					D	1.0
		(LH)		0.407	0.726	1.617	0.015	0.023	0.034					E	1.0
	D → Y	(HL)		0.334	0.573	1.216	0.024	0.037	0.063	F	1.0				
		(LH)		0.394	0.738	1.676	0.015	0.023	0.034						
	E → Y	(HL)		0.343	0.582	1.234	0.024	0.037	0.063						
		(LH)		0.397	0.695	1.545	0.015	0.023	0.034						
	F → Y	(HL)		0.359	0.603	1.271	0.024	0.037	0.063						
		(LH)		0.384	0.707	1.605	0.015	0.023	0.034						

Chapter 2 Function Block

Function	4-4-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F457	10										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-	-	-			
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F457	A → Y	(HL)		0.510	0.826	1.716	0.014	0.019	0.030	A	1.0	Y	19
		(LH)		0.454	0.795	1.785	0.015	0.022	0.034	B	1.0		
	B → Y	(HL)		0.525	0.845	1.748	0.014	0.019	0.030	C	1.0		
		(LH)		0.442	0.807	1.844	0.015	0.022	0.034	D	1.0		
	C → Y	(HL)		0.555	0.885	1.830	0.014	0.019	0.030	E	1.0		
		(LH)		0.435	0.751	1.693	0.015	0.023	0.034	F	1.0		
	D → Y	(HL)		0.570	0.905	1.865	0.014	0.019	0.030	G	1.0		
		(LH)		0.423	0.763	1.752	0.015	0.023	0.034	H	1.0		
	E → Y	(HL)		0.574	1.311	2.732	0.014	0.021	0.034	I	1.0		
		(LH)		0.495	0.906	2.023	0.015	0.023	0.035	J	1.0		
	F → Y	(HL)		0.587	1.328	2.760	0.014	0.021	0.034	K	1.0		
		(LH)		0.483	0.918	2.082	0.015	0.023	0.035	L	1.0		
	G → Y	(HL)		0.624	1.401	2.908	0.014	0.022	0.034				
		(LH)		0.479	0.866	1.936	0.015	0.023	0.035				
	H → Y	(HL)		0.637	1.419	2.939	0.014	0.021	0.034				
		(LH)		0.466	0.878	1.995	0.015	0.023	0.035				
I → Y	(HL)		0.635	1.439	2.964	0.014	0.021	0.034					
	(LH)		0.525	1.006	2.254	0.015	0.024	0.037					
J → Y	(HL)		0.647	1.456	2.993	0.014	0.021	0.034					
	(LH)		0.513	1.018	2.313	0.015	0.024	0.037					
K → Y	(HL)		0.673	1.518	3.128	0.015	0.022	0.034					
	(LH)		0.491	0.937	2.124	0.015	0.024	0.037					
L → Y	(HL)		0.688	1.536	3.159	0.015	0.022	0.034					
	(LH)		0.478	0.949	2.184	0.015	0.024	0.037					

Chapter 2 Function Block

Function	1-1-1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F458	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F458	A → Y	(HL)		0.181	0.342	0.789	0.029	0.049	0.087	A	2.1	Y	2
		(LH)		0.103	0.178	0.328	0.015	0.021	0.031				
	B → Y	(HL)		0.207	0.401	0.968	0.029	0.049	0.086	B	2.0		
		(LH)		0.140	0.222	0.414	0.015	0.022	0.031				
	C → Y	(HL)		0.210	0.427	1.039	0.029	0.050	0.086	C	2.0		
		(LH)		0.156	0.245	0.452	0.015	0.022	0.032				
	D → Y	(HL)		0.278	0.458	1.107	0.032	0.049	0.086	D	2.0		
		(LH)		0.291	0.470	0.957	0.027	0.041	0.061				
	E → Y	(HL)		0.278	0.458	1.107	0.032	0.049	0.086	E	2.0		
		(LH)		0.291	0.470	0.957	0.027	0.041	0.061				

Chapter 2 Function Block

Function	1-1-1-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L459	5										
x1	F459	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output					
	Path			t LDO (ns)			t 1										
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout				
L459	A → Y	(HL)		0.360	0.608	1.301	0.023	0.031	0.047	A	1.0	Y	10				
		(LH)		0.242	0.415	0.864	0.029	0.042	0.061								
	B → Y	(HL)		0.347	0.592	1.308	0.023	0.031	0.047								
		(LH)		0.274	0.451	0.926	0.029	0.042	0.061								
	C → Y	(HL)		0.345	0.725	1.561	0.023	0.031	0.047					B	1.0		
		(LH)		0.257	0.471	0.973	0.029	0.042	0.061								
	D → Y	(HL)		0.369	0.641	1.399	0.023	0.031	0.047	C	1.0						
		(LH)		0.499	0.814	1.781	0.028	0.042	0.061								
	E → Y	(HL)		0.405	0.709	1.565	0.023	0.031	0.047			D	1.0				
		(LH)		0.558	0.973	2.100	0.028	0.042	0.061								
	F → Y	(HL)		0.411	0.719	1.595	0.023	0.031	0.047					E	1.0		
		(LH)		0.561	0.995	2.146	0.028	0.042	0.061								
F459	A → Y	(HL)		0.387	0.672	1.447	0.012	0.017	0.026	A	1.0					Y	22
		(LH)		0.243	0.426	0.886	0.015	0.022	0.031								
	B → Y	(HL)		0.372	0.656	1.454	0.012	0.017	0.026			B	1.0				
		(LH)		0.275	0.462	0.949	0.015	0.022	0.031								
	C → Y	(HL)		0.367	0.784	1.696	0.012	0.017	0.025					C	1.0		
		(LH)		0.253	0.482	1.000	0.015	0.022	0.031								
	D → Y	(HL)		0.390	0.699	1.533	0.012	0.017	0.026	D	1.0						
		(LH)		0.506	0.833	1.821	0.015	0.022	0.031								
	E → Y	(HL)		0.427	0.768	1.701	0.012	0.017	0.026			E	1.0				
		(LH)		0.567	0.996	2.146	0.015	0.022	0.031								
	F → Y	(HL)		0.433	0.779	1.731	0.012	0.017	0.026					F	1.0		
		(LH)		0.570	1.018	2.193	0.015	0.022	0.031								

Chapter 2 Function Block

Function	1-1-1-1-2-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F490	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F490	A → Y	(HL)		0.465	0.823	1.848	0.012	0.017	0.026	A	1.0	Y	22
		(LH)		0.265	0.475	0.987	0.015	0.022	0.031	B	1.0		
	B → Y	(HL)		0.465	0.833	1.912	0.012	0.017	0.026	C	1.0		
		(LH)		0.296	0.511	1.053	0.015	0.022	0.031	D	1.0		
	C → Y	(HL)		0.480	0.852	1.968	0.012	0.017	0.026	E	1.0		
		(LH)		0.341	0.562	1.146	0.015	0.022	0.031	F	1.0		
	D → Y	(HL)		0.379	0.778	1.669	0.012	0.017	0.026				
		(LH)		0.260	0.488	1.004	0.015	0.022	0.031				
	E → Y	(HL)		0.401	0.711	1.551	0.012	0.017	0.026				
		(LH)		0.453	0.727	1.527	0.015	0.022	0.031				
	F → Y	(HL)		0.439	0.777	1.712	0.012	0.017	0.026				
		(LH)		0.469	0.802	1.681	0.015	0.022	0.031				

Chapter 2 Function Block

Function	1-2-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L491	5										
x1	F491	5										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
L491	A → Y	(HL)		0.326	0.546	1.115	0.023	0.031	0.047	A	1.0	Y	10		
		(LH)		0.258	0.431	0.876	0.029	0.042	0.061						
	B → Y	(HL)		0.367	0.772	1.660	0.023	0.031	0.047					B	1.0
		(LH)		0.356	0.677	1.449	0.029	0.042	0.061						
	C → Y	(HL)		0.383	0.813	1.751	0.023	0.031	0.047					C	1.0
		(LH)		0.343	0.690	1.505	0.029	0.042	0.061						
	D → Y	(HL)		0.404	0.774	1.679	0.023	0.031	0.047	D	1.0				
		(LH)		0.684	1.173	2.487	0.029	0.042	0.061						
	E → Y	(HL)		0.418	0.812	1.763	0.023	0.031	0.047	E	1.0				
		(LH)		0.706	1.243	2.640	0.029	0.042	0.061						
	F → Y	(HL)		0.430	0.859	1.878	0.023	0.031	0.047	F	1.0				
		(LH)		0.745	1.332	2.786	0.029	0.042	0.061						
F491	A → Y	(HL)		0.347	0.602	1.245	0.012	0.017	0.025	A	1.0	Y	22		
		(LH)		0.253	0.433	0.884	0.015	0.022	0.031						
	B → Y	(HL)		0.415	0.873	1.899	0.012	0.017	0.026					B	1.0
		(LH)		0.419	0.770	1.658	0.015	0.022	0.032						
	C → Y	(HL)		0.430	0.913	1.988	0.012	0.017	0.026					C	1.0
		(LH)		0.407	0.783	1.712	0.015	0.022	0.032						
	D → Y	(HL)		0.431	0.851	1.865	0.012	0.017	0.026	D	1.0				
		(LH)		0.713	1.222	2.607	0.015	0.022	0.031						
	E → Y	(HL)		0.445	0.888	1.950	0.012	0.017	0.026	E	1.0				
		(LH)		0.734	1.292	2.758	0.015	0.022	0.031						
	F → Y	(HL)		0.459	0.940	2.074	0.012	0.017	0.026	F	1.0				
		(LH)		0.775	1.381	2.905	0.015	0.022	0.031						

Chapter 2 Function Block

Function	3-3-3-Input OR-NAND													
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L493	6												
x1	F493	7												
x2														
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H		-		-		-			
	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"			Logic Diagram for "with inv. B type"								
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"			Logic Diagram for "with inv. E type"								
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"			Logic Diagram for "with inv. H type"								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L493	A → Y	(HL)		0.342	0.571	1.169	0.023	0.031	0.047	A	1.0	Y	10
		(LH)		0.433	0.724	1.612	0.029	0.043	0.062	B	1.0		
	B → Y	(HL)		0.358	0.592	1.206	0.023	0.031	0.047	C	1.0		
		(LH)		0.448	0.788	1.772	0.029	0.043	0.062	D	1.0		
	C → Y	(HL)		0.372	0.610	1.245	0.023	0.031	0.047	E	1.0		
		(LH)		0.480	0.876	1.918	0.029	0.043	0.062	F	1.0		
	D → Y	(HL)		0.391	0.797	1.735	0.023	0.031	0.047	G	1.0		
		(LH)		0.515	0.888	1.986	0.029	0.042	0.061	H	1.0		
	E → Y	(HL)		0.421	0.885	1.933	0.023	0.031	0.047	I	1.0		
		(LH)		0.576	1.047	2.310	0.029	0.042	0.061				
	F → Y	(HL)		0.424	0.909	1.986	0.023	0.031	0.047				
		(LH)		0.578	1.069	2.355	0.029	0.042	0.061				
	G → Y	(HL)		0.404	0.826	1.819	0.023	0.031	0.047				
		(LH)		0.714	1.192	2.553	0.029	0.042	0.061				
	H → Y	(HL)		0.425	0.914	2.013	0.023	0.031	0.047				
		(LH)		0.780	1.353	2.869	0.029	0.042	0.061				
	I → Y	(HL)		0.428	0.938	2.067	0.023	0.031	0.047				
		(LH)		0.784	1.375	2.916	0.029	0.042	0.061				
F493	A → Y	(HL)		0.363	0.625	1.297	0.012	0.017	0.025	A	1.0	Y	22
		(LH)		0.440	0.748	1.666	0.015	0.022	0.031	B	1.0		
	B → Y	(HL)		0.378	0.646	1.334	0.012	0.017	0.025	C	1.0		
		(LH)		0.455	0.812	1.826	0.015	0.022	0.031	D	1.0		
	C → Y	(HL)		0.391	0.666	1.377	0.012	0.017	0.026	E	1.0		
		(LH)		0.487	0.899	1.973	0.015	0.022	0.031	F	1.0		
	D → Y	(HL)		0.441	0.918	2.005	0.012	0.017	0.026	G	1.0		
		(LH)		0.613	1.085	2.370	0.015	0.022	0.032	H	1.0		
	E → Y	(HL)		0.455	0.961	2.098	0.012	0.017	0.026	I	1.0		
		(LH)		0.632	1.151	2.522	0.015	0.022	0.032				
	F → Y	(HL)		0.464	1.011	2.228	0.012	0.017	0.026				
		(LH)		0.668	1.238	2.668	0.015	0.022	0.032				
	G → Y	(HL)		0.448	0.948	2.088	0.012	0.017	0.026				
		(LH)		0.819	1.405	2.960	0.015	0.022	0.032				
	H → Y	(HL)		0.460	0.991	2.182	0.012	0.017	0.026				
		(LH)		0.841	1.475	3.109	0.015	0.022	0.032				
	I → Y	(HL)		0.472	1.043	2.310	0.012	0.017	0.026				
		(LH)		0.885	1.567	3.258	0.015	0.022	0.032				

Chapter 2 Function Block

Function	3-3-3-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F496	8										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-		-		-	
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"			Logic Diagram for "with inv. B type"						
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"			Logic Diagram for "with inv. E type"						
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"			Logic Diagram for "with inv. H type"						

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F496	A	→	Y	(HL)	0.438	0.929	2.043	0.012	0.017	0.026	A	1.0	Y	22
				(LH)	0.568	1.005	2.228	0.015	0.022	0.032	B	1.0		
	B	→	Y	(HL)	0.454	0.974	2.142	0.012	0.017	0.026	C	1.0		
				(LH)	0.587	1.071	2.381	0.015	0.022	0.032	D	1.0		
	C	→	Y	(HL)	0.466	1.033	2.287	0.012	0.017	0.026	E	1.0		
				(LH)	0.625	1.160	2.530	0.015	0.022	0.032	F	1.0		
	D	→	Y	(HL)	0.452	0.960	2.129	0.012	0.017	0.026	G	1.0		
				(LH)	0.737	1.329	2.832	0.015	0.022	0.032	H	1.0		
	E	→	Y	(HL)	0.466	1.006	2.228	0.012	0.017	0.026	I	1.0		
				(LH)	0.759	1.399	2.981	0.015	0.022	0.032	J	1.0		
	F	→	Y	(HL)	0.480	1.064	2.369	0.012	0.017	0.026	K	1.0		
				(LH)	0.800	1.488	3.128	0.015	0.022	0.032	L	1.0		
	G	→	Y	(HL)	0.442	0.918	2.002	0.012	0.017	0.026				
				(LH)	0.608	1.078	2.360	0.015	0.022	0.032				
	H	→	Y	(HL)	0.457	0.960	2.096	0.012	0.017	0.026				
				(LH)	0.628	1.145	2.513	0.015	0.022	0.032				
I	→	Y	(HL)	0.465	1.011	2.226	0.012	0.017	0.026					
			(LH)	0.666	1.234	2.662	0.015	0.022	0.032					
J	→	Y	(HL)	0.447	0.949	2.088	0.012	0.017	0.026					
			(LH)	0.775	1.384	2.930	0.015	0.022	0.032					
K	→	Y	(HL)	0.458	0.989	2.178	0.012	0.017	0.026					
			(LH)	0.797	1.454	3.080	0.015	0.022	0.032					
L	→	Y	(HL)	0.468	1.040	2.304	0.012	0.017	0.026					
			(LH)	0.839	1.543	3.226	0.015	0.022	0.032					



Chapter 2 Function Block

Function	4-4-4-4-Input OR-NAND											
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F498	14										
x2												
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H		-	-	-			
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												
Logic Diagram for "Normal"			Logic Diagram for "with inv. A type"				Logic Diagram for "with inv. B type"					
Logic Diagram for "with inv. C type"			Logic Diagram for "with inv. D type"				Logic Diagram for "with inv. E type"					
Logic Diagram for "with inv. F type"			Logic Diagram for "with inv. G type"				Logic Diagram for "with inv. H type"					

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F498	A	→	Y	(HL)	0.447	0.929	1.924	0.018	0.027	0.045	A	1.0	Y	16
				(LH)	0.473	0.848	1.878	0.015	0.022	0.034	B	1.0		
	B	→	Y	(HL)	0.462	0.948	1.956	0.018	0.027	0.045	C	1.0		
				(LH)	0.461	0.860	1.936	0.015	0.022	0.034	D	1.0		
	C	→	Y	(HL)	0.481	0.986	2.033	0.018	0.027	0.045	E	1.0		
				(LH)	0.449	0.796	1.770	0.015	0.022	0.034	F	1.0		
	D	→	Y	(HL)	0.496	1.005	2.067	0.018	0.027	0.045	G	1.0		
				(LH)	0.436	0.807	1.830	0.015	0.022	0.034	H	1.0		
	E	→	Y	(HL)	0.473	0.994	2.050	0.018	0.027	0.045	I	1.0		
				(LH)	0.498	0.919	2.050	0.015	0.022	0.034	J	1.0		
	F	→	Y	(HL)	0.487	1.011	2.081	0.018	0.027	0.045	K	1.0		
				(LH)	0.486	0.930	2.109	0.015	0.022	0.034	L	1.0		
	G	→	Y	(HL)	0.507	1.050	2.159	0.018	0.027	0.045	M	1.0		
				(LH)	0.471	0.861	1.937	0.015	0.022	0.034	N	1.0		
	H	→	Y	(HL)	0.521	1.069	2.191	0.018	0.027	0.045	O	1.0		
				(LH)	0.458	0.873	1.996	0.015	0.022	0.034	P	1.0		
	I	→	Y	(HL)	0.447	0.930	1.925	0.018	0.027	0.045				
				(LH)	0.474	0.850	1.880	0.015	0.022	0.034				
	J	→	Y	(HL)	0.462	0.949	1.959	0.018	0.027	0.045				
				(LH)	0.462	0.862	1.939	0.015	0.022	0.034				
K	→	Y	(HL)	0.481	0.987	2.034	0.018	0.027	0.045					
			(LH)	0.449	0.796	1.772	0.015	0.022	0.034					
L	→	Y	(HL)	0.496	1.006	2.068	0.018	0.027	0.045					
			(LH)	0.437	0.808	1.831	0.015	0.022	0.034					
M	→	Y	(HL)	0.473	0.994	2.052	0.018	0.027	0.045					
			(LH)	0.498	0.918	2.049	0.015	0.022	0.034					
N	→	Y	(HL)	0.487	1.011	2.082	0.018	0.027	0.045					
			(LH)	0.486	0.930	2.109	0.015	0.022	0.034					
O	→	Y	(HL)	0.507	1.051	2.161	0.018	0.027	0.045					
			(LH)	0.473	0.863	1.940	0.015	0.022	0.034					
P	→	Y	(HL)	0.522	1.070	2.193	0.018	0.027	0.045					
			(LH)	0.460	0.875	1.999	0.015	0.022	0.034					

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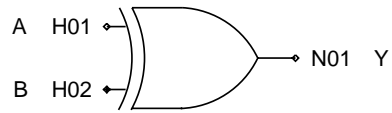
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## 2.7 Exclusive OR, Exclusive NOR

Chapter 2 Function Block

Function	2-Input Exclusive OR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L511	3								
x1	F511	4								
x2										
x4										

Logic Diagram



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

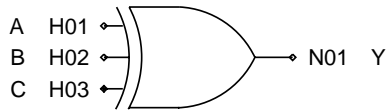
Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
L511	A → Y	(HH)		0.258	0.420	0.930	0.029	0.043	0.064	A B	2.0 1.9	Y	10
		(HL)		0.301	0.488	1.034	0.022	0.029	0.043				
		(LH)		0.274	0.480	1.052	0.029	0.043	0.063				
	B → Y	(LL)		0.369	0.602	1.241	0.024	0.032	0.048				
		(HH)		0.218	0.343	0.752	0.029	0.043	0.063				
		(HL)		0.286	0.471	1.038	0.022	0.029	0.043				
F511	A → Y	(HL)		0.347	0.588	1.273	0.029	0.043	0.064	A B	1.9 1.9	Y	21
		(LL)		0.354	0.531	1.091	0.024	0.032	0.049				
		(HH)		0.264	0.446	0.998	0.015	0.022	0.033				
	B → Y	(HL)		0.314	0.523	1.108	0.011	0.015	0.023				
		(LH)		0.282	0.508	1.125	0.015	0.022	0.033				
		(LL)		0.393	0.670	1.391	0.013	0.017	0.026				
	(HH)		0.221	0.363	0.810	0.015	0.022	0.033					
	(HL)		0.299	0.505	1.112	0.011	0.015	0.023					
	(LH)		0.358	0.620	1.349	0.015	0.022	0.033					
		(LL)		0.375	0.596	1.238	0.013	0.017	0.026				

Chapter 2 Function Block

Function	3-Input Exclusive OR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L516	6								
x1	F516	7								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

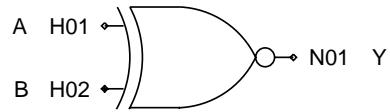
Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L516	A → Y	(HH)		0.611	1.032	2.258	0.029	0.043	0.063	A	1.0	Y	10	
		(HL)		0.475	0.778	1.646	0.024	0.032	0.048					
		(LH)		0.491	0.881	1.927	0.029	0.043	0.063					
	B → Y	(LL)		0.654	1.132	2.452	0.024	0.033	0.049	B	1.0	Y	10	
		(HH)		0.434	0.751	1.604	0.029	0.043	0.063					
		(HL)		0.469	0.839	1.809	0.024	0.033	0.049					
	C → Y	(LL)		0.455	0.855	1.895	0.029	0.043	0.064	C	1.0	Y	10	
		(HL)		0.454	0.818	1.753	0.024	0.032	0.049					
		(HH)		0.307	0.477	0.981	0.029	0.043	0.064					
	F516	A → Y	(HL)		0.442	0.720	1.501	0.024	0.033	0.050	A	1.0	Y	21
			(LH)		0.407	0.675	1.446	0.029	0.043	0.063				
			(LL)		0.350	0.598	1.264	0.025	0.034	0.051				
B → Y		(HH)		0.621	1.057	2.309	0.015	0.022	0.033	B	1.0	Y	21	
		(HL)		0.507	0.850	1.798	0.012	0.017	0.026					
		(LH)		0.513	0.927	2.029	0.015	0.022	0.033					
C → Y		(LL)		0.658	1.169	2.546	0.013	0.017	0.027	C	1.0	Y	21	
		(HH)		0.443	0.782	1.685	0.015	0.022	0.033					
		(HL)		0.478	0.883	1.916	0.012	0.017	0.027					
C → Y		(LH)		0.463	0.881	1.957	0.015	0.022	0.033	C	1.0	Y	21	
		(LL)		0.473	0.888	1.907	0.012	0.017	0.027					
		(HH)		0.305	0.489	1.020	0.015	0.022	0.033					
C → Y	(HL)		0.442	0.749	1.592	0.013	0.017	0.027	C	1.0	Y	21		
	(LH)		0.404	0.685	1.483	0.015	0.022	0.033						
	(LL)		0.349	0.625	1.355	0.013	0.018	0.027						

### Chapter 2 Function Block

Function	2-Input Exclusive NOR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L512	3								
x1	F512	4								
x2										
x4										

Logic Diagram



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

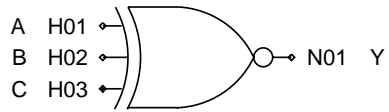
### Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L512	A → Y	(HH)		0.256	0.417	0.919	0.029	0.043	0.064	A	2.0	Y	10
		(HL)		0.306	0.527	1.087	0.023	0.032	0.048				
		(LH)		0.307	0.532	1.140	0.029	0.042	0.061				
	B → Y	(LL)		0.373	0.613	1.262	0.024	0.032	0.049	B	1.9		
		(HH)		0.255	0.415	0.874	0.029	0.043	0.064				
		(HL)		0.436	0.679	1.369	0.024	0.032	0.049				
		(LH)		0.294	0.542	1.194	0.029	0.042	0.061				
		(LL)		0.249	0.465	0.986	0.023	0.032	0.048				
F512	A → Y	(HH)		0.262	0.441	0.986	0.015	0.022	0.033	A	1.9	Y	21
		(HL)		0.330	0.586	1.220	0.012	0.017	0.026				
		(LH)		0.314	0.554	1.184	0.015	0.022	0.031				
	B → Y	(LL)		0.397	0.682	1.411	0.013	0.017	0.026	B	1.9		
		(HH)		0.261	0.438	0.939	0.015	0.022	0.033				
		(HL)		0.461	0.747	1.514	0.013	0.017	0.026				
		(LH)		0.301	0.563	1.238	0.015	0.022	0.031				
		(LL)		0.270	0.523	1.117	0.012	0.017	0.026				

Chapter 2 Function Block

Function	3-Input Exclusive NOR									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power	L517	7								
x1	F517	7								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
L517	A → Y	(HH)		0.613	1.030	2.253	0.029	0.043	0.063	A	1.0	Y	10	
		(HL)		0.471	0.783	1.655	0.024	0.032	0.048					
		(LH)		0.493	0.877	1.919	0.029	0.043	0.063					
	B → Y	(LL)		0.655	1.131	2.452	0.024	0.033	0.049	B	1.0			
		(HH)		0.435	0.749	1.606	0.029	0.043	0.063					
		(HL)		0.470	0.836	1.798	0.024	0.033	0.049					
	C → Y	(LL)		0.451	0.827	1.774	0.024	0.032	0.049	C	1.0			
		(HH)		0.307	0.477	0.980	0.029	0.043	0.064					
		(HL)		0.442	0.720	1.500	0.024	0.033	0.050					
	F517	A → Y	(LH)		0.407	0.675	1.447	0.029	0.043	0.063	A	1.0	Y	21
			(LL)		0.350	0.599	1.264	0.025	0.034	0.051				
			(HL)		0.623	1.055	2.303	0.015	0.022	0.033				
B → Y		(HL)		0.503	0.855	1.805	0.012	0.017	0.026	B	1.0			
		(LH)		0.514	0.925	2.021	0.015	0.022	0.033					
		(LL)		0.660	1.167	2.545	0.012	0.017	0.027					
C → Y		(HH)		0.444	0.780	1.686	0.015	0.022	0.033	C	1.0			
		(HL)		0.480	0.879	1.906	0.012	0.017	0.027					
		(LH)		0.465	0.878	1.951	0.015	0.022	0.033					
		(LL)		0.474	0.893	1.926	0.012	0.017	0.027					
		(HH)		0.305	0.489	1.020	0.015	0.022	0.033					
		(HL)		0.443	0.749	1.592	0.013	0.017	0.027					
	(LH)		0.404	0.685	1.483	0.015	0.022	0.033						
	(LL)		0.349	0.625	1.355	0.013	0.018	0.027						

[MEMO]

[MEMO]



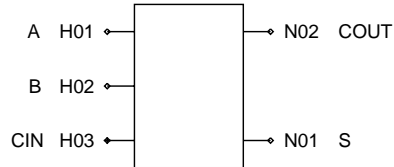
[MEMO]

## 2.8 Adder, 3-State Buffer, Decoder, Multiplexer, Generator

### Chapter 2 Function Block

Function	1-Bit Full Adder									
Block type	Standard type									
	Normal			High speed						
Drivability	Name	cells	Name	cells						
Low Power										
x1	F521	9								
x2										
x4										

Logic Diagram



Truth Table

A	B	CIN	S	COUT
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

### Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.					MAX.
F521	A → S	(HH)		0.546	1.093	2.452	0.015	0.022	0.033	A	1.7	S	21
		(HL)		0.659	1.171	2.597	0.012	0.017	0.026				
		(LH)		0.679	1.541	3.460	0.015	0.022	0.033				
	A → COUT	(LL)		0.723	1.694	3.695	0.011	0.017	0.026	B	2.0	COUT	20
		(HH)		0.470	1.092	2.449	0.015	0.023	0.035				
		(LL)		0.343	1.213	2.561	0.012	0.016	0.026				
	B → S	(HH)		0.591	1.079	2.459	0.015	0.022	0.033	CIN	1.0		
		(HL)		0.654	1.219	2.671	0.011	0.017	0.026				
		(LH)		0.698	1.463	3.280	0.015	0.022	0.033				
	B → COUT	(LL)		0.742	1.621	3.518	0.011	0.017	0.026				
		(HH)		0.515	1.079	2.457	0.015	0.023	0.036				
		(LL)		0.335	1.298	2.713	0.012	0.016	0.025				
	CIN → S	(HH)		0.493	0.830	1.774	0.015	0.022	0.033				
		(HL)		0.614	0.959	1.967	0.013	0.017	0.026				
		(LH)		0.480	0.806	1.698	0.015	0.022	0.033				
	CIN → COUT	(LL)		0.478	0.830	1.793	0.011	0.015	0.023				
		(HH)		0.335	0.537	1.107	0.015	0.022	0.034				
		(LL)		0.393	0.706	1.506	0.013	0.018	0.027				

Chapter 2 Function Block

Function	4-Bit Full Adder									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power										
x1	F523	32								
x2										
x4										

Logic Diagram

Truth Table

An	Bn	CIN	Sn	COUT
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

(Condition of one stage, n=1,2,3,4)

Chapter 2 Function Block

Block type	Switching speed							Input		Output							
	Path			t LDO (ns)			t 1										
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout				
F523	A1 → S1	(HH)		0.566	1.008	2.326	0.015	0.022	0.032	A1	1.7	S1	19				
				0.686	1.200	2.684	0.011	0.015	0.022					B1	2.0	S2	19
				1.085	1.885	4.066	0.015	0.022	0.033								
	A1 → S2	(HH)		0.972	1.711	3.910	0.014	0.021	0.032	A3	1.7	COUT	10				
				1.554	2.410	5.300	0.013	0.017	0.026					B3	2.0	S4	18
				1.114	1.884	3.874	0.015	0.022	0.033								
	A1 → S3	(HH)		0.693	1.213	2.654	0.011	0.015	0.022	B4	2.0	COUT	10				
				1.298	2.298	5.353	0.014	0.022	0.032					CIN	2.1	COUT	10
				1.865	3.109	6.959	0.013	0.017	0.026								
	A1 → S4	(HH)		1.339	2.453	5.257	0.015	0.022	0.033	A4	1.7	S4	18				
				1.339	2.453	5.257	0.015	0.022	0.033					B4	2.0	COUT	10
				0.978	1.764	3.925	0.011	0.015	0.022								
	A1 → COUT	(HH)		1.267	2.379	5.487	0.011	0.015	0.022	A4	1.7	S4	18				
				1.664	3.047	7.383	0.020	0.031	0.049					B4	2.0	COUT	10
				1.260	2.527	6.045	0.022	0.031	0.044								
	B1 → S1	(HH)		0.608	1.093	2.519	0.015	0.022	0.032	A1	1.7	S1	19				
				0.668	1.186	2.694	0.011	0.015	0.022					B1	2.0	S2	19
				1.049	1.794	3.854	0.015	0.022	0.033								
	B1 → S2	(HH)		0.761	1.358	2.964	0.011	0.015	0.022	A3	1.7	COUT	10				
				0.954	1.696	3.919	0.014	0.021	0.032					B3	2.0	S4	18
				1.536	2.396	5.310	0.013	0.017	0.026								
	B1 → S3	(HH)		1.131	1.898	3.890	0.015	0.022	0.033	A4	1.7	S4	18				
				0.721	1.243	2.706	0.011	0.015	0.022					B3	2.0	S4	18
				1.280	2.284	5.363	0.014	0.022	0.032								
	B1 → S4	(HH)		1.847	3.095	6.968	0.013	0.017	0.027	A4	1.7	S4	18				
				1.355	2.465	5.272	0.015	0.022	0.033					B4	2.0	COUT	10
				0.999	1.776	3.931	0.011	0.015	0.022								
	B1 → COUT	(HH)		1.632	2.946	7.056	0.014	0.022	0.032	A4	1.7	S4	18				
				2.005	3.529	8.201	0.012	0.017	0.026					B4	2.0	COUT	10
				1.511	2.901	6.487	0.015	0.022	0.033								
	A2 → S2	(HH)		1.289	2.395	5.513	0.011	0.015	0.022	A1	1.7	S1	19				
				1.646	3.033	7.392	0.020	0.031	0.049					B1	2.0	S2	19
				1.277	2.540	6.059	0.022	0.031	0.044								
	A2 → S3	(HH)		0.563	1.003	2.316	0.015	0.022	0.032	A2	1.7	S3	18				
				0.676	1.185	2.658	0.011	0.015	0.022					B2	2.0	S4	18
				1.051	1.843	4.017	0.015	0.022	0.033								
	A2 → S4	(HH)		0.741	1.279	2.802	0.011	0.015	0.022	A4	1.7	S4	18				
				0.985	1.732	3.945	0.014	0.022	0.032					B3	2.0	S4	18
				1.423	2.307	5.068	0.012	0.017	0.026								
	A2 → COUT	(HH)		0.997	1.703	3.568	0.015	0.022	0.033	A4	1.7	S4	18				
				0.703	1.229	2.679	0.011	0.015	0.022					B4	2.0	COUT	10
				1.286	2.280	5.325	0.014	0.021	0.032								
	B2 → S2	(HH)		1.597	2.752	6.228	0.012	0.017	0.026	A1	1.7	S1	19				
				1.160	2.149	4.699	0.015	0.022	0.033					B1	2.0	S2	19
				0.967	1.751	3.918	0.011	0.015	0.022								
	B2 → S3	(HH)		1.266	2.289	5.435	0.018	0.028	0.045	A3	1.7	COUT	10				
				0.941	1.824	4.273	0.020	0.030	0.044					B3	2.0	S4	18
				0.605	1.088	2.511	0.015	0.022	0.032								
B2 → S4	(HH)		0.658	1.170	2.667	0.011	0.015	0.022	A4	1.7	S4	18					
			1.015	1.752	3.807	0.015	0.022	0.033					B4	2.0	COUT	10	
			0.760	1.355	2.955	0.011	0.015	0.022									CIN
B2 → S3	(HH)		0.967	1.716	3.954	0.014	0.022	0.032	A1	1.7	S1	19					
			1.405	2.291	5.077	0.012	0.017	0.026					B1	2.0	S2	19	
			1.405	2.291	5.077	0.012	0.017	0.026									A2

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B2 → S4	(LH)		1.028	1.730	3.601	0.015	0.022	0.033				
		(LL)		0.730	1.258	2.731	0.011	0.015	0.022				
	B2 → COUT	(HH)		1.268	2.265	5.334	0.014	0.021	0.032				
		(HL)		1.578	2.737	6.237	0.012	0.017	0.026				
	A3 → S3	(LH)		1.191	2.190	4.790	0.015	0.022	0.033				
		(LL)		0.989	1.767	3.939	0.011	0.015	0.022				
	A3 → S4	(HH)		1.248	2.274	5.445	0.018	0.028	0.045				
		(LL)		0.968	1.857	4.364	0.021	0.030	0.044				
	A3 → COUT	(HH)		0.567	1.008	2.325	0.015	0.022	0.032				
		(HL)		0.686	1.200	2.683	0.011	0.015	0.022				
	B3 → S3	(LH)		1.000	1.774	3.905	0.015	0.022	0.033				
		(LL)		0.743	1.283	2.812	0.011	0.015	0.022				
	B3 → S4	(HH)		0.973	1.714	3.916	0.014	0.021	0.032				
		(HL)		1.232	2.092	4.618	0.012	0.017	0.026				
	A3 → COUT	(LH)		0.829	1.449	3.109	0.015	0.022	0.033				
		(LL)		0.693	1.213	2.655	0.011	0.015	0.022				
	B3 → COUT	(HH)		0.926	1.651	3.814	0.017	0.026	0.041				
		(LL)		0.658	1.215	2.685	0.016	0.022	0.033				
	B3 → S4	(HH)		0.608	1.093	2.518	0.015	0.022	0.032				
		(HL)		0.668	1.186	2.693	0.011	0.015	0.022				
	B3 → COUT	(LH)		0.968	1.689	3.707	0.015	0.022	0.033				
		(LL)		0.760	1.357	2.962	0.011	0.015	0.022				
	A4 → S4	(HH)		0.955	1.699	3.926	0.014	0.021	0.032				
		(HL)		1.214	2.077	4.628	0.012	0.017	0.026				
	A4 → COUT	(LH)		0.851	1.463	3.132	0.015	0.022	0.033				
		(LL)		0.720	1.243	2.706	0.011	0.015	0.022				
	B4 → S4	(HH)		0.908	1.636	3.823	0.017	0.026	0.041				
		(LL)		0.682	1.230	2.693	0.016	0.022	0.034				
	A4 → S4	(HH)		0.563	1.003	2.317	0.015	0.022	0.032				
		(HL)		0.677	1.186	2.661	0.011	0.015	0.022				
	A4 → COUT	(LH)		0.885	1.606	3.605	0.014	0.022	0.032				
		(LL)		0.741	1.279	2.803	0.011	0.015	0.022				
	B4 → S4	(HH)		0.637	1.122	2.500	0.016	0.024	0.036				
		(LL)		0.397	0.709	1.479	0.013	0.017	0.027				
	B4 → COUT	(HH)		0.605	1.089	2.512	0.015	0.022	0.032				
		(HL)		0.658	1.171	2.671	0.011	0.015	0.022				
	CIN → S1	(LH)		0.857	1.527	3.423	0.014	0.022	0.032				
		(LL)		0.760	1.355	2.956	0.011	0.015	0.022				
	CIN → S2	(HH)		0.618	1.106	2.510	0.016	0.024	0.036				
		(LL)		0.424	0.739	1.536	0.013	0.017	0.026				
	CIN → S3	(HH)		0.428	0.718	1.541	0.014	0.022	0.032				
		(HL)		0.580	0.914	1.836	0.012	0.017	0.026				
	CIN → S4	(LH)		0.489	0.797	1.670	0.015	0.022	0.033				
		(LL)		0.410	0.708	1.530	0.011	0.015	0.022				
	CIN → S2	(HH)		0.566	0.956	2.094	0.014	0.022	0.032				
		(HL)		0.831	1.281	2.678	0.013	0.017	0.026				
	CIN → S3	(LH)		0.817	1.471	3.076	0.015	0.022	0.033				
		(LL)		0.558	0.996	2.196	0.011	0.015	0.022				
	CIN → S4	(HH)		0.782	1.348	3.022	0.014	0.022	0.032				
		(HL)		1.150	1.828	3.935	0.012	0.017	0.026				
	CIN → S1	(LH)		1.081	2.096	4.561	0.015	0.022	0.033				
		(LL)		0.778	1.469	3.333	0.011	0.015	0.022				
	CIN → S2	(HH)		1.043	1.834	4.233	0.014	0.022	0.032				
		(HL)		1.328	2.262	5.027	0.012	0.017	0.026				
	CIN → S3	(LH)		1.242	2.537	5.789	0.015	0.022	0.033				
		(LL)		1.032	2.053	4.847	0.011	0.015	0.022				

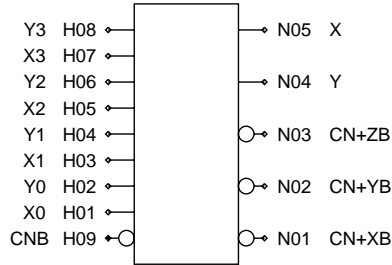
Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
	CIN	→	COUT	(HH)	1.004	1.807	4.233	0.018	0.028	0.043				
				(LL)	1.007	2.177	5.361	0.022	0.031	0.044				

Chapter 2 Function Block

Function	4-Bit Look Ahead Carry Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power										
x1	F526	34								
x2										
x4										

Logic Diagram



Truth Table

Y3	Y2	Y1	Y0	X3	X2	X1	Y
0	X	X	X	X	X	X	0
X	0	X	X	0	X	X	0
X	X	0	X	0	0	X	0
X	X	X	0	0	0	0	0
All other combinations							1

Y0	X0	CnB	Cn+xB
0	X	X	1
X	0	1	1
All other combinations			0

Y2	Y1	Y0	X2	X1	X0	CnB	Cn+zB
0	X	X	X	X	X	X	1
X	0	X	0	X	X	X	1
X	X	0	0	0	X	X	1
X	X	X	0	0	0	1	1
All other combinations							0

X3	X2	X1	X0	X
0	0	0	0	0
All other combinations				1

Y1	Y0	X1	X0	CnB	Cn+yB
0	X	X	X	X	1
X	0	0	X	X	1
X	X	0	0	1	1
All other combinations					0

Chapter 2 Function Block

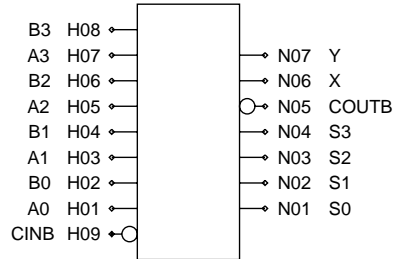
Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F526	X0	→	CN+XB (HL)	0.167	0.237	0.480	0.017	0.025	0.041	X0	6.9	CN+XB	4
			(LH)	0.235	0.355	0.732	0.028	0.042	0.061	Y0	10.5	CN+YB	5
	X0	→	CN+YB (HL)	0.427	0.730	1.618	0.011	0.015	0.023	X1	5.3	CN+ZB	21
			(LH)	0.362	0.634	1.366	0.040	0.060	0.089	Y1	8.8	Y	14
	X0	→	CN+ZB (HL)	0.714	1.232	2.923	0.011	0.015	0.023	X2	3.8	X	22
			(LH)	0.786	1.291	2.746	0.015	0.022	0.033	Y2	7.4		
	X0	→	X (HH)	0.187	0.292	0.551	0.015	0.022	0.032	X3	2.7		
			(LL)	0.444	0.773	1.749	0.014	0.021	0.033	Y3	4.1		
	Y0	→	CN+XB (HL)	0.156	0.324	0.692	0.017	0.025	0.042	CNB	2.1		
			(LH)	0.173	0.364	0.738	0.022	0.033	0.048				
	Y0	→	CN+YB (HL)	0.406	0.756	1.685	0.011	0.015	0.023				
			(LH)	0.389	0.700	1.495	0.040	0.060	0.089				
	Y0	→	CN+ZB (HL)	0.458	1.193	2.899	0.011	0.015	0.023				
			(LH)	0.445	1.053	2.282	0.015	0.022	0.033				
	Y0	→	Y (HH)	0.577	1.088	2.696	0.016	0.025	0.039				
			(LL)	0.492	0.882	1.867	0.018	0.027	0.046				
	X1	→	CN+YB (HL)	0.344	0.570	1.204	0.011	0.015	0.023				
			(LH)	0.332	0.576	1.251	0.040	0.060	0.089				
	X1	→	CN+ZB (HL)	0.447	0.792	1.773	0.011	0.015	0.023				
			(LH)	0.400	0.736	1.631	0.015	0.022	0.033				
	X1	→	Y (HH)	0.420	0.726	1.734	0.016	0.024	0.037				
			(LL)	0.387	0.640	1.377	0.018	0.027	0.046				
	X1	→	X (HH)	0.202	0.312	0.591	0.015	0.022	0.032				
			(LL)	0.479	0.880	1.996	0.014	0.021	0.033				
	Y1	→	CN+YB (HL)	0.325	0.764	1.739	0.011	0.015	0.023				
			(LH)	0.359	0.731	1.555	0.040	0.060	0.088				
	Y1	→	CN+ZB (HL)	0.415	1.188	2.846	0.011	0.015	0.023				
			(LH)	0.370	1.106	2.359	0.015	0.022	0.033				
	Y1	→	Y (HH)	0.421	1.189	2.984	0.016	0.025	0.039				
			(LL)	0.380	0.820	1.717	0.018	0.027	0.045				
	X2	→	CN+ZB (HL)	0.465	0.808	1.749	0.011	0.015	0.023				
			(LH)	0.391	0.745	1.645	0.015	0.022	0.033				
	X2	→	Y (HH)	0.376	0.669	1.515	0.015	0.023	0.035				
			(LL)	0.374	0.677	1.431	0.018	0.027	0.045				
	X2	→	X (HH)	0.215	0.330	0.627	0.015	0.022	0.032				
			(LL)	0.559	1.059	2.312	0.014	0.021	0.033				
	Y2	→	CN+ZB (HL)	0.452	1.397	3.360	0.011	0.015	0.023				
			(LH)	0.476	1.313	2.758	0.015	0.022	0.033				
	Y2	→	Y (HH)	0.392	1.249	3.126	0.016	0.024	0.039				
			(LL)	0.454	0.907	1.884	0.018	0.027	0.045				
X3	→	Y (HH)	0.386	0.668	1.450	0.015	0.022	0.034					
		(LL)	0.357	0.666	1.399	0.018	0.027	0.044					
X3	→	X (HH)	0.215	0.329	0.624	0.015	0.022	0.033					
		(LL)	0.565	1.080	2.358	0.014	0.021	0.033					
Y3	→	Y (HH)	0.385	1.246	3.136	0.015	0.025	0.039					
		(LL)	0.431	0.942	1.942	0.018	0.027	0.045					
CNB	→	CN+XB (HH)	0.372	0.591	1.174	0.029	0.042	0.061					
		(LL)	0.298	0.504	1.053	0.017	0.025	0.042					
CNB	→	CN+YB (HH)	0.567	0.943	1.962	0.040	0.060	0.088					
		(LL)	0.554	0.970	2.157	0.011	0.015	0.023					
CNB	→	CN+ZB (HH)	0.766	1.188	2.533	0.015	0.022	0.033					
		(LL)	0.621	1.081	2.530	0.011	0.015	0.023					

F526

Chapter 2 Function Block

Function	4-Bit Carry Look Ahead Adder									
Block type	Standard type									
	Normal					High speed				
Drivability	Name	cells	Name	cells						
Low Power										
x1	F527	69								
x2										
x4										

Logic Diagram



Truth Table

A0	B0	A1	B1	A2	B2	A3	B3	*1	S0	S1	S2	S3	*2	X	Y	
0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	
0	1	0	1	0	1	0	1	0	0	1	1	1	1	1	0	0
1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	1	0	1	0	1	0	1	1	1	0	1	1	1	1	0	0
1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	

(m=0,1,2,3), \*1:CinB, \*2:CoutB

Sn=(An+Bn+CinB)

X=(A0#B0)+(A1#B1)+(A2#B2)+(A3#B3)

Y=1:(An+Bn)=1111

Y=0:(An+Bn)<1111

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F527	A0 → F0	(HH)		0.592	1.232	2.664	0.015	0.023	0.036	A0	2.9	F0	19
			(HL)	0.665	1.296	2.814	0.013	0.018	0.027	B0	2.9	F1	19
			(LH)	0.664	1.364	2.947	0.015	0.023	0.036	A1	2.9	F2	19
	A0 → F1	(HH)		0.684	1.363	2.918	0.013	0.018	0.026	B1	3.0	F3	19
			(HL)	0.610	1.333	2.980	0.015	0.022	0.033	A2	2.9	COUTB	14
			(LH)	0.626	1.133	2.415	0.012	0.017	0.026	B2	3.0	X	5
	A0 → F2	(HH)		0.628	1.152	2.539	0.016	0.023	0.036	A3	2.8	Y	15
			(HL)	0.652	1.354	2.910	0.013	0.018	0.027	B3	3.0		
			(LH)	0.921	1.656	3.671	0.015	0.022	0.033	CINB	2.1		
	A0 → F3	(HL)		0.941	1.699	3.693	0.012	0.017	0.027				
			(LH)	0.932	1.679	3.668	0.015	0.023	0.036				
			(LL)	0.959	1.753	3.822	0.013	0.017	0.027				
	A0 → COUTB	(HH)		1.087	1.918	4.319	0.015	0.022	0.033				
			(HL)	1.109	1.966	4.358	0.012	0.017	0.027				
			(LH)	1.108	1.956	4.334	0.015	0.023	0.036				
	A0 → X	(LL)		1.138	2.029	4.481	0.013	0.017	0.027				
			(HL)	1.155	2.039	4.627	0.017	0.024	0.039				
			(LH)	1.186	2.090	4.664	0.014	0.021	0.030				
	A0 → Y	(HH)		0.402	0.699	1.468	0.015	0.023	0.034				
			(HL)	0.434	0.750	1.587	0.030	0.047	0.084				
			(LH)	1.055	1.855	4.137	0.017	0.026	0.043				
	B0 → F0	(LL)		1.108	1.949	4.312	0.013	0.018	0.028				
			(HH)	0.604	1.232	2.664	0.015	0.023	0.036				
			(HL)	0.666	1.316	2.851	0.013	0.018	0.027				
	B0 → F1	(LH)		0.633	1.393	2.992	0.015	0.023	0.036				
			(LL)	0.676	1.364	2.917	0.013	0.017	0.027				
			(HH)	0.621	1.333	2.981	0.015	0.022	0.033				
	B0 → F2	(HL)		0.641	1.153	2.453	0.012	0.017	0.026				
			(LH)	0.616	1.164	2.597	0.016	0.023	0.036				
			(LL)	0.639	1.354	2.910	0.013	0.018	0.027				
	B0 → F3	(HH)		0.936	1.676	3.709	0.015	0.022	0.033				
			(HL)	0.956	1.718	3.730	0.012	0.017	0.027				
			(LH)	0.920	1.691	3.726	0.015	0.023	0.036				
	B0 → COUTB	(LL)		0.947	1.765	3.879	0.013	0.017	0.027				
			(HH)	1.102	1.938	4.357	0.015	0.022	0.033				
			(HL)	1.124	1.986	4.395	0.012	0.017	0.027				
	B0 → X	(LH)		1.096	1.968	4.392	0.015	0.023	0.036				
			(LL)	1.125	2.041	4.539	0.013	0.017	0.027				
			(HL)	1.170	2.059	4.665	0.017	0.024	0.039				
	B0 → Y	(LH)		1.174	2.103	4.722	0.014	0.021	0.030				
			(HH)	0.402	0.700	1.468	0.015	0.023	0.034				
			(LL)	0.434	0.750	1.587	0.030	0.047	0.084				
	A1 → F1	(HH)		1.070	1.875	4.174	0.017	0.026	0.043				
			(HL)	1.096	1.961	4.369	0.013	0.018	0.028				
			(LH)	0.622	1.307	2.803	0.015	0.024	0.037				
	A1 → F2	(HL)		0.698	1.346	2.904	0.013	0.018	0.027				
			(LH)	0.710	1.410	3.012	0.015	0.024	0.036				
			(LL)	0.707	1.450	3.088	0.013	0.018	0.027				
A1 → F3	(HH)		0.678	1.266	2.870	0.015	0.022	0.033					
		(HL)	0.698	1.308	2.890	0.012	0.017	0.027					
		(LH)	0.646	1.197	2.644	0.015	0.023	0.036					
A1 → F3	(LL)		0.672	1.271	2.796	0.013	0.017	0.027					
		(HH)	0.928	1.702	3.884	0.015	0.022	0.033					
		(HL)	0.949	1.749	3.922	0.012	0.017	0.027					
A1 → F3	(LH)		0.893	1.614	3.558	0.015	0.023	0.036					
		(LL)	0.919	1.687	3.707	0.013	0.017	0.027					

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
A1 → COUTB	(HL)			1.108	1.968	4.500	0.017	0.024	0.039				
	(LH)			1.066	1.882	4.150	0.014	0.021	0.030				
A1 → X	(HH)			0.424	0.715	1.545	0.015	0.022	0.034				
	(LL)			0.446	0.761	1.643	0.030	0.047	0.084				
A1 → Y	(HH)			1.010	1.784	4.010	0.017	0.026	0.043				
	(LL)			0.988	1.742	3.802	0.013	0.017	0.027				
B1 → F1	(HH)			0.633	1.306	2.803	0.015	0.024	0.037				
	(HL)			0.700	1.365	2.941	0.013	0.018	0.027				
	(LH)			0.679	1.439	3.057	0.015	0.024	0.036				
B1 → F2	(LL)			0.703	1.447	3.089	0.013	0.018	0.027				
	(HH)			0.693	1.285	2.907	0.015	0.022	0.033				
	(HL)			0.713	1.328	2.927	0.012	0.017	0.027				
B1 → F3	(LH)			0.634	1.210	2.702	0.015	0.023	0.036				
	(LL)			0.660	1.283	2.854	0.013	0.017	0.027				
	(HH)			0.943	1.721	3.921	0.015	0.022	0.033				
B1 → COUTB	(HL)			0.965	1.769	3.960	0.012	0.017	0.027				
	(LH)			0.881	1.627	3.615	0.015	0.023	0.036				
	(LL)			0.907	1.700	3.765	0.013	0.017	0.027				
B1 → X	(HL)			1.123	1.987	4.538	0.017	0.024	0.039				
	(LH)			1.054	1.895	4.208	0.014	0.021	0.030				
B1 → Y	(HH)			0.424	0.715	1.545	0.015	0.022	0.034				
	(LL)			0.446	0.761	1.643	0.030	0.047	0.084				
A2 → F2	(HH)			1.025	1.803	4.047	0.017	0.026	0.043				
	(LL)			0.976	1.755	3.860	0.013	0.017	0.027				
	(HH)			0.588	1.240	2.703	0.015	0.024	0.036				
A2 → F3	(HL)			0.671	1.275	2.771	0.013	0.018	0.027				
	(LH)			0.674	1.342	2.890	0.015	0.023	0.036				
	(LL)			0.677	1.382	2.986	0.013	0.018	0.027				
A2 → COUTB	(HH)			0.709	1.338	3.087	0.015	0.022	0.033				
	(HL)			0.730	1.386	3.125	0.012	0.017	0.027				
	(LH)			0.645	1.191	2.616	0.015	0.023	0.036				
A2 → X	(LL)			0.674	1.268	2.772	0.013	0.017	0.027				
	(HL)			0.996	1.818	4.182	0.017	0.024	0.039				
	(LH)			0.903	1.610	3.494	0.014	0.021	0.030				
A2 → Y	(HH)			0.421	0.711	1.543	0.015	0.022	0.034				
	(LL)			0.438	0.750	1.630	0.030	0.047	0.084				
	(HH)			0.899	1.635	3.692	0.017	0.026	0.043				
B2 → F2	(LL)			0.826	1.471	3.150	0.012	0.017	0.027				
	(HH)			0.599	1.239	2.703	0.015	0.024	0.036				
	(HL)			0.672	1.294	2.808	0.013	0.018	0.027				
B2 → F3	(LH)			0.643	1.372	2.934	0.015	0.023	0.036				
	(LL)			0.670	1.381	2.984	0.013	0.018	0.027				
	(HH)			0.724	1.358	3.123	0.015	0.022	0.033				
B2 → COUTB	(HL)			0.745	1.405	3.162	0.012	0.017	0.027				
	(LH)			0.633	1.203	2.674	0.015	0.023	0.036				
	(LL)			0.662	1.280	2.830	0.013	0.017	0.027				
B2 → X	(HL)			1.011	1.838	4.219	0.017	0.024	0.039				
	(LH)			0.891	1.623	3.551	0.014	0.021	0.030				
B2 → Y	(HH)			0.421	0.711	1.543	0.015	0.022	0.034				
	(LL)			0.438	0.750	1.630	0.030	0.047	0.084				
	(HH)			0.914	1.654	3.729	0.017	0.026	0.043				
A3 → F3	(LL)			0.814	1.483	3.208	0.012	0.017	0.027				
	(HH)			0.545	1.117	2.457	0.015	0.023	0.036				
	(HL)			0.600	1.190	2.623	0.013	0.017	0.027				
A3 → COUTB	(LH)			0.593	1.268	2.752	0.015	0.023	0.036				
	(LL)			0.642	1.241	2.740	0.013	0.018	0.027				

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
A3 → COUTB	(HL)			0.730	1.384	3.259	0.017	0.024	0.039				
	(LH)			0.626	1.136	2.441	0.014	0.021	0.030				
A3 → X	(HH)			0.360	0.605	1.312	0.015	0.022	0.034				
	(LL)			0.383	0.658	1.452	0.030	0.047	0.084				
A3 → Y	(HH)			0.632	1.201	2.769	0.017	0.026	0.043				
	(LL)			0.552	0.996	2.098	0.012	0.017	0.027				
B3 → F3	(HH)			0.556	1.116	2.457	0.015	0.023	0.036				
	(HL)			0.601	1.209	2.660	0.013	0.017	0.027				
	(LH)			0.562	1.296	2.796	0.015	0.023	0.036				
B3 → COUTB	(LL)			0.634	1.242	2.739	0.013	0.017	0.027				
	(HL)			0.745	1.403	3.295	0.017	0.024	0.039				
	(LH)			0.614	1.148	2.499	0.014	0.021	0.030				
B3 → X	(HH)			0.360	0.605	1.312	0.015	0.022	0.034				
	(LL)			0.383	0.659	1.452	0.030	0.047	0.084				
	(HH)			0.647	1.220	2.805	0.017	0.026	0.043				
B3 → Y	(LL)			0.540	1.009	2.157	0.012	0.017	0.027				
	(HH)			0.485	0.857	1.757	0.015	0.023	0.036				
	(HL)			0.529	0.947	1.926	0.013	0.017	0.027				
CINB → F0	(LH)			0.457	0.811	1.711	0.015	0.022	0.033				
	(LL)			0.457	0.813	1.649	0.012	0.017	0.026				
	(HH)			0.724	1.271	2.720	0.016	0.023	0.036				
CINB → F1	(HL)			0.749	1.340	2.873	0.013	0.018	0.027				
	(LH)			0.709	1.257	2.756	0.015	0.022	0.033				
	(LL)			0.717	1.276	2.731	0.012	0.017	0.026				
CINB → F2	(HH)			0.922	1.596	3.488	0.015	0.023	0.036				
	(HL)			0.952	1.670	3.640	0.013	0.017	0.027				
	(LH)			0.883	1.560	3.494	0.015	0.022	0.033				
CINB → F3	(LL)			0.903	1.602	3.514	0.012	0.017	0.027				
	(HH)			1.020	1.763	3.923	0.015	0.023	0.036				
	(HL)			1.051	1.836	4.065	0.013	0.017	0.027				
CINB → COUTB	(LH)			0.983	1.738	3.965	0.015	0.022	0.033				
	(LL)			1.004	1.786	4.003	0.012	0.017	0.027				
	(HH)			0.842	1.471	3.410	0.016	0.025	0.039				
CINB → COUTB	(LL)			0.595	0.982	1.995	0.018	0.026	0.043				

### Chapter 2 Function Block

Function	3-State Buffer									
Block type	Buffer type					Inverter type				
	with EN		with ENB			with EN		with ENB		
Drivability	Name	cells	Name	cells		Name	cells	Name	cells	
Low Power	L531	4	L532	4						
x1	F531	5	F532	5		F541	6	F542	6	
x2	F533	7	F534	7		F543	8	F544	8	
x4	F53F	11	F53G	11		F54F	12	F54G	12	
x8										

Logic Diagram for "Buffer with EN"					Logic Diagram for "Buffer with ENB"				
Logic Diagram for "Inverter with EN"					Logic Diagram for "Inverter with ENB"				

With EN				With ENB			
A	EN	Y	Y*	A	ENB	Y	Y*
0	1	0	1	0	0	0	1
1	1	1	0	1	0	1	0
X	0	Z	Z	X	1	Z	Z

X:Irrelevant  
Z:High Impedance  
\*:Inverter type

### Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L531	A → Y	(HH)		0.218	0.343	0.712	0.029	0.043	0.062	A	2.1	Y	10
		(LL)		0.232	0.390	0.813	0.023	0.031	0.047				
	EN → Y	(HZ)		0.441	0.667	1.283				EN	1.0	Y	0.5
		(LZ)		0.276	0.454	0.881							
		(ZH)		0.396	0.650	1.375	0.029	0.042	0.062				
		(ZL)		0.343	0.585	1.191	0.023	0.031	0.047				
F531	A → Y	(HH)		0.181	0.293	0.612	0.015	0.022	0.032	A	2.1	Y	22
		(LL)		0.213	0.363	0.752	0.012	0.016	0.025				
	EN → Y	(HZ)		0.435	0.662	1.280				EN	1.0	Y	0.5
		(LZ)		0.288	0.469	0.901							
		(ZH)		0.362	0.603	1.284	0.015	0.022	0.032				
		(ZL)		0.323	0.560	1.135	0.012	0.016	0.024				
F533	A → Y	(HH)		0.213	0.348	0.742	0.008	0.011	0.017	A	2.1	Y	43
		(LL)		0.250	0.439	0.925	0.006	0.009	0.014				
	EN → Y	(HZ)		0.500	0.757	1.436				EN	1.0	Y	0.9
		(LZ)		0.317	0.516	0.993							
		(ZH)		0.387	0.661	1.423	0.008	0.011	0.017				
		(ZL)		0.352	0.633	1.304	0.006	0.009	0.013				
F53F	A → Y	(HH)		0.271	0.452	0.989	0.004	0.006	0.009	A	2.1	Y	80
		(LL)		0.327	0.599	1.275	0.004	0.005	0.008				
	EN → Y	(HZ)		0.628	0.948	1.747				EN	1.0	Y	2.4
		(LZ)		0.387	0.625	1.189							
		(ZH)		0.434	0.764	1.674	0.004	0.006	0.009				
		(ZL)		0.419	0.788	1.653	0.004	0.005	0.008				
L532	A → Y	(HH)		0.207	0.328	0.685	0.029	0.043	0.062	A	2.1	Y	10
		(LL)		0.246	0.414	0.850	0.023	0.032	0.047				
	ENB → Y	(HZ)		0.342	0.481	0.870				ENB	1.0	Y	0.5
		(LZ)		0.360	0.566	1.093							
		(ZH)		0.307	0.521	1.122	0.029	0.042	0.062				
		(ZL)		0.446	0.782	1.627	0.023	0.032	0.047				
F532	A → Y	(HH)		0.177	0.286	0.601	0.015	0.022	0.032	A	2.1	Y	22
		(LL)		0.217	0.371	0.764	0.012	0.016	0.025				
	ENB → Y	(HZ)		0.347	0.488	0.881				ENB	1.0	Y	0.4
		(LZ)		0.368	0.578	1.109							
		(ZH)		0.277	0.481	1.044	0.015	0.022	0.032				
		(ZL)		0.418	0.744	1.554	0.012	0.016	0.025				
F534	A → Y	(HH)		0.207	0.337	0.721	0.007	0.011	0.017	A	2.1	Y	43
		(LL)		0.258	0.455	0.951	0.006	0.009	0.014				
	ENB → Y	(HZ)		0.397	0.568	1.020				ENB	1.0	Y	0.9
		(LZ)		0.404	0.634	1.209							
		(ZH)		0.293	0.523	1.160	0.008	0.011	0.017				
		(ZL)		0.455	0.826	1.735	0.006	0.009	0.014				
F53G	A → Y	(HH)		0.264	0.433	0.950	0.004	0.006	0.009	A	2.1	Y	81
		(LL)		0.341	0.630	1.329	0.004	0.005	0.009				
	ENB → Y	(HZ)		0.507	0.738	1.308				ENB	1.0	Y	2.4
		(LZ)		0.481	0.749	1.408							
		(ZH)		0.332	0.616	1.395	0.004	0.006	0.009				
		(ZL)		0.535	1.000	2.111	0.004	0.005	0.009				
F541	A → Y	(HL)		0.322	0.542	1.106	0.012	0.016	0.025	A	1.0	Y	22
		(LH)		0.291	0.513	1.120	0.015	0.022	0.032				
	EN → Y	(HZ)		0.445	0.675	1.299				EN	1.0	Y	0.5
		(LZ)		0.290	0.472	0.906							
		(ZH)		0.372	0.619	1.312	0.015	0.022	0.032				
		(ZL)		0.326	0.565	1.147	0.012	0.016	0.025				



Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F543	A → Y	(HL)		0.364	0.628	1.296	0.006	0.009	0.014	A	1.0	Y	43	
		(LH)		0.316	0.565	1.246	0.007	0.011	0.017		EN			1.0
	EN → Y	(HZ)		0.498	0.758	1.441				Y	0.9			
		(LZ)		0.331	0.535	1.020								
		(ZH)		0.391	0.666	1.434	0.008	0.011	0.017					
		(ZL)		0.365	0.652	1.337	0.006	0.009	0.014					
F54F	A → Y	(HL)		0.446	0.796	1.661	0.004	0.005	0.009	A	1.0	Y	81	
		(LH)		0.370	0.667	1.486	0.004	0.006	0.009		EN			1.0
	EN → Y	(HZ)		0.608	0.927	1.726				Y	2.4			
		(LZ)		0.406	0.651	1.227								
		(ZH)		0.431	0.759	1.668	0.004	0.006	0.009					
		(ZL)		0.439	0.818	1.701	0.004	0.005	0.009					
F542	A → Y	(HL)		0.322	0.542	1.106	0.012	0.016	0.025	A	1.0	Y	22	
		(LH)		0.291	0.513	1.120	0.015	0.022	0.032		ENB			1.0
	ENB → Y	(HZ)		0.354	0.496	0.890				Y	0.5			
		(LZ)		0.372	0.585	1.120								
		(ZH)		0.283	0.491	1.065	0.015	0.022	0.032					
		(ZL)		0.419	0.747	1.563	0.012	0.016	0.024					
F544	A → Y	(HL)		0.364	0.628	1.296	0.006	0.009	0.014	A	1.0	Y	43	
		(LH)		0.316	0.565	1.246	0.007	0.011	0.017		ENB			1.0
	ENB → Y	(HZ)		0.408	0.580	1.036				Y	0.9			
		(LZ)		0.410	0.643	1.222								
		(ZH)		0.302	0.539	1.190	0.008	0.011	0.017					
		(ZL)		0.459	0.834	1.751	0.006	0.009	0.014					
F54G	A → Y	(HL)		0.446	0.796	1.661	0.004	0.005	0.009	A	1.0	Y	81	
		(LH)		0.370	0.667	1.486	0.004	0.006	0.009		ENB			1.0
	ENB → Y	(HZ)		0.518	0.750	1.326				Y	2.4			
		(LZ)		0.483	0.753	1.415								
		(ZH)		0.342	0.633	1.428	0.004	0.006	0.009					
		(ZL)		0.533	0.999	2.114	0.004	0.005	0.009					

[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	2 to 4 Decoder											
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L560	6					L561	6				
x1	F560	10					F561	10				
x2												
x4												

Logic Diagram

for "Positive output type"                      for "Positive output with ENB"                      for "Positive output with EN"

for "Negative output type"                      for "Negative output with ENB"                      for "Negative output with EN"

Truth Table

A	B	ENB	Y0	Y1	Y2	Y3	Y0B	Y1B	Y2B	Y3B
0	0	0	1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	1	0	1	1
0	1	0	0	0	1	0	1	1	0	1
1	1	0	0	0	0	1	1	1	1	0
X	X	1	0	0	0	0	1	1	1	1

X: Irrelevant

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LdO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L560	A → Y0	(HL)		0.349	0.566	1.119	0.022	0.030	0.044	A	1.0	Y0	5
		(LH)		0.359	0.625	1.311	0.052	0.078	0.116			B	1.0
	A → Y1	(HH)		0.244	0.387	0.764	0.052	0.078	0.117			Y2	5
		(LL)		0.242	0.406	0.801	0.023	0.031	0.047			Y3	5
	A → Y2	(HL)		0.352	0.569	1.123	0.022	0.030	0.044				
		(LH)		0.363	0.631	1.320	0.052	0.078	0.116				
	A → Y3	(HH)		0.244	0.387	0.764	0.052	0.078	0.117				
		(LL)		0.242	0.407	0.801	0.023	0.031	0.047				
	B → Y0	(HL)		0.369	0.597	1.177	0.022	0.030	0.044				
		(LH)		0.372	0.652	1.356	0.052	0.078	0.115				
	B → Y1	(HL)		0.369	0.597	1.177	0.022	0.030	0.044				
		(LH)		0.372	0.652	1.355	0.052	0.078	0.115				
B → Y2	(HH)		0.254	0.413	0.812	0.052	0.078	0.115					
	(LL)		0.261	0.438	0.860	0.023	0.031	0.047					
B → Y3	(HH)		0.250	0.408	0.803	0.052	0.078	0.115					
	(LL)		0.259	0.435	0.855	0.023	0.031	0.047					
F560	A → Y0	(HL)		0.326	0.533	1.066	0.011	0.015	0.023	A	1.0	Y0	21
		(LH)		0.367	0.655	1.420	0.015	0.022	0.033			B	1.0
	A → Y1	(HH)		0.479	0.819	1.735	0.015	0.022	0.033			Y2	21
		(LL)		0.452	0.788	1.632	0.011	0.015	0.023			Y3	22
	A → Y2	(HL)		0.332	0.541	1.078	0.011	0.015	0.023				
		(LH)		0.373	0.664	1.436	0.015	0.022	0.033				
	A → Y3	(HH)		0.474	0.812	1.723	0.015	0.022	0.033				
		(LL)		0.448	0.782	1.623	0.011	0.015	0.023				
	B → Y0	(HL)		0.370	0.587	1.158	0.011	0.015	0.023				
		(LH)		0.371	0.642	1.372	0.015	0.022	0.033				
	B → Y1	(HL)		0.373	0.592	1.165	0.011	0.015	0.023				
		(LH)		0.375	0.649	1.384	0.015	0.022	0.033				
B → Y2	(HH)		0.477	0.795	1.679	0.015	0.022	0.033					
	(LL)		0.493	0.841	1.723	0.011	0.015	0.023					
B → Y3	(HH)		0.471	0.787	1.665	0.015	0.022	0.033					
	(LL)		0.487	0.833	1.711	0.011	0.015	0.023					
L561	A → Y0B	(HH)		0.221	0.339	0.649	0.029	0.043	0.063	A	1.0	Y0B	9
		(LL)		0.261	0.443	0.912	0.034	0.051	0.085			B	1.0
	A → Y1B	(HL)		0.365	0.599	1.226	0.034	0.050	0.083			Y2B	8
		(LH)		0.338	0.581	1.201	0.029	0.042	0.061			Y3B	9
	A → Y2B	(HH)		0.221	0.339	0.649	0.029	0.043	0.063				
		(LL)		0.261	0.443	0.912	0.034	0.051	0.085				
	A → Y3B	(HL)		0.362	0.595	1.218	0.034	0.050	0.083				
		(LH)		0.336	0.578	1.195	0.029	0.042	0.061				
	B → Y0B	(HH)		0.247	0.373	0.713	0.029	0.043	0.062				
		(LL)		0.252	0.415	0.850	0.034	0.050	0.083				
	B → Y1B	(HH)		0.249	0.376	0.718	0.029	0.043	0.062				
		(LL)		0.255	0.419	0.858	0.034	0.050	0.083				
B → Y2B	(HL)		0.363	0.578	1.174	0.034	0.050	0.082					
	(LH)		0.367	0.619	1.272	0.029	0.042	0.061					
B → Y3B	(HL)		0.362	0.579	1.175	0.034	0.050	0.082					
	(LH)		0.366	0.618	1.271	0.029	0.042	0.061					
F561	A → Y0B	(HH)		0.427	0.715	1.454	0.015	0.022	0.031	A	1.0	Y0B	22
		(LL)		0.521	0.929	1.956	0.012	0.017	0.025			B	1.0
	A → Y1B	(HL)		0.403	0.686	1.407	0.012	0.017	0.025			Y2B	22
		(LH)		0.317	0.556	1.146	0.015	0.022	0.031			Y3B	22
	A → Y2B	(HH)		0.427	0.715	1.454	0.015	0.022	0.031				
		(LL)		0.521	0.929	1.956	0.012	0.017	0.025				
A → Y3B	(HL)		0.403	0.686	1.407	0.012	0.017	0.025					
	(LH)		0.317	0.556	1.147	0.015	0.022	0.031					

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDo (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B → Y0B	(HH)		0.462	0.770	1.551	0.015	0.022	0.031				
		(LL)		0.544	0.972	2.028	0.012	0.017	0.025				
	B → Y1B	(HH)		0.462	0.770	1.551	0.015	0.022	0.031				
		(LL)		0.545	0.972	2.026	0.012	0.017	0.025				
	B → Y2B	(HL)		0.411	0.709	1.446	0.012	0.017	0.025				
		(LH)		0.345	0.600	1.225	0.015	0.022	0.031				
	B → Y3B	(HL)		0.411	0.709	1.446	0.012	0.017	0.025				
		(LH)		0.345	0.600	1.225	0.015	0.022	0.031				

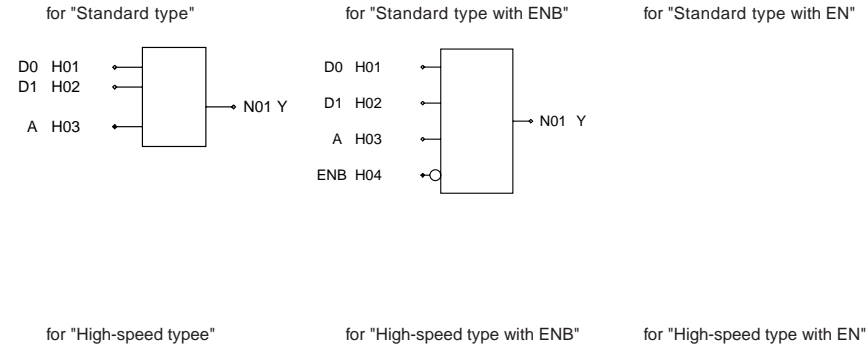
[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	2 to 1 Multiplexer (Positive out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L565	3	L571	4								
x1	F565	4	F571	6								
x2												
x4												

Logic Diagram



Truth Table

D0	D1	A	ENB	Y	YB
X	X	X	1	0	1
A	X	0	0	A	AB
X	B	1	0	B	BB

X:Irrelevant

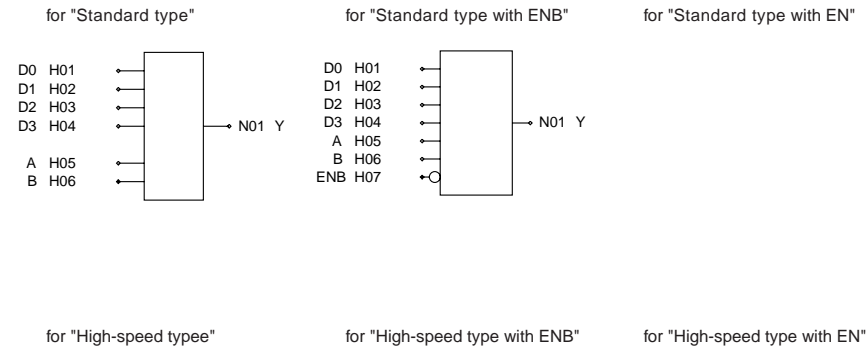
Chapter 2 Function Block

Block type	Switching speed									Input		Output							
	Path			t LDO (ns)			t 1												
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout						
L565	D0 → Y	(HH)		0.291	0.446	0.908	0.029	0.043	0.063	D0	1.0	Y	10						
			(LL)	0.326	0.541	1.119	0.024	0.033	0.049										
	D1 → Y	(HH)		0.290	0.441	0.892	0.029	0.043	0.063					D1	1.0				
			(LL)	0.322	0.541	1.126	0.024	0.032	0.049										
	A → Y	(HH)		0.208	0.324	0.631	0.029	0.043	0.063							A	2.1		
			(HL)	0.274	0.443	0.897	0.024	0.032	0.049										
	(LH)	0.259	0.435	0.908	0.029	0.043	0.063												
	(LL)	0.237	0.373	0.733	0.024	0.032	0.049												
F565	D0 → Y	(HH)		0.287	0.452	0.935	0.015	0.022	0.033	D0	1.0	Y	21						
			(LL)	0.325	0.570	1.215	0.013	0.017	0.027										
	D1 → Y	(HH)		0.284	0.450	0.931	0.015	0.022	0.033					D1	1.0				
			(LL)	0.322	0.566	1.206	0.013	0.017	0.027										
	A → Y	(HH)		0.357	0.608	1.277	0.015	0.022	0.033							A	1.0		
			(HL)	0.358	0.610	1.222	0.012	0.017	0.026										
	(LH)	0.327	0.574	1.219	0.015	0.022	0.033												
	(LL)	0.373	0.691	1.481	0.013	0.017	0.026												
L571	D0 → Y	(HH)		0.299	0.476	1.002	0.052	0.078	0.117	D0	1.0	Y	4						
			(LL)	0.310	0.530	1.115	0.024	0.033	0.049										
	D1 → Y	(HH)		0.304	0.483	1.013	0.052	0.078	0.117					D1	1.0				
			(LL)	0.316	0.539	1.130	0.024	0.033	0.050										
	A → Y	(HH)		0.370	0.634	1.354	0.052	0.078	0.117							A	1.0		
			(HL)	0.333	0.541	1.080	0.024	0.032	0.049										
		(LH)	0.333	0.583	1.252	0.052	0.078	0.117											
		(LL)	0.363	0.656	1.398	0.024	0.032	0.049											
	ENB → Y	(HL)		0.111	0.151	0.232	0.022	0.029	0.041									ENB	1.0
			(LH)	0.097	0.186	0.413	0.052	0.078	0.116										
F571	D0 → Y	(HH)		0.493	0.832	1.826	0.015	0.022	0.033	D0	1.0	Y	21						
			(LL)	0.492	0.860	1.847	0.011	0.015	0.023										
	D1 → Y	(HH)		0.491	0.830	1.823	0.015	0.022	0.033					D1	1.0				
			(LL)	0.489	0.857	1.840	0.011	0.015	0.023										
	A → Y	(HH)		0.558	0.983	2.166	0.015	0.022	0.033							A	1.0		
			(HL)	0.512	0.865	1.801	0.011	0.015	0.023										
		(LH)	0.522	0.934	2.068	0.015	0.022	0.033											
		(LL)	0.537	0.975	2.111	0.011	0.015	0.023											
	ENB → Y	(HL)		0.303	0.487	0.962	0.011	0.015	0.023									ENB	1.0
			(LH)	0.297	0.517	1.129	0.015	0.022	0.033										

Chapter 2 Function Block

Function	4 to 1 Multiplexer (Positive out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F564	8	F570	10								
x2												
x4												

Logic Diagram



Truth Table

D0	D1	D2	D3	A	B	ENB	Y	YB
X	X	X	X	X	X	1	0	1
A	X	X	X	0	0	0	A	AB
X	B	X	X	1	0	0	B	BB
X	X	C	X	0	1	0	C	CB
X	X	X	D	1	1	0	D	DB

X:Irrelevant

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F564	D0 → Y	(HH)		0.429	0.711	1.572	0.015	0.023	0.036	D0	1.0	Y	20	
		(LL)		0.482	0.896	2.029	0.015	0.021	0.031		D1			1.0
	D1 → Y	(HH)		0.426	0.707	1.566	0.015	0.023	0.036	D2	1.0			
		(LL)		0.478	0.890	2.020	0.015	0.021	0.031		D3			1.0
	D2 → Y	(HH)		0.427	0.708	1.565	0.015	0.023	0.036	A	1.0			
		(LL)		0.481	0.894	2.023	0.015	0.020	0.031		B			1.0
	D3 → Y	(HH)		0.422	0.700	1.555	0.015	0.023	0.036					
		(LL)		0.473	0.881	2.007	0.015	0.020	0.031					
	A → Y	(HH)		0.533	0.935	2.054	0.015	0.023	0.036					
		(HL)		0.546	1.025	2.236	0.015	0.020	0.031					
	B → Y	(LH)		0.501	0.907	2.020	0.015	0.023	0.036					
		(LL)		0.549	1.084	2.460	0.015	0.020	0.031					
			(HH)		0.376	0.651	1.398	0.015	0.023	0.036				
			(HL)		0.366	0.647	1.329	0.014	0.019	0.030				
		(LH)		0.343	0.611	1.323	0.015	0.023	0.036					
		(LL)		0.381	0.733	1.609	0.014	0.020	0.031					
F570	D0 → Y	(HH)		0.634	1.082	2.441	0.015	0.022	0.033	D0	1.0	Y	21	
		(LL)		0.654	1.188	2.639	0.011	0.015	0.023		D1			1.0
	D1 → Y	(HH)		0.633	1.081	2.440	0.015	0.022	0.033	D2	1.0			
		(LL)		0.652	1.186	2.636	0.011	0.015	0.023		D3			1.0
	D2 → Y	(HH)		0.628	1.073	2.427	0.015	0.022	0.033	A	1.0			
		(LL)		0.646	1.176	2.620	0.011	0.015	0.023		B			1.0
	D3 → Y	(HH)		0.630	1.077	2.432	0.015	0.022	0.033	ENB	1.0			
		(LL)		0.650	1.182	2.629	0.011	0.015	0.023					
	A → Y	(HH)		0.738	1.310	2.932	0.015	0.022	0.033					
		(HL)		0.718	1.312	2.825	0.011	0.015	0.023					
	B → Y	(LH)		0.705	1.277	2.885	0.015	0.022	0.033					
		(LL)		0.724	1.381	3.078	0.011	0.015	0.023					
			(HH)		0.587	1.037	2.298	0.015	0.022	0.033				
			(HL)		0.534	0.908	1.898	0.011	0.015	0.023				
		(LH)		0.546	0.980	2.182	0.015	0.022	0.033					
		(LL)		0.559	1.030	2.243	0.011	0.015	0.023					
ENB → Y		(HL)		0.303	0.486	0.961	0.011	0.015	0.023					
		(LH)		0.297	0.516	1.128	0.015	0.022	0.033					

Chapter 2 Function Block

Function	8 to 1 Multiplexer (Positive out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F563	18	F569	18								
x2												
x4												

Logic Diagram

for "Standard type"

for "Standard type with ENB"

for "Standard type with EN"

for "High-speed type"

for "High-speed type with ENB"

for "High-speed type with EN"

Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	A	B	C	ENB	Y	YB
X	X	X	X	X	X	X	X	X	X	X	1	0	1
A	X	X	X	X	X	X	X	0	0	0	0	A	AB
X	B	X	X	X	X	X	X	1	0	0	0	B	BB
X	X	C	X	X	X	X	X	0	1	0	0	C	CB
X	X	X	D	X	X	X	X	1	1	0	0	D	DB
X	X	X	X	E	X	X	X	0	0	1	0	E	EB
X	X	X	X	X	F	X	X	1	0	1	0	F	FB
X	X	X	X	X	X	G	X	0	1	1	0	G	GB
X	X	X	X	X	X	X	H	1	1	1	0	H	HB

X: Irrelevant

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LdO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F563	D0 → Y	(HH)		0.641	1.093	2.454	0.015	0.022	0.032	D0	1.0	Y	22
		(LL)		0.763	1.382	3.087	0.011	0.015	0.022				
	D1 → Y	(HH)		0.638	1.089	2.449	0.015	0.022	0.032	D1	1.0		
		(LL)		0.758	1.377	3.076	0.011	0.015	0.022				
	D2 → Y	(HH)		0.639	1.090	2.448	0.015	0.022	0.032	D2	1.0		
		(LL)		0.761	1.378	3.078	0.011	0.015	0.022				
	D3 → Y	(HH)		0.634	1.082	2.438	0.015	0.022	0.032	D3	1.0		
		(LL)		0.754	1.364	3.061	0.011	0.015	0.022				
	D4 → Y	(HH)		0.638	1.087	2.439	0.015	0.022	0.032	D4	1.0		
		(LL)		0.760	1.370	3.066	0.011	0.015	0.022				
	D5 → Y	(HH)		0.633	1.079	2.428	0.015	0.022	0.032	D5	1.0		
		(LL)		0.752	1.357	3.047	0.011	0.015	0.022				
	D6 → Y	(HH)		0.633	1.080	2.428	0.015	0.022	0.032	D6	1.0		
		(LL)		0.754	1.360	3.049	0.011	0.015	0.022				
	D7 → Y	(HH)		0.628	1.073	2.417	0.015	0.022	0.032	D7	1.0		
		(LL)		0.746	1.347	3.030	0.011	0.015	0.022				
	A → Y	(HH)		0.822	1.479	3.290	0.015	0.022	0.032	A	1.0		
		(HL)		0.887	1.592	3.433	0.011	0.015	0.022				
	B → Y	(LH)		0.768	1.416	3.166	0.015	0.022	0.032	B	1.0		
		(LL)		0.906	1.742	3.897	0.011	0.015	0.022				
	C → Y	(HH)		0.616	1.101	2.441	0.015	0.022	0.032	C	1.0		
		(HL)		0.610	1.068	2.337	0.011	0.015	0.022				
		(LH)		0.567	1.026	2.281	0.015	0.022	0.032				
		(LL)		0.664	1.246	2.801	0.011	0.015	0.022				
	(HH)		0.427	0.713	1.518	0.015	0.022	0.032					
	(HL)		0.523	0.883	1.904	0.011	0.015	0.022					
	(LH)		0.519	0.894	1.928	0.015	0.022	0.032					
	(LL)		0.432	0.752	1.651	0.011	0.015	0.022					
F569	D0 → Y	(HH)		0.825	1.422	3.193	0.015	0.022	0.033	D0	1.0	Y	21
		(LL)		0.827	1.480	3.262	0.011	0.015	0.023				
	D1 → Y	(HH)		0.824	1.421	3.191	0.015	0.022	0.033	D1	1.0		
		(LL)		0.826	1.479	3.259	0.011	0.015	0.023				
	D2 → Y	(HH)		0.817	1.410	3.174	0.015	0.022	0.033	D2	1.0		
		(LL)		0.818	1.465	3.238	0.011	0.015	0.023				
	D3 → Y	(HH)		0.819	1.413	3.178	0.015	0.022	0.033	D3	1.0		
		(LL)		0.820	1.467	3.242	0.011	0.015	0.023				
	D4 → Y	(HH)		0.807	1.395	3.148	0.015	0.022	0.033	D4	1.0		
		(LL)		0.811	1.451	3.217	0.011	0.015	0.023				
	D5 → Y	(HH)		0.805	1.393	3.146	0.015	0.022	0.033	D5	1.0		
		(LL)		0.808	1.448	3.210	0.011	0.015	0.023				
	D6 → Y	(HH)		0.803	1.389	3.138	0.015	0.022	0.033	D6	1.0		
		(LL)		0.803	1.439	3.196	0.011	0.015	0.023				
	D7 → Y	(HH)		0.805	1.392	3.142	0.015	0.022	0.033	D7	1.0		
		(LL)		0.805	1.442	3.200	0.011	0.015	0.023				
	A → Y	(HH)		1.024	1.821	4.047	0.015	0.022	0.033	A	1.0		
		(HL)		0.975	1.696	3.617	0.011	0.015	0.023				
	B → Y	(LH)		0.971	1.751	3.914	0.015	0.022	0.033	B	1.0		
		(LL)		0.991	1.856	4.096	0.011	0.015	0.023				
	C → Y	(HH)		0.813	1.445	3.208	0.015	0.022	0.033	C	1.0		
		(HL)		0.726	1.236	2.605	0.011	0.015	0.023				
		(LH)		0.766	1.379	3.060	0.015	0.022	0.033				
		(LL)		0.758	1.394	3.048	0.011	0.015	0.023				
	(HH)		0.460	0.794	1.712	0.015	0.022	0.033					
	(HL)		0.455	0.785	1.667	0.011	0.015	0.023					
	(LH)		0.487	0.903	2.019	0.015	0.022	0.033					
	(LL)		0.420	0.738	1.572	0.011	0.015	0.023					

Chapter 2 Function Block

Block type	Switching speed								Input		Output	
	Path	t LDo (ns)			t 1							
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
	ENB → Y	(HL) 0.296	0.478	0.950	0.011	0.015	0.023					
	(LH)	0.288	0.504	1.111	0.015	0.022	0.033					

[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	Quad 2 to 1 Multiplexer (Negative out)											
Block type	Standard type						High-speed type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power			L572	15								
x1			F572	17								
x2												
x4												

Logic Diagram

for "Standard type"

for "Standard type with ENB"

for "Standard type with EN"

for "High-speed type"

for "High-speed type with ENB"

for "High-speed type with EN"

Truth Table

Da	Da+1	A	ENB	Yn	YnB
A	X	0	0	A	AB
X	B	1	0	B	BB
X	X	X	1	0	1

X: Irrelevant  
a=2\*n(n=0 to 3)

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LdO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L572	D0	→	Y0B (HL)	0.431	0.709	1.500	0.023	0.031	0.047	D0	1.0	Y0B	10
			(LH)	0.377	0.662	1.428	0.029	0.042	0.061	D1	1.0	Y1B	10
	D1	→	Y0B (HL)	0.435	0.714	1.509	0.023	0.031	0.047	D2	1.0	Y2B	10
			(LH)	0.382	0.669	1.440	0.029	0.042	0.061	D3	1.0	Y3B	10
	D2	→	Y1B (HL)	0.430	0.708	1.499	0.023	0.031	0.047	D4	1.0		
			(LH)	0.378	0.664	1.434	0.029	0.042	0.061	D5	1.0		
	D3	→	Y1B (HL)	0.437	0.717	1.513	0.023	0.031	0.047	D6	1.0		
			(LH)	0.386	0.676	1.452	0.029	0.042	0.061	D7	1.0		
	D4	→	Y2B (HL)	0.430	0.708	1.499	0.023	0.031	0.047	A	1.0		
			(LH)	0.378	0.664	1.434	0.029	0.042	0.061	ENB	4.6		
	D5	→	Y2B (HL)	0.436	0.716	1.512	0.023	0.031	0.047				
			(LH)	0.385	0.675	1.451	0.029	0.042	0.061				
	D6	→	Y3B (HL)	0.431	0.709	1.500	0.023	0.031	0.047				
			(LH)	0.377	0.662	1.429	0.029	0.042	0.061				
	D7	→	Y3B (HL)	0.435	0.714	1.509	0.023	0.031	0.047				
			(LH)	0.382	0.669	1.440	0.029	0.042	0.061				
	A	→	Y0B (HH)	0.490	0.816	1.687	0.031	0.045	0.064				
			(HL)	0.653	1.154	2.464	0.023	0.032	0.048				
			(LH)	0.577	1.082	2.346	0.031	0.045	0.064				
			(LL)	0.577	1.032	2.194	0.023	0.032	0.048				
	A	→	Y1B (HH)	0.497	0.826	1.702	0.031	0.045	0.064				
			(HL)	0.654	1.156	2.467	0.023	0.032	0.048				
			(LH)	0.579	1.087	2.354	0.031	0.045	0.064				
			(LL)	0.580	1.037	2.204	0.023	0.032	0.048				
	A	→	Y2B (HH)	0.495	0.824	1.699	0.031	0.045	0.064				
			(HL)	0.654	1.156	2.467	0.023	0.032	0.048				
			(LH)	0.579	1.086	2.353	0.031	0.045	0.064				
			(LL)	0.579	1.036	2.202	0.023	0.032	0.048				
	A	→	Y3B (HH)	0.490	0.816	1.687	0.031	0.045	0.064				
			(HL)	0.653	1.154	2.464	0.023	0.032	0.048				
			(LH)	0.577	1.082	2.346	0.031	0.045	0.064				
			(LL)	0.577	1.032	2.194	0.023	0.032	0.048				
ENB	→	Y0B (HH)	0.186	0.289	0.539	0.031	0.045	0.064					
		(LL)	0.232	0.421	0.910	0.023	0.032	0.048					
ENB	→	Y1B (HH)	0.184	0.287	0.537	0.031	0.045	0.064					
		(LL)	0.228	0.415	0.902	0.023	0.032	0.048					
ENB	→	Y2B (HH)	0.184	0.288	0.538	0.031	0.045	0.064					
		(LL)	0.229	0.416	0.904	0.023	0.032	0.048					
ENB	→	Y3B (HH)	0.186	0.289	0.539	0.031	0.045	0.064					
		(LL)	0.232	0.421	0.910	0.023	0.032	0.048					
F572	D0	→	Y0B (HL)	0.459	0.777	1.650	0.012	0.017	0.026	D0	1.0	Y0B	22
			(LH)	0.386	0.685	1.472	0.015	0.022	0.031	D1	1.0	Y1B	22
	D1	→	Y0B (HL)	0.463	0.783	1.660	0.012	0.017	0.026	D2	1.0	Y2B	22
			(LH)	0.391	0.692	1.484	0.015	0.022	0.031	D3	1.0	Y3B	22
	D2	→	Y1B (HL)	0.462	0.782	1.657	0.012	0.017	0.026	D4	1.0		
			(LH)	0.389	0.689	1.480	0.015	0.022	0.031	D5	1.0		
	D3	→	Y1B (HL)	0.469	0.791	1.672	0.012	0.017	0.026	D6	1.0		
			(LH)	0.397	0.703	1.501	0.015	0.022	0.031	D7	1.0		
	D4	→	Y2B (HL)	0.459	0.777	1.651	0.012	0.017	0.026	A	1.0		
			(LH)	0.386	0.685	1.473	0.015	0.022	0.031	ENB	4.6		
	D5	→	Y2B (HL)	0.464	0.784	1.661	0.012	0.017	0.026				
			(LH)	0.391	0.693	1.485	0.015	0.022	0.031				
	D6	→	Y3B (HL)	0.462	0.782	1.657	0.012	0.017	0.026				
			(LH)	0.389	0.689	1.481	0.015	0.022	0.031				
D7	→	Y3B (HL)	0.466	0.787	1.666	0.012	0.017	0.026					
		(LH)	0.394	0.697	1.492	0.015	0.022	0.031					



Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	A → Y0B	(HH)		0.496	0.835	1.726	0.015	0.022	0.031				
		(HL)		0.689	1.233	2.628	0.012	0.017	0.026				
		(LH)		0.591	1.113	2.401	0.015	0.022	0.031				
		(LL)		0.609	1.105	2.352	0.012	0.017	0.026				
	A → Y1B	(HH)		0.500	0.841	1.735	0.015	0.022	0.031				
		(HL)		0.691	1.237	2.635	0.012	0.017	0.026				
		(LH)		0.593	1.117	2.408	0.015	0.022	0.031				
		(LL)		0.613	1.112	2.363	0.012	0.017	0.026				
	A → Y2B	(HH)		0.496	0.836	1.726	0.015	0.022	0.031				
		(HL)		0.689	1.233	2.629	0.012	0.017	0.026				
		(LH)		0.591	1.113	2.401	0.015	0.022	0.031				
		(LL)		0.609	1.106	2.353	0.012	0.017	0.026				
	A → Y3B	(HH)		0.501	0.843	1.737	0.015	0.022	0.031				
		(HL)		0.691	1.237	2.635	0.012	0.017	0.026				
		(LH)		0.593	1.117	2.408	0.015	0.022	0.031				
		(LL)		0.613	1.112	2.363	0.012	0.017	0.026				
	ENB → Y0B	(HH)		0.186	0.291	0.542	0.015	0.022	0.031				
		(LL)		0.257	0.485	1.053	0.012	0.017	0.026				
	ENB → Y1B	(HH)		0.186	0.291	0.542	0.015	0.022	0.031				
		(LL)		0.257	0.485	1.052	0.012	0.017	0.026				
	ENB → Y2B	(HH)		0.186	0.291	0.542	0.015	0.022	0.031				
		(LL)		0.257	0.485	1.053	0.012	0.017	0.026				
	ENB → Y3B	(HH)		0.186	0.291	0.542	0.015	0.022	0.031				
		(LL)		0.257	0.485	1.052	0.012	0.017	0.026				

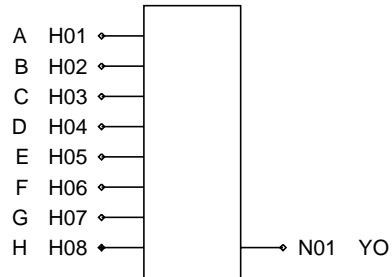
[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	8-Bit Odd Parity Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power										
x1	F581	19								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	D	E	F	G	H	YO
Σ of 1's at A through H is Odd								1
Σ of 1's at A through H is Even								0

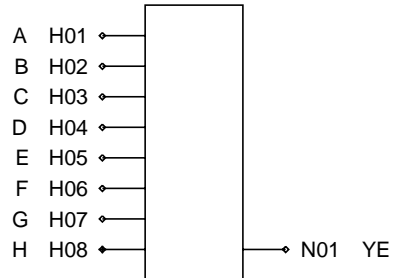
Chapter 2 Function Block

Block type	Switching speed								Input		Output				
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F581	A → YO	(HH)		0.759	1.362	3.137	0.015	0.022	0.033	A	1.7	YO	21		
		(HL)		0.747	1.335	3.022	0.011	0.015	0.023						
		(LH)		0.851	1.567	3.589	0.015	0.022	0.033						
	(LL)		0.843	1.450	3.237	0.011	0.015	0.023							
	B → YO	(HH)		0.800	1.442	3.318	0.015	0.022	0.033					B	2.0
		(HL)		0.735	1.321	3.033	0.011	0.015	0.023						
		(LH)		0.845	1.531	3.493	0.015	0.022	0.033						
	(LL)		0.861	1.526	3.391	0.011	0.015	0.023							
	C → YO	(HH)		0.746	1.320	3.034	0.015	0.022	0.033	C	1.7				
		(HL)		0.752	1.329	2.999	0.011	0.015	0.023						
		(LH)		0.841	1.531	3.496	0.015	0.022	0.033						
	(LL)		0.827	1.416	3.147	0.011	0.015	0.023							
	D → YO	(HH)		0.787	1.400	3.217	0.015	0.022	0.033			D	2.0		
		(HL)		0.738	1.314	3.010	0.011	0.015	0.023						
		(LH)		0.835	1.493	3.397	0.015	0.022	0.033						
	(LL)		0.844	1.489	3.300	0.011	0.015	0.023							
	E → YO	(HH)		0.756	1.336	3.061	0.015	0.022	0.033	E	1.7				
		(HL)		0.756	1.336	3.009	0.011	0.015	0.023						
		(LH)		0.846	1.538	3.513	0.015	0.022	0.033						
	(LL)		0.843	1.439	3.206	0.011	0.015	0.023							
	F → YO	(HH)		0.796	1.414	3.241	0.015	0.022	0.033			F	2.0		
		(HL)		0.743	1.322	3.020	0.011	0.015	0.023						
		(LH)		0.842	1.503	3.417	0.015	0.022	0.033						
	(LL)		0.861	1.514	3.361	0.011	0.015	0.023							
	G → YO	(HH)		0.756	1.313	2.993	0.015	0.022	0.033	G	1.7				
		(HL)		0.774	1.349	3.015	0.011	0.015	0.023						
		(LH)		0.850	1.521	3.452	0.015	0.022	0.033						
	(LL)		0.858	1.448	3.180	0.011	0.015	0.023							
	H → YO	(HH)		0.799	1.395	3.179	0.015	0.022	0.033			H	2.0		
		(HL)		0.761	1.335	3.026	0.011	0.015	0.023						
		(LH)		0.843	1.483	3.352	0.015	0.022	0.033						
	(LL)		0.876	1.523	3.334	0.011	0.015	0.023							

Chapter 2 Function Block

Function	8-Bit Even Parity Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
Low Power										
x1	F582	19								
x2										
x4										

Logic Diagram



Truth Table

A	B	C	D	E	F	G	H	YE
Σ of 1's at A through H is Odd								0
Σ of 1's at A through H is Even								1

Chapter 2 Function Block

Block type	Switching speed								Input		Output				
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F582	A → YE	(HH)		0.703	1.276	2.896	0.015	0.022	0.033	A	1.7	YE	21		
		(HL)		0.720	1.306	2.923	0.012	0.017	0.026						
		(LH)		0.799	1.392	3.111	0.015	0.022	0.033						
	(LL)		0.812	1.510	3.375	0.012	0.017	0.026							
	B → YE	(HH)		0.691	1.262	2.907	0.015	0.022	0.033					B	2.0
		(HL)		0.761	1.385	3.105	0.012	0.017	0.026						
		(LH)		0.817	1.467	3.265	0.015	0.022	0.033						
	(LL)		0.806	1.474	3.278	0.012	0.017	0.026							
	C → YE	(HH)		0.708	1.270	2.873	0.015	0.022	0.033	C	1.7				
		(HL)		0.715	1.275	2.839	0.012	0.017	0.026						
		(LH)		0.783	1.357	3.021	0.015	0.022	0.033						
	(LL)		0.810	1.485	3.301	0.012	0.017	0.026							
	D → YE	(HH)		0.694	1.255	2.884	0.015	0.022	0.033			D	2.0		
		(HL)		0.757	1.356	3.022	0.012	0.017	0.026						
		(LH)		0.800	1.430	3.174	0.015	0.022	0.033						
	(LL)		0.805	1.448	3.201	0.012	0.017	0.026							
	E → YE	(HH)		0.733	1.293	2.923	0.015	0.022	0.033	E	1.7				
		(HL)		0.862	1.478	3.242	0.013	0.017	0.027						
		(LH)		0.821	1.398	3.121	0.015	0.022	0.033						
	(LL)		0.953	1.683	3.694	0.013	0.017	0.027							
	F → YE	(HH)		0.720	1.279	2.933	0.015	0.022	0.033			F	2.0		
		(HL)		0.903	1.556	3.421	0.013	0.017	0.027						
		(LH)		0.839	1.473	3.276	0.015	0.022	0.033						
	(LL)		0.947	1.648	3.597	0.013	0.017	0.027							
	G → YE	(HH)		0.748	1.303	2.923	0.015	0.022	0.033	G	1.7				
		(HL)		0.868	1.464	3.186	0.013	0.017	0.027						
		(LH)		0.832	1.402	3.088	0.015	0.022	0.033						
	(LL)		0.961	1.671	3.645	0.013	0.017	0.027							
	H → YE	(HH)		0.736	1.289	2.935	0.015	0.022	0.033			H	2.0		
		(HL)		0.910	1.546	3.372	0.013	0.017	0.027						
		(LH)		0.850	1.477	3.242	0.015	0.022	0.033						
	(LL)		0.955	1.632	3.545	0.013	0.017	0.027							

[MEMO]

[MEMO]

## 2.9 RS-Latch, RS-F/F

[MEMO]

### Chapter 2 Function Block

Function	RS-Latch									
Block type	Standard type									
	Normal			High speed						
Drivability	Name	cells	Name	cells						
Low Power										
x1	F595	5								
x2										
x4										

Logic Diagram

Truth Table

S	R	G	Q	QB
0	0	1		Latch
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
1	1	1->0		Undefined
X	X	0		Latch

X:Irrelevant

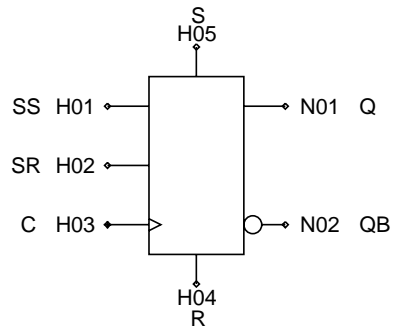
### Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
F595	S → Q	(HH)		0.296	0.509	1.134	0.015	0.022	0.034	S	1.0	Q	21	
		(LL)		0.444	0.774	1.610	0.013	0.018	0.028					
	S → QB	(HL)		0.704	1.209	2.668	0.013	0.018	0.027	R	1.0	QB	21	
		(LL)		0.443	0.774	1.611	0.013	0.018	0.028					
	R → Q	(HH)		0.297	0.509	1.135	0.015	0.022	0.034	G	1.6			
		(LL)		0.443	0.774	1.611	0.013	0.018	0.028					
	G → Q	(HH)		0.297	0.505	1.088	0.015	0.022	0.034					
		(HL)		0.697	1.201	2.614	0.013	0.018	0.026					
	G → QB	(HH)		0.298	0.507	1.090	0.015	0.022	0.034					
		(HL)		0.697	1.202	2.614	0.013	0.018	0.027					
	Set up time	S			1.170		2.150							
	Set up time	R			1.170		2.180							
	Hold time	S			0.080		0.000							
	Hold time	R			0.040		0.000							
Min Pulse	G			1.081		3.300								

### Chapter 2 Function Block

Function	RS-F/F with R, S										
Block type	Standard type										
	Normal				High speed						
Drivability	Name	cells	Name	cells							
Low Power											
x1	F596	11									
x2											
x4											

Logic Diagram



Truth Table

SS	SR	C	R	S	Q	QB
0	0	/	0	0	Hold	
1	0	/	0	0	1	0
X	1	/	0	0	0	1
X	X	\	0	0	Hold	
X	X	X	0	1	1	0
X	X	X	1	0	0	1
X	X	X	1	1	1	1

← Prohibition

X:Irrelevant

### Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F596	C → Q	(HH)		0.470	0.802	1.677	0.015	0.022	0.032	SS	1.0	Q	22
		(HL)		0.625	1.115	2.377	0.012	0.018	0.028				
	C → QB	(HH)		0.814	1.483	3.222	0.015	0.021	0.030	C	1.0	QB	21
		(HL)		0.834	1.455	3.078	0.013	0.019	0.029				
	R → Q	(HL)		0.532	1.048	2.248	0.012	0.017	0.027	R	2.1		
	R → QB	(HH)		0.261	0.462	0.866	0.015	0.023	0.034				
	S → Q	(HH)		0.208	0.324	0.608	0.015	0.022	0.032	S	2.2		
	S → QB	(HL)		0.570	1.229	2.537	0.014	0.021	0.033				
	Set up time	SS		1.000		3.260							
	Set up time	SR		1.020		3.590							
	Hold time	SS		0.270		0.000							
	Hold time	SR		0.450		0.070							
	Release time	R		0.670		2.080							
	Release time	S		0.220		0.000							
Removal time	R		0.620		0.410								
Removal time	S		1.050		1.860								
Min Pulse	C		1.133		3.796								
Min Pulse	R		1.005		2.983								
Min Pulse	S		0.961		3.123								

[MEMO]

[MEMO]



## 2.10 D-Latch

[MEMO]

## Chapter 2 Function Block

Function	D-Latch																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power									L601	4																		
x1	F601	6	F601NQ	5	F601NB	5																						
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	Q	QB	0	1	0	1	1	1	1	0	X	0	Latch	
D	G	Q	QB																									
0	1	0	1																									
1	1	1	0																									
X	0	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	Q	0	1	0	1	1	1	X	0	Latch				
D	G	Q																										
0	1	0																										
1	1	1																										
X	0	Latch																										
Logic Diagram for "QB output"				Truth Table for "QB output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	QB	0	1	1	1	1	0	X	0	Latch				
D	G	QB																										
0	1	1																										
1	1	0																										
X	0	Latch																										

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F601	D → Q	(HH)		0.583	0.979	2.089	0.015	0.022	0.031	D	1.0	Q	20
			(LL)	0.624	1.082	2.317	0.012	0.016	0.023				
	D → QB	(HL)		0.445	0.727	1.510	0.012	0.016	0.024	G	1.0	QB	20
			(LH)	0.448	0.773	1.648	0.015	0.023	0.033				
	G → Q	(HH)		0.653	1.137	2.440	0.015	0.022	0.031				
			(HL)	0.640	1.083	2.266	0.012	0.016	0.023				
	G → QB	(HH)		0.464	0.775	1.599	0.015	0.023	0.033				
			(HL)	0.517	0.886	1.862	0.012	0.016	0.024				
		Set up time	D		0.880		1.560						
		Hold time	D		0.420		0.120						
	Min Pulse	G		0.894		2.953							
L601	D → Q	(HH)		0.322	0.505	1.040	0.030	0.044	0.067	D	1.0	Q	10
			(LL)	0.361	0.624	1.311	0.026	0.036	0.055				
	G → Q	(HH)		0.386	0.652	1.369	0.030	0.044	0.067	G	1.0	QB	10
			(HL)	0.386	0.656	1.311	0.025	0.035	0.055				
		Set up time	D		0.880		1.580						
	Hold time	D		0.450		0.270							
	Min Pulse	G		0.633		1.879							
F601NQ	D → Q	(HH)		0.345	0.553	1.158	0.016	0.023	0.035	D	1.0	Q	18
			(LL)	0.391	0.694	1.480	0.013	0.018	0.028				
	G → Q	(HH)		0.416	0.708	1.495	0.016	0.023	0.035	G	1.0	QB	18
			(HL)	0.427	0.754	1.545	0.013	0.018	0.028				
		Set up time	D		0.900		1.750						
	Hold time	D		0.440		0.190							
	Min Pulse	G		0.679		2.056							
F601NB	D → QB	(HL)		0.441	0.724	1.507	0.012	0.016	0.024	D	1.0	QB	20
			(LH)	0.444	0.768	1.644	0.015	0.023	0.033				
	G → QB	(HH)		0.465	0.778	1.606	0.015	0.023	0.033	G	1.0	QB	20
			(HL)	0.514	0.884	1.861	0.012	0.016	0.024				
		Set up time	D		0.870		1.490						
	Hold time	D		0.450		0.220							
	Min Pulse	G		0.746		2.374							

Chapter 2 Function Block

Function	D-Latch, High Speed																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power																												
x1	F6R1	6																										
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	Q	QB	0	1	0	1	1	1	1	0	X	0	Latch	
D	G	Q	QB																									
0	1	0	1																									
1	1	1	0																									
X	0	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F6R1	D → Q	(HH)		0.320	0.513	1.067	0.015	0.023	0.035	D	1.0	Q	21
			(LL)	0.363	0.649	1.384	0.013	0.019	0.029				
	D → QB	(HL)		0.486	0.828	1.777	0.011	0.015	0.023	G	1.0	QB	22
			(LH)	0.507	0.940	2.062	0.014	0.021	0.030				
	G → Q	(HH)		0.388	0.665	1.397	0.015	0.023	0.034				
			(HL)	0.397	0.707	1.447	0.013	0.019	0.029				
	G → QB	(HH)		0.538	0.994	2.123	0.014	0.021	0.030				
			(HL)	0.555	0.979	2.107	0.011	0.015	0.023				
	Set up time	D		0.950		1.960							
	Hold time	D		0.460		0.230							
Min Pulse	G		0.790		2.635								

Chapter 2 Function Block

Function	D-Latch with R																																				
Block type	Standard type					Low Gate type																															
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power								L602	5																												
x1	F602	6	F602NQ	6	F602NB	5																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	G	R	Q	QB																																	
1	1	0	1	0																																	
0	1	0	0	1																																	
X	0	0	Latch																																		
X	X	1	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>R</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	R	Q	1	1	0	1	0	1	0	0	X	0	0	Latch	X	X	1	0					
D	G	R	Q																																		
1	1	0	1																																		
0	1	0	0																																		
X	0	0	Latch																																		
X	X	1	0																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	G	R	QB																																		
1	1	0	0																																		
0	1	0	1																																		
X	0	0	Latch																																		
X	X	1	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F602	D → Q	(HH)		0.684	1.203	2.605	0.014	0.021	0.030	D	1.0	Q	22
			(LL)	0.608	1.066	2.280	0.012	0.016	0.023				
	D → QB	(HL)		0.518	0.889	1.873	0.013	0.018	0.028	G	1.0	QB	22
			(LH)	0.418	0.736	1.573	0.015	0.022	0.032				
	G → Q	(HH)		0.754	1.358	2.951	0.014	0.021	0.030	R	1.0		
			(HL)	0.621	1.062	2.223	0.012	0.016	0.023				
	G → QB	(HH)		0.432	0.734	1.519	0.015	0.022	0.032				
			(HL)	0.589	1.044	2.219	0.013	0.018	0.028				
	R → Q	(HL)		0.400	0.787	1.582	0.012	0.017	0.026				
			(LH)	0.481	0.910	2.004	0.014	0.021	0.030				
	R → QB	(HH)		0.214	0.332	0.622	0.015	0.022	0.032				
			(LL)	0.316	0.596	1.273	0.013	0.018	0.028				
	Set up time	D		0.900		1.610							
	Hold time	D		0.330		0.000							
Release time	R		0.660		0.920								
Removal time	R		0.550		0.320								
Min Pulse	G		0.986		3.464								
Min Pulse	R		0.751		2.285								
L602	D → Q	(HH)		0.560	0.933	1.997	0.029	0.042	0.062	D	1.0	Q	10
			(LL)	0.544	0.934	1.987	0.023	0.031	0.045				
	G → Q	(HH)		0.620	1.077	2.328	0.029	0.042	0.062	G	1.0		
			(HL)	0.561	0.934	1.932	0.023	0.031	0.045				
	R → Q	(HL)		0.336	0.681	1.341	0.023	0.033	0.051	R	1.0		
			(LH)	0.353	0.632	1.384	0.029	0.042	0.062				
	Set up time	D		0.840		1.440							
	Hold time	D		0.410		0.120							
	Release time	R		0.550		0.430							
	Removal time	R		0.660		0.800							
Min Pulse	G		0.846		2.835								
Min Pulse	R		0.594		1.808								
F602NQ	D → Q	(HH)		0.457	0.781	1.747	0.017	0.026	0.042	D	1.0	Q	17
			(LL)	0.391	0.712	1.518	0.014	0.020	0.031				
	G → Q	(HH)		0.469	0.819	1.751	0.017	0.026	0.042	G	1.0		
			(HL)	0.429	0.777	1.607	0.014	0.020	0.031				
	R → Q	(HL)		0.463	0.806	1.529	0.012	0.019	0.030	R	1.0		
			(LH)	0.531	0.937	2.123	0.017	0.026	0.042				
	Set up time	D		0.980		1.980							
	Hold time	D		0.330		0.000							
	Release time	R		0.980		2.330							
	Removal time	R		0.300		0.000							
Min Pulse	G		0.705		2.272								
Min Pulse	R		0.705		2.493								
F602NB	D → QB	(HL)		0.519	0.892	1.881	0.013	0.018	0.028	D	1.0	QB	22
			(LH)	0.418	0.737	1.575	0.015	0.022	0.032				
	G → QB	(HH)		0.432	0.736	1.524	0.015	0.022	0.032	G	1.0		
			(HL)	0.588	1.046	2.226	0.013	0.018	0.028				
	R → QB	(HH)		0.214	0.333	0.624	0.015	0.022	0.032	R	1.0		
			(LL)	0.317	0.599	1.281	0.013	0.018	0.028				
	Set up time	D		0.870		1.520							
	Hold time	D		0.350		0.000							
	Release time	R		0.630		0.860							
	Removal time	R		0.590		0.480							
Min Pulse	G		0.821		2.739								
Min Pulse	R		0.571		1.550								

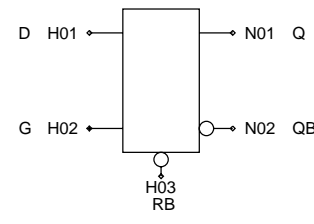
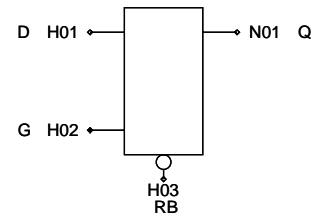
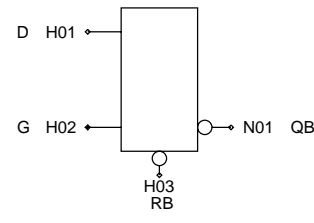
Chapter 2 Function Block

Function	D-Latch with R, High Speed																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F6R2	7																																			
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	G	R	Q	QB																																	
1	1	0	1	0																																	
0	1	0	0	1																																	
X	0	0		Latch																																	
X	X	1	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F6R2	D	→	Q	(HH)	0.452	0.772	1.733	0.017	0.026	0.041	D	1.0	Q	17
				(LL)	0.388	0.705	1.503	0.014	0.020	0.031	G	1.0	QB	22
	D	→	QB	(HL)	0.651	1.147	2.590	0.012	0.016	0.023	R	1.0		
				(LH)	0.555	1.033	2.244	0.014	0.021	0.030				
	G	→	Q	(HH)	0.448	0.789	1.705	0.017	0.026	0.041				
				(HL)	0.411	0.749	1.564	0.014	0.020	0.031				
	G	→	QB	(HH)	0.575	1.074	2.303	0.015	0.021	0.030				
				(HL)	0.646	1.164	2.563	0.012	0.016	0.023				
	R	→	Q	(HL)	0.458	0.797	1.512	0.012	0.019	0.030				
				(LH)	0.523	0.924	2.102	0.017	0.026	0.041				
	R	→	QB	(HH)	0.614	1.108	2.218	0.014	0.021	0.031				
				(LL)	0.721	1.299	2.959	0.012	0.016	0.023				
	Set up time	D			1.050		2.230							
	Hold time	D			0.330		0.000							
	Release time	R			1.050		2.580							
	Removal time	R			0.290		0.000							
Min Pulse	G			0.872		3.074								
Min Pulse	R			0.893		3.330								

Chapter 2 Function Block

Function	D-Latch with RB																																		
Block type	Standard type					Low Gate type																													
	Normal		Q output		QB output	Normal		Q output		QB output																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power							L603	5																											
x1	F603	7	F603NQ	5	F603NB	6																													
x2																																			
x4																																			
Logic Diagram for "Normal"		Truth Table for "Normal"																																	
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D	G	RB	Q	QB																															
1	1	1	1	0																															
0	1	1	0	1																															
X	0	1	Latch																																
X	X	0	0	1																															
Logic Diagram for "Q output"		Truth Table for "Q output"																																	
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D	G	RB	Q																																
1	1	1	1																																
0	1	1	0																																
X	0	1	Latch																																
X	X	0	0																																
Logic Diagram for "QB output"		Truth Table for "QB output"																																	
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D	G	RB	QB																																
1	1	1	0																																
0	1	1	1																																
X	0	1	Latch																																
X	X	0	1																																

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F603	D → Q	(HH)		0.691	1.213	2.620	0.014	0.021	0.030	D	1.0	Q	22
			(LL)	0.613	1.073	2.291	0.012	0.016	0.023				
	D → QB	(HL)		0.521	0.893	1.880	0.013	0.018	0.028	G	1.0	QB	22
			(LH)	0.419	0.738	1.576	0.015	0.022	0.032				
	G → Q	(HH)		0.761	1.368	2.966	0.014	0.021	0.030	RB	1.0		
			(HL)	0.626	1.069	2.234	0.012	0.016	0.023				
	G → QB	(HH)		0.433	0.736	1.522	0.015	0.022	0.032				
			(HL)	0.592	1.049	2.226	0.013	0.018	0.028				
	RB → Q	(HH)		0.596	1.076	2.284	0.014	0.021	0.030				
			(LL)	0.480	0.956	1.973	0.012	0.017	0.026				
	RB → QB	(HL)		0.427	0.757	1.545	0.013	0.018	0.028				
			(LH)	0.290	0.496	1.008	0.015	0.022	0.032				
	Set up time	D		0.910		1.620							
	Hold time	D		0.330		0.000							
Release time	RB		0.780		1.270								
Removal time	RB		0.430		0.000								
Min Pulse	G		0.993		3.479								
Min Pulse	RB		0.782		2.683								
L603	D → Q	(HH)		0.564	0.952	2.026	0.029	0.042	0.062	D	1.0	Q	10
			(LL)	0.564	0.966	2.047	0.023	0.031	0.045				
	G → Q	(HH)		0.627	1.097	2.357	0.029	0.042	0.062	G	1.0		
			(HL)	0.579	0.965	1.992	0.023	0.031	0.045				
	RB → Q	(HH)		0.449	0.757	1.589	0.029	0.042	0.062	RB	1.0		
			(LL)	0.407	0.810	1.638	0.022	0.033	0.051				
	Set up time	D		0.860		1.470							
	Hold time	D		0.430		0.170							
	Release time	RB		0.630		0.590							
	Removal time	RB		0.580		0.640							
Min Pulse	G		0.853		2.865								
Min Pulse	RB		0.676		2.036								
F603NQ	D → Q	(HH)		0.454	0.775	1.738	0.018	0.027	0.043	D	1.0	Q	16
			(LL)	0.385	0.702	1.503	0.014	0.020	0.031				
	G → Q	(HH)		0.462	0.810	1.737	0.018	0.027	0.043	G	1.0		
			(HL)	0.420	0.762	1.585	0.014	0.020	0.031				
	RB → Q	(HH)		0.452	0.785	1.798	0.018	0.027	0.043	RB	1.0		
			(LL)	0.371	0.668	1.254	0.012	0.019	0.030				
	Set up time	D		0.970		1.960							
	Hold time	D		0.340		0.000							
	Release time	RB		0.920		1.970							
	Removal time	RB		0.360		0.000							
Min Pulse	G		0.697		2.257								
Min Pulse	RB		0.787		2.208								
F603NB	D → QB	(HL)		0.522	0.897	1.889	0.013	0.018	0.029	D	1.0	QB	22
			(LH)	0.420	0.739	1.579	0.015	0.022	0.032				
	G → QB	(HH)		0.434	0.738	1.527	0.015	0.022	0.032	G	1.0		
			(HL)	0.592	1.051	2.233	0.013	0.018	0.029				
	RB → QB	(HL)		0.427	0.760	1.553	0.013	0.018	0.029	RB	1.0		
			(LH)	0.290	0.497	1.010	0.015	0.022	0.032				
	Set up time	D		0.870		1.530							
	Hold time	D		0.350		0.000							
	Release time	RB		0.740		1.210							
	Removal time	RB		0.470		0.130							
Min Pulse	G		0.824		2.747								
Min Pulse	RB		0.613		1.951								

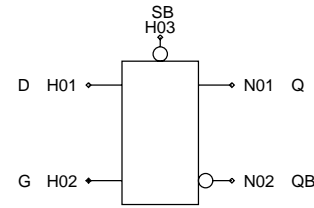
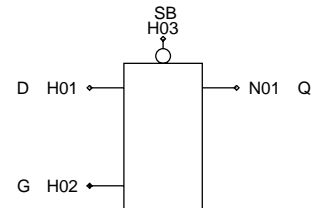
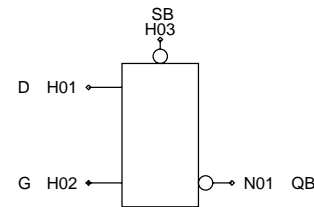
Chapter 2 Function Block

Function	D-Latch with RB, High Speed																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F6R5	6																																			
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	G	RB	Q	QB																																	
1	1	1	1	0																																	
0	1	1	0	1																																	
X	0	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F6R5	D → Q	(HH)		0.450	0.769	1.727	0.017	0.026	0.041	D	1.0	Q	17
			(LL)	0.387	0.703	1.499	0.014	0.020	0.031				
	D → QB	(HL)		0.632	1.119	2.547	0.012	0.016	0.023	G	1.0	QB	22
			(LH)	0.539	1.010	2.210	0.014	0.021	0.030				
	G → Q	(HH)		0.446	0.786	1.700	0.017	0.026	0.041	RB	1.0		
			(HL)	0.409	0.747	1.559	0.014	0.020	0.031				
	G → QB	(HH)		0.560	1.051	2.268	0.014	0.021	0.030				
			(HL)	0.628	1.136	2.520	0.012	0.016	0.023				
	RB → Q	(HH)		0.441	0.770	1.776	0.017	0.026	0.041				
			(LL)	0.368	0.662	1.242	0.012	0.019	0.030				
	RB → QB	(HL)		0.623	1.120	2.596	0.012	0.016	0.023				
			(LH)	0.500	0.939	1.899	0.014	0.021	0.030				
	Set up time	D		1.040		2.210							
	Hold time	D		0.330		0.000							
	Release time	RB		0.980		2.200							
Removal time	RB		0.350		0.000								
Min Pulse	G		0.854		3.031								
Min Pulse	RB		0.967		3.005								

Chapter 2 Function Block

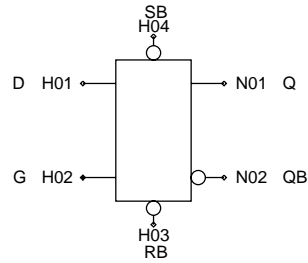
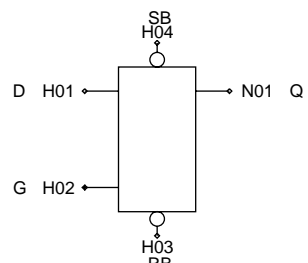
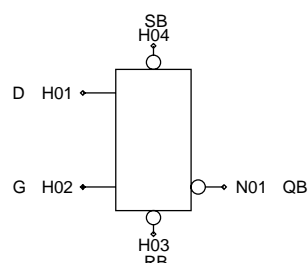
Function	D-Latch with SB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F60K	7	F60KNQ	6	F60KNB	5																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	G	SB	Q	QB																																	
0	1	1	0	1																																	
1	1	1	1	0																																	
X	0	1	Latch																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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D	G	SB	Q																																		
0	1	1	0																																		
1	1	1	1																																		
X	0	1	Latch																																		
X	X	0	1																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	G	SB	QB																																		
0	1	1	1																																		
1	1	1	0																																		
X	0	1	Latch																																		
X	X	0	0																																		

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F60K	D → Q	(HH)		0.346	0.549	1.147	0.015	0.023	0.035	D	1.0	Q	20
		(LL)		0.611	1.054	2.315	0.017	0.025	0.039				
	D → QB	(HL)		0.528	0.887	1.900	0.012	0.016	0.023	G	1.0	QB	21
		(LH)		0.807	1.443	3.195	0.014	0.021	0.029				
	G → Q	(HH)		0.414	0.696	1.466	0.015	0.023	0.035	SB	1.0		
		(HL)		0.464	0.844	1.830	0.017	0.025	0.039				
	G → QB	(HH)		0.655	1.227	2.707	0.014	0.021	0.029				
		(HL)		0.596	1.033	2.216	0.012	0.016	0.023				
	SB → Q	(HL)		0.738	1.272	2.732	0.017	0.025	0.039				
		(LH)		0.361	0.580	1.165	0.015	0.024	0.037				
	SB → QB	(HH)		0.933	1.660	3.612	0.014	0.021	0.029				
		(LL)		0.552	0.944	1.978	0.012	0.016	0.024				
	Set up time	D		1.280		3.160							
	Hold time	D		0.440		0.160							
Release time	SB		1.360		3.610								
Removal time	SB		0.010		0.000								
Min Pulse	G		0.909		3.214								
Min Pulse	SB		1.095		4.013								
F60KNQ	D → Q	(HH)		0.347	0.551	1.151	0.015	0.023	0.035	D	1.0	Q	20
		(LL)		0.615	1.065	2.331	0.018	0.026	0.041				
	G → Q	(HH)		0.411	0.693	1.464	0.015	0.023	0.035	G	1.0		
		(HL)		0.464	0.850	1.842	0.018	0.025	0.041				
	SB → Q	(HL)		0.742	1.282	2.749	0.018	0.026	0.041	SB	1.0		
		(LH)		0.360	0.582	1.169	0.015	0.023	0.036				
	Set up time	D		1.220		2.920							
	Hold time	D		0.430		0.150							
	Release time	SB		1.300		3.370							
	Removal time	SB		0.010		0.000							
Min Pulse	G		0.715		2.346								
Min Pulse	SB		0.903		3.149								
F60KNB	D → QB	(HL)		0.422	0.699	1.455	0.012	0.016	0.024	D	1.0	QB	21
		(LH)		0.485	0.865	1.919	0.015	0.022	0.034				
	G → QB	(HH)		0.500	0.870	1.881	0.015	0.022	0.034	G	1.0		
		(HL)		0.494	0.856	1.804	0.012	0.016	0.024				
	SB → QB	(HH)		0.245	0.421	0.946	0.015	0.022	0.034	SB	1.0		
		(LL)		0.249	0.413	0.812	0.012	0.016	0.024				
	Set up time	D		0.920		1.710							
	Hold time	D		0.450		0.200							
	Release time	SB		0.600		0.620							
	Removal time	SB		0.610		0.610							
Min Pulse	G		0.753		2.397								
Min Pulse	SB		0.525		1.333								



Chapter 2 Function Block

Function	D-Latch with RB, SB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F60J	7	F60JNQ	6	F60JNB	6																																																
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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D	G	RB	SB	Q	QB																																																	
0	1	1	1	0	1																																																	
1	1	1	1	1	0																																																	
X	0	1	1	Latch																																																		
X	X	0	1	0	1																																																	
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Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
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D	G	RB	SB	Q																																																		
0	1	1	1	0																																																		
1	1	1	1	1																																																		
X	0	1	1	Latch																																																		
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Logic Diagram for "QB output"				Truth Table for "QB output"																																																		
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D	G	RB	SB	QB																																																		
0	1	1	1	1																																																		
1	1	1	1	0																																																		
X	0	1	1	Latch																																																		
X	X	0	1	1																																																		
X	X	1	0	0																																																		
X	X	0	0	1																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F60J	D → Q	(HH)		0.480	0.808	1.829	0.017	0.026	0.042	D	1.0	Q	15
		(LL)		0.644	1.132	2.485	0.018	0.026	0.040				
	D → QB	(HL)		0.684	1.191	2.703	0.012	0.016	0.023	G	1.0	QB	21
		(LH)		0.851	1.541	3.402	0.014	0.021	0.029				
	G → Q	(HH)		0.476	0.821	1.788	0.017	0.026	0.042	RB	1.0		
		(HL)		0.477	0.890	1.959	0.018	0.026	0.040				
	G → QB	(HH)		0.681	1.296	2.876	0.015	0.021	0.029	SB	1.0		
		(HL)		0.679	1.203	2.660	0.012	0.016	0.023				
	RB → Q	(HH)		0.464	0.802	1.868	0.017	0.026	0.042				
		(LL)		0.390	0.692	1.315	0.013	0.019	0.031				
	RB → QB	(HL)		0.668	1.185	2.741	0.012	0.016	0.023				
		(LH)		0.549	1.004	2.023	0.015	0.021	0.031				
	SB → Q	(HL)		0.779	1.355	2.906	0.018	0.026	0.040				
		(LH)		0.529	0.893	1.953	0.016	0.027	0.044				
	SB → QB	(HH)		0.986	1.764	3.823	0.014	0.021	0.029				
		(LL)		0.745	1.310	2.916	0.012	0.016	0.024				
		Set up time	D		1.310		3.350						
		Hold time	D		0.270		0.000						
	Release time	RB		1.000		2.290							
	Release time	SB		1.410		3.800							
	Removal time	RB		0.330		0.000							
	Removal time	SB		0.000		0.000							
	Min Pulse	G		0.925		3.382							
	Min Pulse	RB		1.024		3.149							
	Min Pulse	SB		1.144		4.231							
F60JNQ	D → Q	(HH)		0.483	0.816	1.841	0.017	0.026	0.043	D	1.0	Q	15
		(LL)		0.648	1.143	2.501	0.018	0.026	0.042				
	G → Q	(HH)		0.478	0.827	1.797	0.017	0.026	0.043	G	1.0		
		(HL)		0.480	0.900	1.975	0.018	0.026	0.042				
	RB → Q	(HH)		0.468	0.810	1.880	0.017	0.026	0.043	RB	1.0		
		(LL)		0.390	0.696	1.324	0.013	0.019	0.030				
	SB → Q	(HL)		0.783	1.365	2.921	0.018	0.026	0.042	SB	1.0		
		(LH)		0.530	0.901	1.969	0.016	0.027	0.045				
		Set up time	D		1.230		3.100						
		Hold time	D		0.270		0.000						
		Release time	RB		0.950		2.090						
		Release time	SB		1.340		3.550						
		Removal time	RB		0.330		0.000						
		Removal time	SB		0.000		0.000						
		Min Pulse	G		0.726		2.482						
		Min Pulse	RB		0.813		2.288						
		Min Pulse	SB		0.942		3.328						
	F60JNB	D → QB	(HL)		0.548	0.945	2.093	0.012	0.016	0.025	D	1.0	QB
(LH)				0.528	0.958	2.114	0.015	0.022	0.034				
G → QB		(HH)		0.560	0.998	2.125	0.015	0.022	0.034	G	1.0		
		(HL)		0.565	0.995	2.130	0.012	0.016	0.025				
RB → QB		(HL)		0.544	0.950	2.148	0.012	0.016	0.025	RB	1.0		
		(LH)		0.513	0.949	1.990	0.015	0.022	0.034				
SB → QB		(HH)		0.243	0.417	0.937	0.015	0.022	0.034	SB	1.0		
		(LL)		0.246	0.407	0.799	0.012	0.016	0.024				
		Set up time	D		0.940		1.860						
		Hold time	D		0.290		0.000						
		Release time	RB		0.880		1.750						
		Release time	SB		0.560		0.540						
		Removal time	RB		0.340		0.000						
		Removal time	SB		0.660		0.760						

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
	Min Pulse	G	0.814		2.651								
	Min Pulse	RB	0.903		2.572								
	Min Pulse	SB	0.524		1.318								

[MEMO]

Chapter 2 Function Block

Chapter 2 Function Block

Function	D-Latch (GB)																									
Block type	Standard type					Low Gate type																				
	Normal		Q output		QB output	Normal		Q output		QB output																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power							L604	4																		
x1	F604	6	F604NQ	5	F604NB	5																				
x2																										
x4																										
Logic Diagram for "Normal"			Truth Table for "Normal"																							
			<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								D	GB	Q	QB	1	0	1	0	0	0	0	1	X	1	Latch	
D	GB	Q	QB																							
1	0	1	0																							
0	0	0	1																							
X	1	Latch																								
Logic Diagram for "Q output"			Truth Table for "Q output"																							
			<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								D	GB	Q	1	0	1	0	0	0	X	1	Latch				
D	GB	Q																								
1	0	1																								
0	0	0																								
X	1	Latch																								
Logic Diagram for "QB output"			Truth Table for "QB output"																							
			<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								D	GB	QB	1	0	0	0	0	1	X	1	Latch				
D	GB	QB																								
1	0	0																								
0	0	1																								
X	1	Latch																								

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F604	D → Q	(HH)		0.557	0.943	2.017	0.015	0.021	0.031	D	1.0	Q	22
				0.600	1.048	2.248	0.012	0.016	0.023				
	D → QB	(HL)		0.420	0.690	1.433	0.012	0.016	0.024	GB	1.0	QB	22
				0.421	0.734	1.565	0.015	0.022	0.032				
	GB → Q	(LH)		0.589	1.049	2.263	0.015	0.021	0.031				
				0.647	1.165	2.519	0.012	0.016	0.023				
	GB → QB	(LH)		0.469	0.852	1.837	0.015	0.022	0.032				
				0.452	0.795	1.679	0.012	0.016	0.024				
		Set up time	D		0.850		1.450						
		Hold time	D		0.410		0.000						
	Min Pulse	GB		0.881		2.985							
L604	D → Q	(HH)		0.324	0.508	1.044	0.030	0.044	0.067	D	1.0	Q	10
				0.364	0.628	1.317	0.026	0.036	0.055				
	GB → Q	(LH)		0.358	0.619	1.314	0.030	0.044	0.067	GB	1.0	QB	10
				0.400	0.732	1.562	0.025	0.035	0.055				
		Set up time	D		0.870		1.380						
	Hold time	D		0.400		0.000							
	Min Pulse	GB		0.637		2.030							
F604NQ	D → Q	(HH)		0.345	0.553	1.158	0.016	0.023	0.035	D	1.0	Q	18
				0.391	0.694	1.479	0.013	0.018	0.028				
	GB → Q	(LH)		0.389	0.682	1.461	0.016	0.023	0.035	GB	1.0	QB	18
				0.436	0.812	1.745	0.013	0.018	0.028				
		Set up time	D		0.880		1.520						
	Hold time	D		0.390		0.000							
	Min Pulse	GB		0.682		2.219							
F604NB	D → QB	(HL)		0.441	0.723	1.506	0.012	0.016	0.024	D	1.0	QB	20
				0.444	0.768	1.644	0.015	0.023	0.033				
	GB → QB	(LH)		0.495	0.893	1.924	0.015	0.023	0.033	GB	1.0	QB	20
				0.477	0.834	1.761	0.012	0.016	0.024				
		Set up time	D		0.840		1.390						
	Hold time	D		0.430		0.000							
	Min Pulse	GB		0.730		2.391							

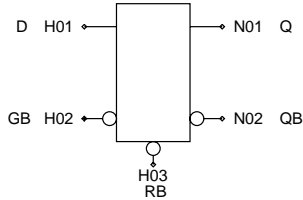
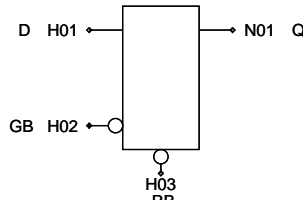
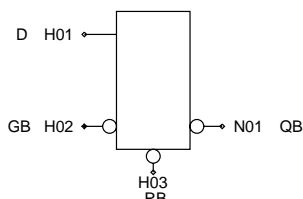
Chapter 2 Function Block

Function	D-Latch (GB), High Speed																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power																												
x1	F6R8	6																										
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	Q	QB	1	0	1	0	0	0	0	1	X	1	Latch	
D	GB	Q	QB																									
1	0	1	0																									
0	0	0	1																									
X	1	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F6R8	D	→	Q (HH)	0.323	0.517	1.072	0.015	0.023	0.035	D	1.0	Q	21
			(LL)	0.368	0.656	1.394	0.013	0.019	0.029				
	D	→	QB (HL)	0.490	0.832	1.783	0.011	0.015	0.023	GB	1.0	QB	22
			(LH)	0.512	0.947	2.073	0.014	0.021	0.030				
	GB	→	Q (LH)	0.362	0.640	1.365	0.015	0.023	0.035				
			(LL)	0.404	0.761	1.640	0.013	0.019	0.029				
	GB	→	QB (LH)	0.546	1.050	2.317	0.014	0.021	0.030				
			(LL)	0.529	0.955	2.077	0.011	0.015	0.023				
	Set up time		D	0.920		1.750							
	Hold time		D	0.390		0.000							
Min Pulse		GB	0.792		2.792								

Chapter 2 Function Block

Function	D-Latch (GB) with RB																																				
Block type	Standard type					Low Gate type																															
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power								L605	5																												
x1	F605	7	F605NQ	5	F605NB	6																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	QB	1	0	1	1	0	0	0	1	0	1	X	1	1	Latch		X	X	0	0	1
D	GB	RB	Q	QB																																	
1	0	1	1	0																																	
0	0	1	0	1																																	
X	1	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td>Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	1	0	1	1	0	0	1	0	X	1	1	Latch	X	X	0	0					
D	GB	RB	Q																																		
1	0	1	1																																		
0	0	1	0																																		
X	1	1	Latch																																		
X	X	0	0																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td>Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	QB	1	0	1	0	0	0	1	1	X	1	1	Latch	X	X	0	1					
D	GB	RB	QB																																		
1	0	1	0																																		
0	0	1	1																																		
X	1	1	Latch																																		
X	X	0	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F605	D → Q	(HH)		0.691	1.212	2.619	0.014	0.021	0.030	D	1.0	Q	22
			(LL)	0.613	1.073	2.291	0.012	0.016	0.023				
	D → QB	(HL)		0.521	0.892	1.879	0.013	0.018	0.028	GB	1.0	QB	22
			(LH)	0.419	0.738	1.577	0.015	0.022	0.032				
	GB → Q	(LH)		0.724	1.318	2.866	0.014	0.021	0.030	RB	1.0		
			(LL)	0.662	1.192	2.563	0.012	0.016	0.023				
	GB → QB	(LH)		0.469	0.858	1.850	0.015	0.022	0.032				
			(LL)	0.554	0.998	2.126	0.013	0.018	0.028				
	RB → Q	(HH)		0.596	1.076	2.284	0.014	0.021	0.030				
			(LL)	0.480	0.956	1.973	0.012	0.017	0.026				
	RB → QB	(HL)		0.427	0.757	1.545	0.013	0.018	0.028				
			(LH)	0.290	0.496	1.008	0.015	0.022	0.032				
	Set up time	D		0.940		1.870							
	Hold time	D		0.420		0.000							
Release time	RB		0.790		1.500								
Removal time	RB		0.420		0.000								
Min Pulse	GB		0.957		3.339								
Min Pulse	RB		0.782		2.683								
L605	D → Q	(HH)		0.561	0.948	2.018	0.029	0.042	0.062	D	1.0	Q	10
			(LL)	0.562	0.963	2.042	0.023	0.031	0.045				
	GB → Q	(LH)		0.593	1.049	2.260	0.029	0.042	0.062	GB	1.0		
			(LL)	0.601	1.069	2.293	0.023	0.031	0.045				
	RB → Q	(HH)		0.445	0.752	1.583	0.029	0.042	0.062	RB	1.0		
			(LL)	0.405	0.805	1.632	0.022	0.033	0.051				
	Set up time	D		0.850		1.400							
	Hold time	D		0.430		0.000							
	Release time	RB		0.650		0.860							
	Removal time	RB		0.560		0.370							
Min Pulse	GB		0.832		2.756								
Min Pulse	RB		0.672		2.027								
F605NQ	D → Q	(HH)		0.448	0.766	1.723	0.017	0.026	0.042	D	1.0	Q	17
			(LL)	0.383	0.700	1.499	0.014	0.020	0.031				
	GB → Q	(LH)		0.428	0.778	1.697	0.017	0.026	0.042	GB	1.0		
			(LL)	0.422	0.805	1.741	0.014	0.020	0.031				
	RB → Q	(HH)		0.445	0.776	1.783	0.017	0.026	0.042	RB	1.0		
			(LL)	0.370	0.666	1.251	0.012	0.019	0.030				
	Set up time	D		1.060		2.300							
	Hold time	D		0.390		0.000							
	Release time	RB		1.010		2.310							
	Removal time	RB		0.240		0.000							
Min Pulse	GB		0.676		2.218								
Min Pulse	RB		0.778		2.193								
F605NB	D → QB	(HL)		0.522	0.896	1.887	0.013	0.018	0.029	D	1.0	QB	22
			(LH)	0.420	0.739	1.579	0.015	0.022	0.032				
	GB → QB	(LH)		0.468	0.858	1.850	0.015	0.022	0.032	GB	1.0		
			(LL)	0.555	1.002	2.136	0.013	0.018	0.029				
	RB → QB	(HL)		0.427	0.760	1.553	0.013	0.018	0.029	RB	1.0		
			(LH)	0.290	0.497	1.010	0.015	0.022	0.032				
	Set up time	D		0.910		1.710							
	Hold time	D		0.430		0.000							
	Release time	RB		0.760		1.330							
	Removal time	RB		0.460		0.000							
Min Pulse	GB		0.787		2.607								
Min Pulse	RB		0.613		1.951								

Chapter 2 Function Block

Function	D-Latch (GB) with RB, High Speed																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F6R9	6																																			
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	QB	1	0	1	1	0	0	0	1	0	1	X	1	1	Latch		X	X	0	0	1
D	GB	RB	Q	QB																																	
1	0	1	1	0																																	
0	0	1	0	1																																	
X	1	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F6R9	D	→	Q (HH)	0.450	0.769	1.727	0.017	0.026	0.041	D	1.0	Q	17	
			(LL)	0.387	0.702	1.499	0.014	0.020	0.031					
	D	→	QB (HL)	0.632	1.119	2.547	0.012	0.016	0.023	GB	1.0	QB	22	
			(LH)	0.539	1.010	2.209	0.014	0.021	0.030					
	GB	→	Q (LH)	0.420	0.765	1.676	0.017	0.026	0.041	RB	1.0			
			(LL)	0.414	0.790	1.715	0.014	0.020	0.031					
	GB	→	QB (LH)	0.565	1.095	2.424	0.014	0.021	0.030					
			(LL)	0.602	1.115	2.496	0.012	0.016	0.023					
	RB	→	Q (HH)	0.441	0.770	1.776	0.017	0.026	0.041					
			(LL)	0.368	0.661	1.242	0.012	0.019	0.030					
	RB	→	QB (HL)	0.623	1.120	2.596	0.012	0.016	0.023					
			(LH)	0.501	0.939	1.899	0.014	0.021	0.030					
	Set up time	D		1.110		2.530								
	Hold time	D		0.380		0.000								
	Release time	RB		1.040		2.530								
	Removal time	RB		0.240		0.000								
Min Pulse	GB		0.845		2.971									
Min Pulse	RB		0.967		3.005									

[MEMO]

[MEMO]

## 2.11 D-F/F

[MEMO]



## Chapter 2 Function Block

Function	D-F/F																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power									L641	6																		
x1	F641	8	F641NQ	7	F641NB	7																						
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↘</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	Q	QB	0	↗	0	1	1	↘	1	0	X	↘	Hold	
D	C	Q	QB																									
0	↗	0	1																									
1	↘	1	0																									
X	↘	Hold																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
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D	C	Q																										
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Logic Diagram for "QB output"				Truth Table for "QB output"																								
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D	C	QB																										
0	↗	1																										
1	↘	0																										
X	↘	Hold																										

## Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F641	C → Q	(HH)		0.452	0.759	1.570	0.015	0.022	0.032	D	1.0	Q	22
		(HL)		0.530	0.926	1.955	0.012	0.016	0.024	C	1.0	QB	22
		(HL)		0.627	1.066	2.241	0.012	0.016	0.023				
	Set up time	D		0.820		1.760							
	Hold time	D		0.530		0.400							
Min Pulse	C		0.929		3.105								
L641	C → Q	(HH)		0.461	0.763	1.571	0.029	0.043	0.063	D	1.0	Q	10
		(HL)		0.536	0.920	1.928	0.023	0.031	0.046	C	1.0	QB	10
		(HL)		0.820		1.760							
	Set up time	D		0.820		1.760							
	Hold time	D		0.530		0.400							
Min Pulse	C		0.802		2.501								
F641NQ	C → Q	(HH)		0.451	0.759	1.571	0.015	0.022	0.032	D	1.0	Q	22
		(HL)		0.530	0.926	1.955	0.012	0.016	0.024	C	1.0	QB	22
		(HL)		0.820		1.770							
	Set up time	D		0.820		1.770							
	Hold time	D		0.530		0.400							
Min Pulse	C		0.796		2.528								
F641NB	C → QB	(HH)		0.427	0.741	1.566	0.015	0.023	0.035	D	1.0	QB	21
		(HL)		0.430	0.742	1.492	0.013	0.019	0.029	C	1.0	QB	21
		(HL)		0.820		1.810							
	Set up time	D		0.820		1.810							
	Hold time	D		0.510		0.440							
Min Pulse	C		0.718		2.142								

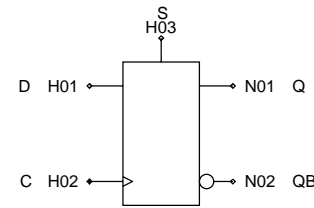
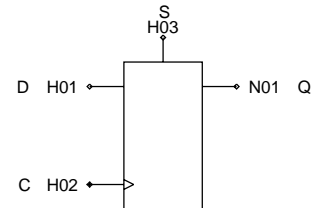
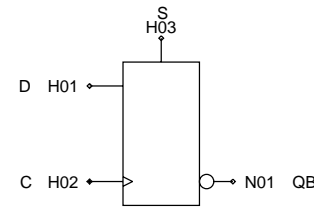
Chapter 2 Function Block

Function	D-F/F with R																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F642	9	F642NQ	8	F642NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"			Truth Table for "Normal"																																		
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D	C	R	Q	QB																																	
0	↗	0	0	1																																	
1	↗	0	1	0																																	
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Logic Diagram for "Q output"			Truth Table for "Q output"																																		
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D	C	R	Q																																		
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Logic Diagram for "QB output"			Truth Table for "QB output"																																		
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D	C	R	QB																																		
0	↗	0	1																																		
1	↗	0	0																																		
X	↘	0	Hold																																		
X	X	1	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F642	C → Q	(HH)		0.468	0.789	1.653	0.015	0.022	0.032	D	1.0	Q	22
				0.534	0.930	1.957	0.012	0.016	0.024				
				0.672	1.192	2.559	0.015	0.021	0.031				
	C → QB	(HH)		0.762	1.319	2.819	0.013	0.018	0.027	C	1.0	QB	21
				0.457	0.820	1.728	0.011	0.016	0.024				
	R → Q	(HL)		0.230	0.411	0.772	0.015	0.022	0.034	R	2.2		
	Set up time	D		0.920		2.790							
	Hold time	D		0.540		0.380							
	Release time	R		0.690		2.090							
	Removal time	R		0.600		0.380							
	Min Pulse	C		1.062		3.404							
	Min Pulse	R		0.839		2.424							
F642NQ	C → Q	(HH)		0.468	0.790	1.656	0.015	0.022	0.032	D	1.0	Q	22
				0.532	0.928	1.954	0.012	0.016	0.024				
	R → Q	(HL)		0.434	0.763	1.595	0.012	0.016	0.024	C	1.0		
	Set up time	D		0.920		2.780							
	Hold time	D		0.540		0.380							
	Release time	R		0.690		2.090							
	Removal time	R		0.600		0.390							
	Min Pulse	C		0.800		2.529							
	Min Pulse	R		0.781		2.256							
F642NB	C → QB	(HH)		0.431	0.746	1.570	0.015	0.023	0.035	D	1.0	QB	21
				0.457	0.818	1.676	0.015	0.021	0.034				
	R → QB	(HH)		0.328	0.574	1.204	0.015	0.023	0.034	C	1.0		
	Set up time	D		0.890		2.910							
	Hold time	D		0.530		0.430							
	Release time	R		0.640		2.220							
	Removal time	R		0.590		0.350							
Min Pulse	C		0.753		2.247								
Min Pulse	R		0.715		1.900								

Chapter 2 Function Block

Function	D-F/F with S																																		
Block type	Standard type					Low Gate type																													
	Normal		Q output		QB output	Normal		Q output		QB output																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																			
x1	F643	9	F643NQ	8	F643NB	8																													
x2																																			
x4																																			
Logic Diagram for "Normal"			Truth Table for "Normal"																																
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D	C	S	Q	QB																															
0	/	0	0	1																															
1	/	0	1	0																															
X	\	0	Hold																																
X	X	1	1	0																															
Logic Diagram for "Q output"			Truth Table for "Q output"																																
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0	/	0	0																																
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Logic Diagram for "QB output"			Truth Table for "QB output"																																
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D	C	S	QB																																
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F643	C → Q	(HH)		0.459	0.776	1.600	0.015	0.022	0.032	D	1.0	Q	22
			(HL)	0.638	1.136	2.412	0.013	0.018	0.028				
	C → QB	(HH)		0.801	1.446	3.139	0.014	0.021	0.030	C	1.0	QB	22
			(HL)	0.647	1.101	2.299	0.012	0.016	0.023				
	S → Q	(HH)		0.214	0.331	0.620	0.015	0.022	0.032	S	2.2		
			(HL)	0.407	0.789	1.581	0.012	0.017	0.026				
	Set up time	D		0.830		1.820							
	Hold time	D		0.520		0.400							
	Release time	S		0.220		0.000							
	Removal time	S		1.040		1.830							
	Min Pulse	C		1.070		3.713							
	Min Pulse	S		0.737		2.194							
	F643NQ	C → Q	(HH)		0.459	0.778	1.605	0.015	0.022	0.032	D	1.0	Q
(HL)				0.638	1.138	2.420	0.013	0.018	0.028				
S → Q		(HH)		0.215	0.333	0.623	0.015	0.022	0.032	C	1.0	QB	22
			(HL)	0.462	1.071	2.325	0.013	0.019	0.028				
Set up time		D		0.830		1.820							
Hold time		D		0.520		0.400							
Release time		S		0.220		0.000							
Removal time		S		1.040		1.830							
Min Pulse		C		0.907		2.994							
Min Pulse		S		0.468		1.231							
F643NB	C → QB	(HH)		0.430	0.744	1.566	0.015	0.023	0.035	D	1.0	QB	21
			(HL)	0.433	0.743	1.493	0.013	0.019	0.030				
	S → QB	(HL)		0.462	1.071	2.325	0.013	0.019	0.028	C	1.0	QB	21
			(HH)	0.462	1.071	2.325	0.013	0.019	0.028				
	Set up time	D		0.830		1.860							
	Hold time	D		0.510		0.440							
	Release time	S		0.200		0.000							
Removal time	S		1.000		1.770								
Min Pulse	C		0.724		2.143								
Min Pulse	S		0.903		2.930								

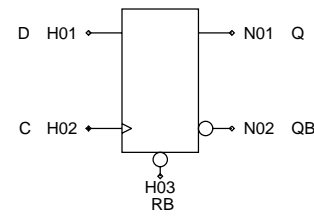
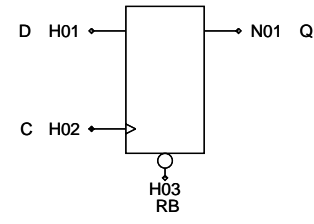
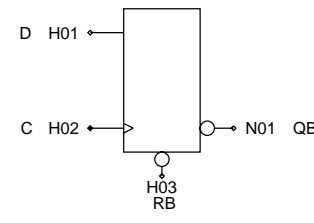
Chapter 2 Function Block

Function	D-F/F with R, S																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power									L644	8																																												
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D	C	R	S	QB																																																		
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X	\	0	0	Hold																																																		
X	X	0	1	0																																																		
X	X	1	0	1																																																		
X	X	1	1	1																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F644	C → Q	(HH)		0.482	0.820	1.705	0.015	0.022	0.032	D	1.0	Q	22	
		(HL)		0.633	1.126	2.394	0.012	0.018	0.028	C	1.0	QB	21	
	C → QB	(HH)		0.782	1.426	3.110	0.014	0.021	0.030	R	2.1			
		(HL)		0.774	1.348	2.869	0.013	0.018	0.027	S	2.3			
	R → Q	(HL)		0.535	1.001	2.150	0.012	0.017	0.027					
	R → QB	(HH)		0.229	0.414	0.775	0.015	0.022	0.034					
	S → Q	(HH)		0.210	0.327	0.612	0.015	0.022	0.032					
	S → QB	(HL)		0.500	1.109	2.300	0.013	0.020	0.031					
	Set up time	D		0.900		2.780								
	Hold time	D		0.540		0.390								
	Release time	R		0.670		2.080								
	Release time	S		0.210		0.000								
	Removal time	R		0.620		0.420								
	Removal time	S		1.050		1.870								
	Min Pulse	C		1.073		3.684								
Min Pulse	R		0.944		2.854									
Min Pulse	S		0.904		2.889									
L644	C → Q	(HH)		0.490	0.821	1.698	0.029	0.043	0.063	D	1.0	Q	10	
		(HL)		0.636	1.107	2.326	0.024	0.034	0.053	C	1.0			
	R → Q	(HL)		0.521	0.903	1.899	0.024	0.033	0.051	R	2.1			
	S → Q	(HH)		0.221	0.338	0.628	0.029	0.043	0.063	S	2.2			
	Set up time	D		0.890		2.750								
	Hold time	D		0.540		0.390								
	Release time	R		0.660		2.060								
	Release time	S		0.210		0.000								
	Removal time	R		0.620		0.420								
	Removal time	S		1.050		1.870								
	Min Pulse	C		0.906		2.903								
	Min Pulse	R		0.867		2.553								
	Min Pulse	S		0.451		1.189								
	F644NQ	C → Q	(HH)		0.481	0.818	1.704	0.015	0.022	0.032	D	1.0	Q	22
			(HL)		0.633	1.129	2.401	0.013	0.018	0.028	C	1.0		
R → Q		(HL)		0.520	0.929	1.985	0.012	0.017	0.027	R	2.1			
S → Q		(HH)		0.209	0.326	0.610	0.015	0.022	0.032	S	2.2			
Set up time		D		0.900		2.770								
Hold time		D		0.540		0.390								
Release time		R		0.660		2.070								
Release time		S		0.210		0.000								
Removal time		R		0.620		0.420								
Removal time		S		1.050		1.870								
Min Pulse		C		0.904		2.978								
Min Pulse		R		0.867		2.637								
Min Pulse		S		0.455		1.212								
F644NB		C → QB	(HH)		0.434	0.750	1.572	0.015	0.023	0.035	D	1.0	QB	20
			(HL)		0.467	0.837	1.706	0.015	0.021	0.034	C	1.0		
	R → QB	(HH)		0.330	0.570	1.188	0.015	0.023	0.035	R	2.1			
	S → QB	(HL)		0.626	1.387	3.098	0.015	0.021	0.033	S	2.2			
	Set up time	D		0.880		2.890								
	Hold time	D		0.530		0.440								
	Release time	R		0.620		2.190								
	Release time	S		0.190		0.000								
	Removal time	R		0.610		0.390								
	Removal time	S		1.010		1.800								
	Min Pulse	C		0.765		2.279								
	Min Pulse	R		0.711		1.880								
	Min Pulse	S		1.057		3.680								

Chapter 2 Function Block

Function	D-F/F with RB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power									L645	7																											
x1	F615	9	F615NQ	8	F615NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	C	RB	Q	QB																																	
0	/	1	0	1																																	
1	/	1	1	0																																	
X	\	1	Hold																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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D	C	RB	Q																																		
0	/	1	0																																		
1	/	1	1																																		
X	\	1	Hold																																		
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Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	C	RB	QB																																		
0	/	1	1																																		
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X	\	1	Hold																																		
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F615	C → Q	(HH)		0.543	0.935	2.024	0.016	0.023	0.034	D	1.0	Q	18
				0.564	0.977	2.059	0.012	0.016	0.024				
				0.733	1.269	2.762	0.012	0.016	0.023				
	C → QB	(HH)		0.709	1.239	2.655	0.015	0.022	0.031	C	1.0	QB	19
				0.273	0.447	0.879	0.012	0.016	0.024				
	RB → Q	(LL)		0.273	0.447	0.879	0.012	0.016	0.024	RB	2.2		
				0.424	0.810	1.678	0.015	0.023	0.033				
	Set up time	D		0.840		1.830							
	Hold time	D		0.530		0.410							
	Release time	RB		0.310		0.090							
	Removal time	RB		0.940		1.510							
	Min Pulse	C		1.023		3.345							
	Min Pulse	RB		0.757		2.216							
L645	C → Q	(HH)		0.519	0.883	1.891	0.029	0.044	0.066	D	1.0	Q	10
				0.542	0.931	1.953	0.023	0.031	0.046				
	RB → Q	(LL)		0.254	0.405	0.783	0.023	0.031	0.047	C	1.0	QB	10
				0.254	0.405	0.783	0.023	0.031	0.047				
	Set up time	D		0.830		1.830							
	Hold time	D		0.530		0.400							
	Release time	RB		0.310		0.060							
	Removal time	RB		0.940		1.510							
	Min Pulse	C		0.813		2.530							
	Min Pulse	RB		0.503		1.273							
F615NQ	C → Q	(HH)		0.546	0.941	2.037	0.016	0.023	0.035	D	1.0	Q	18
				0.566	0.981	2.067	0.012	0.016	0.024				
	RB → Q	(LL)		0.275	0.451	0.888	0.012	0.016	0.024	C	1.0	QB	18
				0.275	0.451	0.888	0.012	0.016	0.024				
	Set up time	D		0.840		1.830							
	Hold time	D		0.530		0.410							
	Release time	RB		0.310		0.100							
Removal time	RB		0.940		1.510								
Min Pulse	C		0.837		2.644								
Min Pulse	RB		0.542		1.415								
F615NB	C → QB	(HH)		0.464	0.796	1.678	0.016	0.023	0.035	D	1.0	QB	18
				0.462	0.781	1.571	0.013	0.019	0.029				
	RB → QB	(LH)		0.454	1.090	2.382	0.016	0.023	0.034	C	1.0	QB	18
				0.454	1.090	2.382	0.016	0.023	0.034				
	Set up time	D		0.830		1.890							
	Hold time	D		0.520		0.440							
	Release time	RB		0.290		0.170							
	Removal time	RB		0.910		1.450							
Min Pulse	C		0.754		2.257								
Min Pulse	RB		0.908		2.913								

Chapter 2 Function Block

Function	D-F/F with SB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F616	9	F616NQ	8	F616NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>/</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>/</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>\</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	SB	Q	QB	0	/	1	0	1	1	/	1	1	0	X	\	1	Hold		X	X	0	1	0
D	C	SB	Q	QB																																	
0	/	1	0	1																																	
1	/	1	1	0																																	
X	\	1	Hold																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>SB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>/</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>/</td> <td>1</td> <td>1</td> </tr> <tr> <td>X</td> <td>\</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	SB	Q	0	/	1	0	1	/	1	1	X	\	1	Hold	X	X	0	1					
D	C	SB	Q																																		
0	/	1	0																																		
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X	\	1	Hold																																		
X	X	0	1																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	C	SB	QB																																		
0	/	1	1																																		
1	/	1	0																																		
X	\	1	Hold																																		
X	X	0	0																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F616	C → Q	(HH)		0.454	0.762	1.573	0.015	0.022	0.032	D	1.0	Q	22
				0.556	0.979	2.096	0.012	0.016	0.024				
				0.639	1.085	2.276	0.012	0.016	0.023				
	C → QB	(HH)		0.767	1.386	3.089	0.015	0.022	0.032	C	1.0	QB	21
				0.477	0.937	2.018	0.015	0.022	0.032				
	SB → Q	(LH)		0.477	0.937	2.018	0.015	0.022	0.032	SB	2.2		
				0.271	0.549	1.064	0.012	0.017	0.027				
	Set up time	D		0.870		2.000							
	Hold time	D		0.520		0.400							
	Release time	SB		0.620		0.980							
	Removal time	SB		0.600		0.570							
	Min Pulse	C		1.035		3.663							
	Min Pulse	SB		0.836		2.600							
F616NQ	C → Q	(HH)		0.454	0.764	1.579	0.015	0.022	0.032	D	1.0	Q	22
				0.555	0.978	2.094	0.012	0.016	0.024				
	SB → Q	(LH)		0.449	0.845	1.809	0.015	0.022	0.032	C	1.0	QB	21
				0.449	0.845	1.809	0.015	0.022	0.032				
	Set up time	D		0.870		2.010							
	Hold time	D		0.510		0.400							
	Release time	SB		0.620		0.990							
Removal time	SB		0.600		0.570								
Min Pulse	C		0.822		2.668								
Min Pulse	SB		0.782		2.377								
F616NB	C → QB	(HH)		0.465	0.817	1.756	0.016	0.024	0.038	D	1.0	QB	19
				0.434	0.750	1.505	0.013	0.019	0.030				
	SB → QB	(LL)		0.394	0.767	1.644	0.013	0.018	0.028	C	1.0	QB	19
				0.394	0.767	1.644	0.013	0.018	0.028				
	Set up time	D		0.890		2.040							
	Hold time	D		0.490		0.440							
	Release time	SB		0.630		1.020							
Removal time	SB		0.580		0.490								
Min Pulse	C		0.733		2.332								
Min Pulse	SB		0.743		2.232								

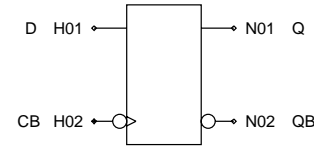
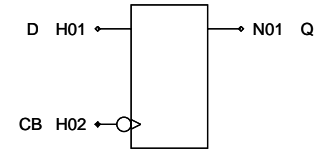
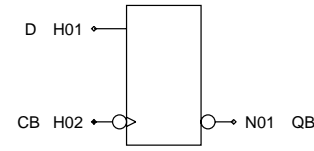
Chapter 2 Function Block

Function	D-F/F with RB, SB																																																					
Block type	Standard type					Low Gate type																																																
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power								L647	8																																													
x1	F647	10	F647NQ	9	F647NB	9																																																
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Logic Diagram for "Normal"			Truth Table for "Normal"																																																			
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D	C	RB	SB	Q	QB																																																	
0	/	1	1	0	1																																																	
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D	C	RB	SB	Q																																																		
0	/	1	1	0																																																		
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X	X	1	0	1																																																		
X	X	0	0	0																																																		
Logic Diagram for "QB output"			Truth Table for "QB output"																																																			
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D	C	RB	SB	QB																																																		
0	/	1	1	1																																																		
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X	X	0	0	0																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F647	C → Q	(HH)		0.520	0.900	1.941	0.015	0.022	0.034	D	1.0	Q	21	
		(HL)		0.563	0.992	2.125	0.012	0.016	0.024	C	1.0	QB	20	
	C → QB	(HH)		0.769	1.390	3.104	0.015	0.022	0.032	RB	2.2			
		(HL)		0.707	1.237	2.707	0.012	0.016	0.023	SB	2.1			
	RB → Q	(LL)		0.239	0.397	0.783	0.012	0.016	0.024					
	RB → QB	(LH)		0.448	0.949	2.093	0.015	0.023	0.036					
	SB → Q	(LH)		0.535	1.071	2.377	0.015	0.022	0.033					
	SB → QB	(LL)		0.266	0.546	1.058	0.012	0.017	0.027					
	Set up time	D		0.860		1.960								
	Hold time	D		0.520		0.410								
	Release time	RB		0.300		0.100								
	Release time	SB		0.590		0.930								
	Removal time	RB		0.950		1.590								
	Removal time	SB		0.630		0.630								
	Min Pulse	C		1.038		3.679								
Min Pulse	RB		0.812		2.625									
Min Pulse	SB		0.916		2.959									
L647	C → Q	(HH)		0.530	0.901	1.919	0.029	0.044	0.066	D	1.0	Q	10	
		(HL)		0.570	0.986	2.092	0.023	0.031	0.047	C	1.0			
	RB → Q	(LL)		0.255	0.404	0.778	0.023	0.031	0.047	RB	2.2			
	SB → Q	(LH)		0.516	0.962	2.103	0.029	0.043	0.064	SB	2.1			
	Set up time	D		0.870		1.990								
	Hold time	D		0.520		0.400								
	Release time	RB		0.300		0.070								
	Release time	SB		0.600		0.950								
	Removal time	RB		0.960		1.600								
	Removal time	SB		0.620		0.620								
	Min Pulse	C		0.840		2.668								
	Min Pulse	RB		0.501		1.266								
	Min Pulse	SB		0.861		2.669								
	F647NQ	C → Q	(HH)		0.517	0.898	1.942	0.015	0.022	0.034	D	1.0	Q	21
			(HL)		0.559	0.987	2.116	0.012	0.016	0.024	C	1.0		
RB → Q		(LL)		0.241	0.400	0.789	0.012	0.016	0.024	RB	2.2			
SB → Q		(LH)		0.504	0.963	2.136	0.015	0.022	0.033	SB	2.1			
Set up time		D		0.860		1.990								
Hold time		D		0.520		0.410								
F647NB	C → QB	(HH)		0.472	0.827	1.772	0.016	0.024	0.038	D	1.0	QB	19	
		(HL)		0.437	0.752	1.500	0.013	0.019	0.030	C	1.0			
	RB → QB	(LH)		0.503	1.271	2.914	0.015	0.024	0.037	RB	2.2			
	SB → QB	(LL)		0.388	0.753	1.601	0.013	0.019	0.030	SB	2.1			
	Set up time	D		0.880		2.020								
	Hold time	D		0.500		0.440								
	Release time	RB		0.280		0.160								
	Release time	SB		0.610		0.990								
	Removal time	RB		0.920		1.500								
	Removal time	SB		0.610		0.550								
	Min Pulse	C		0.742		2.350								
	Min Pulse	RB		0.994		3.436								
	Min Pulse	SB		0.735		2.188								

## Chapter 2 Function Block

Function	D-F/F (CB)																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power									L661	6																		
x1	F661	8	F661NQ	7	F661NB	7																						
x2																												
x4																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	Q	QB	0	\	0	1	1	\	1	0	X	/	Hold	
D	CB	Q	QB																									
0	\	0	1																									
1	\	1	0																									
X	/	Hold																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>0</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> </tr> <tr> <td>X</td> <td>/</td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	Q	0	\	0	1	\	1	X	/	Hold				
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D	CB	QB																										
0	\	1																										
1	\	0																										
X	/	Hold																										

## Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F661	CB → Q	(LH)		0.513	0.938	2.023	0.015	0.022	0.032	D	1.0	Q	22
		(LL)		0.475	0.843	1.782	0.012	0.016	0.024			QB	22
		(LL)		0.691	1.251	2.705	0.012	0.016	0.023				
		Set up time	D		0.850				1.600				
		Hold time	D		0.570				0.700				
		Min Pulse	CB		0.954				3.220				
L661	CB → Q	(LH)		0.520	0.939	2.019	0.029	0.043	0.063	D	1.0	Q	10
		(LL)		0.481	0.838	1.758	0.023	0.031	0.046			CB	1.0
		Set up time	D		0.850				1.590				
		Hold time	D		0.570				0.700				
	Min Pulse	CB		0.784				2.535					
F661NQ	CB → Q	(LH)		0.512	0.936	2.021	0.015	0.022	0.032	D	1.0	Q	22
		(LL)		0.475	0.845	1.787	0.012	0.016	0.024			CB	1.0
		Set up time	D		0.850				1.600				
		Hold time	D		0.570				0.700				
	Min Pulse	CB		0.774				2.536					
F661NB	CB → QB	(LH)		0.388	0.698	1.488	0.015	0.023	0.035	D	1.0	QB	21
		(LL)		0.446	0.845	1.822	0.013	0.019	0.029			CB	1.0
		Set up time	D		0.850				1.580				
		Hold time	D		0.570				0.720				
	Min Pulse	CB		0.720				2.344					



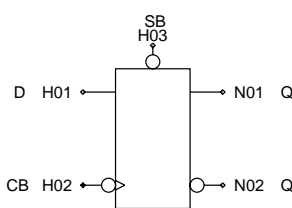
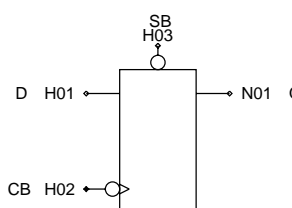
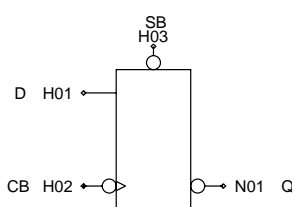
Chapter 2 Function Block

Function	D-F/F (CB) with RB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F665	9	F665NQ	8	F665NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	CB	RB	Q	QB																																	
0	\	1	0	1																																	
1	\	1	1	0																																	
X	/	1	Hold																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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D	CB	RB	Q																																		
0	\	1	0																																		
1	\	1	1																																		
X	/	1	Hold																																		
X	X	0	0																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																	
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D	CB	RB	QB																																		
0	\	1	1																																		
1	\	1	0																																		
X	/	1	Hold																																		
X	X	0	1																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F665	CB → Q	(LH)		0.610	1.121	2.487	0.016	0.023	0.034	D	1.0	Q	18
			(LL)	0.508	0.895	1.888				0.012	0.016	0.024	CB
	CB → QB	(LH)		0.654	1.157	2.483	0.015	0.022	0.031	RB	2.2		
			(LL)	0.799	1.455	3.224				0.012	0.015	0.023	
	RB → Q	(LL)		0.272	0.446	0.877	0.012	0.016	0.024				
			(LH)	0.422	0.808	1.674				0.015	0.023	0.033	
	Set up time	D		0.860									
	Hold time	D		0.570									
	Release time	RB		0.290									
	Removal time	RB		0.960									
	Min Pulse	CB		1.065									
	Min Pulse	RB		0.755									
	F665NQ	CB → Q	(LH)		0.611	1.124	2.494	0.016	0.023	0.035	D	1.0	Q
(LL)				0.510	0.898	1.896	0.012				0.016	0.024	CB
RB → Q		(LL)		0.273	0.448	0.884	0.012	0.016	0.024	RB	2.2		
Set up time		D		0.860									
Hold time		D		0.570									
Release time		RB		0.290									
Removal time		RB		0.960									
Min Pulse		CB		0.878									
Min Pulse		RB		0.539									
F665NB	CB → QB	(LH)		0.425	0.752	1.600	0.016	0.023	0.035	D	1.0	QB	18
			(LL)	0.484	0.898	1.917				0.013	0.019	0.029	CB
	RB → QB	(LH)		0.452	1.096	2.393	0.016	0.023	0.034	RB	2.2		
	Set up time	D		0.860									
	Hold time	D		0.570									
	Release time	RB		0.280									
Removal time	RB		0.920										
Min Pulse	CB		0.762										
Min Pulse	RB		0.914										

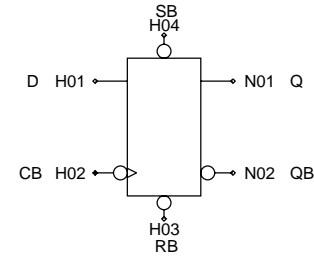
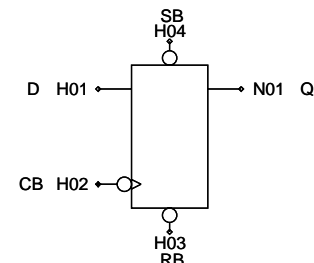
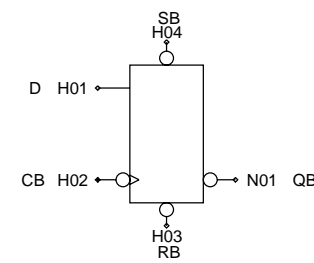
Chapter 2 Function Block

Function	D-F/F (CB) with SB																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F666	9	F666NQ	8	F666NB	8																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	CB	SB	Q	QB																																	
0	\	1	0	1																																	
1	\	1	1	0																																	
X	/	1	Hold																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
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D	CB	SB	QB																																		
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1	\	1	0																																		
X	/	1	Hold																																		
X	X	0	0																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F666	CB → Q	(LH)		0.510	0.932	2.010	0.015	0.022	0.032	D	1.0	Q	22
				0.493	0.882	1.886	0.012	0.016	0.024				
	CB → QB	(LH)		0.704	1.286	2.874	0.015	0.022	0.032	CB	1.0	QB	21
				0.691	1.251	2.709	0.012	0.016	0.023				
	SB → Q	(LH)		0.474	0.992	2.113	0.015	0.022	0.032				
				0.297	0.595	1.136	0.012	0.017	0.027				
	Set up time		D	0.900		2.240							
	Hold time		D	0.580		0.700							
	Release time		SB	0.610		1.260							
	Removal time		SB	0.620		0.720							
	Min Pulse		CB	0.967		3.396							
	Min Pulse		SB	0.914		2.694							
F666NQ	CB → Q	(LH)		0.509	0.931	2.008	0.015	0.022	0.032	D	1.0	Q	22
				0.493	0.883	1.890	0.012	0.016	0.024				
	SB → Q	(LH)		0.447	0.836	1.794	0.015	0.022	0.032	CB	2.2		
				0.900		2.240							
	Set up time		D	0.900		2.240							
	Hold time		D	0.580		0.700							
	Release time		SB	0.610		1.270							
	Removal time		SB	0.620		0.720							
Min Pulse		CB	0.771		2.524								
Min Pulse		SB	0.775		2.360								
F666NB	CB → QB	(LH)		0.421	0.765	1.660	0.016	0.024	0.038	D	1.0	QB	19
				0.446	0.843	1.816	0.013	0.019	0.029				
	SB → QB	(LL)		0.392	0.758	1.630	0.013	0.018	0.028	CB	2.2		
				0.900		2.200							
	Set up time		D	0.900		2.200							
	Hold time		D	0.580		0.720							
	Release time		SB	0.610		1.240							
	Removal time		SB	0.610		0.700							
Min Pulse		CB	0.718		2.338								
Min Pulse		SB	0.737		2.217								

Chapter 2 Function Block

Function	D-F/F (CB) with RB, SB																																																			
Block type	Standard type					Low Gate type																																														
	Normal		Q output		QB output		Normal		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power							L667	8																																												
x1	F667	10	F667NQ	9	F667NB	9																																														
x2																																																				
x4																																																				
Logic Diagram for "Normal"		Truth Table for "Normal"																																																		
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D	CB	RB	SB	Q	QB																																															
0	↘	1	1	0	1																																															
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Logic Diagram for "Q output"		Truth Table for "Q output"																																																		
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X	X	0	1	1																																																
X	X	1	0	0																																																
X	X	0	0	0																																																

Chapter 2 Function Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F667	CB → Q	(LH)		0.574	1.067	2.372	0.015	0.022	0.034	D	1.0	Q	21
		(LL)		0.502	0.899	1.923	0.012	0.016	0.024	CB	1.0	QB	20
	CB → QB	(LH)		0.709	1.298	2.903	0.015	0.022	0.032	RB	2.2		
		(LL)		0.760	1.404	3.139	0.012	0.016	0.023	SB	2.1		
	RB → Q	(LL)		0.241	0.400	0.788	0.012	0.016	0.024				
		(LH)		0.451	0.953	2.100	0.015	0.023	0.036				
	SB → Q	(LH)		0.539	1.069	2.374	0.015	0.022	0.033				
		(LL)		0.266	0.546	1.058	0.012	0.017	0.027				
	Set up time	D		0.900		2.240							
	Hold time	D		0.580		0.700							
	Release time	RB		0.280		0.000							
	Release time	SB		0.600		1.260							
	Removal time	RB		0.980		1.960							
	Removal time	SB		0.640		0.750							
Min Pulse	CB		1.023		3.656								
Min Pulse	RB		0.820		2.633								
Min Pulse	SB		0.915		2.956								
L667	CB → Q	(LH)		0.585	1.066	2.346	0.029	0.044	0.066	D	1.0	Q	10
		(LL)		0.512	0.898	1.900	0.023	0.031	0.047	CB	1.0		
	RB → Q	(LL)		0.253	0.402	0.776	0.023	0.031	0.047	RB	2.2		
		(LH)		0.515	0.960	2.099	0.029	0.043	0.064	SB	2.1		
	SB → Q	(LH)		0.900		2.250							
		D		0.580		0.700							
	Release time	RB		0.280		0.000							
	Release time	SB		0.600		1.260							
	Removal time	RB		0.980		1.970							
	Removal time	SB		0.640		0.750							
	Min Pulse	CB		0.848		2.862							
	Min Pulse	RB		0.499		1.264							
	Min Pulse	SB		0.859		2.666							
	F667NQ	CB → Q	(LH)		0.573	1.066	2.373	0.015	0.022	0.034	D	1.0	Q
(LL)				0.502	0.900	1.926	0.012	0.016	0.024	CB	1.0		
RB → Q		(LL)		0.241	0.400	0.789	0.012	0.016	0.024	RB	2.2		
		(LH)		0.504	0.963	2.135	0.015	0.022	0.033	SB	2.1		
Set up time		D		0.900		2.250							
Hold time		D		0.580		0.700							
Release time	RB		0.280		0.000								
Release time	SB		0.600		1.260								
Removal time	RB		0.980		1.970								
Removal time	SB		0.640		0.750								
Min Pulse	CB		0.836		2.889								
Min Pulse	RB		0.494		1.304								
Min Pulse	SB		0.851		2.700								
F667NB	CB → QB	(LH)		0.428	0.776	1.679	0.016	0.024	0.038	D	1.0	QB	19
		(LL)		0.448	0.844	1.811	0.013	0.019	0.030	CB	1.0		
	RB → QB	(LH)		0.503	1.270	2.912	0.015	0.024	0.037	RB	2.2		
		(LL)		0.387	0.751	1.599	0.013	0.019	0.030	SB	2.1		
	Set up time	D		0.900		2.210							
	Hold time	D		0.580		0.720							
Release time	RB		0.270		0.000								
Release time	SB		0.600		1.230								
Removal time	RB		0.930		1.880								
Removal time	SB		0.630		0.730								
Min Pulse	CB		0.722		2.335								
Min Pulse	RB		0.993		3.434								
Min Pulse	SB		0.735		2.186								

Chapter 2 Function Block

Function	D-F/F with 2 to 1 Selector																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F641S	10	F641SQ	9	F641SB	9																																																
x2																																																						
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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D0	D1	C	A	Q	QB																																																	
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Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
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D0	D1	C	A	QB																																																		
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X	X	\	0	Hold																																																		
X	X	\	1	Hold																																																		

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F641S	C → Q	(HH)		0.456	0.764	1.577	0.015	0.022	0.032	D0	1.0	Q	22	
		(HL)		0.541	0.940	1.977	0.012	0.016	0.024	D1	1.0	QB	22	
	C → QB	(HH)		0.677	1.194	2.562	0.015	0.021	0.031	C	1.0			
		(HL)		0.635	1.077	2.257	0.012	0.016	0.023	A	1.0			
	Set up time		D0	0.980		2.400								
	Set up time		D1	0.980		2.400								
	Set up time		A	1.000		2.720								
	Hold time		D0	0.380		0.000								
	Hold time		D1	0.380		0.000								
	Hold time		A	0.360		0.000								
	Min Pulse		C	0.952		3.141								
F641SQ	C → Q	(HH)		0.457	0.766	1.582	0.015	0.022	0.032	D0	1.0	Q	22	
		(HL)		0.541	0.941	1.979	0.012	0.016	0.024	D1	1.0	QB	22	
	Set up time		D0	0.980		2.390				C	1.0			
	Set up time		D1	0.980		2.390				A	1.0			
	Set up time		A	1.000		2.720								
	Hold time		D0	0.380		0.000								
	Hold time		D1	0.380		0.000								
	Hold time		A	0.360		0.000								
	Min Pulse		C	0.816		2.558								
	F641SB	C → QB	(HH)		0.438	0.757	1.590	0.015	0.023	0.035	D0	1.0	QB	21
			(HL)		0.438	0.749	1.502	0.013	0.019	0.029	D1	1.0		
Set up time			D0	0.990		2.450				C	1.0			
Set up time			D1	0.990		2.440				A	1.0			
Set up time			A	1.010		2.770								
Hold time			D0	0.360		0.000								
Hold time			D1	0.360		0.000								
Hold time			A	0.340		0.000								
Min Pulse			C	0.735		2.172								

## Chapter 2 Function Block

Function	D-F/F with R, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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D0	D1	C	R	A	Q	QB																																																														
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## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F642S	C → Q	(HH)		0.471	0.794	1.660	0.015	0.022	0.032	D0	1.0	Q	22
				0.539	0.938	1.968	0.012	0.016	0.024	D1	1.0	QB	21
				0.674	1.195	2.565	0.015	0.021	0.030	C	1.0		
	C → QB	(HL)		0.756	1.311	2.808	0.013	0.018	0.027	R	2.2		
		(HL)		0.462	0.823	1.732	0.012	0.016	0.024	A	1.0		
	R → Q	(HH)		0.226	0.406	0.765	0.015	0.022	0.034				
		(HH)											
	Set up time	D0		1.080		3.420							
	Set up time	D1		1.080		3.420							
	Set up time	A		1.110		3.740							
	Hold time	D0		0.390		0.000							
	Hold time	D1		0.390		0.000							
	Hold time	A		0.370		0.000							
	Release time	R		0.700		2.110							
	Removal time	R		0.600		0.370							
	Min Pulse	C		1.060		3.390							
Min Pulse	R		0.837		2.424								
F642SQ	C → Q	(HH)		0.467	0.790	1.655	0.015	0.022	0.032	D0	1.0	Q	22
				0.532	0.929	1.956	0.012	0.016	0.024	D1	1.0		
				0.436	0.766	1.600	0.012	0.016	0.024	C	1.0		
	R → Q	(HL)		1.090		3.440				R	2.2		
		(HL)		1.080		3.430				A	1.0		
	Set up time	D0		1.110		3.750							
	Set up time	D1		0.380		0.000							
	Set up time	A		0.380		0.000							
	Hold time	D0		0.370		0.000							
	Hold time	D1		0.370		0.000							
	Hold time	A		0.370		0.000							
	Release time	R		0.700		2.110							
	Removal time	R		0.590		0.370							
	Min Pulse	C		0.798		2.527							
	Min Pulse	R		0.784		2.261							
	F642SB	C → QB	(HH)		0.427	0.741	1.562	0.015	0.023	0.035	D0	1.0	QB
				0.453	0.813	1.670	0.015	0.021	0.034	D1	1.0		
				0.327	0.574	1.203	0.015	0.023	0.034	C	1.0		
R → QB		(HH)		1.060		3.570				R	2.2		
		(HH)		1.050		3.560				A	1.0		
Set up time		D0		1.080		3.880							
Set up time		D1		0.360		0.000							
Set up time		A		0.370		0.000							
Hold time		D0		0.350		0.000							
Hold time		D1		0.640		2.240							
Hold time		A		0.580		0.330							
Release time		R		0.753		2.239							
Removal time		R		0.714		1.900							
Min Pulse		C											
Min Pulse		R											

Chapter 2 Function Block

Function	D-F/F with S, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
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Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F643S	C → Q	(HH)		0.463	0.782	1.608	0.015	0.022	0.032	D0	1.0	Q	22	
		(HL)		0.648	1.150	2.433	0.013	0.018	0.028	D1	1.0	QB	22	
	C → QB	(HH)		0.811	1.460	3.160	0.014	0.021	0.030	C	1.0			
		(HL)		0.651	1.107	2.307	0.012	0.016	0.023	S	2.2			
	S → Q	(HH)		0.214	0.332	0.621	0.015	0.022	0.032	A	1.0			
	S → QB	(HL)		0.408	0.790	1.583	0.012	0.017	0.026					
	Set up time	D0		1.010		2.460								
	Set up time	D1		1.010		2.460								
	Set up time	A		1.020		2.780								
	Hold time	D0		0.370		0.000								
	Hold time	D1		0.380		0.000								
	Hold time	A		0.360		0.000								
	Release time	S		0.210		0.000								
	Removal time	S		1.040		1.830								
	Min Pulse	C		1.086		3.739								
	Min Pulse	S		0.739		2.197								
F643SQ	C → Q	(HH)		0.463	0.783	1.612	0.015	0.022	0.032	D0	1.0	Q	22	
		(HL)		0.647	1.151	2.439	0.013	0.018	0.028	D1	1.0			
	S → Q	(HH)		0.214	0.333	0.623	0.015	0.022	0.032	C	1.0			
	Set up time	D0		1.010		2.460				S	2.2			
	Set up time	D1		1.000		2.460				A	1.0			
	Set up time	A		1.020		2.780								
	Hold time	D0		0.370		0.000								
	Hold time	D1		0.380		0.000								
	Hold time	A		0.360		0.000								
	Release time	S		0.210		0.000								
	Removal time	S		1.040		1.830								
	Min Pulse	C		0.923		3.019								
	Min Pulse	S		0.467		1.230								
	F643SB	C → QB	(HH)		0.440	0.758	1.588	0.015	0.023	0.035	D0	1.0	QB	21
			(HL)		0.440	0.748	1.500	0.013	0.019	0.030	D1	1.0		
		S → QB	(HL)		0.462	1.071	2.325	0.013	0.019	0.028	C	1.0		
Set up time		D0		1.020		2.500				S	2.2			
Set up time		D1		1.010		2.500				A	1.0			
Set up time		A		1.030		2.830								
Hold time		D0		0.350		0.000								
Hold time		D1		0.350		0.000								
Hold time		A		0.330		0.000								
Release time		S		0.200		0.000								
Removal time		S		1.000		1.780								
Min Pulse		C		0.737		2.170								
Min Pulse		S		0.903		2.930								

### Chapter 2 Function Block

Function	D-F/F with R, S, 2 to 1 Selector																																																																																											
Block type	Standard type					Low Gate type																																																																																						
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### Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F644S	C → Q	(HH)		0.476	0.811	1.691	0.015	0.022	0.032	D0	1.0	Q	22
		(HL)		0.627	1.118	2.382	0.012	0.018	0.028	D1	1.0	QB	21
	C → QB	(HH)		0.778	1.420	3.100	0.014	0.021	0.030	C	1.0		
		(HL)		0.769	1.339	2.855	0.013	0.018	0.027	R	2.1		
	R → Q	(HL)		0.529	0.996	2.143	0.012	0.017	0.027	S	2.3		
	R → QB	(HH)		0.231	0.414	0.776	0.015	0.022	0.034	A	1.0		
	S → Q	(HH)		0.209	0.326	0.610	0.015	0.022	0.032				
	S → QB	(HL)		0.500	1.102	2.288	0.013	0.020	0.031				
	Set up time	D0		1.060		3.410							
	Set up time	D1		1.060		3.420							
	Set up time	A		1.090		3.730							
	Hold time	D0		0.380		0.000							
	Hold time	D1		0.370		0.000							
	Hold time	A		0.360		0.000							
	Release time	R		0.660		2.080							
	Release time	S		0.220		0.000							
	Removal time	R		0.620		0.420							
	Removal time	S		1.050		1.850							
Min Pulse	C		1.069		3.675								
Min Pulse	R		0.943		2.846								
Min Pulse	S		0.898		2.877								
F644SQ	C → Q	(HH)		0.476	0.811	1.693	0.015	0.022	0.032	D0	1.0	Q	22
		(HL)		0.629	1.122	2.390	0.013	0.018	0.028	D1	1.0		
	R → Q	(HL)		0.518	0.924	1.977	0.012	0.017	0.027	C	1.0		
	S → Q	(HH)		0.209	0.325	0.610	0.015	0.022	0.032	R	2.1		
	Set up time	D0		1.060		3.410				S	2.3		
	Set up time	D1		1.060		3.420				A	1.0		
	Set up time	A		1.090		3.730							
	Hold time	D0		0.380		0.000							
	Hold time	D1		0.370		0.000							
	Hold time	A		0.360		0.000							
	Release time	R		0.660		2.080							
	Release time	S		0.220		0.000							
Removal time	R		0.620		0.420								
Removal time	S		1.050		1.850								
Min Pulse	C		0.897		2.965								
Min Pulse	R		0.859		2.626								
Min Pulse	S		0.454		1.211								
F644SB	C → QB	(HH)		0.429	0.742	1.561	0.015	0.023	0.034	D0	1.0	QB	20
		(HL)		0.460	0.825	1.689	0.015	0.021	0.034	D1	1.0		
	R → QB	(HH)		0.327	0.564	1.179	0.015	0.023	0.035	C	1.0		
	S → QB	(HL)		0.620	1.378	3.084	0.015	0.021	0.033	R	2.1		
	Set up time	D0		1.040		3.540				S	2.2		
	Set up time	D1		1.050		3.550				A	1.0		
	Set up time	A		1.070		3.860							
	Hold time	D0		0.360		0.000							
	Hold time	D1		0.360		0.000							
	Hold time	A		0.350		0.000							
	Release time	R		0.620		2.200							
	Release time	S		0.200		0.000							
Removal time	R		0.610		0.380								
Removal time	S		1.000		1.780								
Min Pulse	C		0.757		2.260								
Min Pulse	R		0.703		1.870								
Min Pulse	S		1.052		3.668								

Chapter 2 Function Block

Function	D-F/F with RB, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
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Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F615S	C → Q	(HH)		0.542	0.933	2.019	0.016	0.023	0.034	D0	1.0	Q	18	
		(HL)		0.562	0.974	2.054	0.012	0.016	0.024	D1	1.0	QB	19	
	C → QB	(HH)		0.706	1.235	2.649	0.015	0.022	0.031	C	1.0			
		(HL)		0.730	1.265	2.755	0.012	0.015	0.023	RB	2.2			
	RB → Q	(LL)		0.273	0.447	0.879	0.012	0.016	0.024	A	1.0			
	RB → QB	(LH)		0.423	0.810	1.677	0.015	0.023	0.033					
	Set up time	D0		1.000		2.490								
	Set up time	D1		1.000		2.490								
	Set up time	A		1.030		2.810								
	Hold time	D0		0.370		0.000								
	Hold time	D1		0.370		0.000								
	Hold time	A		0.350		0.000								
	Release time	RB		0.310		0.090								
	Removal time	RB		0.930		1.510								
	Min Pulse	C		1.018		3.335								
	Min Pulse	RB		0.756		2.216								
F615SQ	C → Q	(HH)		0.542	0.935	2.027	0.016	0.023	0.035	D0	1.0	Q	18	
		(HL)		0.561	0.975	2.058	0.012	0.016	0.024	D1	1.0			
	RB → Q	(LL)		0.274	0.449	0.885	0.012	0.016	0.024	C	1.0			
	Set up time	D0		1.000		2.490				RB	2.2			
	Set up time	D1		1.000		2.490				A	1.0			
	Set up time	A		1.030		2.810								
	Hold time	D0		0.370		0.000								
	Hold time	D1		0.360		0.000								
	Hold time	A		0.350		0.000								
	Release time	RB		0.310		0.100								
	Removal time	RB		0.930		1.510								
	Min Pulse	C		0.830		2.632								
	Min Pulse	RB		0.539		1.410								
	F615SB	C → QB	(HH)		0.461	0.792	1.673	0.016	0.023	0.035	D0	1.0	QB	18
			(HL)		0.459	0.778	1.567	0.013	0.019	0.029	D1	1.0		
		RB → QB	(LH)		0.453	1.087	2.377	0.016	0.023	0.034	C	1.0		
Set up time		D0		1.010		2.550				RB	2.2			
Set up time		D1		1.010		2.550				A	1.0			
Set up time		A		1.020		2.870								
Hold time		D0		0.340		0.000								
Hold time		D1		0.340		0.000								
Hold time		A		0.330		0.000								
Release time		RB		0.300		0.160								
Removal time		RB		0.900		1.450								
Min Pulse		C		0.749		2.249								
Min Pulse		RB		0.905		2.908								



Chapter 2 Function Block

Function	D-F/F with SB, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F616S	C → Q	(HH)		0.460	0.770	1.585	0.015	0.022	0.032	D0	1.0	Q	22
		(HL)		0.567	0.993	2.119	0.012	0.016	0.024	D1	1.0	QB	21
	C → QB	(HH)		0.777	1.398	3.108	0.015	0.022	0.032	C	1.0		
		(HL)		0.643	1.090	2.283	0.012	0.016	0.023	SB	2.2		
	SB → Q	(LH)		0.475	0.937	2.018	0.015	0.022	0.032	A	1.0		
	SB → QB	(LL)		0.269	0.547	1.061	0.012	0.017	0.027				
	Set up time	D0		1.080		2.870							
	Set up time	D1		1.080		2.860							
	Set up time	A		1.090		3.120							
	Hold time	D0		0.360		0.000							
	Hold time	D1		0.360		0.000							
	Hold time	A		0.350		0.000							
	Release time	SB		0.610		0.970							
	Removal time	SB		0.610		0.570							
	Min Pulse	C		1.051		3.687							
	Min Pulse	SB		0.836		2.599							
	F616SQ	C → Q	(HH)		0.461	0.772	1.591	0.015	0.022	0.032	D0	1.0	Q
		(HL)		0.565	0.992	2.115	0.012	0.016	0.024	D1	1.0		
SB → Q		(LH)		0.452	0.838	1.799	0.015	0.022	0.032	C	1.0		
Set up time		D0		1.070		2.860				SB	2.2		
Set up time		D1		1.070		2.860				A	1.0		
Set up time		A		1.090		3.120							
Hold time		D0		0.360		0.000							
Hold time		D1		0.370		0.000							
Hold time		A		0.350		0.000							
Release time		SB		0.610		0.970							
Removal time		SB		0.610		0.580							
Min Pulse	C		0.840		2.696								
Min Pulse	SB		0.774		2.363								
F616SB	C → QB	(HH)		0.476	0.833	1.780	0.015	0.024	0.037	D0	1.0	QB	19
		(HL)		0.445	0.764	1.524	0.013	0.019	0.030	D1	1.0		
	SB → QB	(LL)		0.396	0.757	1.628	0.013	0.018	0.029	C	1.0		
	Set up time	D0		1.090		2.890				SB	2.2		
	Set up time	D1		1.080		2.880				A	1.0		
	Set up time	A		1.100		3.140							
	Hold time	D0		0.320		0.000							
	Hold time	D1		0.330		0.000							
	Hold time	A		0.310		0.000							
	Release time	SB		0.620		0.990							
	Removal time	SB		0.590		0.500							
Min Pulse	C		0.752		2.363								
Min Pulse	SB		0.737		2.215								

Chapter 2 Function Block

Function	D-F/F with RB, SB, 2 to 1 Selector																																																																																											
Block type	Standard type						Low Gate type																																																																																					
	Normal		Q output		QB output		Normal		Q output		QB output																																																																																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																
Low Power																																																																																												
x1	F647S	12	F647SQ	11	F647SB	11																																																																																						
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F647S	C → Q	(HH)		0.522	0.902	1.944	0.015	0.022	0.034	D0	1.0	Q	21
		(HL)		0.572	1.004	2.143	0.012	0.016	0.024	D1	1.0	QB	20
	C → QB	(HH)		0.779	1.403	3.125	0.015	0.022	0.032	C	1.0		
		(HL)		0.710	1.241	2.712	0.012	0.016	0.023	RB	2.2		
	RB → Q	(LL)		0.241	0.400	0.788	0.012	0.016	0.024	SB	2.1		
	RB → QB	(LH)		0.452	0.954	2.103	0.015	0.023	0.036	A	1.0		
	SB → Q	(LH)		0.539	1.070	2.375	0.015	0.022	0.033				
	SB → QB	(LL)		0.267	0.547	1.060	0.012	0.017	0.027				
	Set up time	D0		1.070		2.870							
	Set up time	D1		1.070		2.870							
	Set up time	A		1.090		3.130							
	Hold time	D0		0.370		0.000							
	Hold time	D1		0.370		0.000							
	Hold time	A		0.350		0.000							
	Release time	RB		0.290		0.080							
	Release time	SB		0.600		0.960							
	Removal time	RB		0.970		1.620							
Removal time	SB		0.630		0.610								
Min Pulse	C		1.056		3.707								
Min Pulse	RB		0.821		2.636								
Min Pulse	SB		0.916		2.958								
F647SQ	C → Q	(HH)		0.522	0.905	1.952	0.015	0.022	0.034	D0	1.0	Q	21
		(HL)		0.571	1.003	2.140	0.012	0.016	0.024	D1	1.0		
	RB → Q	(LL)		0.241	0.400	0.789	0.012	0.016	0.024	C	1.0		
	SB → Q	(LH)		0.504	0.963	2.136	0.015	0.022	0.033	RB	2.2		
	Set up time	D0		1.070		2.870				SB	2.1		
	Set up time	D1		1.070		2.860				A	1.0		
	Set up time	A		1.090		3.130							
	Hold time	D0		0.370		0.000							
	Hold time	D1		0.370		0.000							
	Hold time	A		0.350		0.000							
	Release time	RB		0.290		0.090							
	Release time	SB		0.590		0.950							
	Removal time	RB		0.970		1.620							
	Removal time	SB		0.630		0.620							
	Min Pulse	C		0.848		2.723							
	Min Pulse	RB		0.494		1.304							
	Min Pulse	SB		0.850		2.700							
F647SB	C → QB	(HH)		0.484	0.843	1.796	0.016	0.024	0.038	D0	1.0	QB	19
		(HL)		0.446	0.758	1.510	0.013	0.019	0.030	D1	1.0		
	RB → QB	(LH)		0.503	1.271	2.914	0.015	0.024	0.037	C	1.0		
	SB → QB	(LL)		0.388	0.752	1.601	0.013	0.019	0.030	RB	2.2		
	Set up time	D0		1.090		2.900				SB	2.1		
	Set up time	D1		1.080		2.900				A	1.0		
	Set up time	A		1.100		3.160							
	Hold time	D0		0.330		0.000							
	Hold time	D1		0.330		0.000							
	Hold time	A		0.310		0.000							
	Release time	RB		0.270		0.140							
	Release time	SB		0.610		0.990							
	Removal time	RB		0.930		1.520							
	Removal time	SB		0.610		0.540							
	Min Pulse	C		0.762		2.381							
	Min Pulse	RB		0.994		3.436							
	Min Pulse	SB		0.735		2.188							

Chapter 2 Function Block

Function	D-F/F (CB) with 2 to 1 Selector																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F661S	10	F661SQ	9	F661SB	9																																																
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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D0	D1	CB	A	Q	QB																																																	
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Logic Diagram for "QB output"				Truth Table for "QB output"																																																		
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D0	D1	CB	A	QB																																																		
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				X:Irrelevant																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F661S	CB → Q	(LH)		0.525	0.955	2.049	0.015	0.022	0.032	D0	1.0	Q	22
		(LL)		0.482	0.853	1.797	0.012	0.016	0.024	D1	1.0	QB	22
		(LH)		0.619	1.106	2.381	0.015	0.021	0.031	CB	1.0		
	CB → QB	(LH)		0.703	1.269	2.731	0.012	0.016	0.023	A	1.0		
		(LL)											
		(LH)											
		Set up time	D0		1.020								
		Set up time	D1		1.020								
		Set up time	A		1.040								
		Hold time	D0		0.450								
		Hold time	D1		0.450								
	Hold time	A		0.440									
	Min Pulse	CB		0.972									
F661SQ	CB → Q	(LH)		0.524	0.955	2.049	0.015	0.022	0.032	D0	1.0	Q	22
		(LL)		0.482	0.855	1.802	0.012	0.016	0.024	D1	1.0	QB	22
		(LH)								CB	1.0		
	CB → QB	(LH)		0.703	1.269	2.731	0.012	0.016	0.023	A	1.0		
		(LL)											
		(LH)											
		Set up time	D0		1.020								
		Set up time	D1		1.020								
		Set up time	A		1.040								
		Hold time	D0		0.450								
		Hold time	D1		0.450								
	Hold time	A		0.440									
	Min Pulse	CB		0.794									
F661SB	CB → QB	(LH)		0.396	0.709	1.504	0.015	0.023	0.035	D0	1.0	QB	21
		(LL)		0.459	0.863	1.849	0.013	0.019	0.029	D1	1.0		
		(LH)								CB	1.0		
	CB → Q	(LH)		0.619	1.106	2.381	0.015	0.021	0.031	A	1.0		
		(LL)											
		(LH)											
		Set up time	D0		1.020								
		Set up time	D1		1.020								
		Set up time	A		1.040								
		Hold time	D0		0.450								
		Hold time	D1		0.450								
	Hold time	A		0.440									
	Min Pulse	CB		0.739									

Chapter 2 Function Block

Function	D-F/F (CB) with RB, 2 to 1 Selector																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F665S	11	F665SQ	10	F665SB	10																																																														
x2																																																																				
x4																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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D0	D1	CB	RB	A	Q	QB																																																														
0	X	\	1	0	0	1																																																														
1	X	\	1	0	1	0																																																														
X	X	/	1	0	Hold																																																															
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Logic Diagram for "Q output"				Truth Table for "Q output"																																																																
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D0	D1	CB	RB	A	Q																																																															
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X	X	X	0	X	1																																																															
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Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F665S	CB → Q	(LH)		0.606	1.116	2.479	0.016	0.023	0.034	D0	1.0	Q	18	
			(LL)	0.506	0.891	1.882	0.012	0.016	0.024	D1	1.0	QB	19	
		(LH)	0.652	1.154	2.478	0.015	0.022	0.031	CB	1.0				
	RB → Q	(LL)		0.796	1.451	3.219	0.012	0.016	0.023	RB	2.2			
			(LL)	0.272	0.446	0.877	0.012	0.016	0.024	A	1.0			
	RB → QB	(LH)		0.423	0.809	1.675	0.015	0.023	0.033					
			(LH)	0.423	0.809	1.675	0.015	0.023	0.033					
	Set up time	D0		1.040		2.530								
	Set up time	D1		1.040		2.520								
	Set up time	A		1.060		2.770								
	Hold time	D0		0.420		0.180								
	Hold time	D1		0.430		0.190								
	Hold time	A		0.430		0.000								
	Release time	RB		0.300		0.000								
	Removal time	RB		0.950		1.880								
	Min Pulse	CB		1.060		3.735								
	Min Pulse	RB		0.755		2.213								
F665SQ	CB → Q	(LH)		0.607	1.117	2.484	0.016	0.023	0.034	D0	1.0	Q	18	
			(LL)	0.507	0.894	1.889	0.012	0.016	0.024	D1	1.0			
		(LL)	0.273	0.447	0.883	0.011	0.016	0.024	CB	1.0				
	RB → Q	(LL)		1.040		2.530				RB	2.2			
			(LL)	0.273	0.447	0.883	0.011	0.016	0.024	A	1.0			
	Set up time	D0		1.040		2.520								
	Set up time	D1		1.040		2.520								
	Set up time	A		1.060		2.770								
	Hold time	D0		0.420		0.180								
	Hold time	D1		0.430		0.190								
	Hold time	A		0.430		0.000								
	Release time	RB		0.300		0.000								
	Removal time	RB		0.950		1.880								
	Min Pulse	CB		0.871		3.000								
	Min Pulse	RB		0.537		1.407								
	F665SB	CB → QB	(LH)		0.427	0.754	1.603	0.016	0.023	0.035	D0	1.0	QB	18
				(LL)	0.484	0.898	1.918	0.013	0.019	0.029	D1	1.0		
(LH)			0.455	1.100	2.397	0.016	0.023	0.034	CB	1.0				
RB → QB		(LH)		1.040		2.530				RB	2.2			
			(LH)	0.455	1.100	2.397	0.016	0.023	0.034	A	1.0			
Set up time		D0		1.040		2.520								
Set up time		D1		1.040		2.520								
Set up time		A		1.060		2.770								
Hold time		D0		0.430		0.210								
Hold time		D1		0.430		0.220								
Hold time		A		0.430		0.000								
Release time		RB		0.300		0.000								
Removal time		RB		0.910		1.810								
Min Pulse		CB		0.760		2.442								
Min Pulse		RB		0.915		2.928								

Chapter 2 Function Block

Function	D-F/F (CB) with SB, 2 to 1 Selector																																																																			
Block type	Standard type					Low Gate type																																																														
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F666S	11	F666SQ	10	F666SB	10																																																														
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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D0	D1	CB	SB	A	Q	QB																																																														
0	X	\	1	0	0	1																																																														
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D0	D1	CB	SB	A	Q																																																															
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D0	D1	CB	SB	A	QB																																																															
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X	X	X	0	X	0																																																															
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Chapter 2 Function Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F666S	CB → Q	(LH)		0.522	0.949	2.036	0.015	0.022	0.032	D0	1.0	Q	22
		(LL)		0.502	0.895	1.907	0.012	0.016	0.024	D1	1.0	QB	21
	CB → QB	(LH)		0.713	1.299	2.895	0.015	0.022	0.032	CB	1.0		
		(LL)		0.703	1.269	2.735	0.012	0.016	0.023	SB	2.2		
	SB → Q	(LH)		0.470	0.934	2.013	0.015	0.022	0.032	A	1.0		
		(LL)		0.269	0.545	1.058	0.012	0.017	0.027				
	Set up time	D0		1.080		3.060							
	Set up time	D1		1.080		3.060							
	Set up time	A		1.100		3.320							
	Hold time	D0		0.460		0.220							
	Hold time	D1		0.460		0.220							
	Hold time	A		0.450		0.000							
	Release time	SB		0.600		1.230							
	Removal time	SB		0.630		0.750							
	Min Pulse	CB		0.981		3.421							
	Min Pulse	SB		0.833		2.593							
F666SQ	CB → Q	(LH)		0.521	0.949	2.035	0.015	0.022	0.032	D0	1.0	Q	22
		(LL)		0.502	0.897	1.911	0.012	0.016	0.024	D1	1.0		
	SB → Q	(LH)		0.450	0.829	1.785	0.015	0.022	0.032	CB	1.0		
		(LL)		0.450	0.829	1.785	0.015	0.022	0.032	SB	2.2		
	Set up time	D0		1.080		3.070				A	1.0		
	Set up time	D1		1.080		3.060							
	Set up time	A		1.100		3.320							
	Hold time	D0		0.460		0.220							
	Hold time	D1		0.460		0.220							
	Hold time	A		0.450		0.000							
	Release time	SB		0.600		1.240							
	Removal time	SB		0.630		0.750							
Min Pulse	CB		0.789		2.556								
Min Pulse	SB		0.766		2.348								
F666SB	CB → QB	(LH)		0.433	0.783	1.688	0.016	0.024	0.038	D0	1.0	QB	19
		(LL)		0.458	0.862	1.844	0.013	0.019	0.030	D1	1.0		
	SB → QB	(LH)		0.394	0.749	1.615	0.013	0.018	0.029	CB	1.0		
		(LL)		0.394	0.749	1.615	0.013	0.018	0.029	SB	2.2		
	Set up time	D0		1.090		3.040				A	1.0		
	Set up time	D1		1.090		3.030							
	Set up time	A		1.110		3.290							
	Hold time	D0		0.460		0.240							
	Hold time	D1		0.460		0.250							
	Hold time	A		0.450		0.000							
	Release time	SB		0.600		1.210							
	Removal time	SB		0.620		0.730							
Min Pulse	CB		0.736		2.372								
Min Pulse	SB		0.730		2.201								

Chapter 2 Function Block

Function	D-F/F (CB) with RB, SB, 2 to 1 Selector																																																																																											
Block type	Standard type					Low Gate type																																																																																						
	Normal		Q output		QB output		Normal		Q output		QB output																																																																																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																
Low Power																																																																																												
x1	F667S	12	F667SQ	11	F667SB	11																																																																																						
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Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F667S	CB → Q	(LH)		0.586	1.084	2.398	0.015	0.022	0.034	D0	1.0	Q	21
		(LL)		0.509	0.909	1.939	0.012	0.016	0.024	D1	1.0	QB	20
	CB → QB	(LH)		0.716	1.308	2.918	0.015	0.022	0.032	CB	1.0		
		(LL)		0.772	1.421	3.165	0.012	0.016	0.023	RB	2.2		
	RB → Q	(LL)		0.241	0.400	0.788	0.012	0.016	0.024	SB	2.1		
		(LH)		0.451	0.953	2.100	0.015	0.023	0.036	A	1.0		
	SB → Q	(LH)		0.539	1.069	2.373	0.015	0.022	0.033				
		(LL)		0.266	0.546	1.058	0.012	0.017	0.027				
	Set up time	D0		1.090		3.120							
	Set up time	D1		1.090		3.110							
	Set up time	A		1.110		3.380							
	Hold time	D0		0.450		0.210							
	Hold time	D1		0.450		0.210							
	Hold time	A		0.440		0.000							
	Release time	RB		0.280		0.000							
	Release time	SB		0.590		1.260							
	Removal time	RB		0.980		1.970							
Removal time	SB		0.640		0.770								
Min Pulse	CB		1.040		3.686								
Min Pulse	RB		0.820		2.633								
Min Pulse	SB		0.915		2.956								
F667SQ	CB → Q	(LH)		0.585	1.083	2.398	0.015	0.022	0.034	D0	1.0	Q	21
		(LL)		0.509	0.911	1.942	0.012	0.016	0.024	D1	1.0		
	RB → Q	(LL)		0.241	0.400	0.789	0.012	0.016	0.024	CB	1.0		
		(LH)		0.504	0.963	2.135	0.015	0.022	0.033	RB	2.2		
	SB → Q	(LH)		0.504	0.963	2.135	0.015	0.022	0.033	SB	2.1		
		(LL)		0.241	0.400	0.789	0.012	0.016	0.024	A	1.0		
	Set up time	D0		1.090		3.120							
	Set up time	D1		1.090		3.120							
	Set up time	A		1.110		3.380							
	Hold time	D0		0.450		0.210							
	Hold time	D1		0.450		0.210							
	Hold time	A		0.440		0.000							
	Release time	RB		0.280		0.000							
	Release time	SB		0.590		1.260							
	Removal time	RB		0.980		1.970							
	Removal time	SB		0.640		0.770							
	Min Pulse	CB		0.853		2.920							
Min Pulse	RB		0.494		1.304								
Min Pulse	SB		0.850		2.700								
F667SB	CB → QB	(LH)		0.437	0.789	1.697	0.016	0.024	0.038	D0	1.0	QB	19
		(LL)		0.460	0.862	1.837	0.013	0.019	0.030	D1	1.0		
	RB → QB	(LH)		0.503	1.269	2.912	0.015	0.024	0.037	CB	1.0		
		(LL)		0.387	0.751	1.598	0.013	0.019	0.030	RB	2.2		
	SB → QB	(LH)		0.387	0.751	1.598	0.013	0.019	0.030	SB	2.1		
		(LL)		0.460	0.862	1.837	0.013	0.019	0.030	A	1.0		
	Set up time	D0		1.090		3.090							
	Set up time	D1		1.090		3.090							
	Set up time	A		1.110		3.350							
	Hold time	D0		0.450		0.240							
	Hold time	D1		0.460		0.250							
	Hold time	A		0.450		0.000							
	Release time	RB		0.270		0.000							
	Release time	SB		0.590		1.230							
	Removal time	RB		0.930		1.890							
	Removal time	SB		0.640		0.750							
	Min Pulse	CB		0.740		2.365							
Min Pulse	RB		0.993		3.434								
Min Pulse	SB		0.735		2.186								

## Chapter 2 Function Block

Function	D-F/F with Hold																																				
Block type	Standard type						Low Gate type																														
	Normal		Q output		QB output		Normal		Q output		QB output																										
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Low Power																																					
x1	F641H	10	F641HQ	9	F641HB	9																															
x2																																					
x4																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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## Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F641H	C → Q	(HH)	0.455	0.763	1.574	0.015	0.022	0.032	D	1.0	Q	22	
		(HL)	0.540	0.939	1.974	0.012	0.016	0.024					
	C → QB	(HH)	0.706	1.245	2.663	0.015	0.021	0.031	C	1.0	QB	22	
		(HL)	0.674	1.147	2.391	0.012	0.016	0.025					
	Set up time	D		0.980			2.410						
	Set up time	H		1.000			2.680						
	Hold time	D		0.380			0.000						
	Hold time	H		0.360			0.000						
Min Pulse	C		0.979			3.240							
F641HQ	C → Q	(HH)	0.455	0.763	1.576	0.015	0.022	0.032	D	1.0	Q	22	
		(HL)	0.539	0.938	1.973	0.012	0.016	0.024					
	Set up time	D		0.980			2.410			C	1.0		
	Set up time	H		1.000			2.680						
	Hold time	D		0.380			0.000			H	1.0		
	Hold time	H		0.360			0.000						
Min Pulse	C		0.812			2.550							
F641HB	C → QB	(HH)	0.437	0.755	1.587	0.015	0.023	0.035	D	1.0	QB	21	
		(HL)	0.437	0.746	1.498	0.013	0.019	0.029					
	Set up time	D		0.990			2.450			C	1.0		
	Set up time	H		1.010			2.720						
	Hold time	D		0.350			0.000			H	1.0		
	Hold time	H		0.340			0.000						
Min Pulse	C		0.731			2.167							

Chapter 2 Function Block

Function	D-F/F with RB, Hold																																															
Block type	Standard type						Low Gate type																																									
	Normal		Q output		QB output		Normal		Q output		QB output																																					
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																				
Low Power																																																
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Logic Diagram for "Normal"				Truth Table for "Normal"																																												
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X	/	1	1	Hold																																												
X	\	1	X	Hold																																												
X	X	0	X	1																																												

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F615H	C → Q	(HH)		0.550	0.943	2.034	0.016	0.023	0.034	D	1.0	Q	18
				0.578	0.996	2.088	0.012	0.016	0.024	C	1.0	QB	18
				0.782	1.355	2.928	0.012	0.016	0.024	RB	2.2		
	C → QB	(HH)		0.753	1.313	2.793	0.015	0.022	0.032	H	1.0		
				0.273	0.446	0.878	0.012	0.016	0.024				
	RB → Q	(LL)		0.273	0.446	0.878	0.012	0.016	0.024				
				0.456	0.863	1.781	0.015	0.023	0.033				
	Set up time	D		0.980		2.470							
	Set up time	H		1.000		2.740							
	Hold time	D		0.390		0.000							
	Hold time	H		0.370		0.000							
	Release time	RB		0.300		0.070							
	Removal time	RB		0.950		1.540							
	Min Pulse	C		1.082		3.520							
Min Pulse	RB		0.789		2.322								
F615HQ	C → Q	(HH)		0.551	0.945	2.039	0.016	0.023	0.034	D	1.0	Q	18
				0.578	0.996	2.089	0.012	0.016	0.024	C	1.0	QB	18
				0.273	0.448	0.881	0.012	0.016	0.024	RB	2.2		
	RB → Q	(LL)		0.273	0.448	0.881	0.012	0.016	0.024	H	1.0		
				0.456	0.863	1.781	0.015	0.023	0.033				
	Set up time	D		0.980		2.470							
	Set up time	H		1.000		2.740							
	Hold time	D		0.390		0.000							
	Hold time	H		0.370		0.000							
	Release time	RB		0.300		0.070							
	Removal time	RB		0.950		1.540							
	Min Pulse	C		0.859		2.674							
	Min Pulse	RB		0.538		1.405							
	F615HB	C → QB	(HH)		0.480	0.818	1.711	0.016	0.023	0.035	D	1.0	QB
				0.472	0.789	1.582	0.013	0.019	0.029	C	1.0		
				0.480	1.093	2.386	0.016	0.023	0.035	RB	2.2		
RB → QB		(LH)		0.480	1.093	2.386	0.016	0.023	0.035	H	1.0		
				0.990		2.520							
Set up time		H		1.010		2.790							
Hold time		D		0.370		0.000							
Hold time		H		0.350		0.000							
Release time		RB		0.280		0.140							
Removal time		RB		0.920		1.470							
Min Pulse		C		0.774		2.298							
Min Pulse		RB		0.910		2.916							



Chapter 2 Function Block

Function	D-F/F with SB, Hold																																															
Block type	Standard type					Low Gate type																																										
	Normal		Q output		QB output		Normal		Q output		QB output																																					
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																				
Low Power																																																
x1	F616H	11	F616HQ	10	F616HB	10																																										
x2																																																
x4																																																
Logic Diagram for "Normal"				Truth Table for "Normal"																																												
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>SB</th> <th>H</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>/</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>\</td> <td>1</td> <td>0</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>X</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	SB	H	Q	QB	0	/	1	0	0	1	1	/	1	0	1	0	X	\	1	0	Hold		X	X	1	1	Hold		X	X	0	X	1	0
D	C	SB	H	Q	QB																																											
0	/	1	0	0	1																																											
1	/	1	0	1	0																																											
X	\	1	0	Hold																																												
X	X	1	1	Hold																																												
X	X	0	X	1	0																																											
Logic Diagram for "Q output"				Truth Table for "Q output"																																												
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D	C	SB	H	Q																																												
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1	/	1	0	1																																												
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Logic Diagram for "QB output"				Truth Table for "QB output"																																												
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D	C	SB	H	QB																																												
0	/	1	0	1																																												
1	/	1	0	0																																												
X	\	1	0	Hold																																												
X	X	1	1	Hold																																												
X	X	0	X	0																																												

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F616H	C → Q	(HH)		0.460	0.768	1.582	0.015	0.022	0.032	D	1.0	Q	22	
			(HL)	0.566	0.992	2.117	0.012	0.016	0.024					
	C → QB	(HH)		0.822	1.482	3.286	0.015	0.022	0.034	C	1.0	QB	20	
			(HL)	0.686	1.166	2.426	0.012	0.017	0.025					
	SB → Q	(LH)		0.476	1.026	2.207	0.015	0.022	0.032	SB	2.2			
			(LL)	0.311	0.622	1.202	0.012	0.018	0.028					
	Set up time	D		1.080		2.870								
	Set up time	H		1.090		3.120								
	Hold time	D		0.360		0.000								
	Hold time	H		0.350		0.000								
	Release time	SB		0.610		0.980								
	Removal time	SB		0.610		0.570								
	Min Pulse	C		1.097		3.866								
	Min Pulse	SB		0.900		2.796								
F616HQ	C → Q	(HH)		0.461	0.771	1.588	0.015	0.022	0.032	D	1.0	Q	22	
			(HL)	0.566	0.992	2.115	0.012	0.016	0.024					
	SB → Q	(LH)		0.478	0.875	1.858	0.015	0.022	0.032	C	1.0	QB	20	
			(LL)	0.311	0.622	1.202	0.012	0.018	0.028					
	Set up time	D		1.070		2.860				SB	2.2			
	Set up time	H		1.090		3.120								
	Hold time	D		0.360		0.000				H	1.0			
	Hold time	H		0.350		0.000								
	Release time	SB		0.610		0.970								
	Removal time	SB		0.610		0.570								
	Min Pulse	C		0.842		2.696								
	Min Pulse	SB		0.802		2.433								
	F616HB	C → QB	(HH)		0.479	0.836	1.786	0.016	0.024	0.038	D	1.0	QB	19
				(HL)	0.446	0.764	1.524	0.013	0.019	0.030				
SB → QB		(LH)		0.420	0.793	1.692	0.013	0.018	0.029	C	1.0			
			(LL)	0.311	0.622	1.202	0.012	0.018	0.028					
Set up time		D		1.090		2.890				SB	2.2			
Set up time		H		1.100		3.140								
Hold time		D		0.320		0.000				H	1.0			
Hold time		H		0.310		0.000								
Release time		SB		0.620		0.990								
Removal time		SB		0.590		0.500								
Min Pulse		C		0.755		2.370								
Min Pulse		SB		0.761		2.284								

Chapter 2 Function Block

Function	D-F/F with RB, SB, Hold																																																																			
Block type	Standard type						Low Gate type																																																													
	Normal		Q output		QB output		Normal		Q output		QB output																																																									
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
Low Power																																																																				
x1	F647H	12	F647HQ	11	F647HB	11																																																														
x2																																																																				
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Logic Diagram for "Normal"			Truth Table for "Normal"																																																																	
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D	C	RB	SB	H	Q	QB																																																														
0	/	1	1	0	0	1																																																														
1	/	1	1	0	1	0																																																														
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X	X	1	0	X	1	0																																																														
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Logic Diagram for "Q output"			Truth Table for "Q output"																																																																	
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D	C	RB	SB	H	Q																																																															
0	/	1	1	0	0																																																															
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X	\	1	1	0	Hold																																																															
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Logic Diagram for "QB output"			Truth Table for "QB output"																																																																	
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D	C	RB	SB	H	QB																																																															
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X	X	0	0	X	0																																																															

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F647H	C → Q	(HH)		0.523	0.903	1.944	0.015	0.022	0.034	D	1.0	Q	21	
		(HL)		0.573	1.005	2.146	0.012	0.016	0.024	C	1.0	QB	19	
	C → QB	(HH)		0.828	1.493	3.312	0.015	0.022	0.034	RB	2.3			
		(HL)		0.758	1.326	2.874	0.012	0.016	0.024	SB	2.1			
	RB → Q	(LL)		0.241	0.400	0.789	0.012	0.016	0.024	H	1.0			
	RB → QB	(LH)		0.502	1.045	2.291	0.015	0.024	0.037					
	SB → Q	(LH)		0.541	1.173	2.584	0.015	0.022	0.033					
	SB → QB	(LL)		0.311	0.625	1.205	0.012	0.018	0.029					
	Set up time	D		1.080		2.870								
	Set up time	H		1.090		3.130								
	Hold time	D		0.360		0.000								
	Hold time	H		0.350		0.000								
	Release time	RB		0.290		0.080								
	Release time	SB		0.600		0.960								
	Removal time	RB		0.970		1.620								
	Removal time	SB		0.630		0.610								
	Min Pulse	C		1.105		3.894								
Min Pulse	RB		0.871		2.824									
Min Pulse	SB		0.989		3.176									
F647HQ	C → Q	(HH)		0.522	0.902	1.945	0.015	0.022	0.034	D	1.0	Q	21	
		(HL)		0.570	1.001	2.139	0.012	0.016	0.024	C	1.0			
	RB → Q	(LH)		0.241	0.399	0.787	0.012	0.016	0.024	RB	2.2			
	SB → Q	(LH)		0.541	1.002	2.211	0.015	0.022	0.033	SB	2.1			
	Set up time	D		1.070		2.870				H	1.0			
	Set up time	H		1.090		3.130								
	Hold time	D		0.360		0.000								
	Hold time	H		0.350		0.000								
	Release time	RB		0.290		0.080								
	Release time	SB		0.600		0.960								
	Removal time	RB		0.970		1.620								
	Removal time	SB		0.630		0.610								
	Min Pulse	C		0.848		2.721								
	Min Pulse	RB		0.493		1.302								
	Min Pulse	SB		0.878		2.785								
	F647HB	C → QB	(HH)		0.483	0.843	1.797	0.016	0.024	0.038	D	1.0	QB	19
			(HL)		0.445	0.756	1.506	0.013	0.019	0.030	C	1.0		
RB → QB		(LH)		0.552	1.272	2.917	0.016	0.024	0.037	RB	2.2			
SB → QB		(LL)		0.421	0.781	1.659	0.013	0.019	0.030	SB	2.1			
Set up time		D		1.090		2.910				H	1.0			
Set up time		H		1.100		3.170								
Hold time		D		0.330		0.000								
Hold time		H		0.310		0.000								
Release time		RB		0.270		0.140								
Release time		SB		0.610		0.990								
Removal time		RB		0.930		1.520								
Removal time		SB		0.610		0.540								
Min Pulse		C		0.761		2.381								
Min Pulse		RB		0.995		3.437								
Min Pulse		SB		0.755		2.250								

Chapter 2 Function Block

Function	D-F/F (CB) with 2 to 1 Selector(2 CTRL), RB																																																																																	
Block type	Standard type					Low Gate type																																																																												
	Normal		Q output		QB output	Normal		Q output		QB output																																																																								
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																								
Low Power																																																																																		
x1	F673	11																																																																																
x2																																																																																		
x4																																																																																		
Logic Diagram for "Normal"			Truth Table for "Normal"																																																																															
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D0	D1	S0	S1	CB	RB	Q	QB																																																																											
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Logic Diagram for "Q output"			Truth Table for "Q output"																																																																															
Logic Diagram for "QB output"			Truth Table for "QB output"																																																																															

Chapter 2 Function Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F673	CB	→	Q (LH)	0.614	1.143	2.541	0.015	0.023	0.036	D0	1.0	Q	20	
			(LL)	0.509	0.911	1.922	0.012	0.017	0.026	D1	1.0	QB	22	
	CB	→	QB (LH)	0.612	1.111	2.396	0.015	0.021	0.030	CB	1.0			
			(LL)	0.758	1.409	3.152	0.011	0.015	0.022	RB	2.1			
	RB	→	Q (LL)	0.277	0.467	0.919	0.012	0.017	0.026	S0	1.0			
	RB	→	QB (LH)	0.382	0.668	1.394	0.015	0.021	0.030	S1	1.0			
	Set up time		D0	1.000		2.150								
	Set up time		D1	1.040		2.360								
	Set up time		S0	1.040		2.250								
	Set up time		S1	1.030		2.440								
	Hold time		D0	0.470		0.280								
	Hold time		D1	0.380		0.000								
	Hold time		S0	0.530		0.330								
	Hold time		S1	0.450		0.030								
	Release time		RB	0.290		0.000								
	Removal time		RB	0.960		1.890								
	Min Pulse		CB	1.025		3.671								
Min Pulse		RB	0.674		1.965									

Chapter 2 Function Block

Function	D-F/F (CB) with Hold, 2 to 1 Selector(2 CTRL), RB																																																																																																																							
Block type	Standard type						Low Gate type																																																																																																																	
	Normal		Q output		QB output		Normal		Q output		QB output																																																																																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																																												
Low Power																																																																																																																								
x1	F674	12																																																																																																																						
x2																																																																																																																								
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																																																																																				
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D0	D1	S0	S1	CB	RB	H	Q	QB																																																																																																																
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Logic Diagram for "Q output"				Truth Table for "Q output"																																																																																																																				
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																																																																				

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F674	CB	→	Q (LH)	0.619	1.150	2.551	0.015	0.023	0.035	D0	1.0	Q	20
			(LL)	0.512	0.914	1.927	0.012	0.017	0.026	D1	1.0	QB	22
	CB	→	QB (LH)	0.661	1.192	2.548	0.015	0.021	0.030	CB	1.0		
			(LL)	0.822	1.519	3.359	0.012	0.016	0.023	RB	2.0		
	RB	→	Q (LL)	0.271	0.458	0.904	0.012	0.017	0.026	S0	1.0		
	RB	→	QB (LH)	0.423	0.738	1.528	0.015	0.021	0.031	S1	1.0		
	Set up time		D0	1.260		3.240				H	1.0		
	Set up time		D1	1.290		3.560							
	Set up time		S0	1.320		3.400							
	Set up time		S1	1.360		3.720							
	Set up time		H	1.200		3.310							
	Hold time		D0	0.410		0.070							
	Hold time		D1	0.350		0.000							
	Hold time		S0	0.480		0.120							
	Hold time		S1	0.430		0.000							
	Hold time		H	0.300		0.000							
	Release time		RB	0.300		0.000							
Removal time		RB	0.950		1.880								
Min Pulse		CB	1.090		3.879								
Min Pulse		RB	0.713		2.100								

[MEMO]

[MEMO]

## 2.12 T-F/F, JK-F/F

[MEMO]

Chapter 2 Function Block

Function	T-F/F with R, S																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power							L744	7																																		
x1	F744	9	F744NQ	8																																						
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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T	R	S	Q	QB																																						
/	0	0	Invert																																							
\	0	0	Hold																																							
X	1	0	0	1																																						
X	0	1	1	0																																						
X	1	1	1	1																																						
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
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T	R	S	Q																																							
/	0	0	Invert																																							
\	0	0	Hold																																							
X	1	0	0																																							
X	0	1	1																																							
X	1	1	1																																							
Logic Diagram for "QB output"				Truth Table for "QB output"																																						

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F744	T → Q	(HH)		0.475	0.811	1.694	0.015	0.022	0.032	T	1.0	Q	22
		(HL)		0.625	1.114	2.376	0.012	0.018	0.028	R	2.1	QB	20
	T → QB	(HH)		0.823	1.492	3.254	0.015	0.021	0.030	S	2.2		
		(HL)		0.854	1.471	3.136	0.014	0.019	0.029				
	R → Q	(HL)		0.530	1.135	2.450	0.012	0.017	0.027				
	R → QB	(HH)		0.267	0.537	1.012	0.015	0.023	0.036				
	S → Q	(HH)		0.207	0.323	0.606	0.015	0.022	0.032				
	S → QB	(HL)		0.583	1.456	3.003	0.014	0.023	0.037				
	Release time	R		0.650		2.020							
	Release time	S		0.220		0.000							
	Removal time	R		0.630		0.440							
	Removal time	S		1.040		1.840							
	Min Pulse	T		1.152		3.827							
	Min Pulse	R		1.124		3.226							
Min Pulse	S		1.097		3.580								
L744	T → Q	(HH)		0.457	0.797	1.698	0.052	0.078	0.117	T	1.0	Q	3
		(HL)		0.400	0.655	1.325	0.025	0.035	0.053	R	2.2		
	R → Q	(HL)		0.137	0.181	0.286	0.021	0.029	0.042	S	2.1		
	S → Q	(HH)		0.364	0.723	1.542	0.053	0.080	0.121				
	Release time	R		0.210		0.000							
	Release time	S		0.640		1.990							
	Removal time	R		1.040		1.830							
	Removal time	S		0.630		0.440							
	Min Pulse	T		0.724		2.271							
	Min Pulse	R		0.325		0.789							
Min Pulse	S		0.861		2.285								
F744NQ	T → Q	(HH)		0.476	0.813	1.698	0.015	0.022	0.032	T	1.0	Q	22
		(HL)		0.625	1.115	2.379	0.012	0.018	0.028	R	2.1		
	R → Q	(HL)		0.526	1.036	2.225	0.012	0.017	0.027	S	2.2		
	S → Q	(HH)		0.207	0.323	0.606	0.015	0.022	0.032				
	Release time	R		0.650		2.020							
	Release time	S		0.220		0.000							
	Removal time	R		0.630		0.440							
Removal time	S		1.040		1.830								
Min Pulse	T		0.892		2.951								
Min Pulse	R		1.027		2.967								
Min Pulse	S		0.447		1.203								

Chapter 2 Function Block

Function	T-F/F with RB																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power																												
x1	F745	8	F745NQ	7																								
x2																												
x4																												
Logic Diagram for "Normal"					Truth Table for "Normal"																							
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T	RB	Q	QB																									
/	1	Invert																										
\	1	Hold																										
X	0	0	1																									
Logic Diagram for "Q output"					Truth Table for "Q output"																							
					<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>/</td> <td>1</td> <td>Invert</td> </tr> <tr> <td>\</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								T	RB	Q	/	1	Invert	\	1	Hold	X	0	0				
T	RB	Q																										
/	1	Invert																										
\	1	Hold																										
X	0	0																										
Logic Diagram for "QB output"					Truth Table for "QB output"																							

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F745	T	→	Q (HH)	0.508	0.883	1.917	0.015	0.022	0.034	T	1.0	Q	21
			(HL)	0.534	0.931	1.969	0.012	0.016	0.024				
	T	→	QB (HH)	0.716	1.257	2.700	0.015	0.021	0.031	RB	2.1	QB	20
			(HL)	0.752	1.307	2.858	0.012	0.016	0.024				
	RB	→	Q (LL)	0.248	0.412	0.805	0.012	0.016	0.024				
	RB	→	QB (LH)	0.438	0.900	1.845	0.015	0.023	0.035				
	Release time		RB	0.310		0.090							
	Removal time		RB	0.930		1.510							
	Min Pulse		T	1.041		3.439							
	Min Pulse		RB	0.822		2.392							
F745NQ	T	→	Q (HH)	0.507	0.883	1.919	0.015	0.022	0.034	T	1.0	Q	21
			(HL)	0.532	0.930	1.968	0.012	0.016	0.024				
	RB	→	Q (LL)	0.247	0.411	0.804	0.012	0.016	0.024	RB	2.1		
	Release time		RB	0.310		0.080							
	Removal time		RB	0.930		1.510							
	Min Pulse		T	0.800		2.542							
	Min Pulse		RB	0.506		1.325							



Chapter 2 Function Block

Function	T-F/F with RB, SB																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power									L747	7																																
x1	F747	9	F747NQ	8																																						
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
				<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>/</td> <td>1</td> <td>1</td> <td>Invert</td> <td></td> </tr> <tr> <td>\</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>									T	RB	SB	Q	QB	/	1	1	Invert		\	1	1	Hold		X	0	1	0	1	X	1	0	1	0	X	0	0	0	0
T	RB	SB	Q	QB																																						
/	1	1	Invert																																							
\	1	1	Hold																																							
X	0	1	0	1																																						
X	1	0	1	0																																						
X	0	0	0	0																																						
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
				<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>SB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>/</td> <td>1</td> <td>1</td> <td>Invert</td> </tr> <tr> <td>\</td> <td>1</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>									T	RB	SB	Q	/	1	1	Invert	\	1	1	Hold	X	0	1	0	X	1	0	1	X	0	0	0						
T	RB	SB	Q																																							
/	1	1	Invert																																							
\	1	1	Hold																																							
X	0	1	0																																							
X	1	0	1																																							
X	0	0	0																																							
Logic Diagram for "QB output"				Truth Table for "QB output"																																						

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F747	T	→	Q (HH)	0.516	0.894	1.932	0.015	0.022	0.034	T	1.0	Q	21
			(HL)	0.558	0.983	2.114	0.012	0.016	0.024				
			(LL)	0.759	1.316	2.877	0.012	0.016	0.024				
			(LH)	0.239	0.397	0.784	0.012	0.016	0.024	RB	2.2	QB	17
	T	→	QB (HH)	0.822	1.480	3.314	0.015	0.022	0.034				
			(LL)	0.507	1.176	2.584	0.015	0.025	0.040				
			(LH)	0.528	1.289	2.843	0.015	0.022	0.033	SB	2.0		
	RB	→	Q (LL)	0.239	0.397	0.784	0.012	0.016	0.024				
	RB	→	QB (LH)	0.507	1.176	2.584	0.015	0.025	0.040				
			(LH)	0.528	1.289	2.843	0.015	0.022	0.033				
			(LL)	0.317	0.736	1.430	0.012	0.019	0.030				
		Release time	RB	0.300		0.090							
		Release time	SB	0.590		0.860							
		Removal time	RB	0.950		1.600							
	Removal time	SB	0.630		0.650								
	Min Pulse	T	1.090		3.888								
	Min Pulse	RB	0.954		3.117								
	Min Pulse	SB	1.087		3.443								
L747	T	→	Q (HH)	0.448	0.775	1.652	0.030	0.044	0.067	T	1.0	Q	6
			(HL)	0.414	0.685	1.421	0.035	0.052	0.086				
			(LL)	0.427	0.900	1.931	0.035	0.055	0.092				
			(LH)	0.140	0.194	0.356	0.024	0.042	0.062	RB	2.0		
	RB	→	Q (LL)	0.427	0.900	1.931	0.035	0.055	0.092				
	SB	→	Q (LH)	0.140	0.194	0.356	0.024	0.042	0.062				
		Release time	RB	0.590		0.850							
		Release time	SB	0.300		0.010							
		Removal time	RB	0.630		0.650							
		Removal time	SB	0.950		1.600							
		Min Pulse	T	0.716		2.227							
	Min Pulse	RB	0.877		2.536								
	Min Pulse	SB	0.323		0.785								
F747NQ	T	→	Q (HH)	0.518	0.898	1.940	0.015	0.022	0.034	T	1.0	Q	21
			(HL)	0.558	0.983	2.112	0.012	0.016	0.024				
			(LL)	0.239	0.398	0.784	0.012	0.016	0.024				
			(LH)	0.529	1.122	2.477	0.015	0.022	0.033	RB	2.2		
	RB	→	Q (LL)	0.239	0.398	0.784	0.012	0.016	0.024				
	SB	→	Q (LH)	0.529	1.122	2.477	0.015	0.022	0.033				
		Release time	RB	0.300		0.080							
		Release time	SB	0.590		0.860							
		Removal time	RB	0.950		1.600							
		Removal time	SB	0.630		0.650							
		Min Pulse	T	0.826		2.687							
	Min Pulse	RB	0.491		1.298								
	Min Pulse	SB	0.984		3.080								

Chapter 2 Function Block

Function	T-F/F with Data-Hold R, S																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F791	12																																																				
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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T	TE	R	S	Q	QB																																																	
/	1	0	0		Invert																																																	
\	1	0	0		Hold																																																	
X	0	0	0		Hold																																																	
X	X	1	0	0	1																																																	
X	X	0	1	1	0																																																	
X	X	1	1	1	1																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 2 Function Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
F791	T	→	Q	(HH)	0.534	0.911	1.893	0.015	0.022	0.033	T	1.0	Q	21
				(HL)	0.733	1.314	2.781	0.014	0.020	0.032	TE	1.7	QB	21
	T	→	QB	(HH)	0.901	1.651	3.576	0.014	0.021	0.030	R	2.1		
				(HL)	0.841	1.466	3.110	0.013	0.018	0.027	S	2.2		
	R	→	Q	(HL)	0.639	1.205	2.564	0.013	0.019	0.030				
	R	→	QB	(HH)	0.234	0.420	0.784	0.015	0.022	0.034				
	S	→	Q	(HH)	0.257	0.402	0.761	0.015	0.022	0.033				
	S	→	QB	(HL)	0.562	1.199	2.481	0.013	0.020	0.031				
	Set up time	TE			1.140		3.520							
	Hold time	TE			0.410		0.000							
	Release time	R			0.670		2.090							
	Release time	S			0.220		0.000							
	Removal time	R			0.620		0.420							
	Removal time	S			1.040		1.850							
Min Pulse	T			1.166		4.149								
Min Pulse	R			1.055		3.266								
Min Pulse	S			1.028		3.162								

Chapter 2 Function Block

Function	T-F/F (TB) with RB																											
Block type	Standard type						Low Gate type																					
	Normal		Q output		QB output		Normal		Q output		QB output																	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Low Power																												
x1	F765	8	F765NQ	7																								
x2																												
x4																												
Logic Diagram for "Normal"					Truth Table for "Normal"																							
					<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>↘</td> <td>1</td> <td colspan="2">Invert</td> </tr> <tr> <td>↗</td> <td>1</td> <td colspan="2">Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								T	RB	Q	QB	↘	1	Invert		↗	1	Hold		X	0	0	1
T	RB	Q	QB																									
↘	1	Invert																										
↗	1	Hold																										
X	0	0	1																									
Logic Diagram for "Q output"					Truth Table for "Q output"																							
					<table border="1"> <thead> <tr> <th>T</th> <th>RB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>↘</td> <td>1</td> <td>Invert</td> </tr> <tr> <td>↗</td> <td>1</td> <td>Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>								T	RB	Q	↘	1	Invert	↗	1	Hold	X	0	0				
T	RB	Q																										
↘	1	Invert																										
↗	1	Hold																										
X	0	0																										
Logic Diagram for "QB output"					Truth Table for "QB output"																							
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T	RB	Q	QB																									
↘	1	Invert																										
↗	1	Hold																										
X	0	0	1																									

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F765	TB	→	Q (LH)	0.573	1.064	2.370	0.015	0.022	0.034	TB	1.0	Q	21
			(LL)	0.476	0.847	1.795	0.012	0.016	0.024			QB	20
	TB	→	QB (LH)	0.661	1.173	2.525	0.015	0.021	0.031	RB	2.1		
			(LL)	0.818	1.490	3.315	0.012	0.016	0.024				
	RB	→	Q (LL)	0.248	0.412	0.805	0.012	0.016	0.024				
	RB	→	QB (LH)	0.438	0.900	1.844	0.015	0.023	0.035				
	Release time		RB	0.300		0.000							
	Removal time		RB	0.940		1.870							
	Min Pulse		TB	1.077		3.830							
	Min Pulse		RB	0.822		2.392							
F765NQ	TB	→	Q (LH)	0.571	1.063	2.370	0.015	0.022	0.034	TB	1.0	Q	21
			(LL)	0.476	0.847	1.797	0.012	0.016	0.024			QB	20
	RB	→	Q (LL)	0.247	0.411	0.804	0.012	0.016	0.024	RB	2.1		
	Release time		RB	0.300		0.000							
	Removal time		RB	0.940		1.860							
	Min Pulse		TB	0.831		2.884							
Min Pulse		RB	0.506		1.325								

Chapter 2 Function Block

Function	T-F/F (TB) with RB, SB																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power								L767	7																																	
x1	F767	9	F767NQ	8																																						
x2																																										
x4																																										
Logic Diagram for "Normal"			Truth Table for "Normal"																																							
			<table border="1"> <thead> <tr> <th>TB</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>↘</td> <td>1</td> <td>1</td> <td colspan="2">Invert</td> </tr> <tr> <td>↗</td> <td>1</td> <td>1</td> <td colspan="2">Hold</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>										TB	RB	SB	Q	QB	↘	1	1	Invert		↗	1	1	Hold		X	0	1	0	1	X	1	0	1	0	X	0	0	0	0
TB	RB	SB	Q	QB																																						
↘	1	1	Invert																																							
↗	1	1	Hold																																							
X	0	1	0	1																																						
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Logic Diagram for "Q output"			Truth Table for "Q output"																																							
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TB	RB	SB	Q																																							
↘	1	1	Invert																																							
↗	1	1	Hold																																							
X	0	1	0																																							
X	1	0	1																																							
X	0	0	0																																							
Logic Diagram for "QB output"			Truth Table for "QB output"																																							

Chapter 2 Function Block

Block type	Switching speed								Input		Output				
	Path			t LDO (ns)			t 1								
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout		
F767	TB	→	Q (LH)	0.572	1.064	2.366	0.015	0.022	0.034	TB	1.0	Q	21		
			(LL)	0.499	0.895	1.921	0.012	0.016	0.024			RB		2.2	
	TB	→	QB (LH)	0.765	1.392	3.119	0.015	0.022	0.034			SB		2.0	
			(LL)	0.813	1.486	3.313	0.012	0.016	0.024						
	RB	→	Q (LL)	0.239	0.397	0.784	0.012	0.016	0.024						
	RB	→	QB (LH)	0.507	1.176	2.585	0.015	0.025	0.040						
	SB	→	Q (LH)	0.528	1.290	2.843	0.015	0.022	0.033						
	SB	→	QB (LL)	0.317	0.736	1.430	0.012	0.019	0.030						
	Release time		RB	0.290		0.000									
	Release time		SB	0.580		1.170									
	Removal time		RB	0.960		1.920									
	Removal time		SB	0.640		0.780									
	Min Pulse		TB	1.073		3.827									
	Min Pulse		RB	0.954		3.117									
Min Pulse		SB	1.087		3.444										
L767	TB	→	Q (LH)	0.391	0.689	1.466	0.030	0.044	0.067	TB	1.0	Q	6		
			(LL)	0.468	0.850	1.845	0.035	0.052	0.086			RB		2.0	
	RB	→	Q (LL)	0.427	0.901	1.932	0.035	0.055	0.092			SB		2.2	
	SB	→	Q (LH)	0.140	0.194	0.356	0.024	0.042	0.062						
	Release time		RB	0.580		1.160									
	Release time		SB	0.290		0.000									
	Removal time		RB	0.640		0.780									
	Removal time		SB	0.960		1.920									
	Min Pulse		TB	0.728		2.360									
	Min Pulse		RB	0.876		2.535									
	Min Pulse		SB	0.323		0.785									
	F767NQ	TB	→	Q (LH)	0.572	1.064	2.368	0.015	0.022	0.034	TB	1.0	Q	21	
				(LL)	0.500	0.897	1.925	0.012	0.016	0.024			RB		2.2
		RB	→	Q (LL)	0.239	0.398	0.784	0.012	0.016	0.024			SB		2.0
SB		→	Q (LH)	0.529	1.122	2.477	0.015	0.022	0.033						
Release time			RB	0.290		0.000									
Release time			SB	0.580		1.170									
Removal time			RB	0.960		1.920									
Removal time			SB	0.640		0.780									
Min Pulse			TB	0.832		2.882									
Min Pulse			RB	0.490		1.298									
Min Pulse			SB	0.985		3.080									

Chapter 2 Function Block

Function	T-F/F (TB) with Data-Hold RB, SB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F792	12																																																				
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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TB	TEB	RB	SB	Q	QB																																																	
↘	0	1	1		Invert																																																	
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X	1	1	1		Hold																																																	
X	X	0	1	0	1																																																	
X	X	1	0	1	0																																																	
X	X	0	0	0	0																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F792	TB	→	Q (LH)	0.648	1.205	2.676	0.015	0.023	0.036	TB	1.0	Q	20
			(LL)	0.569	1.022	2.171	0.012	0.017	0.026	TEB	1.7	QB	19
	TB	→	QB (LH)	0.801	1.465	3.239	0.015	0.022	0.032	RB	2.2		
			(LL)	0.847	1.567	3.501	0.012	0.016	0.023	SB	2.0		
	RB	→	Q (LL)	0.304	0.516	1.015	0.012	0.017	0.026				
	RB	→	QB (LH)	0.539	1.113	2.417	0.015	0.023	0.036				
	SB	→	Q (LH)	0.613	1.230	2.715	0.015	0.023	0.035				
	SB	→	QB (LL)	0.273	0.554	1.070	0.012	0.017	0.027				
	Set up time		TEB	1.250		3.300							
	Hold time		TEB	0.510		0.290							
	Release time		RB	0.300		0.000							
	Release time		SB	0.590		1.240							
	Removal time		RB	0.960		1.930							
	Removal time		SB	0.640		0.760							
Min Pulse		TB	1.106		4.013								
Min Pulse		RB	0.951		2.998								
Min Pulse		SB	1.011		3.294								

Chapter 2 Function Block

Function	JK-F/F																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F771	10	F771NQ	9	F771NB	9																																				
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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J	K	C	Q	QB																																						
0	0	/	Hold																																							
0	1	/	0	1																																						
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1	1	/	Invert																																							
X	X	\	Hold																																							
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
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0	0	/	Hold																																							
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Logic Diagram for "QB output"				Truth Table for "QB output"																																						
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0	1	/	1																																							
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1	1	/	Invert																																							
X	X	\	Hold																																							

Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F771	C → Q	(HH)		0.451	0.757	1.565	0.015	0.022	0.032	J	1.0	Q	22
				0.526	0.919	1.944	0.012	0.016	0.024	K	1.0	QB	22
				0.692	1.183	2.469	0.012	0.017	0.025	C	1.0		
	C → QB	(HL)		1.040									
			Set up time	J	0.950								
			Set up time	K	0.310								
			Hold time	K	0.350								
Min Pulse	C	0.976											
F771NQ	C → Q	(HH)		0.421	0.734	1.555	0.015	0.023	0.034	J	1.0	Q	21
				0.423	0.734	1.479	0.013	0.019	0.029	K	1.0		
	C → QB	(HL)		0.980									
			Set up time	J	1.020								
			Set up time	K	0.260								
			Hold time	K	0.310								
Min Pulse	C	0.710											
F771NB	C → QB	(HH)		0.421	0.734	1.555	0.015	0.023	0.034	J	1.0	QB	21
				0.423	0.734	1.479	0.013	0.019	0.029	K	1.0		
	C → Q	(HL)		1.020									
			Set up time	J	0.950								
			Set up time	K	0.310								
			Hold time	K	0.350								
Min Pulse	C	0.710											

Chapter 2 Function Block

Function	JK-F/F, High Speed																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F7D1	10																																								
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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J	K	C	Q	QB																																						
0	0	/	Hold																																							
0	1	/	0	1																																						
1	0	/	1	0																																						
1	1	/	Invert																																							
X	X	\	Hold																																							
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
Logic Diagram for "QB output"				Truth Table for "QB output"																																						

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F7D1	C → Q	(HH)		0.430	0.745	1.570	0.015	0.023	0.035	J	1.0	Q	21
		(HL)		0.434	0.755	1.506	0.013	0.019	0.030	K	1.0	QB	22
	C → QB	(HH)		0.575	1.041	2.182	0.014	0.021	0.030	C	1.0		
		(HL)		0.596	1.058	2.276	0.011	0.015	0.023				
	Set up time	J		0.980		2.180							
	Set up time	K		1.020		2.340							
	Hold time	J		0.260		0.000							
	Hold time	K		0.310		0.000							
	Min Pulse	C		0.861		2.848							

Chapter 2 Function Block

Function	JK-F/F with R, S																																																																										
Block type	Standard type					Low Gate type																																																																					
	Normal		Q output		QB output		Normal		Q output		QB output																																																																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																															
Low Power																																																																											
x1	F774	12	F774NQ	11	F774NB	11																																																																					
x2																																																																											
x4																																																																											
Logic Diagram for "Normal"			Truth Table for "Normal"																																																																								
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J	K	C	R	S	Q	QB																																																																					
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Logic Diagram for "Q output"			Truth Table for "Q output"																																																																								
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J	K	C	R	S	QB																																																																						
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Chapter 2 Function Block

Block type	Switching speed								Input		Output	
	Path			t LDO (ns)			t 1					
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol
F774	C → Q	(HH)	0.471	0.803	1.679	0.015	0.022	0.032	J	1.0	Q	22
		(HL)	0.623	1.111	2.372	0.012	0.018	0.028	K	1.0	QB	21
	C → QB	(HH)	0.826	1.511	3.290	0.015	0.021	0.030	C	1.0		
		(HL)	0.862	1.516	3.218	0.014	0.019	0.030	R	2.1		
	R → Q	(HL)	0.530	1.070	2.305	0.012	0.017	0.027	S	2.2		
	R → QB	(HH)	0.273	0.488	0.922	0.015	0.023	0.035				
	S → Q	(HH)	0.207	0.322	0.606	0.015	0.022	0.032				
	S → QB	(HL)	0.596	1.289	2.679	0.014	0.021	0.034				
	Set up time	J		1.030		3.300						
	Set up time	K		0.980		2.370						
	Hold time	J		0.250		0.000						
	Hold time	K		0.330		0.000						
	Release time	R		0.660		2.070						
	Release time	S		0.220		0.000						
	Removal time	R		0.620		0.420						
Removal time	S		1.050		1.860							
Min Pulse	C		1.160		3.863							
Min Pulse	R		1.032		3.056							
Min Pulse	S		0.986		3.262							
F774NQ	C → Q	(HH)	0.471	0.804	1.681	0.015	0.022	0.032	J	1.0	Q	22
		(HL)	0.622	1.111	2.371	0.012	0.018	0.028	K	1.0		
	R → Q	(HL)	0.527	0.981	2.095	0.012	0.017	0.027	C	1.0		
	S → Q	(HH)	0.207	0.323	0.606	0.015	0.022	0.032	R	2.1		
	Set up time	J		1.030		3.290			S	2.2		
	Set up time	K		0.980		2.380						
	Hold time	J		0.250		0.000						
	Hold time	K		0.330		0.000						
	Release time	R		0.660		2.070						
	Release time	S		0.210		0.000						
	Removal time	R		0.620		0.420						
	Removal time	S		1.050		1.870						
	Min Pulse	C		0.888		2.944						
	Min Pulse	R		0.938		2.801						
	Min Pulse	S		0.447		1.203						
F774NB	C → QB	(HH)	0.426	0.738	1.557	0.015	0.023	0.034	J	1.0	QB	20
		(HL)	0.454	0.814	1.669	0.014	0.021	0.034	K	1.0		
	R → QB	(HH)	0.340	0.615	1.278	0.015	0.023	0.035	C	1.0		
	S → QB	(HL)	0.727	1.373	3.073	0.015	0.022	0.034	R	2.1		
	Set up time	J		1.020		3.420			S	2.2		
	Set up time	K		0.970		2.330						
	Hold time	J		0.240		0.000						
	Hold time	K		0.340		0.000						
	Release time	R		0.620		2.200						
	Release time	S		0.190		0.000						
	Removal time	R		0.610		0.380						
	Removal time	S		1.010		1.800						
	Min Pulse	C		0.749		2.242						
	Min Pulse	R		0.769		2.008						
	Min Pulse	S		1.040		3.647						



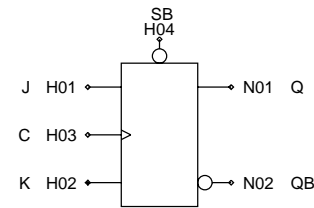
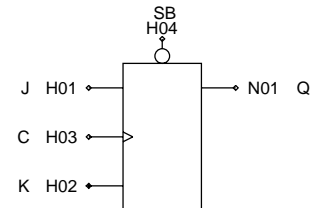
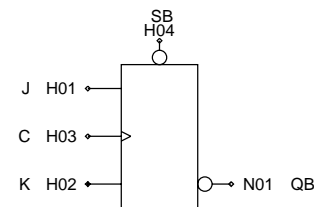
Chapter 2 Function Block

Function	JK-F/F with RB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F775	11	F775NQ	10	F775NB	10																																																
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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J	K	C	RB	Q	QB																																																	
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Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F775	C → Q	(HH)		0.504	0.876	1.904	0.015	0.022	0.034	J	1.0	Q	21
			(HL)	0.532	0.930	1.966	0.012	0.016	0.024	K	1.0	QB	21
	C → QB	(HH)		0.720	1.275	2.734	0.015	0.022	0.031	C	1.0		
			(HL)	0.759	1.334	2.907	0.012	0.016	0.024	RB	2.1		
	RB → Q	(LL)		0.248	0.412	0.804	0.012	0.016	0.024				
			(LH)	0.445	0.847	1.751	0.015	0.022	0.033				
	Set up time	J		1.040		2.350							
	Set up time	K		0.960		2.260							
	Hold time	J		0.300		0.000							
	Hold time	K		0.340		0.000							
	Release time	RB		0.310		0.090							
	Removal time	RB		0.930		1.510							
	Min Pulse	C		1.046		3.488							
	Min Pulse	RB		0.776		2.297							
F775NQ	C → Q	(HH)		0.505	0.878	1.908	0.015	0.022	0.034	J	1.0	Q	21
			(HL)	0.531	0.929	1.966	0.012	0.016	0.024	K	1.0		
	RB → Q	(LL)		0.249	0.412	0.806	0.012	0.016	0.024	C	1.0		
			(LH)	0.445	0.847	1.751	0.015	0.022	0.033	RB	2.1		
	Set up time	J		1.040		2.350							
	Set up time	K		0.960		2.260							
	Hold time	J		0.300		0.000							
	Hold time	K		0.340		0.000							
	Release time	RB		0.310		0.090							
	Removal time	RB		0.930		1.510							
Min Pulse	C		0.799		2.540								
Min Pulse	RB		0.508		1.326								
F775NB	C → QB	(HH)		0.426	0.740	1.564	0.015	0.023	0.035	J	1.0	QB	21
			(HL)	0.422	0.722	1.455	0.013	0.019	0.030	K	1.0		
	RB → QB	(LH)		0.465	1.032	2.263	0.015	0.023	0.034	C	1.0		
			(LH)	0.465	1.032	2.263	0.015	0.023	0.034	RB	2.1		
	Set up time	J		1.020		2.400							
	Set up time	K		0.960		2.240							
	Hold time	J		0.290		0.000							
	Hold time	K		0.340		0.000							
	Release time	RB		0.300		0.140							
	Removal time	RB		0.900		1.450							
Min Pulse	C		0.711		2.141								
Min Pulse	RB		0.867		2.792								

## Chapter 2 Function Block

Function	JK-F/F with SB																																																					
Block type	Standard type						Low Gate type																																															
	Normal		Q output		QB output		Normal		Q output		QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Low Power																																																						
x1	F776	11	F776NQ	10	F776NB	10																																																
x2																																																						
x4																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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## Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F776	C → Q	(HH)		0.481	0.802	1.654	0.014	0.021	0.031	J	1.0	Q	21
			(HL)	0.580	1.014	2.173	0.011	0.016	0.023				
			(LH)	0.698	1.193	2.488	0.012	0.017	0.025				
	C → QB	(HH)		0.830	1.506	3.360	0.015	0.023	0.035	C	1.0	QB	20
			(HL)	0.494	1.088	2.345	0.014	0.021	0.031				
			(LH)	0.325	0.654	1.274	0.012	0.018	0.029				
	SB → Q	(LL)		1.100		2.310				J			
				1.020		2.530							
	SB → QB	(LL)		0.310		0.000				K			
				0.350		0.000							
	Set up time		J	0.600		0.940				SB			
	Set up time		K	0.610		0.580							
	Hold time		J	1.097		3.933							
	Hold time		K	0.941		2.938							
Release time		SB											
Removal time		SB											
Min Pulse		C											
Min Pulse		SB											
F776NQ	C → Q	(HH)		0.482	0.803	1.658	0.014	0.021	0.031	J	1.0	Q	21
			(HL)	0.579	1.013	2.170	0.011	0.016	0.023				
			(LH)	0.496	0.941	2.005	0.014	0.021	0.031				
	SB → Q	(LH)		1.100		2.310				K	1.0		
				1.020		2.530							
				0.310		0.000							
	SB → QB	(LH)		0.350		0.000				C	1.0		
				0.600		0.930							
	Set up time		J	0.610		0.590				SB			
	Set up time		K	0.847		2.744							
	Hold time		J	0.849		2.592							
	Hold time		K										
	Release time		SB										
	Removal time		SB										
Min Pulse		C											
Min Pulse		SB											
F776NB	C → QB	(HH)		0.496	0.863	1.860	0.015	0.023	0.036	J	1.0	QB	17
			(HL)	0.462	0.790	1.590	0.013	0.018	0.028				
			(LH)	0.447	0.871	1.850	0.013	0.018	0.028				
	SB → QB	(LL)		1.080		2.350				K	1.0		
				1.030		2.560							
				0.300		0.000							
	SB → Q	(LL)		0.360		0.000				C	1.0		
				0.610		0.960							
	Set up time		J	0.600		0.520							
	Set up time		K	0.765		2.437							
	Hold time		J	0.814		2.449							
	Hold time		K										
	Release time		SB										
	Removal time		SB										
Min Pulse		C											
Min Pulse		SB											

Chapter 2 Function Block

Function	JK-F/F with RB, SB																																																																										
Block type	Standard type					Low Gate type																																																																					
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Chapter 2 Function Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F777	C → Q	(HH)		0.512	0.887	1.918	0.015	0.022	0.034	J	1.0	Q	21
		(HL)		0.556	0.981	2.110	0.012	0.016	0.024	K	1.0	QB	19
	C → QB	(HH)		0.828	1.509	3.375	0.015	0.023	0.035	C	1.0		
		(HL)		0.763	1.341	2.923	0.012	0.016	0.024	RB	2.2		
	RB → Q	(LL)		0.239	0.397	0.784	0.012	0.016	0.024	SB	2.0		
	RB → QB	(LH)		0.517	1.078	2.383	0.015	0.024	0.037				
	SB → Q	(LH)		0.529	1.197	2.639	0.015	0.022	0.033				
	SB → QB	(LL)		0.326	0.654	1.275	0.012	0.018	0.029				
	Set up time	J		1.100		2.360							
	Set up time	K		1.020		2.540							
	Hold time	J		0.300		0.000							
	Hold time	K		0.350		0.000							
	Release time	RB		0.310		0.100							
	Release time	SB		0.600		0.930							
	Removal time	RB		0.950		1.600							
Removal time	SB		0.630		0.620								
Min Pulse	C		1.096		3.949								
Min Pulse	RB		0.884		2.915								
Min Pulse	SB		1.007		3.235								
F777NQ	C → Q	(HH)		0.512	0.889	1.923	0.015	0.022	0.034	J	1.0	Q	21
		(HL)		0.555	0.980	2.107	0.012	0.016	0.024	K	1.0		
	RB → Q	(LH)		0.239	0.397	0.784	0.012	0.016	0.024	C	1.0		
	SB → Q	(LH)		0.531	1.041	2.290	0.015	0.022	0.033	RB	2.2		
	Set up time	J		1.090		2.360				SB	2.0		
	Set up time	K		1.010		2.540							
	Hold time	J		0.300		0.000							
	Hold time	K		0.350		0.000							
	Release time	RB		0.310		0.100							
	Release time	SB		0.600		0.930							
	Removal time	RB		0.950		1.590							
	Removal time	SB		0.630		0.630							
	Min Pulse	C		0.823		2.681							
	Min Pulse	RB		0.490		1.297							
	Min Pulse	SB		0.909		2.878							
F777NB	C → QB	(HH)		0.465	0.817	1.758	0.016	0.024	0.038	J	1.0	QB	19
		(HL)		0.428	0.736	1.475	0.013	0.019	0.029	K	1.0		
	RB → QB	(LH)		0.569	1.241	2.861	0.016	0.024	0.037	C	1.0		
	SB → QB	(LL)		0.408	0.813	1.726	0.013	0.019	0.029	RB	2.2		
	Set up time	J		1.070		2.410				SB	2.0		
	Set up time	K		1.020		2.560							
	Hold time	J		0.290		0.000							
	Hold time	K		0.350		0.000							
	Release time	RB		0.290		0.150							
	Release time	SB		0.610		0.960							
	Removal time	RB		0.910		1.500							
	Removal time	SB		0.610		0.560							
	Min Pulse	C		0.733		2.334							
	Min Pulse	RB		0.971		3.381							
	Min Pulse	SB		0.777		2.326							

## Chapter 2 Function Block

Function	JK-F/F (CB)																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F781	10	F781NQ	9	F781NB	9																																				
x2																																										
x4																																										
Logic Diagram for "Normal"				Truth Table for "Normal"																																						
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J	K	CB	Q	QB																																						
0	0	\	Hold																																							
0	1	\	0	1																																						
1	0	\	1	0																																						
1	1	\	Invert																																							
X	X	/	Hold																																							
Logic Diagram for "Q output"				Truth Table for "Q output"																																						
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J	K	CB	Q																																							
0	0	\	Hold																																							
0	1	\	0																																							
1	0	\	1																																							
1	1	\	Invert																																							
X	X	/	Hold																																							
Logic Diagram for "QB output"				Truth Table for "QB output"																																						
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J	K	CB	QB																																							
0	0	\	Hold																																							
0	1	\	1																																							
1	0	\	0																																							
1	1	\	Invert																																							
X	X	/	Hold																																							

## Chapter 2 Function Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F781	CB → Q	(LH)		0.506	0.930	2.011	0.015	0.022	0.032	J	1.0	Q	22
		(LL)		0.470	0.835	1.769	0.012	0.016	0.024				
		(LL)		0.747	1.356	2.918	0.012	0.017	0.025				
	CB → QB	(LH)		0.656	1.177	2.531	0.015	0.022	0.032	K	1.0	QB	22
		(LL)		0.747	1.356	2.918	0.012	0.017	0.025				
		Set up time	J		1.080		2.250						
		Set up time	K		1.000		2.170						
Hold time	J		0.320		0.000								
Hold time	K		0.510		0.170								
Min Pulse	CB		1.006		3.428								
F781NQ	CB → Q	(LH)		0.381	0.686	1.470	0.015	0.023	0.035	J	1.0	Q	21
		(LL)		0.438	0.834	1.806	0.013	0.019	0.029				
		Set up time	J		1.030		2.270						
	Set up time	K		1.070		2.230							
	Hold time	J		0.430		0.000							
	Hold time	K		0.300		0.000							
	Min Pulse	CB		0.708		2.324							
F781NB	CB → QB	(LH)		0.381	0.686	1.470	0.015	0.023	0.035	J	1.0	QB	21
		(LL)		0.438	0.834	1.806	0.013	0.019	0.029				
		Set up time	J		1.070		2.230						
	Set up time	K		1.000		2.150							
	Hold time	J		0.300		0.000							
	Hold time	K		0.510		0.190							
	Min Pulse	CB		0.708		2.324							

Chapter 2 Function Block

Function	JK-F/F (CB), High Speed																																									
Block type	Standard type						Low Gate type																																			
	Normal		Q output		QB output		Normal		Q output		QB output																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																														
Low Power																																										
x1	F7E1	10																																								
x2																																										
x4																																										
Logic Diagram for "Normal"			Truth Table for "Normal"																																							
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J	K	CB	Q	QB																																						
0	0	\	Hold																																							
0	1	\	0	1																																						
1	0	\	1	0																																						
1	1	\	Invert																																							
X	X	/	Hold																																							
Logic Diagram for "Q output"			Truth Table for "Q output"																																							
Logic Diagram for "QB output"			Truth Table for "QB output"																																							

Chapter 2 Function Block

Block type	Switching speed									Input		Output	
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
F7E1	CB	→	Q (LH)	0.391	0.701	1.492	0.015	0.023	0.035	J	1.0	Q	21
			(LL)	0.446	0.845	1.819	0.013	0.019	0.030	K	1.0	QB	22
	CB	→	QB (LH)	0.589	1.134	2.497	0.014	0.021	0.030	CB	1.0		
			(LL)	0.558	1.016	2.203	0.011	0.015	0.023				
	Set up time		J	1.030		2.280							
	Set up time		K	1.070		2.230							
	Hold time		J	0.430		0.000							
Hold time		K	0.300		0.000								
Min Pulse		CB	0.860		3.015								

Chapter 2 Function Block

Function	JK-F/F (CB) with RB, SB																																																																										
Block type	Standard type					Low Gate type																																																																					
	Normal		Q output		QB output		Normal		Q output		QB output																																																																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																															
Low Power																																																																											
x1	F787	12	F787NQ	11	F787NB	11																																																																					
x2																																																																											
x4																																																																											
Logic Diagram for "Normal"			Truth Table for "Normal"																																																																								
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J	K	CB	RB	SB	Q	QB																																																																					
0	0	\	1	1	Hold																																																																						
0	1	\	1	1	0	1																																																																					
1	0	\	1	1	1	0																																																																					
1	1	\	1	1	Invert																																																																						
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X	X	X	1	0	1	0																																																																					
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Logic Diagram for "Q output"			Truth Table for "Q output"																																																																								
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J	K	CB	RB	SB	Q																																																																						
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Logic Diagram for "QB output"			Truth Table for "QB output"																																																																								
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X	X	X	1	0	0																																																																						
X	X	X	0	0	0																																																																						

Chapter 2 Function Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F787	CB → Q	(LH)		0.568	1.057	2.358	0.015	0.022	0.034	J	1.0	Q	21
		(LL)		0.496	0.889	1.909	0.012	0.016	0.024	K	1.0	QB	19
	CB → QB	(LH)		0.771	1.420	3.177	0.015	0.023	0.035	CB	1.0		
		(LL)		0.816	1.510	3.361	0.012	0.016	0.024	RB	2.2		
	RB → Q	(LH)		0.239	0.397	0.784	0.012	0.016	0.024	SB	2.0		
		(LL)		0.239	0.397	0.784	0.012	0.016	0.024				
	RB → QB	(LH)		0.517	1.078	2.383	0.015	0.024	0.037				
		(LL)		0.529	1.197	2.641	0.015	0.022	0.033				
	SB → Q	(LH)		0.326	0.654	1.275	0.012	0.018	0.029				
		(LL)		0.326	0.654	1.275	0.012	0.018	0.029				
	Set up time	J		1.150		2.450							
	Set up time	K		1.050		2.780							
	Hold time	J		0.310		0.000							
	Hold time	K		0.510		0.150							
	Release time	RB		0.300		0.000							
Release time	SB		0.590		1.230								
Removal time	RB		0.960		1.930								
Removal time	SB		0.640		0.760								
Min Pulse	CB		1.076		3.873								
Min Pulse	RB		0.884		2.914								
Min Pulse	SB		1.007		3.235								
F787NQ	CB → Q	(LH)		0.567	1.056	2.357	0.015	0.022	0.034	J	1.0	Q	21
		(LL)		0.496	0.890	1.911	0.012	0.016	0.024	K	1.0		
	RB → Q	(LH)		0.239	0.397	0.784	0.012	0.016	0.024	CB	1.0		
		(LL)		0.239	0.397	0.784	0.012	0.016	0.024	RB	2.2		
	SB → Q	(LH)		0.531	1.042	2.290	0.015	0.022	0.033	SB	2.0		
		(LL)		0.531	1.042	2.290	0.015	0.022	0.033				
	Set up time	J		1.150		2.450							
	Set up time	K		1.050		2.780							
	Hold time	J		0.310		0.000							
	Hold time	K		0.510		0.150							
	Release time	RB		0.300		0.000							
	Release time	SB		0.590		1.230							
	Removal time	RB		0.960		1.930							
	Removal time	SB		0.640		0.760							
	Min Pulse	CB		0.827		2.869							
Min Pulse	RB		0.490		1.297								
Min Pulse	SB		0.909		2.878								
F787NB	CB → QB	(LH)		0.419	0.762	1.656	0.016	0.024	0.038	J	1.0	QB	19
		(LL)		0.441	0.834	1.796	0.013	0.019	0.029	K	1.0		
	RB → QB	(LH)		0.569	1.240	2.861	0.016	0.024	0.037	CB	1.0		
		(LL)		0.407	0.814	1.727	0.013	0.019	0.029	RB	2.2		
	SB → QB	(LH)		0.407	0.814	1.727	0.013	0.019	0.029	SB	2.0		
		(LL)		0.407	0.814	1.727	0.013	0.019	0.029				
	Set up time	J		1.140		2.410							
	Set up time	K		1.050		2.740							
	Hold time	J		0.290		0.000							
	Hold time	K		0.520		0.180							
	Release time	RB		0.290		0.000							
	Release time	SB		0.600		1.200							
	Removal time	RB		0.910		1.840							
	Removal time	SB		0.630		0.730							
	Min Pulse	CB		0.712		2.316							
Min Pulse	RB		0.971		3.381								
Min Pulse	SB		0.777		2.326								

# **Chapter 3**

## **Scan Path Block**

[MEMO]

### 3.1 Standard Type



Chapter 3 Scan Path Block

Function	Scan D-F/F with R, S, 2 to 1 Selector																																																																			
Block type	Standard type																																																																			
	Normal				Q output				QB output																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
x1	s000	12																																																																		
x2																																																																				
x4																																																																				
x8																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>S</th> <th>R</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>X</td> <td>0</td> <td>1</td> </tr> <tr> <td>A</td> <td>/</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>X</td> <td>\</td> <td>X</td> <td>0</td> <td>0</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>X</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									SIN	SCK	SMC	S	R	D	Q	QB	X	X	X	1	0	X	1	0	X	X	X	0	1	X	0	1	A	/	0	0	0	X	A	AB	X	/	1	0	0	B	B	BB	X	\	X	0	0	X	Hold		X	X	X	1	1	X	1	1
SIN	SCK	SMC	S	R	D	Q	QB																																																													
X	X	X	1	0	X	1	0																																																													
X	X	X	0	1	X	0	1																																																													
A	/	0	0	0	X	A	AB																																																													
X	/	1	0	0	B	B	BB																																																													
X	\	X	0	0	X	Hold																																																														
X	X	X	1	1	X	1	1																																																													
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S000	SCK	→	Q	(HH)	0.472	0.806	1.683	0.015	0.022	0.032	SIN	1.0	Q	22
				(HL)	0.625	1.116	2.379	0.012	0.018	0.028	SCK	1.0	QB	21
	SCK	→	QB	(HH)	0.774	1.414	3.092	0.014	0.021	0.030	SMC	1.0		
				(HL)	0.762	1.329	2.841	0.013	0.018	0.027	S	2.2		
	S	→	Q	(HH)	0.209	0.325	0.609	0.015	0.022	0.032	R	2.1		
				(HL)	0.496	1.098	2.284	0.013	0.020	0.031	D	1.0		
	R	→	Q	(HL)	0.531	0.993	2.137	0.012	0.017	0.027				
				(HH)	0.228	0.411	0.772	0.015	0.022	0.034				
	Set up time		SIN		1.070		3.450							
	Set up time		SMC		1.100		3.760							
	Set up time		D		1.070		3.460							
	Hold time		SIN		0.370		0.000							
	Hold time		SMC		0.350		0.000							
	Hold time		D		0.360		0.000							
	Release time		S		0.220		0.000							
	Release time		R		0.670		2.090							
Removal time		S		1.050		1.860								
Removal time		R		0.620		0.430								
Min Pulse		SCK		1.059		3.664								
Min Pulse		S		0.891		2.872								
Min Pulse		R		0.935		2.840								

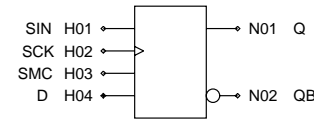
Chapter 3 Scan Path Block

Function	Scan D-F/F with 2 to 1 Selector																																			
Block type	Standard type																																			
	Normal				Q output				QB output																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																								
x1	S002	10																																		
x2																																				
x4																																				
x8																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>↗</td> <td>1</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>A</td> <td>↗</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>↘</td> <td>X</td> <td>X</td> <td></td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									SIN	SCK	SMC	D	Q	QB	X	↗	1	B	B	BB	A	↗	0	X	A	AB	X	↘	X	X		Hold
SIN	SCK	SMC	D	Q	QB																															
X	↗	1	B	B	BB																															
A	↗	0	X	A	AB																															
X	↘	X	X		Hold																															
Logic Diagram for "Q output"				Truth Table for "Q output"																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S002	SCK	→	Q (HH)	0.451	0.758	1.566	0.015	0.022	0.032	SIN	1.0	Q	22
			(HL)	0.527	0.921	1.947	0.012	0.016	0.024	SCK	1.0	QB	22
	SCK	→	QB (HH)	0.662	1.173	2.531	0.015	0.021	0.031	SMC	1.0		
			(HL)	0.629	1.069	2.245	0.012	0.016	0.023	D	1.0		
	Set up time		SIN	1.000		2.420							
	Set up time		SMC	1.010		2.730							
	Set up time		D	1.010		2.430							
	Hold time		SIN	0.360		0.000							
	Hold time		SMC	0.350		0.000							
	Hold time		D	0.350		0.000							
	Min Pulse		SCK	0.926		3.101							

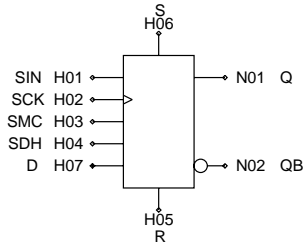
Chapter 3 Scan Path Block

Function	Scan D-F/F with 2 to 1 Selector, High Speed																																			
Block type	Standard type																																			
	Normal				Q output				QB output																											
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																								
Drivability																																				
x1	S003	11																																		
x2																																				
x4																																				
x8																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>↗</td> <td>1</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>A</td> <td>↗</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>↘</td> <td>X</td> <td>X</td> <td></td> <td>Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									SIN	SCK	SMC	D	Q	QB	X	↗	1	B	B	BB	A	↗	0	X	A	AB	X	↘	X	X		Hold
SIN	SCK	SMC	D	Q	QB																															
X	↗	1	B	B	BB																															
A	↗	0	X	A	AB																															
X	↘	X	X		Hold																															
Logic Diagram for "Q output"				Truth Table for "Q output"																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S003	SCK	→	Q (HH)	0.422	0.735	1.553	0.015	0.023	0.034	SIN	1.0	Q	21
			(HL)	0.426	0.738	1.482	0.013	0.019	0.029	SCK	1.0	QB	22
	SCK	→	QB (HH)	0.566	1.022	2.157	0.014	0.021	0.030	SMC	1.0		
			(HL)	0.588	1.049	2.262	0.011	0.015	0.023	D	1.0		
	Set up time		SIN	1.050		2.810							
	Set up time		SMC	1.090		3.080							
	Set up time		D	1.040		2.790							
	Hold time		SIN	0.280		0.000							
	Hold time		SMC	0.270		0.000							
	Hold time		D	0.280		0.000							
	Min Pulse		SCK	0.852		2.834							

Chapter 3 Scan Path Block

Function	Scan D-F/F with R, S, Hold, 2 to 1 Selector																																																																																			
Block type	Standard type																																																																																			
	Normal				Q output				QB output																																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																								
x1	S050	16																																																																																		
x2																																																																																				
x4																																																																																				
x8																																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																																
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>SDH</th> <th>S</th> <th>R</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>/</td> <td>X</td> <td>1</td> <td>0</td> <td>0</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>A</td> <td>/</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>X</td> <td>\</td> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>X</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>X</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>X</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									SIN	SCK	SMC	SDH	S	R	D	Q	QB	X	/	X	1	0	0	X	Hold		A	/	0	0	0	0	X	A	AB	X	/	1	0	0	0	B	B	BB	X	\	X	X	0	0	X	Hold		X	X	X	X	0	1	X	0	1	X	X	X	X	1	0	X	1	0	X	X	X	X	1	1	X	1	1
SIN	SCK	SMC	SDH	S	R	D	Q	QB																																																																												
X	/	X	1	0	0	X	Hold																																																																													
A	/	0	0	0	0	X	A	AB																																																																												
X	/	1	0	0	0	B	B	BB																																																																												
X	\	X	X	0	0	X	Hold																																																																													
X	X	X	X	0	1	X	0	1																																																																												
X	X	X	X	1	0	X	1	0																																																																												
X	X	X	X	1	1	X	1	1																																																																												
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S050	SCK → Q	(HH)		0.516	0.878	1.820	0.015	0.022	0.033	SIN	1.0	Q	21
		(HL)		0.707	1.260	2.650	0.013	0.019	0.031	SCK	1.0	QB	21
	SCK → QB	(HH)		0.863	1.581	3.428	0.014	0.021	0.030	SMC	1.0		
		(HL)		0.809	1.412	3.007	0.013	0.018	0.027	SDH	1.0		
	R → Q	(HL)		0.615	1.142	2.418	0.013	0.019	0.030	R	2.2		
		(HH)		0.228	0.411	0.772	0.015	0.022	0.034	S	2.4		
	S → Q	(HH)		0.245	0.379	0.710	0.015	0.022	0.033	D	1.0		
		(HL)		0.536	1.158	2.402	0.013	0.020	0.031				
	Set up time		SIN		1.350		4.560						
	Set up time		SMC		1.390		4.880						
	Set up time		SDH		1.170		4.070						
	Set up time		D		1.350		4.550						
	Hold time		SIN		0.080		0.000						
	Hold time		SMC		0.080		0.000						
	Hold time		SDH		0.260		0.000						
	Hold time		D		0.090		0.000						
	Release time		R		0.680		2.100						
	Release time		S		0.220		0.000						
Removal time		R		0.620		0.420							
Removal time		S		1.050		1.870							
Min Pulse		SCK		1.127		3.999							
Min Pulse		R		1.017		3.118							
Min Pulse		S		0.986		3.057							

### Chapter 3 Scan Path Block

Function	Scan D-F/F with Hold, 2 to 1 Selector																																														
Block type	Standard type																																														
	Normal				Q output				QB output																																						
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																			
x1	S052	14																																													
x2																																															
x4																																															
x8																																															
Logic Diagram for "Normal"				Truth Table for "Normal"																																											
				<table border="1"> <thead> <tr> <th>SIN</th> <th>SCK</th> <th>SMC</th> <th>SDH</th> <th>D</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>/</td> <td>X</td> <td>1</td> <td>X</td> <td>Hold</td> <td></td> </tr> <tr> <td>A</td> <td>/</td> <td>0</td> <td>0</td> <td>X</td> <td>A</td> <td>AB</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>0</td> <td>B</td> <td>B</td> <td>BB</td> </tr> <tr> <td>X</td> <td>\</td> <td>X</td> <td>X</td> <td>X</td> <td>Hold</td> <td></td> </tr> </tbody> </table> <p>X:Irrelevant</p>									SIN	SCK	SMC	SDH	D	Q	QB	X	/	X	1	X	Hold		A	/	0	0	X	A	AB	X	/	1	0	B	B	BB	X	\	X	X	X	Hold	
SIN	SCK	SMC	SDH	D	Q	QB																																									
X	/	X	1	X	Hold																																										
A	/	0	0	X	A	AB																																									
X	/	1	0	B	B	BB																																									
X	\	X	X	X	Hold																																										
Logic Diagram for "Q output"				Truth Table for "Q output"																																											
Logic Diagram for "QB output"				Truth Table for "QB output"																																											

### Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S052	SCK	→	Q (HH)	0.489	0.821	1.685	0.015	0.022	0.033	SIN	1.0	Q	22
			(HL)	0.575	1.005	2.102	0.012	0.017	0.026	SCK	1.0	QB	22
	SCK	→	QB (HH)	0.716	1.271	2.724	0.015	0.021	0.031	SMC	1.0		
			(HL)	0.669	1.140	2.386	0.012	0.016	0.023	SDH	1.0		
	Set up time		SIN	1.270		3.530				D	1.0		
	Set up time		SMC	1.310		3.860							
	Set up time		SDH	1.080		3.040							
	Set up time		D	1.260		3.530							
	Hold time		SIN	0.080		0.000							
	Hold time		SMC	0.070		0.000							
	Hold time		SDH	0.260		0.000							
	Hold time		D	0.080		0.000							
	Min Pulse		SCK	0.978		3.293							

Chapter 3 Scan Path Block

Function	Scan JK-F/F with R, S, D-F/F Function																																																																																																			
Block type	Standard type																																																																																																			
	Normal				Q output				QB output																																																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																								
x1	S100	14																																																																																																		
x2																																																																																																				
x4																																																																																																				
x8																																																																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																																																
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SIN	SCK	SMC	S	R	J	K	Qn	QBn	Qn+1	QBn+1																																																																																										
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Logic Diagram for "Q output"				Truth Table for "Q output"																																																																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S100	SCK	→	Q	(HH)	0.472	0.804	1.680	0.015	0.022	0.032	SIN	1.0	Q	22
				(HL)	0.626	1.117	2.381	0.012	0.018	0.028	SCK	1.0	QB	21
	SCK	→	QB	(HH)	0.846	1.539	3.333	0.015	0.021	0.030	SMC	1.0		
				(HL)	0.893	1.564	3.293	0.014	0.020	0.031	S	2.2		
	S	→	Q	(HH)	0.209	0.325	0.610	0.015	0.022	0.032	R	2.1		
				(HL)	0.629	1.337	2.750	0.014	0.022	0.035	J	1.0		
	R	→	Q	(HL)	0.537	1.097	2.346	0.012	0.017	0.027	K	1.0		
				(HH)	0.286	0.505	0.948	0.015	0.023	0.035				
	Set up time		SIN		1.060		3.440							
	Set up time		SMC		1.170		4.130							
	Set up time		J		1.240		4.150							
	Set up time		K		1.160		3.190							
	Hold time		SIN		0.370		0.000							
	Hold time		SMC		0.360		0.000							
	Hold time		J		0.070		0.000							
	Hold time		K		0.080		0.000							
	Release time		S		0.220		0.000							
	Release time		R		0.670		2.090							
	Removal time		S		1.050		1.860							
	Removal time		R		0.620		0.420							
	Min Pulse		SCK		1.190		3.904							
Min Pulse		S		1.021		3.335								
Min Pulse		R		1.064		3.105								

Chapter 3 Scan Path Block

Function	Scan JK-F/F with D-F/F Function																																																								
Block type	Standard type																																																								
	Normal				Q output				QB output																																																
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																													
x1	S102	12																																																							
x2																																																									
x4																																																									
x8																																																									
Logic Diagram for "Normal"				Truth Table for "Normal"																																																					
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SIN	SCK	SMC	J	K	Qn	QBn	Qn+1	QBn+1																																																	
A	/	0	X	X	X	X	A	AB																																																	
X	/	1	B	X	0	1	B	BB																																																	
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X	\	X	X	X	X	X	Hold	Hold																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																					
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Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S102	SCK	→	Q (HH)	0.451	0.757	1.564	0.015	0.022	0.032	SIN	1.0	Q	22
			(HL)	0.529	0.923	1.951	0.012	0.016	0.024	SCK	1.0	QB	22
	SCK	→	QB (HH)	0.716	1.268	2.716	0.015	0.022	0.031	SMC	1.0		
			(HL)	0.697	1.191	2.482	0.012	0.017	0.025	J	1.0		
	Set up time		SIN	1.010		2.450				K	1.0		
	Set up time		SMC	1.080		3.130							
	Set up time		J	1.270		3.150							
	Set up time		K	1.170		3.060							
	Hold time		SIN	0.350		0.000							
	Hold time		SMC	0.350		0.000							
	Hold time		J	0.130		0.000							
	Hold time		K	0.080		0.000							
	Min Pulse		SCK	0.981		3.286							

Chapter 3 Scan Path Block

Function	Scan JK-F/F with R, S, Hold, D-F/F Function																																																																																																																							
Block type	Standard type																																																																																																																							
	Normal				Q output				QB output																																																																																																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																																																																												
x1	S150	18																																																																																																																						
x2																																																																																																																								
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																																																																																				
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SIN	SCK	SMC	SDH	S	R	J	K	Qn	QBn	Qn+1	QBn+1																																																																																																													
X	/	X	1	0	0	X	X	X	X	Hold																																																																																																														
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Logic Diagram for "Q output"				Truth Table for "Q output"																																																																																																																				
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																																																																				

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S150	SCK → Q	(HH)		0.472	0.805	1.679	0.015	0.022	0.032	SIN	1.0	Q	22
		(HL)		0.629	1.120	2.386	0.012	0.018	0.028	SCK	1.0	QB	21
	SCK → QB	(HH)		0.874	1.590	3.435	0.015	0.021	0.031	SMC	1.0		
		(HL)		0.948	1.669	3.503	0.015	0.021	0.034	SDH	1.0		
	R → Q	(HL)		0.539	1.143	2.449	0.012	0.017	0.027	R	2.2		
		(HH)		0.308	0.545	1.026	0.015	0.023	0.035	S	2.3		
	S → Q	(HH)		0.209	0.325	0.610	0.015	0.022	0.032	J	1.0		
		(HL)		0.683	1.443	2.966	0.015	0.023	0.037	K	1.0		
	Set up time		SIN		1.320		4.520						
	Set up time		SMC		1.390		4.980						
	Set up time		SDH		1.070		3.710						
	Set up time		J		1.470		4.970						
	Set up time		K		1.450		4.320						
	Hold time		SIN		0.070		0.000						
	Hold time		SMC		0.040		0.000						
	Hold time		SDH		0.350		0.000						
	Hold time		J		0.000		0.000						
	Hold time		K		0.000		0.000						
	Release time		R		0.670		2.100						
	Release time		S		0.220		0.000						
Removal time		R		0.620		0.420							
Removal time		S		1.040		1.850							
Min Pulse		SCK		1.246		4.089							
Min Pulse		R		1.112		3.228							
Min Pulse		S		1.075		3.550							



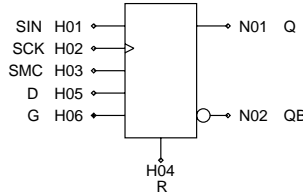
Chapter 3 Scan Path Block

Function	Scan JK-F/F with Hold, D-F/F Function																																																																							
Block type	Standard type																																																																							
	Normal				Q output				QB output																																																															
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																												
x1	S152	16																																																																						
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x4																																																																								
x8																																																																								
Logic Diagram for "Normal"				Truth Table for "Normal"																																																																				
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SIN	SCK	SMC	SDH	J	K	Qn	QBn	Qn+1	QBn+1																																																															
X	/	X	1	X	X	X	X	A	Hold																																																															
A	/	0	0	X	X	X	X	B	AB																																																															
X	/	1	0	B	X	0	1	B	BB																																																															
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X	\	X	X	X	X	X	X	X	Hold																																																															
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																				
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																				

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
S152	SCK	→	Q (HH)	0.451	0.757	1.563	0.015	0.022	0.032	SIN	1.0	Q	22
			(HL)	0.530	0.926	1.954	0.012	0.016	0.024	SCK	1.0	QB	21
	SCK	→	QB (HH)	0.746	1.318	2.813	0.015	0.022	0.032	SMC	1.0		
			(HL)	0.734	1.259	2.611	0.013	0.018	0.027	SDH	1.0		
	Set up time		SIN	1.300		3.610				J	1.0		
	Set up time		SMC	1.330		3.970				K	1.0		
	Set up time		SDH	1.020		2.700							
	Set up time		J	1.480		4.030							
	Set up time		K	1.450		4.230							
	Hold time		SIN	0.060		0.000							
	Hold time		SMC	0.030		0.000							
	Hold time		SDH	0.340		0.000							
	Hold time		J	0.000		0.000							
	Hold time		K	0.000		0.000							
Min Pulse		SCK	1.020		3.384								

Chapter 3 Scan Path Block

Function	Scan D-Latch with R, D-F/F Function																																																																			
Block type	Standard type																																																																			
	Normal				Q output				QB output																																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																								
x1	S201	13																																																																		
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Logic Diagram for "Normal"				Truth Table for "Normal"																																																																
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SIN	SCK	SMC	R	D	G	Q	QB																																																													
X	X	X	1	X	X	0	1																																																													
A	/	0	0	X	X	A	AB																																																													
X	\	0	0	X	X		Hold																																																													
X	X	1	0	B	1	B	BB																																																													
X	X	1	0	X	0		Latch																																																													
X	1	Down	0	1	1	X	X																																																													
Logic Diagram for "Q output"				Truth Table for "Q output"																																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S201	SCK → Q	(HH)		0.964	1.736	3.861	0.014	0.021	0.029	SIN	1.0	Q	22
		(HL)		0.804	1.388	2.995	0.012	0.016	0.023	SCK	1.0	QB	22
	SCK → QB	(HH)		0.622	1.069	2.301	0.015	0.022	0.032	SMC	1.0		
		(HL)		0.803	1.429	3.137	0.013	0.018	0.028	R	2.1		
	R → Q	(HL)		0.474	0.788	1.581	0.012	0.017	0.026	D	1.0		
		(HH)		0.214	0.331	0.620	0.015	0.022	0.032	G	1.0		
	R → QB	(HH)		0.838	1.471	3.262	0.014	0.021	0.029				
		(LL)		0.779	1.421	3.129	0.012	0.016	0.023				
	D → Q	(HL)		0.676	1.163	2.537	0.013	0.018	0.028				
		(LH)		0.596	1.099	2.428	0.015	0.022	0.032				
	G → Q	(HH)		0.958	1.733	3.858	0.014	0.021	0.029				
		(HL)		0.801	1.386	3.003	0.012	0.016	0.023				
	G → QB	(HH)		0.619	1.067	2.308	0.015	0.022	0.032				
		(HL)		0.797	1.426	3.134	0.013	0.018	0.028				
	Set up time	SIN		0.970		3.250							
	Set up time	SMC		1.270		2.790							
	Set up time	D		0.920		2.000							
	Hold time	SIN		0.600		0.620							
	Hold time	SMC		0.000		0.000							
	Hold time	D		0.370		0.000							
Release time	R		0.570		1.320								
Removal time	R		0.790		1.270								
Min Pulse	SCK		1.342		4.510								
Min Pulse	R		0.732		2.188								
Min Pulse	G		1.329		4.501								

Chapter 3 Scan Path Block

Function	Scan D-Latch with D-F/F Function																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
Drivability																																																						
x1	S202	12																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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SIN	SCK	SMC	D	G	Q	QB																																																
A	/	0	X	X	A	AB																																																
X	\	0	X	X		Hold																																																
X	X	1	B	1	B	BB																																																
X	X	1	X	0		Latch																																																
X	1	Down	1	1	X	X																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S202	SCK	→	Q	(HH)	0.833	1.476	3.269	0.015	0.021	0.030	SIN	1.0	Q	22
				(HL)	0.783	1.350	2.932	0.012	0.016	0.023		SCK	1.0	QB
	SCK	→	QB	(HH)	0.608	1.041	2.253	0.015	0.022	0.032	SMC	1.0		
				(HL)	0.699	1.225	2.683	0.012	0.016	0.024		D	1.0	
	D	→	Q	(HH)	0.699	1.199	2.653	0.015	0.021	0.030	G	1.0		
				(LL)	0.775	1.401	3.085	0.012	0.016	0.023				
	D	→	QB	(HL)	0.564	0.946	2.065	0.012	0.016	0.024				
				(LH)	0.598	1.089	2.399	0.015	0.022	0.032				
	G	→	Q	(HH)	0.827	1.472	3.266	0.015	0.021	0.030				
				(HL)	0.785	1.354	2.950	0.012	0.016	0.023				
	G	→	QB	(HH)	0.610	1.045	2.270	0.015	0.022	0.032				
				(HL)	0.693	1.221	2.680	0.012	0.016	0.024				
		Set up time		SIN	0.990		3.180							
		Set up time		SMC	1.270		2.780							
		Set up time		D	0.930		1.980							
		Hold time		SIN	0.620		0.670							
		Hold time		SMC	0.020		0.000							
	Hold time		D	0.490		0.360								
	Min Pulse		SCK	1.214		3.918								
	Min Pulse		G	1.200		3.909								

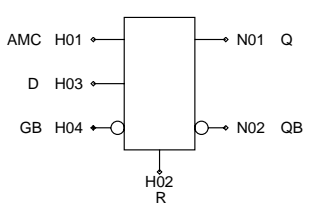
Chapter 3 Scan Path Block

Function	Scan D-Latch with D-F/F Function, High Speed																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	S204	12																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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SIN	SCK	SMC	D	G	Q	QB																																																
A	/	0	X	X	A	AB																																																
X	\	0	X	X		Hold																																																
X	X	1	B	1	B	BB																																																
X	X	1	X	0		Latch																																																
X	1	Down	1	1	X	X																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S204	SCK	→	Q	(HH)	0.607	1.062	2.345	0.016	0.024	0.038	SIN	1.0	Q	19
				(HL)	0.596	1.074	2.291	0.015	0.021	0.034	SCK	1.0	QB	22
	SCK	→	QB	(HH)	0.752	1.403	3.084	0.014	0.021	0.028	SMC	1.0		
				(HL)	0.786	1.405	3.140	0.011	0.015	0.023	D	1.0		
	D	→	Q	(HH)	0.472	0.793	1.755	0.016	0.024	0.038	G	1.0		
				(LL)	0.532	1.012	2.280	0.016	0.022	0.035				
	D	→	QB	(HL)	0.653	1.138	2.556	0.011	0.015	0.023				
				(LH)	0.703	1.367	3.099	0.014	0.020	0.028				
	G	→	Q	(HH)	0.600	1.057	2.339	0.016	0.024	0.038				
				(HL)	0.599	1.083	2.318	0.015	0.021	0.034				
	G	→	QB	(HH)	0.757	1.415	3.114	0.014	0.021	0.028				
				(HL)	0.780	1.400	3.134	0.011	0.015	0.023				
		Set up time		SIN	0.810		3.260							
		Set up time		SMC	1.310		3.390							
		Set up time		D	1.010		2.560							
		Hold time		SIN	0.620		0.680							
	Hold time		SMC	0.020		0.000								
	Hold time		D	0.500		0.270								
	Min Pulse		SCK	1.168		3.790								
	Min Pulse		G	1.154		3.778								

Chapter 3 Scan Path Block

Function	Scan D-Latch with R, Special Function																																																																	
Block type	Standard type																																																																	
	Normal				Q output				QB output																																																									
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																																						
Drivability																																																																		
x1	S301	8																																																																
x2																																																																		
x4																																																																		
x8																																																																		
Logic Diagram for "Normal"				Truth Table for "Normal"																																																														
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AMC	R	D	GB	Q	QB																																																													
1	0	0	0	0	1																																																													
1	0	1	0	1	0																																																													
1	0	X	1	Latch																																																														
X	1	X	X	0	1																																																													
0	0	0	0	0	1																																																													
0	0	0	1	0	1																																																													
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0	0	1	1	1	0																																																													
Logic Diagram for "Q output"				Truth Table for "Q output"																																																														
Logic Diagram for "QB output"				Truth Table for "QB output"																																																														

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S301	AMC → Q	(HH)		0.755	1.349	3.082	0.014	0.021	0.029	AMC	1.8	Q	22
		(LH)		0.754	1.394	3.075	0.014	0.021	0.029				
	AMC → QB	(HL)		0.592	1.038	2.352	0.013	0.018	0.028	R	1.0	QB	22
		(LH)		0.670	1.138	2.477	0.015	0.022	0.032				
	R → Q	(LL)		0.590	1.082	2.346	0.013	0.018	0.028	D	1.0		
		(HL)		0.396	0.650	1.308	0.012	0.016	0.023				
	R → QB	(HH)		0.212	0.330	0.619	0.015	0.022	0.032	GB	1.9		
		(LL)		0.311	0.591	1.267	0.013	0.018	0.028				
	D → Q	(HH)		0.755	1.340	3.023	0.014	0.021	0.029				
		(LL)		0.595	1.054	2.273	0.012	0.016	0.023				
	D → QB	(HL)		0.591	1.029	2.294	0.013	0.018	0.028				
		(LH)		0.411	0.733	1.578	0.015	0.022	0.032				
	GB → Q	(HH)		0.804	1.443	3.292	0.014	0.021	0.029				
		(LH)		0.765	1.392	3.056	0.014	0.021	0.029				
	GB → QB	(LL)		0.637	1.572	3.366	0.012	0.016	0.023				
		(HL)		0.640	1.132	2.562	0.013	0.018	0.028				
		(LH)		0.455	1.244	2.654	0.015	0.022	0.032				
		(LL)		0.602	1.082	2.327	0.013	0.018	0.028				
		Set up time	D		0.990	2.080							
		Hold time	D		0.470	0.120							
		Release time	R		0.640	0.910							
		Removal time	R		0.570	0.320							
	Min Pulse	R		0.743	2.271								
	Min Pulse	GB		1.162	3.847								

Chapter 3 Scan Path Block

Function	Scan D-Latch with Special Function																																																			
Block type	Standard type																																																			
	Normal				Q output				QB output																																											
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																								
Drivability																																																				
x1	S302	7																																																		
x2																																																				
x4																																																				
x8																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																
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AMC	D	GB	Q	QB																																																
1	0	0	0	1																																																
1	1	0	1	0																																																
1	X	1	Latch																																																	
0	0	0	0	1																																																
0	0	1	0	1																																																
0	1	0	0	1																																																
0	1	1	1	0																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output						
	Path			t LDO (ns)			t 1										
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout				
S302	AMC	→ Q	(HH)	0.626	1.092	2.496	0.015	0.021	0.030	AMC	1.8	Q	22				
			(LH)	0.625	1.133	2.483	0.015	0.021	0.030								
		(LL)	0.861	1.453	3.159	0.012	0.016	0.023									
	AMC	→ QB	(HL)	0.486	0.834	1.899	0.012	0.016	0.024					D	1.0	QB	22
			(LH)	0.678	1.133	2.460	0.015	0.022	0.032								
		(LL)	0.485	0.874	1.886	0.012	0.016	0.024									
	D	→ Q	(HH)	0.626	1.083	2.437	0.015	0.021	0.030	GB	1.9						
			(LH)	0.591	1.039	2.245	0.012	0.016	0.023								
		(LL)	0.486	0.824	1.841	0.012	0.016	0.024									
	D	→ QB	(HL)	0.410	0.722	1.557	0.015	0.022	0.032								
			(LH)	0.673	1.185	2.706	0.015	0.021	0.030								
		(LL)	0.637	1.133	2.464	0.015	0.021	0.030									
	GB	→ Q	(HH)	0.673	1.185	2.706	0.015	0.021	0.030								
			(LH)	0.637	1.133	2.464	0.015	0.021	0.030								
		(LL)	0.632	1.562	3.343	0.012	0.016	0.023									
	GB	→ QB	(HL)	0.533	0.926	2.108	0.012	0.016	0.024								
			(LH)	0.452	1.238	2.637	0.015	0.022	0.032								
		(LL)	0.497	0.875	1.869	0.012	0.016	0.024									
Set up time		D	0.910		1.700												
Hold time		D	0.460		0.120												
Min Pulse		GB	1.167		3.823												

Chapter 3 Scan Path Block

Function	Scan D-Latch with Special Function, High Speed																																																			
Block type	Standard type																																																			
	Normal				Q output				QB output																																											
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																								
x1	S303	7																																																		
x2																																																				
x4																																																				
x8																																																				
Logic Diagram for "Normal"				Truth Table for "Normal"																																																
				<table border="1"> <thead> <tr> <th>AMC</th> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									AMC	D	GB	Q	QB	1	0	0	0	1	1	1	0	1	0	1	X	1	Latch		0	0	0	0	1	0	0	1	0	1	0	1	0	0	1	0	1	1	1	0
AMC	D	GB	Q	QB																																																
1	0	0	0	1																																																
1	1	0	1	0																																																
1	X	1	Latch																																																	
0	0	0	0	1																																																
0	0	1	0	1																																																
0	1	0	0	1																																																
0	1	1	1	0																																																
Logic Diagram for "Q output"				Truth Table for "Q output"																																																
Logic Diagram for "QB output"				Truth Table for "QB output"																																																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output			
	Path			t LDO (ns)			t 1							
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout	
S303	AMC	→ Q	(HH)	0.399	0.686	1.602	0.016	0.024	0.037	AMC	1.8	Q	19	
			(LH)	0.404	0.740	1.620	0.016	0.024	0.038					
		(LL)	0.643	1.102	2.404	0.016	0.022	0.034						
	AMC	→ QB	(HL)	0.575	1.024	2.390	0.011	0.015	0.023	D	1.0	QB	21	
			(LH)	0.816	1.449	3.212	0.014	0.020	0.028					
		(LL)	0.582	1.080	2.414	0.011	0.015	0.023						
	D	→ Q	(HH)	0.398	0.676	1.543	0.016	0.024	0.037	GB	1.9			
			(LH)	0.352	0.637	1.372	0.013	0.019	0.029					
	D	→ QB	(HL)	0.575	1.014	2.331	0.011	0.015	0.023					
			(LH)	0.495	0.926	2.048	0.014	0.021	0.030					
	GB	→ Q	(HH)	0.447	0.782	1.818	0.016	0.024	0.037					
			(LH)	0.417	0.740	1.607	0.016	0.024	0.037					
	GB	→ QB	(LL)	0.408	1.189	2.566	0.014	0.022	0.034					
			(HL)	0.625	1.124	2.613	0.011	0.015	0.023					
				(LH)	0.528	1.558	3.403	0.014	0.021	0.030				
				(LL)	0.593	1.078	2.395	0.011	0.015	0.023				
		Set up time	D		0.980		2.070							
		Hold time	D		0.450		0.070							
		Min Pulse	GB		1.132		3.892							

[MEMO]

[MEMO]



## 3.2 NEC Scan

[MEMO]

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch																											
Block type	Standard type																											
	Normal				Q output				QB output																			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Drivability																												
x1	SE601	13																										
x2																												
x4																												
x8																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>0</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	Q	QB	0	1	0	1	1	1	1	0	X	0	Latch	
D	G	Q	QB																									
0	1	0	1																									
1	1	1	0																									
X	0	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SE601	D	→	Q (HH)	0.794	1.425	3.117	0.014	0.021	0.030	D	1.0	Q	22	
			(LL)	0.788	1.404	3.071	0.012	0.016	0.024					
	D	→	QB (HL)	0.610	1.059	2.289	0.014	0.019	0.030	G	2.0	QB	20	
			(LH)	0.585	1.018	2.208	0.015	0.023	0.035					
	G	→	Q (HH)	0.609	1.134	2.511	0.014	0.021	0.030					
			(HL)	0.628	1.126	2.507	0.012	0.016	0.024					
	G	→	QB (HH)	0.427	0.744	1.657	0.015	0.023	0.035					
			(HL)	0.435	0.785	1.708	0.013	0.019	0.030					
		Set up time	D											
		Hold time	D											
	Min Pulse	G												

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch with R																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
x1	SE602	14																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>R</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>0</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	R	Q	QB	1	1	0	1	0	0	1	0	0	1	X	0	0	Latch		X	X	1	0	1
D	G	R	Q	QB																																	
1	1	0	1	0																																	
0	1	0	0	1																																	
X	0	0	Latch																																		
X	X	1	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE602	D → Q	(HH)		0.998	1.839	4.088	0.014	0.020	0.028	D	1.0	Q	21
				0.782	1.403	3.074	0.012	0.016	0.024				
	D → QB	(HL)		0.793	1.412	3.114	0.015	0.023	0.035	G	1.9	QB	20
				0.580	1.018	2.215	0.015	0.023	0.035				
	G → Q	(HH)		0.636	1.224	2.775	0.014	0.021	0.029	R	2.4		
				0.625	1.121	2.495	0.012	0.016	0.024				
	G → QB	(HH)		0.425	0.741	1.649	0.015	0.023	0.035				
				0.449	0.832	1.858	0.015	0.021	0.034				
	R → Q	(HL)		0.522	0.954	2.047	0.012	0.016	0.023				
				0.787	1.540	3.471	0.014	0.020	0.028				
	R → QB	(HH)		0.330	0.587	1.214	0.015	0.023	0.035				
				0.582	1.113	2.497	0.015	0.023	0.035				
	Set up time	D		1.480		4.050							
	Hold time	D		0.110		0.000							
	Release time	R		1.220		3.340							
	Removal time	R		0.000		0.000							
Min Pulse	G		1.076		3.533								
Min Pulse	R		1.097		3.873								

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch with RB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Drivability																																					
x1	SE603	14																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>G</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	G	RB	Q	QB	1	1	1	1	0	0	1	1	0	1	X	0	1	Latch		X	X	0	0	1
D	G	RB	Q	QB																																	
1	1	1	1	0																																	
0	1	1	0	1																																	
X	0	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
SE603	D	→	Q	(HH)	0.769	1.345	2.969	0.015	0.023	0.035	D	1.0	Q	20	
				(LL)	0.714	1.253	2.707	0.012	0.016	0.025					
	D	→	QB	(HL)	0.976	1.713	3.798	0.012	0.016	0.023					
				(LH)	0.866	1.534	3.352	0.015	0.021	0.030	G	1.9	QB	21	
	G	→	Q	(HH)	0.565	1.005	2.273	0.015	0.023	0.035					
				(HL)	0.559	0.987	2.169	0.012	0.016	0.025					
	G	→	QB	(HH)	0.710	1.267	2.812	0.015	0.021	0.030					
				(HL)	0.772	1.373	3.101	0.012	0.016	0.023	RB	2.5			
	RB	→	Q	(HH)	0.270	0.478	1.215	0.015	0.023	0.035					
				(LL)	0.271	0.458	0.907	0.012	0.016	0.025					
	RB	→	QB	(HL)	0.477	0.845	2.044	0.012	0.016	0.023					
				(LH)	0.426	0.839	1.747	0.015	0.022	0.032					
	Set up time	D			1.250		2.880								
	Hold time	D			0.140		0.000								
	Release time	RB			0.680		0.860								
	Removal time	RB			0.550		0.450								
Min Pulse	G			1.185		3.744									
Min Pulse	RB			0.793		2.315									

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch(GB)																											
Block type	Standard type																											
	Normal				Q output				QB output																			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Drivability																												
x1	SE604	13																										
x2																												
x4																												
x8																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td colspan="2">Latch</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	Q	QB	1	0	1	0	0	0	0	1	X	1	Latch	
D	GB	Q	QB																									
1	0	1	0																									
0	0	0	1																									
X	1	Latch																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SE604	D → Q	(HH)		0.791	1.418	3.103	0.014	0.021	0.030	D	1.0	Q	22
		(LL)		0.790	1.409	3.086	0.012	0.016	0.024				
	D → QB	(HL)		0.608	1.051	2.273	0.014	0.019	0.030	GB	2.0	QB	20
		(LH)		0.587	1.023	2.222	0.015	0.023	0.035				
	GB → Q	(LH)		0.668	1.283	2.842	0.014	0.021	0.030				
		(LL)		0.651	1.207	2.666	0.012	0.016	0.024				
	GB → QB	(LH)		0.449	0.823	1.808	0.015	0.023	0.035				
		(LL)		0.491	0.935	2.040	0.013	0.019	0.029				
	Set up time		D		1.200		2.920						
	Hold time		D		0.020		0.000						
Min Pulse		GB		1.108		3.512							

Chapter 3 Scan Path Block

Function	NEC Scan D-Latch(GB) with RB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
x1	SE605	14																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>GB</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td colspan="2">Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	GB	RB	Q	QB	1	0	1	1	0	0	0	1	0	1	X	1	1	Latch		X	X	0	0	1
D	GB	RB	Q	QB																																	
1	0	1	1	0																																	
0	0	1	0	1																																	
X	1	1	Latch																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output							
	Path			t LDO (ns)			t 1											
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout					
SE605	D	→	Q	(HH)	0.768	1.342	2.961	0.015	0.023	0.035	D	1.0	Q	20				
				(LL)	0.714	1.254	2.713	0.012	0.016	0.025					GB	1.9	QB	21
	D	→	QB	(HL)	0.974	1.711	3.791	0.012	0.016	0.023					RB	2.5		
				(LH)	0.866	1.535	3.359	0.015	0.021	0.030								
	GB	→	Q	(LH)	0.642	1.204	2.721	0.015	0.023	0.035								
				(LL)	0.570	1.033	2.232	0.012	0.016	0.025								
	GB	→	QB	(LH)	0.722	1.314	2.877	0.015	0.021	0.030								
				(LL)	0.849	1.571	3.549	0.012	0.016	0.023								
	RB	→	Q	(HH)	0.270	0.478	1.213	0.015	0.023	0.035								
				(LL)	0.272	0.457	0.907	0.012	0.016	0.025								
	RB	→	QB	(HL)	0.477	0.845	2.042	0.012	0.016	0.023								
				(LH)	0.426	0.838	1.747	0.015	0.022	0.032								
	Set up time	D			1.170		2.740											
	Hold time	D			0.080		0.000											
Release time	RB			0.630		0.810												
Removal time	RB			0.590		0.500												
Min Pulse	GB			1.246		4.083												
Min Pulse	RB			0.792		2.315												

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F																											
Block type	Standard type																											
	Normal				Q output				QB output																			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Drivability																												
x1	SE611	11																										
x2																												
x4																												
x8																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↘</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	C	Q	QB	0	↗	0	1	1	↘	1	0	X	↘	Hold	
D	C	Q	QB																									
0	↗	0	1																									
1	↘	1	0																									
X	↘	Hold																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SE611	C → Q	(HH)		0.484	0.824	1.788	0.015	0.022	0.032	D	1.0	Q	22
		(HL)		0.536	0.936	2.055	0.012	0.016	0.024	C	2.3	QB	22
	C → QB	(HH)		0.692	1.228	2.722	0.015	0.021	0.031				
		(HL)		0.690	1.191	2.581	0.012	0.016	0.024				
	Set up time		D		0.880	1.870							
	Hold time		D		0.430	0.270							
Min Pulse		C		1.151	3.472								

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with R, S																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	SE614	13																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>R</th> <th>S</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↘</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td>0</td> <td>0</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>← Prohibition</p> <p>X: Irrelevant</p>									D	C	R	S	Q	QB	0	↗	0	0	0	1	1	↘	0	0	1	0	X	↘	0	0	Hold		X	X	0	1	1	0	X	X	1	0	0	1	X	X	1	1	1	1
D	C	R	S	Q	QB																																																	
0	↗	0	0	0	1																																																	
1	↘	0	0	1	0																																																	
X	↘	0	0	Hold																																																		
X	X	0	1	1	0																																																	
X	X	1	0	0	1																																																	
X	X	1	1	1	1																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE614	C → Q	(HH)		0.494	0.857	1.879	0.015	0.022	0.032	D	1.0	Q	22
		(HL)		0.628	1.124	2.474	0.013	0.018	0.028	C	2.4	QB	21
	C → QB	(HH)		0.803	1.474	3.296	0.014	0.021	0.030	R	2.2		
		(HL)		0.834	1.478	3.241	0.013	0.018	0.028	S	2.4		
	R → Q	(HL)		0.539	1.039	2.245	0.012	0.017	0.027				
	R → QB	(HH)		0.250	0.448	0.846	0.015	0.022	0.034				
	S → Q	(HH)		0.209	0.325	0.611	0.015	0.022	0.032				
	S → QB	(HL)		0.547	1.196	2.494	0.013	0.020	0.032				
	Set up time	D		0.980		2.890							
	Hold time	D		0.450		0.270							
	Release time	R		0.720		2.170							
	Release time	S		0.370		0.580							
	Removal time	R		0.520		0.130							
	Removal time	S		0.900		1.480							
Min Pulse	C		1.313		4.110								
Min Pulse	R		0.984		2.969								
Min Pulse	S		1.010		3.327								



Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with RB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Drivability																																					
x1	SE615	12																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
				<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>RB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>↗</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>↗</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>↘</td> <td>1</td> <td colspan="2">Hold</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X: Irrelevant</p>									D	C	RB	Q	QB	0	↗	1	0	1	1	↗	1	1	0	X	↘	1	Hold		X	X	0	0	1
D	C	RB	Q	QB																																	
0	↗	1	0	1																																	
1	↗	1	1	0																																	
X	↘	1	Hold																																		
X	X	0	0	1																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SE615	C → Q	(HH)		0.554	0.970	2.166	0.015	0.022	0.034	D	1.0	Q	21
		(HL)		0.547	0.956	2.092	0.012	0.016	0.024	C	2.4	QB	21
	C → QB	(HH)		0.707	1.252	2.765	0.015	0.021	0.031	RB	2.5		
		(HL)		0.768	1.358	3.041	0.012	0.016	0.023				
	RB → Q	(LL)		0.246	0.407	0.800	0.012	0.016	0.024				
	RB → QB	(LH)		0.410	0.802	1.662	0.015	0.022	0.033				
	Set up time	D		0.920		2.060							
	Hold time	D		0.440		0.290							
	Release time	RB		0.490		0.500							
	Removal time	RB		0.760		1.120							
	Min Pulse	C		1.218		3.823							
	Min Pulse	RB		0.777		2.334							

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with SB																																				
Block type	Standard type																																				
	Normal				Q output				QB output																												
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																									
Drivability																																					
x1	SE616	12																																			
x2																																					
x4																																					
x8																																					
Logic Diagram for "Normal"				Truth Table for "Normal"																																	
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D	C	SB	Q	QB																																	
0	↗	1	0	1																																	
1	↗	1	1	0																																	
X	↘	1	Hold																																		
X	X	0	1	0																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																	
Logic Diagram for "QB output"				Truth Table for "QB output"																																	

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SE616	C → Q	(HH)		0.488	0.830	1.796	0.015	0.022	0.032	D	1.0	Q	22
		(HL)		0.562	0.992	2.199	0.012	0.016	0.024	C	2.4	QB	21
	C → QB	(HH)		0.799	1.451	3.316	0.015	0.022	0.033	SB	2.3		
		(HL)		0.694	1.199	2.600	0.012	0.016	0.024				
	SB → Q	(LH)		0.485	1.007	2.183	0.015	0.022	0.032				
	SB → QB	(LL)		0.290	0.593	1.159	0.012	0.017	0.028				
	Set up time		D	0.950		2.290							
	Hold time		D	0.400		0.250							
	Release time		SB	0.680		1.240							
	Removal time		SB	0.560		0.460							
	Min Pulse		C	1.221		4.105							
	Min Pulse		SB	0.878		2.767							

### Chapter 3 Scan Path Block

Function	NEC Scan D-F/F with RB, SB																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	SE617	13																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
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D	C	RB	SB	Q	QB																																																	
0	/	1	1	0	1																																																	
1	/	1	1	1	0																																																	
X	\	1	1	Hold																																																		
X	X	0	1	0	1																																																	
X	X	1	0	1	0																																																	
X	X	0	0	0	0																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

### Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE617	C → Q	(HH)		0.536	0.944	2.125	0.015	0.022	0.034	D	1.0	Q	21
		(HL)		0.554	0.981	2.189	0.012	0.016	0.024	C	2.4	QB	19
	C → QB	(HH)		0.789	1.440	3.307	0.015	0.022	0.033	RB	2.3		
		(HL)		0.752	1.338	3.015	0.012	0.016	0.023	SB	2.2		
	RB → Q	(LL)		0.240	0.398	0.786	0.012	0.016	0.024				
	RB → QB	(LH)		0.480	1.010	2.236	0.015	0.023	0.036				
	SB → Q	(LH)		0.537	1.137	2.534	0.015	0.022	0.033				
	SB → QB	(LL)		0.294	0.596	1.164	0.012	0.018	0.028				
	Set up time		D		0.940		2.240						
	Hold time		D		0.400		0.250						
	Release time		RB		0.460		0.470						
	Release time		SB		0.660		1.190						
	Removal time		RB		0.810		1.260						
	Removal time		SB		0.570		0.480						
Min Pulse		C		1.210		4.094							
Min Pulse		RB		0.888		2.955							
Min Pulse		SB		0.957		3.121							

Chapter 3 Scan Path Block

Function	NEC Scan D-F/F (CB)																											
Block type	Standard type																											
	Normal				Q output				QB output																			
	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																
Drivability																												
x1	SE631	11																										
x2																												
x4																												
x8																												
Logic Diagram for "Normal"				Truth Table for "Normal"																								
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td colspan="2">Hold</td> </tr> </tbody> </table> <p>X:Irrelevant</p>									D	CB	Q	QB	0	\	0	1	1	\	1	0	X	/	Hold	
D	CB	Q	QB																									
0	\	0	1																									
1	\	1	0																									
X	/	Hold																										
Logic Diagram for "Q output"				Truth Table for "Q output"																								
Logic Diagram for "QB output"				Truth Table for "QB output"																								

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SE631	CB	→	Q (LH)	0.553	1.016	2.226	0.015	0.022	0.032	D	1.0	Q	22
			(LL)	0.536	0.966	2.092	0.012	0.016	0.024			CB	2.3
	CB	→	QB (LH)	0.693	1.260	2.763	0.015	0.021	0.031				
			(LL)	0.759	1.382	3.019	0.012	0.016	0.024				
	Set up time		D				0.910		1.910				
	Hold time		D				0.460		0.520				
Min Pulse		CB				1.196		3.697					

### Chapter 3 Scan Path Block

Function	NEC Scan D-F/F (CB) with RB, SB																																																					
Block type	Standard type																																																					
	Normal				Q output				QB output																																													
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells																																										
x1	SE637	13																																																				
x2																																																						
x4																																																						
x8																																																						
Logic Diagram for "Normal"				Truth Table for "Normal"																																																		
				<table border="1"> <thead> <tr> <th>D</th> <th>CB</th> <th>RB</th> <th>SB</th> <th>Q</th> <th>QB</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>\</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>\</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>/</td> <td>1</td> <td>1</td> <td>Hold</td> <td></td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>X</td> <td>X</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p>X: Irrelevant ← Prohibition</p>									D	CB	RB	SB	Q	QB	0	\	1	1	0	1	1	\	1	1	1	0	X	/	1	1	Hold		X	X	0	1	0	1	X	X	1	0	1	0	X	X	0	0	0	0
D	CB	RB	SB	Q	QB																																																	
0	\	1	1	0	1																																																	
1	\	1	1	1	0																																																	
X	/	1	1	Hold																																																		
X	X	0	1	0	1																																																	
X	X	1	0	1	0																																																	
X	X	0	0	0	0																																																	
Logic Diagram for "Q output"				Truth Table for "Q output"																																																		
Logic Diagram for "QB output"				Truth Table for "QB output"																																																		

### Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SE637	CB	→	Q (LH)	0.601	1.126	2.547	0.015	0.022	0.034	D	1.0	Q	21
			(LL)	0.551	1.005	2.212	0.012	0.016	0.024	CB	2.4	QB	19
	CB	→	QB (LH)	0.788	1.466	3.334	0.015	0.022	0.033	RB	2.3		
			(LL)	0.816	1.519	3.433	0.012	0.016	0.023	SB	2.2		
	RB	→	Q (LL)	0.240	0.398	0.786	0.012	0.016	0.024				
	RB	→	QB (LH)	0.480	1.009	2.234	0.015	0.023	0.036				
	SB	→	Q (LH)	0.535	1.137	2.534	0.015	0.022	0.033				
	SB	→	QB (LL)	0.293	0.596	1.164	0.012	0.018	0.028				
	Set up time		D	0.970		2.390							
	Hold time		D	0.480		0.530							
	Release time		RB	0.460		0.400							
	Release time		SB	0.680		1.350							
	Removal time		RB	0.810		1.550							
	Removal time		SB	0.570		0.510							
Min Pulse		CB	1.248		4.112								
Min Pulse		RB	0.888		2.955								
Min Pulse		SB	0.957		3.121								

[MEMO]

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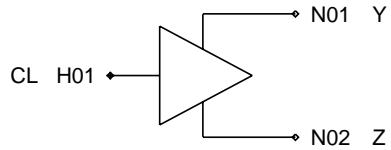
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### 3.3 Scan Controller

### Chapter 3 Scan Path Block

Function	Clock Distributor									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SCD1	8								
x2										
x4										
x8										

Logic Diagram



Truth Table

CL	Y	Z
1	1	1
0	0	0

Y: Must be connected to the clock of Negative edge triggered F/F or the gate of Low enable Latch  
 Z: Must be connected to the clock of Positive edge triggered F/F or the gate of High enable Latch

### Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SCD1	CL	→	Y (HH)	0.269	0.432	0.895	0.015	0.022	0.033	CL	2.1	Y	21
			(LL)	0.302	0.532	1.136	0.013	0.018	0.027			Z	21
	CL	→	Z (HH)	0.268	0.431	0.893	0.015	0.022	0.033				
			(LL)	0.301	0.531	1.134	0.013	0.018	0.027				



### Chapter 3 Scan Path Block

Function	Clock Distributor with Test (Positive Clock)										
Block type	Standard type										
	Normal		High speed								
Drivability	Name	cells	Name	cells							
x1	SCDC	2									
x2											
x4											
x8											

Logic Diagram

```

graph LR
    CL_H01[CL H01] --> Buffer[ ]
    Buffer --> N01_Y[N01 Y]
  
```

Truth Table

CL	Y
1	1
0	0

### Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SCDC	CL	→ Y	(HH) (LL)	0.170 0.265	0.270 0.462	0.504 0.969	0.015 0.012	0.022 0.017	0.031 0.025	CL	1.0	Y	22

Chapter 3 Scan Path Block

Function	Clock Distributor with Test (Negative Clock)										
Block type	Standard type										
	Normal		High speed								
Drivability	Name	cells	Name	cells							
x1	SCDD	2									
x2											
x4											
x8											

Logic Diagram

```

    graph LR
      CL_H01[CL H01] --> Buffer[ ]
      Buffer --> N01_Y[N01 Y]
  
```

Truth Table

CL	Y
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SCDD	CL	→	Y	(HH) 0.221	0.355	0.751	0.015	0.022	0.033	CL	1.0	Y	22
			(LL)	0.184	0.312	0.621	0.011	0.015	0.022				

Chapter 3 Scan Path Block

Function	I/F Control (AMC) with EN															
Block type	Standard type															
	Normal		High speed													
Drivability	Name	cells	Name	cells												
x1	SFEH	3														
x2																
x4																
x8																
<p>Logic Diagram</p> <pre> graph LR     D_H01[D H01] --&gt; Inverter[ ]     Inverter --&gt; N01_EN[N01 EN]     </pre>																
<p>Truth Table</p> <table border="1"> <thead> <tr> <th>D</th> <th>EN</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>											D	EN	1	1	0	0
D	EN															
1	1															
0	0															

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SFEH	D	→ EN	(HH) (LL)	0.221 0.184	0.355 0.313	0.751 0.621	0.015 0.011	0.022 0.015	0.033 0.022	D	1.0	EN	22

Chapter 3 Scan Path Block

Function	I/F Control (AMC) with ENB																
Block type	Standard type																
	Normal		High speed														
Drivability	Name	cells	Name	cells													
x1	SFEL	2															
x2																	
x4																	
x8																	
<p>Logic Diagram</p> <pre> graph LR     D_H01[D H01] --&gt; Inverter[ ]     Inverter --&gt; N01_ENB[N01 ENB]     </pre>																	
<p>Truth Table</p> <table border="1"> <thead> <tr> <th>D</th> <th>ENB</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> </tr> </tbody> </table>												D	ENB	1	1	0	0
D	ENB																
1	1																
0	0																

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SFEL	D → ENB		(HH)	0.170	0.270	0.504	0.015	0.022	0.031	D	1.0	ENB	22
			(LL)	0.265	0.462	0.969	0.012	0.017	0.025				

Chapter 3 Scan Path Block

Function	I/F Control (SMC) with EN									
Block type	Standard type									
	Normal			High speed						
Drivability	Name	cells	Name	cells						
x1	SOEH	3								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    D_H01[D H01] --> Inverter[ ]
    Inverter --> N01_EN[N01 EN]
  
```

Truth Table

D	EN
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SOEH	D	→ EN	(HH) 0.221	(LL) 0.184	0.355 0.313	0.751 0.621	0.015 0.011	0.022 0.015	0.033 0.022	D	1.0	EN	22

Chapter 3 Scan Path Block

Function	I/F Control (SMC) with ENB										
Block type	Standard type										
	Normal		High speed								
Drivability	Name	cells	Name	cells							
x1	SOEL	2									
x2											
x4											
x8											

Logic Diagram

```

graph LR
    D_H01[D H01] --> Inverter[ ]
    Inverter --> N01_ENB[N01 ENB]
  
```

Truth Table

D	ENB
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path		t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SOEL	D	→ ENB	(HH) (LL)	0.170 0.265	0.270 0.462	0.504 0.969	0.015 0.012	0.022 0.017	0.031 0.025	D	1.0	ENB	22

Chapter 3 Scan Path Block

Function	Mega Macro Skip									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SMS1	4								
x2										
x4										
x8										

Logic Diagram

```

    graph LR
      A[A H01] --> Block[ ]
      B[B H02] --> Block
      Block --> Y[N01 Y]
  
```

Truth Table

A	Y
1	1
0	0

Note:H02 is a pin of scan

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output		
	Path			t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SMS1	A → Y			0.288	0.455	0.939	0.015	0.022	0.033	A	1.0	Y	21
	(HH) (LL)			0.327	0.575	1.221	0.013	0.017	0.027	B	1.0		

Chapter 3 Scan Path Block

Function	Set/Reset Control									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SRH1	2								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    SET_H01[SET H01] --> Buffer[ ]
    Buffer --> N01_S[N01 S]
  
```

Truth Table

SET	S
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	SET	1.0	S	22
SRH1	SET	→	S	(HH) 0.221	0.355	0.751	0.015	0.022	0.033	SET	1.0	S	22
			(LL)	0.184	0.312	0.621	0.011	0.015	0.022				



Chapter 3 Scan Path Block

Function	Set-B/Reset-B Control									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SRL1	2								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    SETB_H01[SETB H01] --> Buffer[ ]
    Buffer --> N01_S[N01 S]
  
```

Truth Table

SETB	S
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output		
	Path			t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	SETB	1.0	S	22	
SRL1	SETB	→	S	(HH) (LL)	0.170 0.265	0.270 0.462	0.504 0.969	0.015 0.012	0.022 0.017	0.031 0.025	SETB	1.0	S	22

Chapter 3 Scan Path Block

Function	Loop Cut											
Block type	Standard type											
	Normal			High speed								
Drivability	Name	cells	Name	cells								
x1	SRPD	12										
x2												
x4												
x8												

Logic Diagram

```

graph LR
    RIN_H01[RIN H01] --> Inverter[Inverter]
    Inverter --> N01_ROUT[N01 ROUT]
  
```

Truth Table

RIN	ROUT
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed							Input		Output		
	Path		t LDo (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SRPD	RIN	→ ROUT (HH) (LL)	0.387 0.462	0.609 0.803	1.263 1.699	0.015 0.014	0.023 0.019	0.035 0.030	RIN	1.0	ROUT	20

Chapter 3 Scan Path Block

Function	Clock Generator									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	SCKG	16								
x2										
x4										
x8										

Logic Diagram

```

graph LR
    CL_H01[CL H01] --> Block[ ]
    Block --> N01_SC[N01 SC]
  
```

Truth Table

CL	SC
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed						Input		Output			
	Path		t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	CL	2.1	SC	21
SCKG												

Chapter 3 Scan Path Block

Function	Common Input									
Block type	Standard type									
	Normal		High speed							
Drivability	Name	cells	Name	cells						
x1	sc1	2								
x2										
x4										
x8										

Logic Diagram

Truth Table

A	Y
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed									Input		Output	
	Path			t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	A	1.0	Y	22
SC11	A → Y			(HH)	0.177	0.269	0.498	0.015	0.022	0.031			
				(LL)	0.191	0.315	0.615	0.011	0.015	0.023			

Chapter 3 Scan Path Block

Function	Common Output											
Block type	Standard type											
	Normal			High speed								
Drivability	Name	cells	Name	cells								
x1	SCO1	4										
x2												
x4												
x8												

Logic Diagram

```

graph LR
    A[A H01] --> B[ ]
    B --> Y[N01 Y]
    style B fill:none,stroke:none
  
```

Truth Table

A	Y
1	1
0	0

Chapter 3 Scan Path Block

Block type	Switching speed								Input		Output	
	Path		t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SCO1	A	→ Y	(HH) 0.288	0.454	0.937	0.015	0.022	0.033	A	1.0	Y	21
			(LL) 0.326	0.574	1.219	0.013	0.017	0.027				

Chapter 3 Scan Path Block

Function	GND										
Block type	Standard type										
	Normal		High speed								
Drivability	Name	cells	Name	cells							
x1	SGND	2									
x2											
x4											
x8											

Logic Diagram

Truth Table

Y
0

Chapter 3 Scan Path Block

Block type	Switching speed							Input		Output		
	Path		t LDO (ns)			t 1		Symbol	Fanin	Symbol	Fanout	
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			Y	22
SGND												

# **Chapter 4**

## **Boundary Scan Block**

## 4.1 TAP Macro

[MEMO]



### Chapter 4 Boundary Scan Block

Function	BScan TAP Macro									
Block type	Standard type									
	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells						
-	SBCJ	262								
Logic Diagram										
Equivalent Circuit										

### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output	
	Path		t LDo (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→ OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBCJ												

### Chapter 4 Boundary Scan Block

Function	BScan TAP Macro with NEC Scan									
Block type	Standard type									
Drivability	Name	cells	Name	cells						
-	SBCL	315								

Logic Diagram

Equivalent Circuit

### Chapter 4 Boundary Scan Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBCL													

[MEMO]

[MEMO]

[MEMO]

## 4.2 Level Generator

Chapter 4 Boundary Scan Block

Function	BScan Level Generator (CLANP)									
Block type	Standard type									
	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells						
-	SBZ1	1								
-										

Logic Diagram

Truth Table

L
0

Chapter 4 Boundary Scan Block

Block type	Switching speed							Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBZ1												L	142

[MEMO]

[MEMO]

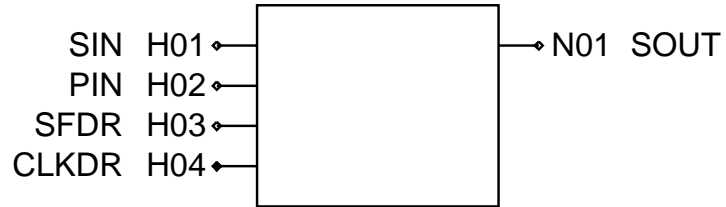
[MEMO]

### 4.3 Data Register

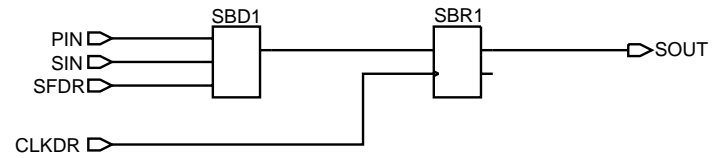
Chapter 4 Boundary Scan Block

Function	BScan Data Register for Input												
Block type	Standard type												
	-	-	-	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells									
-	SVRN12	12											
-													

Logic Diagram



Equivalent Circuit



Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				

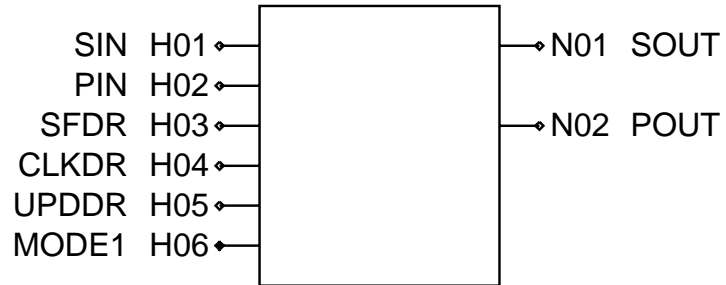
SVRN12



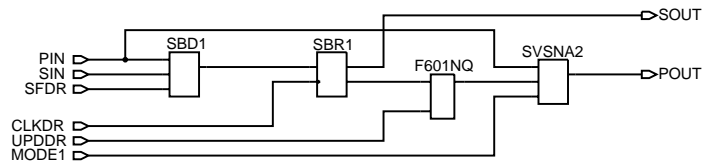
### Chapter 4 Boundary Scan Block

Function	BScan Data Register for Output									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SVRN22	24								
-										

Logic Diagram



Equivalent Circuit



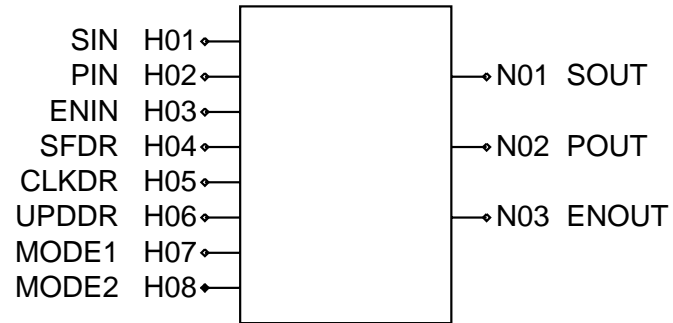
### Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SVRN22													

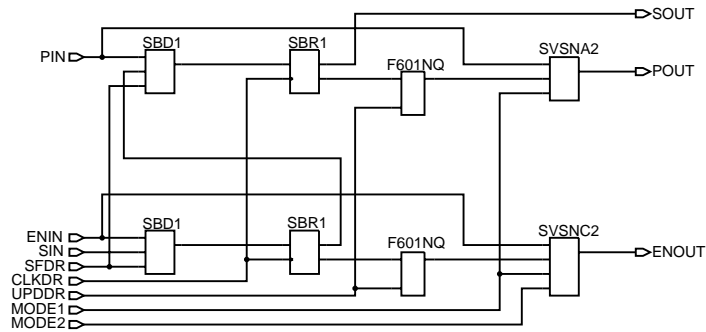
### Chapter 4 Boundary Scan Block

Function	BScan Data Register for 3-state									
Block type	Standard type									
	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells						
-	SVRN32	50								
-										

Logic Diagram



Equivalent Circuit



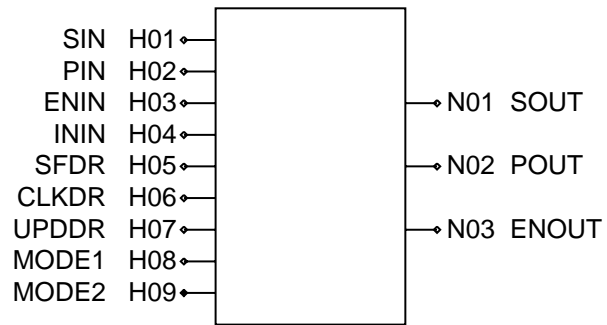
### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output	
	Path		t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
SVRN32												

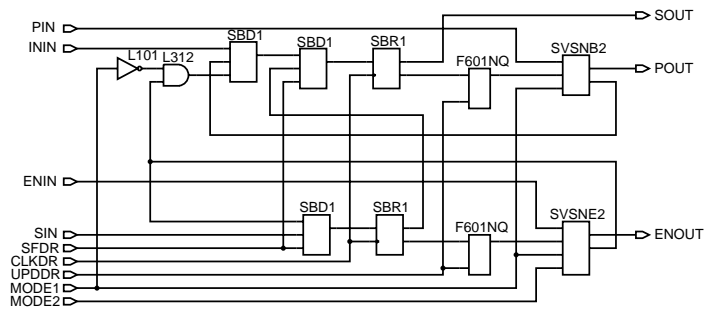
### Chapter 4 Boundary Scan Block

Function	BScan Data Register for Bid									
Block type	Standard type									
	Name	cells	Name	cells						
-	SVRNB2	57								
-										

Logic Diagram



Equivalent Circuit



### Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SVRNB2													

[MEMO]

[MEMO]

[MEMO]

#### 4.4 D-latch, Selector, Shift Register

### Chapter 4 Boundary Scan Block

Function	BScan D-Latch with SB Q Out, Low Power																													
Block type	Standard type																													
	-		-																											
Drivability	Name	cells	Name	cells																										
-	L606	5																												
Logic Diagram																														
Truth Table																														
<table border="1"> <thead> <tr> <th>D</th> <th>C</th> <th>SB</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>X</td> <td>1</td> <td>1</td> <td>Latch</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>1</td> </tr> </tbody> </table>											D	C	SB	Q	1	0	1	1	0	0	1	0	X	1	1	Latch	X	X	0	1
D	C	SB	Q																											
1	0	1	1																											
0	0	1	0																											
X	1	1	Latch																											
X	X	0	1																											
X:Irrelevant																														

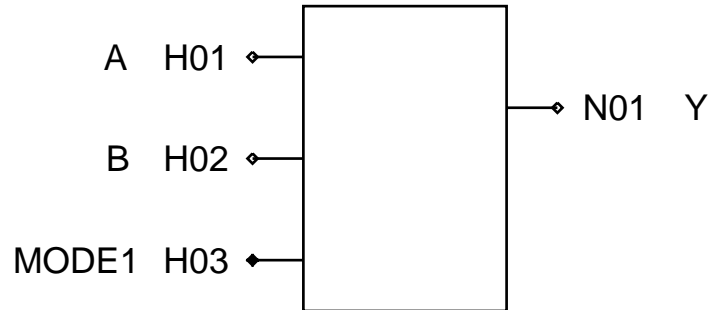
### Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L606	D → Q	(HH)		0.259	0.437	0.889	0.029	0.043	0.063	D	3.7	Q	10
		(LL)		0.322	0.614	1.311	0.024	0.034	0.053				
	C → Q	(HH)		0.396	0.656	1.333	0.029	0.043	0.063	C	1.0		
		(HL)		0.534	0.938	1.961	0.024	0.034	0.053				
	SB → Q	(HL)		0.378	0.648	1.333	0.024	0.034	0.053	SB	1.0		
		(LH)		0.281	0.473	0.964	0.029	0.044	0.064				
	Set up time	D		0.690		0.830							
	Hold time	D		0.590		0.640							
	Release time	SB		0.650		0.760							
	Removal time	SB		0.570		0.570							
Min Pulse	C		0.761		2.468								
Min Pulse	SB		0.592		1.751								

Chapter 4 Boundary Scan Block

Function	BScan Selector									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SBD1	4								
-										

Logic Diagram



Truth Table

A	B	MODE1	Y
A	X	0	A
X	B	1	B

X : Irrelevant

Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output			
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout		
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.						
SBD1	A → Y	(HH)		0.287	0.441	0.906	0.028	0.042	0.061	A	1.0	Y	10		
		(LL)		0.331	0.554	1.152	0.023	0.030	0.045						
	B → Y	(HH)		0.291	0.448	0.915	0.029	0.042	0.061					MODE1	1.0
		(LL)		0.337	0.563	1.166	0.023	0.030	0.045						
	MODE1 → Y	(HH)		0.351	0.591	1.244	0.029	0.042	0.061						
		(HL)		0.344	0.554	1.103	0.022	0.030	0.044						
		(LH)		0.316	0.542	1.144	0.029	0.042	0.061						
		(LL)		0.372	0.665	1.412	0.022	0.030	0.044						

### Chapter 4 Boundary Scan Block

Function	BScan Shift Register											
Block type	Standard type											
Drivability	Name	cells	Name	cells								
-	SBR1	8										
Logic Diagram												
Truth Table												
D	C	Q	U									
A	/	A	Hold									
B	\	Hold	B									
X : Irrelevant												

### Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBR1	C → Q	(LH)		0.501	0.894	1.929	0.026	0.038	0.054	D	3.6	Q	9
		(LL)		0.441	0.752	1.589	0.021	0.027	0.038	C	1.0	U	7
	C → U	(HH)		0.687	1.190	2.530	0.029	0.043	0.062				
		(HL)		0.641	1.083	2.235	0.023	0.031	0.046				
	Set up time	D		0.410		0.350							
	Hold time	D		0.950		1.880							
Min Pulse	C		0.949		3.064								



Chapter 4 Boundary Scan Block

Function	BScan Data Selector for Output									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SVSNA2	7								
Logic Diagram										
<pre> graph LR     H01[PIN H01] --&gt; Block[ ]     H02[BSCAN H02] --&gt; Block     H03[MODE1 H03] --&gt; Block     Block --&gt; POUT[BSCON POUT]     </pre>										
Truth Table										
	PIN	BSCAN	MODE1	POUT						
	A	X	0	A						
	X	B	1	B						
X : Irrelevant										

Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SVSNA2	PIN → POUT	(HH)		0.217	0.373	0.781	0.007	0.011	0.016	PIN	4.1	POUT	40
		(LL)		0.227	0.434	0.950	0.006	0.009	0.013				
	BSCAN → POUT	(HH)		0.354	0.577	1.206	0.008	0.011	0.017	BSCAN	1.0		
		(LL)		0.402	0.736	1.588	0.007	0.010	0.015				
	MODE1 → POUT	(HH)		0.409	0.709	1.510	0.008	0.011	0.017	MODE1	1.0		
		(HL)		0.414	0.764	1.624	0.007	0.010	0.015				
		(LH)		0.343	0.601	1.260	0.007	0.011	0.016				
		(LL)		0.371	0.691	1.492	0.006	0.009	0.013				

Chapter 4 Boundary Scan Block

Function	BScan Data Selector for Bid																								
Block type	Standard type																								
	-		-																						
Drivability	Name	cells	Name	cells																					
-	SVSNB2	7																							
Logic Diagram																									
Truth Table																									
<table border="1"> <thead> <tr> <th>PIN</th> <th>BSCAN</th> <th>MODE1</th> <th>POUT</th> <th>Z1</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>X</td> <td>0</td> <td>A</td> <td>A</td> </tr> <tr> <td>X</td> <td>B</td> <td>1</td> <td>B</td> <td>B</td> </tr> </tbody> </table>											PIN	BSCAN	MODE1	POUT	Z1	A	X	0	A	A	X	B	1	B	B
PIN	BSCAN	MODE1	POUT	Z1																					
A	X	0	A	A																					
X	B	1	B	B																					
X : Irrelevant																									

Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output		
	Path			t LDO (ns)			t 1			Symbol	Fanin	Symbol	Fanout	
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
SVSNB2	PIN	→	POUT	(HH)	0.234	0.406	0.852	0.007	0.011	0.017	PIN	4.1	POUT	39
				(LL)	0.244	0.471	1.039	0.006	0.009	0.014				
	PIN	→	Z1	(HH)	0.269	0.474	1.026	0.029	0.042	0.061	BSCAN	1.0	Z1	8
				(LL)	0.306	0.600	1.325	0.022	0.030	0.043				
	BSCAN	→	POUT	(HH)	0.379	0.624	1.317	0.008	0.012	0.018	MODE1	1.0		
				(LL)	0.433	0.800	1.735	0.007	0.010	0.015				
	BSCAN	→	Z1	(HH)	0.420	0.714	1.555	0.029	0.042	0.062				
				(LL)	0.513	0.970	2.114	0.023	0.031	0.046				
	MODE1	→	POUT	(HH)	0.433	0.754	1.613	0.008	0.012	0.018				
				(HL)	0.441	0.828	1.784	0.007	0.010	0.016				
	MODE1	→	Z1	(LH)	0.362	0.636	1.339	0.007	0.011	0.017				
				(LL)	0.388	0.730	1.581	0.006	0.009	0.014				
	MODE1	→	Z1	(HH)	0.475	0.844	1.852	0.029	0.042	0.062				
				(HL)	0.524	1.002	2.171	0.023	0.031	0.046				
				(LH)	0.396	0.705	1.512	0.029	0.042	0.061				
			(LL)	0.450	0.858	1.866	0.022	0.030	0.043					

### Chapter 4 Boundary Scan Block

Function	BScan Data Enable Selector for 3-state									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SVSNC2	9								
-										

Logic Diagram

```

graph LR
    ENIN[ENIN H01] --> Block
    BSCAN[BSCAN H02] --> Block
    MODE1[MODE1 H03] --> Block
    MODE2[MODE2 H04] --> Block
    Block --> ENOUT[BSCON ENOUT]
  
```

Truth Table

ENIN	BSCAN	MODE1	MODE2	ENOUT
A	X	0	0	A
X	B	1	0	B
X	X	X	1	0

X : Irrelevant

### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t LDO (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SVSNC2	ENIN	→	ENOUT (HH)	0.267	0.467	0.995	0.013	0.020	0.030	ENIN	4.1	ENOUT	17
			(LL)	0.257	0.488	1.061	0.007	0.009	0.014				
	BSCAN	→	ENOUT (HH)	0.406	0.669	1.418	0.013	0.020	0.031	MODE1	1.0	MODE2	4.2
			(LL)	0.433	0.794	1.708	0.008	0.011	0.017				
		MODE1	→	ENOUT (HH)	0.461	0.801	1.721	0.013	0.020				
		(HL)	0.446	0.824	1.749	0.008	0.011	0.016					
		(LH)	0.393	0.694	1.472	0.013	0.020	0.030					
		(LL)	0.401	0.746	1.603	0.007	0.009	0.014					
	MODE2	→	ENOUT (HL)	0.101	0.141	0.221	0.006	0.007	0.010				
			(LH)	0.109	0.188	0.386	0.013	0.020	0.030				

### Chapter 4 Boundary Scan Block

Function	BScan Data Enable Selector for Bid									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SVSNE2	9								
Logic Diagram										

Logic Diagram:

ENIN H01 → [Block] → BSCON ENOUT

BSCAN H02 → [Block] → N02 Z2

MODE1 H03 → [Block]

MODE2 H04 → [Block]

Truth Table					
ENIN	BSCAN	MODE1	MODE2	ENOUT	Z2
A	X	0	0	A	A
X	B	1	0	B	B
A	X	0	1	0	A
X	B	1	1	0	B

X : Irrelevant

### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t Ld0 (ns)			t 1						
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
SVSNE2	ENIN	→	ENOUT (HH)	0.284	0.500	1.069	0.013	0.020	0.030	ENIN	4.1	ENOUT	17
				0.274	0.529	1.161	0.007	0.010	0.015				
	ENIN	→	Z2 (HH)	0.260	0.458	0.968	0.029	0.043	0.063	MODE1	1.0	Z2	8
				0.279	0.567	1.224	0.023	0.032	0.048				
	BSCAN	→	ENOUT (HH)	0.432	0.719	1.535	0.013	0.020	0.031	MODE2	4.2		
				0.463	0.861	1.868	0.008	0.011	0.017				
	BSCAN	→	Z2 (HH)	0.407	0.688	1.460	0.029	0.043	0.065				
				0.467	0.919	1.967	0.024	0.034	0.053				
	MODE1	→	ENOUT (HH)	0.486	0.848	1.830	0.013	0.020	0.031				
				0.473	0.890	1.921	0.008	0.011	0.017				
				0.412	0.730	1.554	0.013	0.020	0.030				
	MODE1	→	Z2 (LL)	0.418	0.787	1.702	0.007	0.010	0.015				
				0.462	0.818	1.756	0.029	0.043	0.065				
				0.479	0.950	2.021	0.024	0.034	0.053				
	MODE2	→	ENOUT (HL)	0.387	0.688	1.454	0.029	0.043	0.063				
				0.423	0.825	1.765	0.023	0.031	0.048				
				0.101	0.142	0.222	0.006	0.007	0.010				
				(LH)	0.109	0.188	0.385	0.013	0.020	0.030			

[MEMO]

[MEMO]

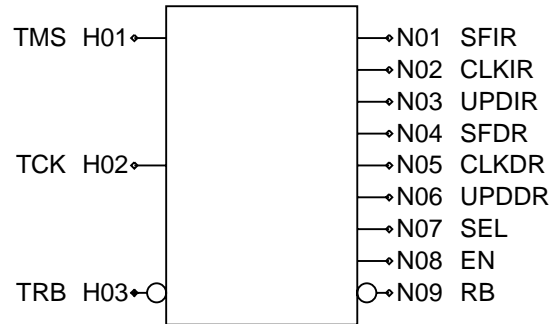
[MEMO]

## 4.5 Soft Macro

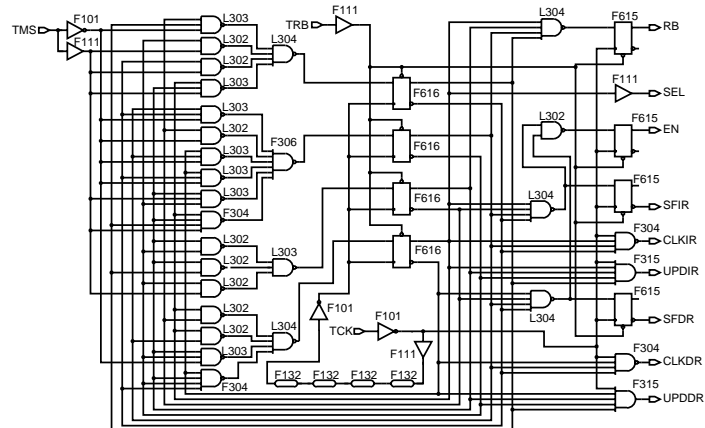
### Chapter 4 Boundary Scan Block

Function	BScan TAP Controller									
Block type	Standard type									
Drivability	Name	cells	Name	cells						
-	SBCK	392								

Logic Diagram



Equivalent Circuit



### Chapter 4 Boundary Scan Block

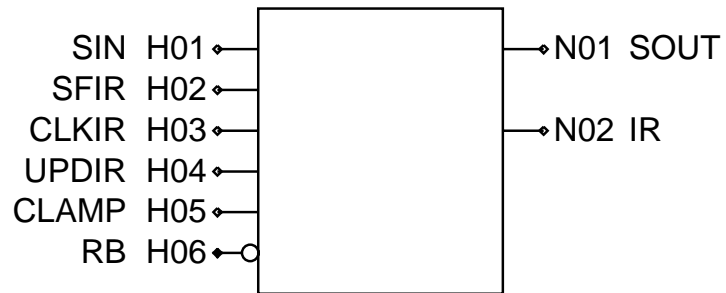
Block type	Switching speed								Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>					
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol

SBCK

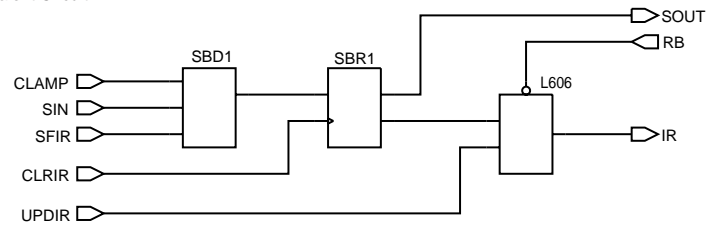
### Chapter 4 Boundary Scan Block

Function	BScan Instruction Register (Internal Circuit)									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SBM4	46								
-										

Logic Diagram



Equivalent Circuit



### Chapter 4 Boundary Scan Block

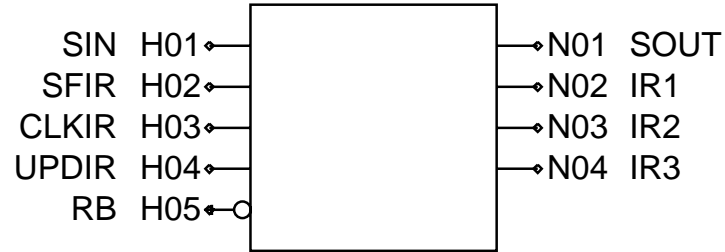
Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBM4													



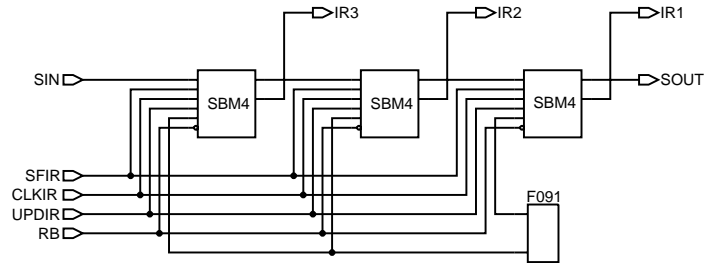
Chapter 4 Boundary Scan Block

Function	BScan Instruction Register									
Block type	Standard type									
	-		-							
Drivability	Name	cells	Name	cells						
-	SBM5	140								
-										

Logic Diagram



Equivalent Circuit



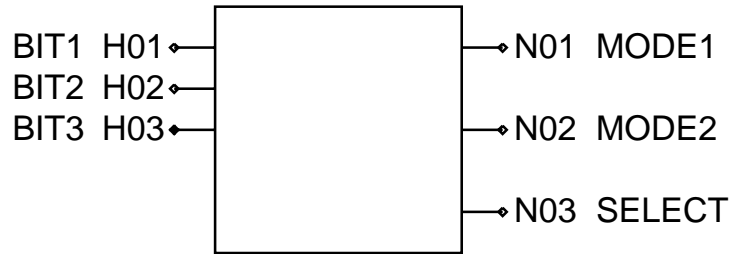
Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t Ld0 (ns)			t 1			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBM5													

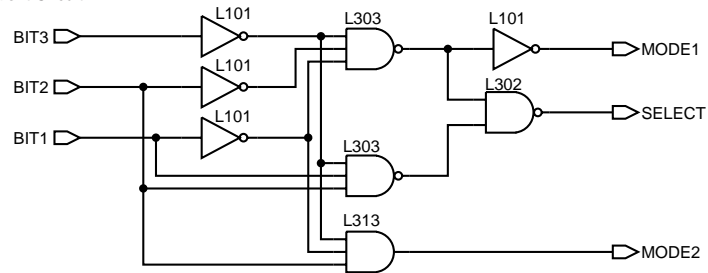
### Chapter 4 Boundary Scan Block

Function	BScan Instruction Decoder											
Block type	Standard type											
Drivability	Name	cells	Name	cells								
-	SBM6	24										

Logic Diagram



Equivalent Circuit



### Chapter 4 Boundary Scan Block

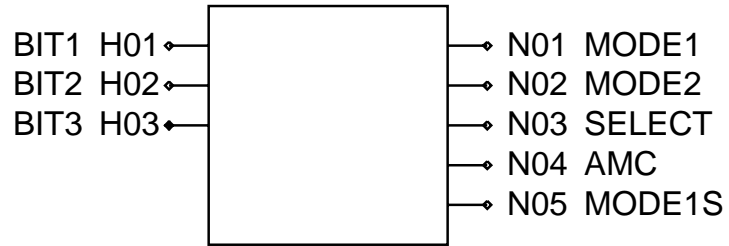
Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				

SBM6

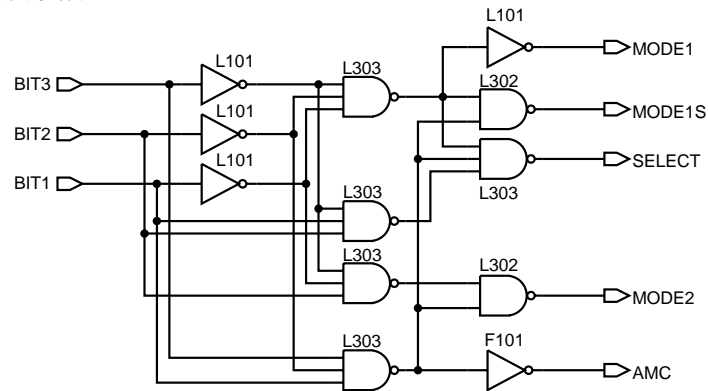
### Chapter 4 Boundary Scan Block

Function	BScan Instruction Decoder with NEC Scan									
Block type	Standard type									
Drivability	Name	cells	Name	cells						
-	SBMC	37								

Logic Diagram



Equivalent Circuit



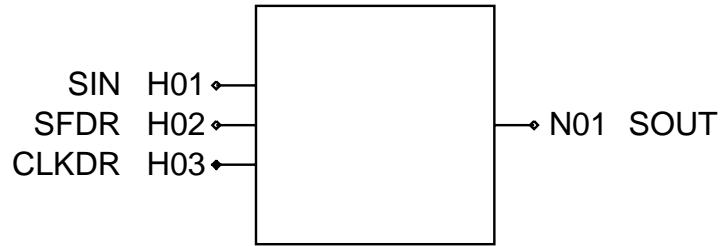
### Chapter 4 Boundary Scan Block

Block type	Switching speed								Input		Output		
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				
SBMC													

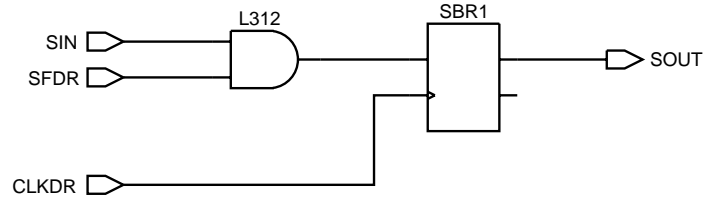
Chapter 4 Boundary Scan Block

Function	BScan Bypass Register												
Block type	Standard type												
	-	-	-	-	-	-	-	-	-	-	-	-	-
Drivability	Name	cells	Name	cells									
-	SBS3	26											
-													

Logic Diagram



Equivalent Circuit



Chapter 4 Boundary Scan Block

Block type	Switching speed									Input		Output	
	Path			t <sub>LD0</sub> (ns)			t <sub>1</sub>			Symbol	Fanin	Symbol	Fanout
	IN	→	OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.				

SBS3

# Index

Block	Function	Cells (I/O)	Page
B001	I/O Buffer 12mA	20 (1)	1-32
B002	I/O Buffer 12mA	20 (1)	1-80
B003	I/O Buffer 9mA	10 (1)	1-32
B004	I/O Buffer 9mA	10 (1)	1-80
B005	I/O Buffer 18mA	20 (1)	1-32
B006	I/O Buffer 18mA	20 (1)	1-80
B007	3-State Buffer 12mA	17 (1)	1-16
B008	3-State Buffer 9mA	7 (1)	1-16
B009	3-State Buffer 18mA	17 (1)	1-16
B00C	I/O Buffer 6mA	10 (1)	1-32
B00D	I/O Buffer 6mA	10 (1)	1-80
B00E	3-State Buffer 6mA	7 (1)	1-16
B00F	I/O Buffer 24mA	20 (1)	1-32
B00G	I/O Buffer 24mA	20 (1)	1-80
B00H	3-State Buffer 24mA	17 (1)	1-16
B00T	3-State Buffer 3mA	7 (1)	1-16
B00U	I/O Buffer 3mA	10 (1)	1-32
B00V	I/O Buffer 3mA	10 (1)	1-80
B0D1	I/O Buffer 12mA 50kΩ Pull-down	20 (1)	1-32
B0D2	I/O Buffer 12mA 50kΩ Pull-down	20 (1)	1-80
B0D3	I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-32
B0D4	I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-80
B0D5	I/O Buffer 18mA 50kΩ Pull-down	20 (1)	1-32
B0D6	I/O Buffer 18mA 50kΩ Pull-down	20 (1)	1-80
B0D7	3-State Buffer 12mA 50kΩ Pull-down	17 (1)	1-16
B0D8	3-State Buffer 9mA 50kΩ Pull-down	7 (1)	1-16
B0D9	3-State Buffer 18mA 50kΩ Pull-down	17 (1)	1-16
B0DC	I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-32
B0DD	I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-80
B0DE	3-State Buffer 6mA 50kΩ Pull-down	7 (1)	1-16
B0DF	I/O Buffer 24mA 50kΩ Pull-down	20 (1)	1-32
B0DG	I/O Buffer 24mA 50kΩ Pull-down	20 (1)	1-80
B0DH	3-State Buffer 24mA 50kΩ Pull-down	17 (1)	1-16
B0DT	3-State Buffer 3mA 50kΩ Pull-down	7 (1)	1-16
B0DU	I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-32
B0DV	I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-80
B0U1	I/O Buffer 12mA 50kΩ Pull-up	20 (1)	1-32
B0U2	I/O Buffer 12mA 50kΩ Pull-up	20 (1)	1-80
B0U3	I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-32
B0U4	I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-80
B0U5	I/O Buffer 18mA 50kΩ Pull-up	20 (1)	1-32

Block	Function	Cells (I/O)	Page
B0U6	I/O Buffer 18mA 50kΩ Pull-up	20 (1)	1-80
B0U7	3-State Buffer 12mA 50kΩ Pull-up	17 (1)	1-16
B0U8	3-State Buffer 9mA 50kΩ Pull-up	7 (1)	1-16
B0U9	3-State Buffer 18mA 50kΩ Pull-up	17 (1)	1-16
B0UC	I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-32
B0UD	I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-80
B0UE	3-State Buffer 6mA 50kΩ Pull-up	7 (1)	1-16
B0UF	I/O Buffer 24mA 50kΩ Pull-up	20 (1)	1-32
B0UG	I/O Buffer 24mA 50kΩ Pull-up	20 (1)	1-80
B0UH	3-State Buffer 24mA 50kΩ Pull-up	17 (1)	1-16
B0UT	3-State Buffer 3mA 50kΩ Pull-up	7 (1)	1-16
B0UU	I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-32
B0UV	I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-80
B0W1	I/O Buffer 12mA 5kΩ Pull-up	20 (1)	1-32
B0W2	I/O Buffer 12mA 5kΩ Pull-up	20 (1)	1-80
B0W3	I/O Buffer 9mA 5kΩ Pull-up	10 (1)	1-32
B0W4	I/O Buffer 9mA 5kΩ Pull-up	10 (1)	1-80
B0W5	I/O Buffer 18mA 5kΩ Pull-up	20 (1)	1-32
B0W6	I/O Buffer 18mA 5kΩ Pull-up	20 (1)	1-80
B0W7	3-State Buffer 12mA 5kΩ Pull-up	17 (1)	1-16
B0W8	3-State Buffer 9mA 5kΩ Pull-up	7 (1)	1-16
B0W9	3-State Buffer 18mA 5kΩ Pull-up	17 (1)	1-16
B0WC	I/O Buffer 6mA 5kΩ Pull-up	10 (1)	1-32
B0WD	I/O Buffer 6mA 5kΩ Pull-up	10 (1)	1-80
B0WE	3-State Buffer 6mA 5kΩ Pull-up	7 (1)	1-16
B0WF	I/O Buffer 24mA 5kΩ Pull-up	20 (1)	1-32
B0WG	I/O Buffer 24mA 5kΩ Pull-up	20 (1)	1-80
B0WH	3-State Buffer 24mA 5kΩ Pull-up	17 (1)	1-16
B0WT	3-State Buffer 3mA 5kΩ Pull-up	7 (1)	1-16
B0WU	I/O Buffer 3mA 5kΩ Pull-up	10 (1)	1-32
B0WV	I/O Buffer 3mA 5kΩ Pull-up	10 (1)	1-80
BE01	Low-noise I/O Buffer 12mA	10 (1)	1-38
BE02	Low-noise I/O Buffer 12mA	10 (1)	1-86
BE03	Low-noise I/O Buffer 9mA	10 (1)	1-38
BE04	Low-noise I/O Buffer 9mA	10 (1)	1-86
BE05	Low-noise I/O Buffer 18mA	10 (1)	1-38
BE06	Low-noise I/O Buffer 18mA	10 (1)	1-86
BE07	Low-noise 3-State Buffer 12mA	7 (1)	1-20
BE08	Low-noise 3-State Buffer 9mA	7 (1)	1-20
BE09	Low-noise 3-State Buffer 18mA	7 (1)	1-20
BE0C	Low-noise I/O Buffer 6mA	10 (1)	1-38
BE0D	Low-noise I/O Buffer 6mA	10 (1)	1-86
BE0E	Low-noise 3-State Buffer 6mA	7 (1)	1-20

Block	Function	Cells (I/O)	Page
BE0F	Low-noise I/O Buffer 24mA	10 (1)	1-38
BE0G	Low-noise I/O Buffer 24mA	10 (1)	1-86
BE0H	Low-noise 3-State Buffer 24mA	7 (1)	1-20
BE0T	Low-noise 3-State Buffer 3mA	7 (1)	1-20
BE0U	Low-noise I/O Buffer 3mA	10 (1)	1-38
BE0V	Low-noise I/O Buffer 3mA	10 (1)	1-86
BED1	Low-noise I/O Buffer 12mA 50kΩ Pull-down	10 (1)	1-38
BED2	Low-noise I/O Buffer 12mA 50kΩ Pull-down	10 (1)	1-86
BED3	Low-noise I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-38
BED4	Low-noise I/O Buffer 9mA 50kΩ Pull-down	10 (1)	1-86
BED5	Low-noise I/O Buffer 18mA 50kΩ Pull-down	10 (1)	1-38
BED6	Low-noise I/O Buffer 18mA 50kΩ Pull-down	10 (1)	1-86
BED7	Low-noise 3-State Buffer 12mA 50kΩ Pull-down	7 (1)	1-20
BED8	Low-noise 3-State Buffer 9mA 50kΩ Pull-down	7 (1)	1-20
BED9	Low-noise 3-State Buffer 18mA 50kΩ Pull-down	7 (1)	1-20
BEDC	Low-noise I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-38
BEDD	Low-noise I/O Buffer 6mA 50kΩ Pull-down	10 (1)	1-86
BEDE	Low-noise 3-State Buffer 6mA 50kΩ Pull-down	7 (1)	1-20
BEDF	Low-noise I/O Buffer 24mA 50kΩ Pull-down	10 (1)	1-38
BEDG	Low-noise I/O Buffer 24mA 50kΩ Pull-down	10 (1)	1-86
BEDH	Low-noise 3-State Buffer 24mA 50kΩ Pull-down	7 (1)	1-20
BEDT	Low-noise 3-State Buffer 3mA 50kΩ Pull-down	7 (1)	1-20
BEDU	Low-noise I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-38
BEDV	Low-noise I/O Buffer 3mA 50kΩ Pull-down	10 (1)	1-86
BEU1	Low-noise I/O Buffer 12mA 50kΩ Pull-up	10 (1)	1-38
BEU2	Low-noise I/O Buffer 12mA 50kΩ Pull-up	10 (1)	1-86
BEU3	Low-noise I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-38
BEU4	Low-noise I/O Buffer 9mA 50kΩ Pull-up	10 (1)	1-86
BEU5	Low-noise I/O Buffer 18mA 50kΩ Pull-up	10 (1)	1-38
BEU6	Low-noise I/O Buffer 18mA 50kΩ Pull-up	10 (1)	1-86
BEU7	Low-noise 3-State Buffer 12mA 50kΩ Pull-up	7 (1)	1-20
BEU8	Low-noise 3-State Buffer 9mA 50kΩ Pull-up	7 (1)	1-20
BEU9	Low-noise 3-State Buffer 18mA 50kΩ Pull-up	7 (1)	1-20
BEUC	Low-noise I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-38
BEUD	Low-noise I/O Buffer 6mA 50kΩ Pull-up	10 (1)	1-86
BEUE	Low-noise 3-State Buffer 6mA 50kΩ Pull-up	7 (1)	1-20
BEUF	Low-noise I/O Buffer 24mA 50kΩ Pull-up	10 (1)	1-38
BEUG	Low-noise I/O Buffer 24mA 50kΩ Pull-up	10 (1)	1-86
BEUH	Low-noise 3-State Buffer 24mA 50kΩ Pull-up	7 (1)	1-20
BEUT	Low-noise 3-State Buffer 3mA 50kΩ Pull-up	7 (1)	1-20
BEUU	Low-noise I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-38
BEUV	Low-noise I/O Buffer 3mA 50kΩ Pull-up	10 (1)	1-86
BEW1	Low-noise I/O Buffer 12mA 5kΩ Pull-up	10 (1)	1-38

Block	Function	Cells (I/O)	Page
BEW2	Low-noise I/O Buffer 12mA 5kΩ Pull-up	10 (1)	1-86
BEW3	Low-noise I/O Buffer 9mA 5kΩ Pull-up	10 (1)	1-38
BEW4	Low-noise I/O Buffer 9mA 5kΩ Pull-up	10 (1)	1-86
BEW5	Low-noise I/O Buffer 18mA 5kΩ Pull-up	10 (1)	1-38
BEW6	Low-noise I/O Buffer 18mA 5kΩ Pull-up	10 (1)	1-86
BEW7	Low-noise 3-State Buffer 12mA 5kΩ Pull-up	7 (1)	1-20
BEW8	Low-noise 3-State Buffer 9mA 5kΩ Pull-up	7 (1)	1-20
BEW9	Low-noise 3-State Buffer 18mA 5kΩ Pull-up	7 (1)	1-20
BEWC	Low-noise I/O Buffer 6mA 5kΩ Pull-up	10 (1)	1-38
BEWD	Low-noise I/O Buffer 6mA 5kΩ Pull-up	10 (1)	1-86
BEWE	Low-noise 3-State Buffer 6mA 5kΩ Pull-up	7 (1)	1-20
BEWF	Low-noise I/O Buffer 24mA 5kΩ Pull-up	10 (1)	1-38
BEWG	Low-noise I/O Buffer 24mA 5kΩ Pull-up	10 (1)	1-86
BEWH	Low-noise 3-State Buffer 24mA 5kΩ Pull-up	7 (1)	1-20
BEWT	Low-noise 3-State Buffer 3mA 5kΩ Pull-up	7 (1)	1-20
BEWU	Low-noise I/O Buffer 3mA 5kΩ Pull-up	10 (1)	1-38
BEWV	Low-noise I/O Buffer 3mA 5kΩ Pull-up	10 (1)	1-86
BFD1W	Low-noise Schmitt I/O Buffer 12mA 50kΩ Pull-down	13 (1)	1-50
BFD2W	Low-noise Schmitt I/O Buffer 12mA 50kΩ Pull-down	13 (1)	1-98
BFD3W	Low-noise Schmitt I/O Buffer 9mA 50kΩ Pull-down	13 (1)	1-50
BFD4W	Low-noise Schmitt I/O Buffer 9mA 50kΩ Pull-down	13 (1)	1-98
BFD5W	Low-noise Schmitt I/O Buffer 18mA 50kΩ Pull-down	13 (1)	1-50
BFD6W	Low-noise Schmitt I/O Buffer 18mA 50kΩ Pull-down	13 (1)	1-98
BFDCW	Low-noise Schmitt I/O Buffer 6mA 50kΩ Pull-down	13 (1)	1-50
BFDDW	Low-noise Schmitt I/O Buffer 6mA 50kΩ Pull-down	13 (1)	1-98
BDFFW	Low-noise Schmitt I/O Buffer 24mA 50kΩ Pull-down	13 (1)	1-50
BFDGW	Low-noise Schmitt I/O Buffer 24mA 50kΩ Pull-down	13 (1)	1-98
BFDUW	Low-noise Schmitt I/O Buffer 3mA 50kΩ Pull-down	13 (1)	1-50
BFDVW	Low-noise Schmitt I/O Buffer 3mA 50kΩ Pull-down	13 (1)	1-98
BFI1W	Low-noise Schmitt I/O Buffer 12mA	13 (1)	1-50
BFI2W	Low-noise Schmitt I/O Buffer 12mA	13 (1)	1-98
BFI3W	Low-noise Schmitt I/O Buffer 9mA	13 (1)	1-50
BFI4W	Low-noise Schmitt I/O Buffer 9mA	13 (1)	1-98
BFI5W	Low-noise Schmitt I/O Buffer 18mA	13 (1)	1-50
BFI6W	Low-noise Schmitt I/O Buffer 18mA	13 (1)	1-98
BFICW	Low-noise Schmitt I/O Buffer 6mA	13 (1)	1-50
BFIDW	Low-noise Schmitt I/O Buffer 6mA	13 (1)	1-98
BFIFW	Low-noise Schmitt I/O Buffer 24mA	13 (1)	1-50
BFIGW	Low-noise Schmitt I/O Buffer 24mA	13 (1)	1-98
BFIUW	Low-noise Schmitt I/O Buffer 3mA	13 (1)	1-50
BFIVW	Low-noise Schmitt I/O Buffer 3mA	13 (1)	1-98
BFU1W	Low-noise Schmitt I/O Buffer 12mA 50kΩ Pull-up	13 (1)	1-50
BFU2W	Low-noise Schmitt I/O Buffer 12mA 50kΩ Pull-up	13 (1)	1-98



Block	Function	Cells (I/O)	Page
BFU3W	Low-noise Schmitt I/O Buffer 9mA 50kΩ Pull-up	13 (1)	1-50
BFU4W	Low-noise Schmitt I/O Buffer 9mA 50kΩ Pull-up	13 (1)	1-98
BFU5W	Low-noise Schmitt I/O Buffer 18mA 50kΩ Pull-up	13 (1)	1-50
BFU6W	Low-noise Schmitt I/O Buffer 18mA 50kΩ Pull-up	13 (1)	1-98
BFUCW	Low-noise Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-50
BFUDW	Low-noise Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-98
BFUFW	Low-noise Schmitt I/O Buffer 24mA 50kΩ Pull-up	13 (1)	1-50
BFUGW	Low-noise Schmitt I/O Buffer 24mA 50kΩ Pull-up	13 (1)	1-98
BFUUW	Low-noise Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-50
BFUVW	Low-noise Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-98
BFW1W	Low-noise Schmitt I/O Buffer 12mA 5kΩ Pull-up	13 (1)	1-50
BFW2W	Low-noise Schmitt I/O Buffer 12mA 5kΩ Pull-up	13 (1)	1-98
BFW3W	Low-noise Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-50
BFW4W	Low-noise Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-98
BFW5W	Low-noise Schmitt I/O Buffer 18mA 5kΩ Pull-up	13 (1)	1-50
BFW6W	Low-noise Schmitt I/O Buffer 18mA 5kΩ Pull-up	13 (1)	1-98
BFWCW	Low-noise Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-50
BFWDW	Low-noise Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-98
BFWFW	Low-noise Schmitt I/O Buffer 24mA 5kΩ Pull-up	13 (1)	1-50
BFWGW	Low-noise Schmitt I/O Buffer 24mA 5kΩ Pull-up	13 (1)	1-98
BFWUW	Low-noise Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-50
BFVWV	Low-noise Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-98
BN21	I/O Buffer with EN(AND) 12mA	23 (1)	1-56
BN22	I/O Buffer with EN(AND) 12mA	24 (1)	1-104
BN23	I/O Buffer with EN(AND) 9mA	13 (1)	1-56
BN24	I/O Buffer with EN(AND) 9mA	14 (1)	1-104
BN25	I/O Buffer with EN(AND) 18mA	23 (1)	1-56
BN26	I/O Buffer with EN(AND) 18mA	24 (1)	1-104
BN2C	I/O Buffer with EN(AND) 6mA	13 (1)	1-56
BN2D	I/O Buffer with EN(AND) 6mA	14 (1)	1-104
BN2F	I/O Buffer with EN(AND) 24mA	23 (1)	1-56
BN2G	I/O Buffer with EN(AND) 24mA	24 (1)	1-104
BN2U	I/O Buffer with EN(AND) 3mA	13 (1)	1-56
BN2V	I/O Buffer with EN(AND) 3mA	14 (1)	1-104
BN31	I/O Buffer with EN(OR) 12mA	21 (1)	1-60
BN32	I/O Buffer with EN(OR) 12mA	21 (1)	1-108
BN33	I/O Buffer with EN(OR) 9mA	11 (1)	1-60
BN34	I/O Buffer with EN(OR) 9mA	11 (1)	1-108
BN35	I/O Buffer with EN(OR) 18mA	21 (1)	1-60
BN36	I/O Buffer with EN(OR) 18mA	21 (1)	1-108
BN3C	I/O Buffer with EN(OR) 6mA	11 (1)	1-60
BN3D	I/O Buffer with EN(OR) 6mA	11 (1)	1-108
BN3F	I/O Buffer with EN(OR) 24mA	21 (1)	1-60

Block	Function	Cells (I/O)	Page
BN3G	I/O Buffer with EN(OR) 24mA	21 (1)	1-108
BN3U	I/O Buffer with EN(OR) 3mA	11 (1)	1-60
BN3V	I/O Buffer with EN(OR) 3mA	11 (1)	1-108
BN41	I/O Buffer with EN(AND) 12mA 50kΩ Pull-down	23 (1)	1-56
BN42	I/O Buffer with EN(AND) 12mA 50kΩ Pull-down	24 (1)	1-104
BN43	I/O Buffer with EN(AND) 9mA 50kΩ Pull-down	13 (1)	1-56
BN44	I/O Buffer with EN(AND) 9mA 50kΩ Pull-down	14 (1)	1-104
BN45	I/O Buffer with EN(AND) 18mA 50kΩ Pull-down	23 (1)	1-56
BN46	I/O Buffer with EN(AND) 18mA 50kΩ Pull-down	24 (1)	1-104
BN4C	I/O Buffer with EN(AND) 6mA 50kΩ Pull-down	13 (1)	1-56
BN4D	I/O Buffer with EN(AND) 6mA 50kΩ Pull-down	14 (1)	1-104
BN4F	I/O Buffer with EN(AND) 24mA 50kΩ Pull-down	23 (1)	1-56
BN4G	I/O Buffer with EN(AND) 24mA 50kΩ Pull-down	24 (1)	1-104
BN4U	I/O Buffer with EN(AND) 3mA 50kΩ Pull-down	13 (1)	1-56
BN4V	I/O Buffer with EN(AND) 3mA 50kΩ Pull-down	14 (1)	1-104
BN51	I/O Buffer with EN(OR) 12mA 50kΩ Pull-down	21 (1)	1-60
BN52	I/O Buffer with EN(OR) 12mA 50kΩ Pull-down	21 (1)	1-108
BN53	I/O Buffer with EN(OR) 9mA 50kΩ Pull-down	11 (1)	1-60
BN54	I/O Buffer with EN(OR) 9mA 50kΩ Pull-down	11 (1)	1-108
BN55	I/O Buffer with EN(OR) 18mA 50kΩ Pull-down	21 (1)	1-60
BN56	I/O Buffer with EN(OR) 18mA 50kΩ Pull-down	21 (1)	1-108
BN5C	I/O Buffer with EN(OR) 6mA 50kΩ Pull-down	11 (1)	1-60
BN5D	I/O Buffer with EN(OR) 6mA 50kΩ Pull-down	11 (1)	1-108
BN5F	I/O Buffer with EN(OR) 24mA 50kΩ Pull-down	21 (1)	1-60
BN5G	I/O Buffer with EN(OR) 24mA 50kΩ Pull-down	21 (1)	1-108
BN5U	I/O Buffer with EN(OR) 3mA 50kΩ Pull-down	11 (1)	1-60
BN5V	I/O Buffer with EN(OR) 3mA 50kΩ Pull-down	11 (1)	1-108
BSD1W	Schmitt I/O Buffer 12mA 50kΩ Pull-down	23 (1)	1-44
BSD2W	Schmitt I/O Buffer 12mA 50kΩ Pull-down	23 (1)	1-92
BSD3W	Schmitt I/O Buffer 9mA 50kΩ Pull-down	13 (1)	1-44
BSD4W	Schmitt I/O Buffer 9mA 50kΩ Pull-down	13 (1)	1-92
BSD5W	Schmitt I/O Buffer 18mA 50kΩ Pull-down	23 (1)	1-44
BSD6W	Schmitt I/O Buffer 18mA 50kΩ Pull-down	23 (1)	1-92
BSDCW	Schmitt I/O Buffer 6mA 50kΩ Pull-down	13 (1)	1-44
BSDDW	Schmitt I/O Buffer 6mA 50kΩ Pull-down	13 (1)	1-92
BSDFW	Schmitt I/O Buffer 24mA 50kΩ Pull-down	23 (1)	1-44
BSDGW	Schmitt I/O Buffer 24mA 50kΩ Pull-down	23 (1)	1-92
BSDUW	Schmitt I/O Buffer 3mA 50kΩ Pull-down	13 (1)	1-44
BSDVW	Schmitt I/O Buffer 3mA 50kΩ Pull-down	13 (1)	1-92
BSI1W	Schmitt I/O Buffer 12mA	23 (1)	1-44
BSI2W	Schmitt I/O Buffer 12mA	23 (1)	1-92
BSI3W	Schmitt I/O Buffer 9mA	13 (1)	1-44
BSI4W	Schmitt I/O Buffer 9mA	13 (1)	1-92

Block	Function	Cells (I/O)	Page
BSI5W	Schmitt I/O Buffer 18mA	23 (1)	1-44
BSI6W	Schmitt I/O Buffer 18mA	23 (1)	1-92
BSICW	Schmitt I/O Buffer 6mA	13 (1)	1-44
BSIDW	Schmitt I/O Buffer 6mA	13 (1)	1-92
BSIFW	Schmitt I/O Buffer 24mA	23 (1)	1-44
BSIGW	Schmitt I/O Buffer 24mA	23 (1)	1-92
BSIUW	Schmitt I/O Buffer 3mA	13 (1)	1-44
BSIVW	Schmitt I/O Buffer 3mA	13 (1)	1-92
BSU1W	Schmitt I/O Buffer 12mA 50kΩ Pull-up	23 (1)	1-44
BSU2W	Schmitt I/O Buffer 12mA 50kΩ Pull-up	23 (1)	1-92
BSU3W	Schmitt I/O Buffer 9mA 50kΩ Pull-up	13 (1)	1-44
BSU4W	Schmitt I/O Buffer 9mA 50kΩ Pull-up	13 (1)	1-92
BSU5W	Schmitt I/O Buffer 18mA 50kΩ Pull-up	23 (1)	1-44
BSU6W	Schmitt I/O Buffer 18mA 50kΩ Pull-up	23 (1)	1-92
BSUCW	Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-44
BSUDW	Schmitt I/O Buffer 6mA 50kΩ Pull-up	13 (1)	1-92
BSUFW	Schmitt I/O Buffer 24mA 50kΩ Pull-up	23 (1)	1-44
BSUGW	Schmitt I/O Buffer 24mA 50kΩ Pull-up	23 (1)	1-92
BSUUW	Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-44
BSUVW	Schmitt I/O Buffer 3mA 50kΩ Pull-up	13 (1)	1-92
BSW1W	Schmitt I/O Buffer 12mA 5kΩ Pull-up	23 (1)	1-44
BSW2W	Schmitt I/O Buffer 12mA 5kΩ Pull-up	23 (1)	1-92
BSW3W	Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-44
BSW4W	Schmitt I/O Buffer 9mA 5kΩ Pull-up	13 (1)	1-92
BSW5W	Schmitt I/O Buffer 18mA 5kΩ Pull-up	23 (1)	1-44
BSW6W	Schmitt I/O Buffer 18mA 5kΩ Pull-up	23 (1)	1-92
BSWCW	Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-44
BSWDW	Schmitt I/O Buffer 6mA 5kΩ Pull-up	13 (1)	1-92
BSWFW	Schmitt I/O Buffer 24mA 5kΩ Pull-up	23 (1)	1-44
BSWGW	Schmitt I/O Buffer 24mA 5kΩ Pull-up	23 (1)	1-92
BSWUW	Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-44
BSWVW	Schmitt I/O Buffer 3mA 5kΩ Pull-up	13 (1)	1-92
EBA1	N-ch open drain I/O Buffer with failsafe 9mA	7 (1)	1-28
EBA2	N-ch open drain I/O Buffer with failsafe 9mA	7 (1)	1-76
EBA5	N-ch open drain I/O Buffer with failsafe 18mA	7 (1)	1-28
EBA6	N-ch open drain I/O Buffer with failsafe 18mA	7 (1)	1-76
EBA9	N-ch open drain I/O Buffer with failsafe 12mA	7 (1)	1-28
EBAA	N-ch open drain I/O Buffer with failsafe 12mA	7 (1)	1-76
EBAD	N-ch open drain I/O Buffer with failsafe 24mA	7 (1)	1-28
EBAE	N-ch open drain I/O Buffer with failsafe 24mA	7 (1)	1-76
EBE1W	N-ch open drain Schmitt I/O Buffer with failsafe 9mA	10 (1)	1-30
EBE2W	N-ch open drain Schmitt I/O Buffer with failsafe 9mA	10 (1)	1-78
EBE5W	N-ch open drain Schmitt I/O Buffer with failsafe 18mA	10 (1)	1-30

Block	Function	Cells (I/O)	Page
EBE6W	N-ch open drain Schmitt I/O Buffer with failsafe 18mA	10 (1)	1-78
EBE9W	N-ch open drain Schmitt I/O Buffer with failsafe 12mA	10 (1)	1-30
EBEAW	N-ch open drain Schmitt I/O Buffer with failsafe 12mA	10 (1)	1-78
EBEDW	N-ch open drain Schmitt I/O Buffer with failsafe 24mA	10 (1)	1-30
EBEEW	N-ch open drain Schmitt I/O Buffer with failsafe 24mA	10 (1)	1-78
EXO1	N-ch open drain Buffer with failsafe 9mA	4 (1)	1-26
EXO5	N-ch open drain Buffer with failsafe 18mA	4 (1)	1-26
EXO9	N-ch open drain Buffer with failsafe 12mA	4 (1)	1-26
EXOD	N-ch open drain Buffer with failsafe 24mA	4 (1)	1-26
EXT1	N-ch open drain Buffer 9mA	4 (1)	1-24
EXT3	N-ch open drain Buffer 9mA 50kΩ Pull-up	4 (1)	1-24
EXT5	N-ch open drain Buffer 18mA	4 (1)	1-24
EXT7	N-ch open drain Buffer 18mA 50kΩ Pull-up	4 (1)	1-24
EXT9	N-ch open drain Buffer 12mA	4 (1)	1-24
EXTB	N-ch open drain Buffer 12mA 50kΩ Pull-up	4 (1)	1-24
EXTD	N-ch open drain Buffer 24mA	4 (1)	1-24
EXTF	N-ch open drain Buffer 24mA 50kΩ Pull-up	4 (1)	1-24
EXW3	N-ch open drain Buffer 9mA 5kΩ Pull-up	4 (1)	1-24
EXW7	N-ch open drain Buffer 18mA 5kΩ Pull-up	4 (1)	1-24
EXWB	N-ch open drain Buffer 12mA 5kΩ Pull-up	4 (1)	1-24
EXWF	N-ch open drain Buffer 24mA 5kΩ Pull-up	4 (1)	1-24
F091	H, L Level Generator	1 (-)	2-4
F101	Inverter Single Out	1 (-)	2-10
F102	Inverter Single Out, x2-drive	2 (-)	2-10
F111	Buffer Single Out	2 (-)	2-12
F112	Buffer Single Out, x2-drive	3 (-)	2-12
F131	Delay Gate	6 (-)	2-16
F132	Delay Gate	10 (-)	2-16
F143	Inverter Single Out, x3-drive	3 (-)	2-10
F144	Inverter Single Out, x4-drive	4 (-)	2-10
F145	Inverter Single Out, x5-drive	5 (-)	2-10
F146	Inverter Single Out, x6-drive	6 (-)	2-10
F148	Inverter Single Out, x8-drive	12 (-)	2-10
F153	Buffer Single Out, x3-drive	4 (-)	2-12
F154	Buffer Single Out, x4-drive	5 (-)	2-12
F158	Buffer Single Out, x8-drive	11 (-)	2-12
F202	2-Input NOR	2 (-)	2-22
F203	3-Input NOR	3 (-)	2-24
F204	4-Input NOR	4 (-)	2-26
F205	5-Input NOR	5 (-)	2-28
F206	6-Input NOR	5 (-)	2-30
F208	8-Input NOR	7 (-)	2-32
F212	2-Input OR	2 (-)	2-34

Block	Function	Cells (I/O)	Page
F213	3-Input OR	3 (-)	2-36
F214	4-Input OR	3 (-)	2-38
F215	5-Input OR	5 (-)	2-40
F216	6-Input OR	5 (-)	2-42
F218	8-Input OR	8 (-)	2-44
F222	2-Input NOR x2-drive	4 (-)	2-22
F223	3-Input NOR x2-drive	6 (-)	2-24
F225	5-Input NOR x2-drive	6 (-)	2-28
F226	6-Input NOR x2-drive	6 (-)	2-30
F228	8-Input NOR x2-drive	8 (-)	2-32
F232	2-Input OR x2-drive	3 (-)	2-34
F233	3-Input OR x2-drive	4 (-)	2-36
F234	4-Input OR x2-drive	4 (-)	2-38
F235	5-Input OR x2-drive	7 (-)	2-40
F236	6-Input OR x2-drive	7 (-)	2-42
F238	8-Input OR x2-drive	9 (-)	2-44
F252	2-Input OR x4-drive	6 (-)	2-34
F282	2-Input NOR x4-drive	6 (-)	2-22
F302	2-Input NAND	2 (-)	2-50
F303	3-Input NAND	3 (-)	2-52
F304	4-Input NAND	4 (-)	2-54
F305	5-Input NAND	5 (-)	2-56
F306	6-Input NAND	5 (-)	2-58
F308	8-Input NAND	6 (-)	2-60
F312	2-Input AND	2 (-)	2-62
F313	3-Input AND	3 (-)	2-64
F314	4-Input AND	3 (-)	2-66
F315	5-Input AND	5 (-)	2-68
F316	6-Input AND	5 (-)	2-70
F318	8-Input AND	6 (-)	2-72
F322	2-Input NAND x2-drive	4 (-)	2-50
F323	3-Input NAND x2-drive	6 (-)	2-52
F324	4-Input NAND x2-drive	8 (-)	2-54
F325	5-Input NAND x2-drive	6 (-)	2-56
F326	6-Input NAND x2-drive	6 (-)	2-58
F328	8-Input NAND x2-drive	7 (-)	2-60
F332	2-Input AND x2-drive	3 (-)	2-62
F333	3-Input AND x2-drive	4 (-)	2-64
F334	4-Input AND x2-drive	4 (-)	2-66
F335	5-Input AND x2-drive	7 (-)	2-68
F336	6-Input AND x2-drive	7 (-)	2-70
F338	8-Input AND x2-drive	8 (-)	2-72
F352	2-Input AND x4-drive	6 (-)	2-62

Block	Function	Cells (I/O)	Page
F382	2-Input NAND x4-drive	6 (-)	2-50
F421	1-2-Input AND-NOR	3 (-)	2-78
F422	1-1-2-Input AND-NOR	4 (-)	2-80
F423	1-3-Input AND-NOR	4 (-)	2-82
F424	2-2-Input AND-NOR	4 (-)	2-84
F427	2-3-Input AND-NOR	5 (-)	2-86
F428	1-2-2-Input AND-NOR	5 (-)	2-88
F429	2-2-2-2-Input AND-NOR	6 (-)	2-90
F430	1-4-Input OR-NAND	5 (-)	2-118
F431	1-2-Input OR-NAND	3 (-)	2-120
F432	1-1-2-Input OR-NAND	4 (-)	2-122
F433	1-3-Input OR-NAND	4 (-)	2-124
F434	2-2-Input OR-NAND	4 (-)	2-126
F439	1-5-Input OR-NAND	6 (-)	2-128
F440	1-4-Input AND-NOR	5 (-)	2-92
F441	1-5-Input AND-NOR	7 (-)	2-94
F444	4-4-4-Input AND-NOR	8 (-)	2-96
F446	1-1-1-2-Input AND-NOR	5 (-)	2-98
F447	1-1-1-3-Input AND-NOR	5 (-)	2-100
F448	1-1-2-2-Input AND-NOR	5 (-)	2-102
F449	3-3-3-3-Input AND-NOR	8 (-)	2-104
F450	2-4-Input OR-NAND	6 (-)	2-130
F451	4-4-Input OR-NAND	8 (-)	2-132
F452	1-1-3-Input OR-NAND	5 (-)	2-134
F453	1-1-4-Input OR-NAND	6 (-)	2-136
F457	4-4-4-Input OR-NAND	10 (-)	2-138
F458	1-1-1-2-Input OR-NAND	5 (-)	2-140
F459	1-1-1-3-Input OR-NAND	5 (-)	2-142
F460	3-3-3-Input AND-NOR	7 (-)	2-106
F464	1-1-4-Input AND-NOR	5 (-)	2-108
F465	1-1-1-1-2-Input AND-NOR	5 (-)	2-110
F466	4-4-4-4-Input AND-NOR	10 (-)	2-112
F490	1-1-1-1-2-Input OR-NAND	5 (-)	2-144
F491	1-2-3-Input OR-NAND	5 (-)	2-146
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F53G	3-State Buffer with ENB, x4-drive	11 (-)	2-182
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F569	8 to 1 Multiplexer (Positive Out) with ENB	18 (-)	2-194
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F602	D-Latch with R	6 (-)	2-222
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F603	D-Latch with RB	7 (-)	2-226
F603NB	D-Latch with RB QB Out	6 (-)	2-226
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F604	D-Latch (GB)	6 (-)	2-236
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F604NQ	D-Latch (GB) Q Out	5 (-)	2-236
F605	D-Latch (GB) with RB	7 (-)	2-240
F605NB	D-Latch (GB) with RB QB Out	6 (-)	2-240
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Block	Function	Cells (I/O)	Page
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F60KNB	D-Latch with SB QB Out	5 (-)	2-230
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F615	D-F/F with RB	9 (-)	2-256
F615H	D-F/F with RB, Hold	11 (-)	2-294
F615HB	D-F/F with RB, Hold QB Out	10 (-)	2-294
F615HQ	D-F/F with RB, Hold Q Out	10 (-)	2-294
F615NB	D-F/F with RB QB Out	8 (-)	2-256
F615NQ	D-F/F with RB Q Out	8 (-)	2-256
F615S	D-F/F with RB, 2 to 1 Selector	11 (-)	2-278
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F616H	D-F/F with SB, Hold	11 (-)	2-296
F616HB	D-F/F with SB, Hold QB Out	10 (-)	2-296
F616HQ	D-F/F with SB, Hold Q Out	10 (-)	2-296
F616NB	D-F/F with SB QB Out	8 (-)	2-258
F616NQ	D-F/F with SB Q Out	8 (-)	2-258
F616S	D-F/F with SB, 2 to 1 Selector	11 (-)	2-280
F616SB	D-F/F with SB, 2 to 1 Selector QB Out	10 (-)	2-280
F616SQ	D-F/F with SB, 2 to 1 Selector Q Out	10 (-)	2-280
F641	D-F/F	8 (-)	2-248
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F641HB	D-F/F with Hold QB Out	9 (-)	2-292
F641HQ	D-F/F with Hold Q Out	9 (-)	2-292
F641NB	D-F/F QB Out	7 (-)	2-248
F641NQ	D-F/F Q Out	7 (-)	2-248
F641S	D-F/F with 2 to 1 Selector	10 (-)	2-270
F641SB	D-F/F with 2 to 1 Selector QB Out	9 (-)	2-270
F641SQ	D-F/F with 2 to 1 Selector Q Out	9 (-)	2-270
F642	D-F/F with R	9 (-)	2-250
F642NB	D-F/F with R QB Out	8 (-)	2-250
F642NQ	D-F/F with R Q Out	8 (-)	2-250
F642S	D-F/F with R, 2 to 1 Selector	11 (-)	2-272
F642SB	D-F/F with R, 2 to 1 Selector QB Out	10 (-)	2-272
F642SQ	D-F/F with R, 2 to 1 Selector Q Out	10 (-)	2-272
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F643NB	D-F/F with S QB Out	8 (-)	2-252
F643NQ	D-F/F with S Q Out	8 (-)	2-252
F643S	D-F/F with S, 2 to 1 Selector	11 (-)	2-274
F643SB	D-F/F with S, 2 to 1 Selector QB Out	10 (-)	2-274



Block	Function	Cells (I/O)	Page
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F644	D-F/F with R, S	10 (-)	2-254
F644NB	D-F/F with R, S QB Out	9 (-)	2-254
F644NQ	D-F/F with R, S Q Out	9 (-)	2-254
F644S	D-F/F with R, S, 2 to 1 Selector	12 (-)	2-276
F644SB	D-F/F with R, S, 2 to 1 Selector QB Out	11 (-)	2-276
F644SQ	D-F/F with R, S, 2 to 1 Selector Q Out	11 (-)	2-276
F647	D-F/F with RB, SB	10 (-)	2-260
F647H	D-F/F with RB, SB, Hold	12 (-)	2-298
F647HB	D-F/F with RB, SB, Hold QB Out	11 (-)	2-298
F647HQ	D-F/F with RB, SB, Hold Q Out	11 (-)	2-298
F647NB	D-F/F with RB, SB QB Out	9 (-)	2-260
F647NQ	D-F/F with RB, SB Q Out	9 (-)	2-260
F647S	D-F/F with RB, SB, 2 to 1 Selector	12 (-)	2-282
F647SB	D-F/F with RB, SB, 2 to 1 Selector QB Out	11 (-)	2-282
F647SQ	D-F/F with RB, SB, 2 to 1 Selector Q Out	11 (-)	2-282
F661	D-F/F (CB)	8 (-)	2-262
F661NB	D-F/F (CB) QB Out	7 (-)	2-262
F661NQ	D-F/F (CB) Q Out	7 (-)	2-262
F661S	D-F/F (CB) with 2 to 1 Selector	10 (-)	2-284
F661SB	D-F/F (CB) with 2 to 1 Selector QB Out	9 (-)	2-284
F661SQ	D-F/F (CB) with 2 to 1 Selector Q Out	9 (-)	2-284
F665	D-F/F (CB) with RB	9 (-)	2-264
F665NB	D-F/F (CB) with RB QB Out	8 (-)	2-264
F665NQ	D-F/F (CB) with RB Q Out	8 (-)	2-264
F665S	D-F/F (CB) with RB, 2 to 1 Selector	11 (-)	2-286
F665SB	D-F/F (CB) with RB, 2 to 1 Selector QB Out	10 (-)	2-286
F665SQ	D-F/F (CB) with RB, 2 to 1 Selector Q Out	10 (-)	2-286
F666	D-F/F (CB) with SB	9 (-)	2-266
F666NB	D-F/F (CB) with SB QB Out	8 (-)	2-266
F666NQ	D-F/F (CB) with SB Q Out	8 (-)	2-266
F666S	D-F/F (CB) with SB, 2 to 1 Selector	11 (-)	2-288
F666SB	D-F/F (CB) with SB, 2 to 1 Selector QB Out	10 (-)	2-288
F666SQ	D-F/F (CB) with SB, 2 to 1 Selector Q Out	10 (-)	2-288
F667	D-F/F (CB) with RB, SB	10 (-)	2-268
F667NB	D-F/F (CB) with RB, SB QB Out	9 (-)	2-268
F667NQ	D-F/F (CB) with RB, SB Q Out	9 (-)	2-268
F667S	D-F/F (CB) with RB, SB, 2 to 1 Selector	12 (-)	2-290
F667SB	D-F/F (CB) with RB, SB, 2 to 1 Selector QB Out	11 (-)	2-290
F667SQ	D-F/F (CB) with RB, SB, 2 to 1 Selector Q Out	11 (-)	2-290
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F674	D-F/F (CB) with Hold, 2 to 1 Selector(2 CTRL), RB	12 (-)	2-302
F6R1	D-Latch, High Speed	6 (-)	2-220

Block	Function	Cells (I/O)	Page
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F6R5	D-Latch with RB, High Speed	6 (-)	2-228
F6R8	D-Latch (GB), High Speed	6 (-)	2-238
F6R9	D-Latch (GB) with RB, High Speed	6 (-)	2-242
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F744NQ	T-F/F with R, S Q Out	8 (-)	2-308
F745	T-F/F with RB	8 (-)	2-310
F745NQ	T-F/F with RB Q Out	7 (-)	2-310
F747	T-F/F with RB, SB	9 (-)	2-312
F747NQ	T-F/F with RB, SB Q Out	8 (-)	2-312
F765	T-F/F (TB) with RB	8 (-)	2-316
F765NQ	T-F/F (TB) with RB Q Out	7 (-)	2-316
F767	T-F/F (TB) with RB, SB	9 (-)	2-318
F767NQ	T-F/F (TB) with RB, SB Q Out	8 (-)	2-318
F771	JK-F/F	10 (-)	2-322
F771NB	JK-F/F QB Out	9 (-)	2-322
F771NQ	JK-F/F Q Out	9 (-)	2-322
F774	JK-F/F with R, S	12 (-)	2-326
F774NB	JK-F/F with R, S QB Out	11 (-)	2-326
F774NQ	JK-F/F with R, S Q Out	11 (-)	2-326
F775	JK-F/F with RB	11 (-)	2-328
F775NB	JK-F/F with RB QB Out	10 (-)	2-328
F775NQ	JK-F/F with RB Q Out	10 (-)	2-328
F776	JK-F/F with SB	11 (-)	2-330
F776NB	JK-F/F with SB QB Out	10 (-)	2-330
F776NQ	JK-F/F with SB Q Out	10 (-)	2-330
F777	JK-F/F with RB, SB	12 (-)	2-332
F777NB	JK-F/F with RB, SB QB Out	11 (-)	2-332
F777NQ	JK-F/F with RB, SB Q Out	11 (-)	2-332
F781	JK-F/F (CB)	10 (-)	2-334
F781NB	JK-F/F (CB) QB Out	9 (-)	2-334
F781NQ	JK-F/F (CB) Q Out	9 (-)	2-334
F787	JK-F/F (CB) with RB, SB	12 (-)	2-338
F787NB	JK-F/F (CB) with RB, SB QB Out	11 (-)	2-338
F787NQ	JK-F/F (CB) with RB, SB Q Out	11 (-)	2-338
F791	T-F/F with Data-Hold R, S	12 (-)	2-314
F792	T-F/F (TB) with Data-Hold RB, SB	12 (-)	2-320
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F7E1	JK-F/F (CB), High Speed	10 (-)	2-336
FC42	CTS Driver (Inverter Type) Single type	80 (-)	2-14
FC44	CTS Driver (Inverter Type) Double type	340 (-)	2-14
FC82	CTS Driver (Inverter Type) Single type, x2-drive	396 (-)	2-14
FC84	CTS Driver (Inverter Type) Double type, x2-drive	1020 (-)	2-14

Block	Function	Cells (I/O)	Page
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FDA2	Input Buffer with failsafe 50kΩ Pull-down	3 (1)	1-70
FDE1W	Input Buffer with failsafe Schmitt 50kΩ Pull-down	6 (1)	1-6
FDE2W	Input Buffer with failsafe Schmitt 50kΩ Pull-down	6 (1)	1-70
FDS1W	Input Buffer Schmitt 50kΩ Pull-down	6 (1)	1-4
FDS2W	Input Buffer Schmitt 50kΩ Pull-down	6 (1)	1-68
FE01	Low-noise Output Buffer 9mA	5 (1)	1-14
FE02	Low-noise Output Buffer 12mA	5 (1)	1-14
FE03	Low-noise Output Buffer 18mA	5 (1)	1-14
FE04	Low-noise Output Buffer 6mA	5 (1)	1-14
FE06	Low-noise Output Buffer 24mA	5 (1)	1-14
FE09	Low-noise Output Buffer 3mA	5 (1)	1-14
FI01	Input Buffer	3 (1)	1-4
FI02	Input Buffer	3 (1)	1-68
FIA1	Input Buffer with failsafe	3 (1)	1-6
FIA2	Input Buffer with failsafe	3 (1)	1-70
FID1	Input Buffer 50kΩ Pull-down	3 (1)	1-4
FID2	Input Buffer 50kΩ Pull-down	3 (1)	1-68
FIE1W	Input Buffer with failsafe Schmitt	6 (1)	1-6
FIE2W	Input Buffer with failsafe Schmitt	6 (1)	1-70
FIS1W	Input Buffer Schmitt	6 (1)	1-4
FIS2W	Input Buffer Schmitt	6 (1)	1-68
FIU1	Input Buffer 50kΩ Pull-up	3 (1)	1-4
FIU2	Input Buffer 50kΩ Pull-up	3 (1)	1-68
FIW1	Input Buffer 5kΩ Pull-up	3 (1)	1-4
FIW2	Input Buffer 5kΩ Pull-up	3 (1)	1-68
FN11	Input Buffer with EN(AND)	6 (1)	1-8
FN12	Input Buffer with EN(AND)	7 (1)	1-72
FN13	Input Buffer with EN(OR)	4 (1)	1-10
FN14	Input Buffer with EN(OR)	4 (1)	1-74
FN21	Input Buffer with EN(AND) 50kΩ Pull-down	6 (1)	1-8
FN22	Input Buffer with EN(AND) 50kΩ Pull-down	7 (1)	1-72
FN23	Input Buffer with EN(OR) 50kΩ Pull-down	4 (1)	1-10
FN24	Input Buffer with EN(OR) 50kΩ Pull-down	4 (1)	1-74
FO01	Output Buffer 9mA	4 (1)	1-12
FO02	Output Buffer 12mA	12 (1)	1-12
FO03	Output Buffer 18mA	12 (1)	1-12
FO04	Output Buffer 6mA	4 (1)	1-12
FO06	Output Buffer 24mA	12 (1)	1-12
FO09	Output Buffer 3mA	4 (1)	1-12
FUS1W	Input Buffer Schmitt 50kΩ Pull-up	6 (1)	1-4
FUS2W	Input Buffer Schmitt 50kΩ Pull-up	6 (1)	1-68
FWS1W	Input Buffer Schmitt 5kΩ Pull-up	6 (1)	1-4

Block	Function	Cells (I/O)	Page
FWS2W	Input Buffer Schmitt 5kΩ Pull-up	6 (1)	1-68
L101	Inverter Single Out, Low Power	1 (-)	2-10
L111	Buffer Single Out, Low Power	1 (-)	2-12
L202	2-Input NOR Low Power	1 (-)	2-22
L205	5-Input NOR Low Power	4 (-)	2-28
L208	8-Input NOR Low Power	7 (-)	2-32
L212	2-Input OR Low Power	2 (-)	2-34
L213	3-Input OR Low Power	2 (-)	2-36
L214	4-Input OR Low Power	3 (-)	2-38
L215	5-Input OR Low Power	4 (-)	2-40
L216	6-Input OR Low Power	4 (-)	2-42
L218	8-Input OR Low Power	6 (-)	2-44
L302	2-Input NAND Low Power	1 (-)	2-50
L303	3-Input NAND Low Power	2 (-)	2-52
L304	4-Input NAND Low Power	2 (-)	2-54
L312	2-Input AND Low Power	2 (-)	2-62
L313	3-Input AND Low Power	2 (-)	2-64
L314	4-Input AND Low Power	3 (-)	2-66
L315	5-Input AND Low Power	4 (-)	2-68
L316	6-Input AND Low Power	4 (-)	2-70
L318	8-Input AND Low Power	5 (-)	2-72
L421	1-2-Input AND-NOR Low Power	2 (-)	2-78
L423	1-3-Input AND-NOR Low Power	2 (-)	2-82
L424	2-2-Input AND-NOR Low Power	2 (-)	2-84
L429	2-2-2-Input AND-NOR Low Power	6 (-)	2-90
L430	1-4-Input OR-NAND Low Power	4 (-)	2-118
L431	1-2-Input OR-NAND Low Power	2 (-)	2-120
L432	1-1-2-Input OR-NAND Low Power	2 (-)	2-122
L439	1-5-Input OR-NAND Low Power	5 (-)	2-128
L441	1-5-Input AND-NOR Low Power	5 (-)	2-94
L444	4-4-4-Input AND-NOR Low Power	8 (-)	2-96
L446	1-1-1-2-Input AND-NOR Low Power	4 (-)	2-98
L447	1-1-1-3-Input AND-NOR Low Power	5 (-)	2-100
L448	1-1-2-2-Input AND-NOR Low Power	5 (-)	2-102
L450	2-4-Input OR-NAND Low Power	5 (-)	2-130
L451	4-4-Input OR-NAND Low Power	7 (-)	2-132
L452	1-1-3-Input OR-NAND Low Power	4 (-)	2-134
L453	1-1-4-Input OR-NAND Low Power	5 (-)	2-136
L459	1-1-1-3-Input OR-NAND Low Power	5 (-)	2-142
L460	3-3-3-Input AND-NOR Low Power	6 (-)	2-106
L464	1-1-4-Input AND-NOR Low Power	5 (-)	2-108
L491	1-2-3-Input OR-NAND Low Power	5 (-)	2-146
L493	3-3-3-Input OR-NAND Low Power	6 (-)	2-148

Block	Function	Cells (I/O)	Page
L511	2-Input Exclusive OR Low Power	3 (-)	2-158
L512	2-Input Exclusive NOR Low Power	3 (-)	2-162
L516	3-Input Exclusive OR Low Power	6 (-)	2-160
L517	3-Input Exclusive NOR Low Power	7 (-)	2-164
L531	3-State Buffer with EN, Low Power	4 (-)	2-182
L532	3-State Buffer with ENB, Low Power	4 (-)	2-182
L560	2 to 4 Decoder Positive Out, Low Power	6 (-)	2-186
L561	2 to 4 Decoder Negative Out, Low Power	6 (-)	2-186
L565	2 to 1 Multiplexer (Positive Out) Low Power	3 (-)	2-190
L571	2 to 1 Multiplexer (Positive Out) with ENB, Low Power	4 (-)	2-190
L572	Quad 2 to 1 Multiplexer (Negative Out) with ENB, Low Power	15 (-)	2-198
L601	D-Latch Q Out, Low Power	4 (-)	2-218
L602	D-Latch with R Q Out, Low Power	5 (-)	2-222
L603	D-Latch with RB Q Out, Low Power	5 (-)	2-226
L604	D-Latch (GB) Q Out, Low Power	4 (-)	2-236
L605	D-Latch (GB) with RB Q Out, Low Power	5 (-)	2-240
L606	BScan D-Latch with SB Q Out, Low Power	5 (-)	4-30
L641	D-F/F Q Out, Low Power	6 (-)	2-248
L644	D-F/F with R, S Q Out, Low Power	8 (-)	2-254
L645	D-F/F with RB Q Out, Low Power	7 (-)	2-256
L647	D-F/F with RB, SB Q Out, Low Power	8 (-)	2-260
L661	D-F/F (CB) Q Out, Low Power	6 (-)	2-262
L667	D-F/F (CB) with RB, SB Q Out, Low Power	8 (-)	2-268
L744	T-F/F with R, S Q Out, Low Power	7 (-)	2-308
L747	T-F/F with RB, SB Q Out, Low Power	7 (-)	2-312
L767	T-F/F (TB) with RB, SB Q Out, Low Power	7 (-)	2-318
OSI1	Oscillator Input Buffer	0 (1)	1-116
OSI2	Oscillator Input Buffer for Enable	0 (1)	1-118
OSI4	Oscillator Input Buffer for OSO9	0 (1)	1-120
OSO1	Oscillator Output Buffer (Internal Feedback Resistor)	0 (1)	1-122
OSO7	Oscillator Output Buffer (for Enable Type)	0 (1)	1-124
OSO9	Oscillator Output Buffer (External Feedback Resistor)	0 (1)	1-126
S000	Scan D-F/F with R, S, 2 to 1 Selector	12 (-)	3-4
S002	Scan D-F/F with 2 to 1 Selector	10 (-)	3-6
S003	Scan D-F/F with 2 to 1 Selector, High Speed	11 (-)	3-8
S050	Scan D-F/F with R, S, Hold, 2 to 1 Selector	16 (-)	3-10
S052	Scan D-F/F with Hold, 2 to 1 Selector	14 (-)	3-12
S100	Scan JK-F/F with R, S, D-F/F Function	14 (-)	3-14
S102	Scan JK-F/F with D-F/F Function	12 (-)	3-16
S150	Scan JK-F/F with R, S, Hold, D-F/F Function	18 (-)	3-18
S152	Scan JK-F/F with Hold, D-F/F Function	16 (-)	3-20
S201	Scan D-Latch with R, D-F/F Function	13 (-)	3-22
S202	Scan D-Latch with D-F/F Function	12 (-)	3-24

Block	Function	Cells (I/O)	Page
S204	Scan D-Latch with D-F/F Function, High Speed	12 (-)	3-26
S301	Scan D-Latch with R, Special Function	8 (-)	3-28
S302	Scan D-Latch with Special Function	7 (-)	3-30
S303	Scan D-Latch with Special Function, High Speed	7 (-)	3-32
SBCJ	BScan TAP Macro	262 (-)	4-4
SBCK	BScan TAP Controller	392 (-)	4-48
SBCL	BScan TAP Macro with NEC Scan	315 (-)	4-6
SBD1	BScan Selector	4 (-)	4-32
SBM4	BScan Instruction Register (Internal Circuit)	46 (-)	4-50
SBM5	BScan Instruction Register	140 (-)	4-52
SBM6	BScan Instruction Decoder	24 (-)	4-54
SBMC	BScan Instruction Decoder with NEC Scan	37 (-)	4-56
SBR1	BScan Shift Register	8 (-)	4-34
SBS3	BScan Bypass Register	26 (-)	4-58
SBZ1	BScan Level Generator (CLANP)	1 (-)	4-12
SCD1	Clock Distributor	8 (-)	3-66
SCDC	Clock Distributor with Test (Positive Clock)	2 (-)	3-68
SCDD	Clock Distributor with Test (Negative Clock)	2 (-)	3-70
SCI1	Common Input	2 (-)	3-90
SCKG	Clock Generator	16 (-)	3-88
SCO1	Common Output	4 (-)	3-92
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