Application Note

RZ/T2H and RZ/N2H Groups

PCB Design Guide for LPDDR4

RZ/T Series for Real-Time Control
RZ/N Series for Industrial Network
RZ Family
64-Bit & 32-Bit Arm®-Based High-End MPUs

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Contents

1. Overview

This guide provides a PCB design method that takes into account fulfilling verification items in “RZ/T2H and RZ/N2H Groups PCB verification guide for LPDDR4” (R01AN7260EJ****).

Renesas provides reference design of LPDDR4 which is fully verified according to verification guide. PCB structure and topologies which are used in this guide refer to reference design. You can copy the PCB layout of the reference design. However, all the verification item listed in the verification guide should be verified through SI and PDN simulations basically, even if you copied the data.

The following documents apply to these LSI. Make sure to refer to the latest versions of these documents. Last four digits of document number (described as ****) indicate version information of each document. The latest versions of the documents listed are obtained from the Renesas Electronics Web site.

Table 1.1 List of reference documents

Document Type	Description	Document Title	Document No.
User’s manual for Hardware	Hardware specifications (pin assignments, peripheral function specifications, electrical characteristics, timing charts) and operation description	RZ/T2H and RZ/N2H Groups User’s Manual: Hardware	R01UH1039EJ****
Application Note	PCB verification guide for LPDDR4	RZ/T2H and RZ/N2H Groups PCB Verification Guide for LPDDR4	R01AN7260EJ****

2. Basic Information

2.1 PCB structure

This guide is for an 8-layer board with through-hole vias.

Each layer's assignment signal or power (GND) for an 8-layer board is shown in **Figure 2.1**, the numerical value for each layer indicates its thickness.

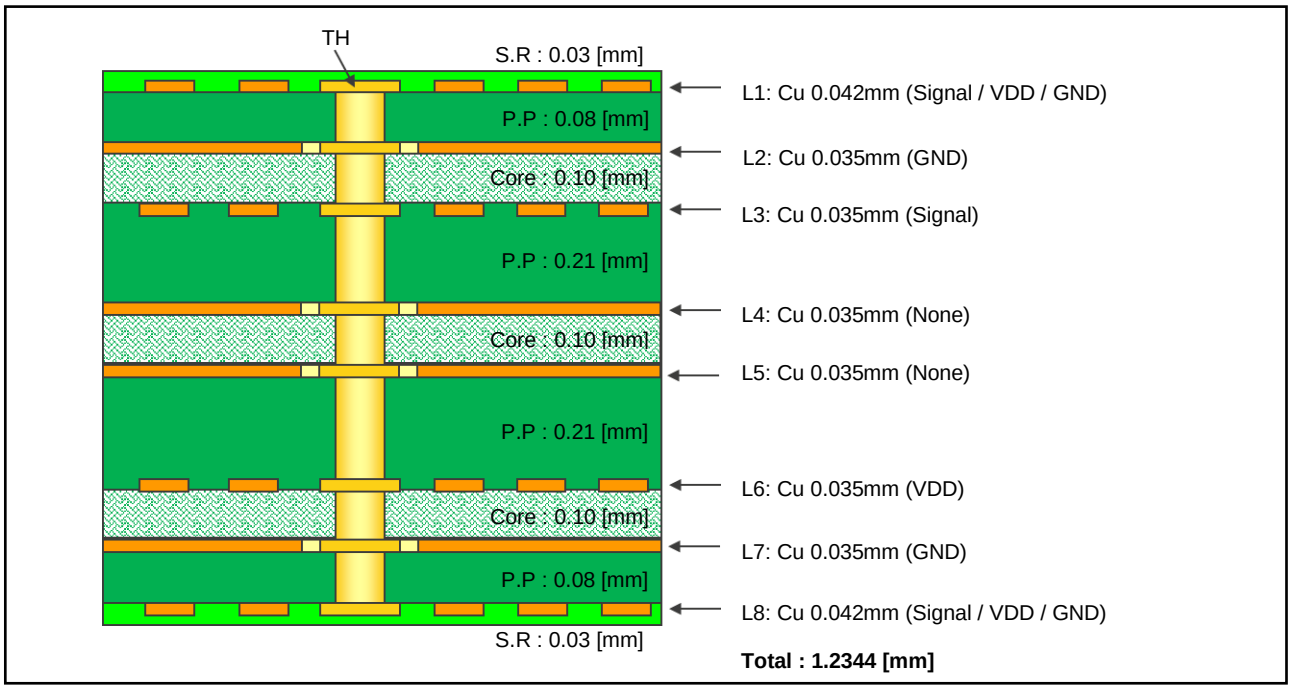


Figure 2.1 PCB structure

- 8-Layer Through-hole
  Base Material : FR-4
  [Dielectric constant : Relative permittivity / Loss tangent]
  Solder Resist (S.R) : 3.7/0.017 (for 1GHz)
  Prepreg (P.P) 0.08 mm: 4.2/0.012 (for 1GHz)
  Prepreg (P.P) 0.21 mm: 4.6/0.010 (for 1GHz)
  Core : 4.6/0.010 (for 1GHz)

2.2 Design rules

- VIA specifications

  VIA diameter : 0.25mm
  Surface land diameter : 0.5mm
  Internal layer land diameter : 0.5mm
  Internal layer clearance diameter : 0.7mm
  VIA center - VIA center : 0.8mm (LSI)
  VIA land – VIA land : 0.3mm (LSI)
  VIA center – VIA center : 0.65mm (DRAM)
  VIA land – VIA land : 0.15mm (DRAM)

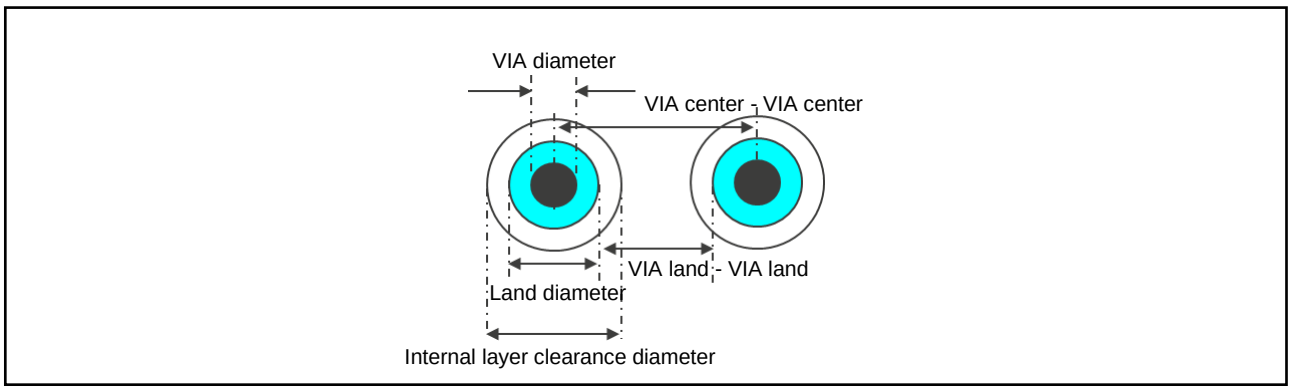


Figure 2.2 VIA specifications

- Minimum trace width : 0.1mm
- Minimum space

  Wiring – Wiring : 0.1mm
  Wiring – VIA : 0.1mm
  Wiring – BGA land : 0.1mm
  VIA – BGA land : 0.1mm
  Wiring – BGA resist : 0.05mm

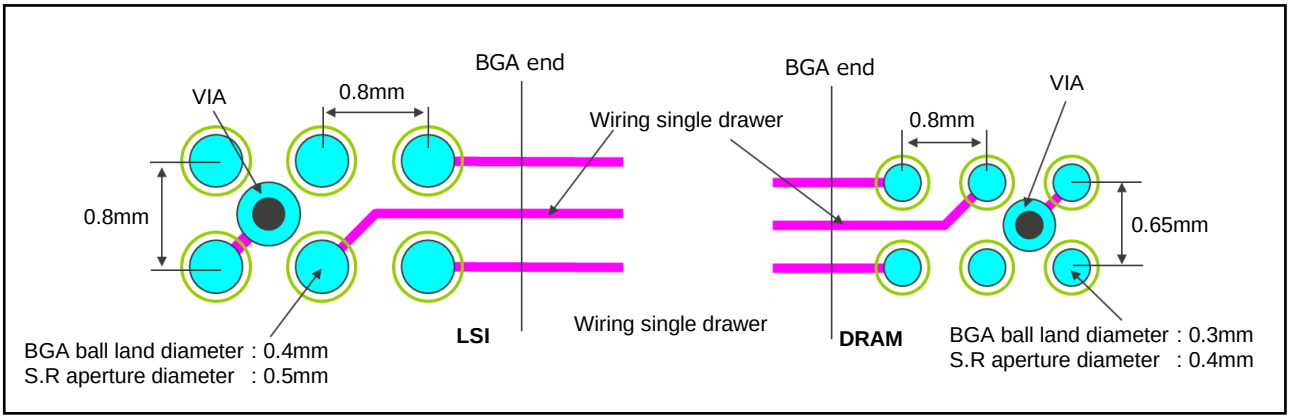


Figure 2.3 BGA land diameter (PAD dimension)

3. Net swap

3.1 Net swap restriction

Some of the external pins are swappable. No register settings are required since DDR parameter generation tool (gen_tool) provides the swap setting.

As for the detail of external pin swizzling, refer to “RZ/T2H and RZ/N2H Groups User’s Manual: Hardware, 57.4.1 External Pin Swizzling” (R01UH1039EJ****) and DDR parameter generation tool.

3.2 Example of swizzling for RZ/T2H

Table 3.1 shows an example of swizzling supported by reference design PCB layout data for RZ/T2H.

Table 3.1 Example of swizzling for RZ/T2H (1 of 3)

RZ/T2H		LPDDR4		Remark
Pin No	Signal name	Pin No	Signal name	
K2	DDR_DQA0	F11	DQA11	—
K3	DDR_DQA1	F9	DQA12	—
K1	DDR_DQA2	E11	DQA10	—
K4	DDR_DQA3	E9	DQA13	—
J1	DDR_DQA4	C9	DQA14	—
H2	DDR_DQA5	B9	DQA15	—
H1	DDR_DQA6	C11	DQA9	—
J4	DDR_DQA7	B11	DQA8	—
F2	DDR_DQA8	B4	DQA7	—
E2	DDR_DQA9	C2	DQA1	—
G3	DDR_DQA10	C4	DQA6	—
F3	DDR_DQA11	E2	DQA2	—
E1	DDR_DQA12	F2	DQA3	—
E4	DDR_DQA13	B2	DQA0	—
F4	DDR_DQA14	F4	DQA4	—
G1	DDR_DQA15	E4	DQA5	—
J3	DDR_DMIA0	C10	DMIA1	—
G4	DDR_DMIA1	C3	DMIA0	—
K5	DDR_DQSA_T0	D10	DQSA_T1	—
G5	DDR_DQSA_T1	D3	DQSA_T0	—
J5	DDR_DQSA_C0	E10	DQSA_C1	—
F5	DDR_DQSA_C1	E3	DQSA_C0	—

Table 3.1 Example of swizzling for RZ/T2H (2 of 3)

RZ/T2H		LPDDR4		Remark
Pin No	Signal name	Pin No	Signal name	
U4	DDR_DQB0	U9	DQB12	—
V2	DDR_DQB1	V9	DQB13	—
V1	DDR_DQB2	U11	DQB11	—
V4	DDR_DQB3	Y9	DQB14	—
W2	DDR_DQB4	V11	DQB10	—
Y3	DDR_DQB5	AA11	DQB8	—
Y1	DDR_DQB6	AA9	DQB15	—
W3	DDR_DQB7	Y11	DQB9	—
AA1	DDR_DQB8	V4	DQB5	—
AB2	DDR_DQB9	Y2	DQB1	—
AB4	DDR_DQB10	AA2	DQB0	—
AC4	DDR_DQB11	AA4	DQB7	—
AC1	DDR_DQB12	U2	DQB3	—
AC3	DDR_DQB13	V2	DQB2	—
AB1	DDR_DQB14	Y4	DQB6	—
AA3	DDR_DQB15	U4	DQB4	—
W4	DDR_DMIB0	Y10	DMIB1	—
AB3	DDR_DMIB1	Y3	DMIB0	—
V5	DDR_DQSB_T0	W10	DQSB_T1	—
AA5	DDR_DQSB_T1	W3	DQSB_T0	—
W5	DDR_DQSB_C0	V10	DQSB_C1	—
AB5	DDR_DQSB_C1	V3	DQSB_C0	—

Table 3.1 Example of swizzling for RZ/T2H (3 of 3)

RZ/T2H		LPDDR4		Remark
Pin No	Signal name	Pin No	Signal name	
N1	DDR_CKA_T	J8	CKA_T	No remapping
M1	DDR_CKA_C	J9	CKA_C	No remapping
M6	DDR_CKEA0	J4	CKEA0	No remapping
L6	DDR_CKEA1	J5	CKEA1	No remapping
M4	DDR_CSA0	H4	CSA0	No remapping
M5	DDR_CSA1	H3	CSA1	No remapping
P4	DDR_CAA0	H11	CAA4	—
L2	DDR_CAA1	H2	CAA0	—
N3	DDR_CAA2	H9	CAA2	—
M2	DDR_CAA3	J2	CAA1	—
M3	DDR_CAA4	H10	CAA3	—
N5	DDR_CAA5	J11	CAA5	—
R1	DDR_CKB_T	P8	CKB_T	No remapping
T1	DDR_CKB_C	P9	CKB_C	No remapping
R2	DDR_CKEB0	P4	CKEB0	No remapping
P2	DDR_CKEB1	P5	CKEB1	No remapping
T6	DDR_CSB0	R4	CSB0	No remapping
U6	DDR_CSB1	R3	CSB1	No remapping
P3	DDR_CAB0	R9	CAB2	—
T2	DDR_CAB1	R2	CAB0	—
T4	DDR_CAB2	R10	CAB3	—
U1	DDR_CAB3	R11	CAB4	—
U3	DDR_CAB4	P11	CAB5	—
T5	DDR_CAB5	P2	CAB1	—
P7	DDR_RESET_N	T11	RESET_N	No remapping
R8	DDR_ZN	—	—	No remapping
R7	DDR_DTEST	—	—	No remapping
P8	DDR_ATEST	—	—	No remapping

4. Common guidelines

4.1 Component placement

Figure 4.1 shows component placement assumptions, U1 indicates LSI and M1 indicates DRAM.

- 2RANK case : Place U1 and M1 on L1.

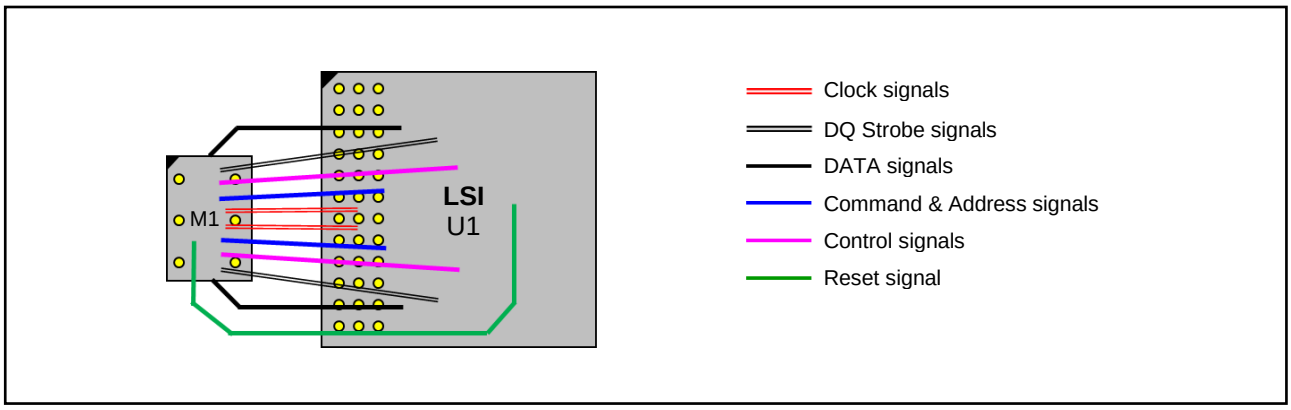


Figure 4.1 Component placement assumptions

4.2 IO Power supply layout guideline

The IO power supply (DDR_VDDQ) should be formed on L6 as a plane and should be large enough to cover all signal traces and DRAM. As shown **Figure 4.2**, place one VIA for every one or two PADs of the IO power supply near the LSI and place a capacitor per number of VIAs. Use GND PADs near DDR_VDDQ place VIAs for GND using the same rule. To shorten the current return path for the IO power supply, consider placing capacitors with the shortest possible trace to the IO power supply and GND. Verify the layout using PDN analysis and check if the results satisfy the specification described in the verification guide.

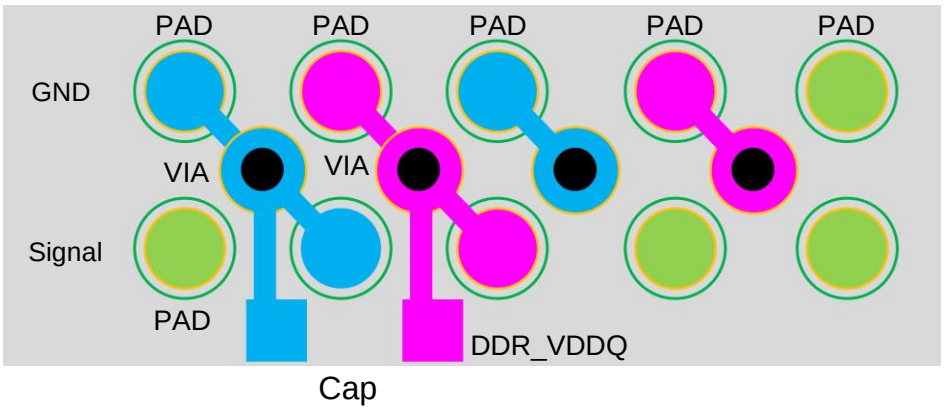


Figure 4.2 IO Power supply layout near the LSI

5. Topology

As for the detail of skew between wires for each signal, refer to “RZ/T2H and RZ/N2H Groups PCB verification guide for LPDDR4, 4.1.1 Skew restrictions” (R01AN7260EJ****).

The PCB configuration of reference design is shown below.

5.1 Topology RZ/T2H

System RANK : Dual

LPDDR4 SDRAM : 64GB

Target Device : MT53E2G32D4DE-046 AIT:C (Z42N QDP)

PCB : 8layers / One to One / Top mounting

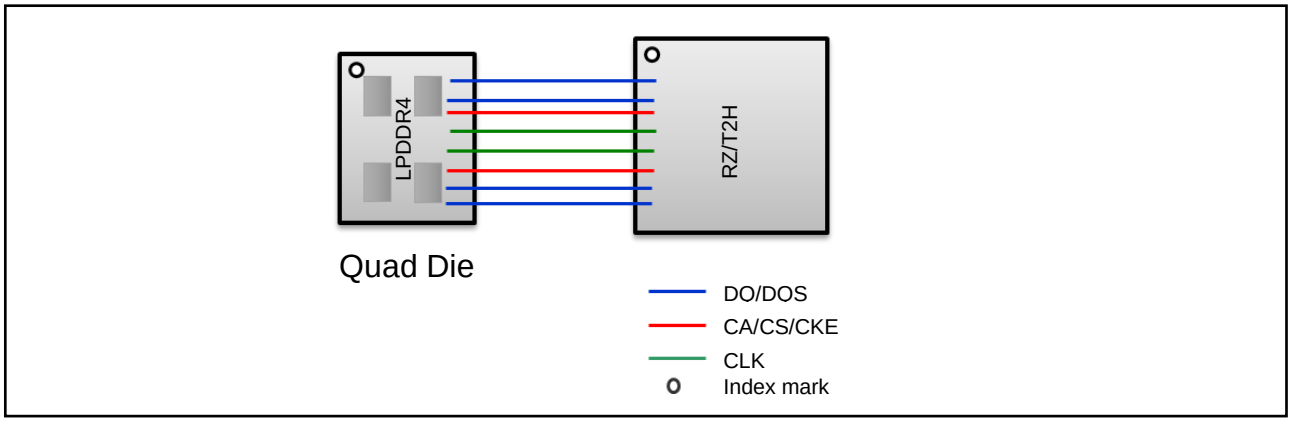


Figure 5.1 PCB configuration

Table 5.1 shows recommended IO setting. Reference design PCB layout data used 2Rank for DRAM model.

Table 5.1 Recommended IO setting

Signal	LSI		DRAM		Damping resistance	Number of Rank
	Driver setting	ODT	Driver setting	ODT		
CLK	60Ω	—	—	60Ω	—	1
				60Ω (Rank0 side) OFF (Rank1 side)		2
CA	60Ω	—	—	60Ω	—	1
				60Ω (Rank0 side) OFF (Rank1 side)		2
CS	60Ω	—	—	60Ω	—	1, 2
CKE	FIXED	—	—	—	22Ω	1, 2
RESET	FIXED	—	—	—	—	1, 2
DQ, DQS (Write)	40Ω	OFF	OFF	40Ω	—	1
				40Ω (access side) OFF (non-access side)		2
DQ, DQS (Read)	OFF	40Ω	RONPD = 40Ω LSI ODT = 40Ω VOH = VDDQ / 3	OFF	—	1
				OFF (access side) OFF (non-access side)		2

5.1.1 CLK topology

Figure 5.2 shows CLK topology.
L1 indicates the trace layers, a0 to a0# indicate the trace length.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#
2. Keep 0.25mm or more between other signal traces.
3. Verify the layout using SI simulation and check its result to satisfy the timing and waveform restrictions in the verification guide. (Mandatory)

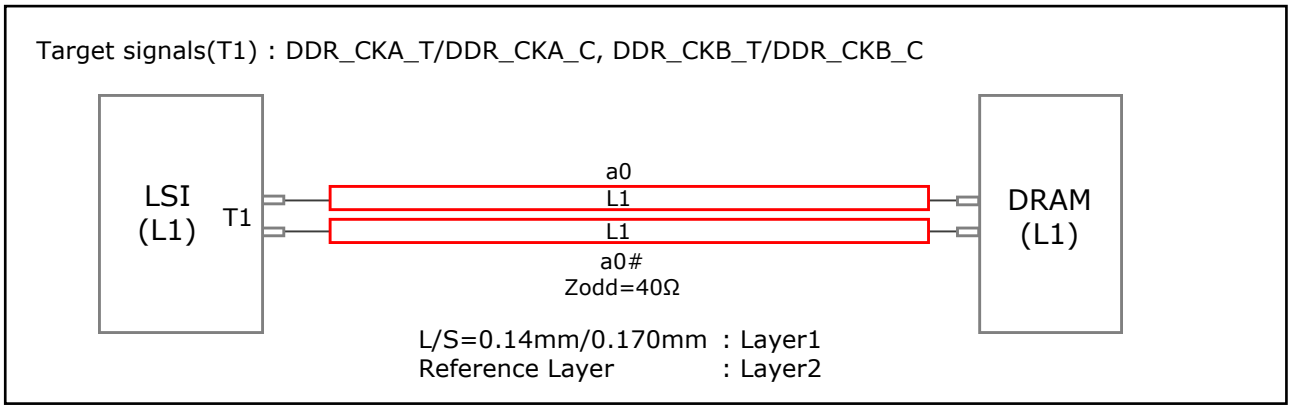


Figure 5.2 CLK topology

5.1.2 CA topology

Figure 5.3 shows CA topology.
L1, L3 and L8 indicate the trace layers, a0 to c2 indicate the trace length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 50Ω±10%.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation and check its result to satisfy the timing and waveform restrictions in the verification guide. (Mandatory)

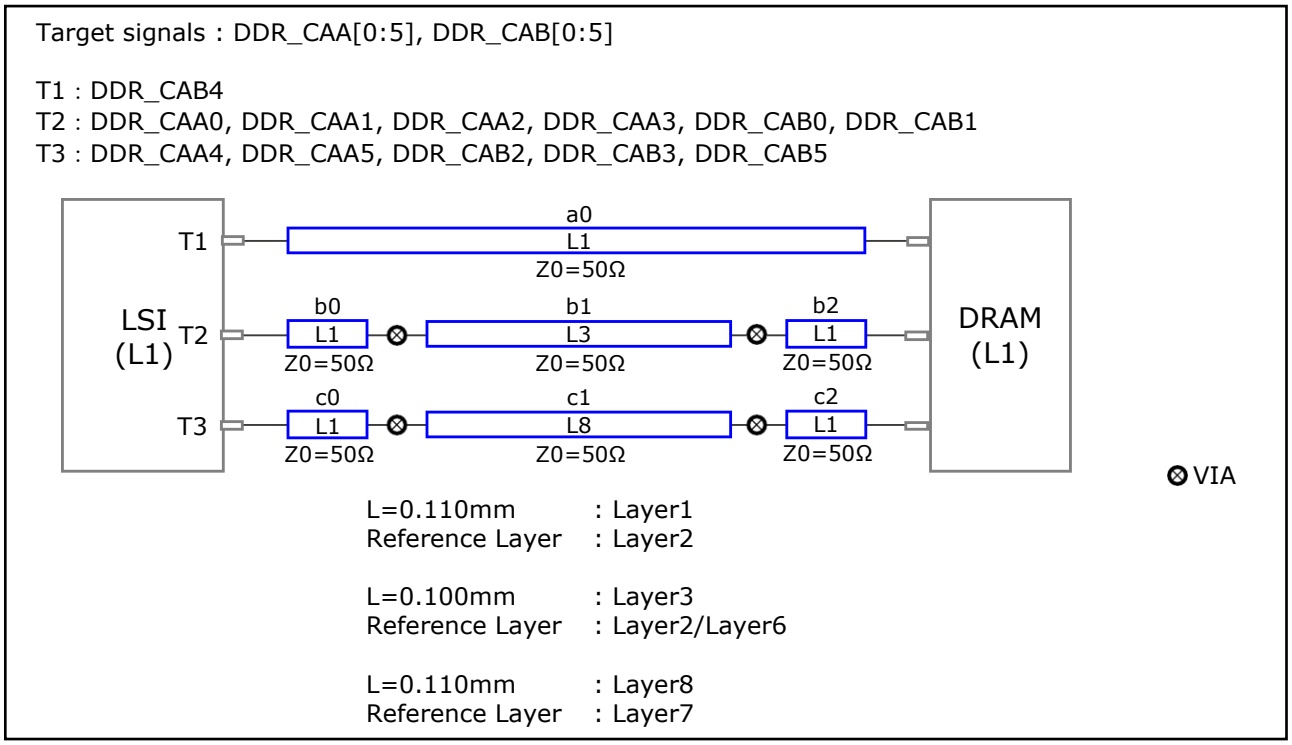


Figure 5.3 CA topology

5.1.3 CTRL topology

Figure 5.4 shows CTRL topology.
L1, L3 and L8 indicate the trace layers, a0 to c3 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 50Ω±10%.

Design control signals following the topology described in this figure.

1. Verify the layout using SI simulation and check its result to satisfy the timing and waveform restrictions in the verification guide. (Mandatory)

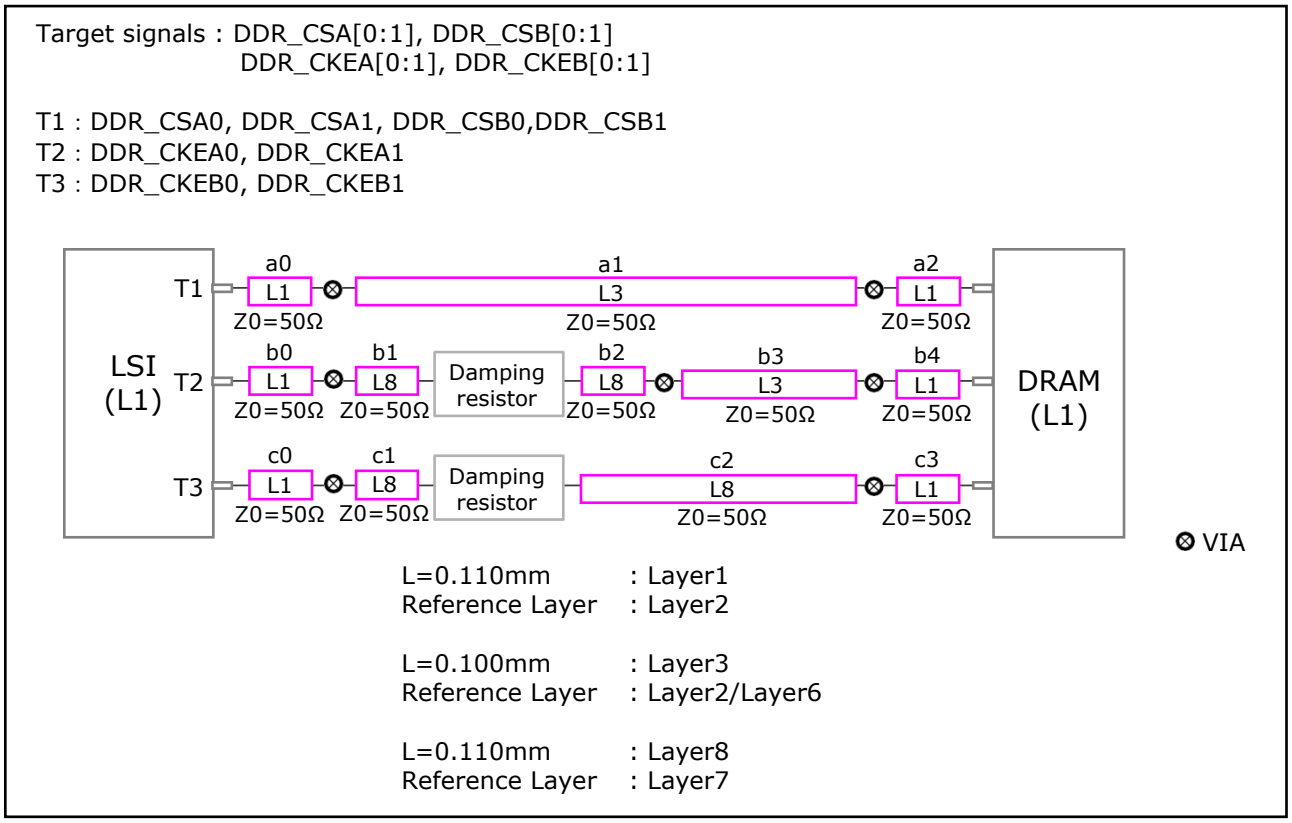


Figure 5.4 CTRL topology

5.1.4 RESET topology

Figure 5.5 shows RESET topology.
L1 and L3 indicate trace layers, a0 to a2 indicate the trace length. " ⊗ " are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 50Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Verify the layout using SI simulation and check its result to satisfy the timing and waveform restrictions in the verification guide. (Mandatory)

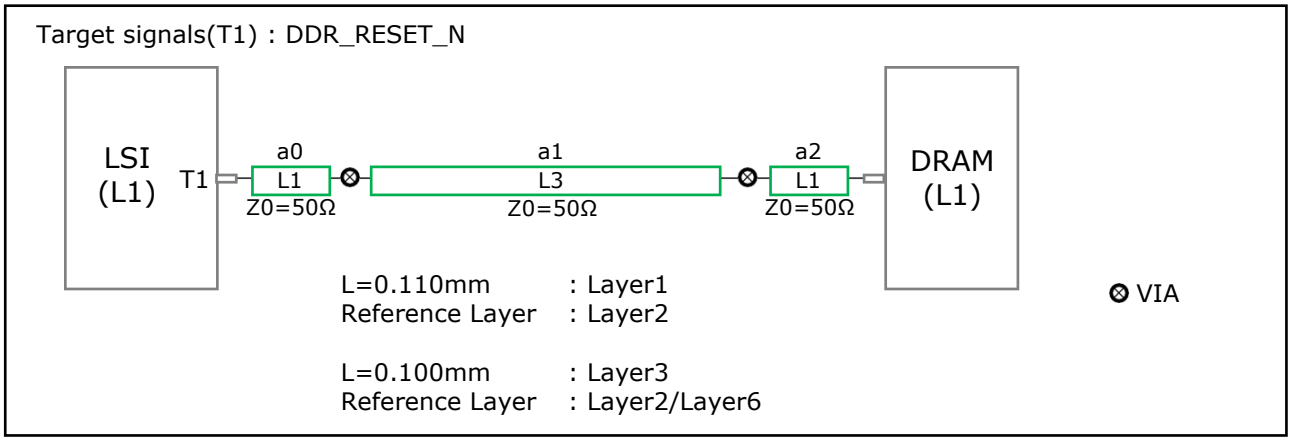


Figure 5.5 RESET topology

5.1.5 DQS/DQ topology

Figure 5.6 and **Figure 5.7** show DQS/DQ topology.
L1, L3 and L8 in the figure below indicate the trace layers, a0 to b2 indicate the trace length. " ⊗ " are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 45Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#
2. Keep 0.25mm or more between other signal traces.
3. Verify the layout using SI simulation and check its result to satisfy the timing and waveform restrictions in the verification guide. (Mandatory)

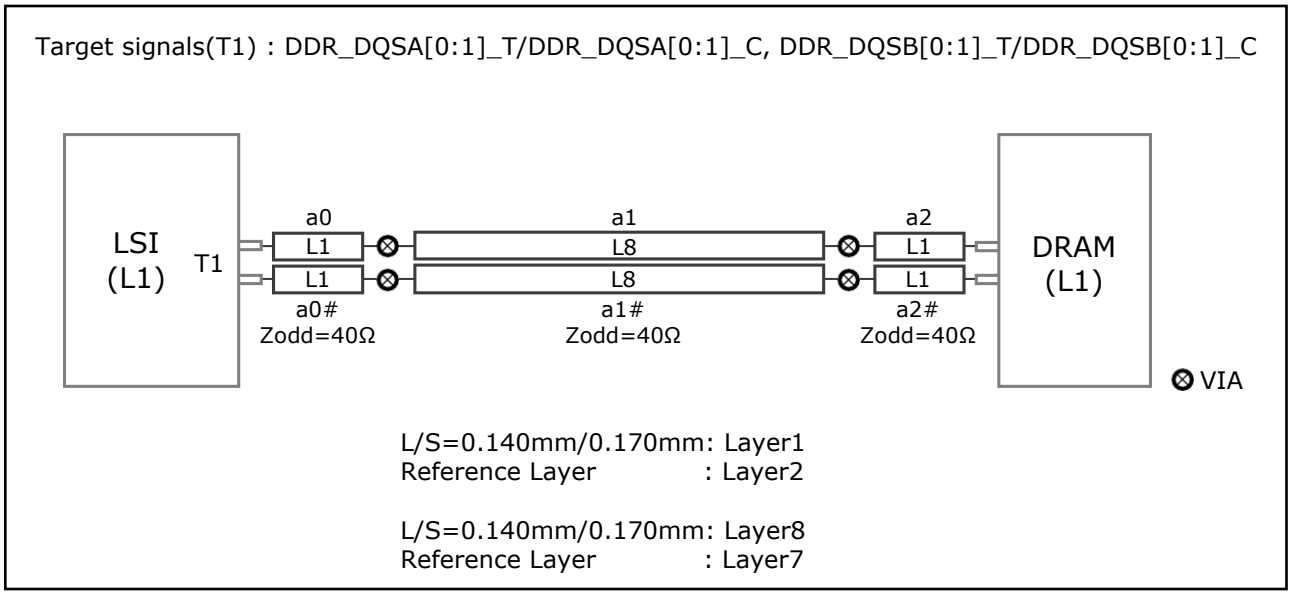
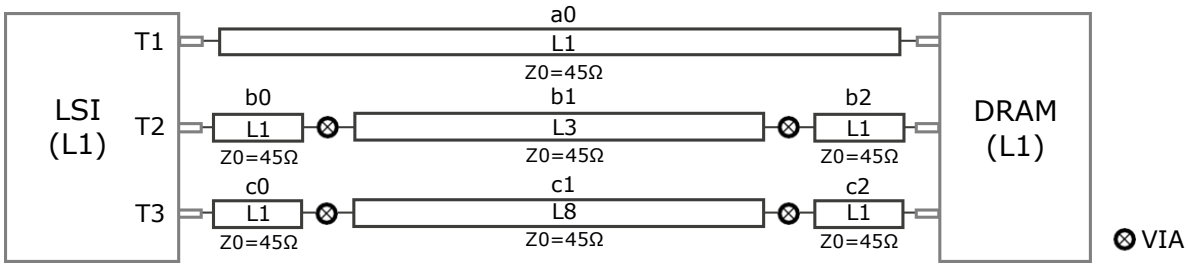


Figure 5.6 DQS topology

Target signals : DDR_DMIA[0:1], DDR_DQA[0:15],DDR_DMIB[0:1],DDR_DQB_[0:15]

T1 : DDR_DQA1, DDR_DQA5, DDR_DQA6, DDR_DQA7, DDR_DQA9, DDR_DQA10, DDR_DQA11
DDR_DQA15, DDR_DQB1, DDR_DQB5, DDR_DQB6, DDR_DQB9, DDR_DQB10, DDR_DQB11
DDR_DQB15
T2 : DDR_DQA0, DDR_DQA2, DDR_DQA3, DDR_DQA4, DDR_DMIA0, DDR_DQA8, DDR_DQA12
DDR_DQA13, DDR_DQA14, DDR_DQB0, DDR_DQB2, DDR_DQB3, DDR_DQB4, DDR_DQB7
DDR_DMIB0, DDR_DQB8, DDR_DQB12, DDR_DQB13, DDR_DQB14, DDR_DMIB1
T3 : DDR_DMIA1



L=0.135mm : Layer1
Reference Layer : Layer2

L=0.130mm : Layer3
Reference Layer : Layer2/Layer6

L=0.135mm : Layer8
Reference Layer : Layer7

Figure 5.7 DQ topology

6. Handling of Other Pins

Handling of Other Pins is as follows.

- DDR_ZN : 120 (±1%) Ω external resistor must be connected between DDR_ZN and VSS (GND).
- DDR_DTEST, DDR_ATEST : Keep these pins open.

REVISION HISTORY	RZ/T2H and RZ/N2H Groups PCB Design Guide for LPDDR4

Rev.	Date	Description	
		Page	Summary
0.70	Mar 26, 2024	—	First Preliminary Edition issued
1.00	Sep 30, 2024	5	1 Overview: Description about reference design, added.
		8	3.1 Net swap restriction: Description about DDR parameter generation tool, added.

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