RX family, H8S family

H8S to RX Migration Guide: Timer(GPTW)

Introduction

This application note explains how to migrate from the TPU of the H8S Family to the GPTW of the RX Family.

Target Device

- RX Family
- H8S Family

An example of migrating from the H8S Family to the RX Family is presented, with the RX Family represented by the RX261 Group and the H8S Family represented by the H8S/2378 Group. When using this application note with other microcontrollers, appropriate changes should be made to match the specifications of the microcontroller used and thorough evaluation should be performed.

Devices on Which Operation Has Been Confirmed

- RX Family: RX261
- H8S Family: H8S/2378

Some terminology differs between the RX Family and the H8S Family. Differences in timer-related terminology are listed in the table below.

Table Differences in Terminology between RX Family and H8S Family

Item	H8S family	RX family
Names of timer modules	16-bit timer pulse unit (TPU) Watchdog timer (WDT)	General PWM Timer (GPTW) Watch Dog Timer (WDTA)
Channel names (TPU)	Channel m (m: channel number)	GPTWm (m: count of channel)
Register names (TGRA)	TGRA_m (m: channel number)	GPTWm.GTCCRn (m: channel number, n: A to F)
Pin names (TIOCA)	TIOCAm (m: channel number)	GTETRGA to D、 GPTWm.GTIOC0A to 7A、 GPTWm.GTIOC0B to 7B (m: channel number) GTIU、GTIV、GTIW GTOUUP、GTOULO、GTOVUP GTOVLO、GTOWUP、 GTOWLO
Peripheral function operating clock	ϕ	Peripheral module clock PCLKA(GPTW)
Timer operating clock (count clock)	Counter input clock	Count Clock

Contents

1. Timer Comparison

1.1 Timer Functions of Each Microcontroller

Table 1.1 lists points of difference between the timer functions of the H8S/2378 Group and RX261 Group.

Table 1-1 Points of Difference between Timer Functions of H8S/2378 Group and RX261 Group

H8S (H8S/2378)	RX (RX261)
8-bit timer (TMR)	8-bit timer (TMR)
16-bit timer pulse unit (TPU)	General PWM timer (GPTWa)
Not available	GPTW Port Output Enable (POEGc)
	Compare match timer (CMT)
	Low power timer (LPT)
Watchdog timer (WDT)	Watchdog timer (WDTA)
Not available	Independent Watchdog Timer (IWDTa)

As shown in Table 1.1, the following options are available when migrating from the timer functions of the H8S/2378 Group to the RX261 Group:

This document presents points of difference and points requiring caution when switching from TPU to GPTW.

1.2 Comparison of TPU Functions

Table 1.2 lists points of difference between the TPU functions of the H8S/2378 Group and GPTW of the RX261 Group.

Table 1-2 Points of Difference between TPU of H8S/2378 Group and GPTW of RX261 Group

Item	H8S (H8S/2378)	RX (RX261)
Pulse input/output	Maximum 16	Maximum 16 (GTIOCnA/B×8ch n=0,1)
Pulse input	Not available	7(GTERGA to D, GTIU, GTIV, GTIW)
Count clocks	8 clocks per channel	15 clock per channel (PCLKA, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLKA/32, PCLKA/64, PCLKA/128, PCLKA/256, PCLKA/512, PCLKA/1024, GTETRGA, GTETRGB, GTETRGC, GTETRGD)
Available operations	Channel 0 to 5 • Waveform output at compare match. • Input capture function. • Counter clear operation. • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare-match or input capture. • Simultaneous register input/output by synchronous counter operation • Up to 15-phase PWM output in combination with synchronous operation Channel0, 3 • Ability to specify buffer operation. • Channels 1, 2, 4, and 5 Ability to specify phase counting mode Counter clear operation	GPTW0 to 7 • Waveform output at compare match. • Input capture function. • Counter clear operation. • Simultaneous writing to multiple timer counters (GTCNT) • Simultaneous clearing by compare-match or input capture. • Simultaneous register input/output by synchronous counter operation • Up to 16-phase PWM output in combination with synchronous operation • Ability to specify buffer operation. GPTW3 to 7 • Ability to specify phase counting mode. • Sawtooth-wave PWM mode1,3. • Sawtooth-wave one shot pulse mode. • Triangle-wave PWM mode 1 to 3. • GPTW0 to 2 • Automatic Dead Time Setting Function • Sawtooth-wave PWM mode1,2. • Sawtooth-wave one shot pulse mode. • Triangle-wave PWM mode 1 to 3. • complementary PWM mode1 to 4 GPTW3 to 5 • External pulse width measuring function. GPTW0 • PWM Synchronous Output
Interrupt sources	26	64(8 source x 8ch)
Buffer operation	Automatic transfer of register data	Automatic transfer of register data

Item	H8S (H8S/2378)	RX (RX261)
A/D converter trigger generation	A/D converter start triggers can be generated. (Channels 0 to 5)	A/D converter start triggers can be generated (GPTW 0 to 2).
PPG trigger generation	Programmable pulse generator (PPG) output trigger generation is available.	Not available
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2. TPU to GPTW Migration

2.1 Peripheral Functions Used

Table 2-1 lists the peripheral functions and modes used in the TPU on H8S and GPTW on RX261 operation examples.

Table 2-1 Peripheral Functions and Modes Used in TPU and GPTW Operation Examples

No	Operation Example	H8S (H8S/2378)		RX(RX261)		Reference
		Peripheral Function	Mode	Peripheral Function	Mode	
1	Waveform output operation using compare match	TPU	Normal mode	GPTW	Sawtooth- Wave PWM mode1	2.2
2	Input capture operation					2.3
3	PWM mode 1		PWM mode 1			2.4
4	PWM mode 2		PWM mode 2			2.5

2.2 Waveform Output Operation Using Compare Match

Points of difference in compare match operation on the H8S/2378 Group and RX261 Group are described below.

Table 2-2 lists preconditions for compare match operation on using TPU on the H8S/2378 Group and GPTW on the RX261 Group.

Table 2-2 Conditions for compare match operation using H8S TPU and RX GPTW.

Item	Operation Conditions	
	H8S (H8S/2378)	**RX (RX261)**
Peripheral function operating clock	ϕ: 20 MHz	PCLKA: 64MHz
Channels used	Channel 3 of TPU	GPTW0
Channels used	TIOCA3: P20 TIOCB3: P21	GTIOC0A: P22 GTIOC0B: P23
Clearing of TCNT register	None (free-running count operation)	GTCNT register was cleared by GPTW.GTPR compare match.
Pin output	High output at compare match A Low output at compare match B	High output at GPTW0.GTCCRA compare match. Low output at GPTW0.GTCCRB compare match. Initial output : GTIOC0A=Low output GTIOC0B=High output End of period output: GTIOC0A=High output GTIOC0B=Low output

2.2.1 Operation

Figure 2-1 shows an example of waveform output operation on the H8S/2378 Group and RX261 Group.

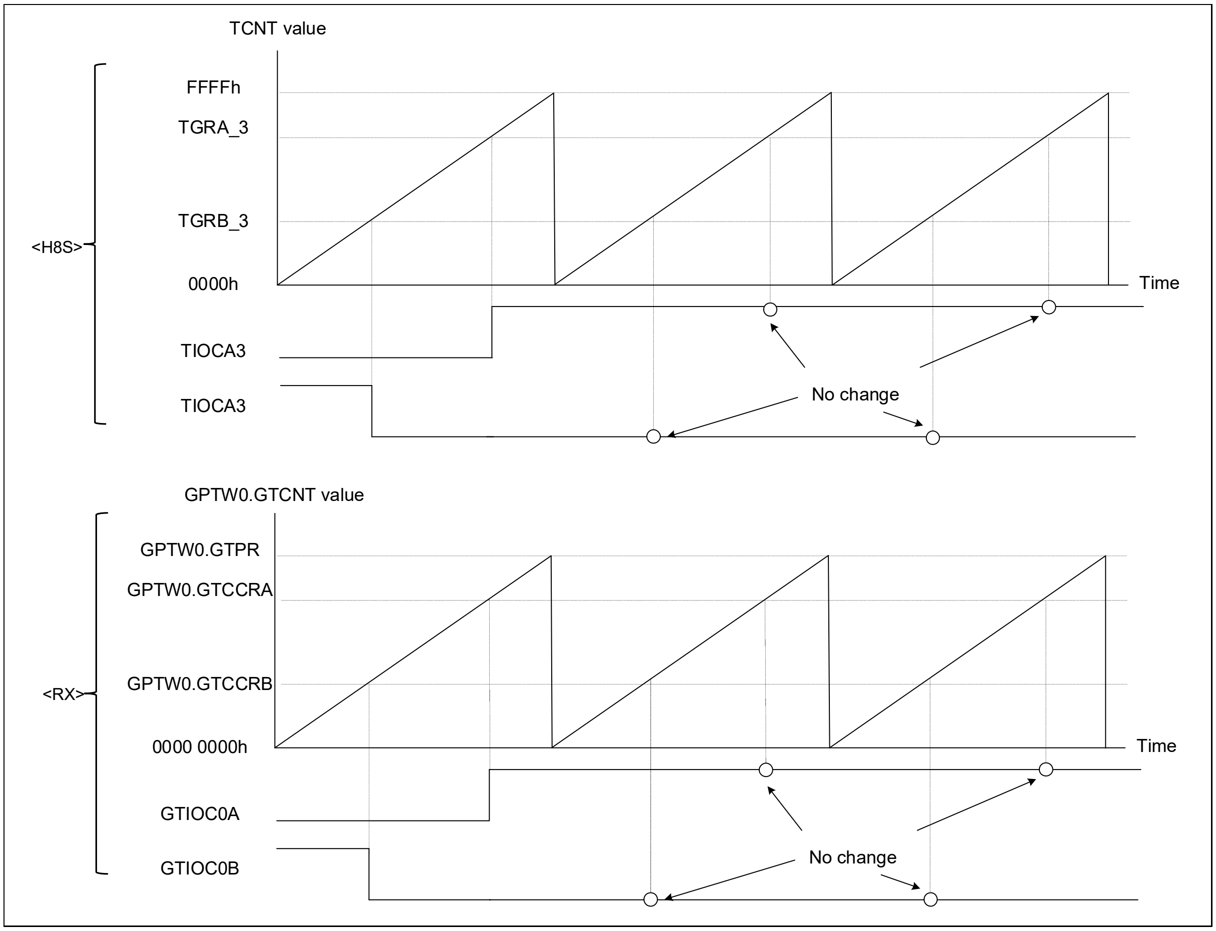

Figure 2-1 Example of Waveform Output Operation on H8S/2378 Group and RX261 Group

2.2.2 Compare match Setting Procedure

Table 2-3 lists procedures for compare match operation using RX261 GPTW.

Table 2-3 procedure for compare match operation using RX261 GPTW.

No.	procedure	RX(RX261)
1.	Cancel module stop state.	SYSTEM.PRCR.WORD = 0xA502; MSTP(GPTW) = 0; SYSTEM.PRCR.WORD = 0xA500;
2.	Disable write protection	GPTW0.GTWP=0x0000A5xx xx: When write protection is enabled, write “0” to each bit.
3.	Disable interrupts.	IEN(GPTW0.GTCIA0) = 0b; IEN(GPTW0.GTCIB0) = 0b; GPTW0.GTINTAD.BIT.GTINTA = 0b; GPTW0.GTINTAD.BIT.GTINTB = 0b;
4.	Stop count operation.	GPTW0.GTCR.BIT.CST = 0b;
5.	Clear counter.	GPTW0.GTCNT = 0x00000000;
6.	Make I/O port function settings.	PORT2.PMR.BIT.B2 = 0b; PORT2.PMR.BIT.B3 = 0b; PORT2.PDR.BIT.B2 = 0b; PORT2.PDR.BIT.B3 = 0b; MPC.PWPR.BIT.B0WI = 0b; MPC.PWPR.BIT.PFSWE = 1b; MPC.P22PFS.BYTE = 0x14; MPC.P23PFS.BYTE = 0x14; MPC.PWPR.BIT.PFSWE = 0b; MPC.PWPR.BIT.B0WI = 1b; PORT2.PMR.BIT.B2 = 1b; PORT2.PMR.BIT.B3 = 1b;
7.	Make operation mode settings.	GTCR.MD[3:0]=0000b
8.	Make count direction.	GPTW0.GTUDDTYC.BIT.UD=1b GPTW0.GTUDDTYC.BIT.UDF=1b;
9.	Make count clock setting.	GPTW0.GTCR.BIT.TPCS = 0000b;
10.	Make end of period settings	GPTW0.GTPR＝0xFFFF;
11.	Make initial value to count settings	GPTW0.GTCNT＝0x0000;
12.	Make GTIOCnm pin settings	GPTW0.GTIOR.BIT.GTIOA = 01010b; GPTW0.GTIOR.BIT.GTIOB = 10101b;
13.	Make GTIOCnm pin output enable settings.	GPTW0.GTIOR.OAE = 1b; GPTW0.GTIOR.OBE = 1b;
14.	Make compare match value settings	GPTW0.GTCCRA = xx; GPTW0.GTCCRB = xx; xx: optional value.
15.	Clear interrupt request.	IR(GPTW0.GTCIA0) = 0b; IR(GPTW0.GTCIB0) = 0b;
16.	Make interrupt priority settings.	IPR(GPTW0.GTCIA0) = 0x000F; IPR(GPTW0.GTCIB0) = 0x000F;
17.	Make to enable interrupt request	GPTW0.GTINTAD.BIT.GTINTA = 1b; GPTW0.GTINTAD.BIT.GTINTB = 1b; IEN(GPTW0.GTCIA0) = 1b; IEN(GPTW0.GTCIB0) = 1b; setpsw_i();
18.	Count start	GPTW0.GTCR.CST = 1b;

2.3 Input Capture Operation

Points of difference in input capture operation on the H8S/2378 Group and RX261 Group are described below.

Table 2-4 lists conditions for input capture operation on the H8S/2378 Group and RX261 Group.

Table 2-4 Conditions for Input Capture Operation using H8S TPU and RX GPTW

Item	Operating conditions	
	H8S (H8S/2378)	RX (RX261)
Peripheral function operating clock	ϕ: 20 MHz	PCLKA: 64MHz
Channels used	Channel 3 of TPU	GPTW0
Pins used	TIOCA3: P20 TIOCB3: P21	GTIOC0A: P22 GTIOC0B: P23
Clearing of TCNT register	Clearing of counter at TGRB register input capture	GTCNT is cleared by GPTW.GTCCRB input capture.
Input capture input edge	TIOCA3 pin: Both rising and falling edge. TIOCB3 pin: Falling edge.	GTIOC0A pin Both rising and falling edge. GTIOC0B pin Falling edge.

2.3.1 Operation

Figure 2-2 shows an example of input capture operation on the H8S/2378 Group and RX261 Group.

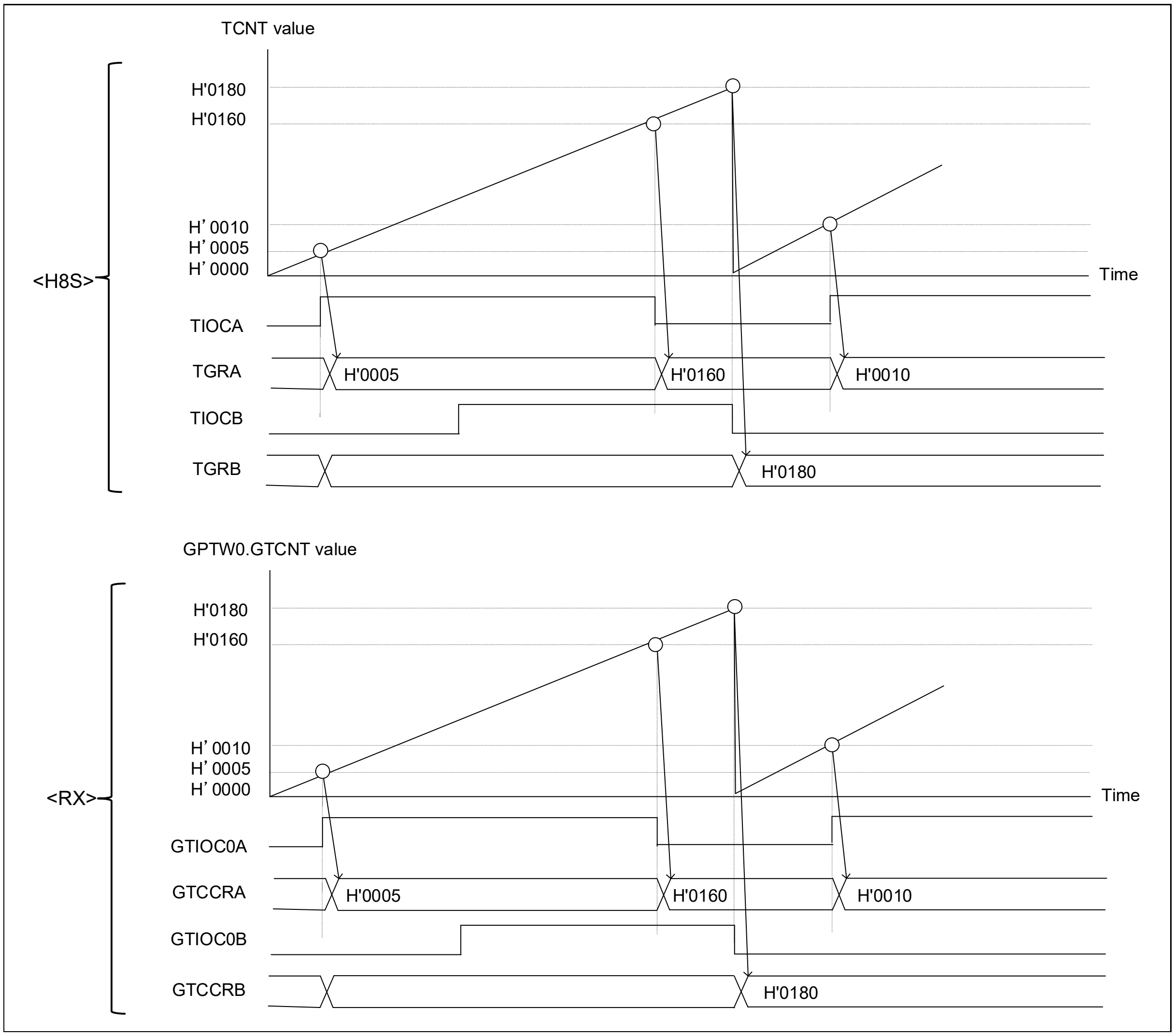

Figure 2-2 Example of Input Capture Operation on H8S/2378 Group and RX261 Group

2.3.2 Input capture Setting Procedure

Table 2-5 lists procedure for input capture operation using RX261 GPTW.

Table 2-5 procedure for input capture operation using RX261 GPTW.

No	procedure	RX(RX261)
1.	Cancel module stop state.	SYSTEM.PRCR.WORD = 0xA502; MSTP(GPTW) = 0; SYSTEM.PRCR.WORD = 0xA500;
2.	Disable write protection	GPTW0.GTWP=0x0000A5xx xx: When write protection is enabled, write “0” to each bit.
3.	Disable interrupts.	IEN(GPTW0.GTCIA0) = 0b; IEN(GPTW0.GTCIB0) = 0b; GPTW0.GTINTAD.BIT.GTINTA = 0b; GPTW0.GTINTAD.BIT.GTINTB = 0b;
4.	Stop count operation.	GPTW0.GTCR.BIT.CST = 0b;
5.	Clear counter.	GPTW0.GTCNT = 0x00000000;
6.	Make I/O port function settings.	PORT2.PMR.BIT.B2 = 0b; PORT2.PMR.BIT.B3 = 0b; PORT2.PDR.BIT.B2 = 0b; PORT2.PDR.BIT.B3 = 0b; MPC.PWPR.BIT.B0WI = 0b; MPC.PWPR.BIT.PFSWE = 1b; MPC.P22PFS.BYTE = 0x14; MPC.P23PFS.BYTE = 0x14; MPC.PWPR.BIT.PFSWE = 0b; MPC.PWPR.BIT.B0WI = 1b; PORT2.PMR.BIT.B2 = 1b; PORT2.PMR.BIT.B3 = 1b;
7.	Make operation mode settings	GTCR.MD[3:0]=0000b
8.	Make count direction settings.	GPTW0.GTUDDTYC.BIT.UD=1b GPTW0.GTUDDTYC.BIT.UDF=1b;
9.	Make count clock setting.	GPTW0.GTCR.BIT.TPCS = 0000b;
10.	Make end of period settings	GPTW0.GTPR＝0xFFFF;
11.	Make initial value to count setting	GPTW0.GTCNT＝0x0000;
12.	Make input capture sourse settings	GPTW0.GTICASR.BIT.ASCARBH=1b; GPTW0.GTICASR.BIT.ASCARBL=1b; GPTW0.GTICASR.BIT.ASCAFBH=1b; GPTW0.GTICASR.BIT.ASCAFBL=1b; GPTW0.GTICASR.BIT.ASCBRAH=0b; GPTW0.GTICASR.BIT.ASCBRAL=0b; GPTW0.GTICASR.BIT.ASCBFAH=1b; GPTW0.GTICASR.BIT.ASCBFAL=1b;
13.	Clear interrupt request.	IR(GPTW0.GTCIA0) = 0b; IR(GPTW0.GTCIB0) = 0b;
14.	Make interrupt priority settings.	IPR(GPTW0.GTCIA0) = 0x000F; IPR(GPTW0.GTCIB0) = 0x000F;
15.	Make to enable interrupt request	GPTW0.GTINTAD.BIT.GTINTA = 1b; GPTW0.GTINTAD.BIT.GTINTB = 1b; IEN(GPTW0.GTCIA0) = 1b; IEN(GPTW0.GTCIB0) = 1b; setpsw_i();
16.	Count start	GPTW0.GTCR.CST = 1b;

2.4 PWM Mode 1 operation

In H8S/2378 Group PWM mode 1 operation use Two pairs of registers — the TGRA and TGRB register, and the TGRC and TGRD register — are used to generate PWM output on the TIOCA (MTIOCA) pin and TIOCC (MTIOCC) pin.

In RX261 Group use sawtooth-wave PWM mode1.Period set to GTPR.
Duty set to GTCCRA and generate PWM output on the GTIOC0A pin.

Table 2-6 lists the preconditions for PWM mode 1 operation on the H8S/2378 Group and for sawtooth-wave PWM mode 1 operation on the RX261 Group.

Table 2-6 Conditions for H8S PWM Mode 1 and RX261 sawtooth-wave PWM mode1 Operation

Item	Operation Conditions	
	H8S (H8S/2378)	**RX (RX261)**
Peripheral function operating clock	ϕ: 20 MHz	PCLKA: 64MHz
Channels used	Channel 3 of TPU	GPTW0
Pins used	TIOCA3: P20	GTIOC0A: P22
Clearing of TCNT register	Clearing of counter at TGRA compare match	Clearing of counter at GTPR compare match
PWM output waveform	Frequency: 1kHz MTIOC0A: 70% duty, high output at TGRB compare match	Frequency:1kHz GTIOC0A: 70% Duty High output by GTCCRA compare match End of period: GTIOC0A=Low output.

2.4.1 Operation

Figure 2-3 shows an example of PWM mode 1 operation on the H8S/2378 Group and sawtooth-wave PWM mode1 on RX261 Group.

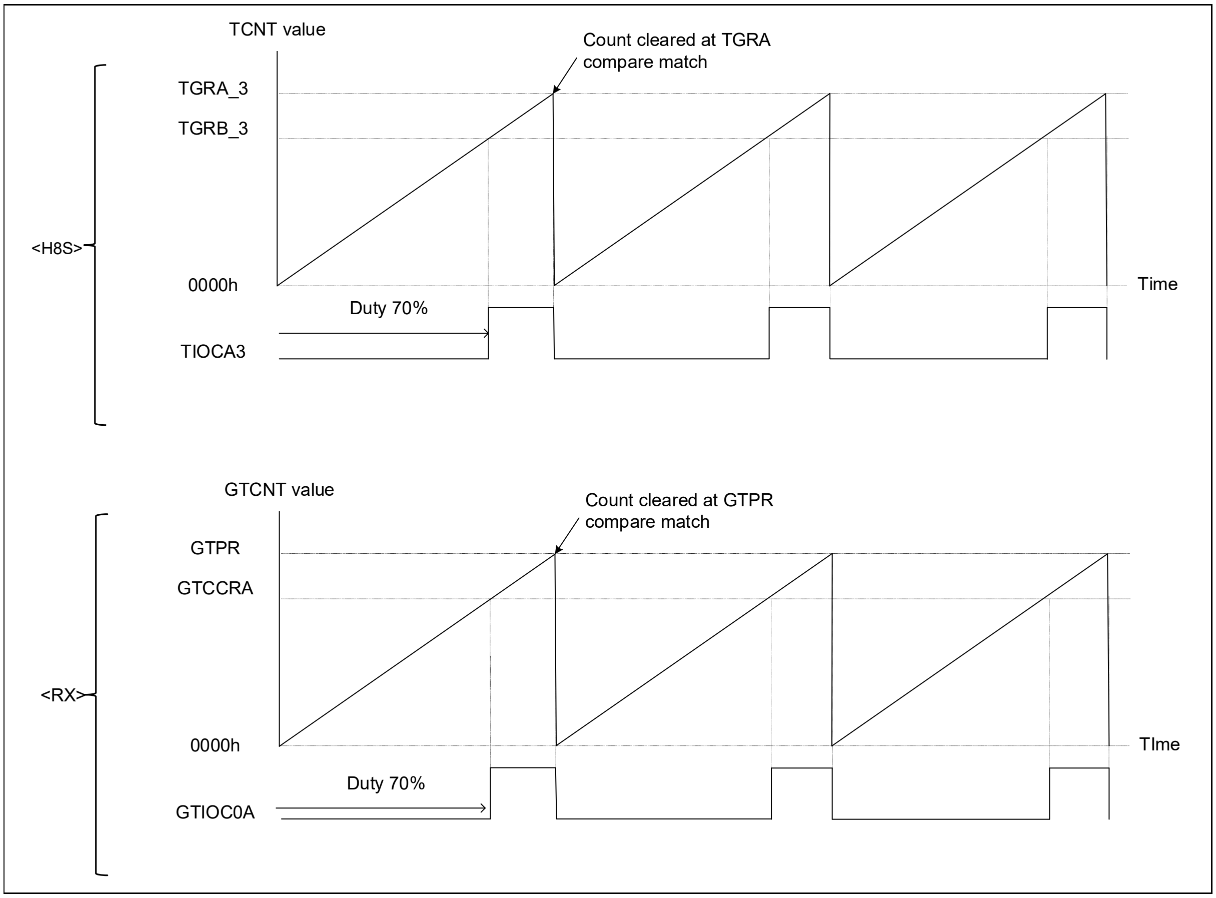

Figure 2-3 Example of PWM Mode 1 Operation on H8S/2378 Group and sawtooth-wave PWM mode1 on RX261 Group

2.4.2 sawtooth-wave PWM mode1 Setting Procedure

Table 2-7 lists procedure for using sawtooth-wave PWM mode1 on RX261.

Table 2-7 procedure for using sawtooth-wave mode1 on RX261.

No.	Procedure	RX(RX261)
1.	Cancel module stop state.	SYSTEM.PRCR.WORD = 0xA502; MSTP(GPTW) = 0; SYSTEM.PRCR.WORD = 0xA500;
2.	Disable write protection	GPTW0.GTWP=0x0000A5xx xx: When write protection is enabled, write “0” to each bit.
3.	Disable interrupts.	IEN(GPTW0.GTCIA0) = 0b; IEN(GPTW0.GTCIB0) = 0b; GPTW0.GTINTAD.BIT.GTINTA = 0b; GPTW0.GTINTAD.BIT.GTINTB = 0b;
4.	Stop count operation.	GPTW0.GTCR.BIT.CST = 0b;
5.	Clear counter.	GPTW0.GTCNT = 0x00000000;
6.	Make I/O port function settings.	PORT2.PMR.BIT.B2 = 0b; PORT2.PDR.BIT.B2 = 0b; MPC.PWPR.BIT.B0WI = 0b; MPC.PWPR.BIT.PFSWE = 1b; MPC.P22PFS.BYTE = 0x14; MPC.PWPR.BIT.PFSWE = 0b; MPC.PWPR.BIT.B0WI = 1b; PORT2.PMR.BIT.B2 = 1b;
7.	Make operation mode settings.	GTCR.MD[3:0]=0000b
8.	Make count direction.	GPTW0.GTUDDTYC.BIT.UD=1b; GPTW0.GTUDDTYC.BIT.UDF=1b;
9.	Make count clock setting.	GPTW0.GTCR.BIT.TPCS = 0000b;
10.	Make end of period settings	GPTW0.GTPR＝0xFFFF;
11.	Make initial value to count settings	GPTW0.GTCNT＝0x0000;
12.	Make GTIOCnm pin settings	GPTW0.GTIOR.BIT.GTIOA = 00110b; GPTW0.GTIOR.BIT.GTIOB = 00110b;
13.	Make GTIOCnm pin output enable settings.	GPTW0.GTIOR.OAE = 1b; GPTW0.GTIOR.OBE = 1b
14.	Make compare match value settings	GPTW0.GTPR = 0xFFFF; GPTW0.GTCCRA = 0xB333;
15.	Clear interrupt request.	IR(GPTW0.GTCIA0) = 0b; IR(GPTW0.GTCIB0) = 0b;
16.	Make interrupt priority settings.	IPR(GPTW0,GTCIA0) = 0x000F; IPR(GPTW0,GTCIB0) = 0x000F;
17.	Make to enable interrupt request	GPTW0.GTINTAD.BIT.GTINTA = 1b; GPTW0.GTINTAD.BIT.GTINTB = 1b; IEN(GPTW0.GTCIA0) = 1b; IEN(GPTW0.GTCIB0) = 1b; setpsw_i();
18.	Count start	GPTW0.GTCR.CST = 1b;

2.5 PWM Mode 2 operation

In H8S/2378 Group PWM mode 2 operation — One TGR register is used as a cycle register and the other TGR registers as duty registers to generate PWM output.

In RX261 Group use sawtooth-wave PWM mode 1, output 3 signal PWM output using GPTW0 and GPTW1 synchronous operation.

Table 2-8 lists the preconditions for PWM mode 1 operation on the H8S/2378 Group and for sawtooth-wave PWM mode 1 operation on the RX261 Group.

Table 2-8 preconditions for PWM mode 1 operation on the H8S/2378 Group and for sawtooth-wave PWM mode 1 operation on the RX261 Group.

Item	Operation condition	
	H8S (H8S/2378)	RX (RX261)
Peripheral function operating clock	ϕ: 20 MHz	PCLKA: 64MHz
Channels used	Channel 3 of TPU	GPTW0 and GPTW1
Pins used	TIOCB3: P21 TIOCC3: P22 TIOCD3: P23	GTIOC0A: P22 GTIOC0B: P23 GTIOC1A: P24
Clearing of TCNT register	Clearing of counter at TGRA compare match	Clearing of counter at GPTW0.GTPR and GPTW1.GTPR
PWM output waveform	Frequency: 1 kHz TIOCB3: Duty 30% TIOCC3: Duty 50% TIOCD3: Duty 70%	Frequency: 1kHz GPTW0.GTIOC0A: Duty 30% GPTW0.GTIOC0B: Duty 50% GPTW1.GTIOC1A: Duty 70% Initial output: Low output End of period: Low output Occur the compare match: High output
Synchronous start	N/A	GPTW0.GTSTR＝0x0003;

2.5.1 Operation

Figure 2-4 Example of PWM Mode 2 Operation on H8S/2378 Group and sawtooth-wave PWM mode1 with synchronous operation on RX261 Group.

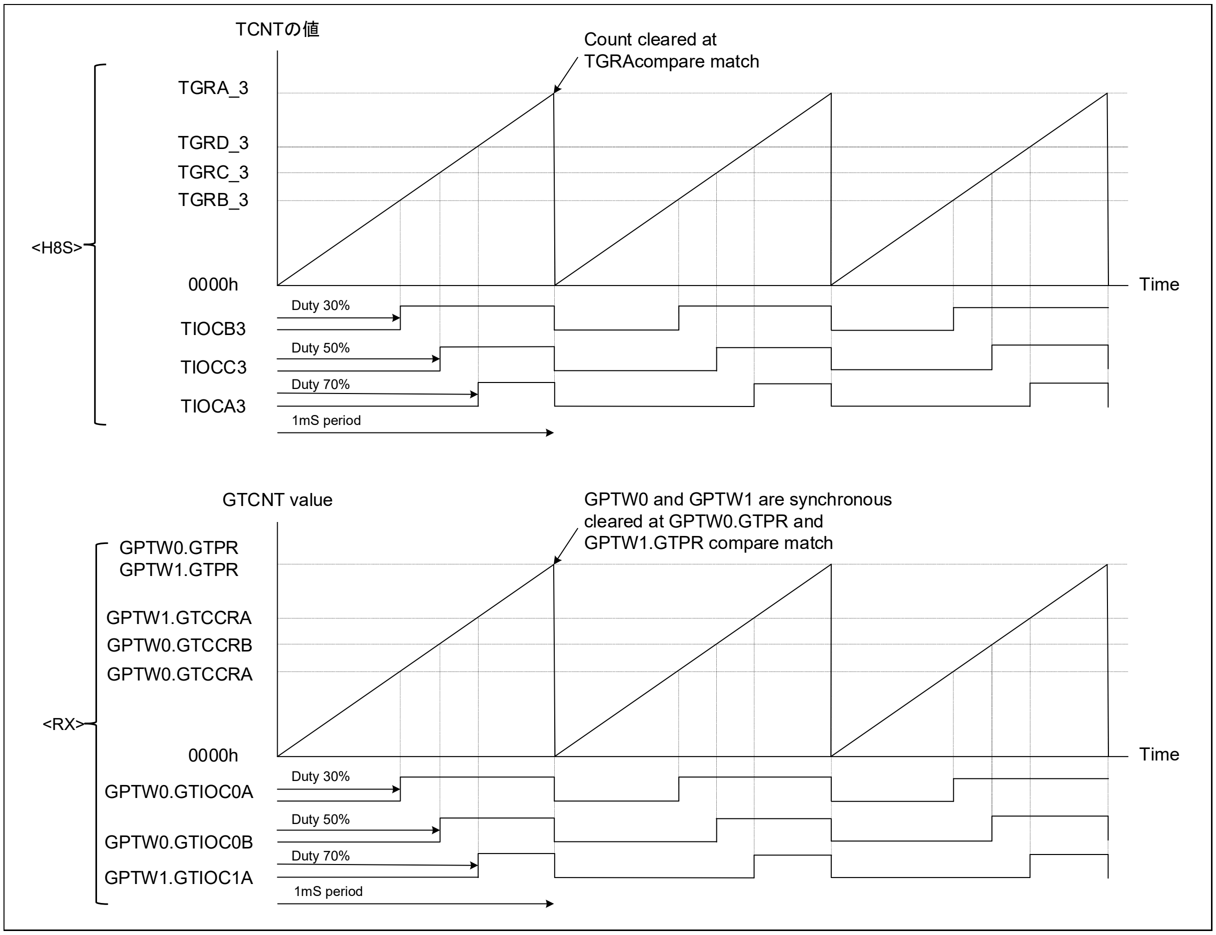

Figure 2-4 Example of PWM Mode 2 Operation on H8S/2378 Group and sawtooth-wave PWM mode1 with synchronous operation on RX261 Group

2.5.2 sawtooth-wave PWM mode1 with synchronous operation Setting Procedure

Table 2-9 procedure for using sawtooth-wave PWM mode1 with synchronous operation on RX261.

Table 2-9 procedure for using sawtooth-wave mode1 with synchronous operation on RX261.

No.	Procedure	RX(RX261)
1.	Cancel module stop state.	SYSTEM.PRCR.WORD = 0xA502; MSTP(GPTW) = 0; SYSTEM.PRCR.WORD = 0xA500;
2.	Disable write protection	GPTW0.GTWP=0x0000A5xx xx: When write protection is enabled, write “0” to each bit.
3.	Disable interrupts.	IEN(GPTW0.GTCIA0) = 0b; IEN(GPTW0.GTCIA1) = 0b; IEN(GPTW1.GTCIB0) = 0b; GPTW0.GTINTAD.BIT.GTINTA = 0b; GPTW0.GTINTAD.BIT.GTINTB = 0b; GPTW1.GTINTAD.BIT.GTINTA = 0b;
4.	Stop count operation.	GPTW0.GTCR.BIT.CST = 0b; GPTW1.GTCR.BIT.CST = 0b;
5.	Clear counter.	GPTW0.GTCNT = 0x00000000; GPTW1.GTCNT = 0x00000000;
6.	Make I/O port function settings.	PORT2.PMR.BIT.B2 = 0b; PORT2.PMR.BIT.B3 = 0b; PORT2.PMR.BIT.B4 = 0b; PORT2.PDR.BIT.B2 = 0b; PORT2.PDR.BIT.B3 = 0b; PORT2.PDR.BIT.B4 = 0b; MPC.PWPR.BIT.B0WI = 0b; MPC.PWPR.BIT.PFSWE = 1b; MPC.P22PFS.BYTE = 0x14; MPC.P23PFS.BYTE = 0x14; MPC.P24PFS.BYTE = 0x14; MPC.PWPR.BIT.PFSWE = 0b; MPC.PWPR.BIT.B0WI = 1b; PORT2.PMR.BIT.B2 = 1b; PORT2.PMR.BIT.B3 = 1b; PORT2.PMR.BIT.B4 = 1b;
7.	Make operation mode settings.	GPTW0.GTCR.MD[3:0]=0000b GPTW1.GTCR.MD[3:0]=0000b
8.	Make count direction.	GPTW0.GTUDDTYC.BIT.UD=1b; GPTW0.GTUDDTYC.BIT.UDF=1b;
9.	Make count clock setting.	GPTW0.GTCR.BIT.TPCS = 0000b; GPTW1.GTCR.BIT.TPCS = 0000b;
10.	Make end of period settings	GPTW0.GTPR＝0xFFFF GPTW1.GTPR＝0xFFFF
11.	Make initial value to count settings	GPTW0.GTCNT＝0x0000; GPTW1.GTCNT＝0x0000;
12.	Make GTIOCnm pin settings	GPTW0.GTIOR.BIT.GTIOA = 00110b; GPTW0.GTIOR.BIT.GTIOB = 00110b; GPTW1.GTIOR.BIT.GTIOA = 00110b;
13.	Make GTIOCnm pin output enable settings.	GPTW0.GTIOR.OAE = 1b; GPTW0.GTIOR.OBE = 1b; GPTW1.GTIOR.OAE = 1b;

No.	Procedure	RX(RX261)
14.	Make compare match value settings	GPTW0.GTCCRA =0x4CCD; GPTW0.GTCCRB =0x8000; GPTW1.GTCCRA =0xB333;
15.	Clear interrupt request.	IR(GPTW0.GTCIA0) = 0b; IR(GPTW0.GTCIB0) = 0b; IR(GPTW1.GTCIA1) = 0b;
16.	Make interrupt priority settings.	IPR(GPTW0.GTCIA0) = 0x000F; IPR(GPTW0.GTCIB0) = 0x000F; IPR(GPTW1.GTCIA1) = 0x000F;
17.	Make to enable interrupt request	GPTW0.GTINTAD.BIT.GTINTA = 1b; GPTW0.GTINTAD.BIT.GTINTB = 1b; GPTW1.GTINTAD.BIT.GTINTA = 1b; IEN(GPTW0.GTCIA0) = 1b; IEN(GPTW0.GTCIB0) = 1b; IEN(GPTW1.GTCIA1) = 1b; setpsw_i();
18.	Count start	GPTW0.GTSTR＝0x0003;

3. Appendix

3.1 Points of migration between H8S to RX

3.1.1 Interrupt

Interrupts can be accepted on the RX261 Group when the following conditions are met:

- The I flag (PSW.I bit) is set to 1.
- The interruption is enabled in the IER and IPR registers of the ICU.
- Interrupt requests are enabled by the corresponding peripheral function interrupt request enable bit.

Table 3-1 is a comparative listing of the interrupt generation conditions on the H8S/2378 Group and RX261 Group.

Table 3-1 Comparative Listing of Interrupt Generation Conditions on RX261 Group and

Item	H8S (H8S/2378)	RX (RX261)
Interrupt enable bit (I bit)	In interrupt control mode 0, setting the I bit to 0 (enabled) in the CCR register enables acceptance of maskable interruptions. In interrupt control mode 2 the I bit in the CCR register is not used.	Setting the I bit in the PSW register to 1 (enabled) enables acceptance of maskable interrupts.
Processor interrupt priority level	In interrupt control mode 2 only interruption requests with a higher priority level than those indicated by bits I2 to I0 in the EXR register are accepted. In interrupt control mode 0 the bits I2 to I0 in the EXR register is not used.	Only interrupt requests with a higher priority level than those indicated by the IPL [3:0] bits in the PSW register are accepted.
Interrupt priority level	In interrupt control mode 0 the default settings are used. In interrupt control mode 2 the IPR register settings are used.	Set in the IPR register.
Interrupt request flag	The interrupt controller manages interrupt status flags for external interrupts, and interrupt status flags for internal interrupt sources are managed within each on-chip peripheral function.	The interrupt controller manages all interrupt status flags for peripheral functions, external pins, NMI interrupts, etc.
Interrupt request enable	IRQ interrupts are enabled by settings in the IER register.	Set in the IER register for maskable interruptions and in the NMIER register for non-maskable interruptions.
Peripheral function interrupt enable	Interrupts can be enabled or disabled by each peripheral function.	

In detail, refer to the interrupt controller (ICU), CPU and using peripheral function chapter in the User’s Manual: hardware.

3.1.2 IO port

On the RX261 Group it is necessary to make settings to the MPC to assign pins to peripheral function I/O signals.

To apply I/O control to a pin on the RX261 Group, make the following two settings:

- PFS register of MPC: Select the peripheral function to be assigned to the pin.
- PMR register of I/O port: Select whether to assign the pin to a general I/O port or a peripheral function.

Table 3-2 provides a comparative listing of I/O settings for peripheral function pins on the H8S/2378 Group and RX261 Group.

Table 3-2 Comparison of I/O settings for Peripheral Function Pins on H8S/2378 Group and RX261 Group

Function	H8S (H8S/2378)	RX (RX261)
Pin function selection	Pins can be switched between general I/O port and peripheral function settings and pin functions selected through combinations of the MCU operating mode, the setting of the SYSCR.EXPE bit, the PFCR registers, the DDR registers, and the settings of the various peripheral functions.	I/O pins for peripheral functions can be assigned from a selection of multiple pins by making settings in the PFS register.
General I/O port/peripheral function switching		Settings in the PMR register can be used to select whether specific pins are used as I/O ports or as peripheral functions.

For details, refer to the sections describing the multi-function pin controller (MPC) and I/O ports in User's Manual: Hardware.

3.1.3 Module Stop Function

On the H8S/2378 Group and RX261 Group it is possible to halt the functioning of individual peripheral modules.

Power consumption can be reduced by transitioning unused peripheral modules to the module stop state. Modules not listed in Table 3-3 are in the module stop state after a reset.

Table 3-3 Modules that Operate under Initial Settings on H8S/2378 Group and RX261 Group

H8S (H8S/2378)	RX (RX261)
EXDMAC, DMAC, DTC	DMAC, DTC, RAM

When a module is in the module stop state, its registers cannot be read or written to.

Before using any module not listed in Table 3-3, it is necessary to cancel the module stop state and then make initial settings.

For details, refer to the section describing the low power consumption functions in User's Manual: Hardware.

3.1.4 Register Write Protection Function

On the RX261 Group it is possible to protect important registers from being overwritten if program runaway occurs. The protect register (PRCR) is used to specify the registers that are protected by this function. Register protection can be enabled for the clock generation circuit–related registers, flash memory–related registers, operating mode–related registers, low power consumption function–related registers, low-power timer–related registers, LVD–related registers, and software reset register.
For details, refer to the section on the register write protection function in User's Manual: Hardware.

3.1.5 I/O Register Macros

The macro definitions listed below are contained in the I/O register definition file (iodefine.h) of the RX261 Group.

Using macro definitions can make program code easier to read.

Table 3-4 lists macro usage examples.

Table 3-4 Macro Usage Examples

Macro	Usage Example
IR(“module name”,”bit name”)	IR(GPTW 0,TGIA0) = 0; Clears the IR bit corresponding to TGIA0 of GPTW0 to 0 (clear interrupt request).
DTCE(“module name”,”bit name”)	DTCE(GPTW0,TGIA0) = 1; Sets the DTCE bit corresponding to TGIA0 of GPTW0 to 1 (enable DTC start).
IEN(“module name”,”bit name”)	IEN(GPTW0,TGIA0) = 1; Sets the IEN bit corresponding to TGIA0 of GPTW0 to 1 (enable interrupt).
IPR(“module name”,”bit name”)	IPR(GPTW0,TGIA0) = 0x02; Sets the IPR bits corresponding to TGIA0 of GPTW0 to 2 (interrupt priority level 2).
MSTP(“module name”)	MSTP(GPTW) = 0; Clears the module stop setting bit of GPTW0 to 0 (cancel module stop state).
VECT(“module name”,”bit name”)	#pragma interrupt(Excep_GPTW0_TGIA0(vect=VECT(GPTW0,TGIA0))) Declares the interrupt function corresponding to TGIA0 of GPTW0.

3.1.6 Embedded Functions

On the RX261 Group interrupt functions are provided to implement control register settings or special instructions. To use these embedded functions, including the file machine.h.

Table 3-5 lists (examples of) points of difference between control register settings and special instructions on the H8S/2378 Group and RX261 Group.

Table 3-5 Points of Difference between Control Register Settings and Special Instructions on H8S/2378 Group and RX261 Group (Example)

Item	Format	
	H8S (H8S/2378)	**RX (RX261)**
Set I flag to 1.	set_imask_ccr(1); *1*2	setpsw_i(); *1
Clear I flag to 0.	set_imask_ccr(0); *1*2	clrpsw_i(); *1
Expand to WAIT instruction.	None	wait(); *1
Expand to NOP instruction.	nop(); *1	nop(); *1

Note 1. It is necessary to include the file machine.h.

Note 2. I = 1 means enable interrupts on the RX261 Group, and I = 1 means mask interrupts on the H8S/2378 Group.

4. Reference Documents

User's Manual: Hardware
 H8S/2378 Group, H8S/2378R Group Hardware Manual Rev.7.00 (REJ09B0109-0700)
 RX260 Group and RX261 Group User's Manual: Hardware Rev.1.10 (R01UH1045)
 (The latest versions can be downloaded from the Renesas Electronics website.)

Application Note
 M16C Family, RX Family Migrating from the M16C Family to the RX Family: Timers(R01AN1729)
 (The latest versions can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
 (The latest versions can be downloaded from the Renesas Electronics website.)

User's Manual: Development Environment
 CC-RX Compiler User's Manual(R20UT3248)
 H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package Ver.7.00 User's Manual (REJ10J2039-0100)
 (The latest versions can be downloaded from the Renesas Electronics website.)

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 30, 2025	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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