Multi-pulse Testing for GaN Layout Verification

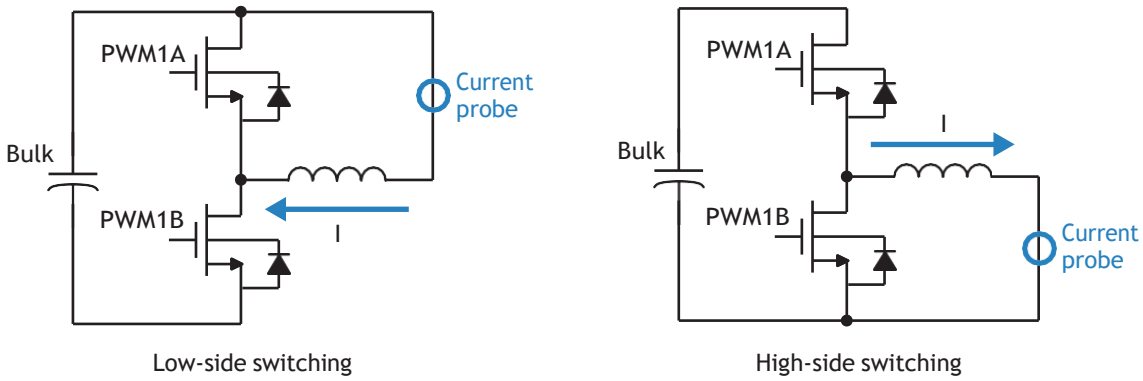

Figure 1. Simplified schematic for half-bridge low-side switching (left) and high-side switching (right)

Introduction

This Design Guide is a tutorial on verifying the power train of a half- or full-bridge under high voltage and high current operating conditions to check for parasitic oscillation at the switching edges. Oscillation can usually be fixed with a better PCB layout and the use of appropriate ferrite beads. (See Application Note AN0009 for recommendations.)

An optional ultrafast electronic breaker circuit can also be used to reduce damage in case of catastrophic failure of the switches during the testing. For more information, see the Ultrafast Overcurrent Breaker Circuit for Prototyping Design Guide.

Even though this test can be executed with an advanced signal generator (one that allows fixing the number of pulses), this Design Guide will focus on using a DSP to drive the switches. The code can be freely downloaded at Renesasusa.com/multipulse-code.

Test setup

The multi-pulse testing should be done in the actual layout that is going to be used in the application. All the components in or around the power train should be on the board (drivers, low voltage auxiliary supply, ferrite beads and any other gate components, inductor, switches, DC bulk and decoupling capacitors).

The code in the appendix was tested on the TMS320F28035PN from the Texas Instruments C2000™ family, but it can be easily ported to any variant of the C280xx family. An emulator such as the XDS100 v1 will be required for the testing.

The setup for a half-bridge is shown on Figure 1. If the circuit is an LLC resonant converter the secondary of the transformer should be shorted. This circuit can also be easily used in the buck, buck-boost or boost topologies (both standard or synchronous variants). For the boost converter variant connect the output back into the input to recirculate the inductor current, as shown in Figure 2. This image also shows the location to connect the breaker circuit. The location is similar in all topologies, where the breaker is located between the bulk capacitor and the decoupling capacitors.

Figure 3 shows the setup necessary when testing a full bridge.

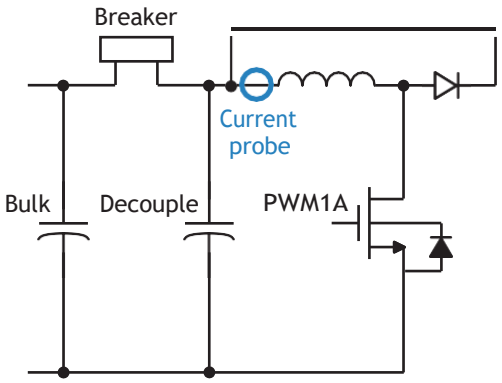

Figure 2. Simplified schematic for boost test

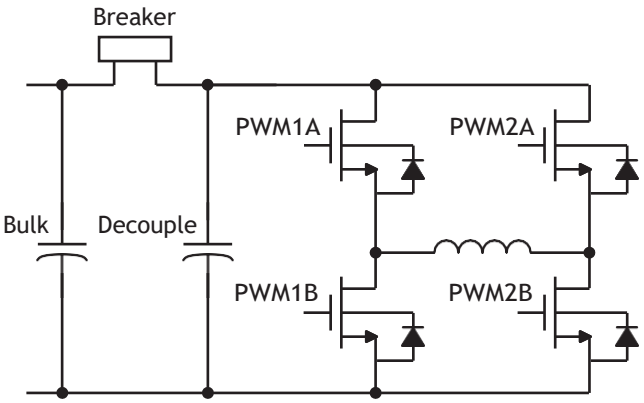

Figure 3. Simplified schematic for full-bridge test

The switching frequency should be set for the highest normal operation switching frequency the system will see in operation, and the test should run at the maximum operating DC voltage. The current should go to about 125% of the expected design maximum current.

For details on how to properly probe the voltage on the switch, please consult Application Note AN0003.

Code

Two define directives are used to conditionally compile the code. These directives can be found on the file "allHeaderIncludes.h":

- FULL_BRIDGE – When this directive is set to 1, it will activate PWM2 to generate the signal for a full-bridge using four GaN switches. When set to 0, it is used for a half-bridge.
- HALF_BRIDGE_MAIN_SWITCH – This directive will determine which one is the main switch. Setting the directive to 0 will make the system work in low-side switching, and setting it to 1 will make the system work in high switching (half-bridge only).

To control the switching, the emulator should be connected to the DSP. A few variables are then used to configure and control the code:

Reset – This register will immediately trigger a new run when set to 1. It will go back to 0 automatically at the end of the run.

Pulses – Total number of switching pulses in one run.

Period – Period counter for the PWM (inversely proportional to the switching frequency, *Fsw*). 600 corresponds to 100kHz, and 1200 to 50kHz, etc. *GlobalClk* corresponds to the DSP's main clock.

$$Period = \frac{GlobalClk}{Fsw}$$

CMP – Duty cycle control. Seeing that the PWM is configured as an up-down counter, any value above half of the *Period* variable will lead to 100% duty cycle.

$$DutyCycle = \frac{CMP}{Period/_2}$$

DeadTime – Controls the dead time between switches, and by default it is ~16.667ns per count (assuming a 60MHz *GlobalClk*). The required value will be dependent on the tolerances at the DSP or controller, as well as tolerances on the driver, and on the rise/fall time of the GaN devices. Typically, a value between 60ns and 100ns will be enough, but this should be verified on a case-by-case basis.

Polarity – This variable is only used when testing a full bridge. It determines which leg of the full bridge will be switching. If it is set to 0, PWM1A and PWM1B will switch, whereas PWM2A is always off and PWM2B is always on. If it is set to 1, PWM2A and PWM2B will be the switching leg.

Example results and troubleshooting

To prevent potential issues, start the testing with a low DC voltage (e.g. 20V) and a low duty cycle or low number of pulses, and then gradually increase these parameters until the desired input voltage and output current are tested. In most situations, it will be possible to see signs of issues before any destructive oscillation occurs.

Figure 4 is an example of a waveform where the drain to source voltage (pink) has oscillation that is showing signs of amplification. At this point, corrective measures should be taken before attempting to increase the voltage or the current.

Figure 5 does not indicate a reliability issue; however, there will be an increase in EMI and in the losses of the system. Adding a ferrite bead in this situation will very likely increase the overall system efficiency and reduce EMI.

Figure 6 shows an example of acceptable behavior. Please note that if using drain ring beads that are directly on the pin of the GaN device, it is still necessary to measure the drain to source voltage as the drain beads will cause a slightly higher voltage spike on the drain.

Several things can be done to mitigate the issues shown in Figures 4 and 5, such as changing the driver voltage or driver circuit, adding beads or improving the layout. More detail about this topic can be found in Application Note AN0009.

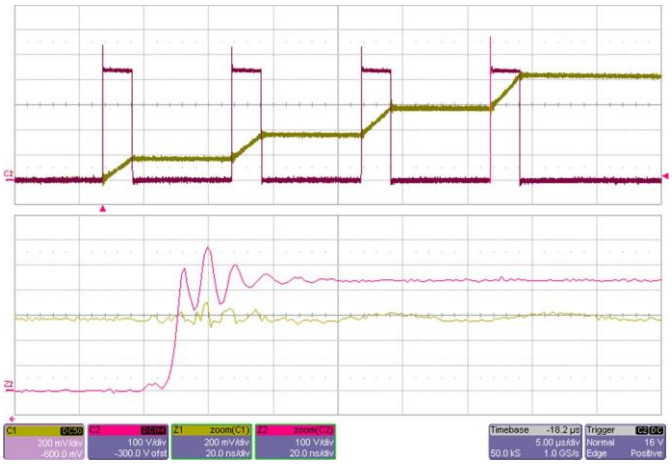

Figure 4. Example waveform with problematic ringing

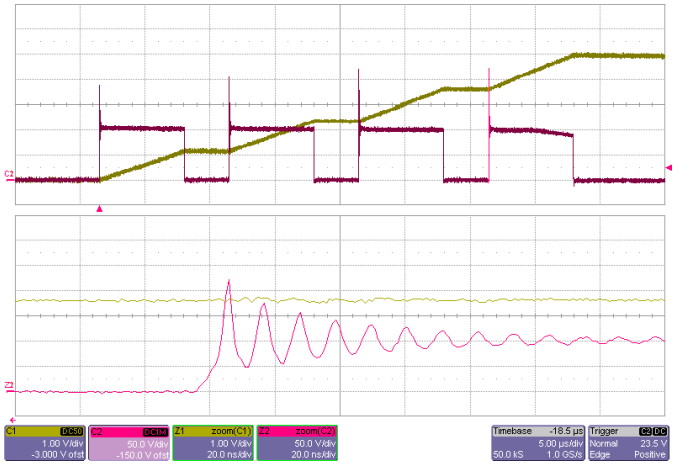

Figure 5. Example waveform with excessing ringing

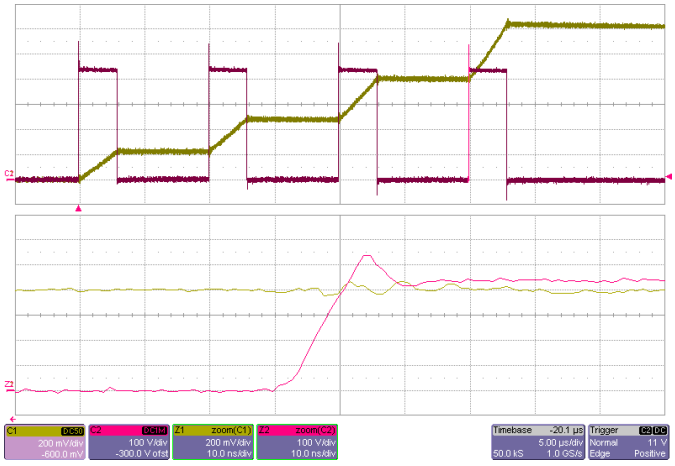

Figure 6. Example waveform with no ringing

References and further reading

DSP Code (Renesasusa.com/multipulse-code)

Application Note AN0009: Recommended External Circuitry for Renesas GaN FETs (Renesasusa.com/an0009)

Application Note AN0003: Printed Circuit Board Layout and Probing for GaN FETs (Renesasusa.com/an0003)

Design Guide DG005: Ultrafast Overcurrent Breaker Circuit for Prototyping (Renesasusa.com/dg005)