32-bit RISC CPU IP

SH-4A CPU

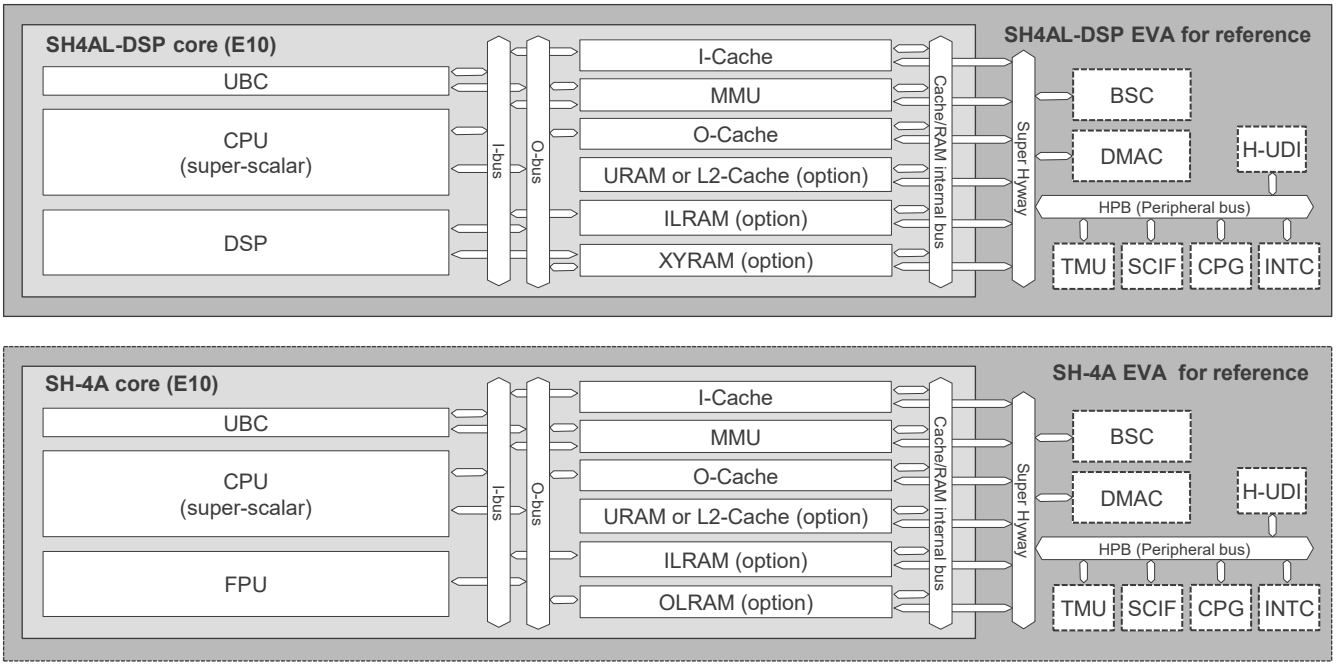
Overview

The SH-4A is a 32-bit RISC (reduced instruction set computer) microprocessor, featuring object code upward-compatibility with Renesas SuperH SH-1, SH-2, SH-3, and SH-4 microcomputers. It includes separate instruction and operand caches, the latter supporting both copy-back and write-through modes.

Key Features

- 32-bit internal data bus
- General purpose register file:
  - 16 32-bit general-purpose registers (and 8 32-bit shadow registers)
  - Seven 32-bit control registers
  - Four 32-bit system registers
- RISC type instruction set (with upward compatibility with SH-1, SH-2, SH-3, SH-4):
  - Instruction length: 16 bits fixed length for improving code efficiency
- Two-instruction simultaneous execution superscalar including FPU
- Instruction execution time: Up to 2 instructions / cycle
- Virtual address space: 4G bytes
- Built-in multiplier
- 7 stage pipeline
- Peripherals for reference : BSC, DMAC, TMU, SCIF, CPG, INTC and H-UDI

Block diagram



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