CAN FD IP

CAN FD controller

Overview

This IP is CAN FD controller that is compliant with ISO 11898-1 (2015) Specifications.
It embeds multiple CAN channels. 2,4,6 and 8 channel version are available.
Each CAN channel can be configurable to CAN FD or classic CAN and transmits and receives both ID formats of messages, namely the standard identifier (11 bits) (identifier is hereafter referred to as ID) and extended ID (29 bits).

IMPORTANT: When selling a device that includes the Renesas CAN FD IP core, you must contract CAN FD Protocol license with Bosch(Robert Bosch GmbH).

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Key Features

key features are as below. (*n*=1,3,5,7)

Item	Specification
Communication	CAN functionality is compliant to CAN FD ISO 11898-1 (2015)
Gateway Function	CAN 2.0 <> CAN 2.0 CAN 2.0 <> CAN FD Gateway (Only 8 Byte Payload) CAN FD <> CAN FD
Data transfer rate	up to 1Mbps for arbitration phase and up to 8Mbps for data phase , individually for each CAN channel
CAN channels	*n*+1
Selectable ID type	11-bit Standard ID
	11-bit Standard ID + 18-bit Extended ID
Selectable Frame Type	Data Frame (RTR = 0) (classic CAN and CAN FD frames)
	Remote Frame (RTR = 1) (in only classic CAN frames)
Variable Data Byte Count for Data Frames	DLC range: 0 to F
Message Buffer	Up to 16*(*n*+1) reception message buffers, shared among all the CAN channels
	64 transmit message buffers per channel
	4 transmission queue per channel Automatic message transfer into transmission queues supported
FIFO number	8 Reception FIFO Buffers Up to 3*(*n*+1) FIFOs individually configurable as -Reception FIFO -Transmission FIFO -CAN to CAN Gateway FIFO
Automatic delay interval timer for transmission	The delay timer can be applied to: -Transmission FIFO -CAN to CAN Gateway FIFO
Enhanced reception filtering	support of 11bit and 29bit CAN identifier
	programmable 29bit CAN identifier acceptance filter mask for each entry
	programmable GW routing capability for each channel (up to 8 routing destinations)
	RTR and IDE masking
	DLC filter
	Message buffer payload overload protection
	Payload filter
	Updating AFL entry during communication
General SW Support	Automatic label information added to receive message (for upper SW layer support)
Timer	TX and RX Time Stamp function
Power down function	Module start stop function for each CAN node (Channel & Global Sleep Mode)
Bus traffic measurement	CAN bus traffic measurement of each channel is possible
FFI mode	Freedom From Interference in CAN channel unit
	Freedom From Interference in message buffer unit

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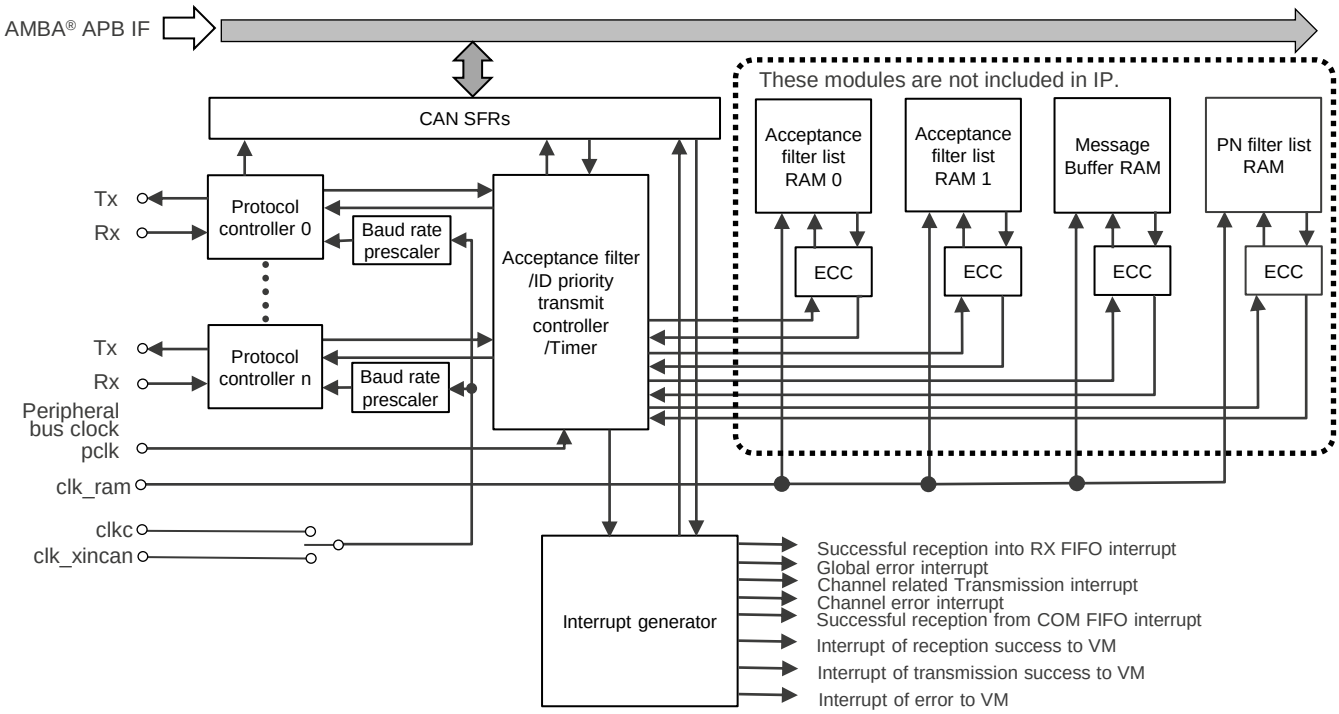
Block Diagram



Tx/Rx:
Input/Output pins of the CAN module

Protocol controller:
Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, error handling, etc.

Acceptance filter list RAM:
This RAM is used to store message acceptance filtering entries for all channels.
Each acceptance filter entry has an individual ID, data length code, payload data, a message pointer for an upper layer application usage, and a message direction pointer.
The AFLRAM is divided in two parts to accelerate AFL access process.

Message Buffer RAM:
This RAM is used to store messages for reception and for transmission using a normal Message Buffer or a FIFO. Each message entry has an individual ID, data length code, payload data, a message pointer for an upper layer application usage, and a time stamp.

Acceptance filter:
Performs filtering of received messages. The entries in the Acceptance filter list RAM are used for the filtering process.

Timer:
Two timers
-Reception Timestamp function
-Transmission separation time for FIFO Buffers

Interrupt generator:
Generates several types of global and channel interrupts

CAN SFRs:
CAN FD controller registers

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