Errata

SLG47105

CE-GP-003

Abstract

This document contains the known errata for SLG47105 and the recommended workarounds.

1 Information

Package(s)	20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

2 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Incorrect 32 mV and 64 mV Hysteresis Operation with ACMPxH
2	ACMPxH Erroneous Behavior when Used with Wake-Sleep Controller for Certain Vref Selection
3	Abnormal ACMPs Behavior

3 Errata Details

3.1 Incorrect 32 mV and 64 mV Hysteresis Operation with ACMPxH

3.1.1 Effect

ACMP0H and ACMP1H

3.1.2 Conditions

V_{DD} > 4.6 V, with hysteresis 32 mV at Vref range 1.344 V to 2.016 V.

V_{DD} > 3.6 V, with hysteresis 32 mV at Vref range 1.344 V to 1.504 V.

V_{DD} > 4.6 V, with hysteresis 64 mV at Vref range 1.376 V to 1.664 V.

3.6 V < V_{DD} < 4.6 V, with hysteresis 64 mV only when Vref is set to 1.376 V.

3.1.3 Technical Description

If using ACMPxH in with 32 mV or 64 mV hysteresis, ACMPxH output could be glitching when ACMPxH positive input (IN+) is close to the negative input (IN-). It can happen when VDD higher 4.6 V and Vref is in a range from 1.344 V to 2.016 V for 32 mV hysteresis, and Vref is in a range from 1.376 V to 1.664 V for 64 mV hysteresis.

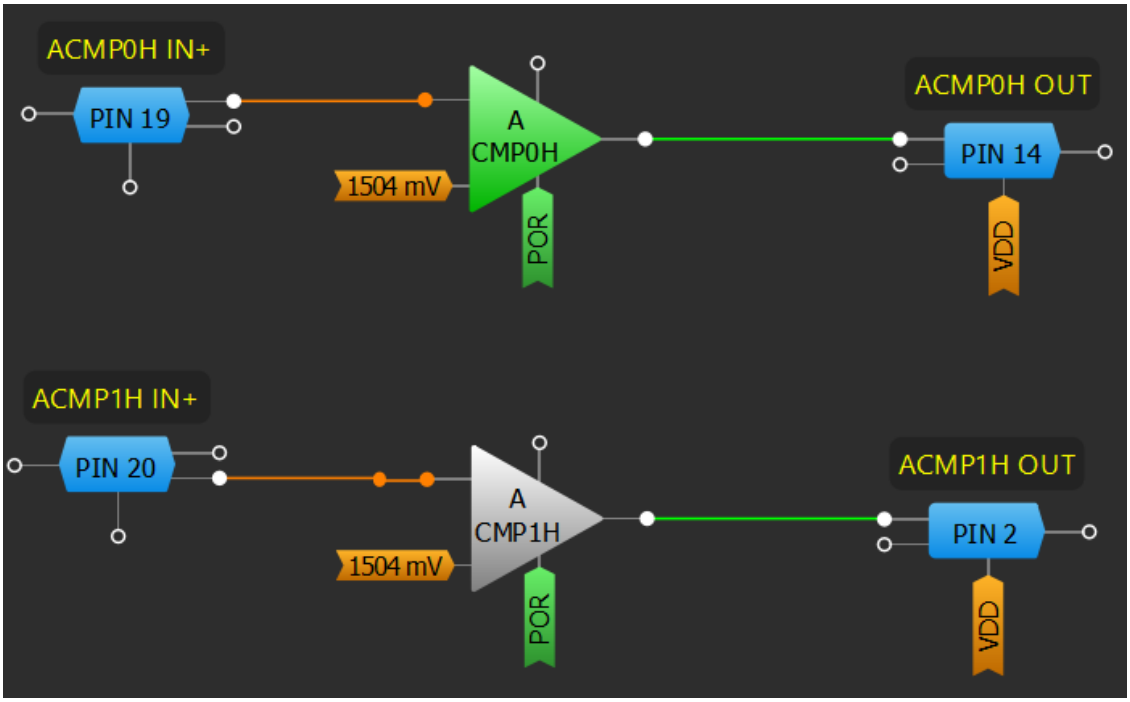

Figure 1: Testing Design

Channel 1 (yellow/top line) - PIN#19 (ACMP0H IN+)

Channel 2 (light blue/2nd line) - PIN#14 (ACMP0H OUT)

1. Waveform at Vref = 1504 mV, hysteresis is equal to 32 mV.

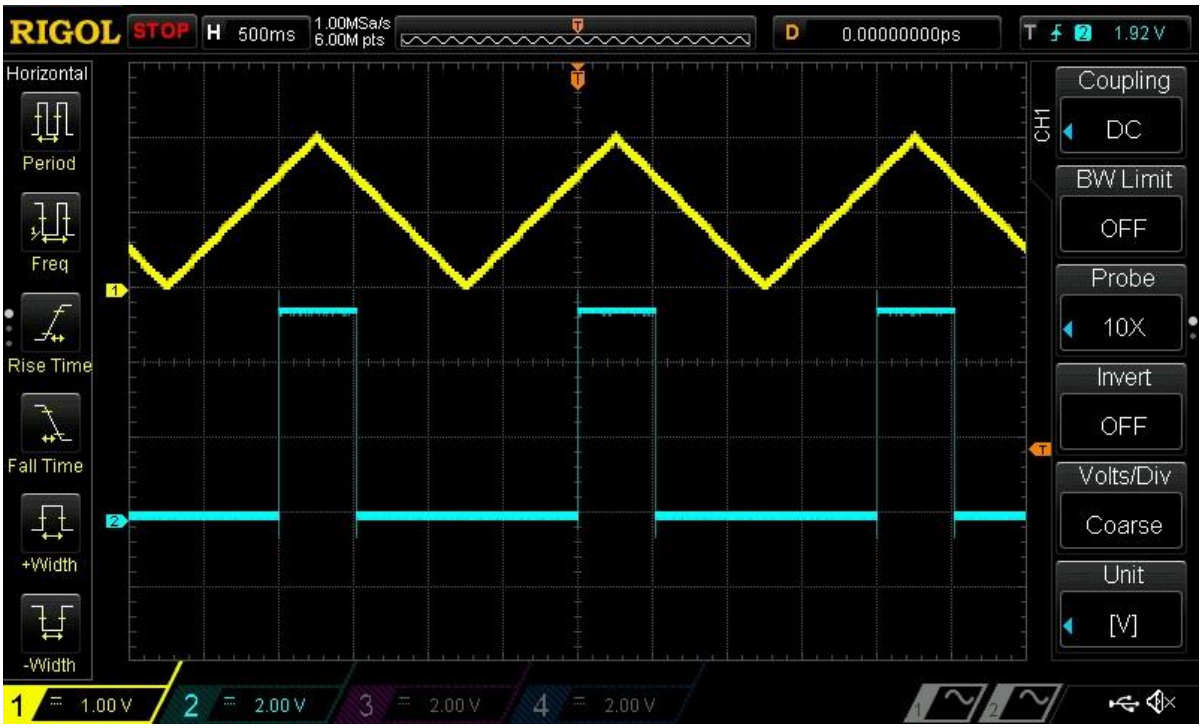

Figure 2: ACMP Output during Glitching

2. Waveform at Vref = 1504 mV, hysteresis is equal to 32 mV (zoomed rising edge).

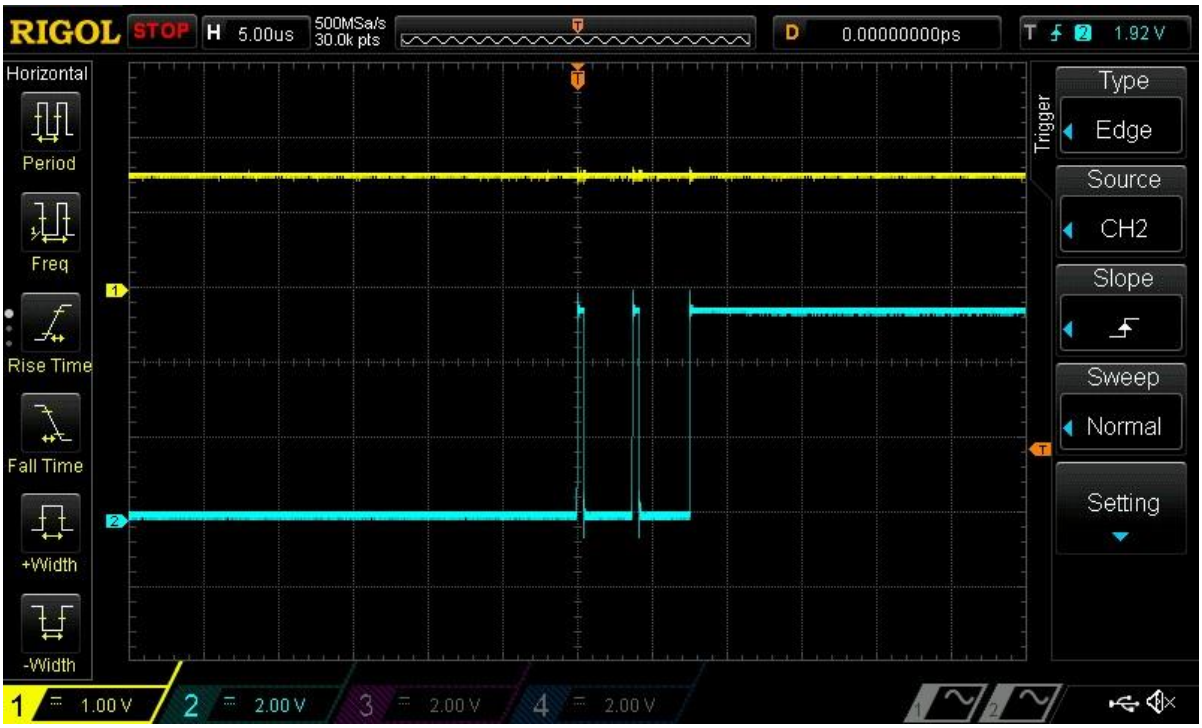

Figure 3: Zoomed ACMP Output during Glitching

3.1.4 Workaround

Use the deglitch filter connected to the ACMPxH output.

Avoid conditions described in paragraph 3.1.2.

Decrease the reference to avoid conditions described in paragraph 3.1.2 at IN- and add the IN+ gain to keep the needed threshold.

3.2 ACMPxH Erroneous Behavior when Used with Wake-Sleep Controller for Certain Vref Selection

3.2.1 Effect

ACMP0H and ACMP1H

3.2.2 Conditions

ACMPxH is used with the macrocell CNT0 configured as a wake-sleep controller (WS Ctrl).

WS Ctrl Short wake time mode is selected, for Vref range 1.312 V to 1.440 V.

WS Ctrl Normal wake time is selected, for two Vref ranges 0.832 V to 0.896 V and 1.312 V to 1.440 V.

3.2.3 Technical Description

When WS Ctrl is used for controlling the power on/off of analog macrocells ACMPs for power saving, ACMPxH shows erroneous behavior for certain Vref selection. Vref transient settling error is observed for both WS Ctrl Wake time modes, Short wake time and Normal wake time (selections under CNT0 settings).

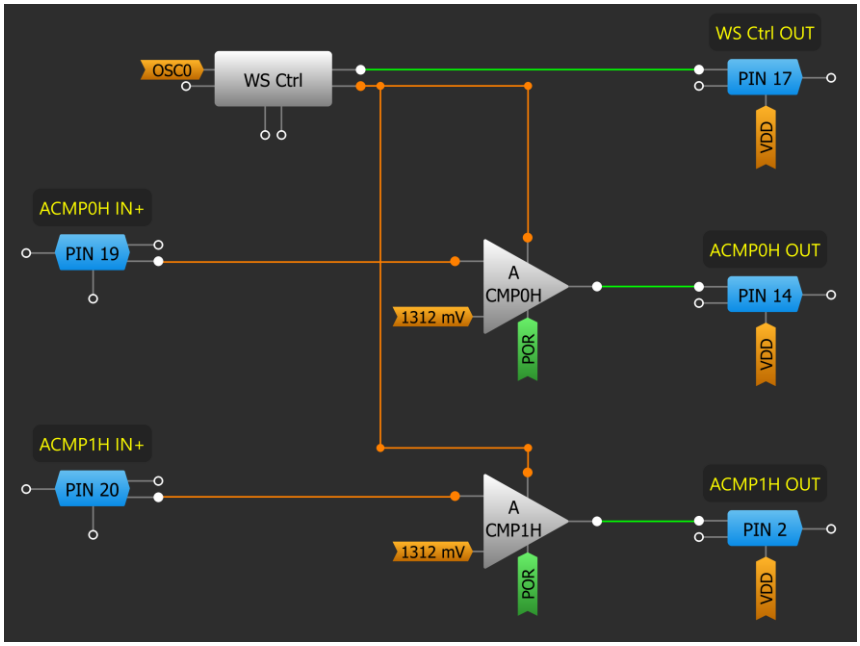

Figure 4: Testing Design

Channel 1 (yellow/top line) - PIN#19 (ACMP0H IN+)

Channel 2 (light blue/2nd line) - PIN#17 (WS Ctrl OUT)

Channel 3 (magenta /3rd line) - PIN#14 (ACMP0H OUT)

1. Waveform at Vref = 1312 mV, hysteresis is equal to 32 mV

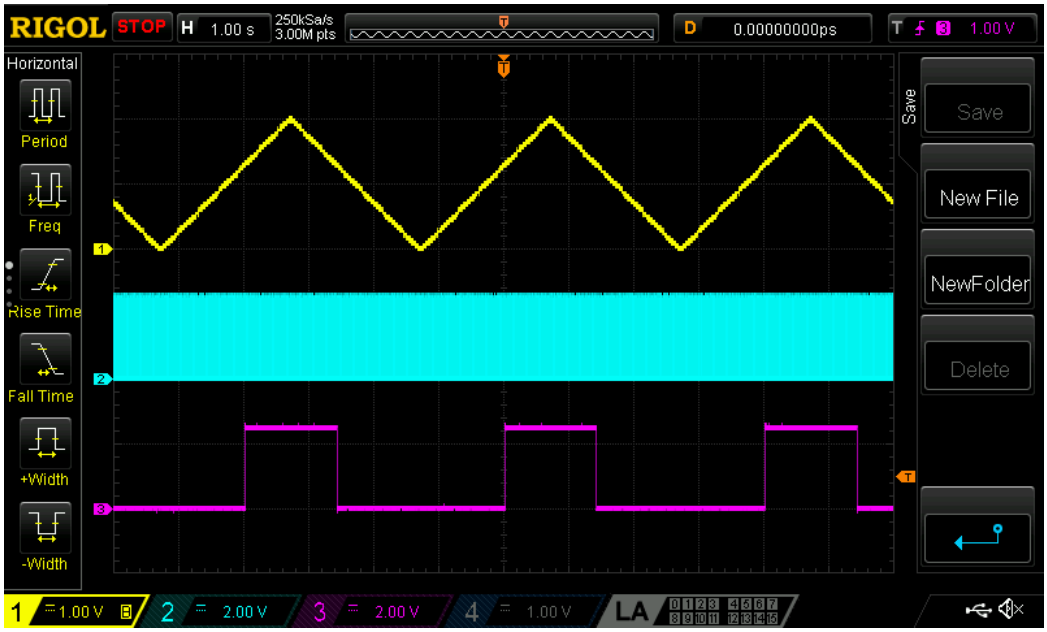

Figure 5: ACMP0H Output during Glitching

2. Waveform at Short wake time mode, Vref = 1312 mV, hysteresis is equal to 32 mV (zoomed rising edge).

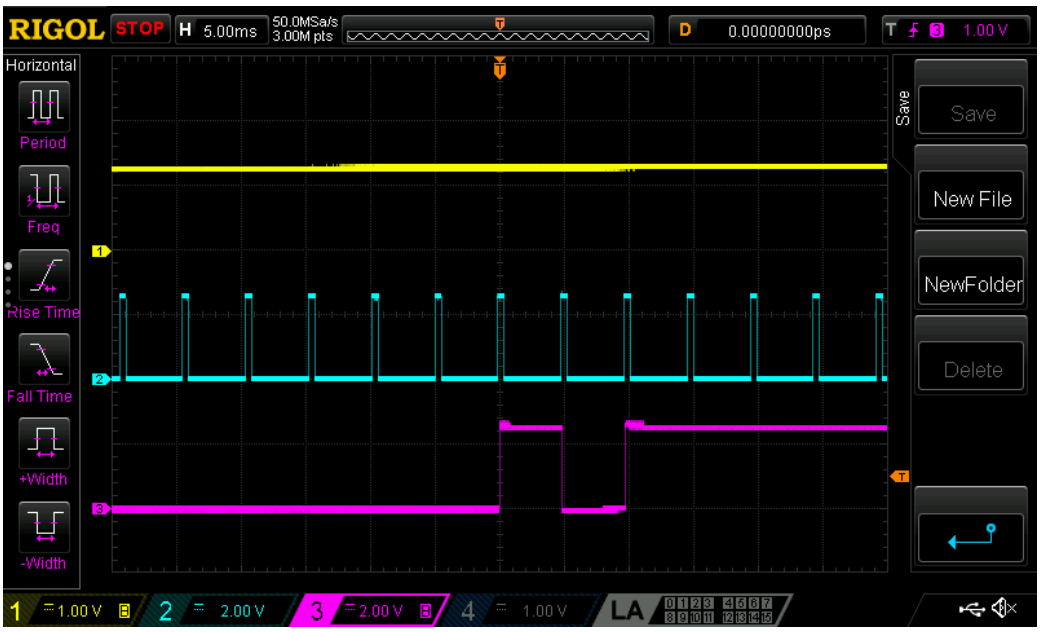

Figure 6: Zoomed ACMP Output During Glitching at Short Wake Time Mode

3. Waveform at Normal wake time mode, Vref = 1312 mV, hysteresis is equal to 32 mV (zoomed rising edge).

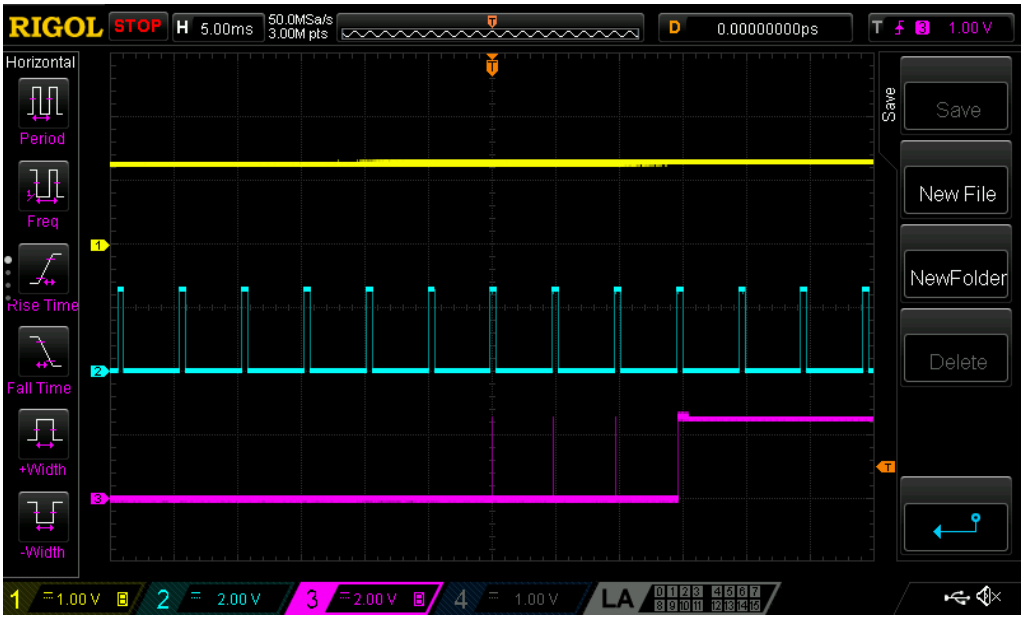

Figure 7: Zoomed ACMP Output during Glitching at Normal Wake Time Mode

3.2.4 Workaround

1. If ACMP is used with WS Ctrl counter, CNT0, avoid conditions described in paragraph 3.2.2.

2. Decrease the reference to avoid conditions described in paragraph 3.2.2 at IN- and add the IN+ gain to keep the needed threshold.

3.3 Abnormal ACMPs Behavior

3.3.1 Effect

GPIO5, ACMP0H and ACMP1H

3.3.2 Conditions

The ACMP0H IN+ source is set to V_{DD} and GPIO5 is set to Analog IO or 3-State Output

3.3.3 Technical Description

When GPIO5 is configured as “Analog Input/Output”, “Digital Input/Output in Analog In Mode”, or “3-State Output” mode, ACMP behavior may be abnormal in the following cases:

1. ACMP0H IN+ source set to V_{DD}

2. ACMP1H IN+ source set to ACMP0H IN+ source.

Each of two ACMPs has an input MUX which selects the IN+ source for the comparator. The MUX Options are shown in the Table 2.

Table 2: ACMP Input Options

ACMP IN+ MUX Options	
ACMP0H	GPIO5 V_{DD}
ACMP1H	GPIO6 ACMP0H IN+ source

In GreenPAK Designer, the input source is selected by the IN+ source dropdown within the ACMP's properties window. When input source is selected and ACMP is enabled, the analog switch connects the source to the ACMP's IN+ port.

GPIO5 can be repurposed as Digital IO if the ACMPs are disabled or if another input source is selected for the ACMP by the IN+ input MUX. Whenever GPIO5 input mode is configured as an "Analog IO" in accordance with the register definition below then the ACMP behavior may be abnormal if the ACMP is enabled and connected to another input source.

Table 3: GPIO5 Input/Output Mode Configurations

Byte	Register Bit	Signal Function	Register Bit Definition
GPIO5			
0x6A	849:848	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	851:850	Output mode configuration	00: Push-Pull 1x / 3-State Output 1x 01: Push-Pull 2x / 3-State Output 2x 10: Open-Drain 1x 11: Open-Drain 2x

There are 3 standard GPIO5 settings that use the "Analog IO" configuration: Analog input/output, Digital input/output (with "Input mode" set to Analog input), and Digital output (with "Output mode" set to 1x/2x 3-State Output). The first setting is reserved for use with the ACMP, but the other two settings use the "Analog IO" configuration as a high-impedance input.

As example Figure 8 shows the GreenPAK configured with GPIO5 as a Digital Input/Output (with "Input mode" set to Analog input and "Output mode" set to 1x Push Pull) with a 1M pull-down resistor. GPI0 is being used as a digital input and is connected to OE input of GPIO5. This is used to determine the input/output mode:

1. when OE Input is LOW, then GPIO5 is acting as Analog Input
2. when OE Input is High, then GPIO5 is acting as 1x Push Pull Output.

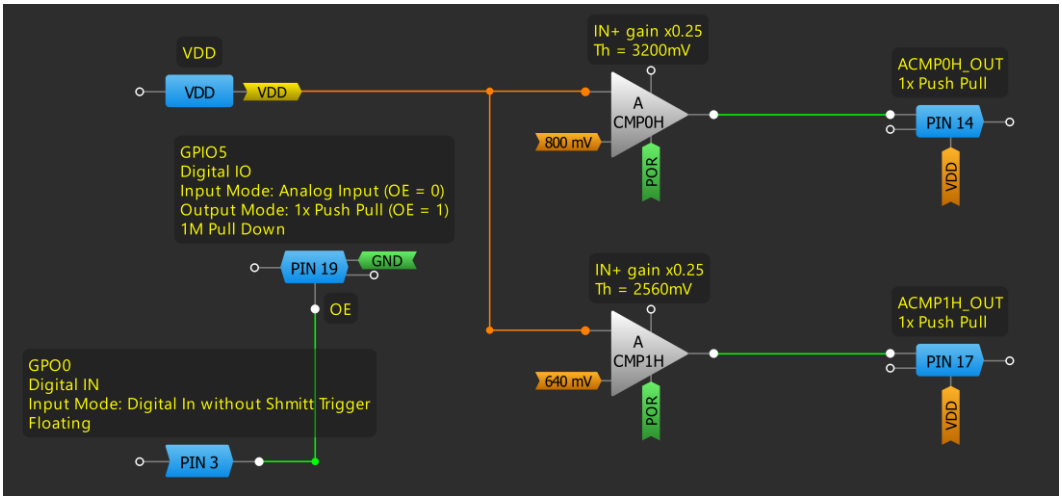

Figure 8: Testing Design

Figure 9 shows that when GPIO5 in Analog input mode then abnormal ACMPs behavior.
Channel 1 (yellow/top line) – PIN#1 (V_{DD})
D10 – PIN#2 (GPO0)
D11 – PIN#14 (ACMP0H_OUT)
D12 – PIN#17 (ACMP1H_OUT)

Figure 9: ACMPs Output Behavior

3.3.4 Workaround

There is no workaround for this behavior. With this in mind, the GPIO5 should not be used as Digital IO (with “Input mode” set to Analog input) or as digital outputs (with “Output mode” set to 1x/2x 3-State Output) if the respective ACMP is enabled and connected to another input source.

Document Revision History

Revision	Date	Description
1.4	8-Mar-2022	Renesas rebranding
1.3	9-Nov-2021	Removed fixed isuues #1 and #2 Added issue Abnormal ACMPs behavior
1.2	27-Jul-2021	Added issues #3 and #4
1.1	24-Jun-2020	Updated according to new Dialog's format

SLG47105 Errata

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.