SLG46857-A Errata Note

Abstract

This document contains the known errata for SLG46857-A and the recommended workarounds.

Contents

1. Information

Package(s)	14-pin STQFN: 3.0 mm x 3.1 mm x 0.75 mm, 0.65 mm pitch

2. Errata Summary

Issue #	Issue Title
1	Leakage from ACMP IN+ to Analog Input Pins

3. Errata Details

3.1 Leakage from ACMP IN+ to Analog Input Pins

3.1.1. Effect

GPIO4/5/6/7, ACMP0/1H, ACMP2/3L

3.1.2. Conditions

Multiple input sources are connected to the ACMP IN+ port simultaneously.

3.1.3. Technical Description

When configured in “Analog IO” mode, GPIO4/5/6/7 can experience abnormal leakage behavior. This behavior occurs when multiple input sources are simultaneously connected to the ACMP IN+ port. Each of the 4 ACMPs has an input MUX which selects the IN+ source for the comparator. The MUX options are shown in the table below.

Table 1. ACMP Input Options

ACMP IN+ MUX Options	
ACMP0H	GPIO4 Buffered GPIO4 V_{DD}
ACMP1H	GPIO5 Buffered GPIO5 ACMP0H IN+ source
ACMP2L	GPIO6 ACMP0H IN+ source ACMP1H IN+ source
ACMP3L	GPIO7 ACMP2L IN+ source VREF0 output

In the GreenPAK Designer, the input source is selected by the IN+ source dropdown within the ACMP’s properties window. When an input source is selected and the ACMP is enabled, an analog switch connects the source to the ACMP’s IN+ port. If multiple sources are connected to the ACMP’s IN+ port, there will be leakage between the sources.

The GPIOs shown above can be repurposed as Digital IOs if the ACMPs are disabled or if another input source is selected for the ACMP by the IN+ input MUX. Whenever a GPIO input mode is configured as an “Analog IO” in accordance with the register definition below, the GPIO will be connected to the ACMP’s IN+ port through an internal switch. This can create a leakage scenario if the ACMP is enabled and connected to another input source.

Table 2. GPIO Input Mode Configurations

Byte	Register Bit	Signal Function	Register Bit Definition
GPIO4			
0x66	821	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	822		
GPIO5			
0x67	829	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	830		
GPIO6			
0x68	836	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	837		
GPIO7			
0x69	843	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	844		

There are 3 standard GPIO settings that use the “Analog IO” configuration: Analog input/output, Digital input/output (with “Input mode” set to Analog input), and Digital output (with “Output mode” set to 1/2/4x 3-State Output). The first setting is reserved for use with the ACMP, but the other two settings use the “Analog IO” configuration as a high-impedance input. It is important to note that these input modes won’t be high impedance if the ACMP is enabled and connected to another input source. When two signals are connected to the ACMP’s IN+ source, the voltage level at the ACMP’s input depends upon the drive strength of the competing sources.

Figure 1 shows the GreenPAK configured with GPIO4 as a Digital IO with a 1 MΩ pull-down resistor. Since the OE pin is connected to 0 V, this pin is acting as an “Analog IO.” As seen in Table 1, GPIO4 and VDD are both input options for ACMP0H. In this example, GPI0 is being used as a digital input to enable and disable the ACMP.

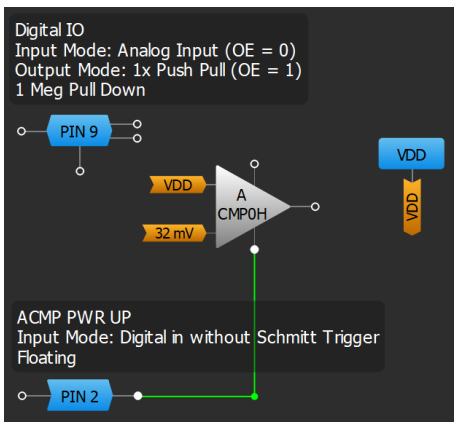

Figure 1. GreenPAK Input Structure Test Schematic

Figure 2 shows that GPIO4 in analog input mode is pulled HIGH by the VDD signal whenever the ACMP is enabled despite having an internal pull-down resistor. This behavior is cause by an internal connection between VDD and GPIO4. Similar behavior can be reproduced when one ACMP's IN+ port is connected to another ACMP's IN+ port.

CH1 (Yellow): ACMP PWR UP (GPI0)

CH2 (Light Blue): Digital IO w/ Analog Input Mode Configuration (GPIO4)

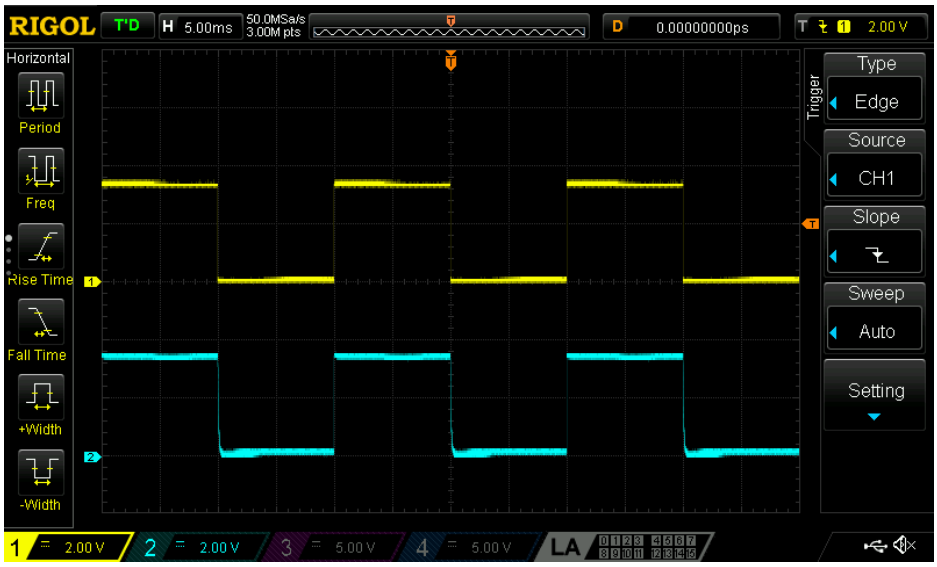

Figure 2. ACMP Input Structure Behavior

3.1.4. Workaround

If an ACMP is disabled, the GPIO associated with that ACMP will operate as expected under any configuration. Please reference Table 1 for more information regarding which GPIOs are associated with which ACMPs.

When the ACMPs are enabled, it is possible to inadvertently connect multiple ACMP sources together through the input structure. This is possible when the ACMP input is connected to a source other than its analog GPIO and that GPIO's input mode is set to "Analog IO".

There is no workaround for this behavior. With this in mind, the GPIOs should not be used as digital IOs (with "Input mode" set to Analog input) or as digital outputs (with "Output mode" set to 1/2/4x 3 State Output) if the respective ACMP is enabled and connected to another input source.

4. Revision History

Revision	Date	Description
1.00	Sep 12, 2024	Initial release.

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