Errata

SLG46580 Errata

CE-GP-002

Abstract

This document contains the known errata for SLG46580 and the recommended workarounds.

1 Information

Packages	20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch

2 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Long 2 MHz OSC Settling Time
2	Possible Glitch on ACMP Output
3	Possible Glitch on ACMP Output
4	ACMP's Erroneous Behavior when Internally Tied to the LDO's Input
5	Non-Zero LDO Output Voltage Step during LDO Enable
6	FILTER Cell does not Filter Out Repetitive Glitches
7	Incorrect I2C Reads of the 8-bit Counter Registers
8	Inaccurate Data Transfer between the RTC's Shadow Buffer and the RTC's Counter Registers
9	Invalid I2C Data Return for Initial "Current Address Read" or "Sequential Read" after an I2C Write
10	ACMP Additional IN- Leakage Current
11	Input Glitch Pattern Combination into DLYs Fails to Trigger Auto Power On of 25 kHz or 2 MHz OSC
12	OSC Long Start-Up Time

3 Errata Details

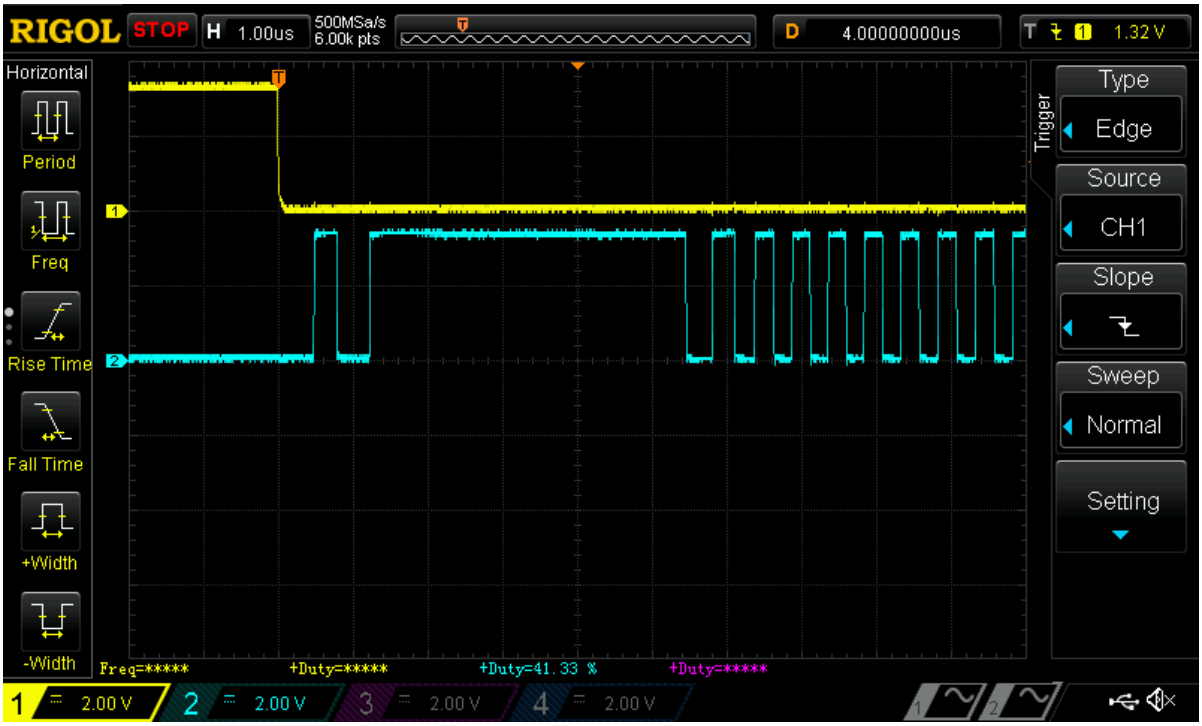
3.1 Long 2 MHz OSC Settling Time

3.1.1 Effect

OSC, Counter, Delay

3.1.2 Technical Description

2 MHz OSC has an additional ~ 9 cycles settling period. Higher V_{DD} shows longer settling time.



Channel 1 – OSC Power Down; Channel 2 –OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

3.1.3 Workaround

- Enable Fast Start-up option. Fast Start-up means forcing bias ready at the power-up instead of automatic enabling at OSC event. The standby current consumption difference between Fast start-up disabled and enabled is only an additional 300 nA.
- Use the “Force power on” OSC power control option to make the OSC operate at all times. However, this will cause increased constant current consumption.

3.2 Possible Glitch on ACMP Output

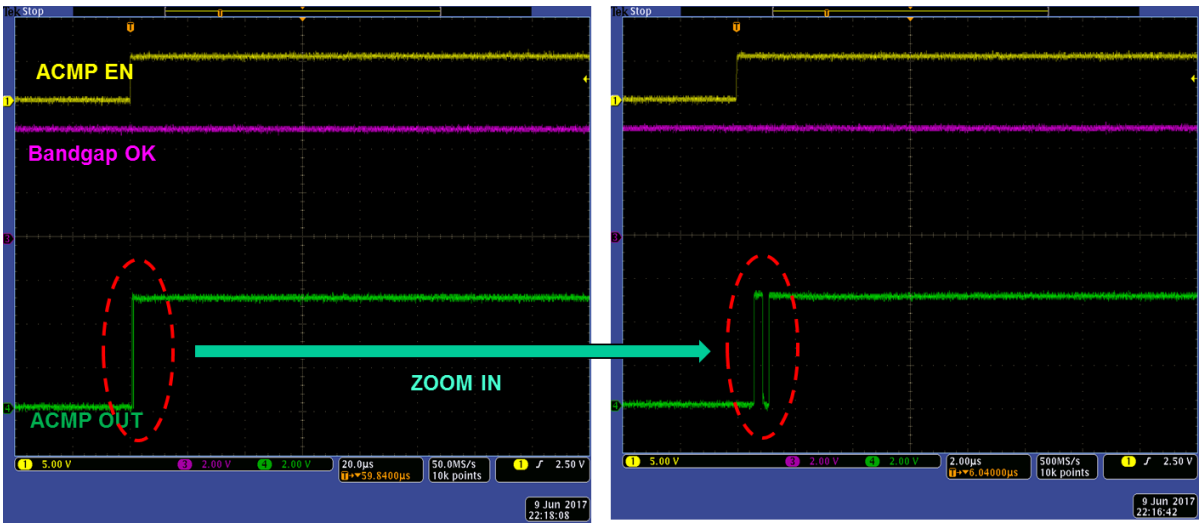
3.2.1 Effect

ACMP

3.2.2 Technical Description

After power-up, if LDO is enabled earlier than ACMP, its output may generate a glitch.

V_{DD} = 5.0 V, ACMP IN+ > IN-, one of LDOs enabled.



Because BG_OK is already released by LDO, there is no gating signal. Depending on the ACMP VREF condition & the positive input value, it is possible for the ACMP to have a glitch. Subsequently, the other ACMP will not have an issue unless the customer repeats LDO enable first and ACMP later during power stable.

3.2.3 Workaround

Use both edge delay on the output to filter out the glitch.

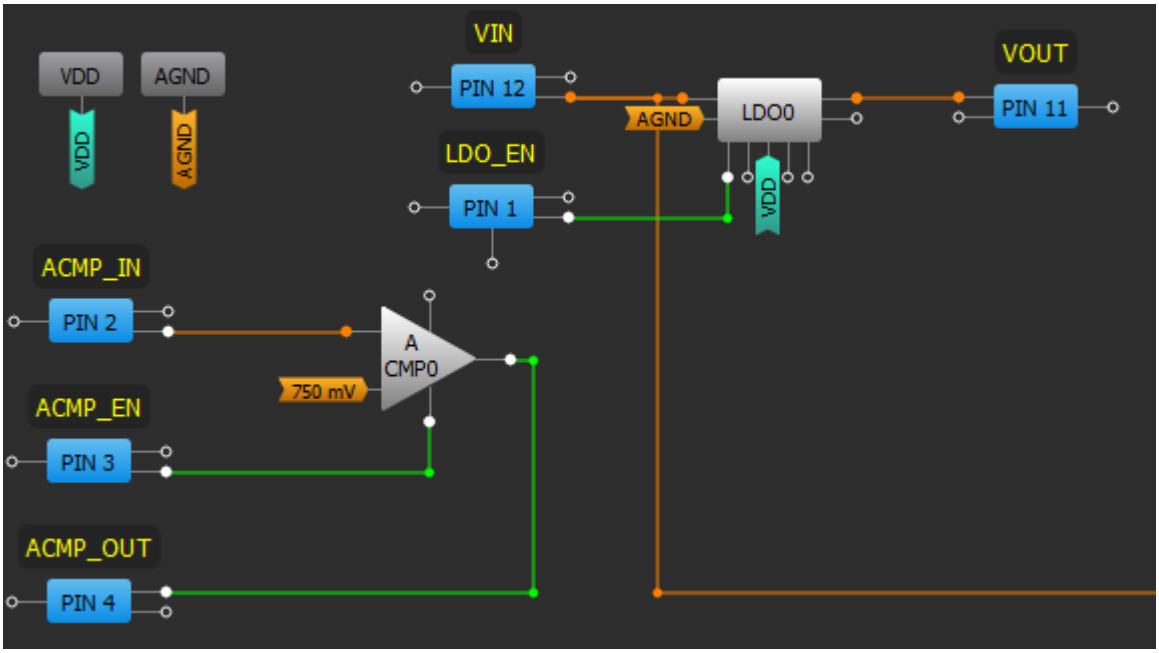
3.3 Possible Glitch on ACMP Output

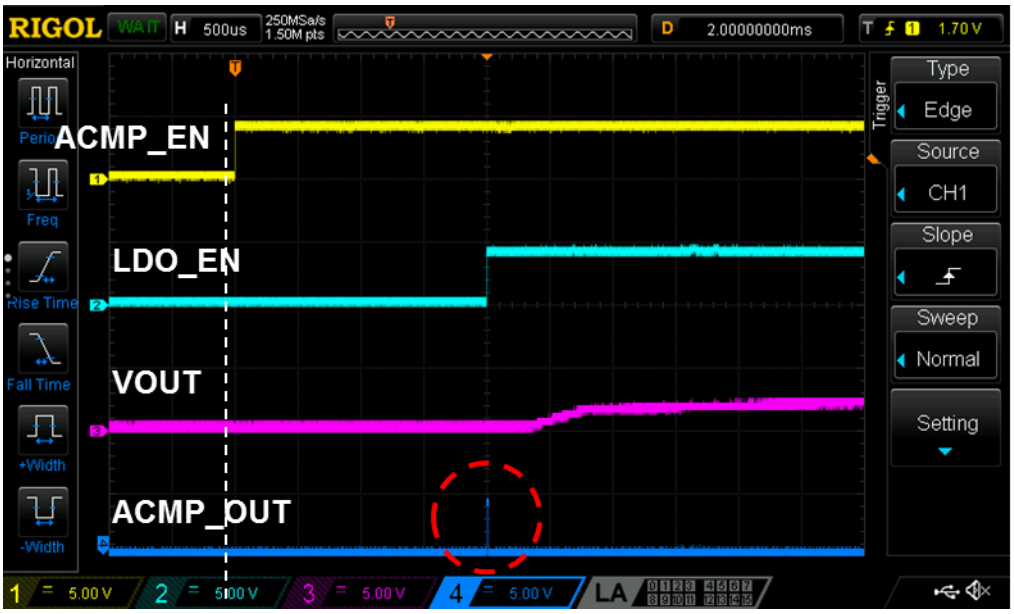
3.3.1 Effect

ACMP

3.3.2 Technical Description

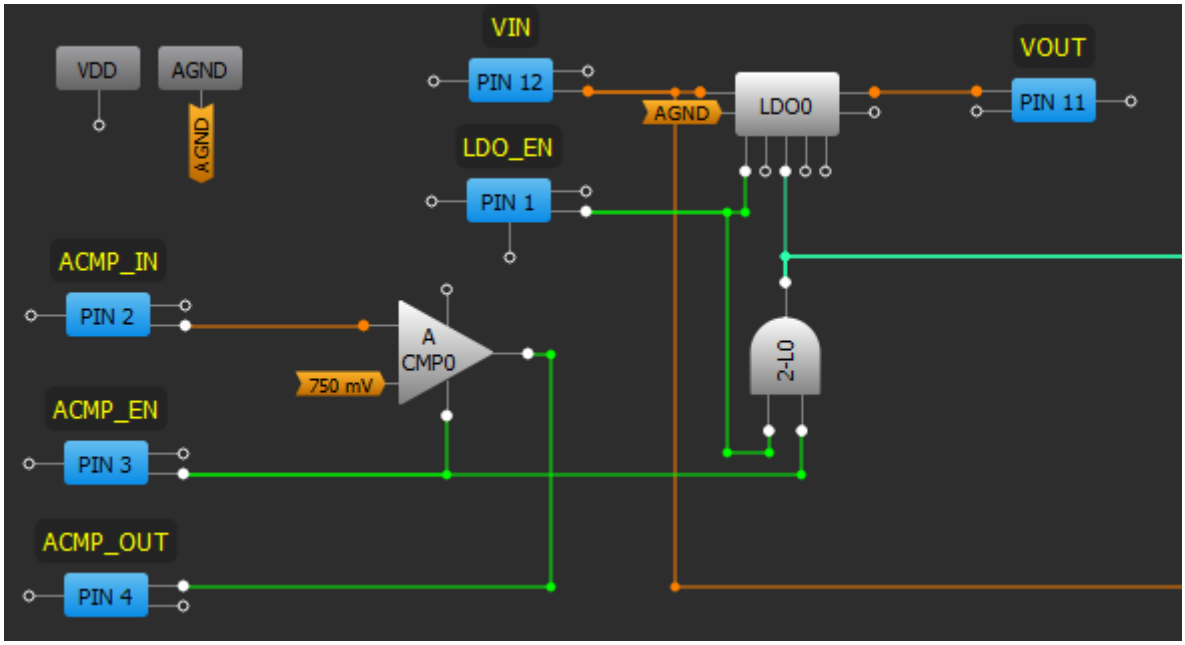
If an LDO's Low Power Mode is selected (for example tied to V_{DD}) a glitch may appear on the ACMP's output after the first LDO is enabled. When the first LDO is turned on, the Low Power Mode switch causes a drop in the internal bandgap voltage that is used to derive the ACMP reference voltages.





3.3.3 Workaround

- Use both edge delay on the output to filter out the glitch.
- Use some logic to avoid turning on Low Power Mode before enabling LDO and powering up the ACMP. Example is shown below.



3.4 ACMP's Erroneous Behavior when Internally Tied to the LDO's Input

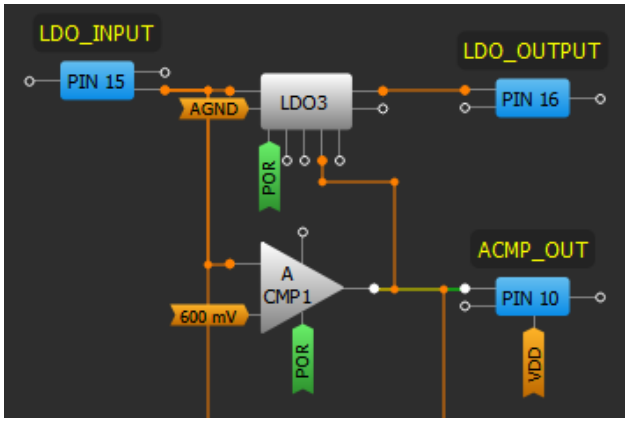
3.4.1 Effect

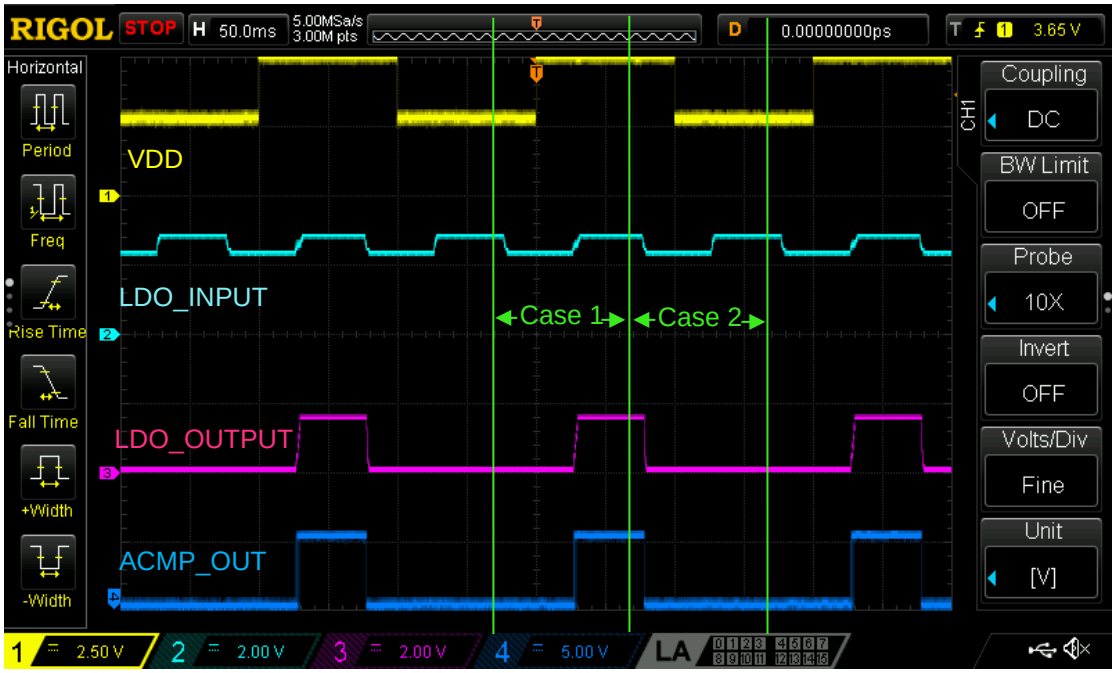
ACMP and LDO

3.4.2 Technical Description

If an LDO's VIN pin (LDO_INPUT) has an internal connection (depicted with an orange wire) to the ACMP's IN+ port, the ACMP's output may give an erroneous result with respect to the LDO's input voltage. The switch between the LDO's VIN pin and the ACMP's IN+ port is implemented using an NMOS-only based transmission gate with its gate controlled by logic supplied from V_{DD}. As a result, this switch is unable to pass LDO input voltages that are close to V_{DD}. This can result in the ACMP's IN+ port seeing a lower voltage than the actual voltage present at LDO_INPUT. This lower input voltage may cause the output of the ACMP to behave unexpectedly.

If the LDO's UVLO feature is enabled, the ACMP's output will cause unexpected LDO behavior that results from the previously described transmission gate voltage drop.





Case 1: proper behavior at V_{DD} = 5 V.
With a 5 V V_{DD}, the NMOS transmission gate passes the 2.25 and 2.75 V LDO_INPUT pin voltages to the ACMP's IN+ port. When the input voltage exceeds the 2.4 V IN- threshold of the ACMP, the LDO is enabled.

Case 2: erroneous behavior at V_{DD} = 2.75 V.
When the V_{DD} is reduced to 2.75 V, the NMOS transmission gate is unable to pass LDO_INPUT's full magnitude to the ACMP's IN+ port. Since the IN+ port of the ACMP doesn't exceed the 2.4 V IN- threshold, the ACMP's output stays low and keeps the LDO disabled.

3.4.3 Workaround

If the GreenPAK's V_{DD} is always powered up before the LDO's VIN input, you can externally short the LDO's VIN to another dedicated analog input pin for the desired ACMP.

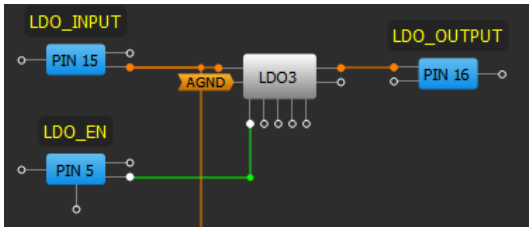
3.5 Non-Zero LDO Output Voltage Step during LDO Enable

3.5.1 Effect

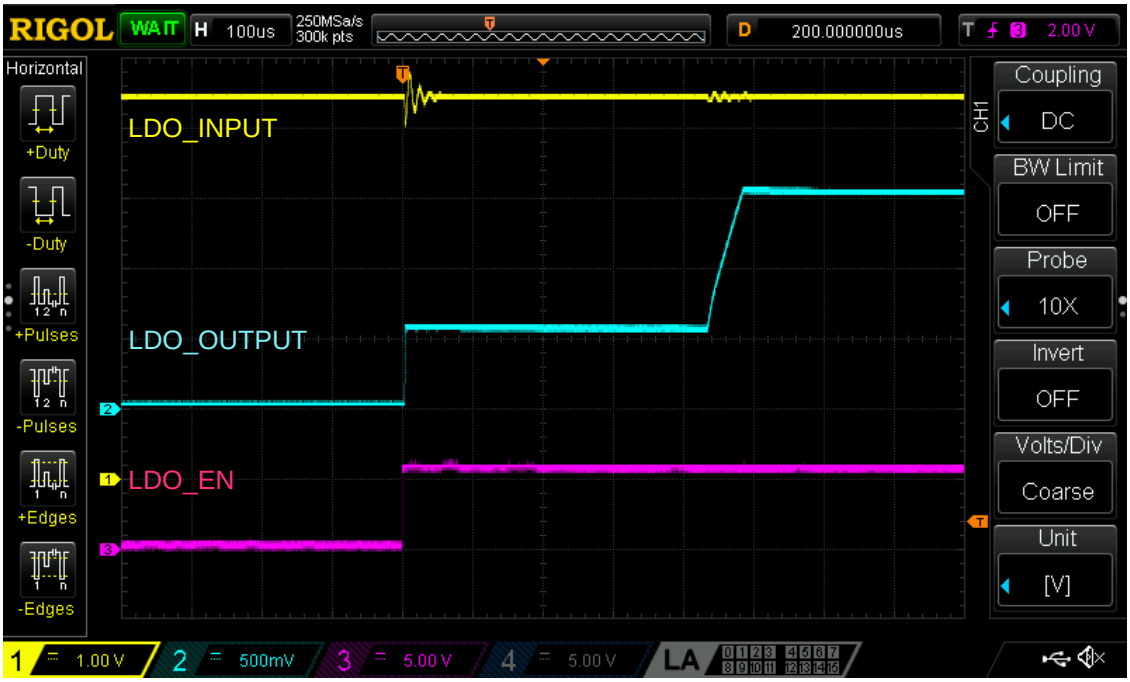
LDO

3.5.2 Technical Description

When a GreenPAK's first LDO is enabled, the LDO's VOUT will step to a non-zero voltage during its 500 µs wait time. The magnitude of this step is directly proportional to the LDO's VIN and the GreenPAK's V_{DD}. With a large LDO input voltage and V_{DD}, this step can exceed 500 mV.



V_{DD} = 5.5 V, LDO_INPUT = 5.5 V, all other LDOs disabled.



3.5.3 Workaround

If your GreenPAK design has an unused LDO, you can reduce the magnitude of this voltage step by keeping an unused LDO enabled in high power mode.

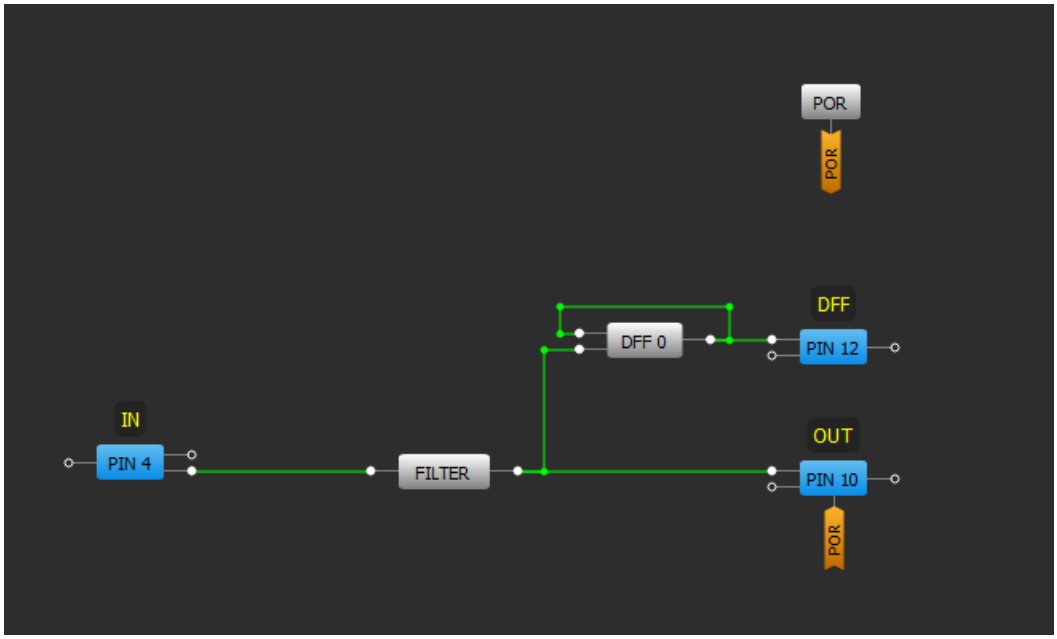
3.6 FILTER Cell does not Filter Out Repetitive Glitches

3.6.1 Effect

Filter

3.6.2 Technical Description

If the FILTER cell's input signal contains multiple consecutive pulses within short time intervals, the FILTER cell may not filter the input pulses as expected. The errant behavior applies only to repeated input pulses and depends on both their frequency and duty cycle.



Channel 1 (yellow/top line) – PIN#4 (IN).
Channel 2 (light blue/2nd line) – PIN#10 (OUT).
Channel 3 (magenta /3rd line) – PIN#12 (DFF).

1. Period is 60 ns. Pulse width is 10 ns, DC = 16.7 % (correct functionality).

2. Period is 60 ns. Pulse width is 20 ns, DC = 33.3 % (incorrect functionality).

3. Period is 60 ns. Pulse width is 30 ns, DC = 50 % (incorrect functionality).

4. Period is 60 ns. Pulse width is 40 ns, DC = 66.67 % (correct functionality).

3.6.3 Workaround

Currently, there is no workaround for this issue. The FILTER block correctly filters isolated glitches, but it shouldn't be used to filter repetitive, high frequency input signals.

3.7 Incorrect I²C Reads of the 8-bit Counter Registers

3.7.1 Effect

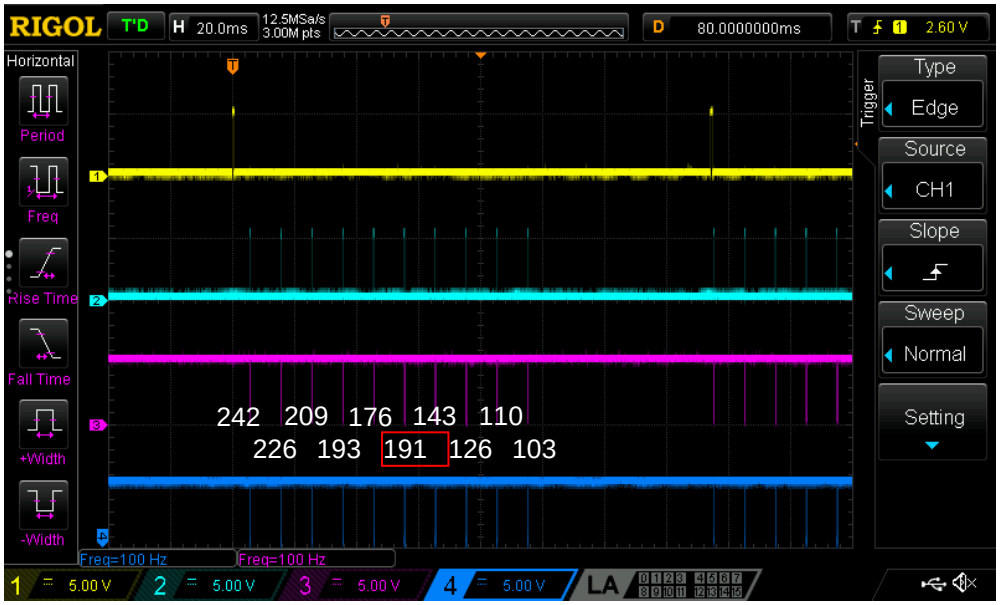
CNT2/DLY2 and CNT4/DLY4

3.7.2 Technical Description

Asynchronous interaction between the CNT/DLY clock input and the I²C latch signal (generated by an I²C read command of the CNT/DLY block's count value) can result in an incorrect I²C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I2C read register might be loaded incompletely if the I²C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I²C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I²C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

Channel 1 (yellow/top line) – PIN#2 (CNT2/DLY2 Out).
Channel 2 (light blue/2nd line) – PIN#1 (I²C Read Triggers).
Channel 3 (magenta /3rd line) – PIN#8 (I²C SCL).
Channel 3 (dark blue /4th line) – PIN#9 (I²C SDA).



3.7.3 Workaround

If the possibility of incorrect I²C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I²C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look-up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I²C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I²C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I²C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select "Ext. CLK. (From Matrix)." This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, a LUT can be used to gate the clock during an I²C read.

3.8 Inaccurate Data Transfer between the RTC's Shadow Buffer and the RTC's Counter Registers

3.8.1 Effect

RTC

3.8.2 Technical Description

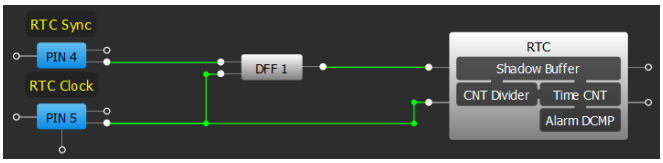
The SLG46580's I²C feature uses an internal shadow buffer to read from and write to the RTC's count registers. The data transfer between the count registers and the shadow buffer can be triggered through either the RTC block's Sync input or I²C.

Issue 2 describes an issue related to asynchronously clocking and latching data for I²C reading in various CNT/DLY blocks. Similar behavior affects the RTC block. When triggered by an I²C read, the data transfer from the counter registers to the shadow buffer should return the correct data, but when the I²C block triggers a data write to the counter registers or when the Sync input triggers the data transfer, a simultaneous rising edge on the Clock input might corrupt the data transfer.

3.8.3 Workaround

As described in Issue 2, one can guarantee proper operation with I²C by disabling the clock of the RTC block during I²C reads and writes. This can be done by disabling the oscillator clocking the RTC or by gating the matrix clock using a LUT.

Alternatively, if the Sync input is used, one can synchronize the Clock and Sync inputs using a DFF as shown below. This method requires the RTC's Sync input to have an active high pulse width that exceeds 1.5 times the period of the Clock input.



3.9 Invalid I²C Data Return for Initial "Current Address Read" or "Sequential Read" after an I²C Write

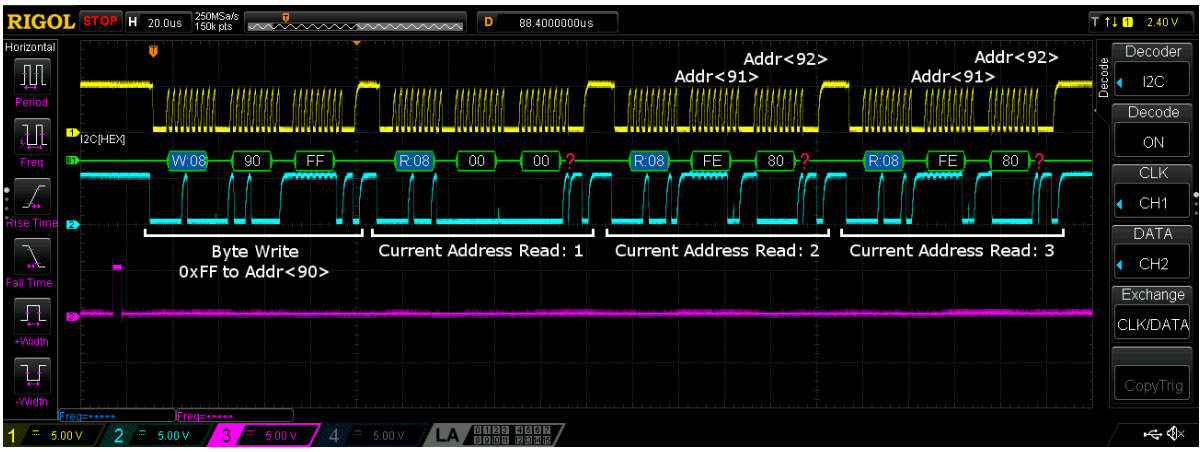
3.9.1 Effect

I²C

3.9.2 Technical Description

The first "Current Address Read" or "Sequential Read" command following an I²C "Byte Write" or a "Sequential Write" command will produce incorrect data. Additional read commands will return the expected data. See the waveform below for more information.

Channel 1 (yellow/top line) – PIN#8 (SCL).
Channel 2 (light blue/2nd line) – PIN#9 (SDA).
Channel 3 (magenta /3rd line) – I²C Software Trigger.
Note: In the GreenPAK test design, Addr<91> and Addr<92> expect FE and 80 respectively.



3.9.3 Workaround

If possible, use the "Random Read" command as described in the datasheet for SLG46580. This command will output the correct data.

If you expect consecutive reads of the same register, we recommend sending a "Random Read" command to the register preceding the register of interest. After the "Random Read" command finishes, the chip's register pointer will increment to the desired register and the following "Current

Address Read" or "Sequential Read" commands will produce the correct data. Note that the "Current Address Read" and "Sequential Read" commands don't increment the GreenPAK's register pointer.

3.10 ACMP Additional IN- Leakage Current

3.10.1 Effect

ACMP, PIN

3.10.2 Technical Description

The SLG46580 has an additional leakage current through the PIN connected to the ACMP IN- input when all of the ACMPs are powered down. Typically, leakage through the PIN connected to IN- is much less than 1 µA. But when the ACMP is powered down and voltage is applied to the PIN, the leakage current may grow up to several µA (depending on the V_{DD} and voltage applied).

3.10.3 Workaround

Currently there is no workaround for this issue.

3.11 Input Glitch Pattern Combination into DLYs Fails to Trigger Auto Power On of 25 kHz or 2 MHz OSC

3.11.1 Effect

25 kHz / 2 MHz OSC

3.11.2 Technical Description

Auto Power On can potentially fail to enable OSC when all following conditions are present together:

- 25 kHz or 2 MHz OSC is in Auto Power On mode.
- DLYs are clocked by such OSC.
- Input to one more such DLY have glitches < 200 ns.
- OR of OSC trigger signals from all DLYs clocked by same OSC together form a long+short glitch pattern with precise (ns) timings as shown in Figure 1. The trigger signal generation per DLY is detailed in section **Error! Reference source not found.**.
- During glitch period, no other DLY is active, meaning has already enabled OSC.

OSC generators have an Auto Power On mode which can be selected to automatically power on the OSC only when needed, such as when a DLY needs to count OSC cycles to time the delay output, thereby reducing quiescent power. Each individual DLY starts waiting in an inactive state, and when upon receiving an input edge (of polarity set by DLY configuration) then sets its individual trigger signal high. For example, in a rising-edge DLY, a rising edge input sets this trigger high. For a falling-edge, the situation is inverted. In either case (or both edge DLY), the individual DLY trigger is reset if either an opposite edge is detected (therefore, canceling the DLY function) or the DLY finishes timing its output upon reaching the desired count per its setting. Therefore, an input pulse shorter than the DLY time is filtered out. The global Auto Power On circuitry then takes the OR of all the individual DLY triggers and subsequently sends the controller enable signal to activate the OSC.

For this chip, the Auto Power On circuitry of the 25 kHz/2 MHz generators contains a circuit errata, which can potentially fail to power on the OSC for a specific pattern and timing of the OR of all related DLY trigger signals. The pattern is shown in Figure 1 (boxed in red) and consists of a relatively longer pulse (~145 ns) followed by a shorter (~5 ns) glitch of opposite polarity.

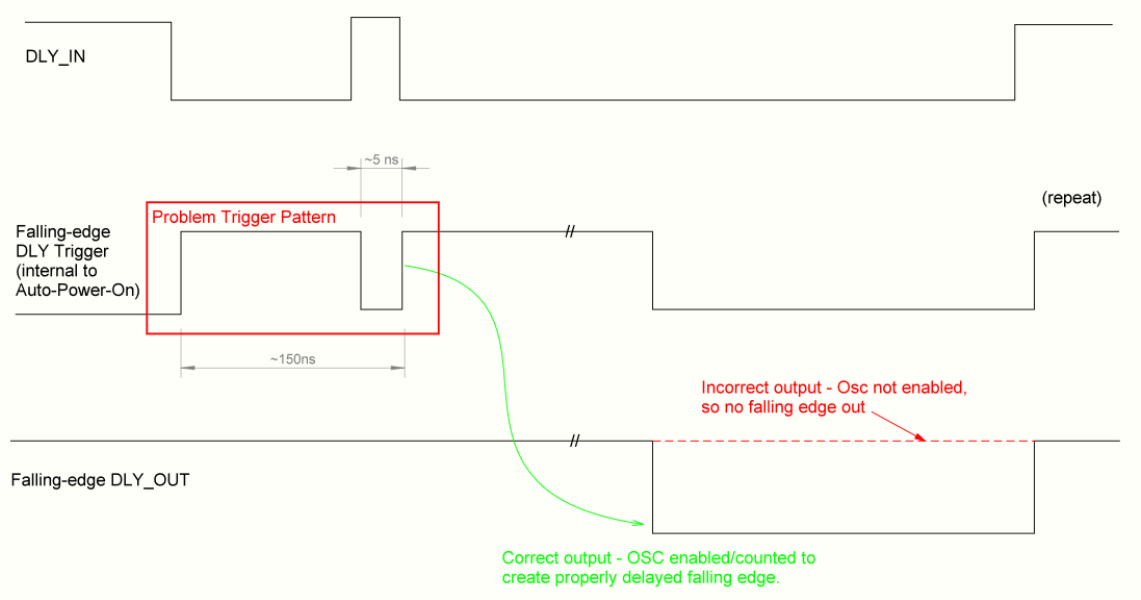


Figure 1: Problem Trigger Pattern

The error is difficult to capture as the timing must be exact within ns, and short (ns) pulses are difficult to generate glitch precise enough to induce the problem. GPIO naturally filter out ns pulses, so for purposes of errata capture, two simultaneous falling-edge DLY circuits (as shown in Figure 2) were used. By lining up two delays precisely at a particular timing relationship, we can use the internal Auto Power On (OR logic) to generate the glitch pattern necessary to cause the error.

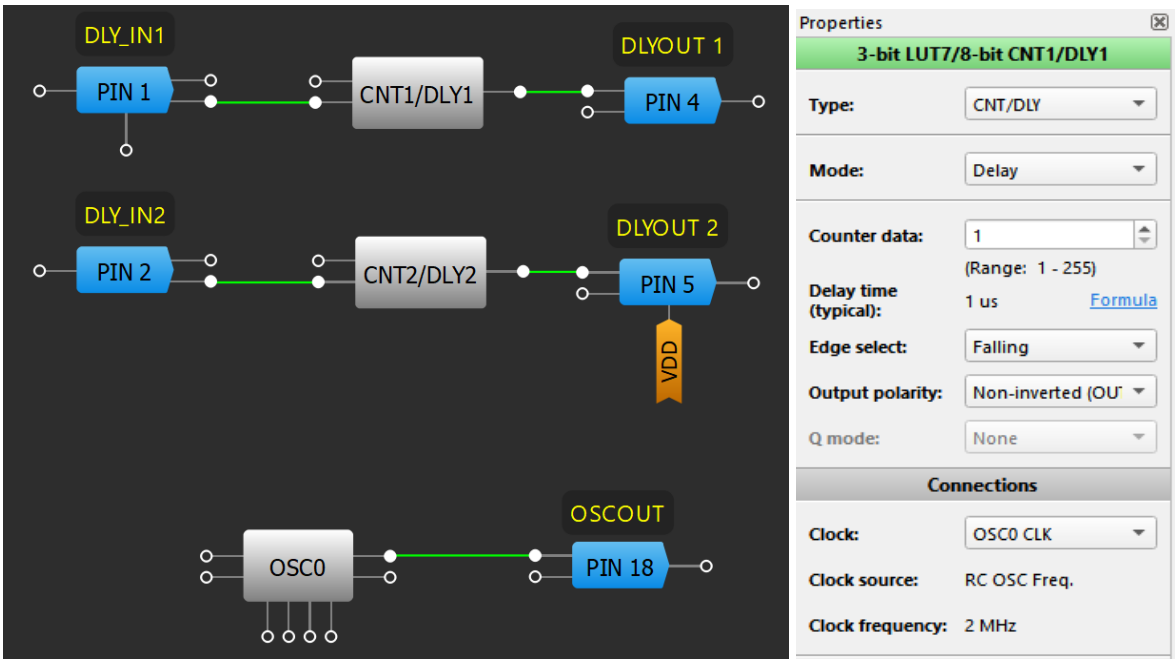


Figure 2: Test Circuit

Figure 3 shows a series of DLY output events are missing, where the OSC is correspondingly not triggering when it was supposed to. Figure 4 is a zoom in of the boxed region from Figure 3. The total glitch/chatter time was measured in this case at 152 ns. By using the composite OR of the two delay channels, we can asynchronously strobe with tiny frequency variations, and so tune the timing to induce this errata. Note that the error is not persistent – the system is recovered when all DLYs are returned to inactive state, such as when input of falling edge DLY goes high, thus canceling delay, or after DLY out finishes.

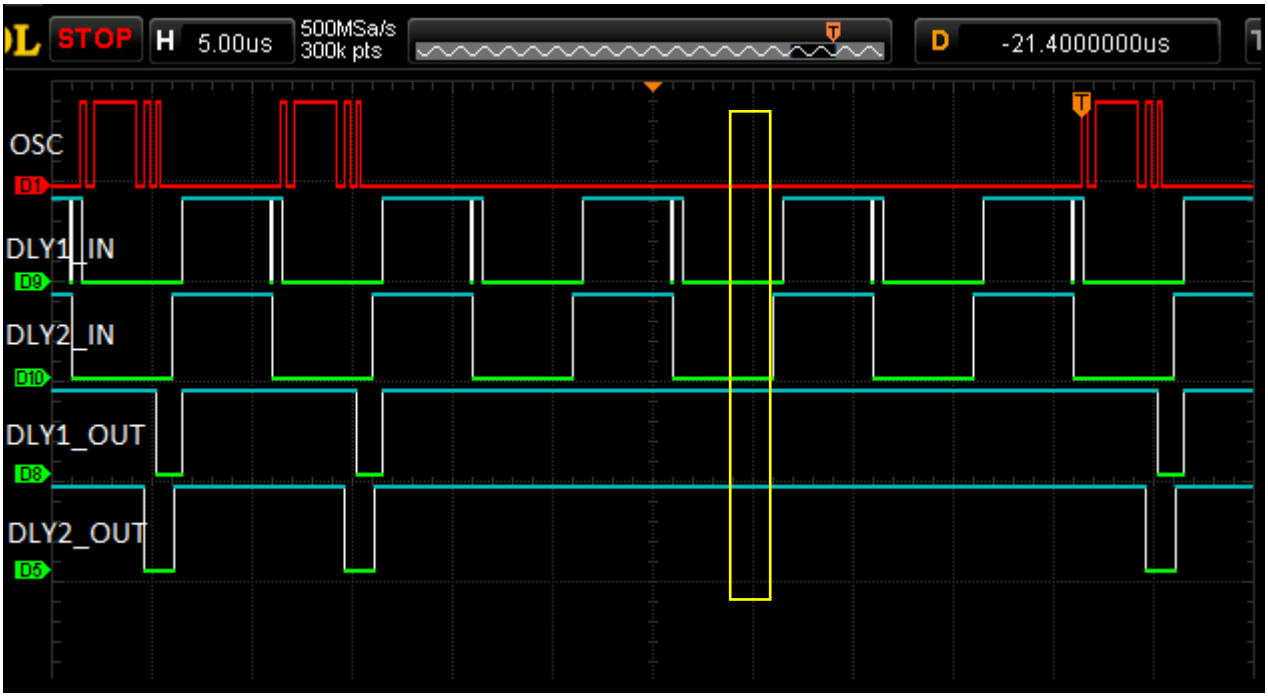


Figure 3: Errata Capture (Zoom Out)

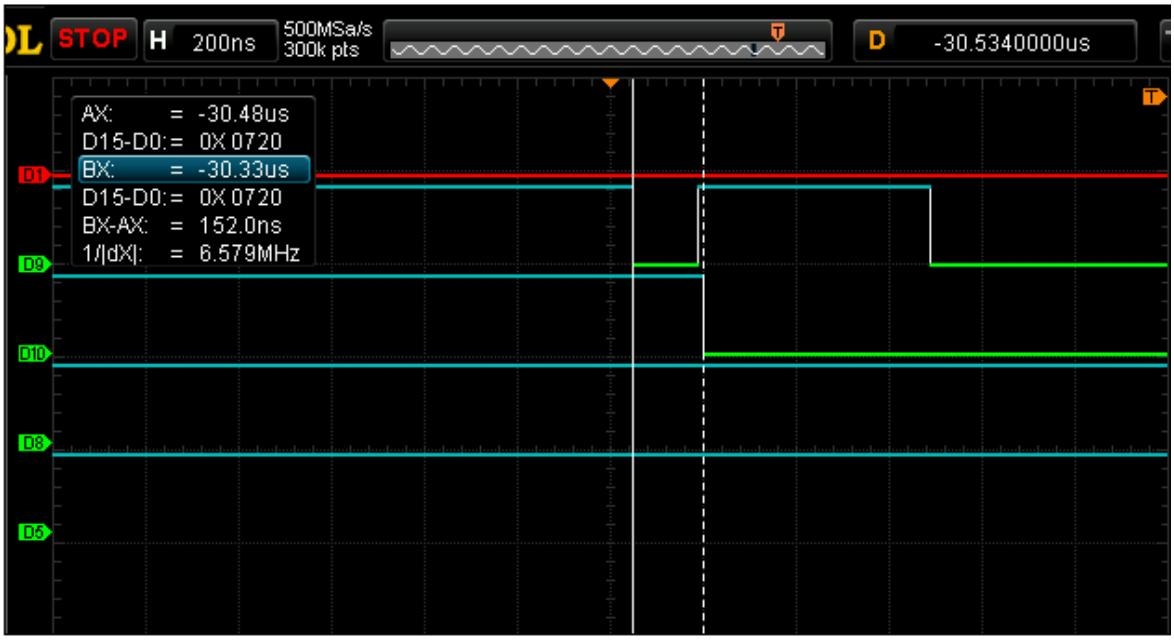


Figure 4: Errata Capture (Zoom In)

3.11.3 Workaround

Any one of the following prevents the issue:

1. Use signal conditioning circuits to prevent glitch on DLY inputs < 200 ns. Examples:
   a. ACMP with Hysteresis
   b. External RC in front of Digital Input with Schmitt Trigger
   c. Filter cell.
2. Set OSC power mode to Force Power On mode instead of Auto Power On.
3. Use different oscillator, such as 25 MHz Ring OSC, which does not have Auto Power On issue.

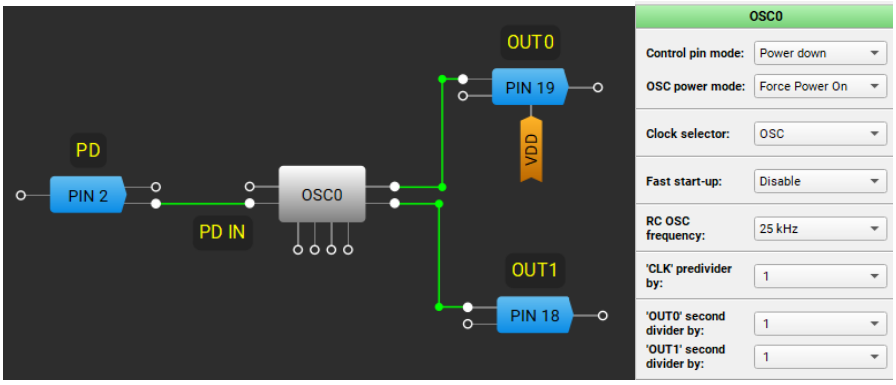
3.12 OSC Long Start-Up Time

3.12.1 Effect

When a short pulse is applied to the PWR DOWN input, the oscillator exhibits a long start-up time.

3.12.2 Conditions

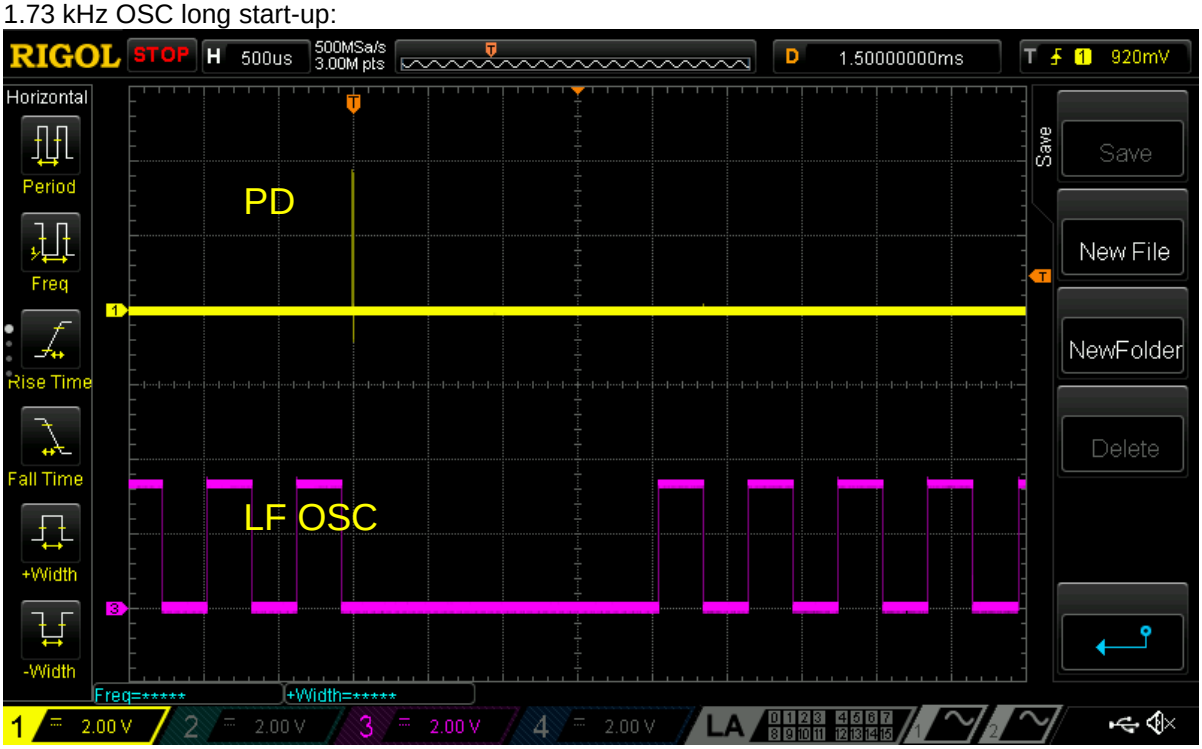
Short pulse of less than ~40ns is applied to PWR DOWN OSC.



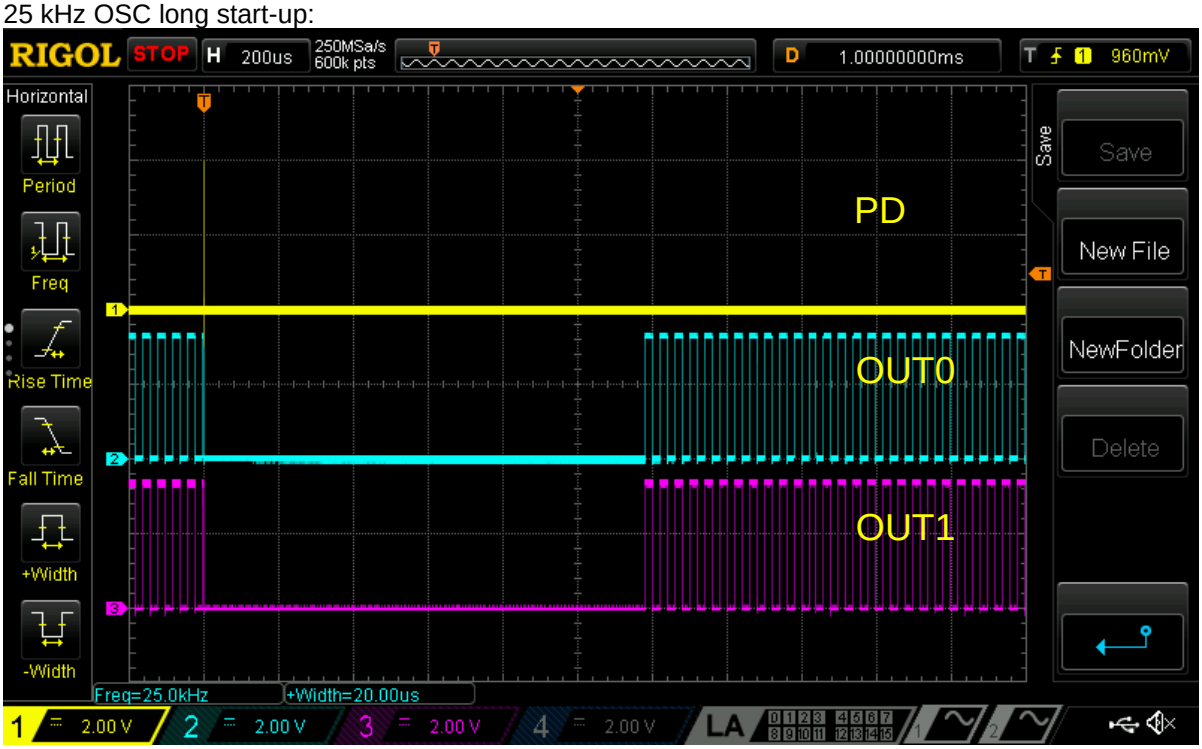
3.12.3 Technical Description

If a pulse with a duration of less than ~40 ns is applied to the PWR DOWN input of an oscillator, the oscillator outputs remain stuck for milliseconds.
The issue is observed for all available oscillators.

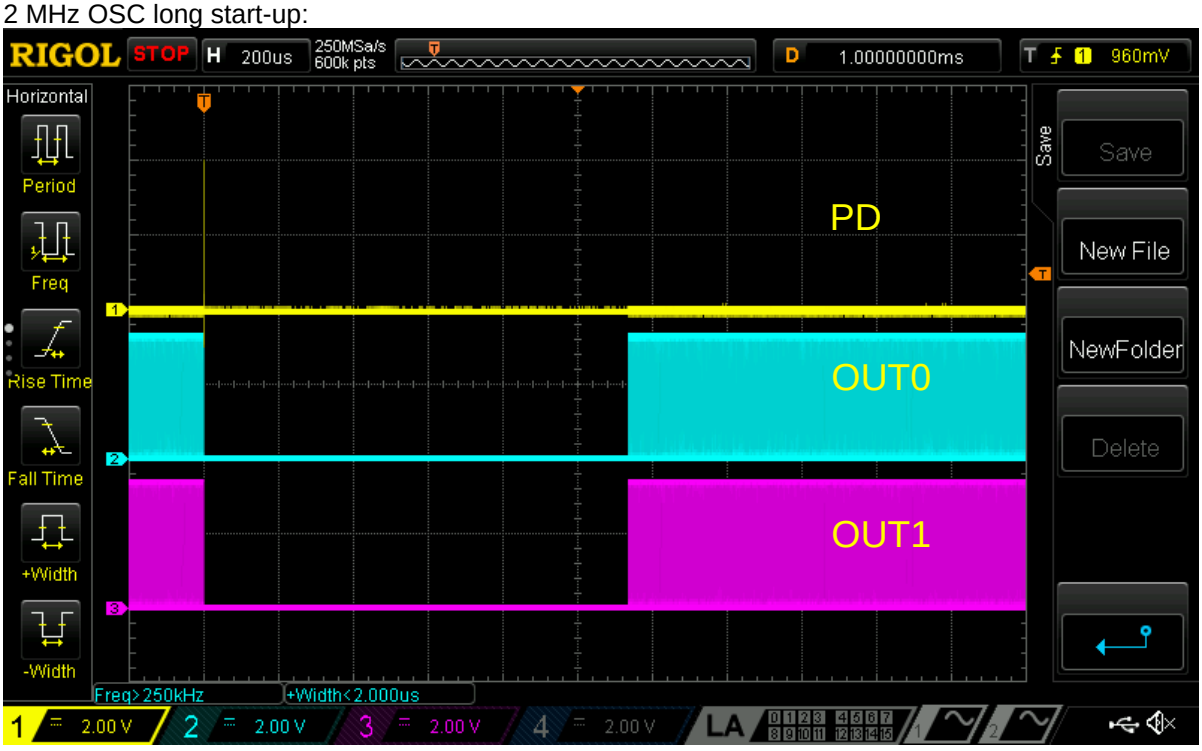
1.73 kHz OSC long start-up:



25 kHz OSC long start-up:

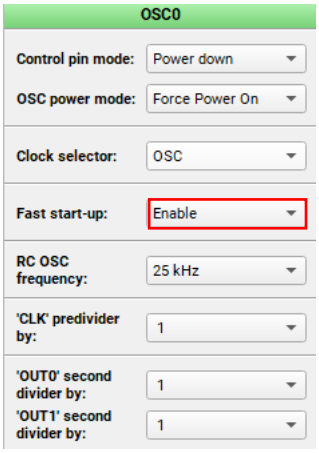


2 MHz OSC long start-up:



3.12.4 Workaround

Change Fast start-up setting to Enable or omit applying glitches at PWR DOWN input in OSC.



Document Revision History

Revision	Date	Description
0.20	6-May-2025	Updated document template
0.19	8-Apr-2025	Added issue OSC Long Start-Up Time

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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