SLG46120 Errata Note

Abstract

This document contains the known errata for the SLG46120 and the recommended workarounds.

Contents

1. Information

Package(s)	12-pin STQFN 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch 12-pin STQFN 2 mm x 2 mm x 0.55 mm, 0.5 mm pitch

2. Errata Summary

Issue #	Issue Title
1	Long RC OSC Settling Time
2	Glitches on ACMP Output
3	Delay Lock-up by a Short Pulse
4	Device Damage by High Input Voltage on External VREF Pin of ACMP
5	FILTER Cell Does Not Filter Out Glitches
6	Extra Short RC OSC Settling Time
7	OSC Long Start-Up Time
8	ACMP1 Output Is Always HIGH

3. Errata Details

3.1 Long RC OSC Settling Time

3.1.1 Effect

RC OSC, Counter, Delay

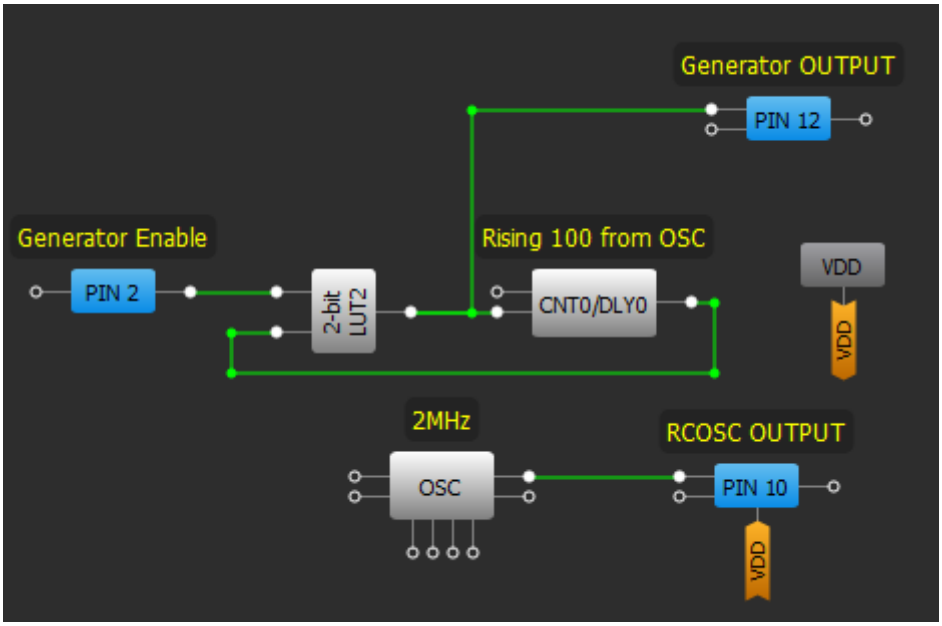
3.1.2 Conditions

RC OSC configured as 2 MHz with Auto Power-on.

3.1.3 Technical Description

Figure 1 shows blocks configuration for this issue.

The RC OSC has a longer settling time when configured as 2 MHz with Auto Power-on in designs that have very short RC OSC disable time.



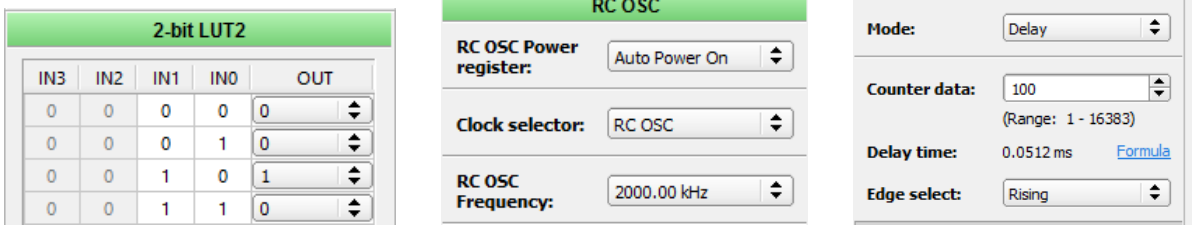


Figure 1. Design and Block Configurations That Cause the Issue

The configuration shown in Figure 1 generates a periodic signal with a frequency defined by the Delay cell and started by a HIGH signal on PIN 2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). Figure 2 shows the waveform.

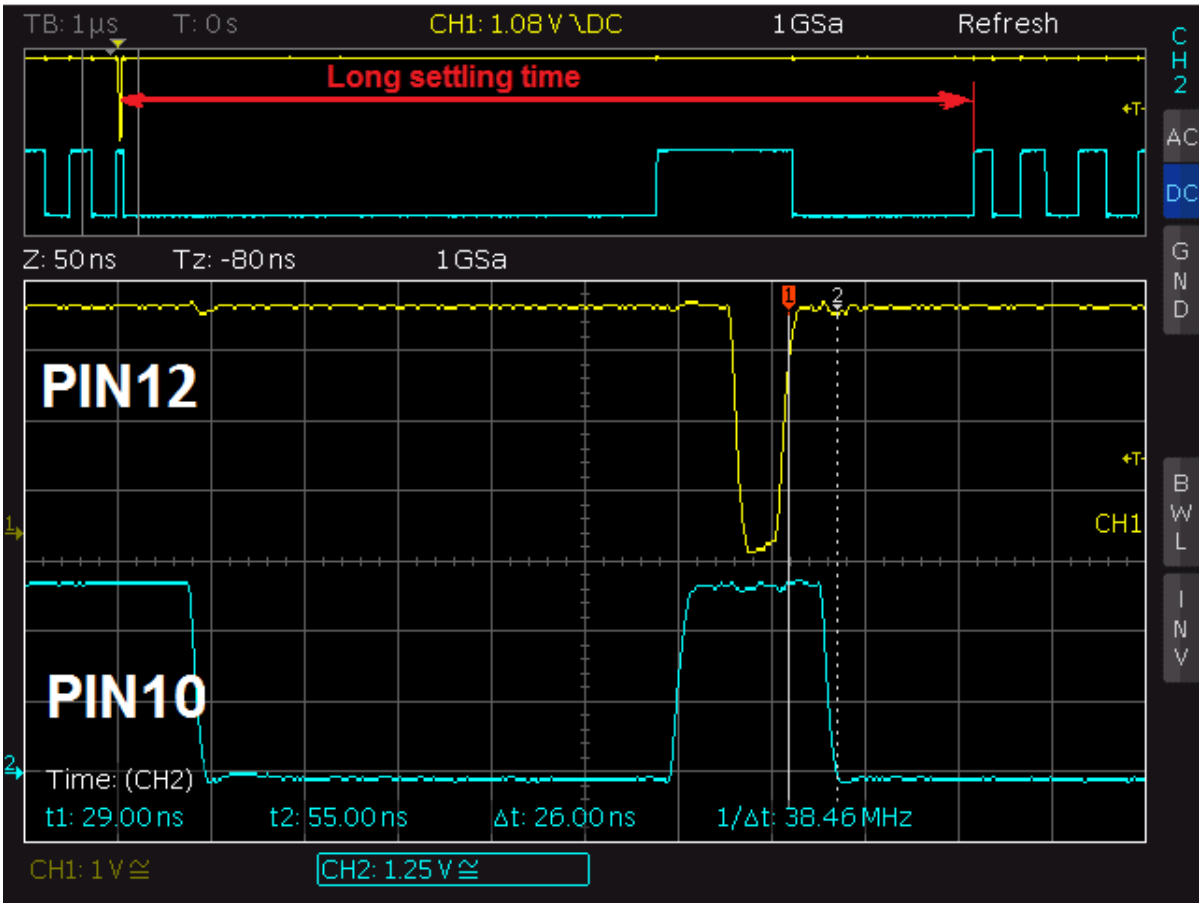


Figure 2. Waveforms: Channel 1 - 2-bit LUT0 Output; Channel 2 - RC OSC Output

Such behaviour will lead to substantial error in period calculations if the delay time is relatively small.

The same situation occurs when using two connected delays (all edge detect types except for a pair Rising edge DLY – Falling edge DLY).

Figure 3 shows an example of how Delay0 and Delay1 are configured in the same way. However, Delay1 time is 17.8 µs instead of the expected 11.3 µs (Delay0 time).

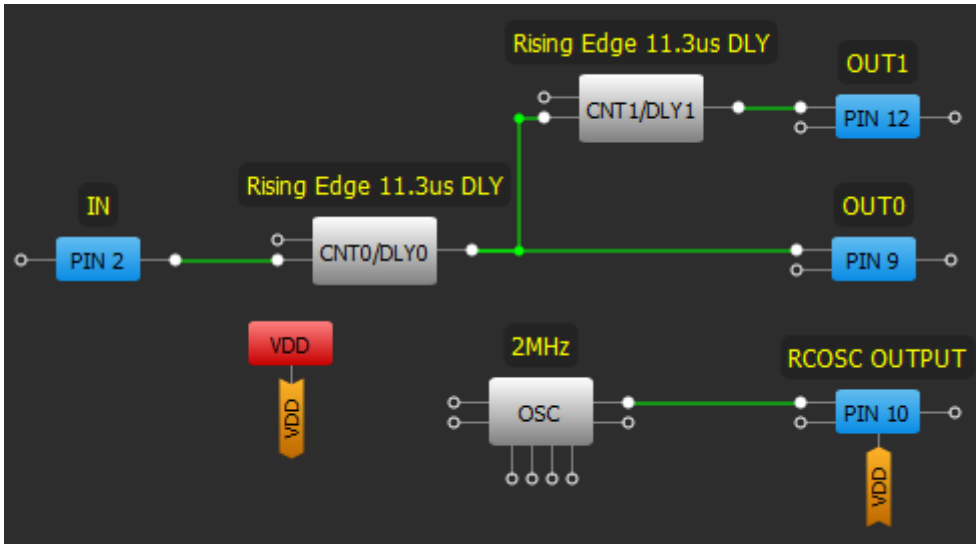


Figure 3. Delay0 and Delay1 Configuration

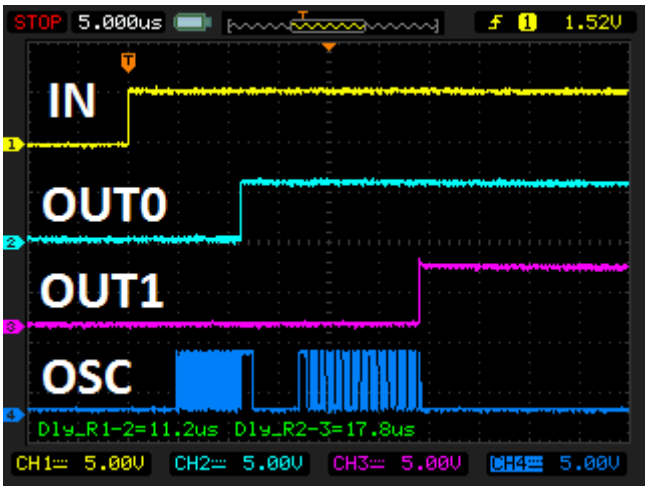


Figure 4. Delay0 and Delay1 Measured Delay Timing

If there are some inner blocks that use RC OSC at the moment or RC OSC is forced to be powered on when such an error appears, RC OSC will be operational, and the delay value will be correct.

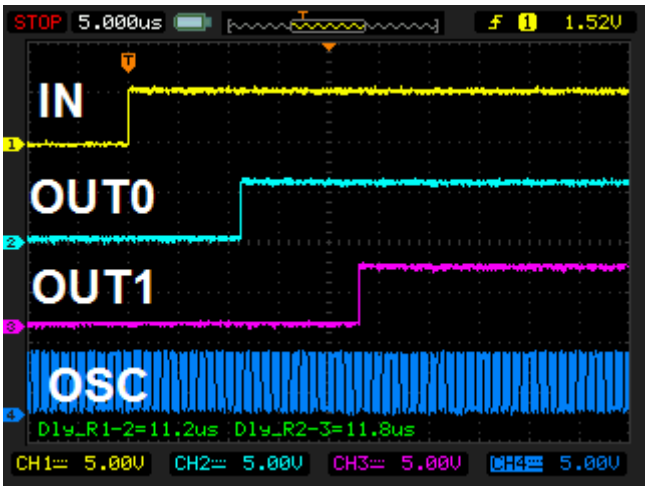
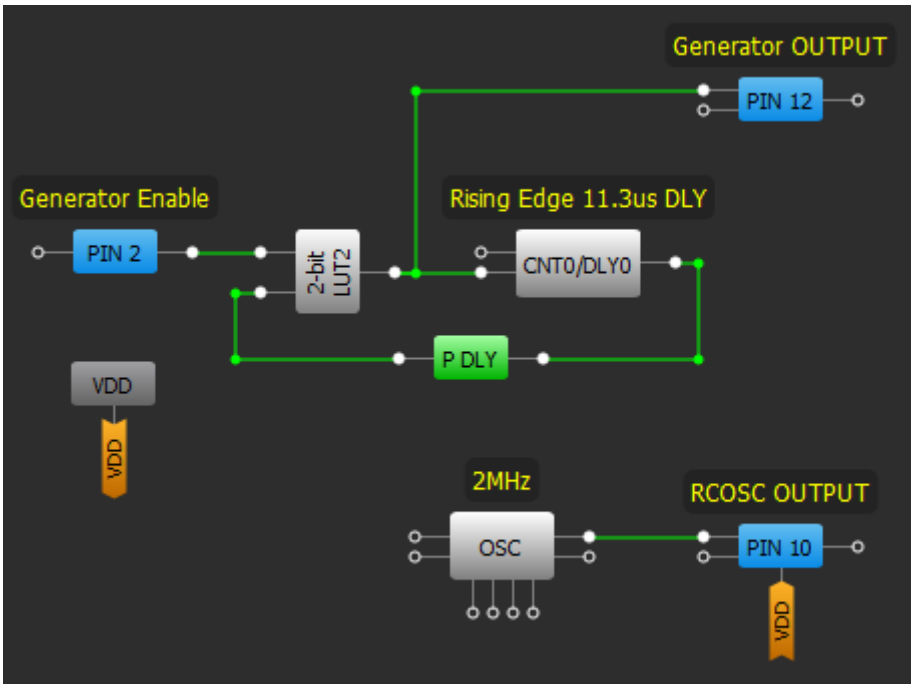


Figure 5. Delay Timing When RC OSC Is Already Operational

3.1.4 Workaround

- In the first case, use a block with a longer propagation time.



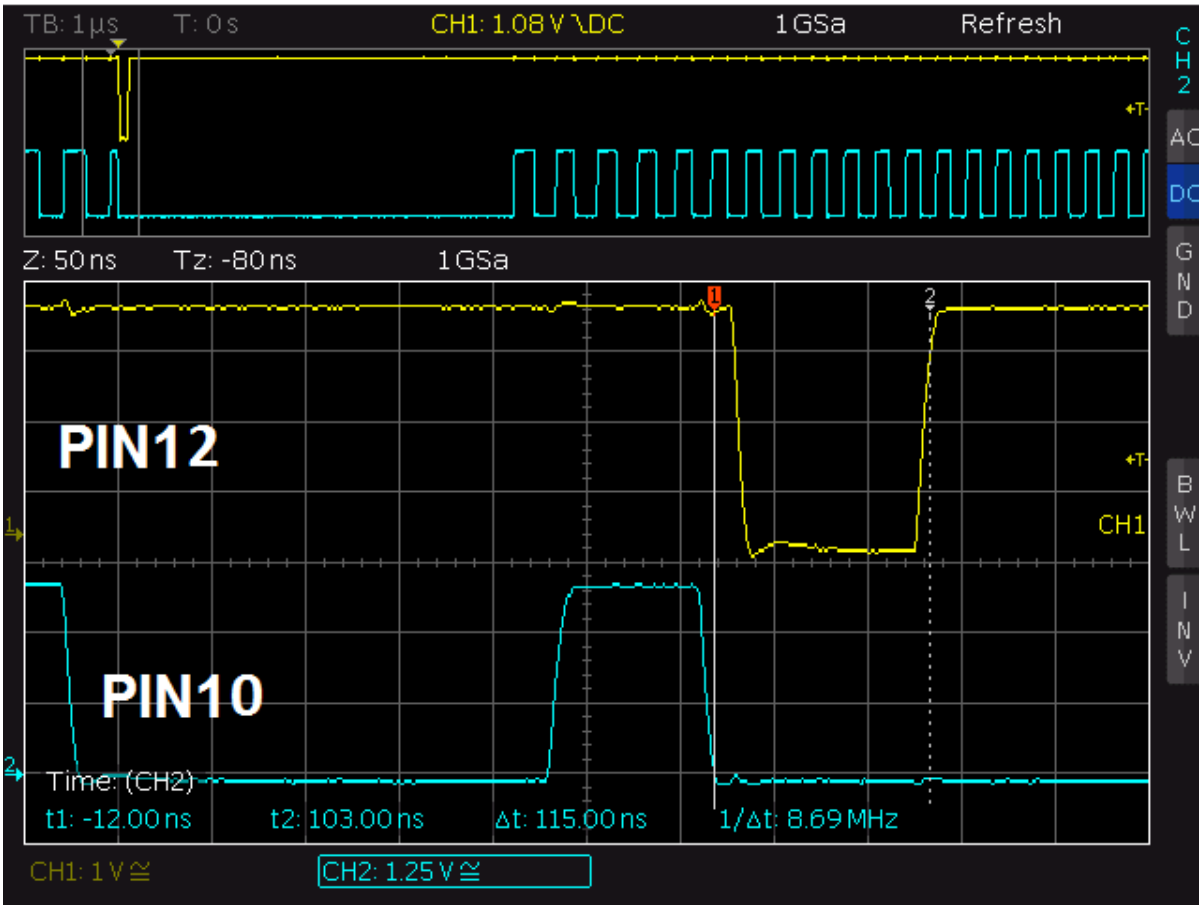


Figure 6. Workaround Using a Block with Longer Propagation Time and Resulting Waveforms

Channel 1 – 2-bit LUT0 output; Channel 2 – RC OSC output.

- Using two Delays in series (except for a pair Rising edge DLY – Falling edge DLY), use one FILTER cell or P DLY between Delay blocks. Using LUTs will not help in this case.

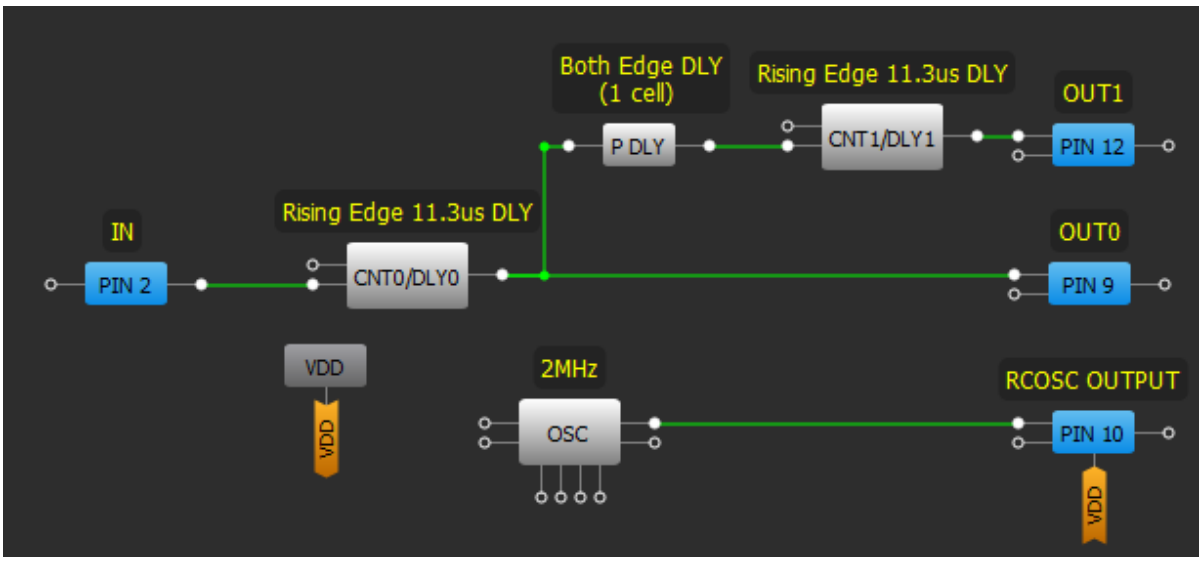


Figure 7. Workaround for Two Delay Blocks Using P DLY or FILTER Cell

- Use the Force Power-on RC OSC power control option to make the RC OSC operate continuously.

3.2 Glitches on ACMP Output

3.2.1 Effect

ACMP

3.2.2 Conditions

Conditions of glitches appearing are determined by IN- voltage, V_{DD} value, and V_{DD} Ramp (see Table 1).

Table 1. ACMP Glitch Conditions

IN- Voltage, mV	V_{DD}, V	V_{DD} Ramp Time	Glitch Presence
50	1.8	10 µs	+
50	1.8	1 s	-
50	3.3	10 µs	+
50	3.3	1 s	+
50	5.5	10 µs	+
50	5.5	1 s	+
600	1.8	10 µs	-
600	1.8	1 s	-
600	3.3	10 µs	+
600	3.3	1 s	-
600	5.5	10 µs	+
600	5.5	1 s	-
1200	1.8	10 µs	-
1200	1.8	1 s	-
1200	3.3	10 µs	-

IN- Voltage, mV	V_{DD}, V	V_{DD} Ramp Time	Glitch Presence
1200	3.3	1 s	-
1200	5.5	10 µs	+
1200	5.5	1 s	-

3.2.3 Technical Description

In some cases, ACMP may have short high-level glitches on its output (even if IN+ voltage is less than IN- voltage) after the GreenPAK chip is powered up. Such cases may appear when using ACMP with Low Bandwidth mode enabled and when Power-Up is connected directly to the V_{DD}.

To detect such glitches, a circuit with an additional LUT was used. This LUT detects a high level on the ACMP output and stays HIGH until the device is powered down.

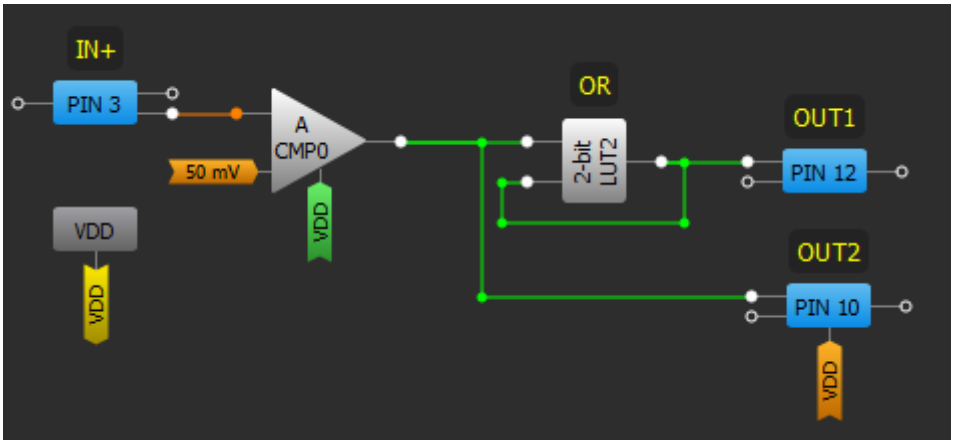


Figure 8. Circuit Used to Detect Glitches on the ACMP Output

ACMP IN+ is connected to the ground.

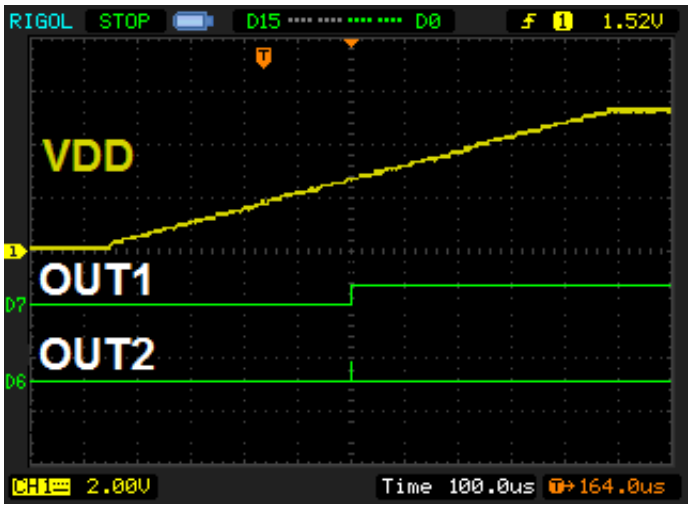


Figure 9. V_{DD} Ramp and ACMP Output Glitch Waveforms

3.2.4 Workaround

Use a POR block connected to the ACMP's Power-Up pin. However, in this case, ACMP will start working with low-level output and will be able to go HIGH only after POR goes HIGH and ACMP power-on time passes.

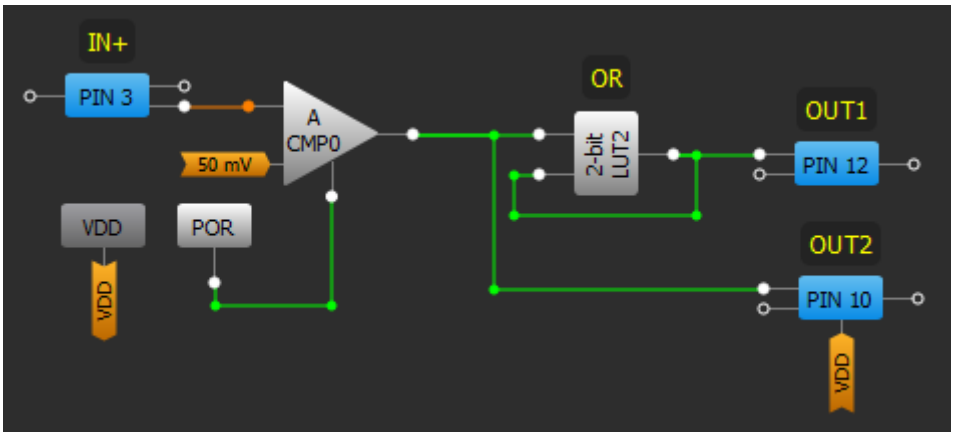


Figure 10. POR-based Workaround for ACMP Output Glitches

3.3 Delay Lock-up by a Short Pulse

3.3.1 Effect

Delay

3.3.2 Conditions

When a short pulse appears on Delay input.

3.3.3 Technical Description

The Delay output could be latched despite the input change when a short pulse is an input. For example, if the Delay cell is configured as a falling edge delay, the short pulse (see Note) will appear on its input and the Delay cell output will switch from LOW to HIGH but may not switch from HIGH to LOW even after the delay time has passed.

Note: The pulse width varies between devices and with different V_{DD} voltages. It is in the range of 5 ns to 15 ns and in the window of ±0.2 ns, so it should be very precise for the issue to happen.

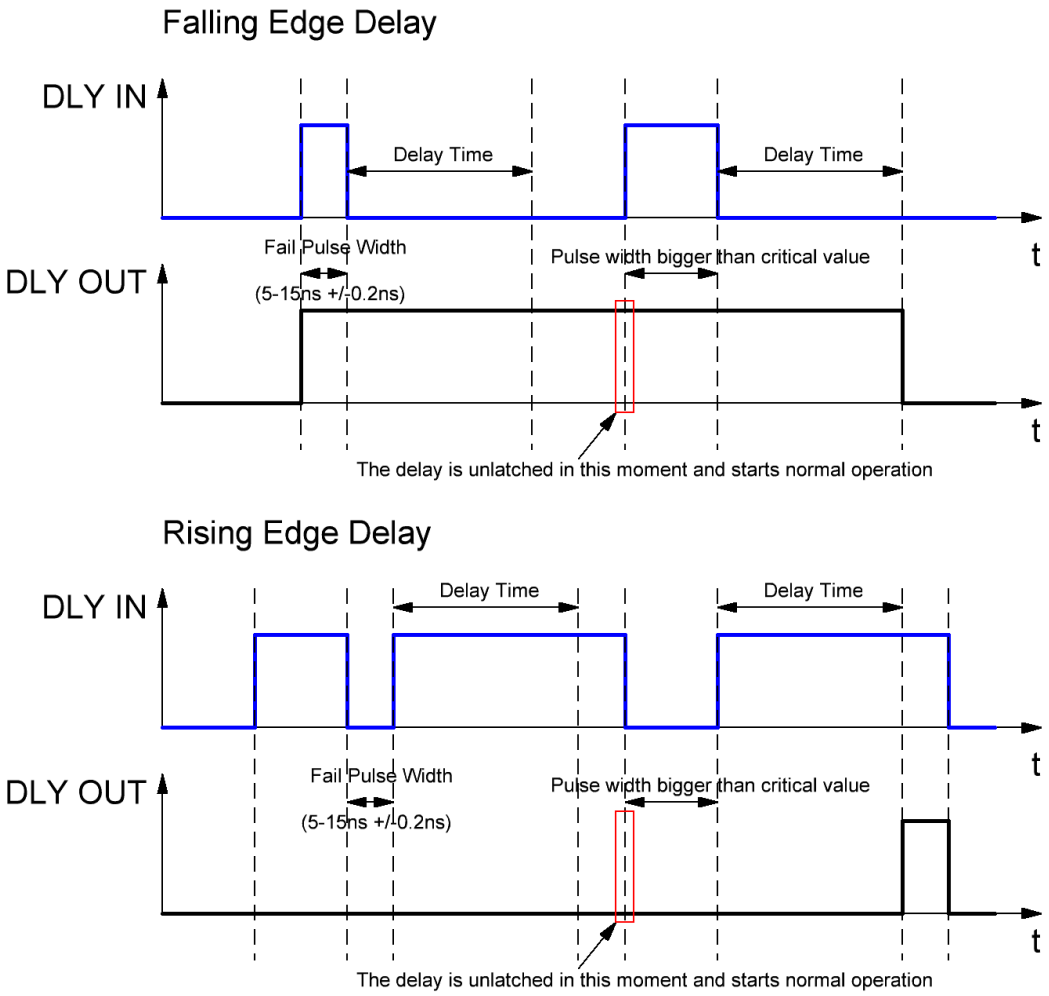


Figure 11. Delay Lock-Up and Recovery Timing for Short Input Pulses

Also, note that both edge delays do not have such an issue.

3.3.4 Workaround

Use P DLY or FILTER block configured as both edge delay or FILTER.

3.4 Device Damage by High Input Voltage on External V_{REF} Pin of ACMP

3.4.1 Effect

ACMPs

3.4.2 Conditions

Voltage higher than 2 V applied to IN- of ACMP as an external reference voltage.

3.4.3 Technical Description

The device may be damaged by a voltage higher than 2 V applied to IN- of ACMP as an external reference voltage.

3.4.4 Workaround

There is no workaround for this issue. Avoid applying more than 2 V on IN- of ACMP used as an external voltage reference.

3.5 FILTER Cell Does Not Filter Out Glitches

3.5.1 Effect

FILTER Cell

3.5.2 Conditions

If a high-frequency clock input comes in.

3.5.3 Technical Description

If a high-frequency clock input comes in, the FILTER cell may not filter it out. There are several factors such as input frequency, duty cycle, and short duration in such a signal that may lead to its passing through the FILTER block.

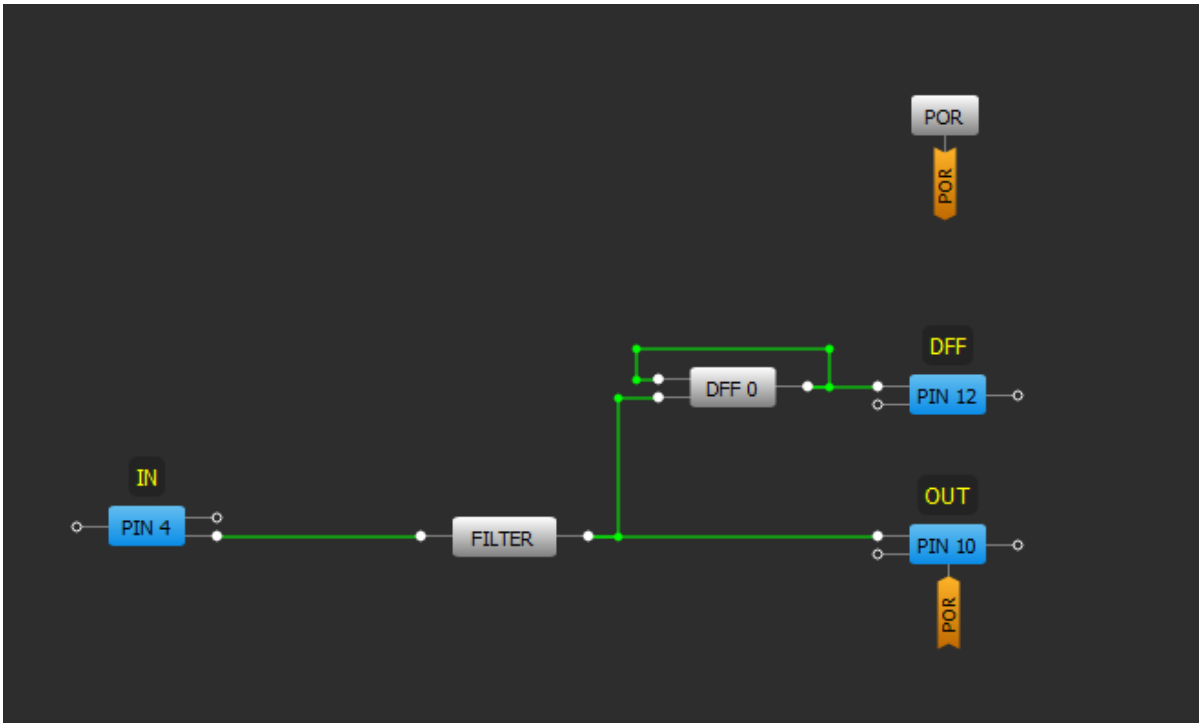


Figure 12. FILTER Cell Test Configuration

Channel 1 (yellow/top line) – PIN 4 (IN).
Channel 2 (light blue/2nd line) – PIN 10 (OUT).
Channel 3 (magenta /3rd line) – PIN 12 (DFF).

Figure 13. Waveforms at 60 ns Period and 10 ns Pulse Width (Correct Functionality)

Figure 14. Waveforms at 60 ns Period and 20 ns Pulse Width (Incorrect Functionality)

Figure 15. Waveforms at 60 ns Period and 30 ns Pulse Width (Incorrect Functionality)

Figure 16. Waveforms at 60 ns Period and 40 ns Pulse Width (Correct Functionality)

3.5.4 Workaround

Currently, there is no workaround for this issue. The filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the Delay cell to avoid its latching (see issue #5).

3.6 Extra Short RC OSC Settling Time

3.6.1 Effect

RC OSC, Counter, Delay

3.6.2 Conditions

OSC configured as 25 kHz with Auto Power-on.

3.6.3 Technical Description

The first period of the RC OSC can be very short when the OSC is configured as 25 kHz with Auto Power-on in the designs. This can occur when V_{DD} is above 4.0 V. Critical for CNT/DLY with a low counter data (less than 10) or if it is necessary to use the frequency of the OSC to clock external elements.

Figure 17 shows an example configuration of such an issue.

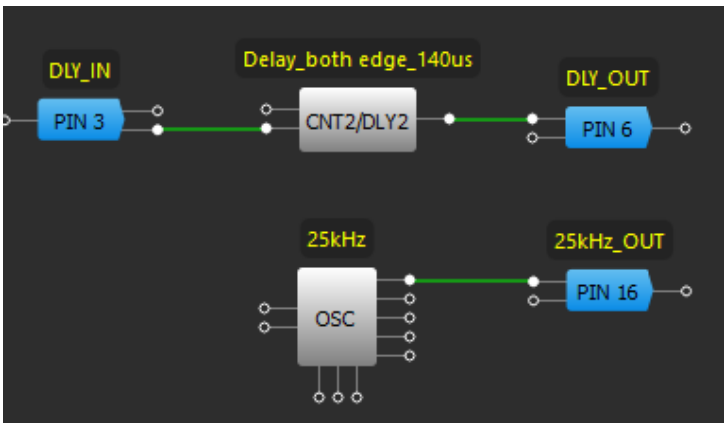


Figure 17. Design and Block Configuration That Causes the Issue

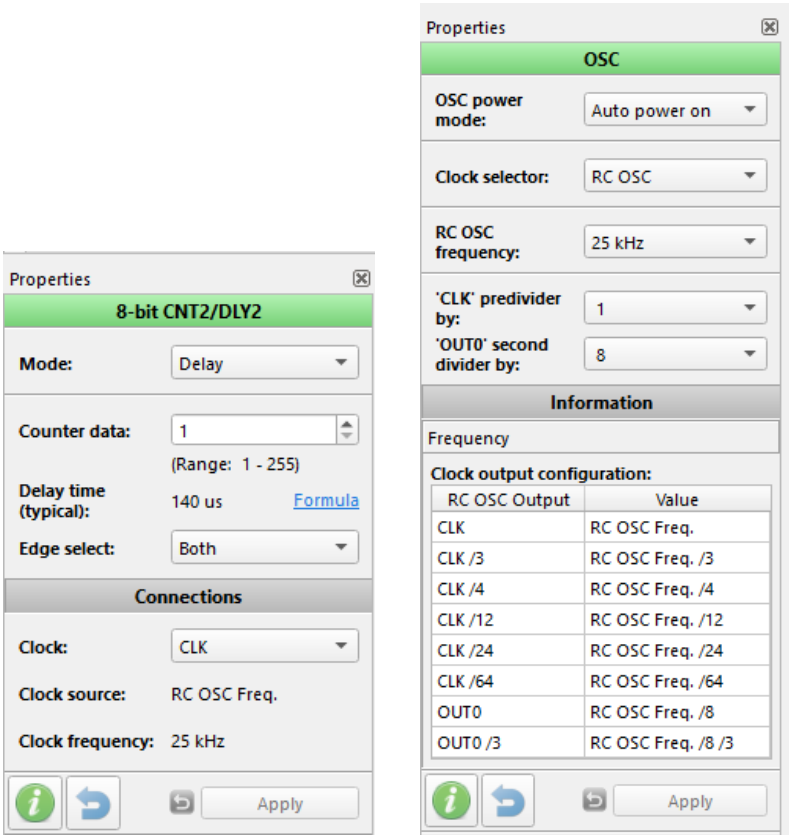


Figure 18. 25 kHz RC OSC and Delay Test Configuration

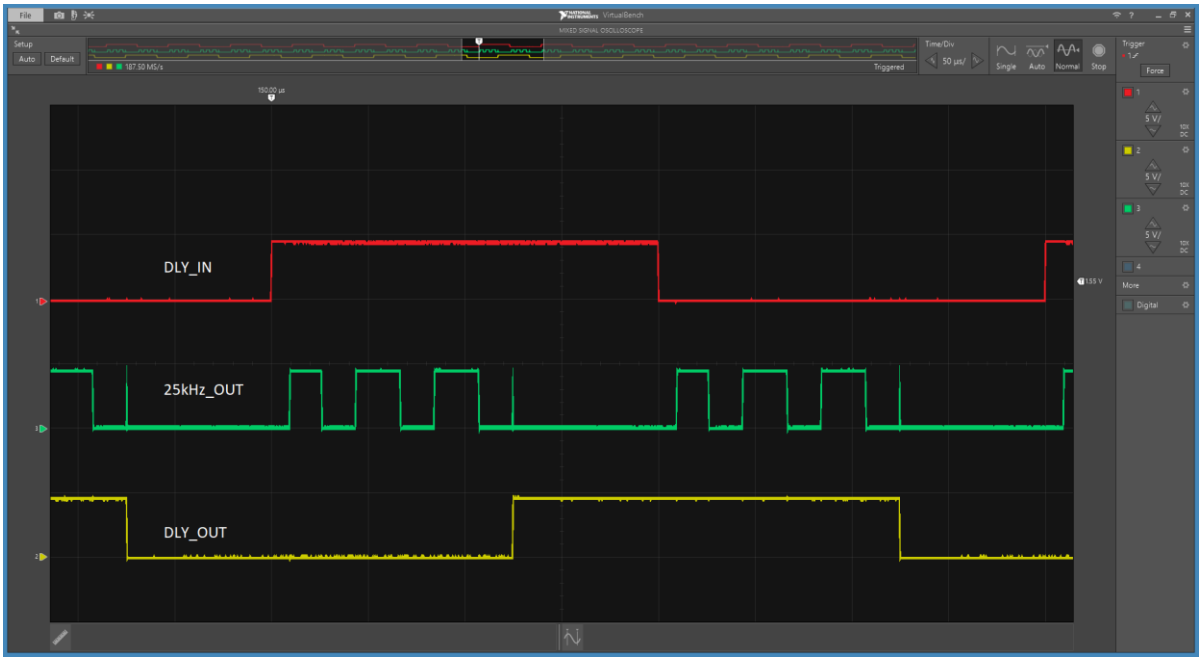


Figure 19. Normal 25 kHz RC OSC Behavior

Figure 20. Abnormal 25 kHz RC OSC Behavior

3.6.4 Workaround

- Avoid V_{DD} higher than 4 V
- Force on OSC

3.7 OSC Long Start-Up Time

3.7.1 Effect

When a short pulse is applied to the PWR DOWN input, the oscillator exhibits a long start-up time.

3.7.2 Conditions

When a pulse shorter than approximately 40 ns is applied to the PWR DOWN input.

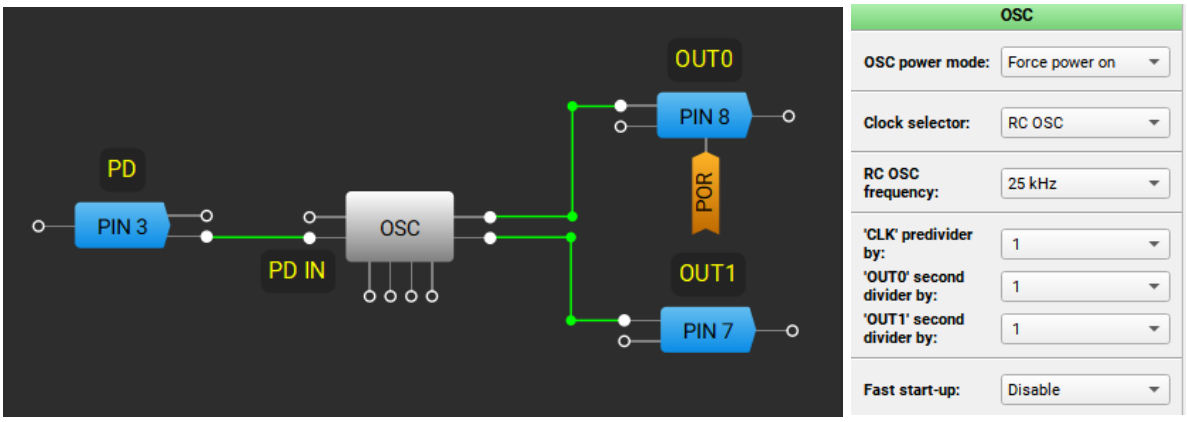


Figure 21. Oscillator Configuration and Properties

3.7.3 Technical Description

If a pulse shorter than approximately 40 ns is applied to the oscillator's PWR DOWN input, the oscillator outputs remain stuck for several milliseconds, as shown in Figure 22 and Figure 23. This issue occurs with both the 25 kHz and 2 MHz oscillators.

Figure 22. 25 kHz OSC Long Start-Up Timing Diagram

Figure 23. 2 MHz OSC Long Start-Up Timing Diagram

3.7.4 Workaround

Avoid applying glitches to the oscillator's PWR DOWN input.

3.8 ACMP1 Output Is Always HIGH

3.8.1 Effect

ACMP1

3.8.2 Conditions

When the gain is not equal to 1, and the 100 µA pull-ups on the input is enabled.

3.8.3 Technical Description

If the IN+ gain setting is not disabled (that is, any of the x0.25, x0.33, or x0.5 settings is selected) and the 100 µA pull-up on input setting is enabled, the ACMP1 output goes HIGH immediately upon power-up. The output remains in this HIGH state regardless of the voltage levels applied to the ACMP1 IN+ pin.

3.8.4 Workaround

Currently, there is no workaround for this issue.

4. Revision History

Revision	Date	Description
1.32	Sep 11, 2026	Re-added the issue OSC Long Start-Up Time Corrected revision history descriptions
1.31	Sep 4, 2026	Converted to the new template Removed the issue OSC Long Start-Up Time
1.3	Feb 2, 2026	Added issue ACMP1 Output Is Always HIGH
1.2	Dec 19, 2024	Added issue OSC Long Start-Up Time
1.1	Mar 8, 2022	Fixed typos Renesas rebranding
1.0	Dec 30, 2021	Added issue Extra Short RC OSC Settling Time Updated according to Dialog's format