Brief Description

The ZSPM4013B is a DC/DC synchronous switching regulator with fully integrated power switches, internal compensation, and full fault protection. The 1MHz switching frequency enables using small filter components, resulting in reduced board space and reduced bill-of-materials costs.

The ZSPM4013B utilizes current mode feedback in normal regulation pulse-width modulation (PWM) mode. When the regulator is disabled (EN pin is low), the ZSPM4013B draws less than 10µA quiescent current.

The ZSPM4013B integrates a wide range of protection circuitry, including input supply under-voltage lockout, output voltage soft start, current limit, V_{OUT} over-voltage, and thermal shutdown. The ZSPM4013B includes supervisory reporting through the PG (Power Good) open-drain output to interface other components in the system.

Features

- Output voltage options (depends on order code):
  - Fixed output voltages: 1.5V, 1.8V, 2.5V, 3.3V, or 5V with +/- 2% output tolerance
  - Adjustable output voltage range: 0.9V to 5.5V with +/- 1.5% reference
- Wide input voltage range: 4.5V to 18V
- 1MHz +/- 10% fixed switching frequency
- 3A continuous output current
- High efficiency – up to 95%
- Current mode PWM control with pulse-frequency modulation (PFM) mode for improved light load efficiency
- Voltage supervisor for V_{OUT} reported at the PG pin
- Input supply under-voltage lockout
- Soft start for controlled startup with no overshoot
- Full protection for over-current, over-temperature, and V_{OUT} over-voltage
- Less than 10µA in Disabled Mode
- Low external component count

Benefits

- Increased battery life
- Minimal external component count (3 capacitors, 1 inductor)
- Inherent fault protection and reporting

Available Support

- Evaluation Kit
- Documentation

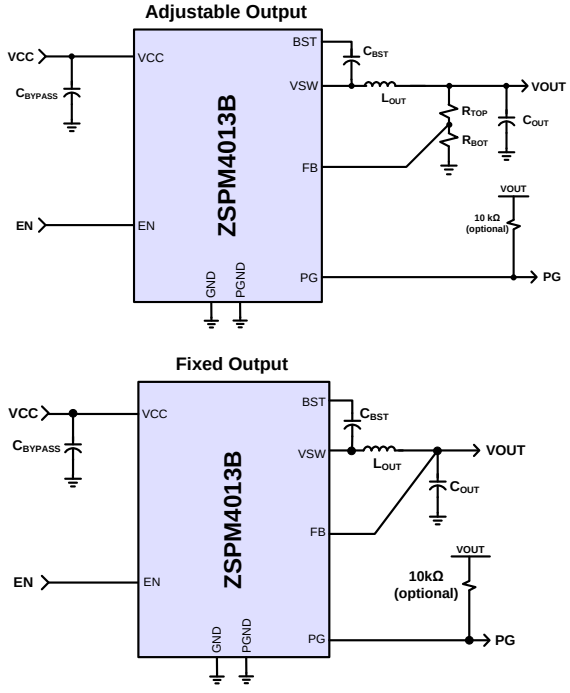
Physical Characteristics

- Junction operating temperature: -40°C to 125°C
- Packaged in a 16-pin QFN (3x3mm)

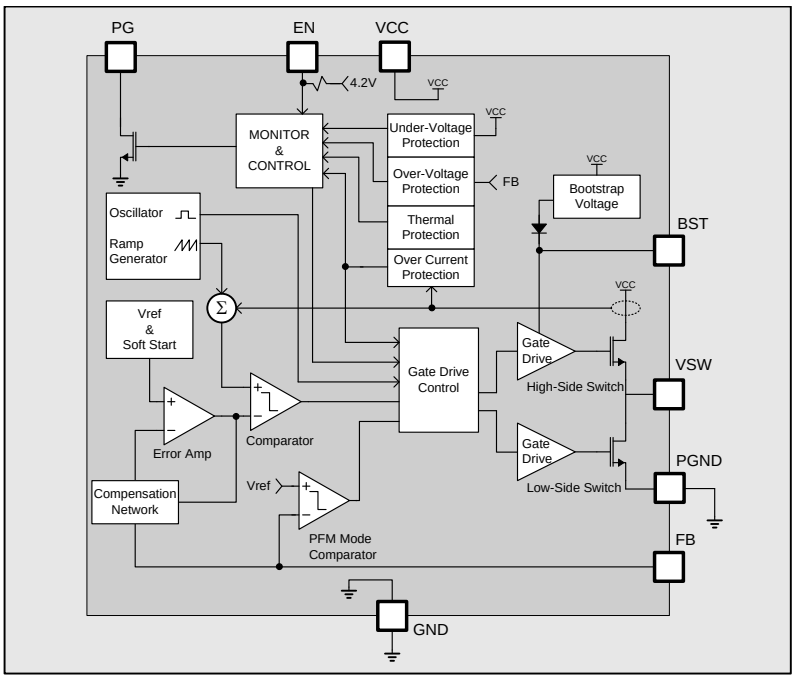
Related IDT Products

- ZSPM4011B/ZSPM4012B: 1A/2A synchronous buck converters, available with adjustable output from 0.9 to 5.5V or fixed output voltages at 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (16-lead 3x3mm QFN)
- ZSPM1000: >5A single-phase, single-rail, true digital PWM controller (24-lead 4x4mm QFN)

ZSPM4013B Application Circuits



ZSPM4013B Block Diagram



Typical Applications

- Wireless access points, cable modems
- Set-top boxes
- DVD, LCD, LED supplies
- Portable products, including GPS, smart phones, tablet PCs
- Printers

Ordering Information

Ordering Code	Description	Package
ZSPM4013BA1W00	3A Synchronous Buck Converter: adjustable output, 0.9V to 5.5V, 16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W15	3A Synchronous Buck Converter: fixed output, 1.5V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W18	3A Synchronous Buck Converter: fixed output, 1.8V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W25	3A Synchronous Buck Converter: fixed output, 2.5V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W33	3A Synchronous Buck Converter: fixed output, 3.3V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W50	3A Synchronous Buck Converter: fixed output, 5.0V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BKIT	ZSPM4013BKIT, Evaluation Kit for 3A Synchronous Buck Converter	Kit

Contents

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List of Tables

1 ZSPM4013B Characteristics

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” (section 1.3) is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

1.1. Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted.

Table 1.1 Absolute Maximum Ratings

Parameter	Value[1)]	UNIT
Voltage on VCC pin	-0.3 to 20	V
Voltage on BST pin	-0.3 to (VCC+6)	V
Voltage on VSW pin	-1 to 20	V
Voltage on EN, PG, FB pins	-0.3 to 6	V
Electrostatic Discharge – Human Body Model [2)]	+/-2k	V
Electrostatic Discharge – Charge Device Model [2)]	+/-500	V
Lead Temperature (soldering, 10 seconds)	260	°C

1) All voltage values are with respect to network ground terminal.
2) ESD testing is performed according to the respective JESD22 JEDEC standard.

1.2. Thermal Characteristics

Table 1.2 Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance Junction to Air [1)]	θ_{JA}	34.5	°C/W
Thermal Resistance Junction to Case [1)]	θ_{Jc}	2.5	°C/W
Storage Temperature Range	T_{STG}	-65 to 150	°C
Maximum Junction Temperature	$T_{J\ MAX}$	150	°C
Operating Junction Temperature Range	T_J	-40 to 125	°C

1) Assumes 1 in^2 area of 2 oz. copper and 25°C ambient temperature.

1.3. Recommended Operating Conditions

Table 1.3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Operating Voltage	VCC	4.5	12	18	V
Bootstrap Capacitor	C_{BST}	17.6	22	26.4	nF
Output Filter Inductor Typical Value [1)]	L_{OUT}	3.76	4.7	5.64	µH
Output Filter Capacitor Typical Value [2)]	C_{OUT}	33	44 (2 x 22)		µF
Output Filter Capacitor ESR	$C_{OUT-ESR}$	2	35	100	mΩ
Input Supply Bypass Capacitor Typical Value [3)]	C_{BYPASS}	8	10		µF

1) For best performance, use an inductor with a saturation current rating higher than the maximum V_{OUT} load requirement plus the inductor current ripple.

2) For best performance, a low ESR ceramic capacitor should be used.

3) For best performance, a low ESR ceramic capacitor should be used. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1µF ceramic capacitor should be added in parallel to C_{BYPASS}.

1.4. Electrical Characteristics

Electrical Characteristics, T_J = -40°C to 125°C, VCC = 12V (unless otherwise noted)

Table 1.4 Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VCC Supply Voltage						
Input Supply Voltage	VCC		4.5		18	V
Quiescent Current: Normal Mode	$I_{CC-NORM}$	VCC = 12V, I_{LOAD} = 0A, EN ≥ 2.2V		5.2		mA
Quiescent Current: Normal Mode, Non-switching	$I_{CC-NOSWITCH}$	VCC=12V, I_{LOAD}=0A, EN ≥ 2.2V Non-switching		2.3		mA
Quiescent Current: Disabled Mode	$I_{CC-DISABLE}$	VCC = 12V, EN = 0V		5	10	µA
VCC Under-Voltage Lockout						
Input Supply Under-Voltage Threshold	VCC_{-UV}	VCC Increasing	4.1	4.3	4.5	V
Input Supply Under-Voltage Threshold Hysteresis	VCC_{-UV_HYST}		300	325	350	mV
Oscillator						
Oscillator Frequency	f_{OSC}		0.9	1	1.1	MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
PG Open-Drain Output						
PG Release Timer	t_{PG}			10		ms
High-Level Output Leakage	I_{OH-PG}	V_{PG} = 5V		0.5		µA
Low-Level Output Voltage	V_{OL-PG}	I_{PG} = -0.3mA			0.01	V
EN Input Voltage Thresholds						
High Level Input Voltage	V_{IH-EN}		2.2			V
Low Level Input Voltage	V_{IL-EN}				0.8	V
Input Hysteresis	$V_{HYST-EN}$			480		mV
Input Leakage	I_{IN-EN}	V_{EN}=5V		3.5		µA
		V_{EN}=0V		-1.5		µA
Thermal Shutdown						
Thermal Shutdown Junction Temperature	TSD	Note: Guaranteed by design	150	170		°C
TSD Hysteresis	TSD_{HYST}			10		°C

1.5. Regulator Characteristics

Electrical Characteristics, T_J = -40°C to 125°C, VCC = 12V (unless otherwise noted).

Table 1.5 Regulator Characteristics

See important table notes at the end of the table.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Switch Mode Regulator: L_{OUT}=4.7µH and C_{OUT}=2 x 22µF						
Output Voltage Tolerance in Pulse-Width Modulation (PWM) Mode	$V_{OUT-PWM}$	I_{LOAD} =1A	V_{OUT} – 2%	V_{OUT}	V_{OUT} + 2%	V
Output Voltage Tolerance in Pulse-Frequency Modulation (PFM) Mode	$V_{OUT-PFM}$	I_{LOAD} = 0A	V_{OUT} – 1%	V_{OUT} + 1%	V_{OUT} + 3.5%	V
Differential Voltage Between V_{OUT} and V_{CC}	V_{IN-OUT}	Steady State. (Example, VOUT maximum is 3.3V with VCC min of 4.5V)	1.2			V
High-Side (HS) Switch On Resistance [1)]	R_{DSON}	I_{VSW} = -1A		180		mΩ
Low-Side (LS) Switch On Resistance [1)]		I_{VSW} = 1A		120		mΩ
Output Current	I_{OUT}				3	A
Over-Current Detection	I_{OCD}	HS switch current	3.4	3.8	4.4	A

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Feedback Reference (Adjustable Mode)	FB_{TH}		0.886	0.9	0.914	V
Soft Start Ramp Time	t_{SS}			4		ms
PFM Mode FB Comparator Tolerance	FB_{TH-TOL}	For the adjustable version, the ratio of VCC/V_{OUT} cannot exceed 16.	-1.5		1.5	%
PFM Mode FB Comparator Threshold	FB_{TH-PFM}			V_{OUT} +1%		V
V_{OUT} Under-Voltage Threshold	V_{OUT-UV}		88% V_{OUT}	90% V_{OUT}	92% V_{OUT}	
V_{OUT} Under-Voltage Hysteresis	V_{OUT-UV_HYST}			1.5% V_{OUT}		
V_{OUT} Over-Voltage Threshold	V_{OUT-OV}			103% V_{OUT}		
V_{OUT} Over-Voltage Hysteresis	V_{OUT-OV_HYST}			1% V_{OUT}		
Max Duty Cycle [2]	$DUTY_{MAX}$		95%	97%	99%	

1) R_{DSON} is characterized at 1A and tested at lower current in production.
2) Regulator VSW pin is forced off for 240ns every 8 cycles to ensure the BST cap is replenished.

2 Typical Performance Characteristics

Figure 2.1 Startup Response

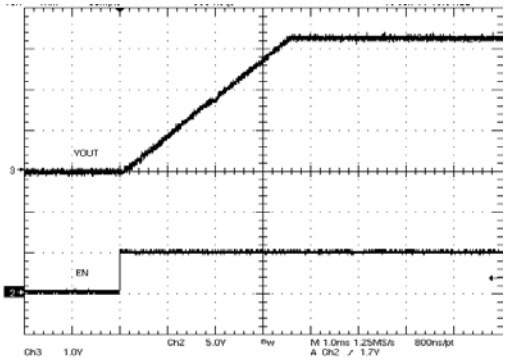


Figure 2.2 100mA to 1A Load Step (VCC= 12V, VOUT=1.8V)

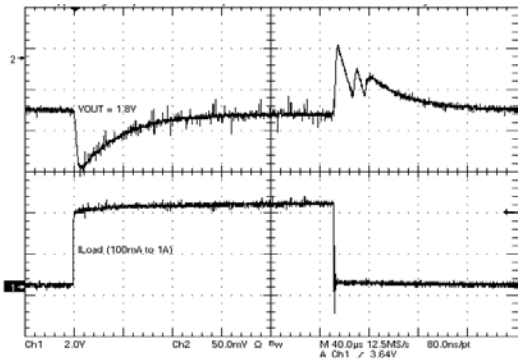


Figure 2.3 100mA to 2A Load (VCC=12V, VOUT = 1.8V)

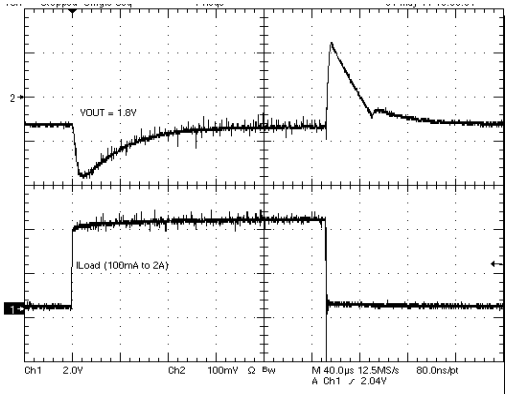


Figure 2.4 100mA to 1A Load Step (VCC=12V, VOUT= 3.3V)

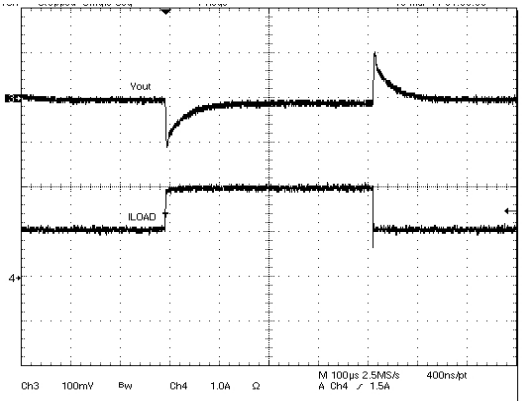


Figure 2.5 100mA to 2A Load Step (VCC=12V, VOUT= 3.3V)

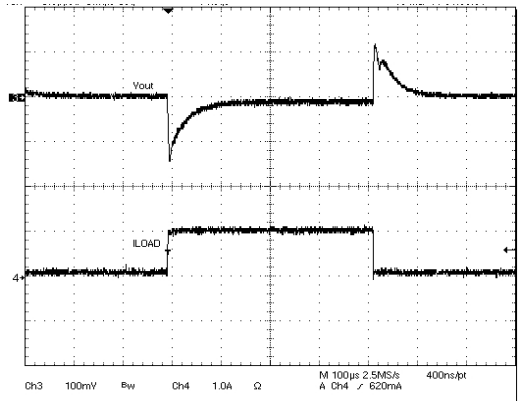


Figure 2.6 Line Transient Response (VCC=12V, VOUT = 3.3V)

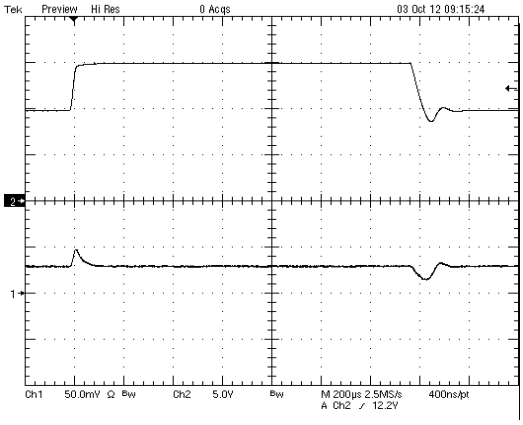


Figure 2.7 Load Regulation

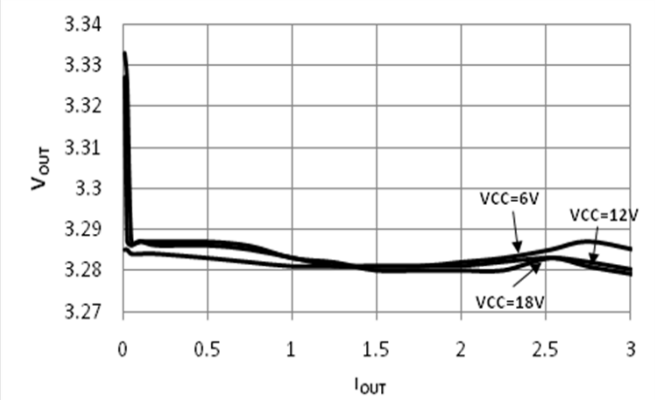


Figure 2.8 Line Regulation (I_{OUT}=1A)

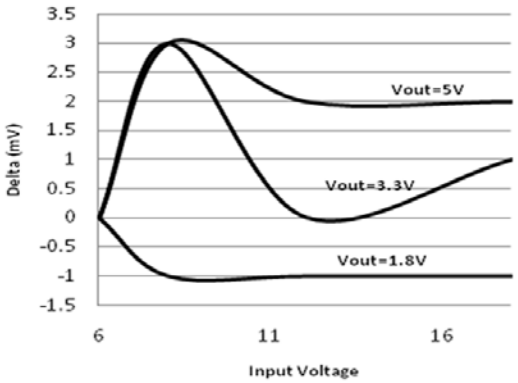


***Figure 2.9 Efficiency* vs. Output Current (V*OUT* = 1.8V)**

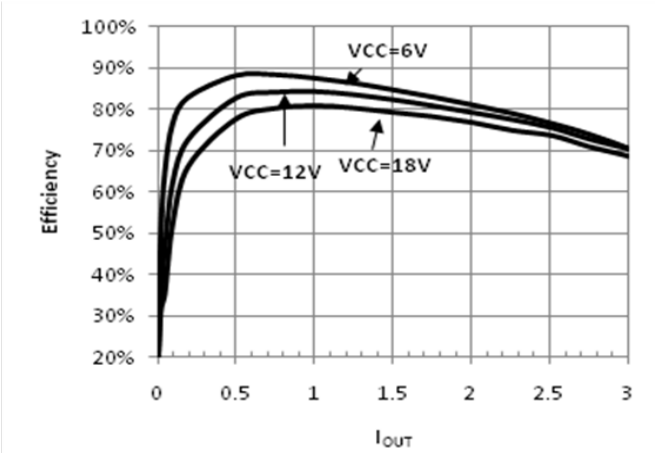


***Figure 2.10 Efficiency* vs. Output Current (V*OUT* = 3.3V)**

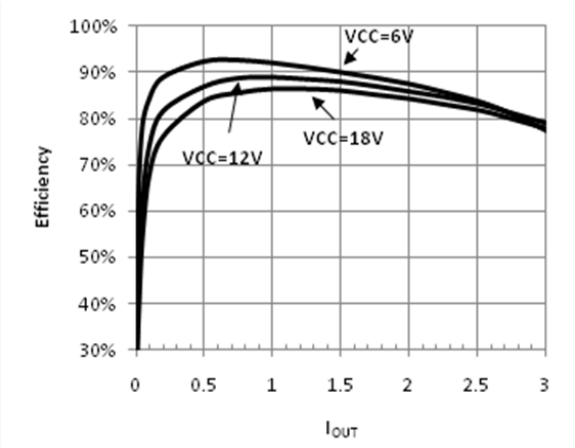


***Figure 2.11 Efficiency* vs. Output Current (V*OUT* = 5V)**

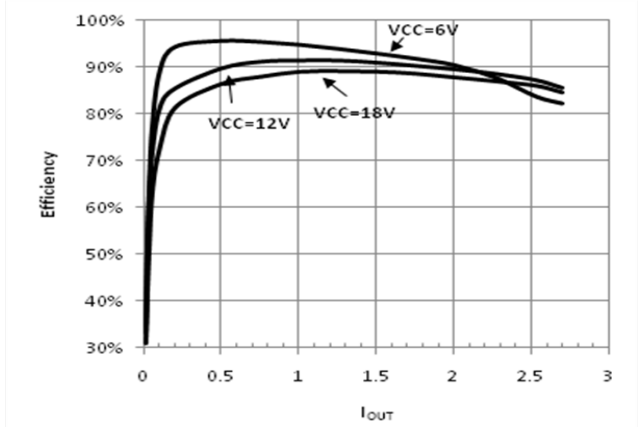


***Figure 2.12 Efficiency* vs. Input Voltage (V*OUT* = 3.3V)**

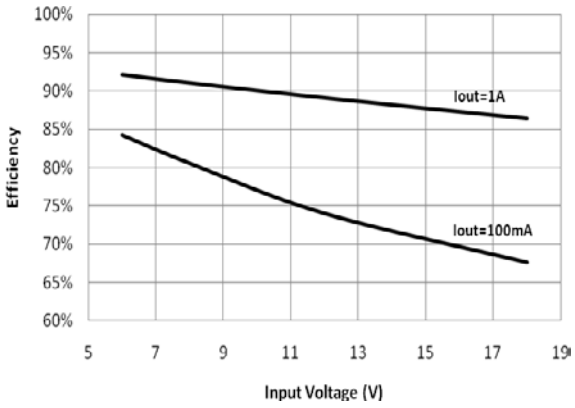


Figure 2.13 **Standby Current vs. Input Voltage**

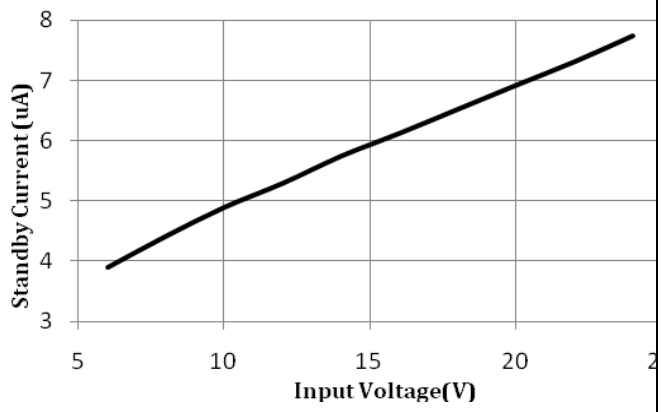


Figure 2.14 **Standby Current vs. Temperature**

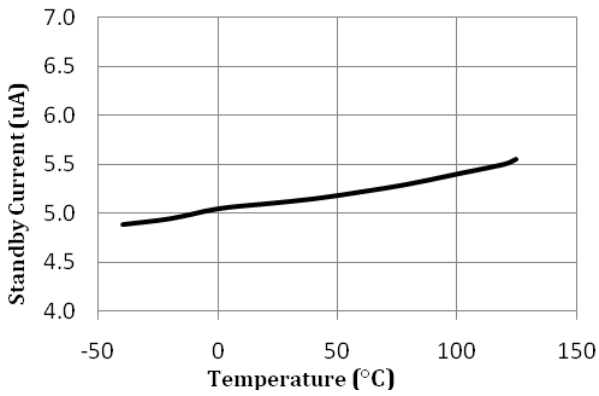


Figure 2.15 **Output Voltage vs. Temperature**

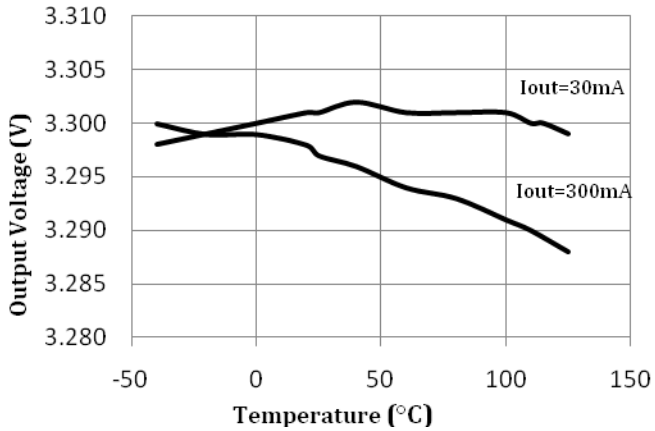


Figure 2.16 **Oscillator Frequency vs. Temperature (Iout=300mA)**

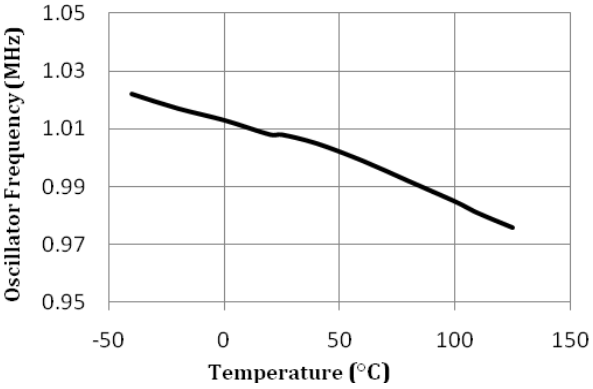


Figure 2.17 **Quiescent Current vs. Temperature (No load)**

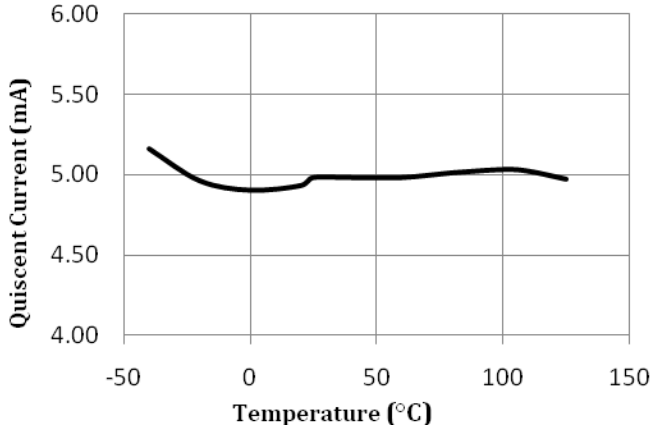
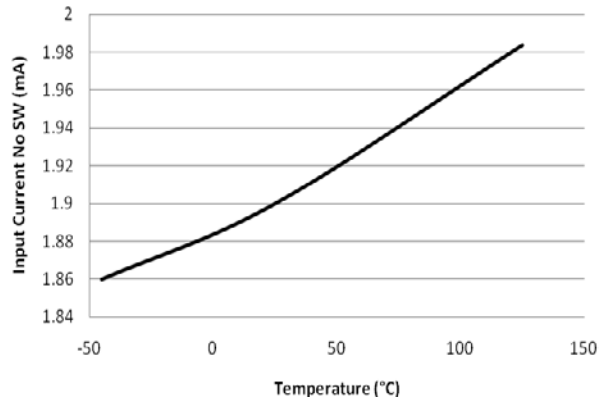


Figure 2.18 **Input Current vs. Temperature (No load, No switching)**



3 Description of Circuit

The ZSPM4013B current-mode synchronous step-down power supply IC can be used in the commercial, industrial, and automotive market segments. It includes flexibility for a wide range of output voltages and is optimized for high-efficiency power conversion with low R_{DSON} integrated synchronous switches. A 1MHz internal switching frequency facilitates low-cost LC filter combinations. The fixed-output versions also enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The regulator automatically transitions between pulse frequency modulation (PFM) and pulse width modulation (PWM) mode to maximize efficiency for the load demand.

See section 5.4.3 for details for adjusting V_{OUT} for the adjustable output version of the ZSPM4013B.

3.1. Block Diagram

Figure 3.1 provides a block diagram of the ZSPM4013B, and Figure 3.2 illustrates its monitor and control logic functions, which are explained in section 3.2.

Figure 3.1 ZSPM4013B Block Diagram

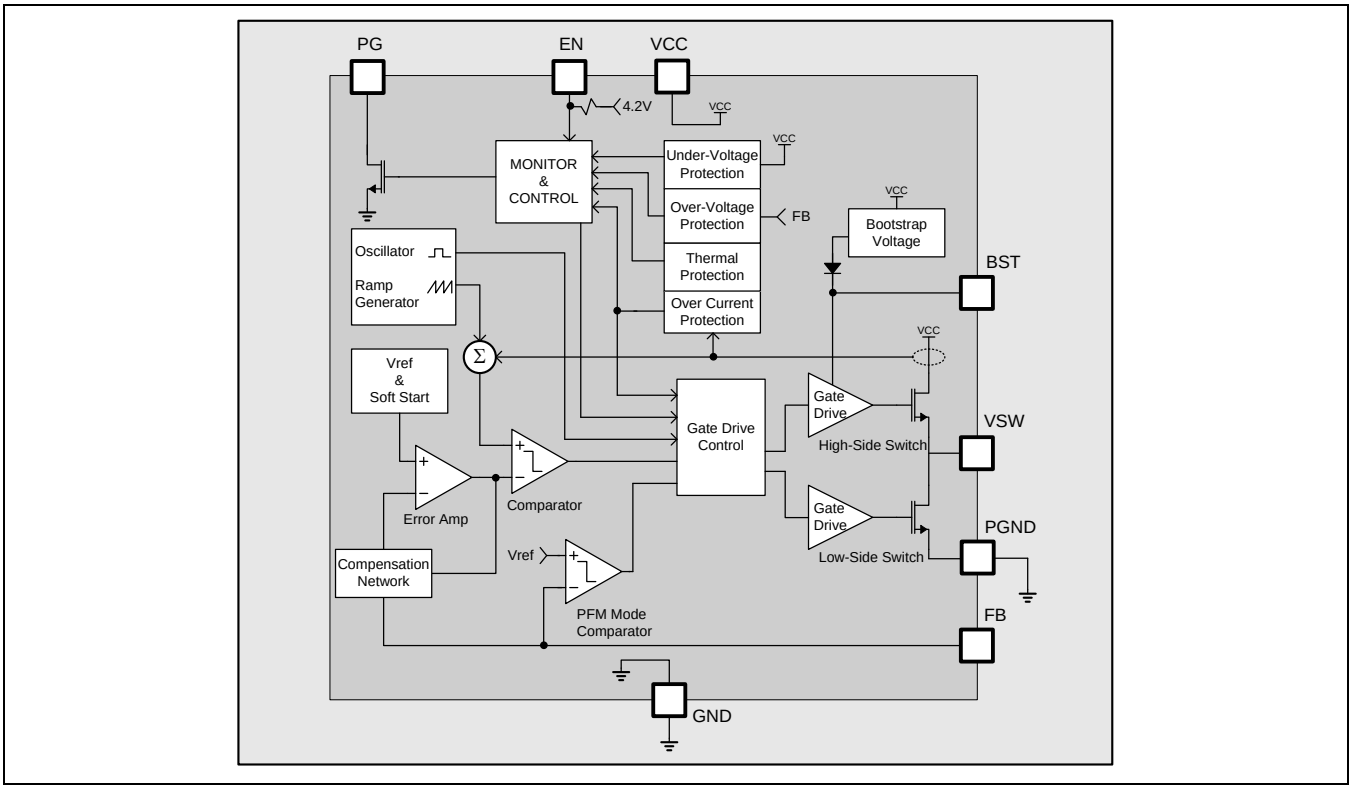
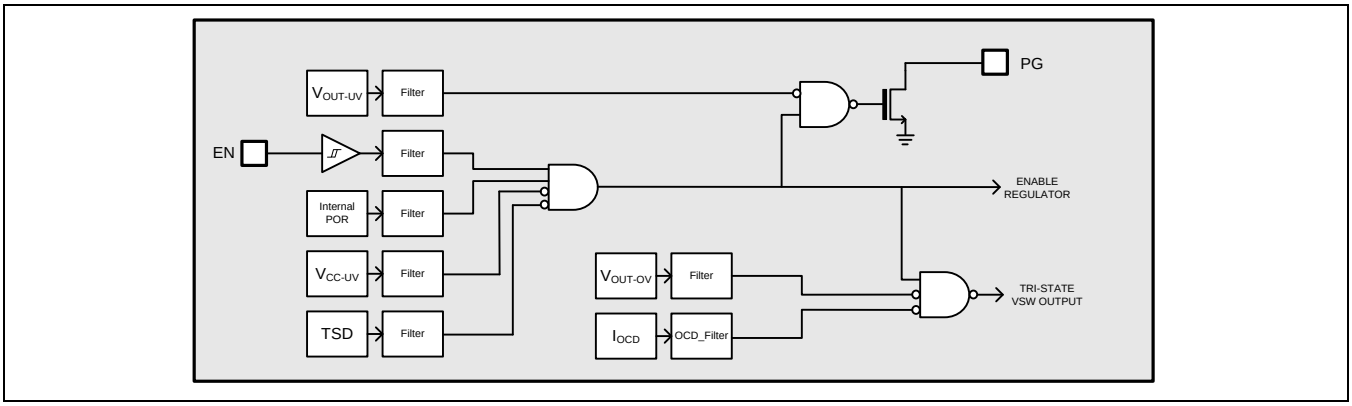


Figure 3.2 Monitor and Control Logic Functionality



3.2. Internal Protection Details

3.2.1. Internal Current Limit

The current through the high-side FET is sensed on a cycle-by-cycle basis, and if the current limit is reached, the over-current detection (OCD) circuit will abbreviate the cycle. The device also senses the FB pin to identify hard short conditions and will direct the VSW output to skip 4 cycles if the current limit occurs when FB is low. This allows current built up in the inductor during the minimum on-time to decay sufficiently. The current limit is always active when the regulator is enabled. Soft start ensures that the current limit does not prevent regulator startup.

An additional feature of the over-current protection circuitry is that under extended over-current conditions, the device will automatically disable. A simple toggle of the EN enable pin will return the device to normal operation.

3.2.2. Thermal Shutdown

If the temperature of the die exceeds 170°C (typical), the thermal shutdown (TSD) circuit will set the VSW outputs to the tri-state level to protect the device from damage. The PG and all other protection circuitry will stay active to inform the system of the failure mode. If the ZSPM4013B cools to 160°C (typical), it will attempt to start up again, following the normal soft start sequence. If the device reaches 170°C, the shutdown/restart sequence will repeat.

3.2.3. Voltage Reference Soft-Start

The voltage reference in this device is ramped at a rate of 4ms to prevent the output from overshoot during startup. This ramp restarts whenever there is a rising edge sensed on the EN pin. This occurs in both the fixed and adjustable versions. During the soft start ramp, current limit is still active and still protects the device if the output is shorted.

3.2.4. VCC Under-Voltage Lockout

The ZSPM4013B is held in the off state until VCC reaches 4.3V (typical). See section 1.4 for the input hysteresis.

3.2.5. Output Over-Voltage Protection

If the output of the regulator exceeds 103% of the regulation voltage, the output over-voltage (OUT-OV) protection circuit will set the VSW outputs to the tri-state level to protect the ZSPM4013B from damage. (See Figure 3.2.) This check occurs at the start of each switching cycle. If it occurs during the middle of a cycle, the switching for that cycle will complete and the VSW outputs will tri-state at the start of the next cycle.

3.2.6. Output Under-Voltage Monitoring

The switched mode output voltage is also monitored by the output under-voltage circuit (OUT-UV) as shown in Figure 3.2. The PG line remains low until the output voltage reaches the V_{OUT-UV} threshold (see Table 1.5). Once the internal comparator detects that the output voltage is above the desired threshold, an internal delay timer is activated and the PG line is de-asserted (to high) once this delay timer expires. In the event that the output voltage decreases below V_{OUT-UV}, the PG line will be asserted low and remain low until the output rises above V_{OUT-UV} and the delay timer times out. There is a hysteresis for the V_{OUT-UV} threshold (see Table 1.5).

4 Application Circuits

4.1. Selection of External Components

The internal compensation is optimized for a 44µF output capacitor (C_{OUT}) and a 4.7µH inductor (L_{OUT}). The minimum allowable value for the output capacitor is 33µF. To keep the output ripple low, a low ESR (less than 35mΩ) ceramic is recommended. The inductor range is 4.7µH +/-20%. For optimal over-current protection, the inductor should be able to handle up to the regulator current limit without saturation.

Connect the VCC pin to the bypass capacitor C_{BYPASS} to improve performance (see section 5.4.1 and Table 1.3).

Connect the BST pin to the bootstrap capacitor C_{BST} as described in section 5.4.2. See Table 1.3 for the recommended value.

For the adjustable version of the ZSPM4013B, an external voltage resistor divider is required (R_{TOP} and R_{BOT}). See section 5.4.3 for details.

4.2. Typical Application Circuits

Figure 4.1 Typical Application for Adjustable Output Voltage

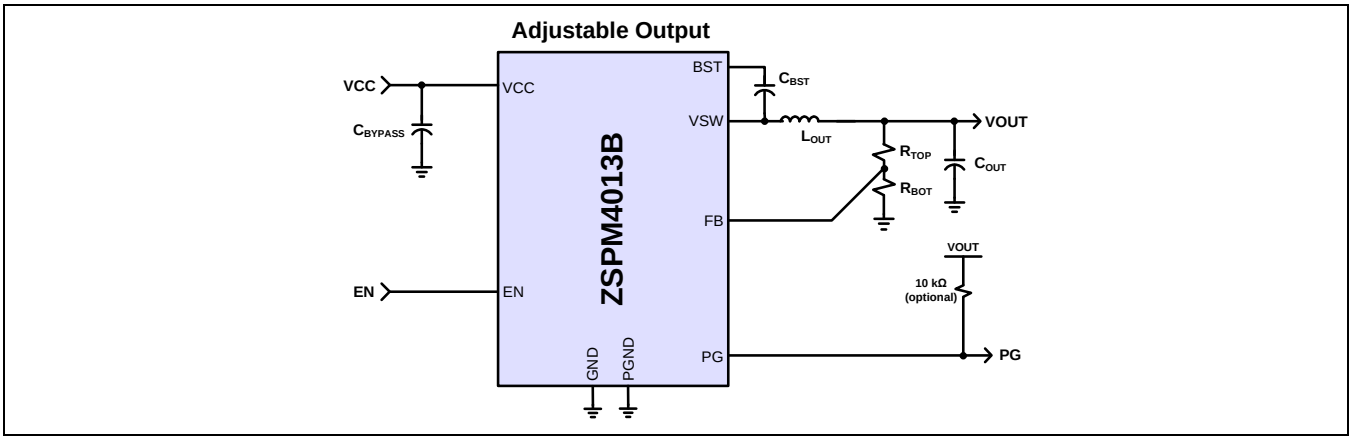
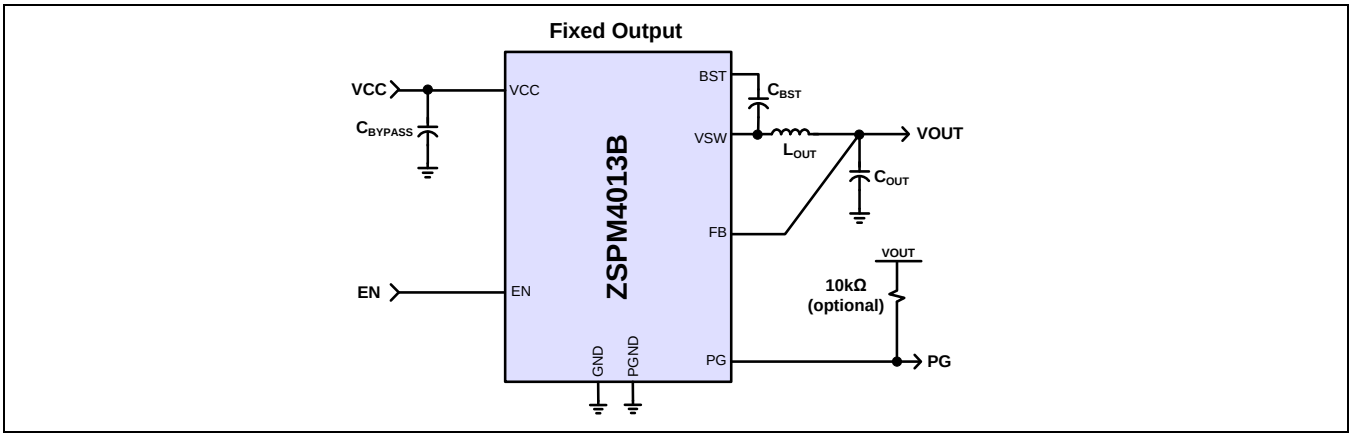


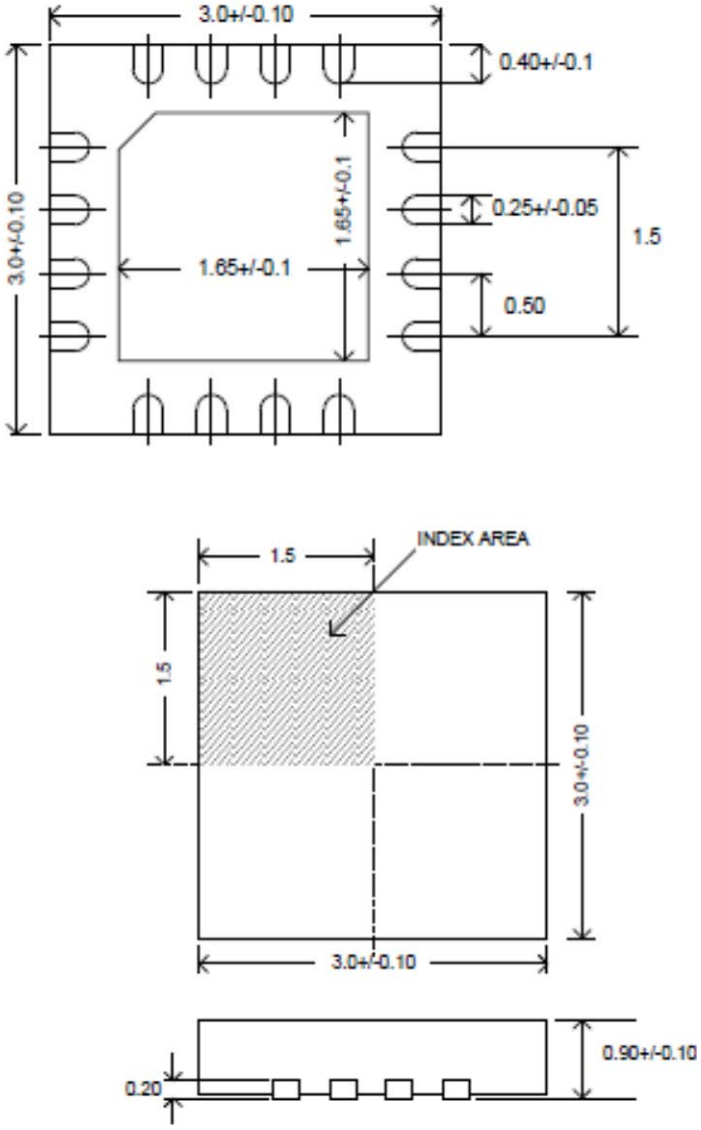
Figure 4.2 Typical Application for Fixed Output Voltage



5 Pin Configuration and Package

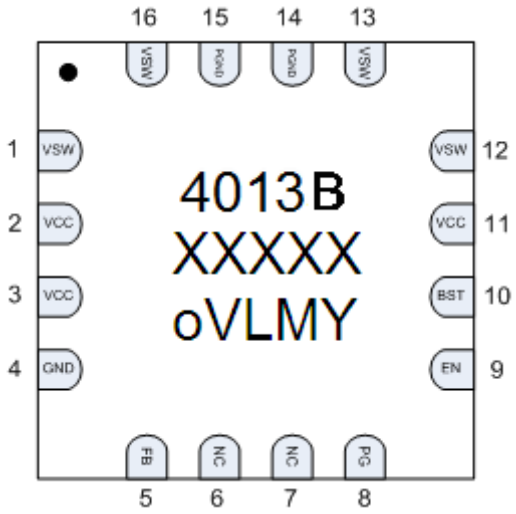
5.1. Package Dimensions

Figure 5.1 ZSPM4013B Package Drawing



5.2. Marking Diagram and Pin-Out

Figure 5.2 16 Lead 3x3mm QFN (top view)



4013B: Part Name
B: Revision
XXXXX: Lot number (last five digits)
O: Pin 1 mark
VL: Voltage level

- 15 1.5V
- 18 1.8V
- 25 2.5V
- 33 3.3V
- 50 5.0V
- 00 0.9V – 5.5V variable

MY: Date Code
M = Month

- 1 January
- 2 February
- 3 March
- 4 April
- 5 May
- 6 June
- 7 July
- 8 August
- 9 September
- A October
- B November
- C December

Y = Year

- A 2011
- B 2012
- C 2013
- etc.

5.3. Pin Description for 16-LEAD 3x3mm QFN

Table 5.1 Pin Description, 16-lead, 3x3mm QFN

Name	Pin #	Function	Description
VSW	1	Switching Voltage Node	Connected to a 4.7µH (typical) inductor. Also connect to additional VSW pins 12, 13, and 16.
VCC	2	Input Voltage	Input voltage. Also connect to additional VCC pins 3 and 11.
VCC	3	Input Voltage	Input voltage. Also connect to additional VCC pins 2 and 11.
GND	4	GND	Primary ground for the majority of the device except the low-side power FET.
FB	5	Feedback Input	Regulator FB voltage. Connects to V_{OUT} for fixed-mode and the output resistor divider for adjustable mode.
NC	6	No Connect	Not connected.
NC	7	No Connect	Not connected.
PG	8	PG Output	Open-drain output.
EN	9	Enable Input	Above 2.2V the device is enabled. Ground this pin to disable the ZSPM4013B. Includes internal pull-up.
BST	10	Bootstrap Capacitor	Bootstrap capacitor for the high-side FET gate driver. Connect a 22nF ceramic capacitor from BST pin to VSW pin.
VCC	11	Input Voltage	Input voltage. Also connect to additional VCC pins 2 and 3.
VSW	12	Switching Voltage Node	Connect to additional VSW pins 1, 13, and 16.
VSW	13	Switching Voltage Node	Connect to additional VSW pins 1, 12, and 16.
PGND	14	Power GND	GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 15.
PGND	15	Power GND	GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 14.
VSW	16	Switching Voltage Node	Connect to additional VSW pins 1, 12, and 13.

5.4. Detailed Pin Description

5.4.1. Unregulated Input, VCC (Pins # 2, 3)

This terminal is the unregulated input voltage source for the ZSPM4013B. It is recommended that a 10µF bypass capacitor be placed close to the device for best performance. Since this is the main supply for the ZSPM4013B, good layout practices must be followed for this connection.

5.4.2. Bootstrap Control, BST (Pin #10)

This terminal will provide the bootstrap voltage required for the high-side internal NMOS switch of the buck regulator. An external ceramic capacitor placed between the BST input terminal and the VSW pin will provide the necessary voltage for the high-side switch. In normal operation, the capacitor is re-charged on every low-side synchronous switching action. If the switch mode approaches 100% duty cycle for the high-side FET, the device will automatically reduce the duty cycle switch to a minimum off time on every 8^{th} cycle to allow this capacitor to re-charge.

5.4.3. Sense Feedback, FB (Pin #5)

This is the input terminal for the output voltage feedback. For the fixed-mode versions, this should be connected directly to V_{OUT}. The connection on the PCB should be kept as short as possible and should be made as close as possible to the capacitor. The trace should not be shared with any other connection. For adjustable-mode versions of the ZSPM4013B, this should be connected to the external resistor divider. To choose the resistors, use the following equation:

$$V_{OUT} = 0.9\ (1 + R_{TOP}/R_{BOT})$$

The input to the FB pin is high impedance, and input current should be less than 100nA. As a result, good layout practices are required for the feedback resistors and feedback traces. When using the adjustable version, the feedback trace should be kept as short and narrow as possible to reduce stray capacitance and the injection of noise.

5.4.4. Switching Output, VSW (Pins #12, 13)

This is the switching node of the regulator. It should be connected directly to the 4.7µH inductor with a wide, short trace and to one end of the bootstrap capacitor. It switches between VCC and PGND at the switching frequency.

5.4.5. Ground, GND (Pin #4)

This ground is used for the majority of the device including the analog reference, control loop, and other circuits.

5.4.6. Power Ground, PGND (Pins #14, 15)

This is a separate ground connection used for the low-side synchronous switch to isolate switching noise from the rest of the device.

5.4.7. Enable, EN (Pin #9)

This is the input terminal to activate the regulator. The input threshold is TTL/CMOS compatible. It also has an internal pull-up to ensure a stable state if the pin is disconnected.

5.4.8. Power Good Output, PG (Pin #8)

This is an open-drain, active-low output. See section 3.2.6 for a description of the function of this pin.

6 Ordering Information

Ordering Code	Description	Package
ZSPM4013BA1W00	3A Synchronous Buck Converter: adjustable output, 0.9V to 5V, 16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W15	3A Synchronous Buck Converter: fixed output, 1.5V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W18	3A Synchronous Buck Converter: fixed output, 1.8V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W25	3A Synchronous Buck Converter: fixed output, 2.5V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W33	3A Synchronous Buck Converter: fixed output, 3.3V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BA1W50	3A Synchronous Buck Converter: fixed output, 5.0V,16-pin 3x3mm QFN	7” reel with 1000 ICs
ZSPM4013BKIT	ZSPM4013B Evaluation Kit for 3A Synchronous Buck Converter	Kit

7 Related Documents

Document
ZSPM4013B Feature Sheet
ZSPM4013B Evaluation Kit Description

Visit IDT’s website www.IDT.com or contact your nearest sales office for the latest version of these documents.

8 Glossary

Term	Description
ESR	Equivalent series resistance.
PFM	Pulse frequency modulation (fixed pulse width).
POR	Power-on reset
PWM	Pulse width modulation (fixed frequency).

9 Document Revision History

Revision	Date	Description
1.00	April 1, 2013	First release of ZSPM4013B, based on ZSPM4013, silicon revision A.
1.10	June 21, 2013	Update to allow for 5.5V output voltage, addition of thermal parameter for “Thermal Resistance Junction to Case (θ_{Jc})” specification, and revision of “Thermal Resistance Junction to Ambient (θ_{JA})” specification.
1.20	February 18, 2014	Revision of specifications for “Input Supply Under Voltage Threshold Hysteresis” in Table 1.4.
	January 25, 2016	Changed to IDT branding.

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