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RENESAS

MOS INTEGRATED CIRCUIT

μPD78F0066

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F0066 is a product of the μPD780065 Subseries in the 78K/0 Series. It is equivalent to the μPD780065 with a flash memory in place of internal ROM[Note]. Because this device can be written and erased electrically without being removed from the substrate, it is ideally suited for evaluation at system development, small-scale production, and for systems likely to be upgraded frequently.

Note The internal ROM capacity is different (refer to **1. DIFFERENCES BETWEEN μPD78F0066 AND MASK ROM VERSIONS** for details).

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μPD780065 Subseries User's Manual : Under preparation
78K/0 Series User's Manual Instruction : U12326E

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory : 48 Kbytes[Note]
- Internal high-speed RAM : 1024 bytes
- Internal expansion RAM : 4096 bytes
- Buffer RAM : 32 bytes
- Operable with the same power supply voltage as that of mask ROM version (V_{DD} = 2.7 to 5.5 V)

Note The flash memory capacity can be changed with the memory size switching register (IMS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to **1. DIFFERENCES BETWEEN μPD78F0066 AND MASK ROM VERSIONS**.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0066GC-8BT	80-pin plastic QFP (14 × 14 mm)	Flash memory

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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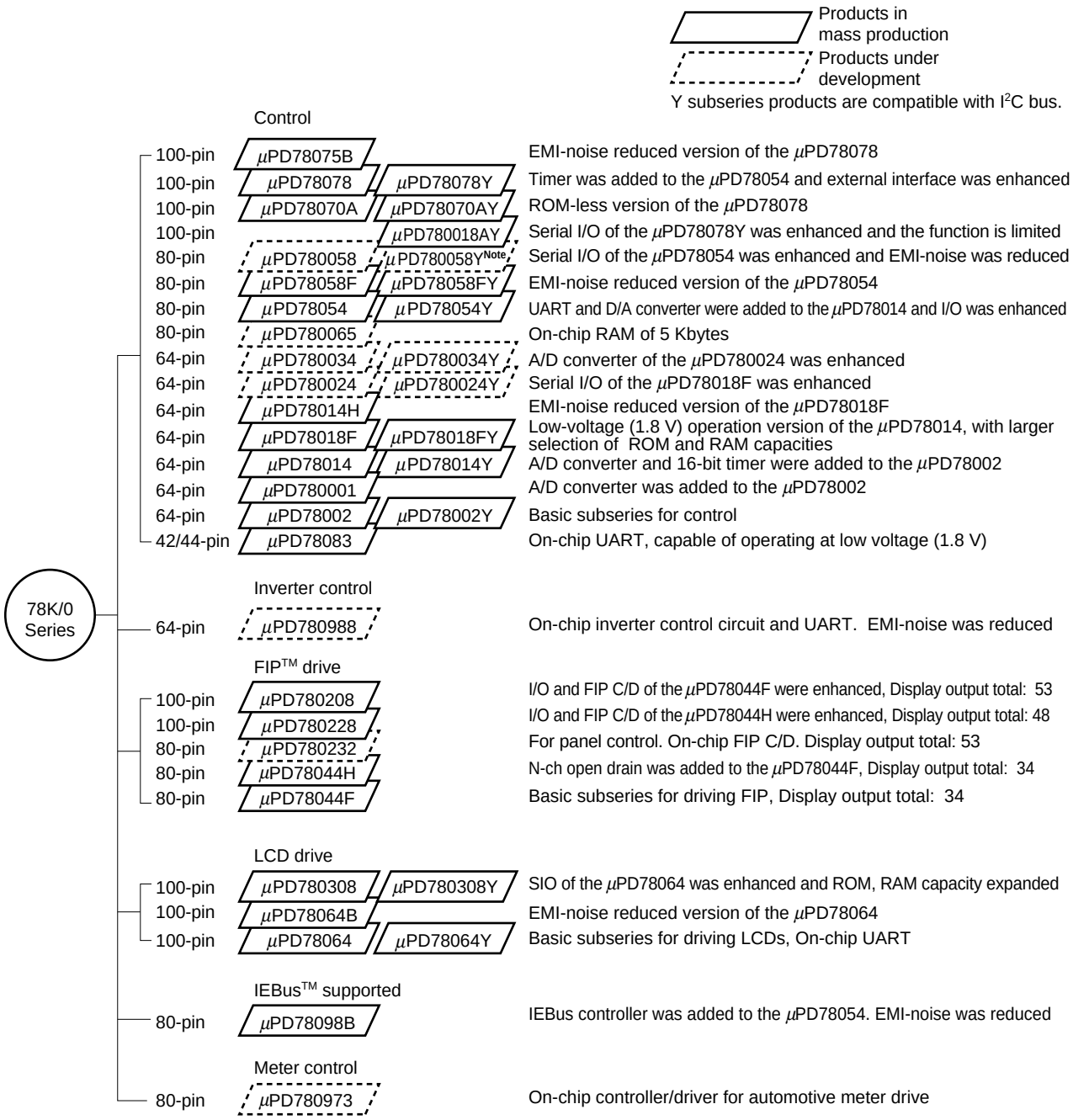
78K/0 SERIES PRODUCT DEVELOPMENT

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available
	μPD78078	48 K to 60 K											
	μPD78070A	—									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							—	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780034	8 K to 32 K					—	8 ch		3 ch (UART: 1 ch, time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	—					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78014	8 K to 32 K										2.7 V	
	μPD780001	8 K		—	—					1 ch	39		—
	μPD78002	8 K to 16 K			1 ch		—				53		Available
	μPD78083				—		8 ch			1 ch (UART: 1 ch)	33	1.8 V	—
Inverter control	μPD780988	32 K to 60 K	3 ch	**Note**	—	1 ch	—	8 ch	—	3 ch (UART: 2 ch)	47	4.0 V	Available
FIP drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780228	48 K to 60 K	3 ch	—	—					1 ch	72	4.5 V	
	μPD780232	16 K to 24 K					4 ch			2 ch	40		
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780308	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (time division UART: 1 ch)	57	2.0 V	—
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
IEBus supported	μPD78098B	40 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	69	2.7 V	Available
Meter control	μPD780973	24 K to 32 K	3 ch	1 ch	1 ch	1 ch	5 ch	—	—	2 ch (UART: 1 ch)	56	4.5 V	—

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

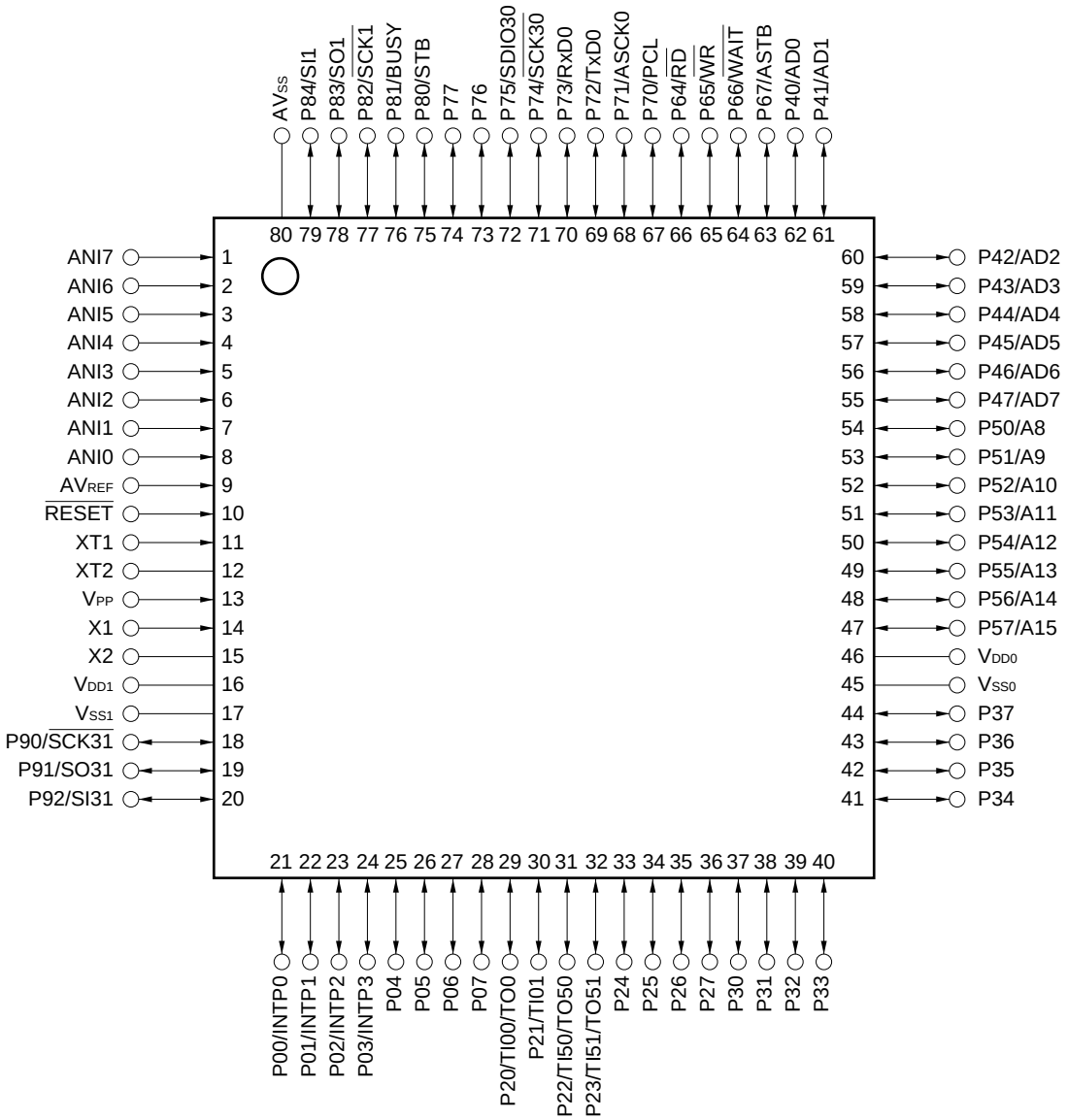
OVERVIEW OF FUNCTION

Item		Function
Internal memory	Flash memory	48 Kbytes[Note]
	High-speed RAM	1024 bytes
	Expansion RAM	4096 bytes
	Buffer RAM	32 bytes
Memory space		64 Kbytes
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time modification function
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38-MHz operation)
	When subsystem clock selected	122 μs (at 32.768-kHz operation)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD correction, etc.
I/O ports		• CMOS I/O : 60
A/D converter		• 8-bit resolution × 8 channels
Serial interface		• 3-wire serial I/O mode : 1 channel • 3-wire serial I/O mode (MAX. 32-byte on-chip automatic transmission/reception function) : 1 channel • 2-wire serial I/O mode : 1 channel • UART mode : 1 channel
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		3 (8-bit PWM output capable: 2)
Clock output		131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 8.38 MHz (main system clock: at 8.38-MHz operation) 32.768 kHz (subsystem clock: at 32.768-kHz operation)
Vectored interrupt source	Maskable	Internal : 13, External : 4
	Non-maskable	Internal : 1
	Software	1
Power supply voltage		V_{DD} = 2.7 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		80-pin plastic QFP (14 × 14 mm)

Note The flash memory capacity can be changed with the memory size switching register (IMS).

PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (14 × 14 mm)**
  μPD78F0066GC-8BT



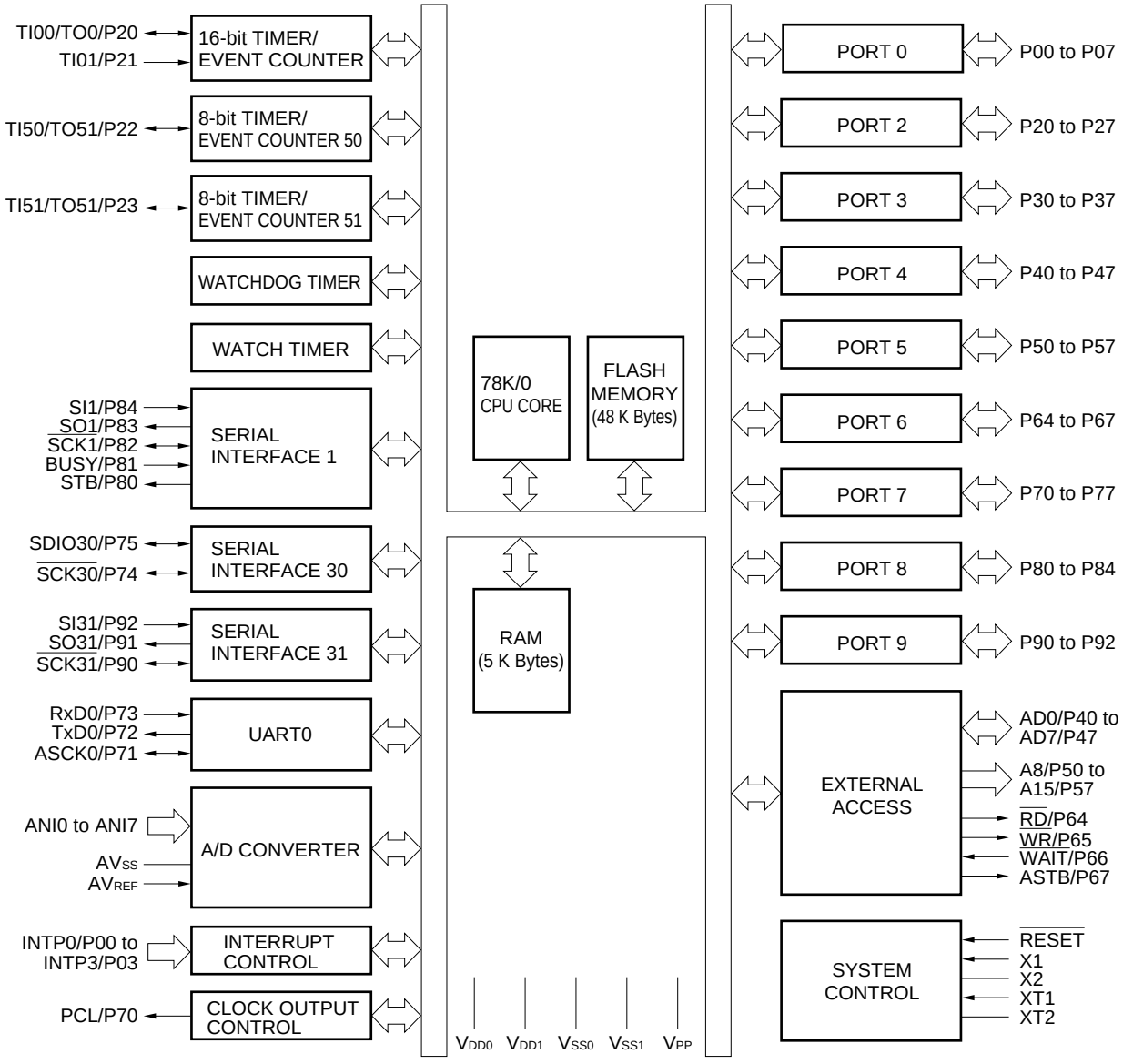
Cautions 1. Connect the V_{PP} pin directly to V_{SS0} in normal operation mode.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD78F0066 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15	: Address Bus	$\overline{RD}$	: Read Strobe
AD0 to AD7	: Address/Data Bus	$\overline{RESET}$	: Reset
ANI0 to ANI7	: Analog Input	RxD0	: Receive Data
ASCK0	: Asynchronous Serial Clock	$\overline{SCK1}$, $\overline{SCK30}$, $\overline{SCK31}$	: Serial Clock
ASTB	: Address Strobe	SDIO30	: Serial Data Input/Output
AV_{REF}	: Analog Reference Voltage	SI1, SI31	: Serial Input
AV_{SS}	: Analog Ground	SO1, SO31	: Serial Output
BUSY	: Busy	STB	: Strobe
INTP0 to INTP3	: Interrupt from Peripherals	TI00, TI01, TI50, TI51	: Timer Input
P00 to P07	: Port0	TO0, TO50, TO51	: Timer Output
P20 to P27	: Port2	TxD0	: Transmit Data
P30 to P37	: Port3	V_{DD0}, V_{DD1}	: Power Supply
P40 to P47	: Port4	V_{PP}	: Programming Power Supply
P50 to P57	: Port5	V_{SS0}, V_{SS1}	: Ground
P64 to P67	: Port6	$\overline{WAIT}$	: Wait
P70 to P77	: Port7	$\overline{WR}$	: Write Strobe
P80 to P84	: Port8	X1, X2	: Crystal (Main system Clock)
P90 to P92	: Port9	XT1, XT2	: Crystal (Subsystem Clock)
PCL	: Programmable Clock		

BLOCK DIAGRAM



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1. DIFFERENCES BETWEEN μPD78F0066 AND MASK ROM VERSIONS

The μPD78F0066 is a product provided with a flash memory that enables on-board writing, erasing, and rewriting of programs with the device mounted on the target system. The functions of the μPD78F0066 (except the functions specified for flash memory) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory version (μPD78F0066) and the mask ROM version (μPD780065).

Table 1-1. Differences between μPD78F0066 and Mask ROM Version

Item	μPD78F0066	Mask ROM Version
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacity	48 Kbytes[Note]	40 Kbytes
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided

Note Flash memory capacity can be set to 40 Kbytes or 48 Kbytes by the memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	INTP0 to INTP3
P04 to P07				—
P20	I/O	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	TI00/TO0
P21				TI01
P22				TI50/TO50
P23				TI51/TO51
P24 to P27				—
P30 to P37	I/O	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	—
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	$\overline{RD}$
P65				$\overline{WR}$
P66				$\overline{WAIT}$
P67				ASTB
P70	I/O	Port 7 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	PCL
P71				ASCK0
P72				TxD0
P73				RxD0
P74				$\overline{SCK30}$
P75				SDIO30
P76, P77				—
P80	I/O	Port 8 5-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	STB
P81				BUSY
P82				$\overline{SCK1}$
P83				SO1
P84				SI1

2.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P90	I/O	Port 9 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, an internal pull-up resistor can be connected by software.	Input	$\overline{SCK31}$
P91				SO31
P92				SI31

2.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP3	Input	External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00 to P03
TI00	Input	External count clock input to 16-bit timer (TM0). Capture trigger signal input to capture register (CR01) of TM0.	Input	P20/TO0
TI01		Capture trigger signal input to capture register (CR00) of TM0.		P21
TI50		External count clock input to 8-bit timer (TM50).		P22/TO50
TI51		External count clock input to 8-bit timer (TM51).		P23/TO51
TO0	Output	16-bit timer output.	Input	P20/TI00
TO50		8-bit timer output (shared with 8-bit PWM output).		P22/TI50
TO51				P23/TI51
SI1	Input	Serial interface serial data input.	Input	P84
SI31	Input			P92
SO1	Output	Serial interface serial data output.	Input	P83
SO31	Output			P91
SDIO30	I/O	Serial interface serial data input/output.	Input	P75
$\overline{SCK1}$	I/O	Serial interface serial clock input/output.	Input	P82
$\overline{SCK30}$			Input	P74
$\overline{SCK31}$			Input	P90
BUSY	Input	Busy input for serial interface automatic transmission/reception.	Input	P81
STB	Output	Strobe output for serial interface automatic transmission/reception.	Input	P80
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P73
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P72
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P71
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P70
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{WR}$	Output	Strobe signal output for write operation of external memory.	Input	P65
$\overline{WAIT}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	—

2.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
AV_{REF}	Output	A/D converter reference voltage input (shared with analog power supply).	—	—
AV_{SS}	—	A/D converter ground potential. Voltage equal to V_{SS0} or V_{SS1}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
V_{DD0}	—	Positive power supply voltage for ports.	—	—
V_{DD1}	—	Ground potential of ports.	—	—
V_{SS0}	—	Positive power supply (except ports).	—	—
V_{SS1}	—	Ground potential (except ports).	—	—
V_{PP}	—	Applying high-voltage for program write/verify. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	—	—

2.3 Recommended Connection of Unused Pins

Table 2-1 shows the recommended connection of unused pins.

Table 2-1. Recommended Connection of Unused Pins

Pin Name	I/O	Recommended Connection when Not Used
P00/INTP0	I/O	Independently connect to V_{SS0} through resistor.
P01/INTP1		
P02/INTP2		
P03/INTP3		
P04 to P07		
P20/TI00/TO0		Independently connect to V_{DD0} or V_{SS0} through resistor.
P21/TI01		
P22/TI50/TO50		
P23/TI51/TO51		
P24 to P27		
P30 to P37		Independently connect to V_{DD0} or V_{SS0} through resistor.
P40/AD0 to P47/AD7		Independently connect to V_{DD0} through resistor.
P50/A8 to P57/A15		Independently connect to V_{DD0} or V_{SS0} through resistor.
P64/$\overline{RD}$		
P65/$\overline{WR}$		
P66/$\overline{WAIT}$		
P67/ASTB		
P70/PCL		
P71/ASCK0		
P72/TxD0		
P73/RxD0		
P74/$\overline{SCK30}$		
P75/SDIO30		
P76, P77		
P80/STB		
P81/BUSY		
P82/$\overline{SCK1}$		
P83/SO1		
P84/SI1		
P90/$\overline{SCK31}$		
P91/SO31		
P92/SI31		
ANI0 to ANI7	Input	Connect to V_{SS0}.
XT1		Connect to V_{DD0}.
XT2	—	Leave open.
AV_{REF}		Connect to V_{SS0}.
AV_{SS}		
V_{PP}		Directly connect to V_{SS0} or V_{SS1}.

3. MEMORY SIZE SWITCHING REGISTER (IMS)

This register sets a part of internal memory unused by software. The memory map can be made the same as that of mask ROM versions with different types of internal ROM capacities by setting the memory size switching register (IMS).

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Caution To initialize the program, be sure to set IMS to the value shown in Figure 3-1. Also be sure to set IMS to the value shown in Figure 3-1 after resetting, because reset input sets IMS to CFH.

Figure 3-1. Format of Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
1	0	1	0	40 Kbytes
1	1	0	0	48 Kbytes
Others				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-speed RAM Capacity
1	1	0	1024 bytes
Others			Setting prohibited

Table 3-1 shows the IMS set value to make the memory map the same as those of mask ROM versions.

Table 3-1. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780065	CAH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

The internal expansion RAM size switching register (IXS) is the register that sets the internal expansion RAM capacity.

IXS is set with a 1-bit memory manipulation instruction or an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IXS to 0CH.

Caution To initialize the program, be sure to set IXS to 04H. Also be sure to set IXS to 04H after resetting, because reset input sets IXS to 0CH.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of Internal Expansion RAM Capacity
0	1	0	0	4096 bytes
Others				Setting prohibited

5. FLASH MEMORY PROGRAMMING

Writing to a flash memory can be performed without removing the memory from the target system (on-board). Writing is performed by connecting the dedicated flash programmer (Flashpro II) to the host machine and the target system.

Also, writing to a flash memory can be performed on an adapter for flash memory writing, which is connected to Flashpro II.

Remark Flashpro II is a product of Naitou Densei Machidaseisakusho Co., Ltd.

5.1 Selection of Transmission Method

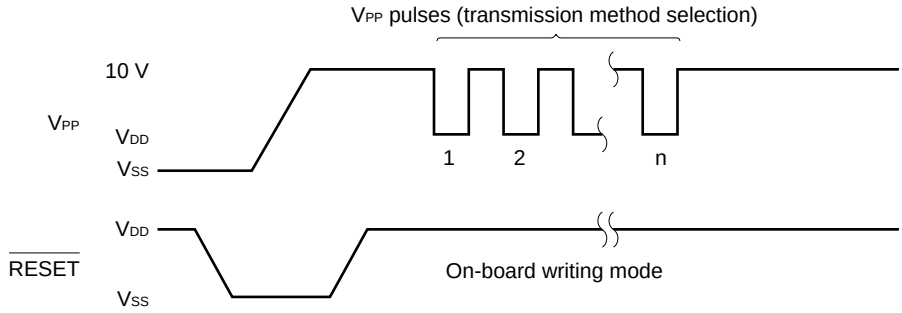
Writing to a flash memory is performed using Flashpro II with a serial transmission mode. One of the transmission method is selected from those in Table 5-1. The selection of the transmission method is made by using the format shown in Figure 5-1. Each transmission method is selected by the number of V_{PP} pulses shown in Table 5-1.

Table 5-1. List of Transmission Method

Transmission Method	Channels	Pin	V_{PP} Pulses
3-wire serial I/O	2	$\overline{SCK31}$/P90 SO31/P91 SI31/P92	0
		$\overline{SCK1}$/P82 SO1/P83 SI1/P84	1
UART	1	TxD0/P72 RxD0/P73	8

Caution Select a transmission method always using the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Format of Transmission Method Selection



5.2 Function of Flash Memory Programming

Operations such as writing to a flash memory are performed by various command/data transmission and reception operations according to the selected transmission method. Table 5-2 shows major functions of flash memory programming.

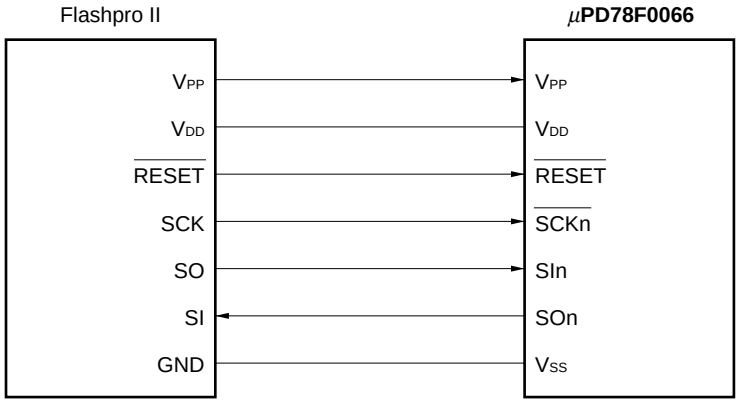
Table 5-2. Major Functions of Flash Memory Programming

Function	Description
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch delete	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Delete time setting	Sets the memory delete time.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

5.3 Connection of Flashpro II

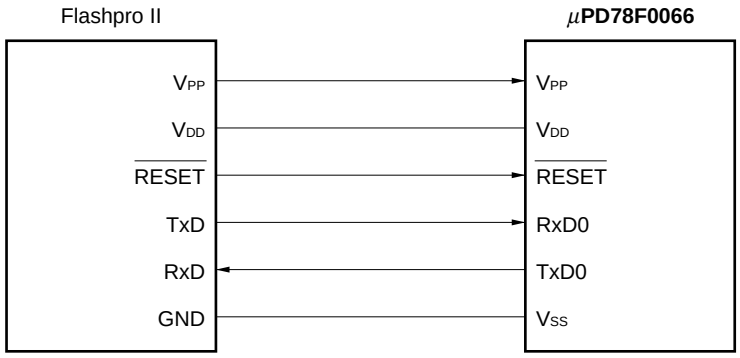
The connection of the Flashpro II and the μPD78F0066 differs according to the transmission method. The connection for each transmission method is shown in Figures 5-2 and 5-3.

Figure 5-2. Connection of Flashpro II for 3-wire Serial I/O System



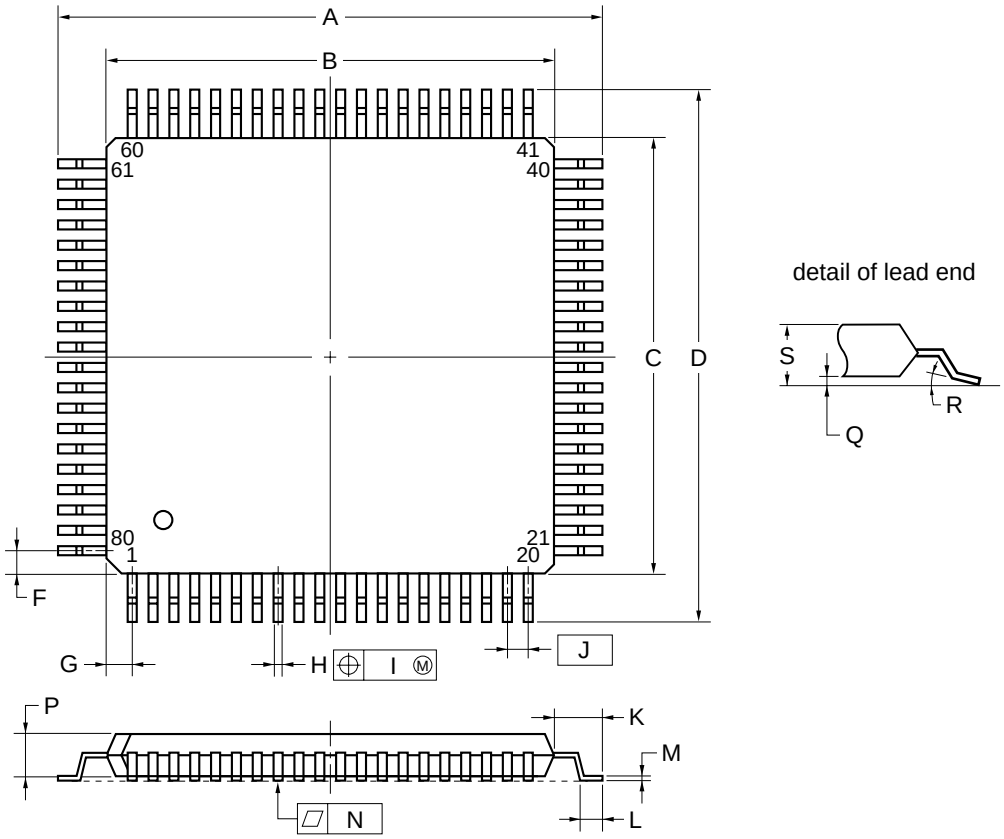
n = 1, 31

Figure 5-3. Connection of Flashpro II for UART System



6. PACKAGE DRAWING

80 PIN PLASTIC QFP (14×14)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD780065 Subseries. Refer to **(5) Cautions when the development tools are used.**

(1) Language processing software

RA78K/0	78K/0 Series common assembler package
CC78K/0	78K/0 Series common C compiler package
DF780065[Note]	Device file for the μPD780065 Subseries
CC78K/0-L	78K/0 Series common C compiler library source file

Note Under development

(2) Flash memory writing tools

Flashpro II (Part number: FL-PR2)	Dedicated flash programmer for microcomputers incorporating flash memory
FA-80GC[Note]	Adapter for flash memory writing

Note Under development

(3) Debugging tools

- **When using the IE-78K0-NS in-circuit emulator**

IE-78K0-NS	78K/0 Series common in-circuit emulator
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 Series computer (except notebook-type personal computer) is used as host machine
IE-70000-CD-IF	PC card and interface cable necessary when a PC-9800 Series notebook-type personal computer is used as host machine
IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT™ or a compatible machine is used as host machine
IE-780065-NS-EM4[Note]	Probe board necessary when emulating the μPD780065 Subseries
IE-78K0-NS-P01	I/O board necessary when emulating the μPD780065 Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GC-8BT type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	78K/0 Series common system simulator
DF780065[Note]	Device file for the μPD780065 Subseries

Note Under development

- **When using the IE-78001-R-A in-circuit emulator**

IE-78001-R-A	78K/0 Series common in-circuit emulator
IE-70000-98-IF-B IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 Series computer (except notebook-type personal computer) is used as host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT or a compatible machine is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as host machine
IE-780065-NS-EM4**Note**	Probe board necessary when emulating the μPD780065 Subseries
IE-78K0-NS-P01	I/O board necessary when emulating the μPD780065 Subseries
IE-78K0-R-EX1**Note**	Emulation probe conversion board necessary when the IE-780065-NS-EM4 + IE-78K0-NS-P01 is used in the IE-78001-R-A.
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GC-8BT type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	78K/0 Series common system simulator
DF780065**Note**	Device file for the μPD780065 Subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions when the development tools are used

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780065.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and DF780065.
- Flashpro II, FA-80GC, and NP-80GC are products of Naitou Densei Machidaseisakusho Co., Ltd. (TEL: (044) 822-3813). Contact an NEC distributor when purchasing these products.
- Refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.
- Host machines and OSs compatible with the software are as follows:

Host Machine [OS] / Software	PC PC-9800 Series [Windows™] IBM PC/AT and compatible machines [Japanese/English Windows]	EWS HP9000 Series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√Note	√
CC78K/0	√Note	√
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS based software

APPENDIX B. RELATED DOCUMENTS

Documents Related Devices

Document Name	Document No.	
	English	Japanese
μPD780065 Subseries User's Manual	To be prepared	Under preparation
μPD780065 Preliminary Product Information	To be prepared	Under preparation
μPD78F0066 Preliminary Product Information	This document	U13419J
78K/0 Series User's Manual - Instruction	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J

Development Tool Documents (User's Manual)

Document Name		Document No.	
		English	Japanese
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K/0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-How	U13034E	U13034J
CC78K Series Library Source File		—	U12322J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-EM		To be prepared	To be prepared
IE-780065-NS-EM4		To be prepared	To be prepared
EP-78230		EEU-1515	EEU-985
SM78K0 System Simulator Windows Based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger PC Based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS Based	Reference	—	U11151J
ID78K0 Integrated Debugger PC Based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows Based	Guide	U11649E	U11649J

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Embedded Software Documents (User's Manual)

Document Name		Document No.	
		English	Japanese
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
OS for 78K/0 Series MX78K0	Basics	U12257E	U12257J

Other Related Documents

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer Product Series Guide	—	U11416J

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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