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April 1st, 2010
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RENESAS

MOS INTEGRATED CIRCUIT

μPD789011, 789012

8-BIT SINGLE-CHIP MICROCONTROLLER

Phase-out/Discontinued

The μPD789011 and 789012 are products in the μPD789014 Subseries of compact, general-purpose microcontrollers in the 78K/0S Series. In addition to an 8-bit CPU, these products have substantial hardware such as on-chip I/O ports, timers, serial interface, and interrupt controls.

The μPD78P9014, one-time PROM product that can be written only once, and various development tools are also available.

These user's manuals contain detailed descriptions of the functions. Be sure to read them before designing.

μPD78P9014 Subseries User's Manual : U11187E
78K/0S Series User's Manual — Instruction : U11047E

FEATURES

- ROM and RAM capacity

Item / Product Name	Program Memory (ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD789011	2 Kbytes	128 bytes	28-pin plastic shrink DIP (400 mil) 28-pin plastic SOP (375 mil)
μPD789012	4 Kbytes		

- Minimum instruction execution time changeable to the high-speed (0.4 μs) and the low-speed (1.6 μs)
- I/O ports: 22
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode selectable
- Timers: 3 channels
  - 8-bit timer/event counter: 2 channels
  - Watchdog timer: 1 channel
- Power supply voltage : V_{DD} = 1.8 to 5.5 V

The information in this document is subject to change without notice.

Document No. U11095EJ1V0DS00 (1st edition)
Date Published November 1997 N
Printed in Japan

The mark ★ shows major revised points.

APPLICATION FIELDS

Compact household appliances, remote controls, games, etc.

ORDERING INFORMATION

Part Number	Package
μPD789011CT-×××	28-pin plastic shrink DIP (400 mil)
μPD789011GT-×××	28-pin plastic SOP (375 mil)
μPD789012CT-×××	28-pin plastic shrink DIP (400 mil)
μPD789012GT-×××	28-pin plastic SOP (375 mil)

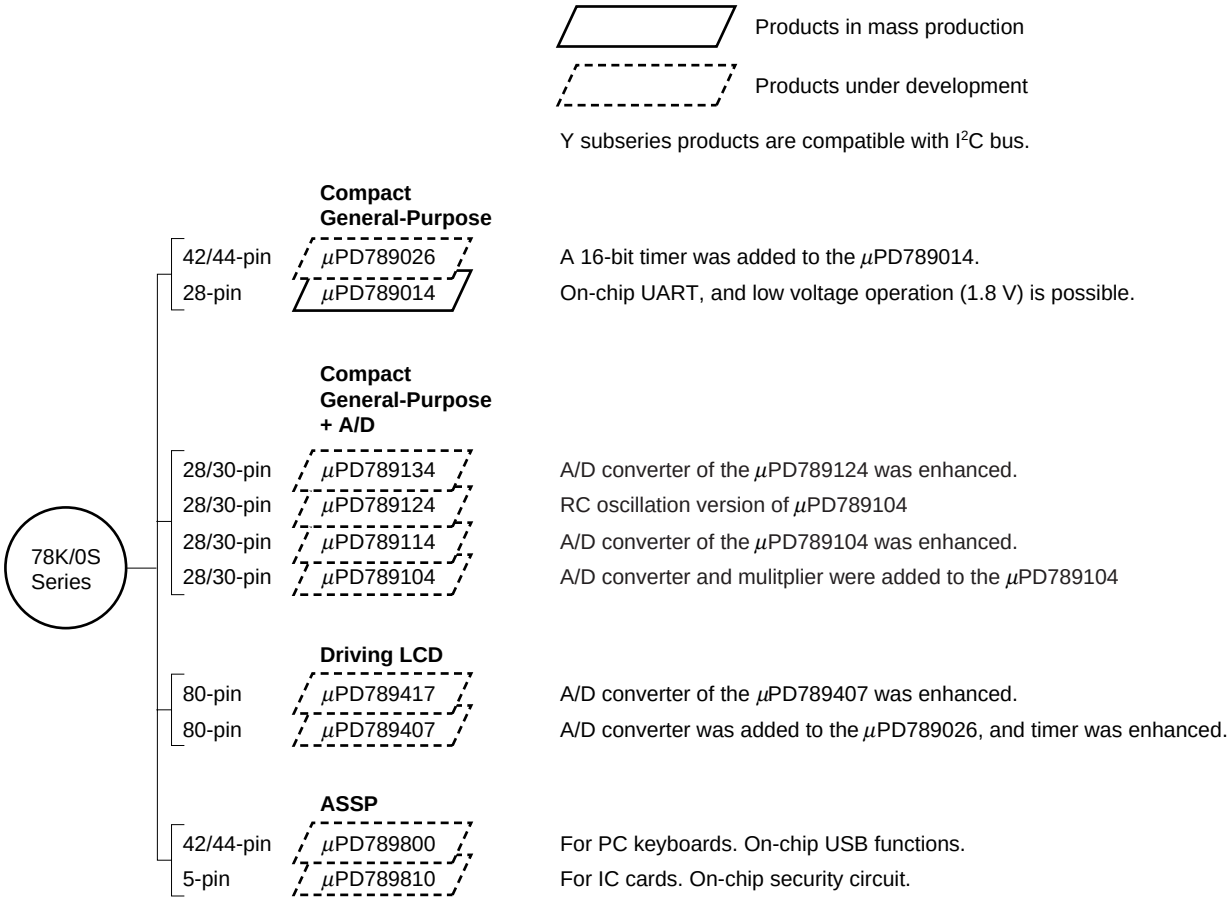
Remark ××× indicates the ROM code suffix.

OVERVIEW OF THE FUNCTIONS

Item		μPD789011	μPD789012
On-chip memory	ROM	2 Kbytes	4 Kbytes
	High-speed RAM	128 bytes	
General-purpose registers		8 bits × 8 registers	
Minimum instruction execution time		0.4 μs or 1.6 μs (at 5.0-MHz operation with main system clock)	
Instruction set		• 16-bit calculations • Bit manipulation (set, reset, test)	
I/O ports		CMOS I/O : 22	
Serial interface		3-wire serial I/O mode/UART mode selectable : 1 channel	
Timers		• 8-bit timer/event counter : 2 channels • Watchdog timer : 1 channel	
Timer output		2	
Vector interrupt source	Maskable	Internal: 6, External: 3	
	Non-maskable	Internal: 1	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Ambient operating temperature		T_A = –40 to +85°C	
Package		• 28-pin plastic shrink DIP (400 mil) • 28-pin plastic SOP (375 mil)	

78K/0S Series Expansion

The following shows the 78K/0S Series products development. Subseries names are shown inside frames.



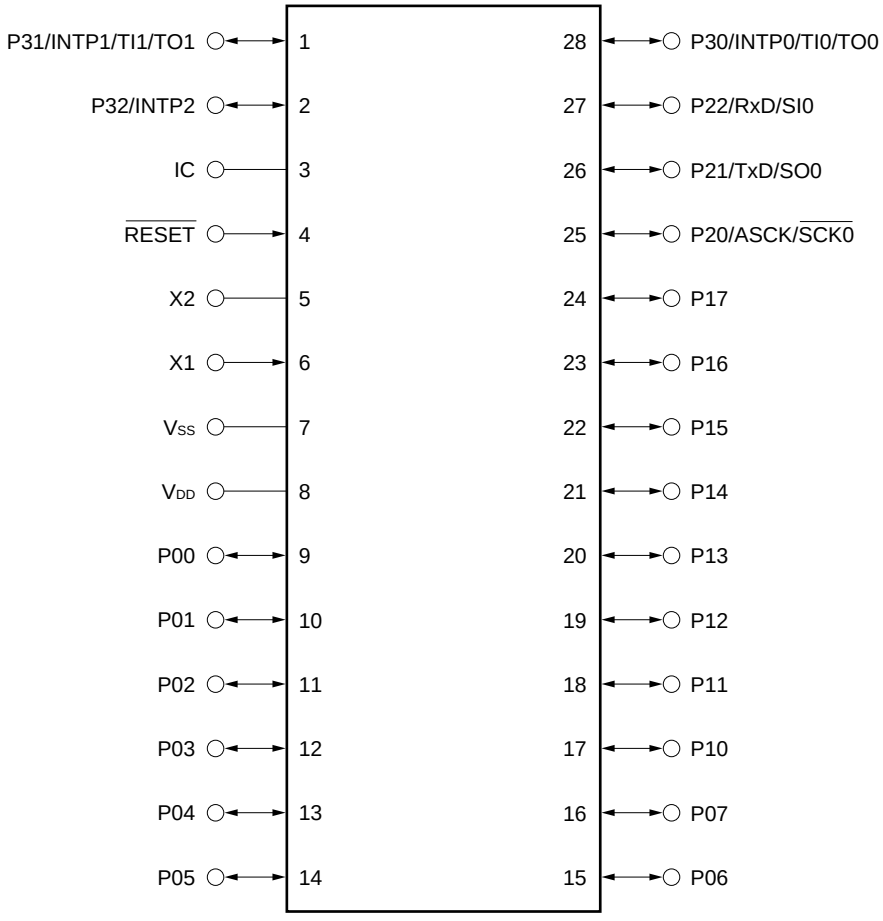
The following lists the main functional differences between subseries products.

Subseries Name / Function		ROM Capacity	Timers				8-bit A/D	10-bit A/D	Serial Interface	I/O	Minimum V_{DD}	Remark
			8-bit	16-bit	Watch	WDT						
Compact, general-purpose	μPD789026	4K to 16K	1ch	1ch	—	1ch	—	—	1ch (UART :1 ch)	34	1.8 V	—
	μPD789014	2K to 4K	2ch	—						22		
Compact, general-purpose + A/D	μPD789134	2K to 8K	1ch	1ch	—	1ch	—	4ch	1ch (UART : 1ch)	20	1.8 V	RC oscillation version
	μPD789124						4ch	—				
	μPD789114						—	4ch				—
	μPD789104						4ch	—				
LCD driving	μPD789417	12K to 24K	3ch	1ch	1ch	1ch	—	7ch	1ch (UART : 1ch)	43	1.8 V	—
	μPD789407						7ch	—				
ASSP	μPD789800	8K	2ch	—	—	1ch	—	—	2ch (USB : 1ch)	31	4.0 V	—
	μPD789810	6K	—							1	1.8 V	On-chip EEPROM™

CONTENTS

1. PIN CONFIGURATION (Top View)

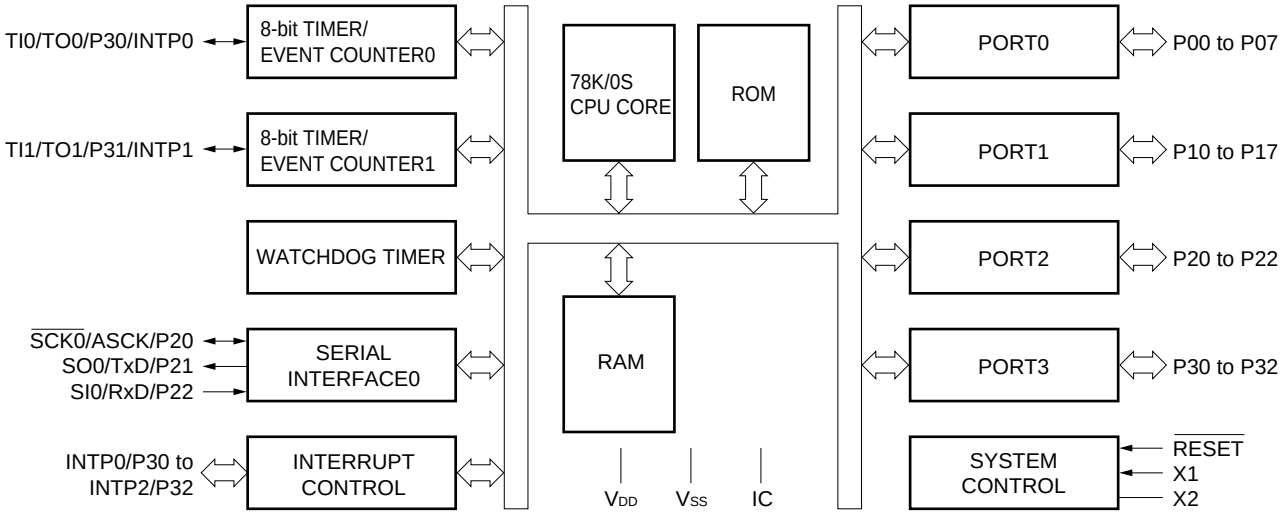
- **28-pin plastic shrink DIP (400 mil)**
  μPD789011CT-×××
  μPD789012CT-×××
- **28-pin plastic SOP (375 mil)**
  μPD789011GT-×××
  μPD789012GT-×××



Caution Connect IC pin directly to V_{SS}.

ASCK	:	Asynchronous Serial Clock	$\overline{SCK0}$	:	Serial Clock
IC	:	Internally Connected	SI0	:	Serial Input
INTP0 to INTP2	:	Interrupt from Peripherals	SO0	:	Serial Output
P00 to P07	:	Port0	TI0, TI1	:	Timer Input
P10 to P17	:	Port1	TO0, TO1	:	Timer Output
P20 to P22	:	Port2	TxD	:	Transmit Data
P30 to P32	:	Port3	V_{DD}	:	Power Supply
$\overline{RESET}$	:	Reset	V_{SS}	:	Ground
RxD	:	Receive Data	X1, X2	:	Crystal

2. BLOCK DIAGRAM



3. PIN FUNCTION LIST

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	—
P10 to P17	I/O	Port 1 8-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	—
P20	I/O	Port 2 3-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	ASCK/$\overline{\text{SCK0}}$
P21				TxD/SO0
P22				RxD/SI0
P30	I/O	Port 3 3-bit I/O port Input/output specifiable bit-wise When used as an input port, on-chip pull-up resistor can be used by software. LEDs can be directly driven.	Input	INTP0/TI0/TO0
P31				INTP1/TI1/TO1
P32				INTP2

3.2 Non-port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0**Note**	Input	External interrupt input whose valid edge can be specified (rising edge, falling edge, or both the rising and falling edges).	Input	P30/TI0/TO0
INTP1**Note**				P31/TI1/TO1
INTP2**Note**				P32
SI0**Note**	Input	Serial data input in the serial interface	Input	P22/RxD
SO0	Output	Serial data output in the serial interface	Input	P21/TxD
$\overline{\text{SCK0}}$**Note**	I/O	Serial clock I/O for the serial interface	Input	P20/ASCK
RxD**Note**	Input	Serial data input for the asynchronous serial interface	Input	P22/SI0
TxD	Output	Serial data output for the asynchronous serial interface	Input	P21/SO0
ASCK**Note**	Input	Serial clock input for the asynchronous serial interface	Input	P20/SCK0
TI0**Note**	Input	External count clock input to the 8-bit timer (TM0)	Input	P30/INTP0/TO0
TI1**Note**		External count clock input to the 8-bit timer (TM1)		P31/INTP1/TO1
TO0	Output	8-bit timer output	Input	P30/INTP0/TI0
TO1				P31/INTP1/TI1
$\overline{\text{RESET}}$	Input	System reset input	Input	—
X1	Input	Crystal connection for the main system clock oscillation	—	—
X2	—		—	—
V_{DD}	—	Positive power supply	—	—
IC	—	Internally connected. Connect directly to V_{SS}.	—	—
V_{SS}	—	Ground potential	—	—

★ **Note** These pins are input through Schmitt triggers (See **Type 5-D in Figure 3-1 Pin I/O Circuit Types**).

3.3 Pin I/O Circuit and Recommended Connections of Unused Pins

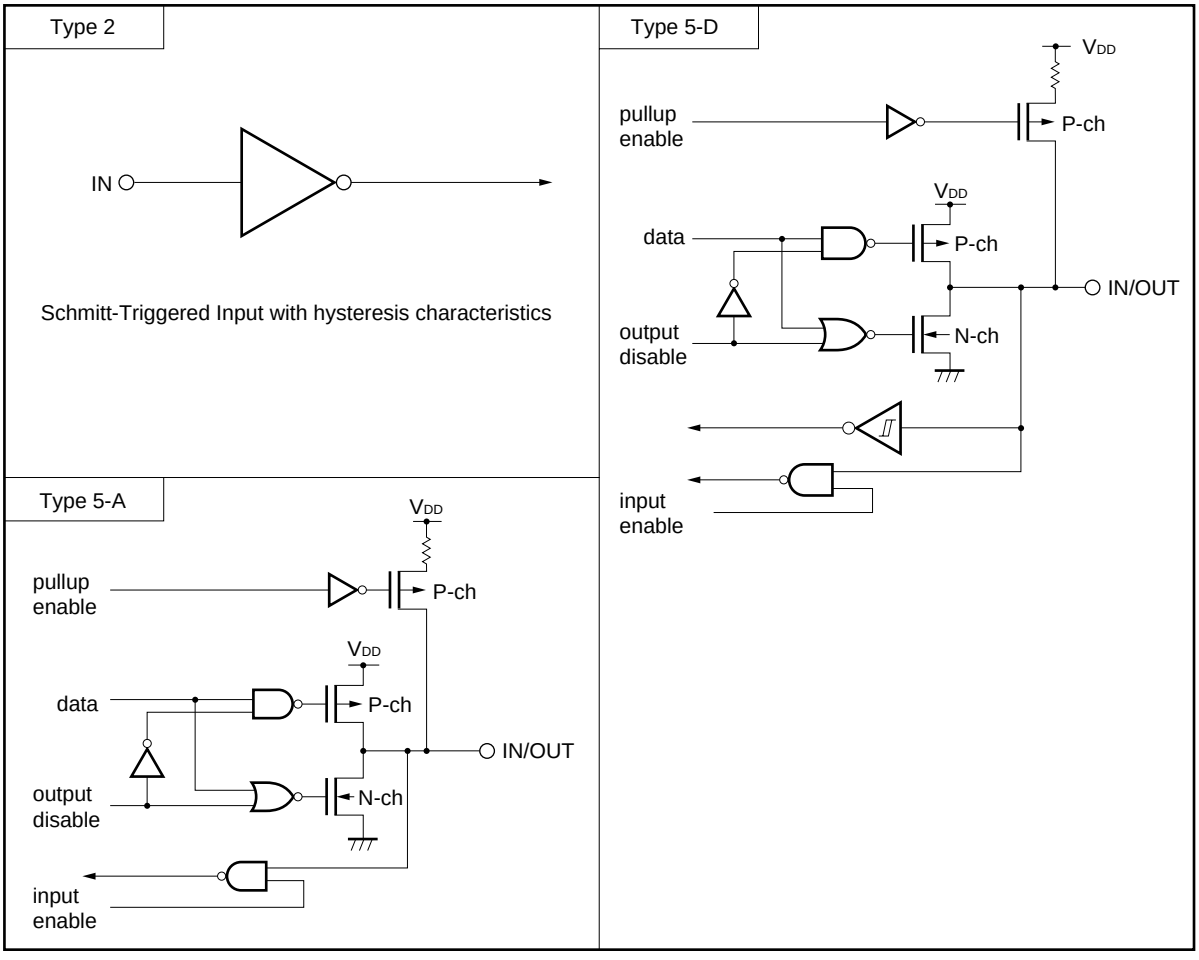
Table 3-1 shows the types of the I/O circuits of each pin and the connections for unused pins.

See Figure 3-1 for the structure of each type of I/O circuit.

Table 3-1. Types of Pin I/O Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection for Unused Pins
P00-P07	5-A	I/O	Connect to V_{DD} or V_{SS} via a resistor independently.
P10-P17			
P20/ASCK/$\overline{SCK0}$	5-D		
P21/TxD/SO0	5-A		
P22/RxD/SI0	5-D		
P30/INTP0/TI0/TO0			Connect to V_{SS} via a resistor independently.
P31/INTP1/TI1/TO1			
P32/INTP2			
$\overline{RESET}$	2	—	—
IC	—	—	Connect directly to V_{SS}.

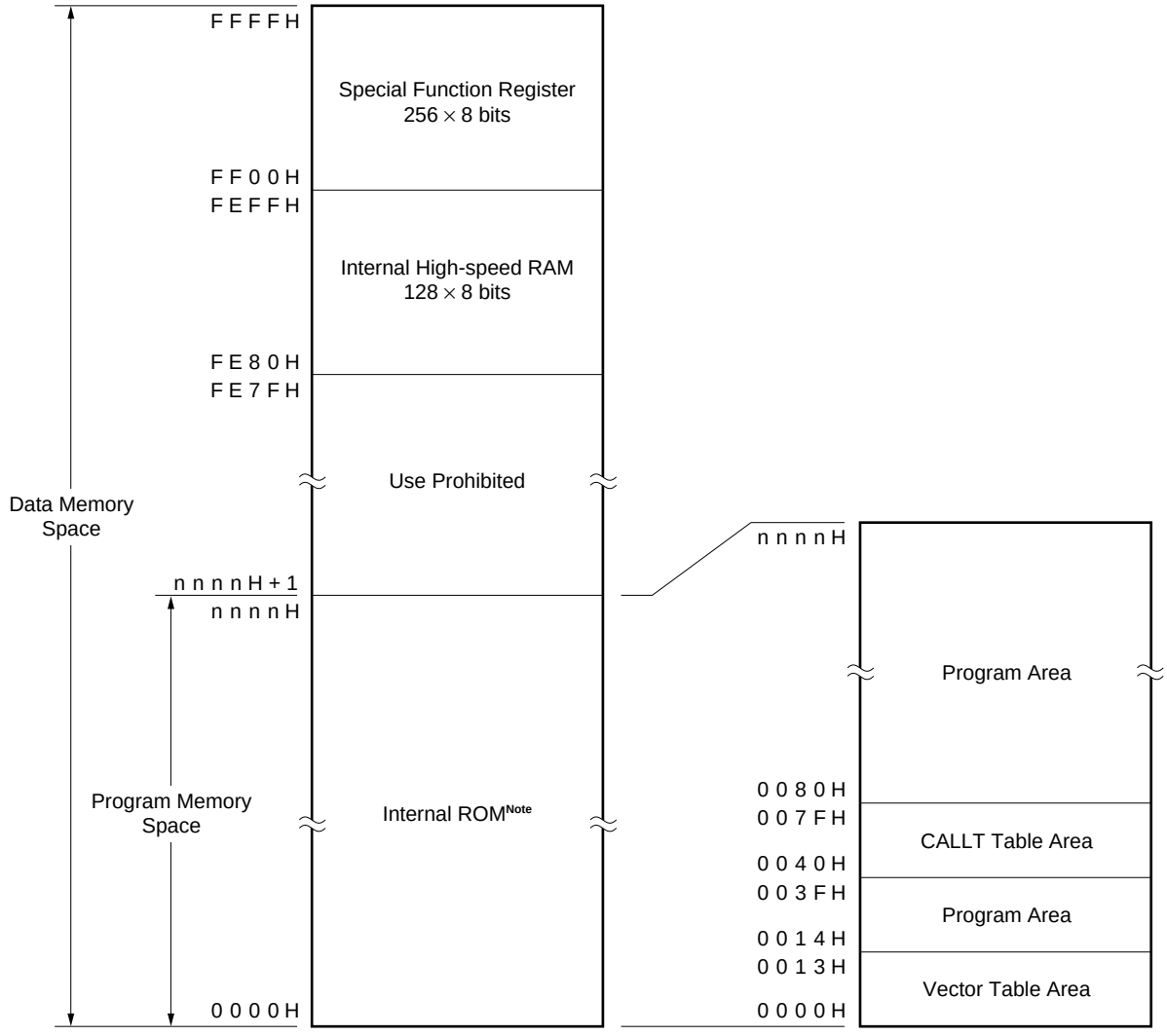
Figure 3-1. Summary of the Pin I/O Circuits



4. MEMORY SPACE

Figure 4-1 shows the μPD789011 and 789012 memory map.

Figure 4-1. Memory Map



Note Internal ROM capacity differs depending on the product (see the table below).

Product Name	Internal ROM Bottom Address nnnnH
μPD789011	07FFH
μPD789012	0FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The μPD789011 and 789012 are provided with the ports shown below, which enable various types of control.

Table 5-1. Port Functions

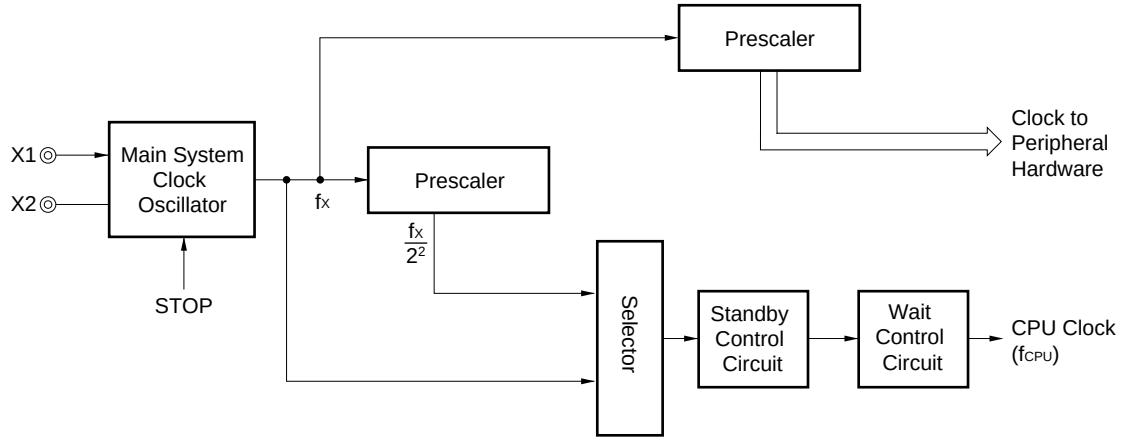
Name	Pin Name	Function
Port 0	P00 to P07	8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 2	P20 to P22	3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.
Port 3	P30 to P32	3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.

5.2 Clock Generator

The main system clock generator is incorporated. Also, the minimum instruction execution can be changed.

- 0.4 μs/1.6 μs (at 5.0-MHz operation with main system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

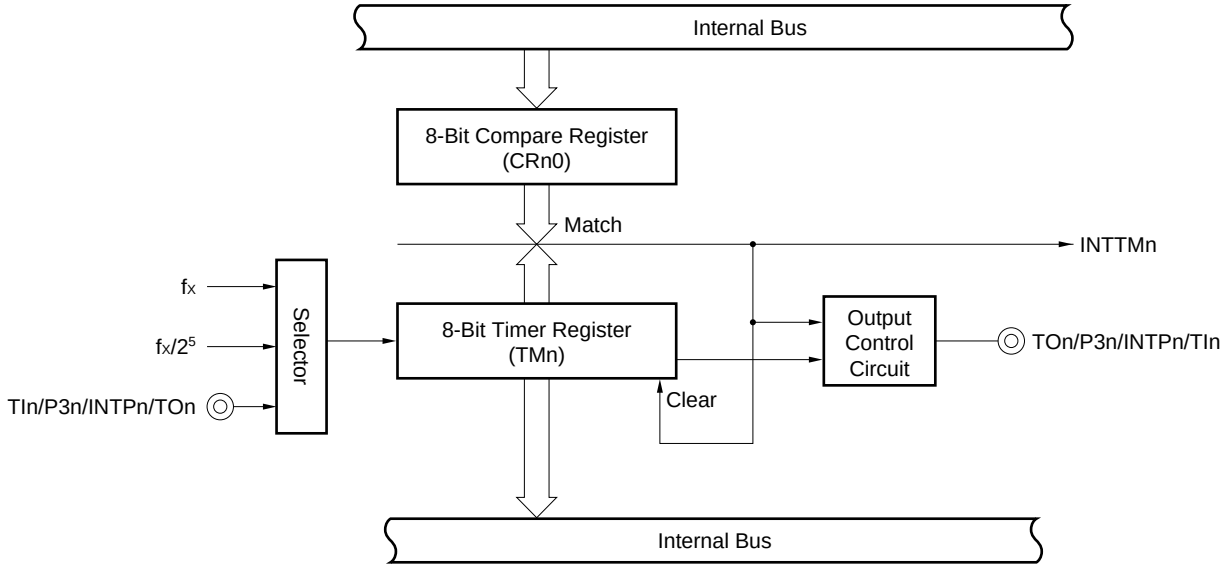
The μPD789011 and 789012 incorporate 3 channels of the timer.

- 8-bit timer/event counter : 2 channels
- Watchdog timer : 1 channel

Table 5-2. Operations of Timer

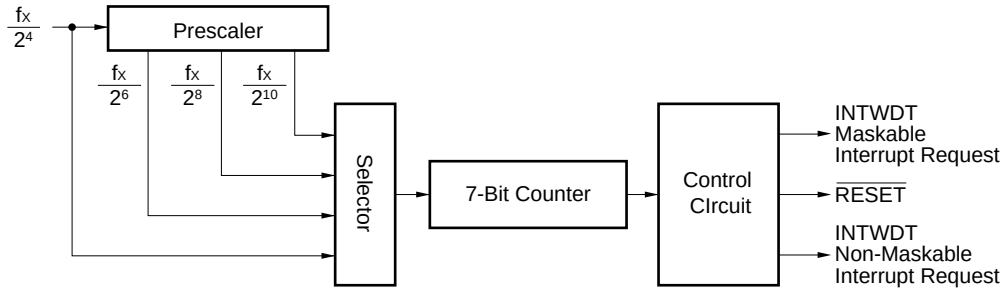
		8-bit Timer/Event Counter	Watchdog Timer
Operation mode	Interval timer	2 channels	1 channel
	External event counter	2 channels	—
Function	Timer output	2 outputs	—
	Interrupt request	2	1

Figure 5-2. 8-Bit Timer/Event Counter Block Diagram



Remark n = 0 or 1

Figure 5-3. Watchdog Timer Block Diagram



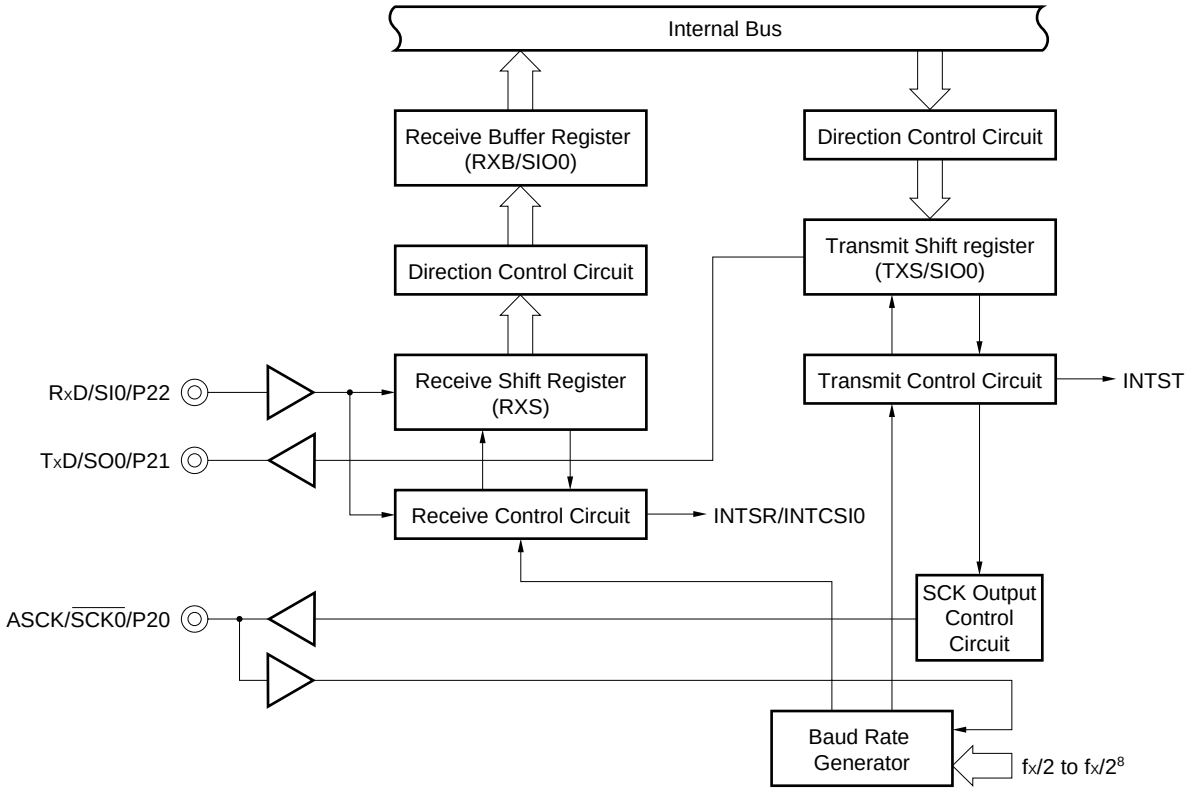
5.4 Serial Interface

1 channel of serial interface is incorporated.

Serial interface channel 0 has the following two modes.

- 3-wire serial I/O mode : MSB/LSB first switchable
- Asynchronous serial interface (UART) mode : Dedicated baud rate generator incorporated

Figure 5-4. Serial Interface Channel 0 Block Diagram



6. INTERRUPT FUNCTIONS

There are 10 interrupt functions of 2 different sources as follows.

- Non-maskable : 1
- Maskable : 9

Table 6-1. Interrupt Source List

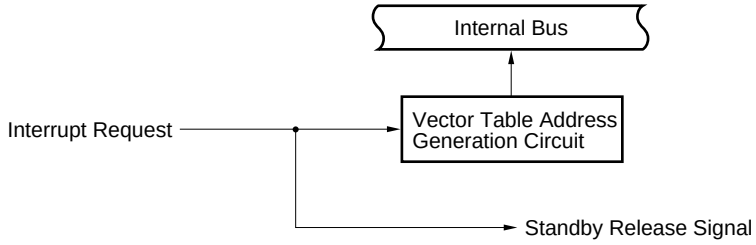
Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (when the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when the interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTSR	Completion of serial interface channel 0 UART reception	Internal	000CH	(B)
		INTCSI0	Completion of serial interface channel 0 3-wire transfer			
	5	INTST	Completion of serial interface channel 0 UART transmission		000EH	
	6	INTTM0	Generation of matching signal of 8-bit timer/ event counter 0		0010H	
	7	INTTM1	Generation of matching signal of 8-bit timer/ event counter 1		0012H	

Notes 1. The priority is the priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 7 the lowest.

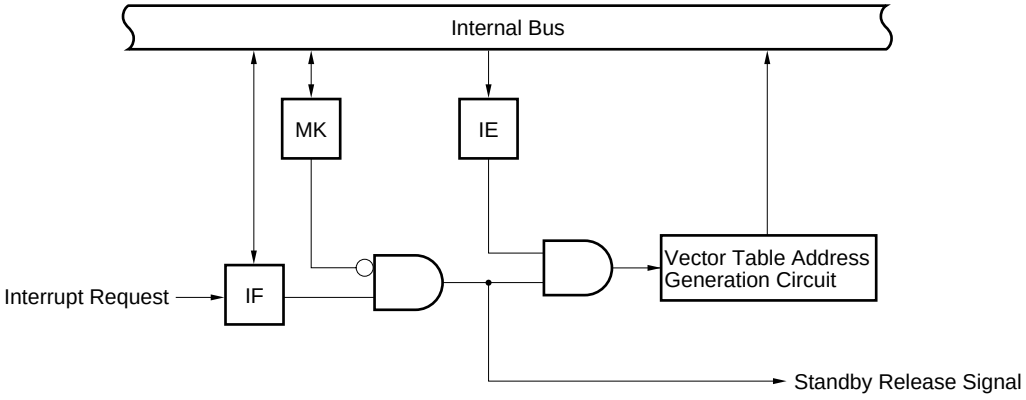
2. Basic configuration types (A) to (C) correspond to those in Figure 6-1, respectively.

Figure 6-1. Basic Configuration of Interrupt Functions

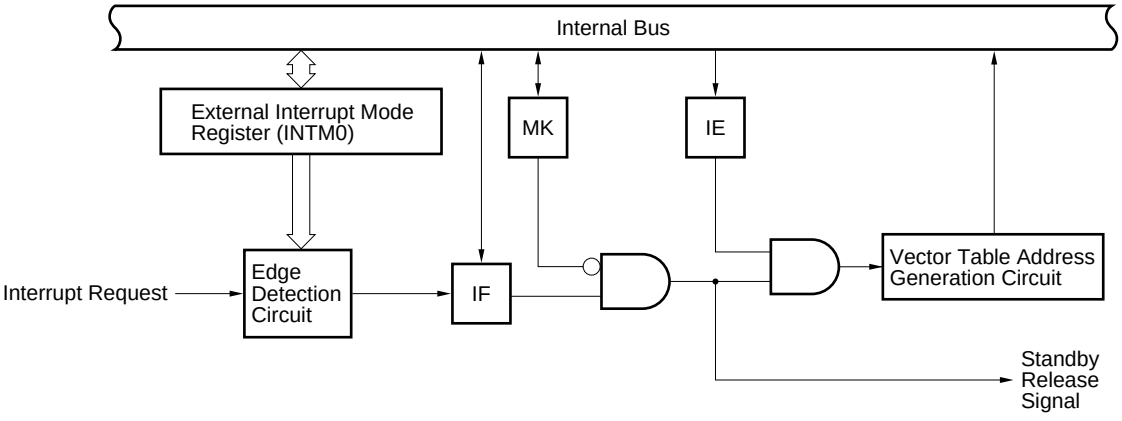
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



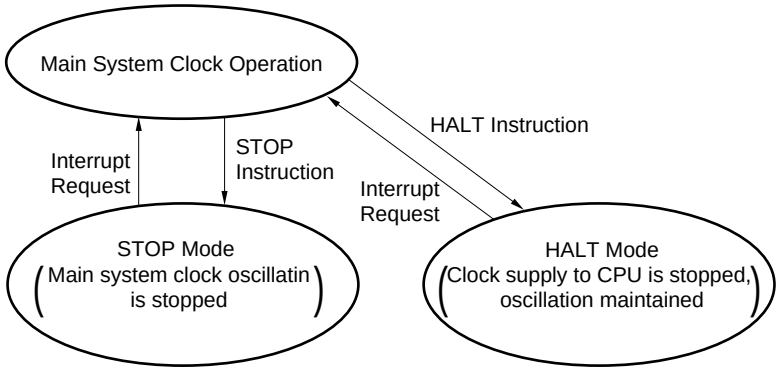
IF : Interrupt request flag
IE : Interrupt enable flag
MK : Interrupt mask flag

7. STANDBY FUNCTIONS

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operation clock is stopped.
  The average current consumption can be reduced by intermittent operation in combination with the normal operation mode.
- STOP mode: The main system clock oscillation is stopeed. All the operations performed on the main system clock is stopped, and power consumption becomes extremely small.

Figure 7-1. Standby Function



8. RESET FUNCTIONS

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

9. OVERVIEW OF THE INSTRUCTION SET

The instruction set of μPD789011 and 789012 is shown in the table below.

9.1 Legend

9.1.1 Operand identifiers and methods of use

Operands are described in “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and symbols, #, !, $, and [ ] are keywords and must be described as they are. Each symbol has the following meaning.

- # : Immediate data specification
- ! : Absolute address specification
- $: Relative address specification
- [ ] : Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, Be sure to describe the #, !, $, and [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 9-1. Operand Identifiers and Description Methods

Identifier	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special-function register symbol
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even addresses only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses in a 16-bit data transfer instructions)
addr5	0040H to 007FH Immediate data or labels (even addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

9.1.2 Description of “Operation” column

A	:	A register ; 8-bit accumulator
X	:	X register
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
AX	:	AX register pair; 16-bit accumulator
BC	:	BC register pair
DE	:	DE register pair
HL	:	HL register pair
PC	:	Program counter
SP	:	Stack pointer
PSW	:	Program status word
CY	:	Carry flag
AC	:	Auxiliary carry flag
Z	:	Zero flag
IE	:	Interrupt request enable flag
NMIS	:	Non-maskable interrupt servicing flag
( )	:	Memory contents indicated by the address or register contents in parentheses
X_H, X_L	:	High 8 bits and low 8 bits of a 16-bit register
∧	:	Logical product (AND)
∨	:	Logical sum (OR)
∀	:	Exclusive logical sum (exclusive OR)
$\overline{\quad}$	:	Inverted data
addr16	:	16-bit immediate data or label
jdisp8	:	signed 8-bit data (displacement value)

9.1.3 Description of “Flag Operation” column

(Blank)	:	Unchanged
0	:	Clear to 0.
1	:	Set to 1.
×	:	Set/cleared according to the result
R	:	Previously saved value is restored.

★ 9.2 Operation List

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z	Flags AC	Flags CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r **Note 1**	2	4	A ← r			
	r, A **Note 1**	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r **Note 2**	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp **Note 3**	1	4	AX ← rp			
	rp, AX **Note 3**	1	4	rp ← AX			
XCHW	AX, rp **Note 3**	1	8	AX ↔ rp			

Notes 1. Except r = A
2. Except r = A or X
3. Only when rp = BC, DE, or HL

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (add16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ∀ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∀ byte	×		
	A, r	2	4	A ← A ∀ r	×		
	A, saddr	2	4	A ← A ∀ (saddr)	×		
	A, !addr16	3	8	A ← A ∀ (addr16)	×		
	A, [HL]	1	6	A ← A ∀ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∀ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	$(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$			×
ROL	A, 1	1	2	$(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$			×
RORC	A, 1	1	2	$(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$			×
ROLC	A, 1	1	2	$(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$			×

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP–1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP – 2			
CALLT	[addr5]	1	8	(SP–1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP – 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp$_H$, (SP – 2) ← rp$_L$, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z	Flags AC	Flags CY
BC	$saddr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

★ 10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltages	V_{DD}			–0.3 to + 7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH} **Note**	1 pin	Peak value	–10	mA
			r.m.s.	–5	mA
		Total of all pins	Peak value	–30	mA
			r.m.s.	–15	mA
Output current, low	I_{OL} **Note**	1 pin	Peak value	30	mA
			r.m.s.	15	mA
		Total of all pins	Peak value	160	mA
			r.m.s.	80	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The r.m.s. should be calculated as follows : [r.m.s.] = [peak value] × $\sqrt{\text{duty}}$

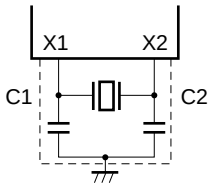
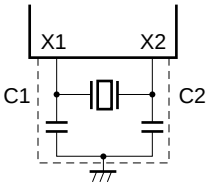
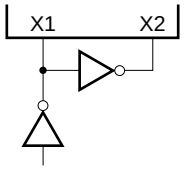
Caution Product quality may suffer if the absolute maximum rating is exceeded for even single parameter or even momentarily. That is, the absolute maximum ratings are the rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx)**Note 1**	V_{DD} = Oscillating voltage range	1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillating frequency (fx)**Note 1**		1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx)**Note 1**		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to AC characteristics for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the main system clock oscillator, wiring the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

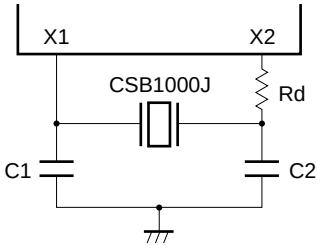
- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying higher current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

Recommended Oscillating Circuit Constants

Ceramic Resonator (T_A = –40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Oscillation Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSB1000J[Note]	1.00	100	100	1.9	5.5	Rd = 1.0 kΩ
	CSA2.00MG040	2.00	100	100	2.1	5.5	
	CST2.00MG040		–	–			Product containing capacitor
	CSA4.19MG	4.19	30	30	1.8	5.5	
	CST4.19MGW		–	–			Product containing capacitor
	CSA5.00MG	5.00	30	30	2.2	5.5	
	CST5.00MGW		–	–			Product containing capacitor
	CSA5.00MGU		30	30	2.0	5.5	
	CST5.00MGWU		–	–			Product containing capacitor

Note If the ceramic resonator is the CSB1000J (1.0 MHz) by Murata Mfg. Co., Ltd., the limiting resistor (Rd = 1.0 kΩ) is needed (see the following figure). If another recommended oscillator is used, the limiting resistor is not needed.



Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee the accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact manufacturer of the resonator being used.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	1 pin				15	mA
		Total of all of the pins				80	mA
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P20 to P22, P30 to P32	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.9 V_{DD}		V_{DD}	V
	V_{IH2}	INTP0 to INTP2, SI0, RxD, ASCK, $\overline{SCK0}$, TI0, TI1, $\overline{RESET}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.9 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P20 to P22, P30 to P32	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL2}	INTP0 to INTP2, SI0, RxD, ASCK, $\overline{SCK0}$, TI0, TI1, $\overline{RESET}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA				1.0	V
		I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1 and X2			3	μA
	I_{LIH2}		X1, X2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Pins other than X1 and X2			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA

Remark The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Software pull-up resistor	R	V_{IN} = 0 V		50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	5.0 MHz Crystal oscillation operation	V_{DD} = 5.0 V ±10%[Note 2]		1.1	2.0	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.3	0.45	mA
	I_{DD2}	5.0 MHz Crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 2]		0.6	0.85	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.2	0.35	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5	μA
			T_A = 25°C		0.05	3	
			V_{DD} = 2.0 V ±10%		0.05	3	μA

Notes 1. This does not include the port current (containing the current flowing through the on-chip pull-up resistor).

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when PCC is set to 02H)

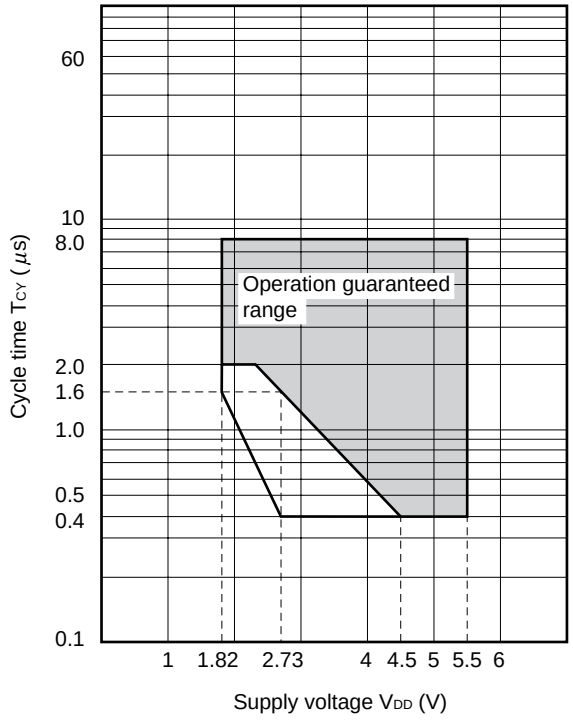
Remark The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	V_{DD} = 2.7 to 5.5 V		0.4		8	μs
				1.6		8	μs
TI0, TI1 inputs High/low level widths	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
Interrupt request input High/low level widths	t_{INTH}, t_{INTL}	INTP0 to INTP2	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ Low level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

T_{CY} vs V_{DD} (Main System Clock)



Remark The shaded area indicates the operation guaranteed range of the μPD78P9014.

(2) Serial interface channel 0 (T_A = –40 to +85°, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{SCK0}$: internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low level widths	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2 - 50$			ns
				$t_{KCY1}/2 - 150$			ns
SI0 setup time (on $\overline{SCK0}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI0 hold time (on $\overline{SCK0}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK0}$ ↓ → SO0 Output delay time	t_{KSO1}	R = 1k Ω, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$: external clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low level widths	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI0 setup time (on $\overline{SCK0}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI0 hold time (on $\overline{SCK0}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK0}$ ↓ → SO0 Output delay time	t_{KSO2}	R = 1k Ω, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line.

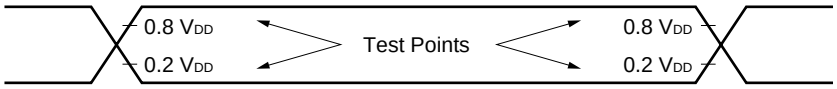
(iii) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

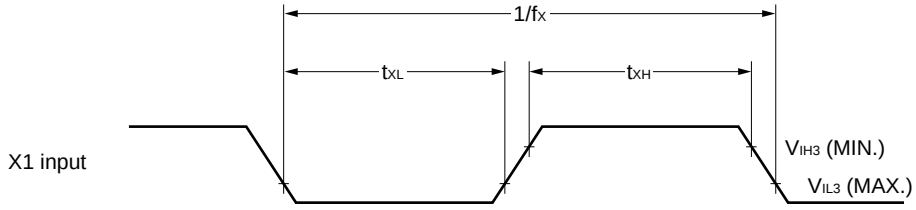
(iv) UART mode (external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
			3200			ns
ASCK high and low level widths	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK rise and fall times	t_R, t_F				1	μs

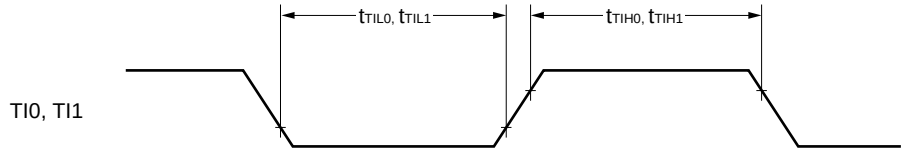
AC Timing Test Points (Except for X1 input)



Clock Timing

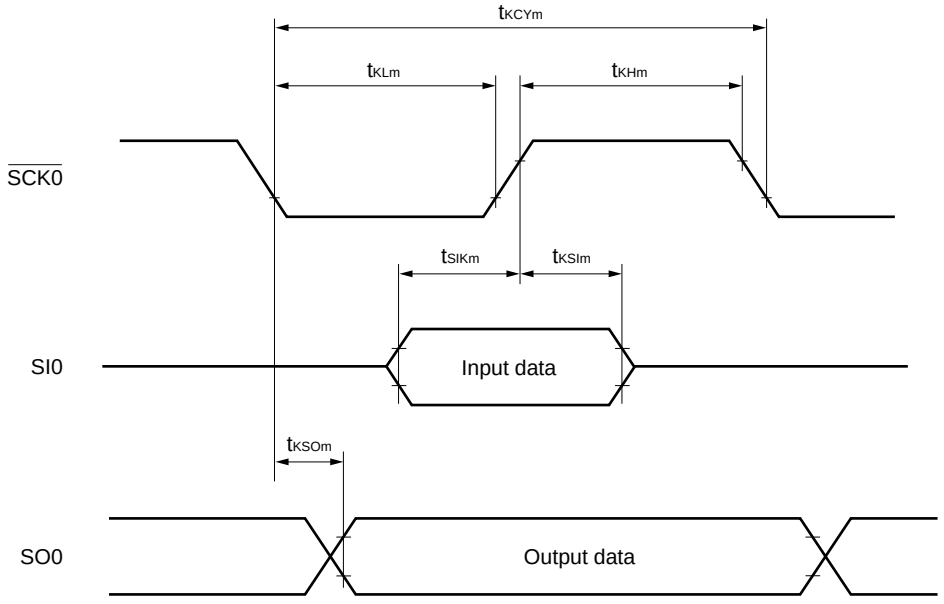


TI Timing

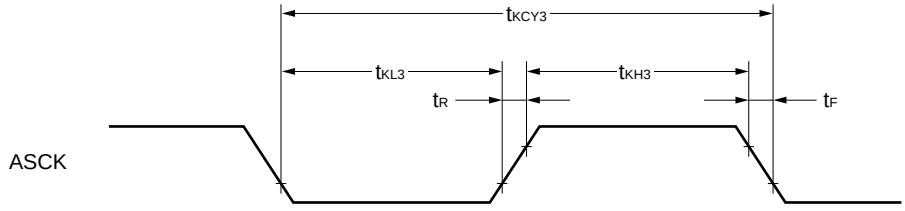


Serial Transfer Timing

3-Wire serial I/O mode:



UART mode (external clock input):



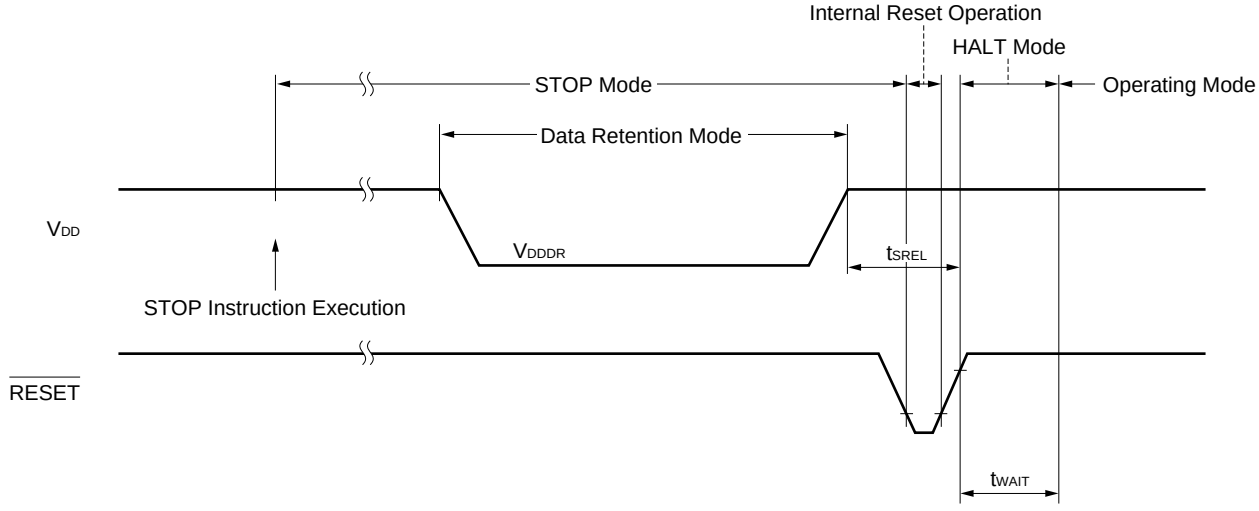
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	v
Release signal set time	t_{SREL}		0		0	μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note**		ms

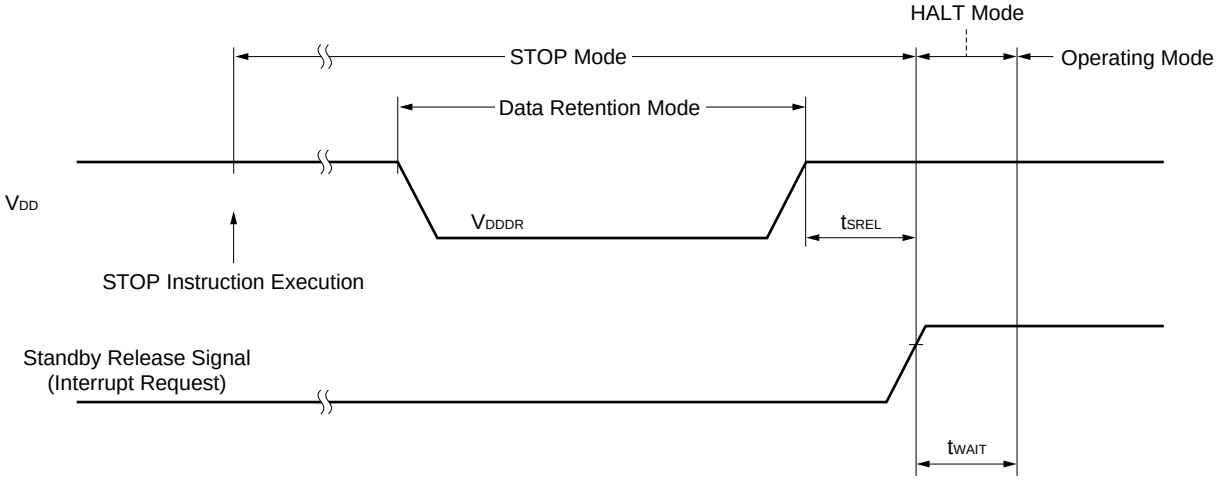
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible.

Remark f_X: Main system clock oscillation frequency

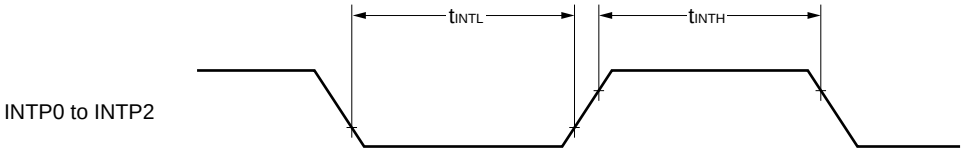
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



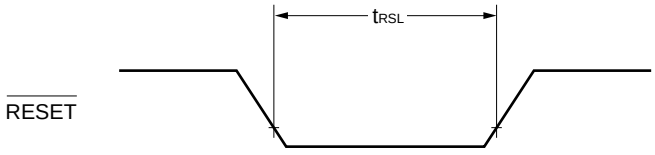
Data Retention Timing (Standby Release Signal: STOP Release by Interrupt Request Signal)



Interrupt Request Input Timing

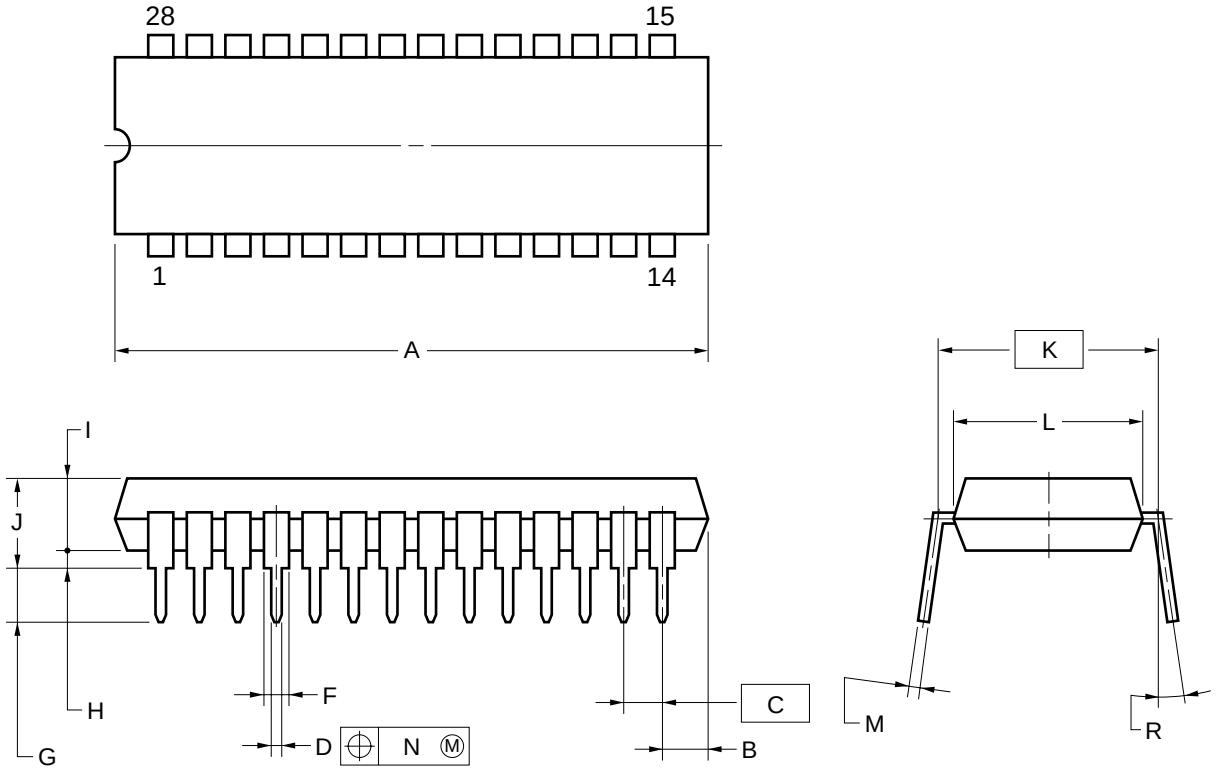


$\overline{\text{RESET}}$ Input Timing



11. PACKAGE DRAWINGS

28PIN PLASTIC SHRINK DIP (400 mil)



NOTES

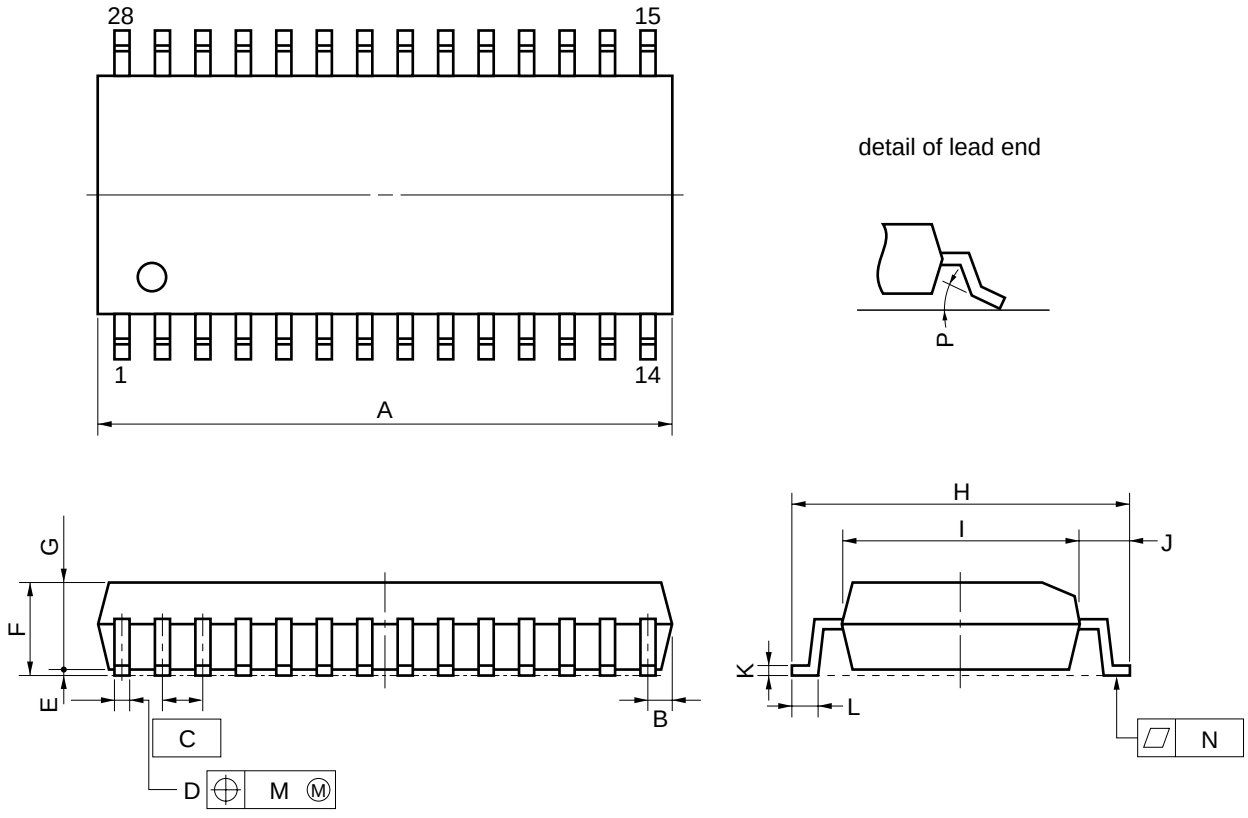
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P28C-70-400A-1

28 PIN PLASTIC SOP (375 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.15	0.006
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P28GM-50-375B-3

★ 12. RECOMMENDED SOLDERING CONDITIONS

The μPD789011 and 789012 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual** (C10535E).

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 12-1. Soldering Conditions for Surface-mount Devices

μPD789011GT-×××: 28-pin Plastic SOP (375 mil)
μPD789012GT-×××: 28-pin Plastic SOP (375 mil)

Soldering Method	Soldering Conditions	Recommended Condition Code
Infrared reflow	Package peak temperature: 235°C, Duration: 30 seconds max. (at 210°C or above) Number of times: two times max.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 seconds max. (at 200°C or above) Number of times: two times max.	VP15-00-2
Wave soldering	Soldering bath temperature: 260°C max., Duration: 10 seconds max., Number of times: Once Preheating temperature: 120°C max.(Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Duration: 3 seconds max. (per device side)	—

Note The storage conditions are 25°C and 65% RH for the number of storage days after opening the seal of the dry pack.

Caution Using more than one soldering method should be avoided. (except in the case of partial heating)

Table 12-2. Soldering Conditions for Through-hole Devices

μPD789011CT-×××: 28-pin Plastic Shrink DIP (400 mil)
μPD789012CT-×××: 28-pin Plastic Shrink DIP (400 mil)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260 °C max., Duration: 10 seconds max.
Partial heating	Pin temperature: 300 °C max., Duration: 3 seconds max.(per pin)

Caution Wave soldering is only for the lead part in order that jet solder cannot contact with the chip directly.

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the μPD789011 and 789012.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	78K/0S Series common assembler package
CC78K0S[Notes 1, 2, 3]	78K/0S Series common C compiler package
DF789014[Notes 1, 2, 3]	μPD789014 Subseries common device file
CC78K0S-L[Notes 1, 2, 3, 5]	78K/0S Series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P9014GT	PROM programmer adapter connected to PG-1500
PG-1500 controller	PG-1500 control program

Debugging Tools

IE-78K0S-NS[Note 5]	In-circuit emulator common to 78K/0S Series
IE-70000-98-IF-B[Note 5]	Interface adapter when PC-9800 Series (except for notebooks) is used as host machine of IE-78K0S-NS.
IE-70000-98N-IF[Note 5]	Interface adapter and cable when PC-9800 Series notebook is used as host machine of IE-78K0S-NS.
IE-70000-PC-IF-B[Note 5]	Interface adapter when IBM PC/AT™ or its compatibles is used as host machine of IE-78K0S-NS.
IE-789014-NS-EM1[Note 5]	Emulation board for μPD789014 Subseries
NP-28CT[Note 4]	Emulation probe for 28-pin plastic shrink DIP
NP-28GT[Note 4]	Emulation probe for 28-pin plastic SOP
SM78K0S[Notes 1, 2, 3]	System simulator common to 78K/0S Series
DF789014[Notes 1, 2, 3]	Device file in common with μPD7890914 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	78K/0S Series OS

Notes 1. PC-9800 Series (MS-DOS™ + Windows™) based
2. IBM PC/AT and compatibles (PC DOS™/IBM DOS™/MS-DOS + Windows) based
3. HP9000 Series 700™ (HP-UX™) based, SPARCstation™ (SunOS™) based, NEWS™ (NEWS-OS™) based
4. This is a product of Naito Densei Machida Seisakusho Co., Ltd. (044-822-3813). To purchase, contact Naito Densei Machida Seisakusho Co., Ltd.
5. Under development

Remark RA78K0S, CC78K0S, and SM78K0S are used with DF789014.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Device

Document Name	Document No.	
	English	Japanese
μPD78P9014 Data Sheet	U10912E	U10912J
μPD789011, 789012 Data Sheet	This document	U11095J
μPD789014 Subseries User's Manual	U11187E	U11187J
78K/0S Series User's Manual — Instruction	U11047E	U11047J
78K/0S Series Instruction Summary Sheet	—	To be prepared
78K/0S Series Instruction Set	—	To be prepared

Development Tool Documents (User's Manual)

Document Name		Document No.	
		English	Japanese
RA78K0S Assembler Package	Operation	U11622E	U11622J
	Assembly language	U11599E	U11599J
	Structured Assembly Language	U11623E	U11623J
CC78K/0S C Compiler	Operation	U11816E	U11816J
	Language	U11817E	U11817J
SM78K0S System Simulator Windows based	Reference	U11489E	U11489J
SM78K Series System Simulator	External Components User-open Interface Specification	U10092E	U10092J
PG-1500		U11940E	U11940J

Documents Related to Embedded Software (User's Manual)

Document Name	Document No.	
	English	Japanese
78K/0S Series OS MX78K0S	To be prepared	To be prepared

Other Related Documents

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	C11893J
Microcontroller Related Product Guide — Third Party	—	C11416J

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing, etc.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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800-729-9288

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