DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
V850E/PHO3

V850E/PHO3
32-Bit Single-Chip Microcontroller

DESCRIPTION

The V850E/PHO3 single-chip microcontroller devices make the performance gains attainable with 32-bit RISC-based controllers available for embedded control applications. The V850E/PHO3 devices provide an excellent combination of general purpose peripheral functions like serial communication interfaces, timers/counters,measurement and control functions, with dedicated motor control timers and full CAN network support. The integrated FlexRay™ interface implements the FlexRay™ network protocol. Thus equipped, the V850E/PHO3 product is ideally suited for automotive control and electric power steering (EPS) applications. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

FEATURE

- 32-bit RISC CPU with Harvard Architecture
- Internal flash memory: 992 KB
- Internal RAM: 60 KB
- Data Flash: 32 KB
- Operating Clocks
  CPU Frequency: 80 / 128MHz with PLL factor 5 / 8
  MainOsc: operates on 16MHz crystal
  PLL ratio: factor 5
  FlexRay™: 80MHz
- I/O lines: 143 + 5 input only
- Timers
  10 ch 16-bit general purpose timer/counter
  2 ch 16-bit timer/counter with Motor Control
  2 ch 16-bit general purpose timer/counter with PWM function
- A/D Converter: 2 x 10 channels
  10 bit resolution
- FlexRay Interface: 1 (2 channels) (protocol specification v2.1)
- CAN Interface: 2 channel (AFCAN)
- Serial Interfaces: 7 channels
  - clocked serial: 2 channels (CSIB)
  - clocked serial: 2 channels (CSIE)
  - UARTC: 3 channels
- DMA: 8 channels
- Random Number Generator
- Aux. Frequency Output
- Clock Monitor
- Power Save Mode: HALT
- On Chip Debug: N-Wire and Non Break Debug interface
- Power supply: 3.3V +/- 0.3V and 1.5V+/-10% (refer to related chapter)
- Temperature range:
  Package: -40°C to +125°C
  Bare Die: -40°C to +150°C
- Package: 357 pin FPBGA, 0.8 mm ball-pitch (20 × 20 mm)

ORDERING INFORMATION

Product Name	Product Family	Package	Flash	RAM
μPD70F3483F1(A2)-JA1	V850E/PHO3	FPBGA 20 × 20 mm	768 KB	60 KB
μPD70F3483W-CAR	V850E/PHO3	Bare Die	768 KB	60 KB
μPD70F3441F1(A2)-JA1	V850E/PHO3	FPBGA 20 × 20 mm	992 KB	60 KB
μPD70F3441W-CAR	V850E/PHO3	Bare Die	992 KB	60 KB

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1. Electrical Target Specification

1.1 Absolute Maximum Ratings

T_a = 25°C, V_{SS15x} = CV_{SS15} = V_{SS3x} = $AV_{SS0,1}$ = 0V

Table 1-1: Absolute Maximum Ratings

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD15x}			-0.5 to +2.0	V
	CV_{DD15}			-0.5 to +2.0	V
	V_{DD3x}			-0.5 to +4.6	V
	AV_{DD}			-0.5 to +4.6	V
Input voltage	V_I	The pin X1 is excluded.		-0.5 to V_{DD3}+0.3 (Note 1)	V
Analog input voltage	V_{IN}	ANI00 to ANI09 ANI10 to ANI19		-0.3 to AV_{DD}+0.3 (Note 1)	V
A/D Converter	$AV_{REF0,1}$			-0.3 to AV_{DD}+0.3 (Note 1)	V
High level output current	I_{OH}	For 1 pin	1 pin	-4.0	mA
		Total of all pins (Note 2)	Total	-100.0	mA
Low level output current	I_{OL}	For 1 pin	1 pin	4.0	mA
		Total of all pins (Note 2)	Total	100.0	mA
Operating ambient temperature	T_a	Normal operating mode (Package)		-40 to +125	°C
		NBD Operation		-40 to + 80	°C
		Flash programming mode, when flash memory is written. (Package)		-40 to +125	°C
Operating junction temperature	T_j	Normal operating mode (Bare Die)		-40 to +150	°C
		Flash programming mode, when flash memory is written. (Bare Die)		-40 to +150	°C
Storage temperature	T_{stg}	In tray.		-65 to +125	°C
		Off tray, mounted but not powered.		-65 to + 150	°C

Notes: 1. Please do not exceed absolute maximum rating (max. +4.6V) of each power supply voltage.
2. Total sum of all input and output currents of all pins.

Cautions: 1. Cautions: 1. Do not directly connect output (or I/O) pins of IC products to each other, or to VDD, VSS, and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

1.2 Capacitance

T_a = 25°C
$V_{DD15} = CV_{DD15} = V_{DD3x} = AV_{DD} = V_{SS15x} = CV_{SS15} = V_{SS3x} = AV_{SS0,1}$ = 0V

Table 1-2: Pin Leak Current

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc=1MHz			15	pF
Input/output capacitance	C_{IO}	All pins are at 0V excluding the pin that is measured.			15	pF
Output capacitance	C_O				15	pF

1.3 Operation Conditions

Table 1-3: Operating Conditions

Internal system clock frequency	Operating Temperature (Topt)		Power Supply Voltage
80MHZ, 128MHz	T_a = -40 to +125°C	Normal operating mode (Package)	VDD15x=CVDD15=1.5V±0.15V VDD3x=3.3V±0.3V
	T_j = -40 to +150°C	Normal operating mode (Bare Die)	

1.4 Oscillator Characteristics

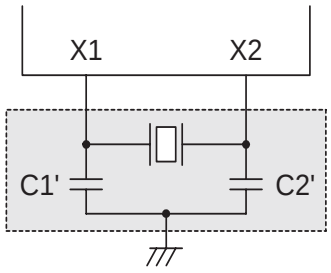


Figure 1-1: Oscillator Recommendations

Remark: Values of capacitors C1' and C2' depend on used crystal and must be specified in cooperation with the crystal manufacturer.

Cautions: 1. External clock input is prohibited.
2. Wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.
• Place the oscillation circuit as close as possible to X1 and X2 pins.
• Keep the wiring length as short as possible.
• Do not cross the wiring with the other signal lines.

• Do not route the wiring near a signal line through which a high fluctuating current flows.
• Always make the ground point of the oscillator capacitor the same potential as CV_{SS15}.
• Do not ground the capacitor to a ground pattern through which a high current flows.
• Do not fetch signals from the oscillator.

Table 1-4: Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	fosc			16		MHz
Oscillation stabilization time	t_{OST}	The oscillation stabilization time depends on the crystal and circuit and must be specified in cooperation with the crystal manufacturer. Ensure that all conditions and tolerances of all components are considered for determination of oscillation stabilization time: Resistance value Capacity value Voltage Temperature Manufacturing range	n/a	n/a	n/a	
PLL lockup time	PSTC	Internal digital counter, counting with fosc (fx=fosc) frequency.		2^{14}/fx		s

1.5 DC Characteristics

1.5.1 Input/Output Level

T_a= -40 to +125°C
T_j = -40 to +150°C
VDD15x = CVDD15 = 1.5V +/-10%,
VDD3x = 3.3V +/- 0.3V,
VSS15x = CVSS15 = VSS3x = 0V

Table 1-5: Input/Output Level (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	PAL,PAH,PDL,PDH,PCD,PCS, PCM,MODE1,DDI,DMS,DCK	$0.7V_{DD3}$		V_{DD3}+0.3	V
		P0,P1,P2,P3,P4,P5,P6,P7,P8, P9,P10,P11, ADn_DBG,MODE3, FRXDA,FRXDB, SYNC,CLK_DBG	$0.7V_{DD3}$		V_{DD3}+0.3	V
		_DRST, MODE_DBG	$0.75V_{DD3}$		V_{DD3}+0.3	V
		MODE0,MODE2, _RESET	$0.8V_{DD3}$		V_{DD3}+0.3	V

Table 1-5: Input/Output Level (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL}	PAL,PAH,PDL,PDH,PCD,PCS, PCM,MODE1,DDI,DMS,DCK	-0.5		$0.3V_{DD3}$	V
		P0,P1,P2,P3,P4,P5,P6,P7,P8, P9,P10,P11, ADn_DBG,MODE3, FRXDA,FRXDB, SYNC,CLK_DBG	-0.5		$0.3V_{DD3}$	V
		_DRST, MODE_DBG	-0.5		$0.3V_{DD3}$	V
		MODE0,MODE2, _RESET	-0.5		$0.2V_{DD3}$	V
Output voltage, high	V_{OH}	I_{OH}=-2.5 mA (Note 2)	V_{DD3}-1.0			V
		I_{OH}=-0.1 mA	V_{DD3}-0.4			V
Output voltage, low	V_{OL}	I_{OL}=2.5mA (Note 2)			0.8	V
		I_{OL}=0.1mA			0.4	V
Build in pull down resistor	R_L	Note 1	10	50	120	KΩ

Notes: 1. _DRST, MODE_DBG
2. Max +/-2.5 mA x 20 of output current simultaneously.
Only the output port pins and the FlexRay outputs have to be considered.
(The output pins of the debugger (NBD/DCU) are excluded).

1.5.2 Pin Leak Current

T_a= -40 to +125°C
T_j = -40 to +150°C
V_{DD15x} = CV_{DD15} = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
V_{SS15x} = CV_{SS15} = V_{SS3x} = 0V

Table 1-6: Pin Leak Current

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH}	V_I=V_{DD3x}	All pins except for the below mentioned			10.0	µA
		V_I=AV_{DD}	ANI00 to ANI09, ANI10 to ANI19			3.0	µA
Input leakage current, low	I_{LIL}	V_I = 0V	All pins except for the below mentioned			-10.0	µA
		V_I = 0V	ANI00 to ANI09, ANI10 to ANI19			-3.0	µA
Output leakage current, high	I_{LOH}	V_O = V_{DD3x}	All pins			10.0	µA
Output leakage current, low	I_{LOL}	V_O = 0V	All pins			-10.0	µA

1.5.3 Operation and HALT Mode Supply Current

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V

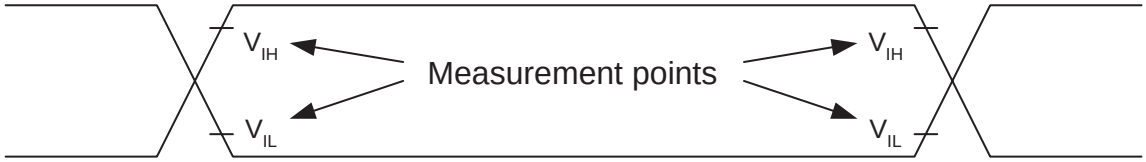
Table 1-7: Power Supply Current

Parameter	Conditions		Symbol	MIN.	TYP. (Note 2)	MAX.	Unit
Supply current (Note 1)	Normal Operation mode	V_{DD15x}, CV_{DD15} fXX = 128MHz	I_{DD15}		220	430	mA
		V_{DD15x}, CV_{DD15} fXX = 80MHz	I_{DD15}		195	400	mA
		V_{DD3x}	I_{DD3}		35	100	mA
	Flash programming mode	V_{DD15x}, CV_{DD15} fXX = 128MHz	I_{DDF15}		230	450	mA
		V_{DD15x}, CV_{DD15} fXX = 80MHz	I_{DDF15}		205	420	mA
		V_{DD3x}	I_{DDF3}		60	100	mA
	Halt mode	V_{DD15x}, CV_{DD15} fXX = 128MHz	I_{DDH15}		200	390	mA
		V_{DD15x}, CV_{DD15} fXX = 80MHz	I_{DDH15}		180	365	mA

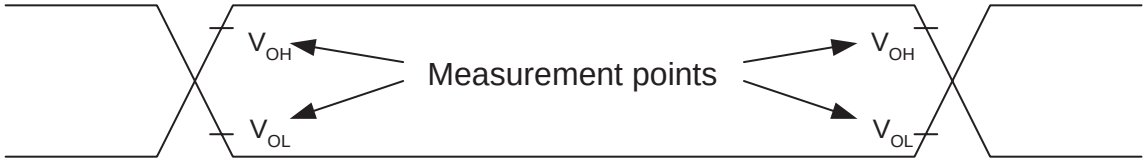
Notes: 1. The port output current resulting from built-in pull-up or pull-down resistances is not included.
2. The typical value refers to Ta = 25°C, VDD15x = 1.5V and VDD3x = 3.3V

1.6 AC Characteristics

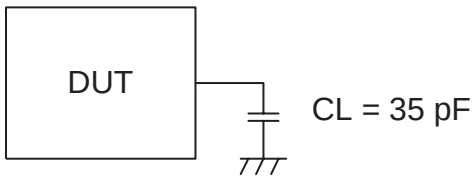
AC Test Input Measurement Points,



AC Test Output Measurement Points



Load Conditions



Caution: If the load capacitance exceeds 35 pF due to the circuit configuration, bring the load capacitance of the device to 35 pF or less by inserting a buffer or by some other means.

1.6.1 Power Supply Turning On / Interception Timing

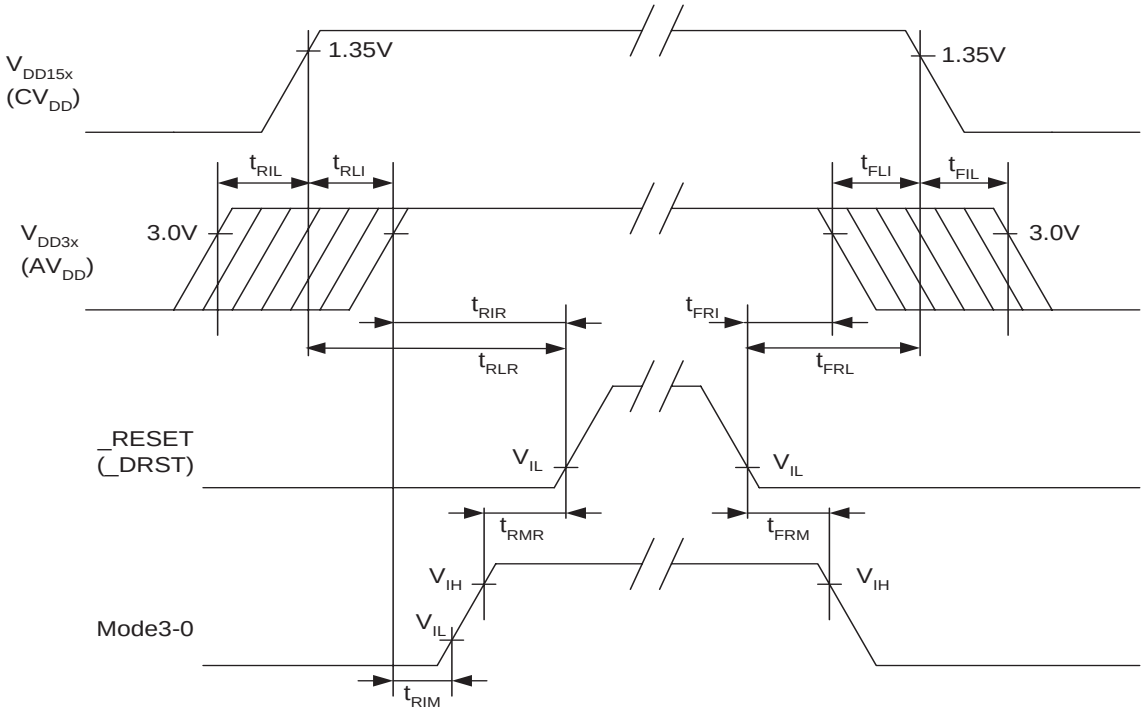
T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V

Table 1-8: Turning On / Interception Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
V_{DD15x} to V_{DD3x}	t_{RLI}		0	1	s
V_{DD3x} to V_{DD15x}	t_{RIL}		0	1	s
V_{DD15x} to $\overline{RESET}$	t_{RLR}		0.5+t_{OSC}[a]		ms
V_{DD3x} to $\overline{RESET}$	t_{RIR}		0.5+t_{OSC}[b]		ms
V_{DD3x} to MODE3-0	t_{RIM}		0.2		ms
MODE3-0 to $\overline{RESET}$	t_{RMR}		0		ns
$\overline{RESET}$ to MODE3-0	t_{FRM}		0		ns
$\overline{RESET}$ to V_{DD3x}	t_{FRI}		500		ns
$\overline{RESET}$ to V_{DD15x}	t_{FRL}		500		ns
V_{DD3x} to V_{DD15x}	t_{FLI}		0	1	s
V_{DD15x} to V_{DD3x}	t_{FIL}		0	1	s

a. t_{OSC} depends on the external oscillator's stabilization time, crystal type and circuit and should be specified / evaluated in cooperation with the oscillator manufacturer.
b. t_{OSC} depends on the external oscillator's stabilization time, crystal type and circuit and should be specified / evaluated in cooperation with the oscillator manufacturer.

Figure 1-2: Turning On / Interception Timing



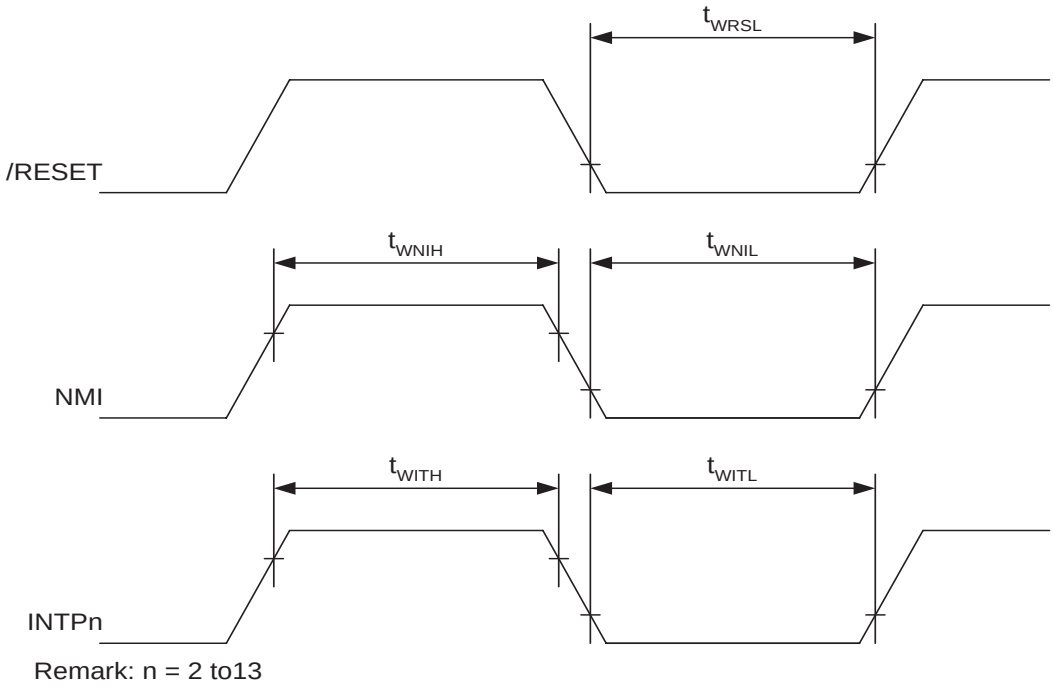
1.6.2 *Reset And Interrupt Timing*

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V

Table 1-9: Reset And Interrupt Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}	except for power on	500		ns
NMI input low level width	t_{WNIL}	(analog filter)	500		ns
NMI input high level width	t_{WNIH}	(analog filter)	500		ns
INTPn input low level width	t_{WITL}	n=0,1 (analog filter)	500		ns
		n=2...13 (digital filter)	Sampling clock × 5T		ns
INTPn input high level width	t_{WITH}	n=0,1 (analog filter)	500		ns
		n=2...13 (digital filter)	Sampling clock × 5T		ns

Figure 1-3: Reset And Interrupt Timing



Remark: n = 2 to13

1.6.3 External Asynchronous Memory Access Read Timing

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V

Table 1-10: External Asynchronous Memory Access Read Timing

Parameter		Symbol	MIN.	MAX.	Unit
Data input set up time (vs. address)	<10>	t_{SAID}		$(2 + w_{AS} + w_{AH} + w_D + w)$ T - 19	ns
Data input set up time (vs. $\overline{CSn}$, $\overline{BEN0\text{-}3}$)	<10>	t_{SAID}		$(2 + w_{AS} + w_{AH} + w_D + w)$ T - 19	ns
Data input set up time (vs. $\overline{RD}\downarrow$)	<11>	t_{SRDID}		$(1.5 + w_D + w)$ T - 19	ns
$\overline{RD}$ Low level width	<12>	t_{WRDL}	$(1.5 + w_D + w)$ T - 6		ns
$\overline{RD}$ High level width	<13>	t_{WRDH}	$(0.5 + w_{AS} + i)$ T - 6		ns
Address, $\overline{CSn}$, $\overline{BEN0\text{-}3}$ $\rightarrow$ $\overline{RD}\downarrow$ delay time	<14>	t_{DARD}	$(0.5 + w_{AS})$ T - 8.2		ns
$\overline{RD}\uparrow \rightarrow$ address delay time	<15>	t_{DRDA}	i*T		ns
$\overline{RD}\uparrow \rightarrow \overline{CSn}$ delay time	<15'>	t_{DRDCS}	0		ns
$\overline{RD}\uparrow \rightarrow \overline{BEN0\text{-}3}$ delay time	<15">	t_{DRDBEN}	0		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	t_{HRDID}	0		ns
$\overline{RD}\uparrow \rightarrow$ data output delay time	<17>	t_{DRDOD}	$(1 + i + w_{AS} + w_{AH})$ T - 8		ns
$\overline{WAIT}$ set up time (vs. address, $\overline{CSn}$, $\overline{BEN0\text{-}3}$)	< 31 >	t_{SAW}		$(1 + w_D + w + w_{AS} + w_{AH})$ T - 19	ns
$\overline{WAIT}$ hold time (vs. address, $\overline{CSn}$, $\overline{BEN0\text{-}3}$)	<32>	t_{WWH}	$(1 + w_D + w + w_{AS} + w_{AH})$ T - 3		ns

Remarks: **1.** T: $1/f_{XX}$

2. i: Number of idle states specified by BCC register

3. w_{AS}: Number of waits specified by AWC register
w_{AH}: Number of waits specified by AWC register

4. w_D: Number of waits specified by DWC0, DWC1 register; $w_D \geq 1$

5. w: Number of waits due to external wait signal ($\overline{WAIT}$)

6. n = 0, 2, 3, 4

Figure 1-4: External Asynchronous Memory Access Read Timing

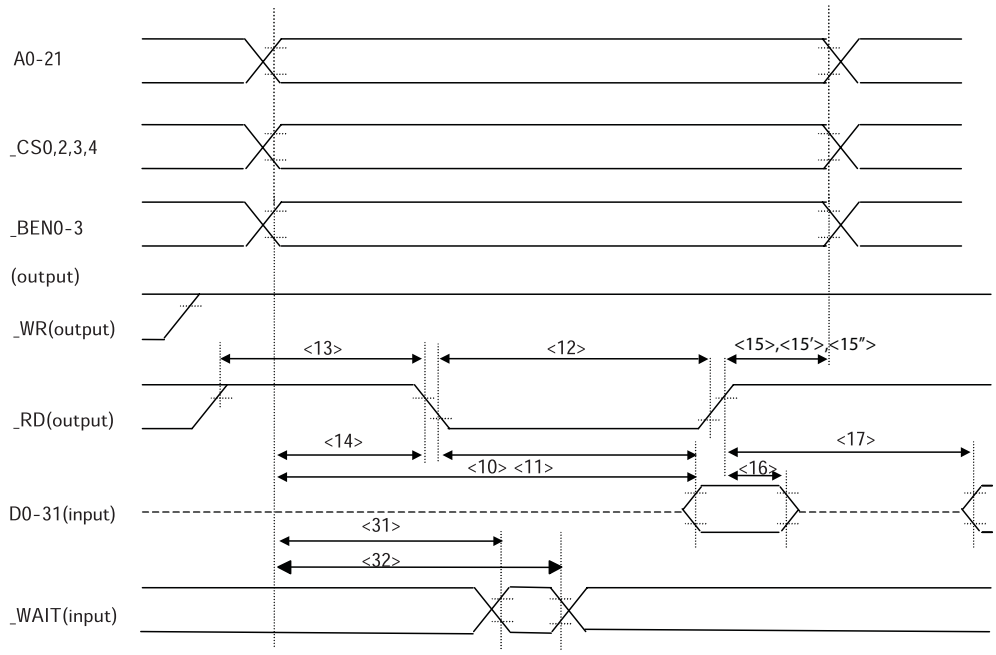
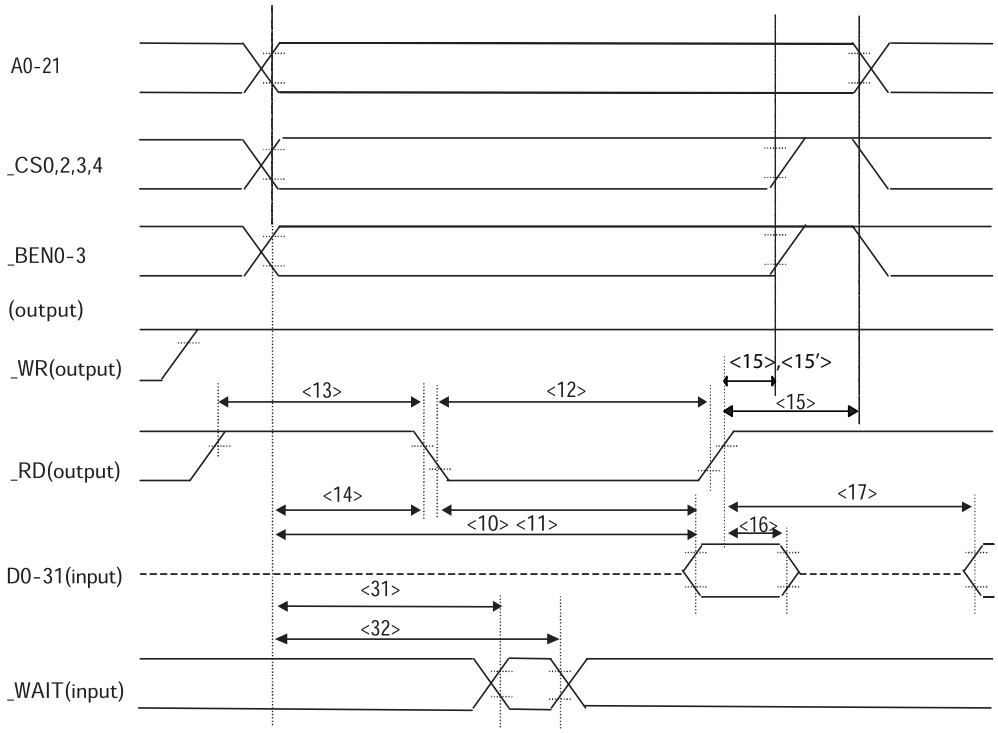


Figure 1-5: External Asynchronous Memory Access Read Timing With Idle Cycle



1.6.4 External Asynchronous Memory Access Write Timing

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V

Table 1-11: External Asynchronous Memory Access Write Timing

Parameter		Symbol	MIN.	MAX.	Unit
Address, $\overline{CSn}$, $\overline{BEN0\text{-}3}$ → $\overline{WR}$ ↓ delay time	<20>	T_{DAWR}	$(1 + w_{AS} + w_{AH})T - 5$		ns
$\overline{WR}$↓ bus output delay time	<33>	T_{DWROD1}	0		ns
$\overline{WR}$↓data output delay time	<34>	T_{DWROD2}		5	ns
$\overline{WR}$↑ data float delay time	<35>	T_{FWROD}		0.5T+3	ns
Address, $\overline{CSn}$, $\overline{BEN0\text{-}3}$ set up (vs. $\overline{WR}$↑)	<21>	T_{SAWR}	$(1.5 + w_{AS} + w_{AH} + w_D + w)$ T - 7		ns
$\overline{WR}$↑ → address delay time	<22>	T_{DWRA}	(0.5 + i) T - 3		ns
$\overline{WR}$↑ → $\overline{CSn}$ delay time	<22'>	T_{DWRCS}	0.5 T - 3		ns
$\overline{WR}$↑ → $\overline{BEN0\text{-}3}$ delay time	<22">	T_{DWRBEN}	0.5 T - 3		ns
$\overline{WR}$ High level width	<23>	T_{WWRH}	$(1.5 + i + w_{AS} + w_{AH})$ T - 6		ns
$\overline{WR}$ Low level width	<24>	T_{WWRL}	$(0.5 + w + w_D)$ T - 6		ns
Data output set up time (vs. $\overline{WR}$↑)	<25>	T_{SODWR}	$(0.5 + w_D + w)$ T -5		ns
Data output hold time (vs. $\overline{WR}$↑)	<26>	T_{HWROD}	0.5 T - 6		ns
$\overline{WAIT}$ set up time (vs. address, $\overline{CSn}$, $\overline{BEN0\text{-}3}$)	<31>	T_{SAW}		$(1 + w_D + w + w_{AS} + w_{AH})$T - 19	ns
$\overline{WAIT}$ hold time (vs. address, $\overline{CSn}$, $\overline{BEN0\text{-}3}$)	<32>	T_{WWH}	$(1 + w_D + w + w_{AS} + w_{AH})$T - 3		ns

Remarks: **1.** T: $1/f_{XX}$

2. i: Number of idle states specified by BCC register

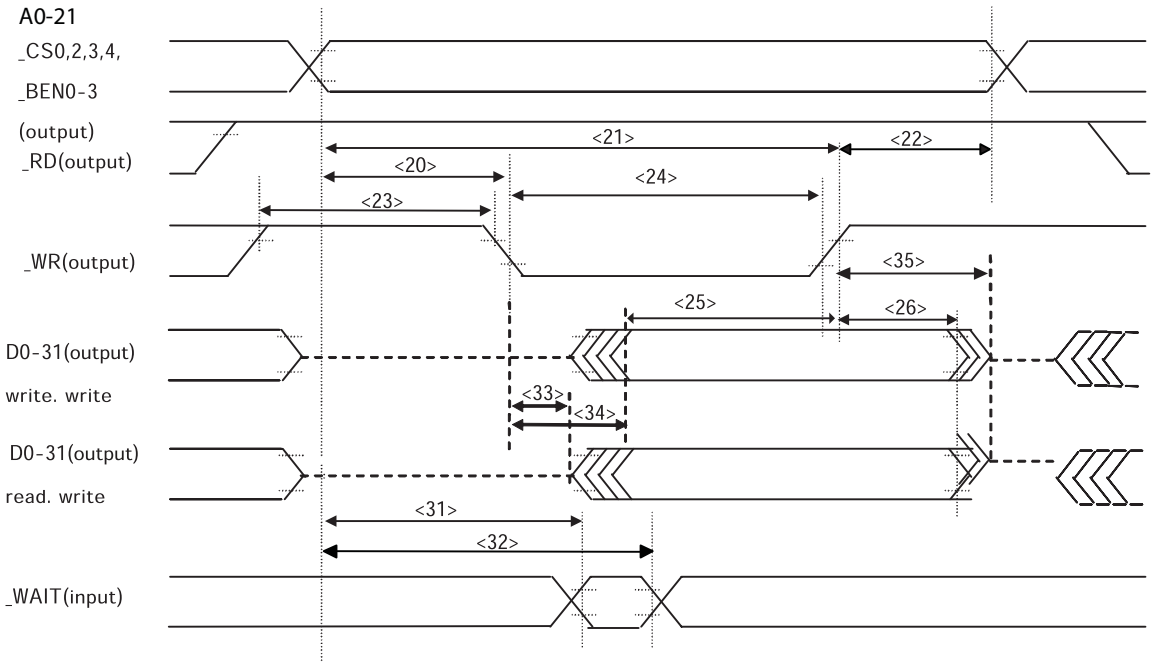
3. w_{AS}: Number of waits specified by AWC register
w_{AH}: Number of waits specified by AWC register

4. w_D: Number of waits specified by DWC0, DWC1 register; $w_D \geq 1$

5. w: Number of waits due to external wait signal ($\overline{WAIT}$)

6. n = 0, 2, 3, 4

Figure 1-12: External Asynchronous Memory Access Write Timing



1.6.5 Clocked Serial Interface B (CSIB) Characteristics

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V
The load capacity of the output terminal is CL=35pF.

Table 1-13: CSIB Characteristics (Master Mode)

CBnCKS2 to CBnCKS0 ≠ 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{CYSKM}	125		ns
$\overline{SCKBn}$ high level width	t_{WSKHM}	0.5 t_{CYSKM} - 10		ns
$\overline{SCKBn}$ low level width	t_{WSKLM}	0.5 t_{CYSKM} - 10		ns
SIBn setup time	t_{SSISKM}	20		ns
SIBn hold time	t_{HSKSIM}	10		ns
SOBn delay	t_{DSKSOM}		10	ns
SOBn hold time	t_{HSKSOM}	0.5 t_{CYSKM} - 10		ns

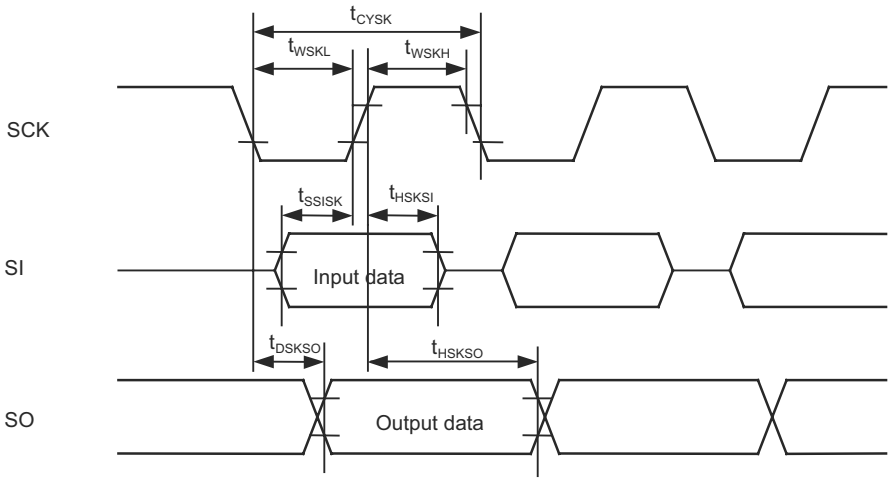
Table 1-14: CSIB Characteristics (Slave Mode)

CBnCKS2 to CBnCKS0 = 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{SCKBn}$ clock cycle time	t_{CYSKS}	125		ns
$\overline{SCKBn}$ high level width	t_{WSKHS}	0.5 t_{CYSKS} - 10		ns
$\overline{SCKBn}$ low level width	t_{WSKLS}	0.5t_{CYSKS} - 10		ns
SIBn setup time	t_{SSISKS}	5		ns
SIBn hold time	t_{HSKSIS}	10		ns
SOBn delay	t_{DSKSOS}		25	ns
SOBn hold time	t_{HSKSOS}	t_{WSKHS}		ns

Remark: n = 0, 1

Figure 1-15: CSIB Master/Slave Mode Timing



1.6.6 Clocked Serial Interface E (CSIE) Timing

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V
The load capacity of the output terminal is CL=35pF.

Table 1-16: CSIE Characteristics (Master Mode)

Parameter		Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time		t_{KCY}	31.25		ns
$\overline{SCKEn}$ cycle time		t_{KCYM}	125		ns
$\overline{SCKEn}$ high, low width		t_{KWHM}, t_{KWLM}	t_{KCYM}/2 - 10		ns
SIEn input setup time (vs. $\overline{SCKEn}$)		t_{SSIM}	20		ns
SIEn input hold time (vs. $\overline{SCKEn}$)		t_{HSIM}	10		ns
SOEn output delay (vs. $\overline{SCKEn}$)		t_{DSOM}		10	ns
SOEn output hold time (vs. $\overline{SCKEn}$)		t_{HSOM}	t_{KCYM}/2 - 10		ns
SCSEnm inactive (High) width	CEnSIT=x CEnOPE=0 CEnMD=x	t_{WSCSB0}	t_{KCYM}/2 - 10		ns
	CEnSIT=x CEnOPE=1 CEnMD=x	t_{WSCSB1}	$(CS_{IDLE} + 0.5)*t_{KCYM}$ - 10		ns
$\overline{SCSEnm}$ setup time (vs. $\overline{SCKEn}$)	CEnSIT=x CEnOPE=0 CEnIDL=x CEnMD=0	t_{SSCSB0}	t_{KCY} - 10		ns
	CEnSIT=x CEnOPE=1 CEnIDL=0 CEnMD=0	t_{SSCSB1}	$CS_{SETUP} * t_{KCYM} + t_{KCY}$ - 10		ns
	CEnSIT=x CEnOPE=1 CEnIDL=1 CEnMD=1	t_{SSCSB2}	$CS_{SETUP} * t_{KCYM} + t_{KCY}$ - 10		ns

Table 1-16: CSIE Characteristics (Master Mode)

Parameter		Symbol	MIN.	MAX.	Unit
SCSEnm hold time (vs. $\overline{SCKEn}$)	CEnSIT=0 CEnOPE=0 CEnMD=x	t_{HSCSB0}	t_{KCY} - 10		ns
	CEnSIT=1 CEnOPE=0 CEnMD=x	t_{HSCSB1}	t_{KCYM}/2 - 10		ns
	CEnSIT=0 CEnOPE=1 CEnMD=x	t_{HSCSB2}	CS_{HOLD} * t_{KCYM} - 10		ns
	CEnSIT=1 CEnOPE=1 CEnMD=x	t_{HSCSB3}	(CS_{HOLD} + 0.5)* t_{KCYM} - 10		ns
SCSEnm interframe time	CEnSIT=x CEnOPE=1 CEnMD=x	t_{INTER}	CS_{INTER} * t_{KCYM}		ns
	CEnSIT=x CEnOPE=0 CEnMD=x	-	Not Applicable		ns

Remark: n=0,1
m=7-0(n=0),3-0(n=1)
CS_{SETUP},CS_{INTER}: are set by register CEnOPT0
CS_{IDLE},CS_{HOLD}: are set by register CEnOPT1

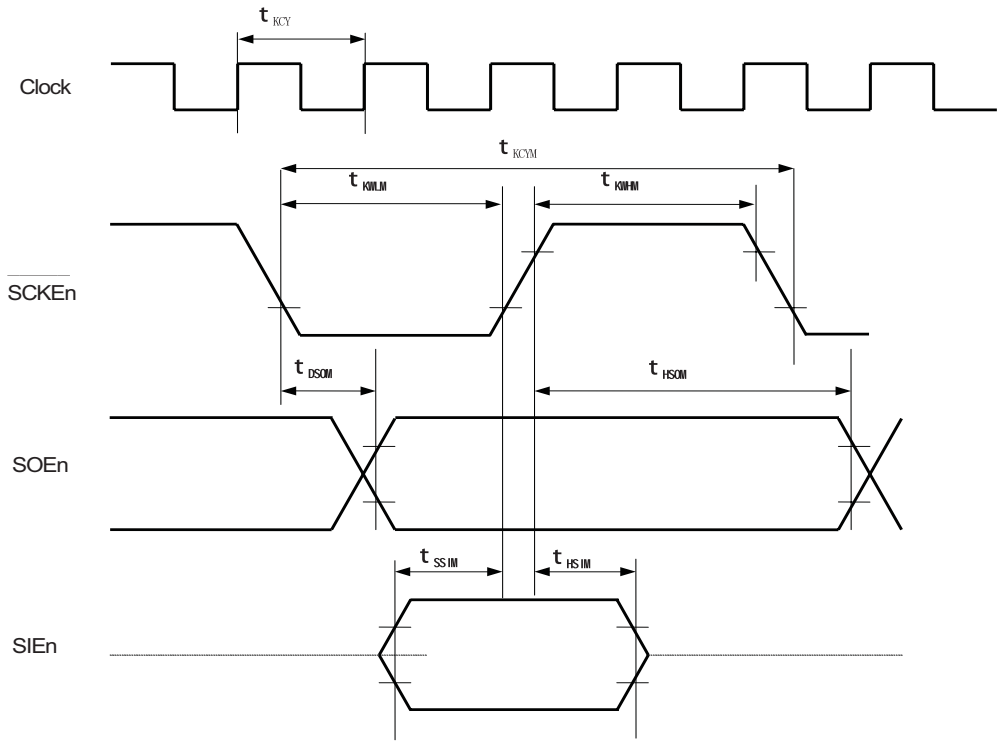
Table 1-17: CSIE Characteristics (Slave Mode)

Parameter	Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time	t_{KCY}	31.25		ns
$\overline{SCKEn}$ cycle time	t_{KCYS}	125		ns
$\overline{SCKEn}$ high, low width	t_{KWHS}, t_{KWLS}	t_{KCYS}/2 - 10		ns
SIEn input setup time (vs. $\overline{SCKEn}$)	t_{SSIS}	10		ns
SIEn input hold time (vs. $\overline{SCKEn}$)	t_{HSIS}	t_{KCY}*1.5 + 10		ns
SOEn output delay (vs. $\overline{SCKEn}$)	t_{DSOS}		20	ns
SOEn output hold time (vs. $\overline{SCKEn}$)	t_{HSOS}	t_{KCYS}/2 - 10		ns

Remark: n=0,1

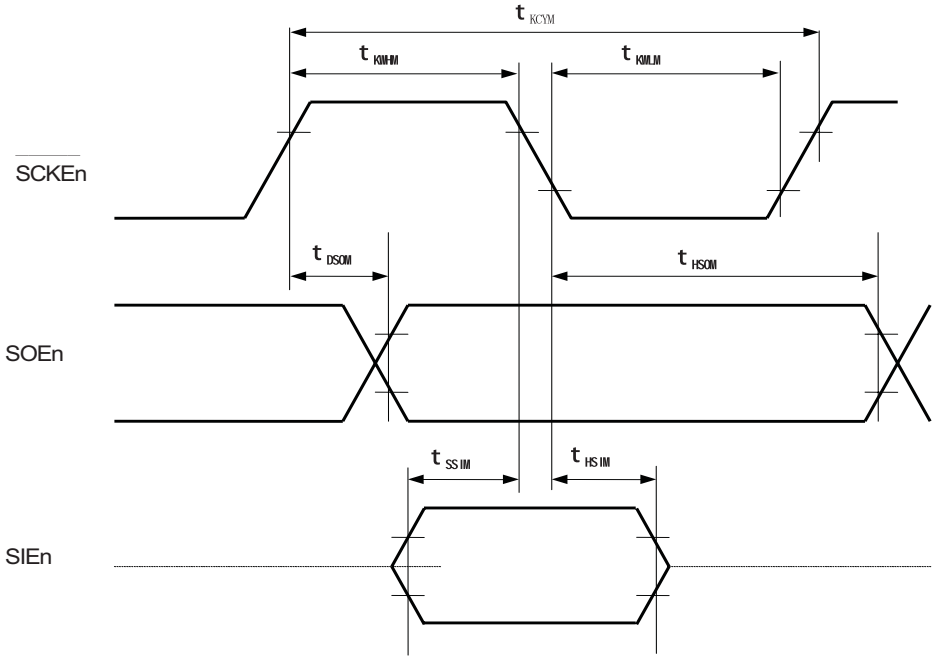
Figure 1-18: CSIEn Timings

(a) [$\overline{SCKEn}$/SIEn/SOEn] Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)



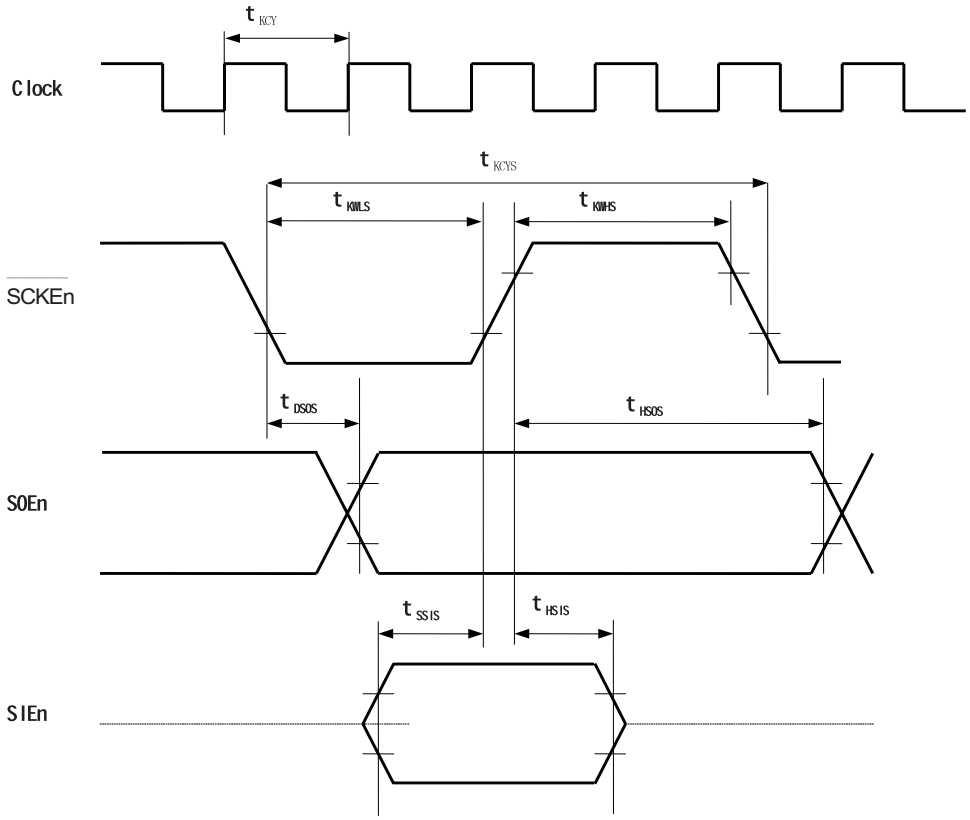
Remark: n=0-1

(b) [$\overline{SCKEn}$/SIEn/SOEn] Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)



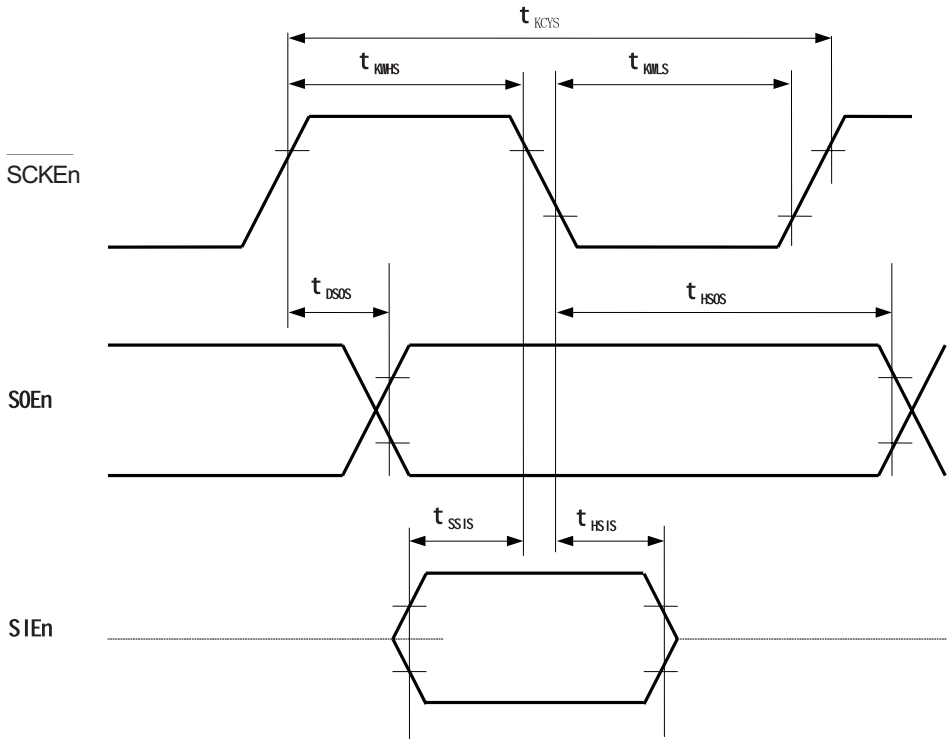
Remark: n=0-1

(c) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)



Remark: n=0-1

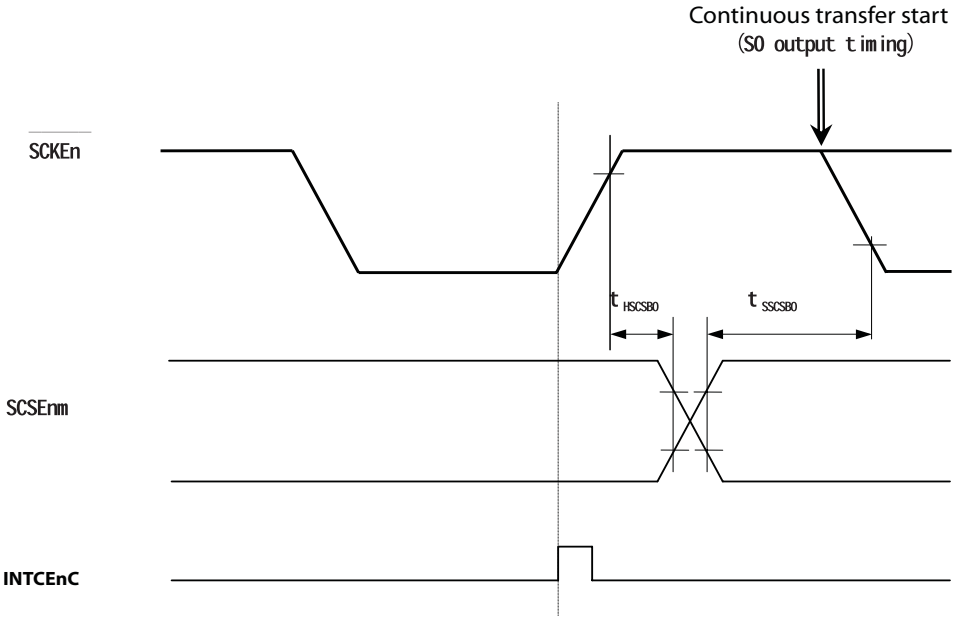
(d) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)



Remark: n=0-1

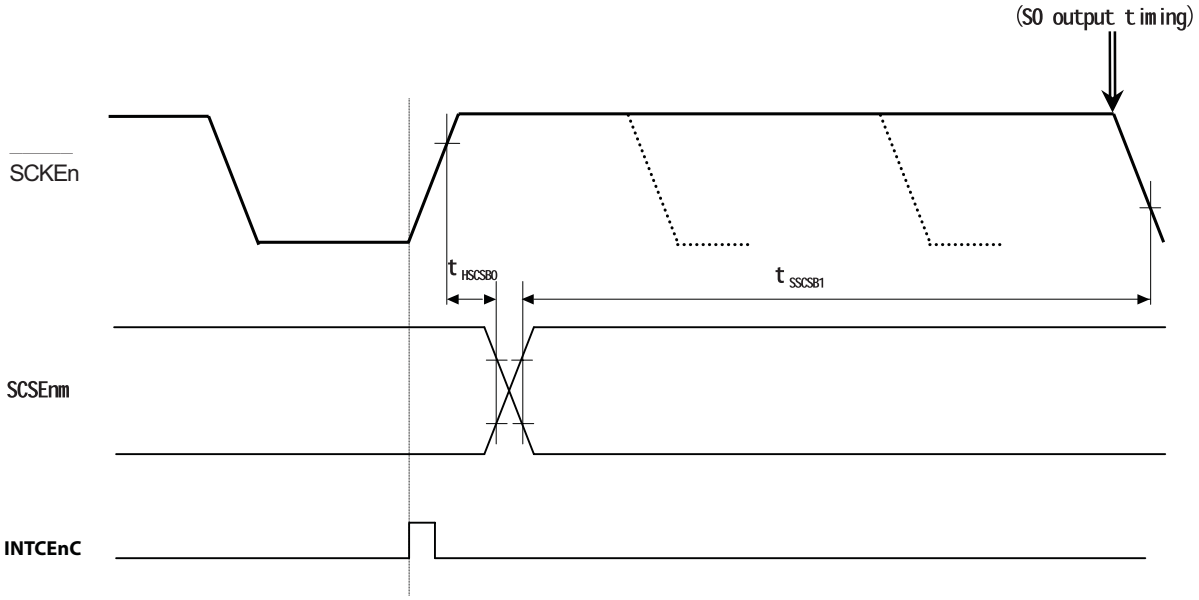
Figure 1-19: CSEn7 - CSEn0 Pin Timings

(e) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=0/0)



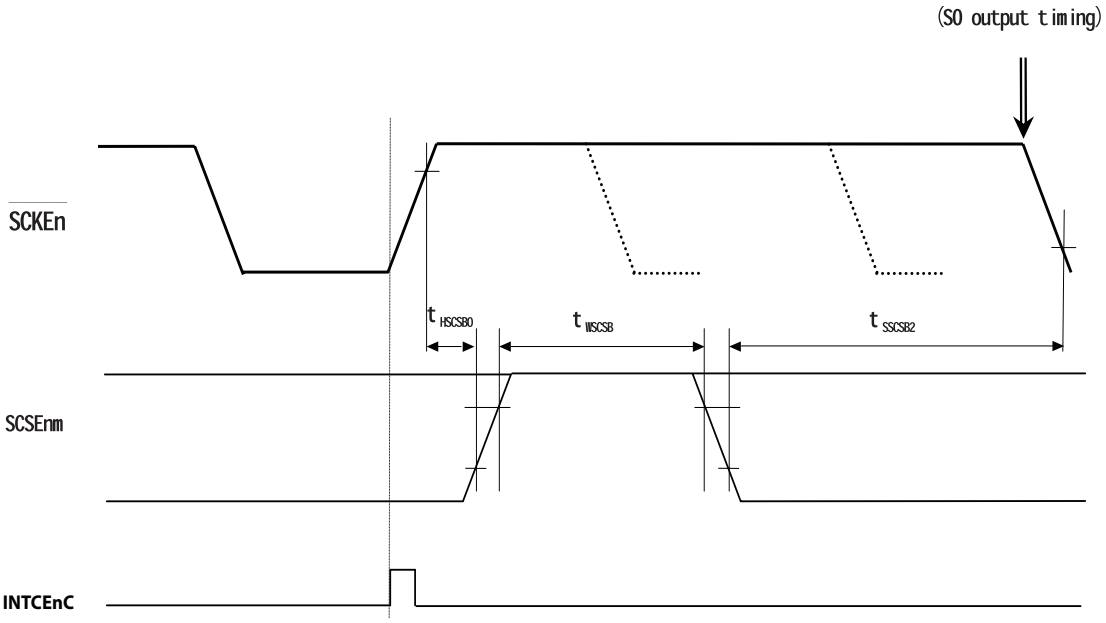
Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

(f) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=1/0)



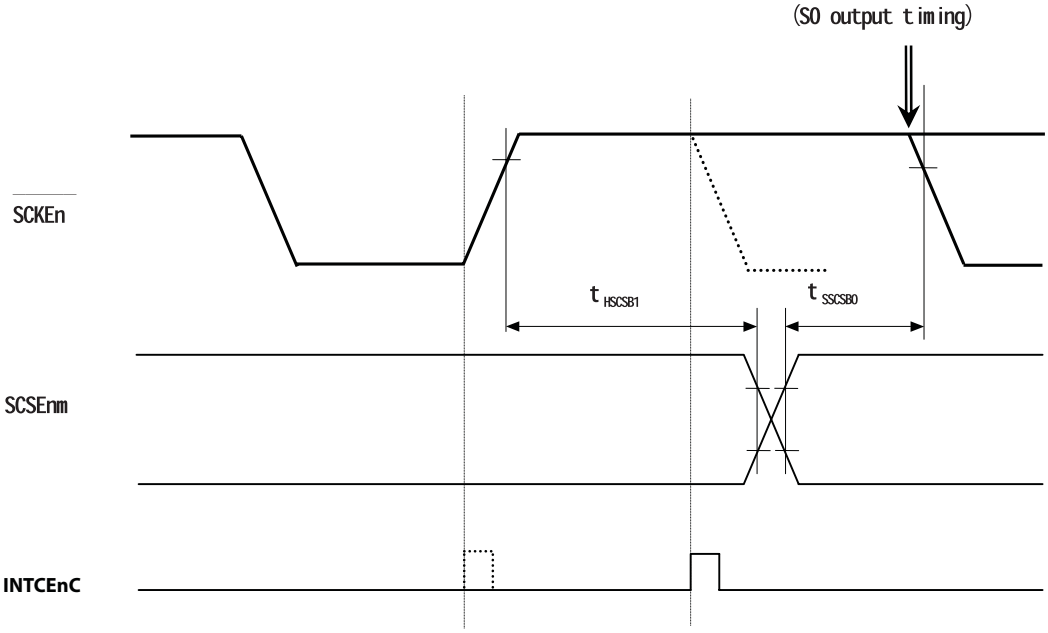
Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

(g) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=1/1)



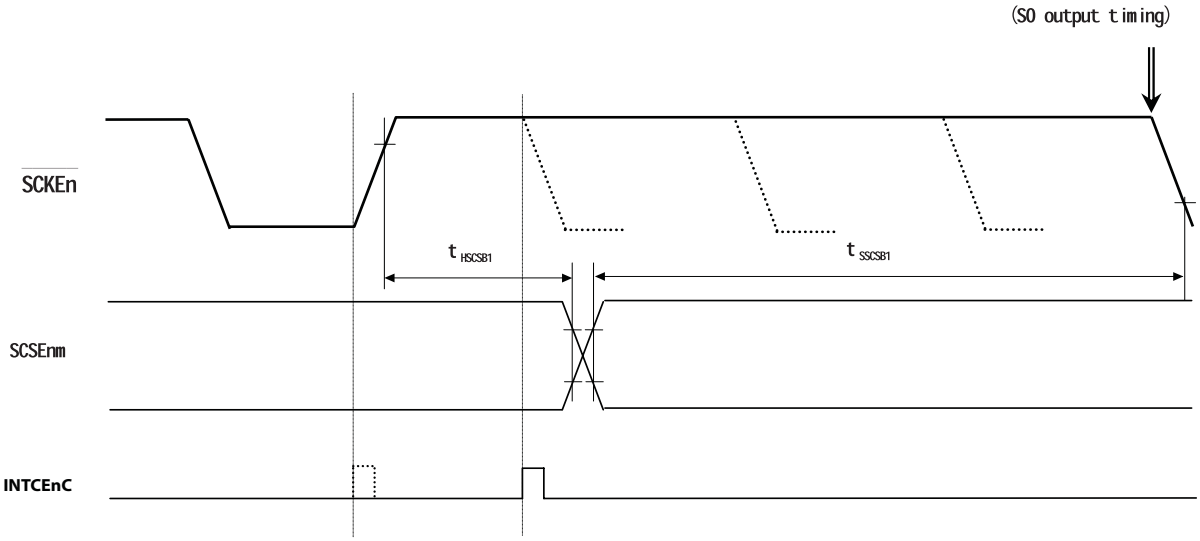
Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

(h) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=0/0)



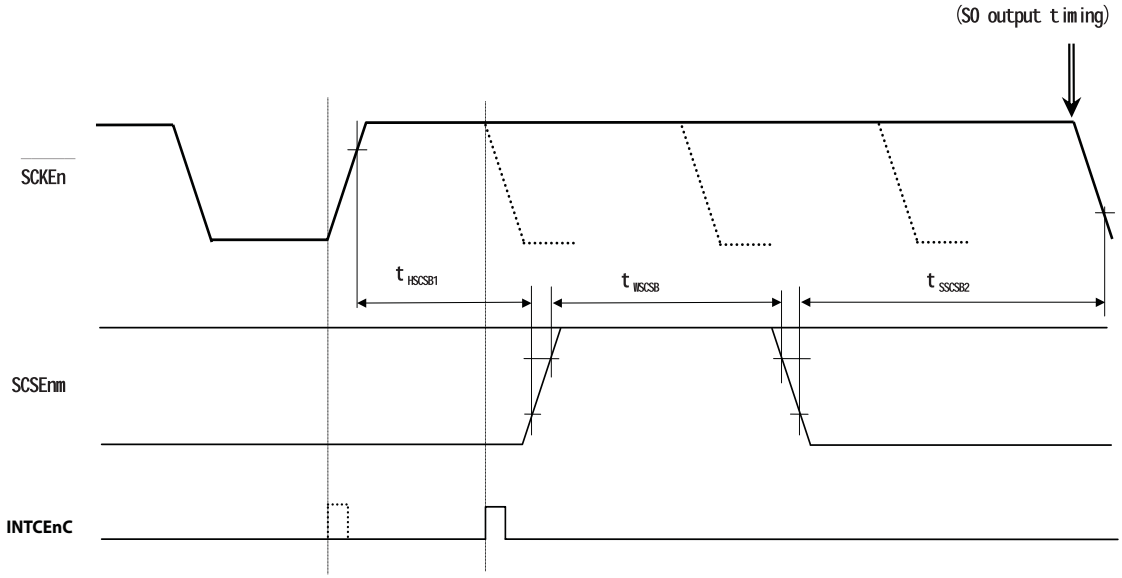
Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

(i) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=1/0)



Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

(j) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=1/1)



Remark: n=0-1
m=7-0(n=0),3-0(n=1)
INTCEnC: CSIEn transfer end interrupt

1.6.7 UARTC Timing

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V
The load capacity of the output terminal is CL=35pF.

Table 1-20: UARTC Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UARTC}			4	Mbps

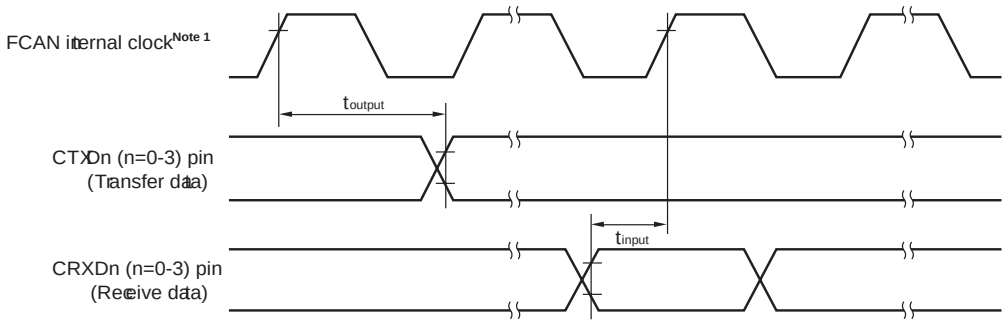
1.6.8 CAN Timing

T_a= -40 to +125°C
T_j = -40 to +150°C
$V_{DD15x} = CV_{DD15}$ = 1.5V +/-10%,
V_{DD3x} = 3.3V +/- 0.3V,
$V_{SS15x} = CV_{SS15} = V_{SS3x}$ = 0V
The load capacity of the output terminal is CL=35pF.

Table 1-21: CAN Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Internal transmit to receive data delay	t_{node}	$t_{node} = t_{output} + t_{input}$		75	ns

Figure 1-22: CAN Timing



Notes: 1. The FCAN internal clock corresponds to the FCAN macro clock.

Figure 1-23: Internal Delay

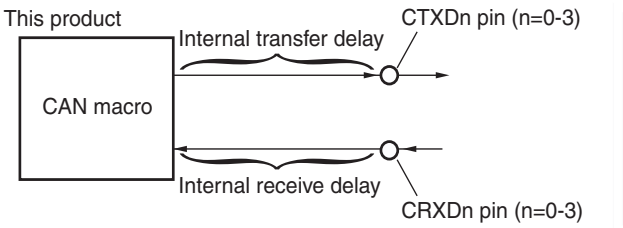


Image figure of internal delay

1.6.9 AD Converter

T_a= -40 to +125°C
T_j = -40 to +150°C
VDD15x = CVDD15 = 1.5V +/- 10%V,
VDD3x = 3.3V +/- 0.3V,
AVDD = AVREF0,1 = 3.3V +/- 0.3V,
VSS15x = CVSS15 = VSS3x = 0V,

Table 1-24: AD Converter

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution				10		bit
Overall error[a]	TOE				+/-4	LSB
Quantisation error					+/-0.5	LSB
Conversion time (Note 2)	t_{CONV}		2.0		8.0	µs
Sampling time	t_{SAMP}	(Note 1)		3 x t_{CONV} / 16		s
Analog input voltage	V_{IAN}		$AV_{SS0,1}$		$AV_{REF0,1}$	V
AV_{REFn} input voltage	$AV_{REF0,1}$	$AV_{REF0,1}$ = AV_{DD}			AV_{DD}	V
AV_{REFn} input current	$AI_{REF0,1}$			60	300	µA
AV_{DD} electric current	AI_{DD}				6	mA

a. The quantization error is not included.

Notes: 1. The conversion time is set by the ADMn1 register. For ADMn1 register setting please refer to the users manual.

2. The conversion time only in the analog part. The conversion time depends on register setting ADMn1. For ADMn1 register setting please refer to the users manual.

1.6.10 Flash Memory Programming Characteristics

(1) Basic Characteristics

T_a= -40 to +125°C
T_j = -40 to +150°C
VDD15x = CVDD15 = 1.5V +/- 10%V,
VDD3x = 3.3V +/- 0.3V,
AVDD = AVREF0,1 = 3.3V +/- 0.3V,
VSS15x = CVSS15 = VSS3x = 0V,
The load capacity of the output terminal is CL=35pF.

Table 1-25: Flash Programming Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	f_{xx}		80		128	MHz
High Level Input Voltage	VIH	FLMD0	0.7VDD3x		VDD3x	
Low Level Input Voltage	VIL	FLMD0	-0.5		0.3VDD3x	
Code Flash	Reprogramming				100	times
	Data retention				15	years
Data Flash	Reprogramming				10000	times
	Data retention				3	years

(2) Serial Writing Operating Conditions

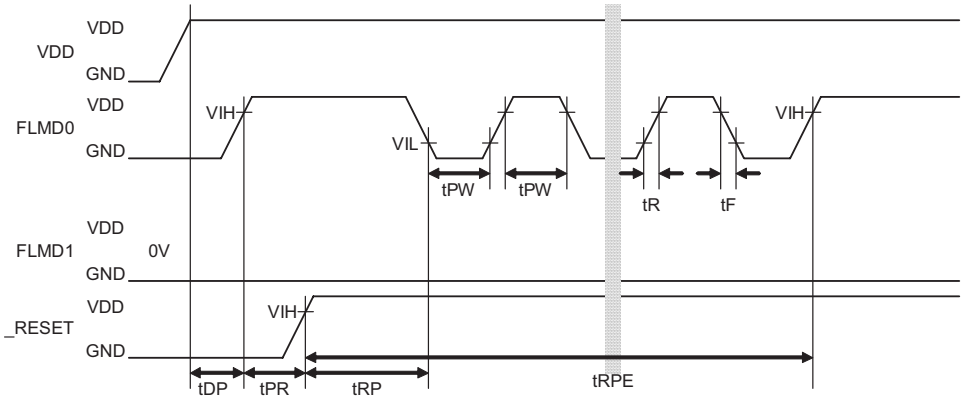
T_a= -40 to +125°C
T_j = -40 to +150°C
VDD15x = CVDD15 = 1.5V +/- 10%V,
VDD3x = 3.3V +/- 0.3V,
AVDD = AVREF0,1 = 3.3V +/- 0.3V,
VSS15x = CVSS15 = VSS3x = 0V,
The load capacity of the output terminal is CL=35pF.

Table 1-26: Serial Writing Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	t_{DP}		1			ms
RESET release (from FLMD0)	t_{PR}	(Note 1)	2			ms
Count start time from $\overline{\text{RESET}}$ to FLMD0	f_{RP}		1.2			ms
Count finish time from $\overline{\text{RESET}}$ to FLMD0	f_{RPE}				10	ms
FLMD0 high / low level width	t_{PW}		10		100	µs
FLMD0 raise / fall time	t_R / t_F				1	µs

Notes: 1. Please consider also the power supply turning on to $\overline{\text{RESET}}$ release timing.

Figure 1-27: Serial Write Operation Timing



2. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to the Joint Industry Standard:

JEDEC J-STD-020C (MSL=3)

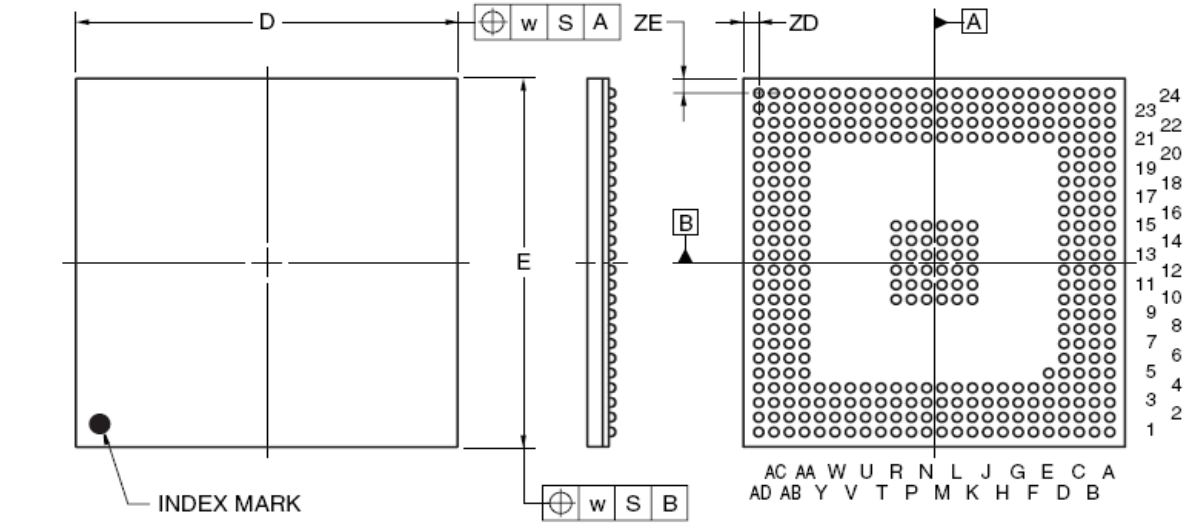
For soldering methods and conditions other than those recommended please consult NEC.

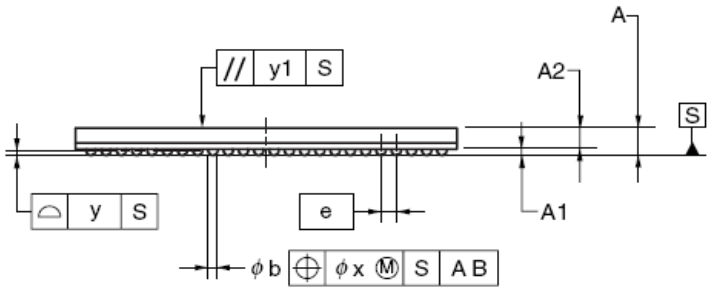
[MEMO]

3. Package Drawings

Figure 3-1: µPD70F3483F1(A2)-JA1, µPD70F3441F1(A2)-JA1

357-PIN PLASTIC FBGA (20x20)





(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.10
E	20.00±0.10
w	0.20
A	1.43±0.10
A1	0.30±0.05
A2	1.13
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.12
y	0.10
y1	0.20
ZD	0.80
ZE	0.80

P357F1-80-JA1-1

[MEMO]

4. Revision History

Table 4-1: Revision History

Version	Date	Remarks.
1.0	2006/05/31	Initial revision
1.1	2007/07/05	I_{DD} currents for 80 MHz added (Table 1-7 on page 7)
		Revision history added
		Adjusted min timings for tRLR and tRIR
		Flash characteristics added
		Added special storage temperature
		Changed naming from CV_{DD} to CV_{DD15}
		Added reset timing
		NBD operating temperature added
		Junction temperature for bare die added
		External asynchronous memory access timing updated
		CSIB timing updated
		CSIE slave mode, formula of t_{HSIS} corrected
		CSIE master mode, formula of t_{SSCSB2} corrected
		Turning On / Interception timing modified
		Package drawing, parameters A and A1, updated.
2.0	2008/05/19	μPD70F3483 added
		Temperature range for Bare Die added
		MSL for soldering conditions added

[MEMO]

Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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