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April 1st, 20<mark>10</mark> Renesas Electronics Corporation

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BIPOLAR ANALOG INTEGRATED CIRCUITS μ PC815, μ PC816

ULTRA LOW OFFSET VOLTAGE, LOW DRIFT, LOW NOISE HIGH SLEW RATE, WIDEBAND, OPERATIONAL AMPLIFIER

DESCRIPTION

The μ PC815, μ PC816 are high accuracy OP amps which realize 20 μ V input offset voltage and 2.8 nV/ $\sqrt{\rm Hz}$ input noise by using advanced on-chip resistor trimming technique and ultra low noise NPN transistor for input stage. The μ PC816, high speed version of the μ PC815, realizes 25 MHz bandwidth and 7 V/ μ s slewrate with full frequency compensation characteristics by the effect of output stage high speed PNP transistors. Input stage Is canceling circuits which minimize-input bias current are also distinctive feature. By these features, the μ PC815, μ PC816 are optimum choice for instrumentation amplifier, audio pre-amplifier and buffer amplifier for high resolution DAC.

FEATURES

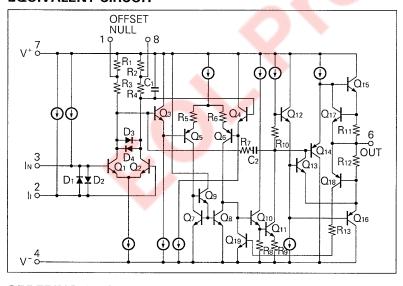
- Wide supply voltage range: ±3 to ±22 V
- Ultra low offset voltage: $\pm 20 \mu V$ TYP.
- Ultra low offset voltage drift: $\pm 0.3 \,\mu\text{V/}^{\circ}\text{C}$ TYP. (unnull)
- Ultra low noise: 2.8 nV/ $\sqrt{\text{Hz}}$ (TYP.) (fo = 10 Hz)
- High slew-rate: μ PC815: 1.6 V/ μ s TYP. (A $_{0}$ = 1)
 - μ PC816: 7.6 V/ μ s TYP. (A₀ = 1)
- Wide bandwidth product:

 μ PC815: 7 MHz TYP. (fo = 100 kHz) μ PC816: 25 MHz TYP. (fo = 100 kHz)

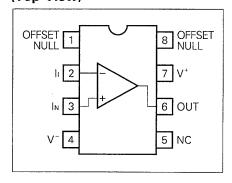
- Low input bias current: ±10 nA TYP.
- Internal full frequency compensation
- Stable operation under capacitive load:

μPC815: 100 pF μPC816: 1 000 pF

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM (Top View)



ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPC815D	O DIN OFF AND DIR (OCC. 1)	Standard
μPC815D(1)	8 PIN CERAMIC DIP (300 mil)	Standard
μPC815C	O DIN DI ACTIO DID (CCC)	Standard
μPC815C(1)	8 PIN PLASTIC DIP (300 mil)	Standard
μPC816D	8 PIN CERAMIC DIP (300 mil)	Standard
μPC816C	8 PIN PLASTIC DIP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.



ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

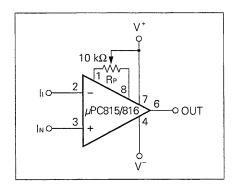
PARAMETER		SYMBOL	μPC815D	μPC815C	μPC816D	μPC816C	UNIT
Voltage between V ⁺ and V ⁻	(Note 1)	V+ - V-		V			
Differential Input Current		lib		mA			
Input Voltage	(Note 2)	Vı		V			
Output Voltage	(Note 3)	VD		V			
Power Dissipation		Рт	500 (Note 4) 350 (Note 5) 500 (Note 4) 350 (Note 5)				mW
Output Short Circuit Duration (Note 6)				Inde	finite		sec
Operating Temperature Ran	ge	Topt	-20 to +80 -20 to +70 -20 to +80 -20 to +70				
Storage Temperature Range		T _{stg}	-55 to +150	-55 to +125	-55 to +150	-55 to +125	°C

- Note 1. Reverse connection of supply voltage can cause destruction.
- **Note 2.** The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.
- **Note 3.** This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.
- Note 4. Thermal derating factor is -5.0 mV / °C when ambient temperature is higher than 50 °C.
- Note 5. Thermal derating factor is -5.0 mV / °C when ambient temperature is higher than 55 °C.
- Note 6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings,
 Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V [±]	± 3	± 15	± 20	V
Output Current		lo			± 25	mA
Consisting Lond / A 1 Page 0.01	μPC815	C .			1000	- pF
Capacitive Load (A ₀ = +1, Rf = 0 Ω)	μPC816	CL			100	pr

OFFSET VOLTAGE NULL CIRCUIT



ELECTRICAL CHARACTERISTICS (V $^{\pm}$ = ± 15 V, Ta = 25 °C)

CHARACTERISTIC	2	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Voltage		Vio		±20	±60	μV	Rs ≦ 100 Ω
Input Offset Current		lio		±7	±50	nA	
Input Bias Current		lв		±10	±55	nA	
Input Resistance – Comr	non Mode	Rincм		3		GΩ	
Large Signal Voltage Ga	in	Αυ	5	20		V/μV	$RL \geqq 2 \ k\Omega, \ Vo = \pm 12 \ V$
Supply Current		lcc		3.0	4.6	mA	Io = 0 A
Common Mode Rejectio	n Ratio	CMR	110	130		dB	
Supply Voltage Rejection	n Ratio	SVR	106	126		dB	$V^{\pm} = \pm 3 \text{ V} \rightarrow \pm 18 \text{ V}$
Output Voltage Swing		Vom	±12.5	+13.5 -14.0		v	RL ≧ 2 kΩ
Output Voltage Swilig		Vom	±10.5	+12.5 -13.5		V	RL ≥ 600 Ω
Common Mode Input Volta	age Range	Vicм	±11	+12.5 -13.5		v	L
Slew Rate	μPC815	SR	0.8	1.6		V/μs 🥒	$RL = 2 k\Omega$
olew flate	μPC816	311	3	7.6		V /μ3	$R_L = 2 k\Omega$
Gain Bandwidth Product	μPC815	GBW	4	7		MHz	fo = 100 kHz
Gain Banawian Froduct	μPC816	GBW	15	25		141112	fo = 100 kHz
Input Equivalent Noise \	'oltage	NL		0.06	0.13	μV _{p-p}	Rs = 100 Ω , f = 0.1 to 10 Hz
				2.8	4.5		fo = 10 Hz
Input Equivalent Noise Volta	ge Density	e n		2.7	4.0	nV/√Hz	fo = 100 Hz
				2.7	3.8		fo = 1 000 Hz
Input Equivalent Noice Curr	ant Deneity	İn		1.5	4.0	pA/√Hz	fo = 10 Hz
mpat Equivalent Noise Curr	Input Equivalent Noise Current Density			0.4	0.6	pAy v 112	fo = 1 000 Hz
Vio Adjustment Range				±3		mV	$R_p = 10 \text{ k}\Omega$
Long Term Vio Stability	(Note 7)			±0.2	±1.0	μV/Mo	

Note 7. Long term input offset voltage stability refers to the average trend line of offset vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vio during 30 days are typically 2.5 μ V – refer to typical performance curve.

$-20 \le T_a \le 80 \, ^{\circ}\text{C} \, (\mu\text{PC815D}, \, 816\text{D}), \, -20 \le T_a \le 70 \, ^{\circ}\text{C} \, (\mu\text{PC815C}, \, 816\text{C}), \, V^{\pm} = \pm 15 \, \text{V}$

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Voltage	Vio		±20	±110	μV	Rs ≦ 100 Ω
Input Offset Current	lio		±7	±70	nA	
Input Bias Current	lв		±10	±75	nA	
Large Signal Voltage Gain	Αυ	2.5	20		V/μV	$RL \ge 2 k\Omega$, $Vo = \pm 10 V$
Supply Current	lcc	-	3	5	mA	
Common Mode Rejection Ratio	CMR	106	130		dB	$V^{\pm} = \pm 3 \text{ V} \rightarrow \pm 18 \text{ V}$
Supply Voltage Rejection Ratio	SVR	102	126		dB	RL ≧ 2 kΩ
Output Voltage Swing	Vom	±12	+13.5 -14.0		V	
Common Mode Input Voltage Range	Vicм	±10.5	+12.5 -13.5		٧	
Average Vio Temperature Drift	⊿Vio/⊿T		±0.3	±1.5	μV/°C	Rs ≤ 100 Ω



The μ PC815D(1) & 815C(1) are temperature drift sorted for high accuracy application. The Δ Vio/ Δ T spec is shown below.

μ PC815D(1), 815C(1)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Average Vio Temperature Drift	⊿V10/⊿T			±0.8	μV/°C	Rs ≦ 100 Ω

APPLICATION INFORMATION

1. Over differential input voltage application

The μ PC815/816 contain the input protection back-to-back diodes at input stage. However the input current limit resistors are not used in order to achieve ultra low noise. (See EQUIVALENT CIRCUIT) Therefore, when the over differential input voltage is applied, the differential input current should be kept less than 25 mA by inserting the series resistors at the inputs.

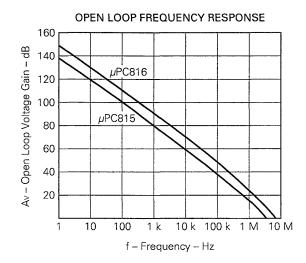
2. Unity gain buffer application

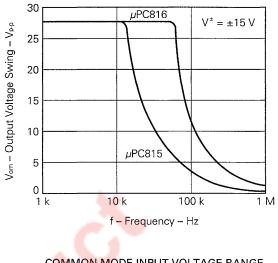
When the input is driven faster than the Slew Rate under the condition of Rf & Rs = 0 Ω , the input protection diodes will short the input to the output, and the input current is limited only by the output drive capability. The solution of this problem is inserting the feedback resistor Rf \gg 1 k Ω , or the source resistor Rs \gg 1 k Ω to limit the input short current.

If the feedback resistor Rf becomes bigger, a pole created with Rf and Cin (input capacitance) at $f = \frac{1}{2\pi R_f C_{in}}$ reduces the phase margin. Considering the worst case, the oscillation will occur.

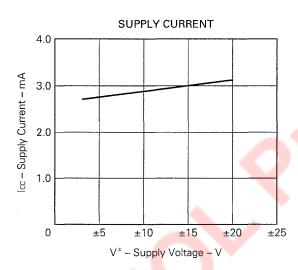
The solution of this problem is connecting the small capacitor (several 10 pF) in parallel with Rf.

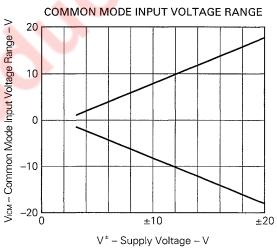
TYPICAL PERFORMANCE CHARACTERISTICS (Ta = 25 °C)

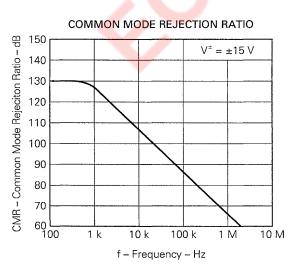


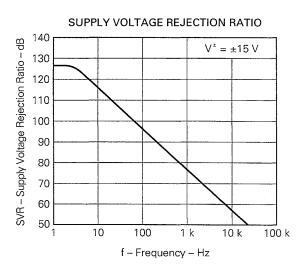


LARGE SIGNAL FREQUENCY RESPONSE









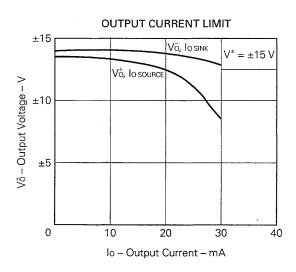
(V)

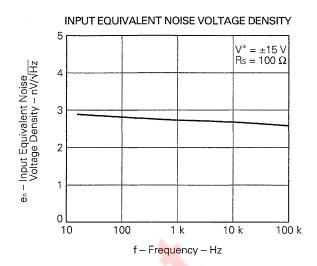
+10

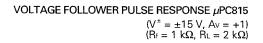
0

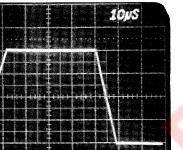
-10

0







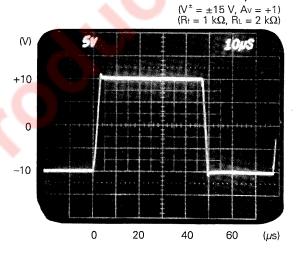


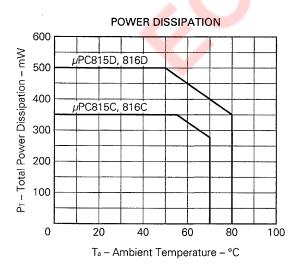
40

(µs)

60

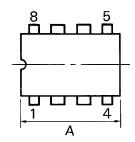


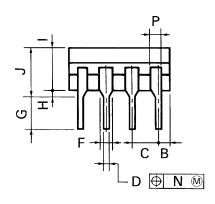


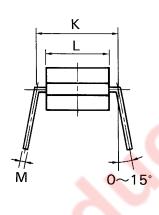


20

8PIN CERAMIC DIP (300 mil)







P8DH-100-300A,B

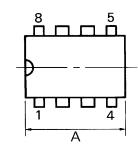
NOTES

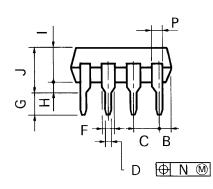
- Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition
- 2) Item "K" to center of leads when formed parallel.

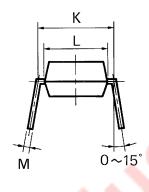
ITEM	MILLIMETERS	INCHES
Α	10.16 MAX.	0.400 MAX.
В	1.27 MAX.	0.050 MAX.
С	2.54 (T.P.)	0.100 (T.P.)
D	0.46 ± 0.05	0.018 + 0.002
F	1.42 MIN.	0.055 MIN.
G	3.0 ^{±0.3}	0.118 ^{±0.012}
Н	0.51 MIN.	0.020 MIN.
I	3.80	0.150
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.30	0.248
M	0.25 ^{±0.05}	0.010+0.002
N	0.25	0.01
Р	0.89 MIN.	0.035 MIN.



8PIN PLASTIC DIP (300 mil)







P8C-100-300B,C

NOTES

- Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
А	10.16 MAX.	0.400 MAX.
В	1.27 MAX.	0.050 MAX.
С	2.54 (T.P.)	0.100 (T.P.)
D	0.50 + 0.10	0.020 +0.004
F	1.4 MIN.	0.055 MIN.
G	3.2 ^{±0.3}	0.126 +0.012
Н	0.51 MIN.	0.020 MIN.
ı	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
К	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
М	0.25 -0.05	0.010 +0.004
N	0.25	0.01
Р	0.9 MIN.	0.035 MIN.



RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF THROUGH HOLE DEVICE

[μ PC815D, μ PC815C, μ PC816D, μ PC816C]

Soldering method	Soldering conditions	Recommended condition symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	



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M4 92.6