UPC4082

J-FET Input Dual Operational Amplifier

DESCRIPTION

UPC4082 is a dual operational amplifier incorporating well matched ion implant P-channel J-FET on the same chip with standard bipolar transistors. The key feature of this op amp is very low input bias current and high slew rate for ten times faster than conventional general purpose op amps. By these features the UPC4082 is excellent choice for wide variety of applications including integrator, active filter, pulse amp etc.

FEATURES

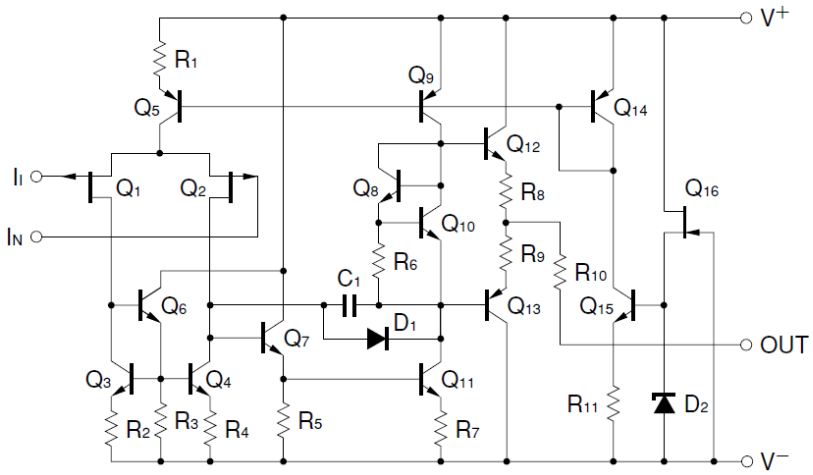
- Input Offset Voltage ±5 mV (TYP.)
- Input Bias Current 30 pA (TYP.)
- Slew Rate 13 V/μs (TYP.)
- Unity Gain Frequency 3 MHz (TYP.))
- Input Equivalent Noise Voltage Density 25 nV/$\sqrt{\text{Hz}}$ (TYP.) (f = 1 kHz)
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Dual Op-Amp terminal connection (pin compatible)

ORDERING INFORMATION

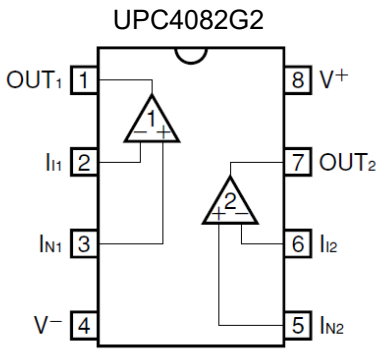
Order Name (1)	Package
UPC4082G2-AP	8-Pin plastic SOP (5.72 mm (225))

(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping. Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

EQUIVALENT CIRCUIT (1/2 Circuit)



PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	UPC4082G2	Unit
Supply Voltage Note1	$V^+ - V^-$	-0.3 ~ +36	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Note 2	V_I	V^- -0.3 ~ V^+ +0.3	V
Output Applied Voltage Note3	V_O	V^- -0.3 ~ V^+ +0.3	V
Total Power Dissipation Note4	P_T	440	mW
Output Short Circuit Duration Note5		Indefinite	s
Operating Ambient Temperature	T_A	-20 ~ +80	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

【Note】 **1.** Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

4. This is the value at $T_A \leq +25$ °C. Thermal derating factor is -4.4 mW/°C when operating ambient temperature is higher than 25 °C.

5. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	$V^{\pm}$	±5		±16	V
Load Current	I_O			±10	mA
Load Capacitance (A_V = +1, R_f = 0Ω)	C_L			100	pF

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±5	±15	mV	R_S ≤ 50 Ω
Input Offset Current Note6	I_{IO}		±5	±200	pA	
Input Bias Current Note6	I_B		30	400	pA	
Large Signal Voltage Gain	A_V	25000	200000			R_L ≥ 2 kΩ, V_O = ±10 V
Circuit Current Note7	I_{CC}		4.0	5.6	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	76		dB	
Supply Voltage Rejection Ratio	SVR	70	76		dB	
Output Voltage Swing	V_{om}	±12	±13.5		V	R_L ≥ 10 kΩ
Output Voltage Swing	V_{om}	±10	±12		V	R_L ≥ 2 kΩ
Common Model Input Voltage Range	V_{ICM}	±10	+15 -12.7		V	
Slew Rate	SR		13		V/μs	A_V = 1
Unity Gain Frequency	f_{unity}		3		MHz	
Input Equivalent Noise Voltage Density	e_n		25		nV/√Hz	R_S = 100 Ω, f = 1 kHz
Channel Separation			120		dB	
Input Offset Voltage	V_{IO}			±20	mV	R_S ≤ 50 Ω, T_A = -20 ~ +70 °C
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$		±10		μV/°C	T_A = -20 ~ +70 °C
Input Offset Current Note6	I_{IO}			±5	nA	T_A = -20 ~ +70 °C
Input Bias Current Note6	I_B			10	nA	T_A = -20 ~ +70 °C

【Note】 **6.** The direction of the input bias current is the same direction that flows into the IC because the first stage is composed of Pch J-FET. When T_J = 25°C or higher, it increases exponentially with increase in temperature (please see I_B - T_A characteristics). During measurement, please kindly take care of $T_J \fallingdotseq T_A$.

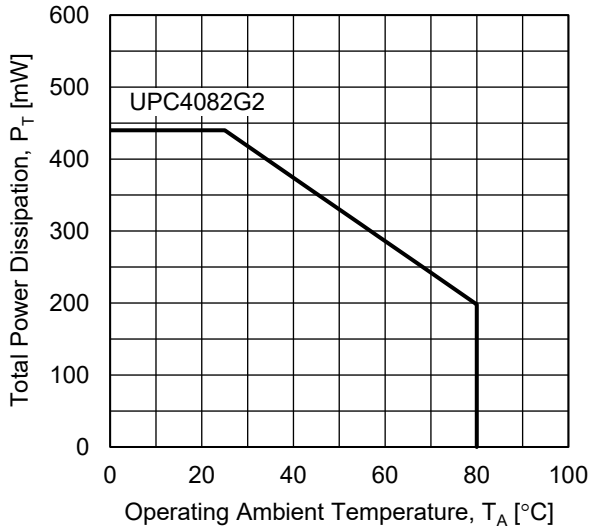
7. It is the current that flows into the internal circuit. This current flows irrespective of the channel usage.

Caution

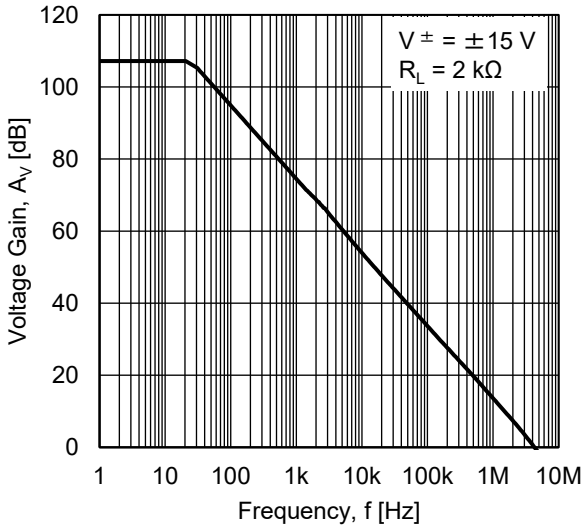
Since UPC4082 has high input impedance characteristics, please be careful of insulation between the terminals on the board.

ELECTRICAL CHARACTERISTICS CURVE (T_A = 25 °C, TYP.)

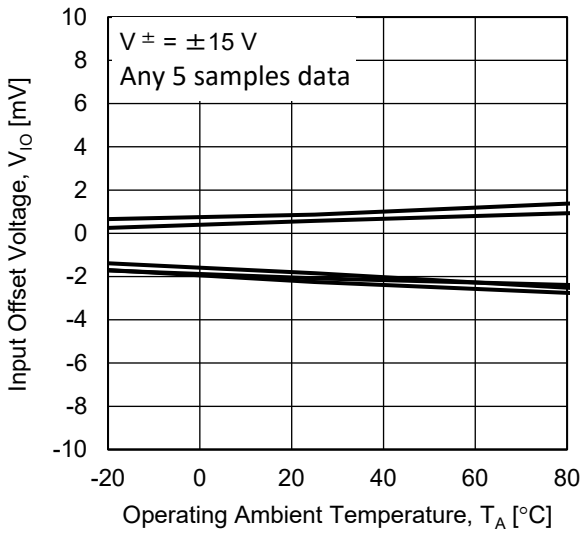
P_T vs. T_A (Absolute maximum rating)



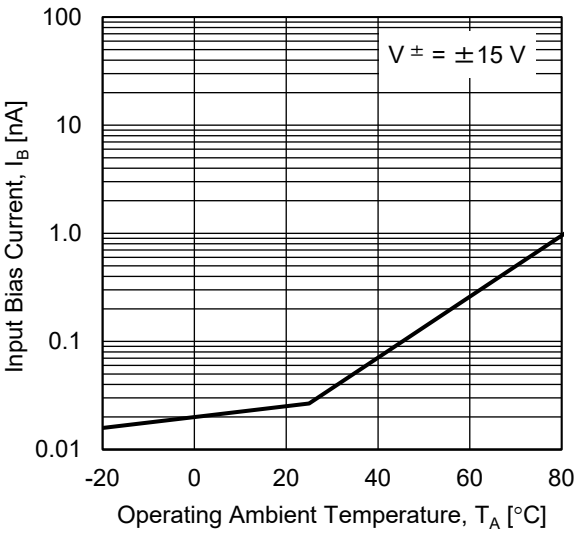
A_V vs. f



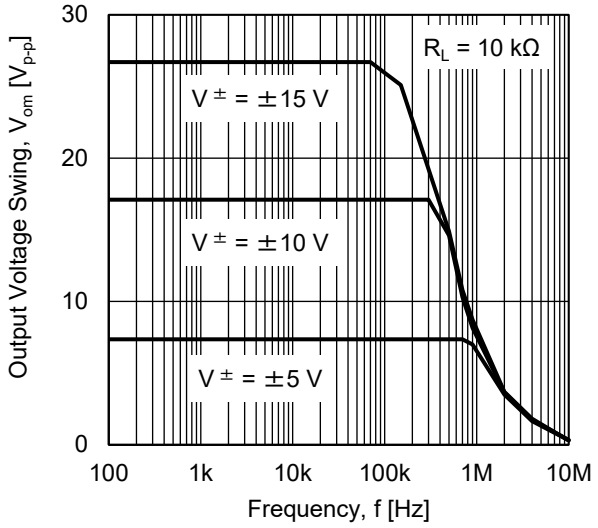
V_{IO} vs. T_A



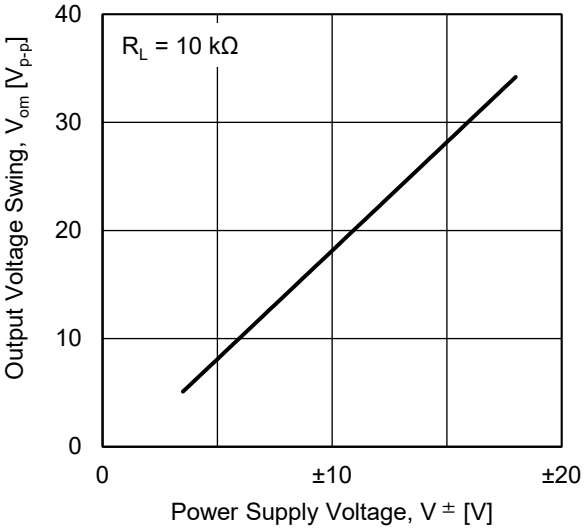
I_B vs. T_A

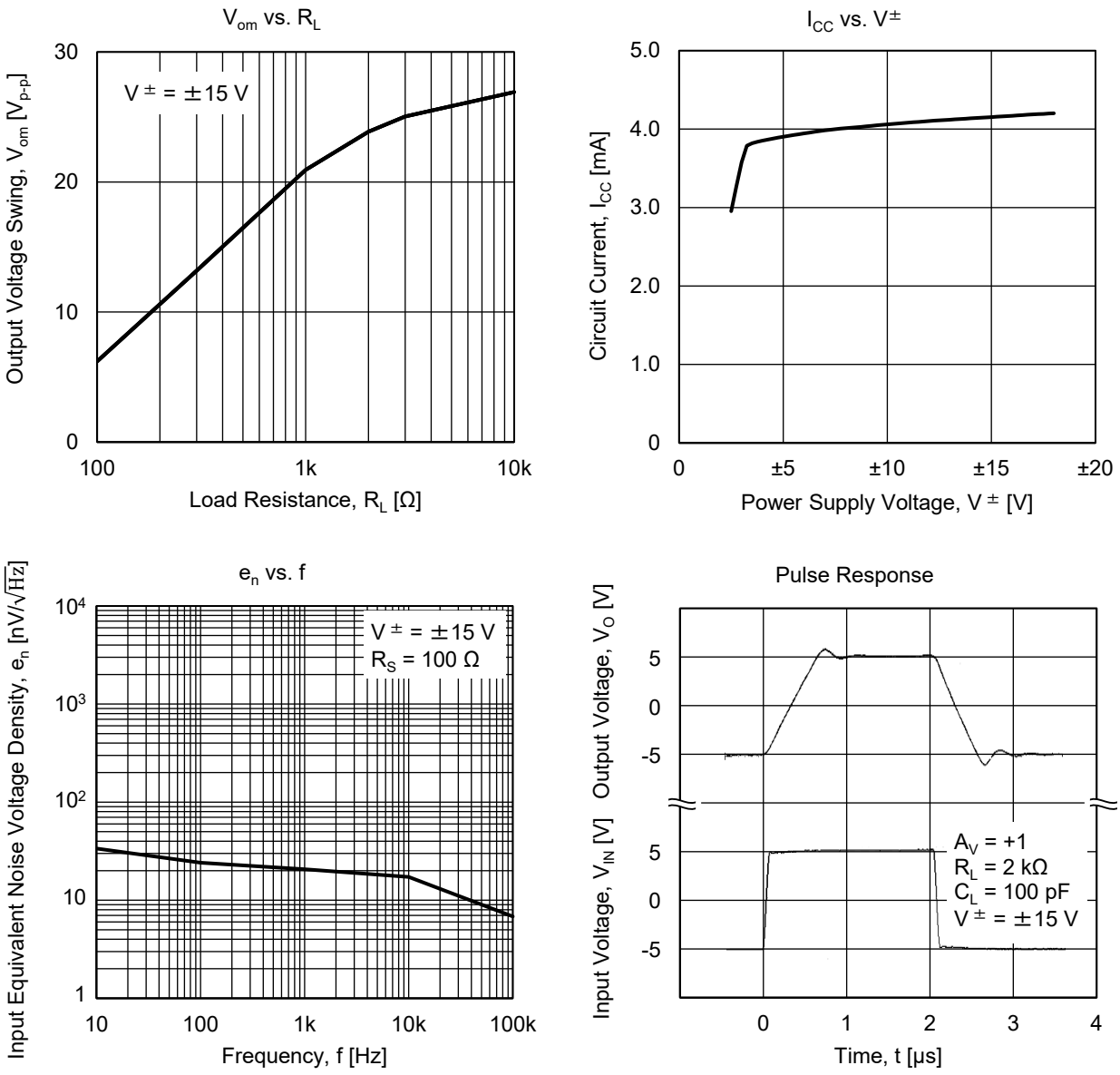


V_{om} vs. f



V_{om} vs. $V^{\pm}$

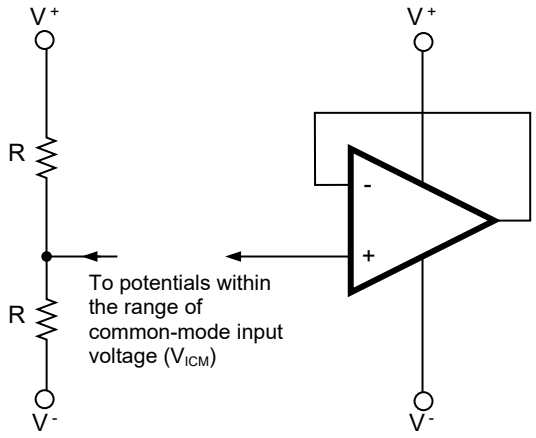



V_{om} vs. R_L
Output Voltage Swing, V_{om} [V_{p-p}]
$V^{\pm}$ = ±15 V
30
20
10
0
100
1k
10k
Load Resistance, R_L [Ω]
I_{CC} vs. $V^{\pm}$
Circuit Current, I_{CC} [mA]
5.0
4.0
3.0
2.0
1.0
0
0
±5
±10
±15
±20
Power Supply Voltage, $V^{\pm}$ [V]
e_n vs. f
Input Equivalent Noise Voltage Density, e_n [nV/√Hz]
$V^{\pm}$ = ±15 V
R_S = 100 Ω
10^4
10^3
10^2
10
1
10
100
1k
10k
100k
Frequency, f [Hz]
Pulse Response
Input Voltage, V_{IN} [V]
Output Voltage, V_O [V]
5
0
-5
5
0
-5
A_V = +1
R_L = 2 kΩ
C_L = 100 pF
$V^{\pm}$ = ±15 V
0
1
2
3
4
Time, t [μs]

USE WITH PRECAUTIONS

- Managing unused circuits
  If there is an unused circuit, the following connection is recommended.

Example of handling unused circuit



Note in this example, an intermediate voltage of V^+ and V^- is applied.

- **Power Supply (Dual Power Supply / Single Power Supply)**

  The op amp operates when a predetermine voltage is applied between $V^+ - V^-$. Therefore, while it operates from a single power supply (V^- = GND), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

- **Ratings of input/output pin voltage**

  When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^-, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

  V_{ICM} (TYP.) : $V^- + 2.3 \sim V^+$ [V] (T_A = 25°C).

  During designing, do include some margin by considering characteristics variation, temperature characteristics etc.

- **Maximum output voltage**

  The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

  V_{om}^+ (TYP.): $V^+ - 1.5$ [V] (T_A = 25°C), V_{om}^- (TYP.): $V^- + 1.5$ [V] (T_A = 25°C)

  During designing, do include some margin by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{om}^+ - V_{om}^-$) will become narrow when the output current increases.

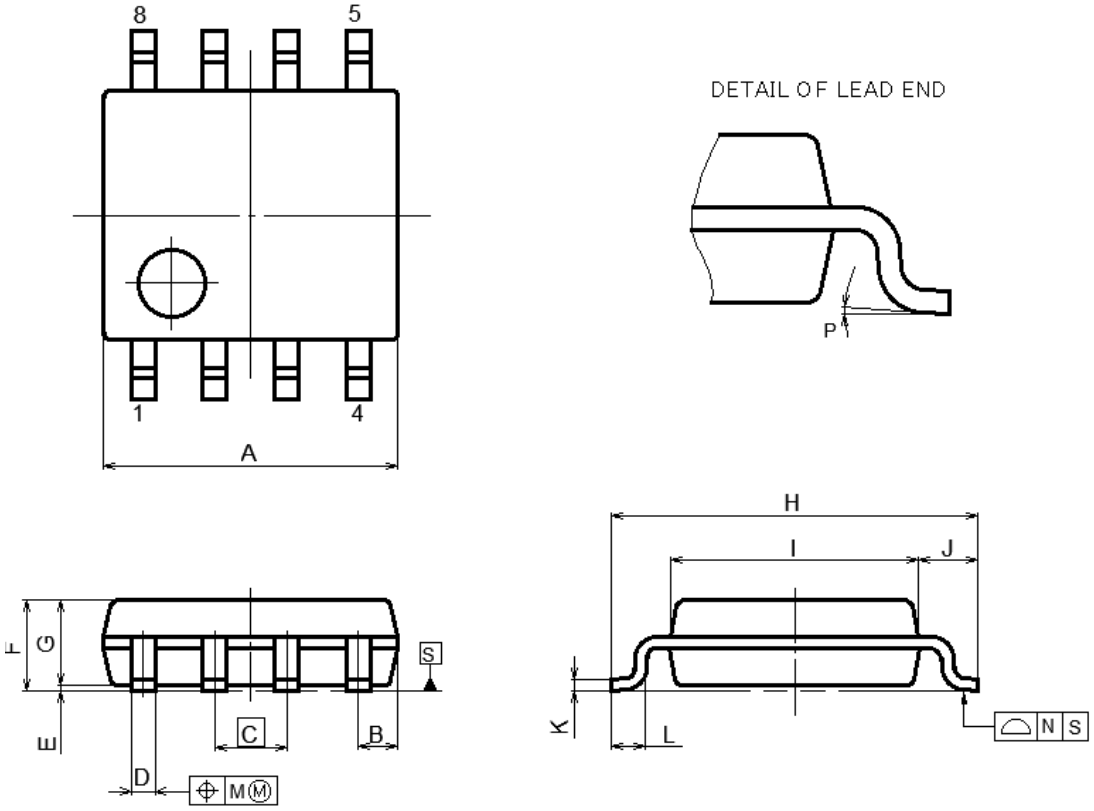
- **Handling of ICs**

  When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP8-4.4×5.2-1.27	PLSP0008DE-A	0.09[g]



NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF
ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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