

TW9990

Low Power NTSC/PAL/SECAM Video Decoder with Differential CVBS Inputs

Features

Video Decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM support with automatic format detection
- Software selectable analog input control allows for combinations of single-ended CVBS, differential CVBS and S-Video
- Built-in analog anti-alias filter
- Two 10-bit ADCs and analog clamping circuit
- Fully programmable static gain or automatic gain control for the Y-channel
- Programmable white peak control for the Y-channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with peaking and CTI
- Digital subcarrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast and sharpness
- Automatic color control and color killer
- Chroma IF compensation
- VBI slicer supporting industrial standard data services
- VBI data passthrough, raw ADC data output
- Programmable output cropping

Digital Output

- 8-bit ITU-R 601 or ITU-R 656 compatible YCbCr (4:2:2) output format

Miscellaneous

- Short-to-Battery Detection test
- Short-to-Ground Detection test
- Two-wire MPU serial bus interface
- Supports real-time control interface
- Power save and power down mode
- Low power consumption
- Single 27MHz crystal for all operations
- Supports 24.54MHz and 29.5MHz crystal for high resolution square pixel format decoding
- 3.3V tolerant I/O
- 1.8V/3.3V power supply
- 32 Ld WFQFN (QFN with wettable flanks)
- AEC-Q100 qualified

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Ordering Information

PART NUMBER (NOTES 2, 3)	PART MARKING	PACKAGE (ROHS COMPLIANT)	PKG. DWG. #
TW9990AT-NA1-GR	TW9990AT NA1-GR	32 Ld WFQFN (bulk tray packaging)	L32.5x5H
TW9990AT-NA1-GRT (Note1)	TW9990AT NA1-GR	32 Ld WFQFN (T&R packaging)	L32.5x5H

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for [TW9990](#). For more information on MSL, please see tech brief [TB363](#).

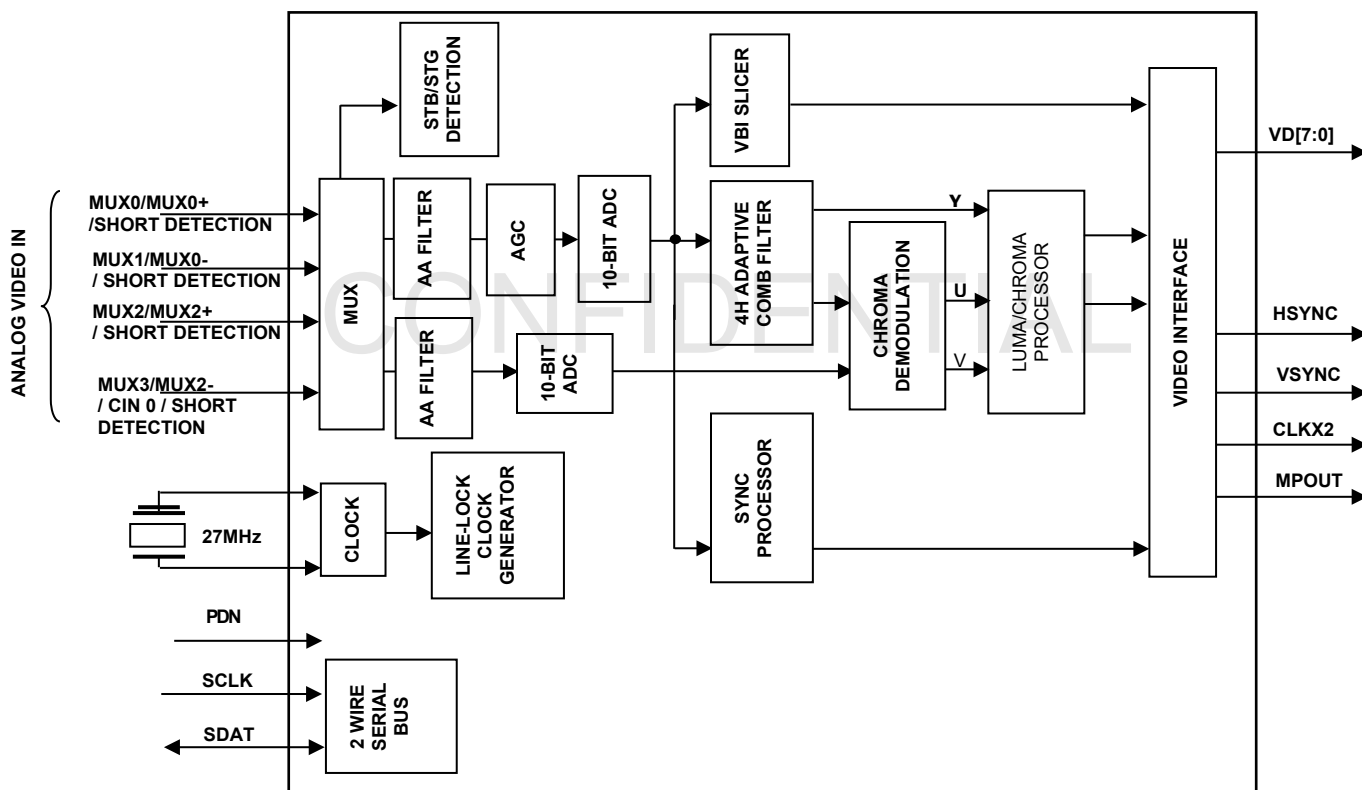
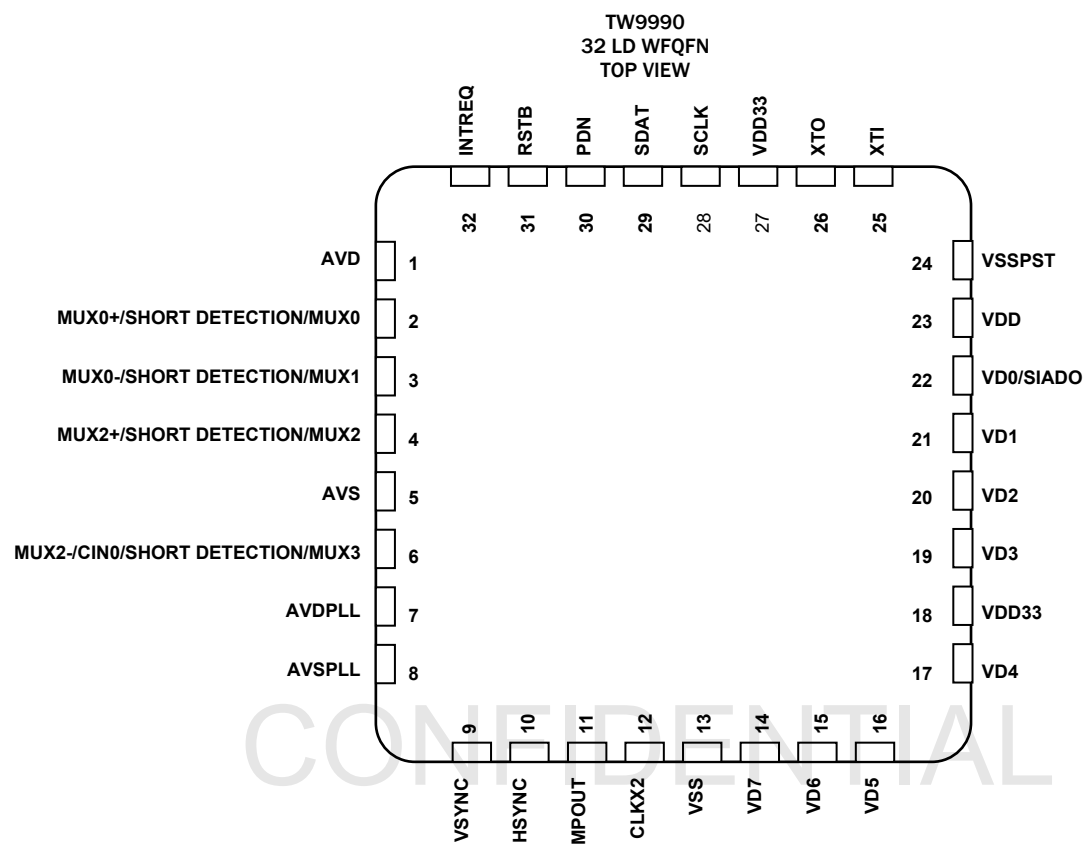


FIGURE 1. TW9990 BLOCK DIAGRAM

Pin Configuration



Pin Descriptions

PIN#	I/O	PIN NAME	DESCRIPTION
ANALOG VIDEO SIGNALS			
2	I	MUX0/MUX0+/ Short Detection	Single-ended Analog CVBS or Y input. For differential CVBS connect positive input. STB/STG detection mode disables pin as a video input. Connect unused input to AGND.
3	I	MUX1/MUX0-/ Short Detection	Single-ended Analog CVBS or Y input. For differential CVBS connect negative input. STB/STG detection mode disables pin as a video input. Connect unused input to AGND.
4	I	MUX2/MUX2+/ Short Detection	Single-ended Analog CVBS or Y input. For differential CVBS connect positive input. STB/STG detection mode disables pin as a video input. Connect unused input to AGND.
6	I	MUX3/ MUX2-/ CIN0/Short Detection	Single-ended Analog CVBS or chroma input. For differential CVBS connect negative input. STB/STG detection mode disables pin as a video input. Connect unused input to AGND.
CLOCK SIGNALS			
25	I	XTI	Clock input. A 27MHz fundamental (or 3rd overtone) crystal or a single-ended oscillator can be connected.
26	O	XTO	Clock output. For connecting a crystal.
HOST INTERFACE			
28	I	SCLK	The MPU Serial interface Clock Line.
29	I/O	SDAT	The MPU Serial interface Data Line.
GENERAL SIGNALS			
31	I	RSTB	Reset input. Low active.
30	I	PDN	Power down control pin. High active.
32	O	INTREQ	Interrupt output signal.
VIDEO OUTPUT SIGNALS			
10	O	HSYNC	Horizontal sync and multi-purpose output pin. See register for control information.
9	O	VSYNC	Vertical Sync and multi-purpose output. See register for control information.
12	O	CLKX2	Data Clock output. See register for control information.
11	O	MPOUT	Multi-purpose output pin. The output function can be selected by RTSEL of register 0x19
14 15 16 17 19 20 21	I/O	VD[7:1]	Digitized video data output of 4:2:2 YCbCr. VD[7] is the MSB.
22	I/O	VD[0] / SIADO	LSB of digitized video data output of 4:2:2 YCbCr. SIADO: The MPU interface address select pin 0. A pull-up or pull-down resistor is needed to select one of the two addresses that the chip will respond.

Pin Descriptions (continued)

PIN#	I/O	PIN NAME	DESCRIPTION
POWER AND GROUND PINS			
23	I	VDD	1.8V digital core power.
13	I	VSS	1.8V digital core return
18 27	I	VDD33	3.3V digital I/O power.
24	I	VSSPST	3.3V digital I/O return
1	I	AVD	1.8V analog ADC supply
5	I	AVS	1.8V analog ADC return
7	I	AVDPLL	1.8V PLL supply
8	I	AVSPLL	1.8V PLL return

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Functional Description

Introduction

The TW9990 is a low power NTSC/PAL/SECAM video decoder chip that is designed for automotive applications. It supports both single-ended and differential composite video as well as S-Video. Typical power consumption is 110mW for composite input applications, and the available power-down mode further reduces power consumption. It uses 1.8V for both analog and digital supply voltage and 3.3V for I/O power. A single 27MHz crystal is all that is needed to decode all analog video standards.

The video decoder converts base-band analog CVBS or S-Video signals into digital 8-bit 4:2:2 YCbCr video output format. It consists of an analog front-end with input source selection, variable gain amplifier, analog-to-digital converters, a Y/C separation circuit, a multistandard color decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC 4.43 and SECAM), and synchronization circuitry. The Y/C separation is done with a high quality adaptive 4H comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard and weak signals. The output of the decoder is line-locked and formatted to the ITU-R 656 output standard with embedded sync.

The TW9990 also includes circuits to detect and process Vertical Blanking Interval (VBI) signals. It slices and processes VBI data for output through the video bus. Some information can also be retrieved through the host interface.

A 2-wire serial host interface is used to simplify system integration and all functions can be controlled through this interface.

Analog Front-End

The analog front-end preprocesses and digitizes the AC-coupled analog signal for further processing. All channels have built-in anti-alias filters and 10-bit high speed over-sampling ADCs. The characteristics of the filter are available in the [“Filter Curves on page 29”](#). There is a 4-input multiplexer and a variable gain amplifier for automatic gain control (AGC on the Y-channel). All channels have a built-in variable gain amplifier that can be individually programmed. The Y-channel gain can be automatically controlled in decoder mode if enabled. It can support a maximum input voltage range of 1.4V without attenuation. All channels also have a clamping circuit that restores the proper DC level through manual or automatic control. Software selectable analog inputs allow for the following input combinations:

- Four selectable single-ended composite video inputs
- Two selectable single-ended composite video inputs and one S-video input
- One differential composite video input and two single-ended composite video inputs
- One differential composite video input and one S-video input
- Two differential composite video inputs

Sync Processor

The sync processor of TW9990 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video signal. The processor contains a digital phase-locked loop and decision logic to achieve reliable sync detection in stable signals as well as in unstable signals such as those from VCR fast forward or rewind. It allows sampling of the video signal in line-locked fashion.

Y/C Separation

For NTSC and PAL standard signals in decoder mode, the luma/chroma separation can be done either by adaptive comb filtering or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the [“Filter Curves on page 29”](#).

TW9990 employs a high quality 4-H adaptive comb filter to reduce artifacts such as hanging dots and crawling dots. Due to the line buffer used in the comb filter, there is always a two line processing delay in the output images no matter what standard or filter option is chosen.

Color Demodulation

The color demodulation of NTSC and PAL signals are done by first quadrature down mixing and then low-pass filtering. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM decoding process consists of FM demodulation and de-emphasis filtering. During FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The subcarrier signal for use in the color demodulator is generated by a direct digital synthesis PLL that locks onto the input subcarrier reference (color burst). This arrangement allows any substandard signal of NTSC and PAL to be demodulated easily with a single crystal frequency.

AUTOMATIC CHROMA GAIN CONTROL

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in the video signal. The range of ACC control is -6db to +26db.

COLOR KILLER

For low color amplitude signals, black and white video, or very noisy signals, the color will be “killed”. The color killer uses the burst amplitude measurement as well as the subcarrier PLL status to switch-off the color.

AUTOMATIC STANDARD DETECTION

The TW9990 has built-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Any of these standards can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW9990 supports all common video formats as shown in [Table 1 on page 10](#). The video decoder needs to be programmed appropriately for each of the composite video input format.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW9990

FORMAT	LINES	FIELDS	FSC (MHz)	COUNTRY
NTSC-M	525	60	3.579545	U.S., many others
NTSC-Japan (Note 4)	525	60	3.579545	Japan
PAL-B, G, N	625	50	4.433619	Many
PAL-D	625	50	4.433619	China
PAL-H	625	50	4.433619	Belgium
PAL-I	625	50	4.433619	Great Britain, others
PAL-M	525	60	3.575612	Brazil
PAL-CN	625	50	3.582056	Argentina
SECAM	625	50	4.406, 4.250	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619	China
NTSC (4.43)	525	60	4.433619	Transcoding
NTSC 50	625	50	3.579545	

Note:

4. NTSC-Japan has 0 IRE setup.

Component Processing

The TW9990 supports brightness, contrast, color saturation and Hue adjustment for changing the video characteristic. The Cb and Cr gain can be adjusted independently for flexibility.

SHARPNESS

The TW9990 also provides a sharpness control function through control registers. It provides control up to +9dB. The center frequency of the enhancement curve is selectable. A coring function is provided to prevent noise enhancement.

COLOR TRANSIENT IMPROVEMENT

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low level noise enhancement can be suppressed by programmable coring logic. Overshoot and undershoot are also removed by a special circuit to prevent false color generation at the color edge.

Short Detection

TW9990 provides a Short-to-Battery (STB) and Short-to-Ground (STG) detection capability. The short diagnostics module has 2 channels: A and B. Each channel is completely independent and may be assigned to any of the 4 analog input pin, therefore, any of the 4 analog video input pins can be configured to act as a short detection input instead of as a video input. Both STB and STG support a 4 step programmable threshold level (2 bits per threshold). The short-to-ground thresholds range from 5/16, 3/16, 2/16 and 1/16 of the 3.3V power supply. The short-to-battery thresholds range from 7/8, 5/8, 3/8 and 1/8 of the 3.3V power supply. A short event can be detected by either polling registers or by using the interrupt pin.

Power Management

The TW9990 can be put into power-down mode through both software and hardware control. The Y and C path can be powered down separately.

Host Interface

The TW9990 registers are accessed via a 2-wire serial MPU interface. It operates as a slave device. Serial clock and data lines, SCLK and SDAT, transfer data from the bus master at a rate of 400kbits/s. The TW9990 has one serial interface address select pin (VD[0]/SIAD0) to program up to two unique serial addresses. This allows as many as two TW9990 to share the same serial bus. Reset signals are also available to reset the control registers to their default values.

Cropping

Cropping allows only a subsection of a video image to be output. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of the VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from the vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and locations of the active video are determined by the HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits are, respectively: HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bits share the same register CROP_HI.

In order for the cropping to work properly, the following equation should be satisfied.

$HDELAY + HACTIVE < \text{Total number of pixels per line.}$

$VDELAY + VACTIVE < \text{Total number of lines per field}$

[Table 2](#) shows some popular video formats and its recommended register settings. The CCIR601 format refers to the sampling rate of 13.5MHz. The SQ format for 60Hz system refers to the sampling rate of 12.27MHz, and the SQ format for 50Hz system refers to the use of a sampling rate of 14.75MHz.

TABLE 2. SOME POPULAR VIDEO FORMATS

SCALING RATIO	FORMAT	TOTAL RESOLUTION	OUTPUT RESOLUTION
1:1	NTSC SQ	780x525	640x480
	NTSC CCIR601	858x525	720x480
	PAL SQ	944x625	768x576
	PAL CCIR601	864x625	720x576

Output Interface

ITU-R BT.656

ITU-R BT.656 defines strict EAV/SAV Code, video data output timing, H blanking timing and V Blanking timing. In this mode, VD[7:0] are the only effective pins and CLK0 pin should be used for the data clock signal. EAV/SAV Code format is shown in [Table 3](#). Bit 7 of the forth byte in EAV/SAV code must be “1” in ITU-R BT.656 standard.

TABLE 3. ITU-R BT.656 SAV AND EAV CODE SEQUENCE

	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0
1ST BYTE	1	1	1	1	1	1	1	1
2ND BYTE	0	0	0	0	0	0	0	0
3RD BYTE	0	0	0	0	0	0	0	0
4TH BYTE	1	F	V	H	V XOR H	F XOR H	F XOR V	F XOR V XOR H

For complete ITU-R BT.656 standard, following setting shown in [Table 4](#) is recommended.

TABLE 4. ITU-R BT.656 REGISTER SET UP

REGISTER	525 LINE SYSTEM	625 LINE SYSTEM
VDELAY	0x012	0x018
VACTIVE	0x0F4	0x120
HACTIVE	0x2D0	0x2D0
NTSC656	1	0

ITU-R BT.656 for 525-line system has 244 video active lines in odd field and 243 vide active lines in even field. NTSC656 register bit controls this video active line length.

CONTROL SIGNALS

TW9990 outputs several control signals. VSYNC is vertical timing control signals. HSYNC is horizontal timing control signals.

VERTICAL TIMING DIAGRAM

[Figure 3](#) shows typical vertical timing for 60Hz/525 lines system. [Figure 2](#) shows typical vertical timing for 50Hz/625 lines system. In [Figure 3](#), VDELAY register is 19 decimal(0x13) and VACTIVE register is 241 decimal(0x0F1). [Figure 3](#) shows typical NTSC-M setting. In [Figure 2](#), VDELAY register is 24 decimal (0x18) and VACTIVE register is 286 decimal (0x11E). [Figure 2](#) shows typical PAL-B setting. The leading edge of VACTIVE is controlled by VDELAY register value. The length of video active lines is controlled by VACTIVE register value. As shown in [Figure 2](#) and [Figure 3](#), output video data stream has 2 lines vertical delay compared to input VIDEO line timing.

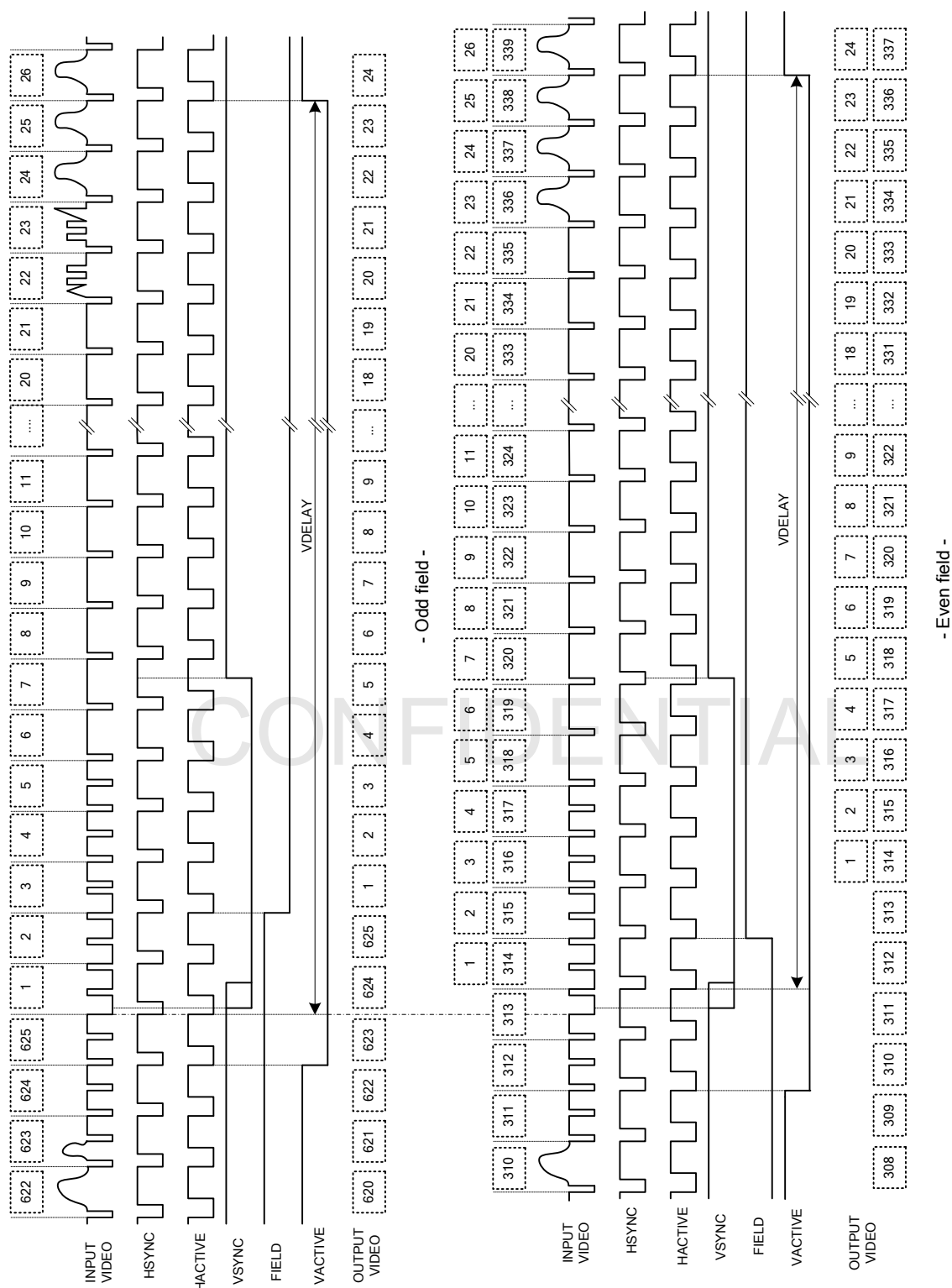


FIGURE 2. VERTICAL TIMING DIAGRAM FOR 50HZ/625 LINE SYSTEM

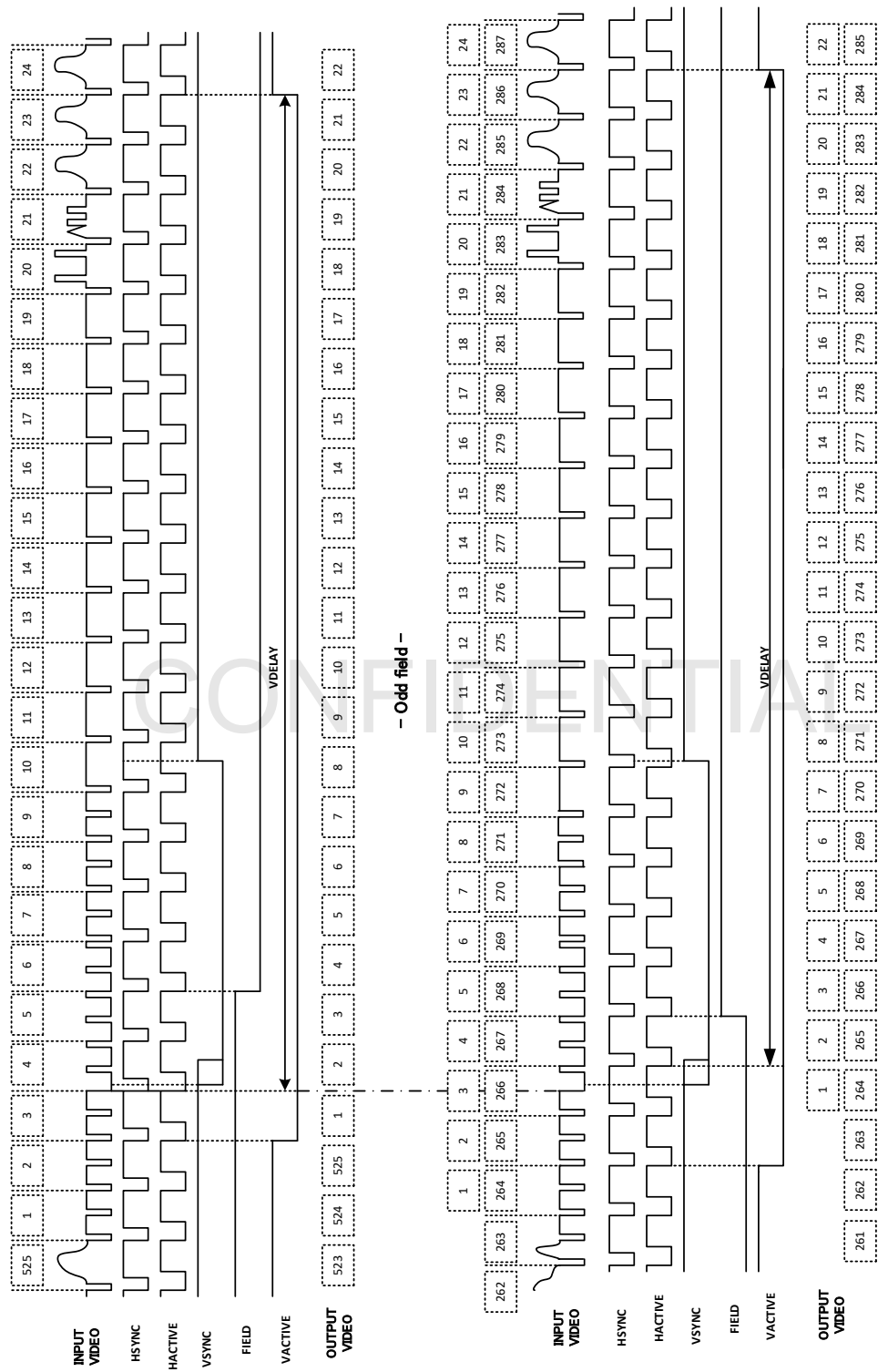


FIGURE 3. VERTICAL TIMING DIAGRAM FOR 60HZ/525 LINE SYSTEM

HSYNC

The leading edge of the HSYNC signal is synchronized to input Video horizontal sync timing. The start position of the HSYNC signal is programmable by the HSBEGIN register. The end position of the HSYNC signal is also programmable by the HSEND registers.

VSYNC

The leading edge of the VSYNC signal is synchronized to vertical sync pulse of input Video. The leading edge position of the VSYNC signal is programmable by the OVSDLY register on a per clkx2 clock basis. The trailing edge of the VSYNC signal is in the middle of the HSYNC "1" period in the odd field and in the middle of the HSYNC "0" period in the even field. The trailing edge of the VSYNC changes on line 10 in 525 lines system and on line 7 in 625-line system as the default. This line number is programmable by the OVSEND register on a per line basis.

FIELD

The FIELD signal can be output on the MPOUT pin if the RTSEL register selects FIELD output. [Figure 2](#) and [Figure 3](#) show the field signal output assuming default OFDLY register 2H. The line output timing of the FIELD signal is programmable by the OFDLY register value (1H to 6H). The default FIELD signal shows the ITU-R BT.656 field timing in the 656 output stream by the OFDLY register 2H.

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VBI Data Processing

RAW VBI DATA OUTPUT

TW9990 supports raw VBI data output. Raw VBI data output has the same vertical line delay timing as video output. Horizontal output timing is also programmable by VBIDELAY register. Raw VBI data is generated during HACTIVE active period (from SAV to EAV) as Video data output. Total pixel number of raw VBI data per line is twice as many as HACTIVE register value. If VBI EN register is set to "1", all vertical blanking output while VACTIVE is inactive will be raw VBI data output. If VVBI registers are set to more than "1", the VVBI number lines from top video active lines will also be raw VBI data output lines.

VBI DATA SLICER

The following VBI standards are supported by VBI Data slicer. The VBI Data slicing is controlled by the registers LCTL6 to LCTL26. Registers LCTL6 to LCTL26 are controlling the slicing process itself. LCTL6 to LCTL26 defines the Data Type to be decoded. The Data Type can be specified on a line by line basis for line6 to line26 and for even and odd field depending on the detected TV system standard. The setting for LCTL26 is valid for the rest of the corresponding field. Normally no text data 0H (video data) should be selected to render the VBI Data slicer inactive during active video. LCTRL26 is useful for Full-Field Teletext mode in the case of NABTS.

NABTS is 525 Teletext-C. Japan's MOJI is 525 Teletext-D. Didon Antiope is 625 Teletext-A. VBI Data slicer supports up to Physical layer, Link layer in ITU-R BT.653-2. Japan's EIAJ CPR-1204 shown as 525 WSS has the same physical layer protocol as that of CGMS.

The sliced VBI data is embedded in the ITU-R BT.656 output stream, using the intervals between the End of Active Video (EAV) and the Start of Active Vide(SAV) codes of each line and formatted according to ITU-R BT.1364 Ancillary data packet Type 2.

TABLE 5. VBI STANDARD

STANDARD TYPE	TV SYSTEMS (LINES/FREQ)	BIT RATE (MBITS/S)	MODULATION	DATA TYPE
625 Teletext-B	625/50	6.9375	NRZ	1H
525 Teletext-B	525/60	5.727272	NRZ	1H
625 Teletext-C	625/50	5.734375	NRZ	2H
525 Teletext-C	525/60	5.727272	NRZ	2H
625 Teletext-D	625/50	5.6427875	NRZ	3H
525 Teletext-D	525/60	5.727272	NRZ	3H
625 CC	625/50	0.500	NRZ	4H
525 CC	525/60	0.503	NRZ	4H
625 WSS	626/50	5	Bi-phase	5H
525 WSS(CGMS)	525/60	0.447443	NRZ	5H
625 VITC	625/50	1.8125	NRZ	6H
525 VITC	525/60	1.7898	NRZ	6H
Gemstar 2x	525/60	1.007	NRZ	7H
Gemstar 1x	525/60	0.503	NRZ	8H
VPS	625/50	5	Bi-phase	9H
625 Teletext-A	625/50	6.203125	NRZ	AH

SLICED VBI DATA OUTPUT FORMAT

After 4 bytes of EAV code, sliced VBI ANC data packets are generated by following format. Byte1 to Byte4N+7 data stream is formatted according to ITU-R BT.1364 ANC data packet Type 2. BC data byte is optional and not included in ANC data packet Type 2 BC data byte is inserted after ANC data packet Type 2.

TABLE 6. SLICED VBI ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	NEP	EP	DC5	DC4	DC3	DC2	DC1	DC0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	DT3	DT2	DT1	DT0	IDI2. UDW 2
9	Sliced VBI Data byte 1								Sliced VBI Data No.1. UDW3
10	Sliced VBI Data byte 2								Sliced VBI Data No.2. UDW4
11	Sliced VBI Data byte 3								Sliced VBI Data No.3. UDW5
12	Sliced VBI Data byte 4								Sliced VBI Data No.4. UDW6
13	Sliced VBI Data byte 5								Sliced VBI Data No.5. UDW7
.									
.									
4N+6	Sliced VBI Data byte last or FILLDATA								Sliced VBI Data Last or FILLDATA. UDW 4N
4N+7	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
4N+8	OP	0	BC5	BC4	BC3	BC2	BC1	BC0	BC

NOTES:

5. EP is Even Parity of bits 5 to 0 in same 1 byte.
6. NEP is inverted EP in same 1 byte.
7. {DID4, DID3, DID2, DID1, DID0} is DID register value.
8. {SDID5, SDID4, SDID3, SDID2, SDID1, SDID0} is SDID register value.
9. {DC5, DC4, DC3, DC2, DC1, DC0} is the number of DOWRD data length from UDW1 to UDW4N. {DC5, DC4, DC3, DC2, DC1, DC0} is N (decimal).
10. OP is Odd Parity of bits 6 to 0 in same 1 byte.
11. FID=0: odd field; FID=1: even field.
12. {LN8, LN7, LN6, LN5, LN4, LN3, LN2, LN1, LN0} is the line number of current sliced VBI data.
13. {DT3, DT2, DT1, DT0} is the Data Type shown on Table
14. NCS6 is inverted CS6.
15. {CS6, CS5, CS4, CS3, CS2, CS1, CS0} is the checksum value calculated from DID to UDW4N.
16. UDW1 to UDW4N are the User data words (UDW) shown on ITU-R BT.1364 ANC data packet Type 2.
17. {BC5, BC4, BC3, BC2, BC1, BC0} is the number of valid bytes from UDW1 to UDW4N.
18. FILLDATA is FILLDATA register value. FILLDATA is inserted after last valid bytes to make 4N number byte stream sometimes.

Table 7 through Table 18 shows various types of ANC data packets to be output.

TABLE 7. CLOSED CAPTIONING ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

TABLE 8. CGMS ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3		D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0		0	0	0	Ancillary dataflag
2	1	1	1	1	1		1	1	1	
3	1	1	1	1	1		1	1	1	
4	NEP	EP	0	DID4	DID3		DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3		SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0		0	1	0	DC
7	OP	FID	LN8	LN7	LN6		LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0		1	0	1	IDI2. UDW 2
9		WSS[7:0]								UDW3
10		WSS[7:0]								UDW4
11		{0H,WSS[19:16]}								UDW5
12		CRCERRORCODE								UDW6
13		FILLDATA								UDW7
14		FILLDATA								UDW8
15	NCS6	CS6	CS5	CS4	CS3		CS2	CS1	CS0	CS
16	1	0	0	0	0		1	1	0	BC

Note:

19. CRCERRORCODE is optional byte. 41H means "this wss data has CRC Error". 80H means no CRC error.

TABLE 9. 625 LINE WIDE SCREEN SIGNALING ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	1	IDI2. UDW 2
9	WSS[7:0]								UDW3
10	{00b,WSS[13:8]}								UDW4
12	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
13	0	0	0	0	0	1	0	0	BC

TABLE 10. 625 TELETEXT-A ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	1	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
46	BYTE40								UDW40
47	HAMM84ERROR								UDW41
48	FILLDATA								UDW42
49	FILLDATA								UDW43
50	FILLDATA								UDW44
51	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
52	0	0	1	0	1	0	0	1	BC

NOTES:

20. FRAME CODE is E7H if it's received correctly.
 21. HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet, 80H means no 8/4 Hamming error.

TABLE 11. 625 TELETEXT-B ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	1	0	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
50	BYTE44								UDW44
51	BYTE45								UDW45
52	HAMM84ERROR								UDW46
53	FILLDATA								UDW47
54	FILLDATA								UDW48
55	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
56	1	0	1	0	1	1	1	0	BC

NOTES:

22. FRAME CODE is 27H if it is received correctly.
 23. HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet, 80H means no 8/4 Hamming error.

TABLE 12. 525 TELETEXT-B ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
30	BYTE36								UDW36
31	BYTE37								UDW37
32	HAMM84ERROR								UDW38
33	FILLDATA								UDW39
34	FILLDATA								UDW40
35	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
36	1	0	1	0	0	1	1	0	BC

NOTES:

24. FRAME CODE is 27H if it's received correctly.
 25. HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet, 80H means no 8/4 Hamming error.

TABLE 13. 625 TELETEXT-C AND 525 TELETEXT-C ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	HAMM84ERROR								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

NOTES:

26. FRAME CODE is E7H if it's received correctly.
 27. HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet, 80H means no 8/4 Hamming error.

TABLE 14. 625 TELETEXT-D AND 525 TELETEXT-D ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	1	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	BYTE37								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

Note:

28. FRAME CODE is A7H if it's received correctly.

TABLE 15. LINE16 VPS ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	1	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	1	IDI2. UDW 2
9	START CDDE1(51H)								UDW3
10	START CODE2(99H)								UDW4
11	BYTE3								UDW5
.	.								
.	.								
22	BYTE14								UDW16
23	BYTE15								UDW17
24	BI-PHASEERROR								UDW18
25	FILLDATA								UDW19
26	FILLDATA								UDW20
27	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
28	1	0	0	1	0	0	1	0	BC

NOTES:

29. START CODE1 is the first byte of Start Code by 5Mbps slicing.
30. START CODE2 is the second byte of Start Code by 5Mbps slicing.
31. BYTE3~BYTE15 are data bytes by 5/2 Mbps Bi-phase slicing.
32. BI-PHASEERROR is Bi-phase coding error detection. 80H means No error. 41H means Bi-phase coding error is detected.

TABLE 16. VITC ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	0	IDI2. UDW 2
9	Bit[9:2]								UDW3
10	Bit[19:12]								UDW4
11	Bit[29:22]								UDW5
12	.Bit[39:32]								UDW6
13	.Bit[49:42]								UDW7
14	Bit[59:52]								UDW8
15	Bit[69:62]								UDW9
16	Bit[79:72]								UDW10
17	Bit[89:82]								UDW11
18	CRCERROR								UDW12
19	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
20	1	0	0	0	1	1	0	0	BC

Note:

33. CRCERROR is CRC Error information. 41H means CRC Error is detected. 80H means no CRC error.

TABLE 17. GEMSTAR 1X ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

TABLE 18. GEMSTAR 2X ANC DATA PACKET

BYTE NO.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	1	IDI2. UDW 2
9	FRAMECODE1								UDW3
10	FRAMECODE2								UDW4
11	Data Byte 1								UDW5
12	Data Byte 2								UDW6
13	Data Byte 3								UDW7
14	Data Byte 4								UDW8
15	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
16	0	0	0	0	1	0	0	0	BC

NOTES:

34. FRAMCODE1 is B9H if Frame Code is correctly received.

35. FRAMCODE2 is 05H if Frame Code is correctly received.

VBI CONTROL REGISTERS

PDNSVBI=1 makes VBI slicer function enable. ANCEN=1 makes VBI ANC data output enable. HAMM84=1 makes 8/4Hamming code decoding enable in 8/4 Hamming codes data on Teletext ANC data output. At this time, received 7-0 8-bit data is converted to 3-0 4-bit nibble data with 7-4 bits fixed to 0h. 3-0 4bits has meanings in this HAMM84=1 mode. Typical LCTLn register setting for WSS and CCF1/CCF2 are as follows.

NTSC-M	PAL/SECAM
LCTL20=0x55	LCTL22=0x44
LCTL21=0x44	LCTL23=0x50

Typical European 625-Line Teletext-B settings are as follows.

LCTL6 =0x11	LCTL7 =0x11	LCTL8 =0x11	LCTL9 =0x11	LCTL10=0x11
LCTL11=0x11	LCTL12=0x11	LCTL13=0x11	LCTL14=0x11	LCTL15=0x11
LCTL16=0x11	LCTL17=0x00	LCTL18=0x00	LCTL19=0x00	LCTL20=0x11
LCTL21=0x11	LCTL22=0x11	LCTL23=0x50	LCTL24=0x00	LCTL25=0x00
LCTL26=0x00				

VBI RECEIVED DATA REGISTERS

TW9990 supports two type VBI received data registers. CCF1DATA1/CCF1DATA2 registers contain Field 1 Closed Captioning data. CCF2DATA1/CCF2DATA2 registers contain Field 2 Closed Captioning data(EDS data). WSS registers contain 20-bit CGMS(WSS) data for NTSC or 14-bit WSS data for PAL. [Figure 4](#) shows typical access flow of VBI Received Data Registers.

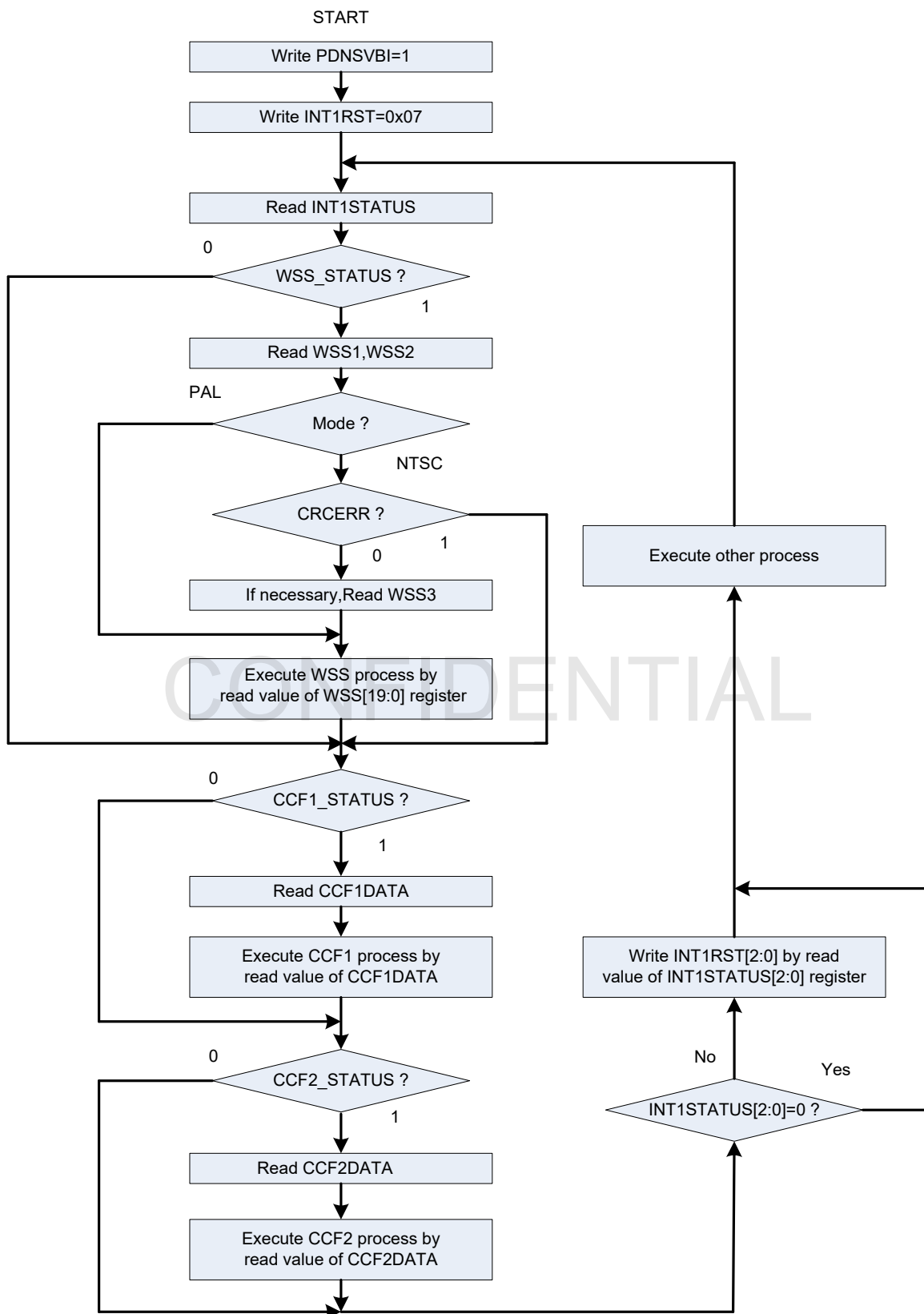


FIGURE 4. VBI RECEIVED DATA REGISTER ACCESS

Two-Wire Serial Bus Interface

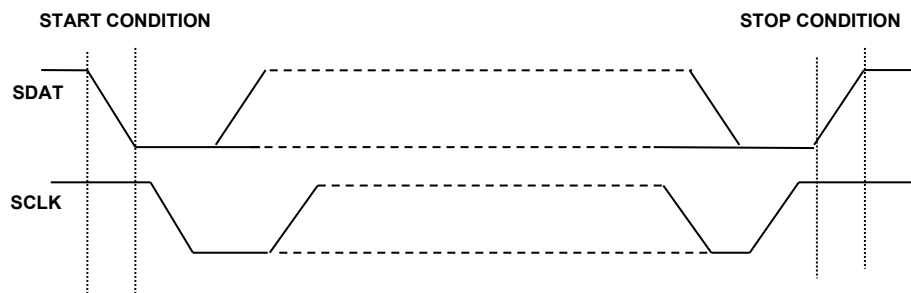


FIGURE 5. DEFINITION OF THE SERIAL BUS INTERFACE BUS START AND STOP

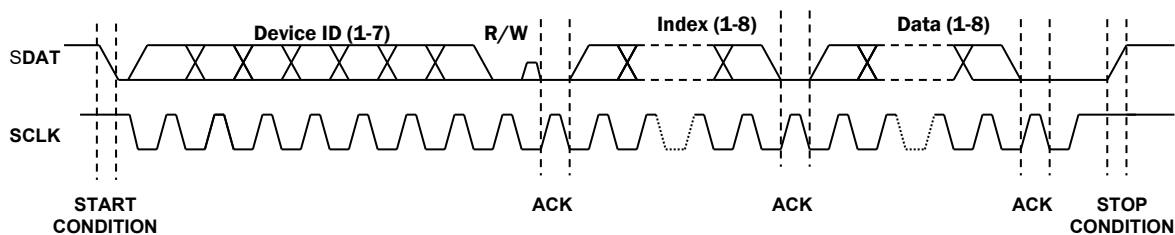


FIGURE 6. ONE COMPLETE REGISTER WRITE SEQUENCE VIA THE SERIAL BUS INTERFACE

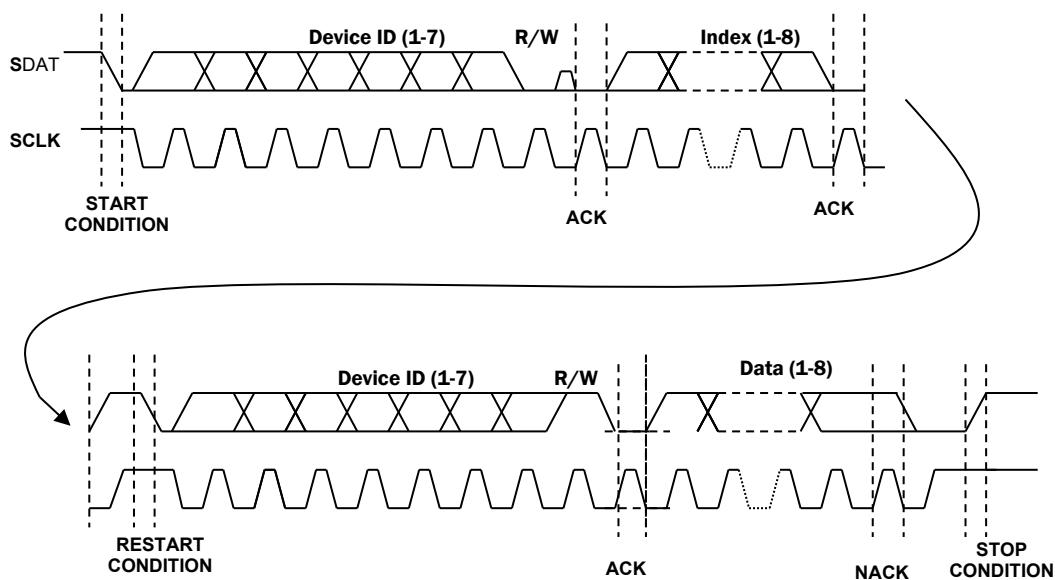


FIGURE 7. ONE COMPLETE REGISTER READ SEQUENCE VIA THE SERIAL BUS INTERFACE

TABLE 19. TW9990 SERIAL BUS INTERFACE 7-BIT SLAVE ADDRESS AND READ WRITE BIT

SERIAL BUS INTERFACE 7-BIT SLAVE ADDRESS							READ/WRITE BIT
1	0	0	0	1	0	SIAD	1 = Read 0 = Write

The two-wire serial bus interface is used to allow an external microcontroller to write control data to, and read control or other information from the TW9990 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDD33. ICs communicate on the bus by pulling SCLK and SDAT low through open-drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW9990 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD (Serial Interface Address) pin to either VDD33 or VSS33 (see [Table 19](#)) through a pull-up or pull-down resistor. If the SIAD pin is tied to VDD33, then the least significant bit of the 7-bit address is a "1". If the SIAD pin is tied to VSS33 then the least significant bit of the 7-bit address is a "0". The most significant 6-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high, the next byte will be read from the slave device. If it is low, the next byte will be write to the slave. When a bus master (the host microprocessor) drives SDAT from HIGH to LOW, while SCLK is high, this is defined to be a start condition (see [Figure 5](#)). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in [Figure 6](#). (For the TW9990, the next byte is normally the index to the TW9990 registers and is a write to the TW9990 therefore the first R/W bit is normally low.)

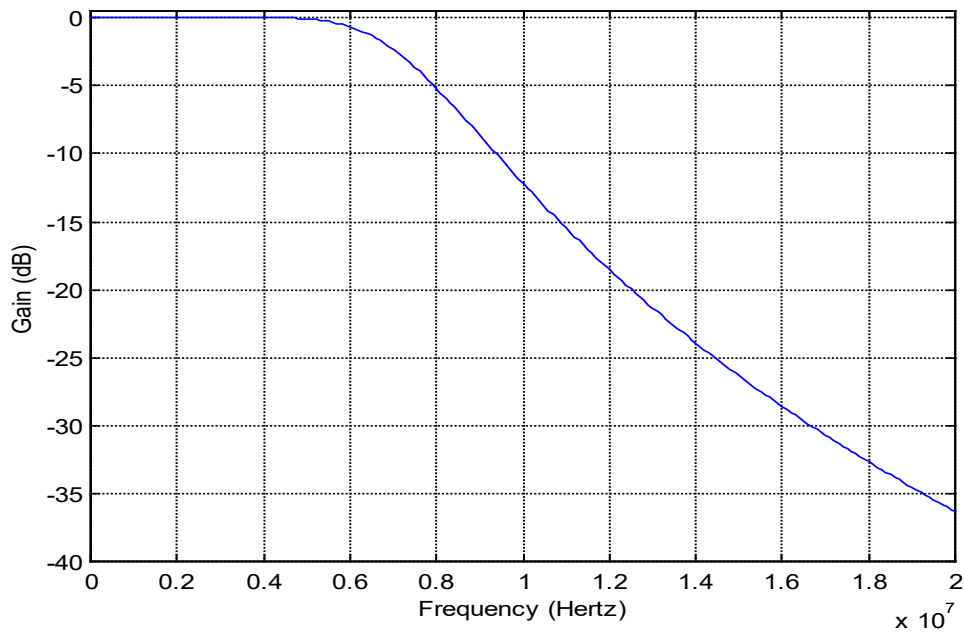
After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of the TW9990, the master sends another 8-bits of data, the TW9990 loads this to the register pointed by the internal index register. The TW9990 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW9990 if they are in ascending sequential order. After each 8-bit transfer, the TW9990 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW9990 the host will issue a stop condition.

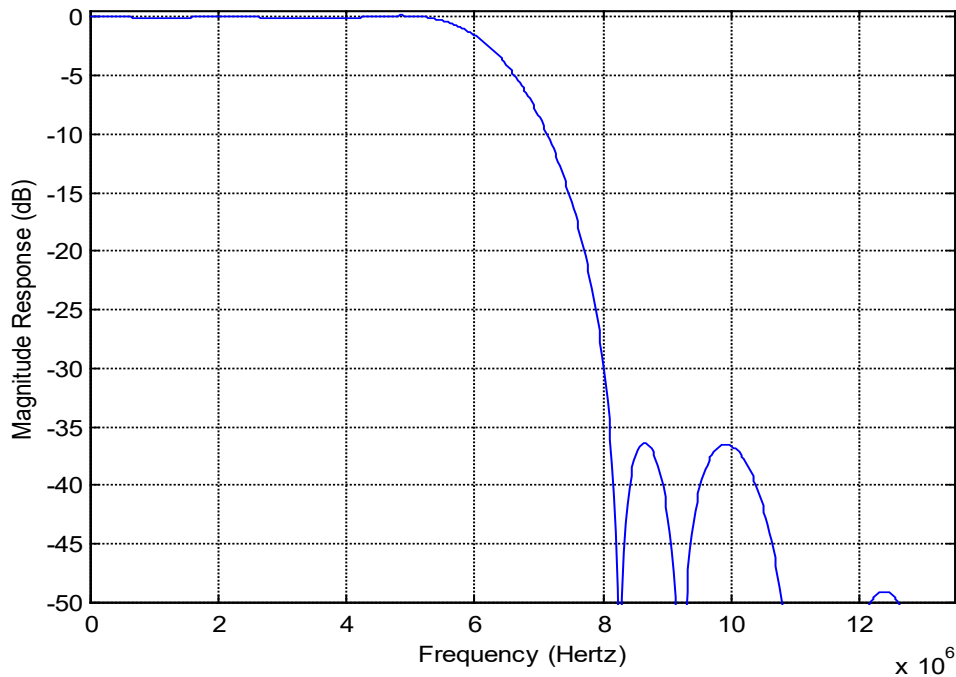
A TW9990 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. See [Figure 7](#). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases, the master takes control of the SDAT line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

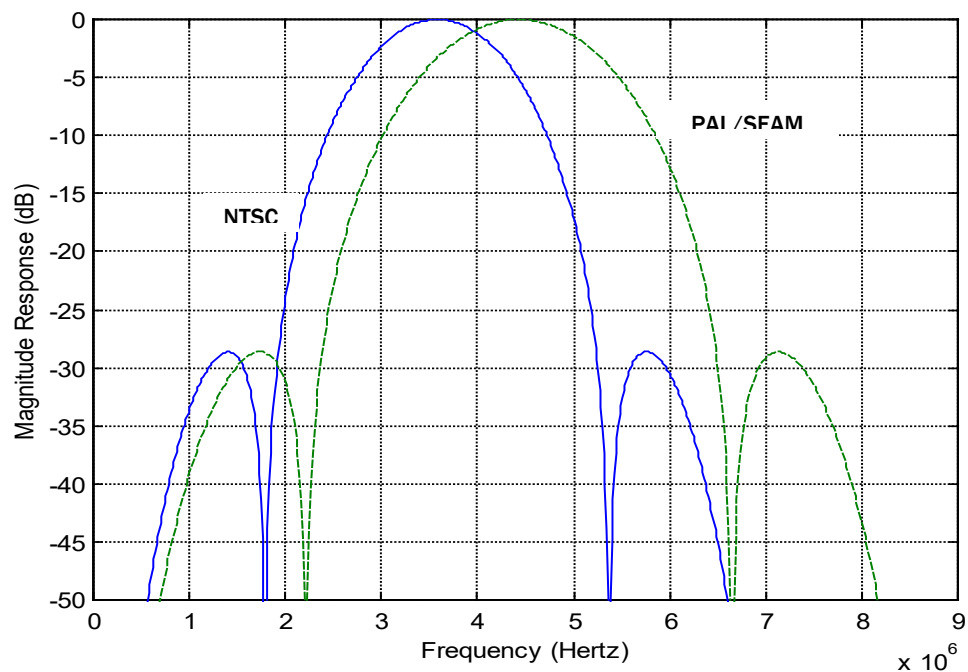
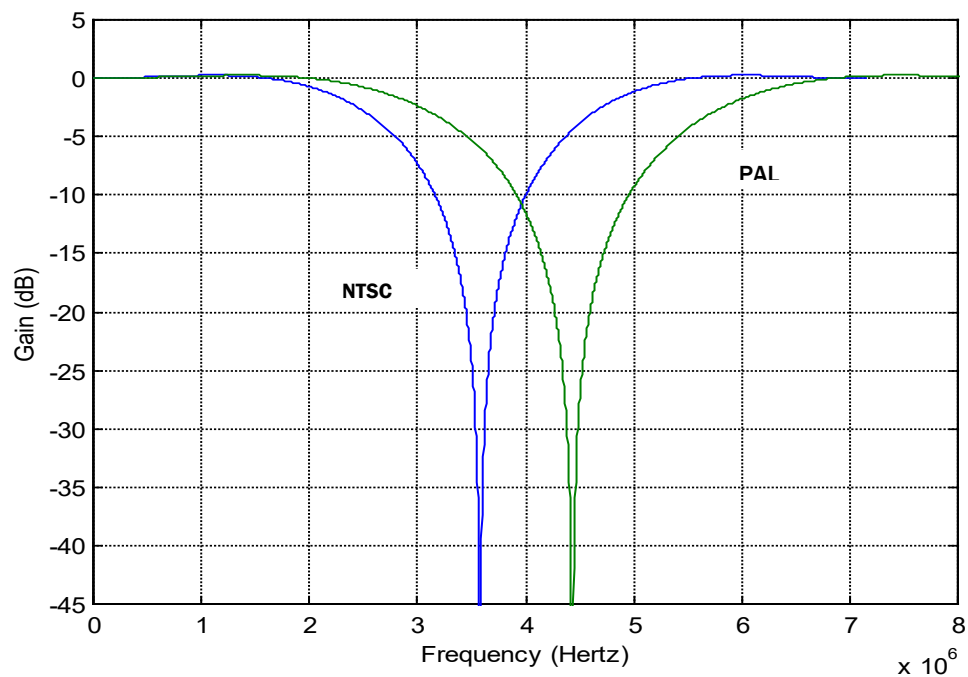
Filter Curves

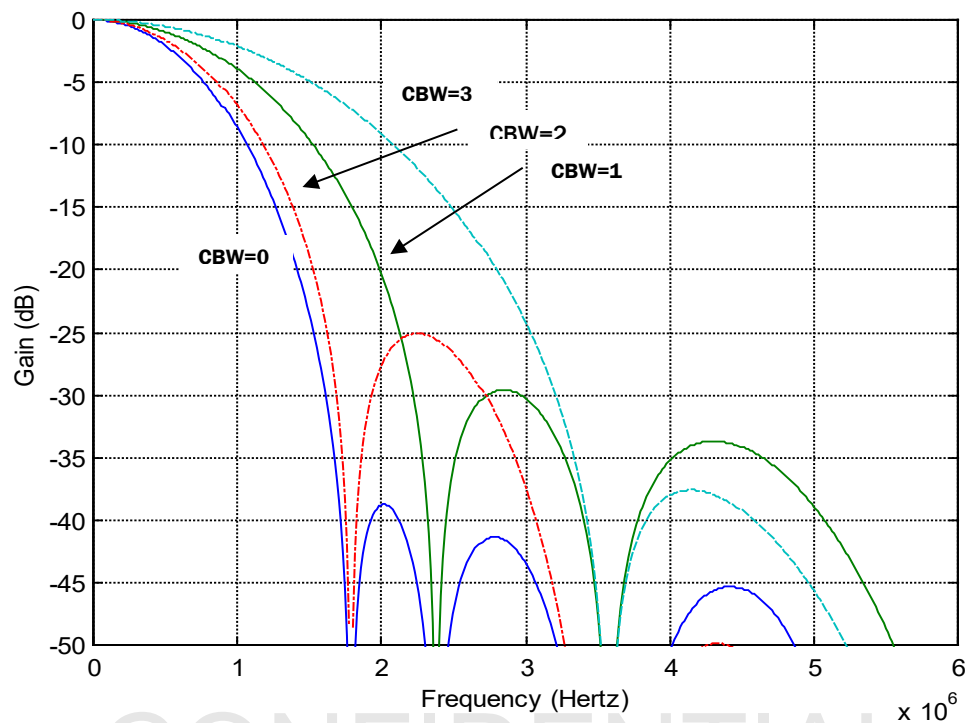
ANTI-ALIAS FILTER



DECIMATION FILTER



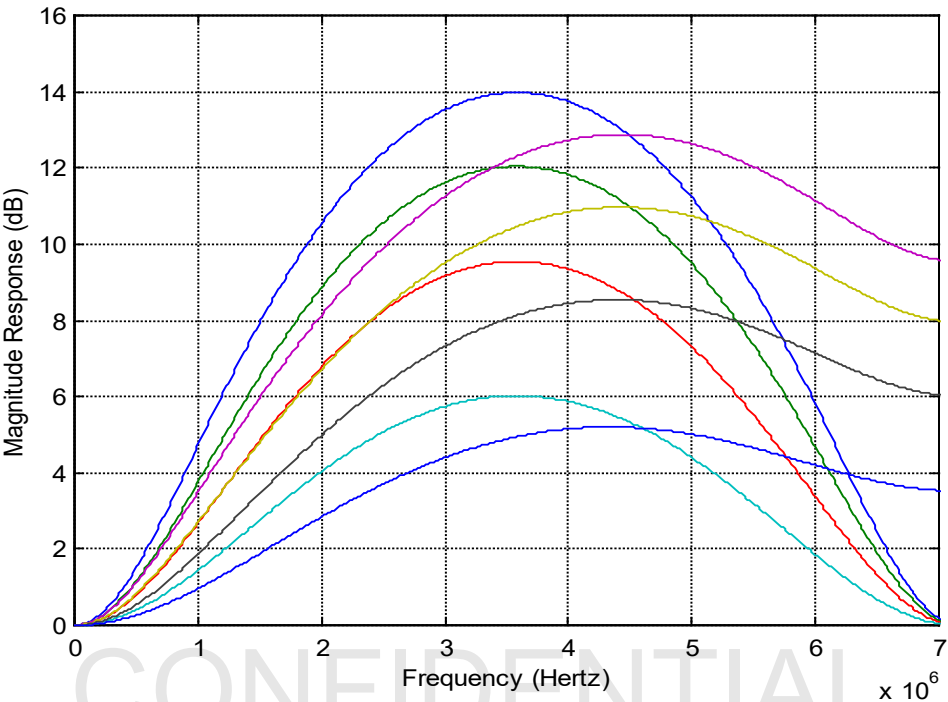
CHROMA BAND PASS FILTER CURVES**LUMA NOTCH FILTER CURVE FOR NTSC AND PAL/SECAM**

CHROMINANCE LOW-PASS FILTER CURVE

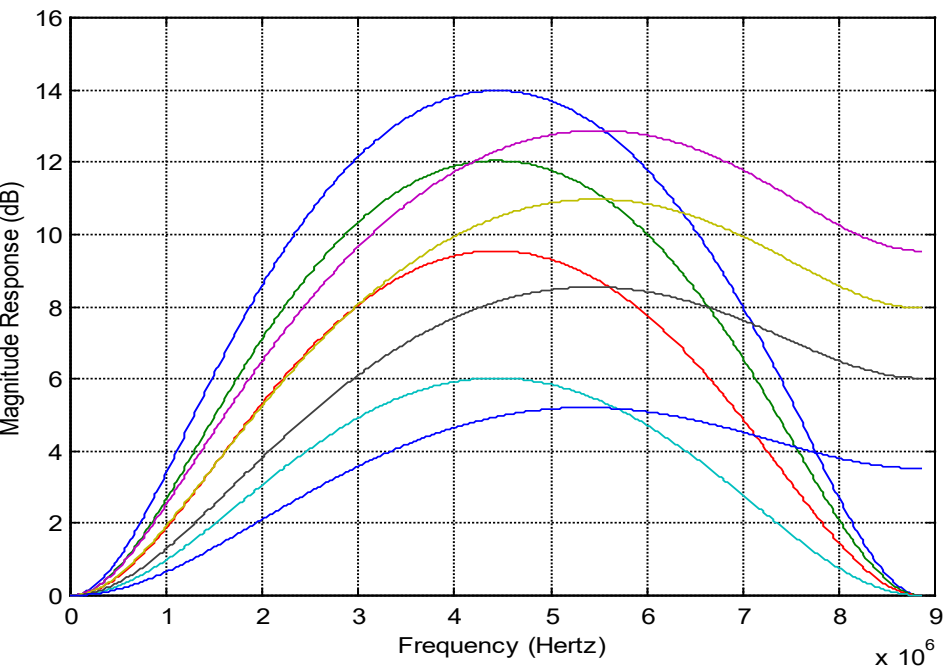
CONFIDENTIAL

PEAKING FILTER CURVES

NTSC



PAL



Parametric Information

AC/DC Electrical Parameters

TABLE 20. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
AVD, AVDLL (measured to AVS, AVSPLL)	VDDAM	-	-	1.98	V
VDD (measured to VSS)	VDDM	-	-	1.98	V
VDD33 (measured to VSSPST)	VDD33M	-	-	3.6	V
Voltage on any digital signal pin (See the note below)	-	VSSPST - 0.5	-	5.5	V
Analog Input Voltage	-	AVS - 0.5	-	1.98	V
Storage Temperature	T S	-65	-	+150	°C
Junction Temperature	T J	-	-	+125	°C
Reflow Soldering	T _{PEAK}	255 +5/-0 (10 to 30 seconds)			°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Note: THIS DEVICE EMPLOYS HIGH-IMPEDANCE CMOS DEVICES ON ALL SIGNAL PINS. IT MUST BE HANDLED AS AN ESD-SENSITIVE DEVICE. VOLTAGE ON ANY SIGNAL PIN THAT EXCEEDS THE RANGES LISTED IN TABLE 20 CAN INDUCE DESTRUCTIVE LATCH-UP.

TABLE 21. CHARACTERISTICS

PARAMETER	SYMBOL	MIN (NOTE 37)	TYP	MAX (NOTE 37)	UNIT
SUPPLY					
Power Supply—I/O	VDD33	3.00	3.3	3.6	V
Power Supply—Analog	VDDA	1.62	1.8	1.98	V
Power Supply—Digital	VDD	1.62	1.8	1.98	V
Maximum VDD - AVD		-	-	0.3	V
MUX0, MUX1 Input Range (AC coupling required)		0.5	1.00	1.40	V
CIN0 Amplitude Range (AC coupling required)		0.5	1.00	1.40	V
Ambient Operating Temperature	T _A	-40		+105	°C
Analog Supply Current : CVBS Differential S-video	I _{aa}	-	14.8	-	mA
		-	24.9	-	mA
		-	24.7	-	
Digital I/O Supply current	I _{dde}	-	13.0	-	mA
Digital Core Supply Current	I _{dd}	-	24.4	-	mA
DIGITAL INPUTS					
Input High Voltage (TTL)	V _{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V _{IL}	-	-	0.8	V
Input High Voltage (XTI)	V _{IH}	2.0	-	VDD33 + 0.5	V
Input Low Voltage (XTI)	V _{IL}	-	-	0.8	V

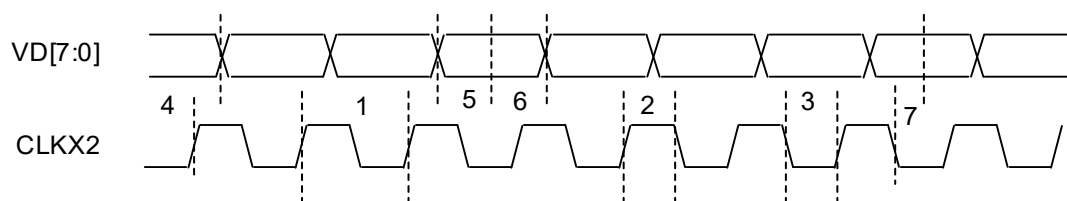
PARAMETER	SYMBOL	MIN (NOTE 37)	TYP	MAX (NOTE 37)	UNIT
Input High Current (VIN = VDD)	IIH	-	-	10	μA
Input Low Current (VIN = VSS)	IIL	-	-	-10	μA
Input Capacitance (f = 1 MHz, VIN = 2.4V)	CIN	-	5	-	pF
DIGITAL OUTPUTS					
Output High Voltage (IOH = -2 mA)	VOH	2.4	-	VDD33	V
Output Low Voltage (IOL = 2 mA)	VOL	-	0.2	0.4	V
3-State Current	IOZ	-	-	10	μA
Output Capacitance	CO	-	5	-	pF
ANALOG INPUT					
Analog Pin Input Voltage	Vi	-	1	-	Vp.p
Analog Pin Input Capacitance	CA	-	7	-	pF
ADCS					
ADC Resolution	ADCR	-	10	-	bits
ADC Integral Nonlinearity	AINL	-	±1	-	LSB
ADC Differential Nonlinearity	ADNL	-	±1	-	LSB
ADC Clock Rate	f _{ADC}	24	27	30	MHz
Video Bandwidth (-3db)	BW	-	10	-	MHz
HORIZONTAL PLL (DECODER)					
Line Frequency (50Hz)	f _{LN}	-	15.625	-	kHz
Line Frequency (60Hz)	f _{LN}	-	15.734	-	kHz
Static Deviation	Δf _H	-	-	6.2	%
SUBCARRIER PLL (DECODER)					
Subcarrier Frequency (NTSC-M)	f _{sc}	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGI)	f _{sc}	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	f _{sc}	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	f _{sc}	-	3582056	-	Hz
Lock-in Range	Δf _H	±450	-	-	Hz
CRYSTAL SPEC					
Nominal frequency (fundamental)		-	27	-	MHz
Deviation* (Note 36)		-	-	±50	ppm
Load capacitance	CL	-	20	-	pF
Series resistor	RS	-	80	-	Ω
OSCILLATOR INPUT					
Nominal frequency		-	27	-	MHz
Deviation		-	-	±50	ppm
Duty cycle		-	-	55	%

PARAMETER	SYMBOL	MIN (NOTE 37)	TYP	MAX (NOTE 37)	UNIT
OUTPUT CLK					
CLKX2	1	24	27	30	MHz
CLKX2 Duty Cycle	2	-	-	55	%
CLKX2 to Data Delay	4	-	5	-	ns
CLKX2 (Falling Edge) to VCLK (Rising Edge)	7	-	0	-	ns

NOTES:

36. Crystal deviation is based on normal operation condition

37. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

CLOCK TIMING DIAGRAM

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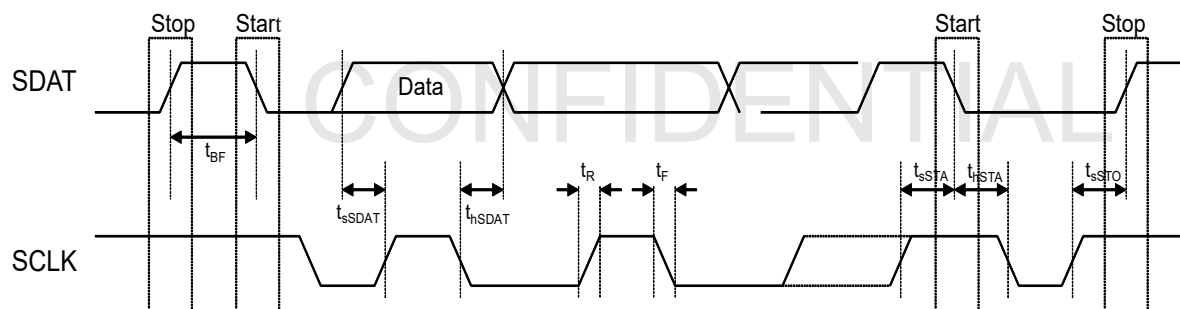
SERIAL HOST INTERFACE TIMING

PARAMETER	SYMBOL	MIN (NOTE 38)	TYP	MAX (NOTE 38)	UNIT
Bus Free Time between STOP and START	t_{BF}	740			ns
SDAT Set-up Time	t_{sSDAT}	74			ns
SDAT Hold Time	t_{hSDAT}	50		900	ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for Each Bus Line	C_{BUS}			400	pF
SCLK Clock Frequency	f_{SCLK}			400	kHz

NOTE:

38. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

SERIAL HOST INTERFACE TIMING DIAGRAM



Video Decoder Parameter 1

PARAMETER	SYMBOL	MIN (NOTE 39)	TYP	MAX (NOTE 39)	UNIT
ADCS					
ADC Resolution	ADCR		10		Bits
ADC Integral Non-Linearity	AINL		±1		LSB
ADC Differential Non-Linearity	ADNL		±1		LSB
ADC Clock Rate	f _{ADC}	24	27	30	MHz
Video Bandwidth (-3db)	BW		10		MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f _{LN}		15.625		kHz
Line Frequency (60Hz)	f _{LN}		15.734		kHz
Static Deviation	Δf _H			6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f _{SC}		3579545		Hz
Subcarrier Frequency (PAL-BDGI)	f _{SC}		4433619		Hz
Subcarrier Frequency (PAL-M)	f _{SC}		3575612		Hz
Subcarrier Frequency (PAL-N)	f _{SC}		3582056		Hz
Lock-In Range	Δf _H				Hz
OSCILLATOR INPUT					
Nominal Frequency			27		MHz
Deviation				±50	ppm
Duty cycle				55	%
LOCK SPECIFICATION					
Sync Amplitude Range		1		200	%
Color Burst Range		5		200	%
Horizontal Lock Range		-5		5	%
Vertical Lock Range		45		65	Hz
Fsc Lock Range			±450		Hz
Color Burst Position Range			±2.2		μs
Color Burst Width Range		1			cycle
VIDEO BANDWIDTH					
B/W			6		MHz
NOISE SPECIFICATION					
SNR (Luma Flat Field)			57		dB

NOTE :

39. Parameters with MIN and/or MAX limits are tested at +25 °C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Video Decoder Parameter 2

PARAMETER	SYMBOL	MIN (NOTE 40)	TYP	MAX (NOTE 40)	UNIT
NONLINEAR SPECIFICATION					
Y Non-Linearity			0.5	0.7	%
Differential Phase	DP		0.4	0.6	°
Differential Gain	DG		0.6	0.8	%
CHROMA SPECIFICATION					
Hue Accuracy			1		°
Chroma ACC Range				400	%
Chroma Amplitude Error			1		%
Chroma Phase Error			0.3		%
Chroma Luma Intermodulation			0.2		%

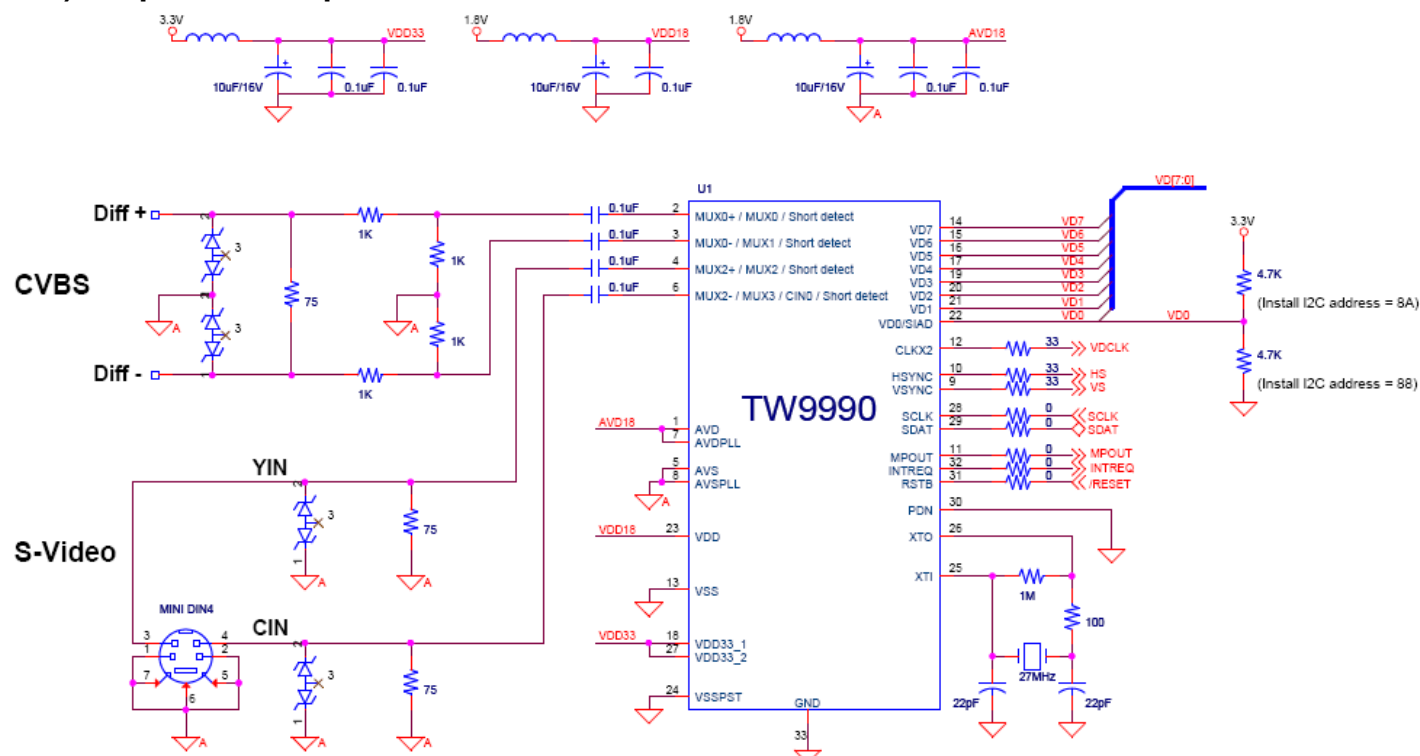
NOTE :

40. Parameters with MIN and/or MAX limits are tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

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Application Schematic

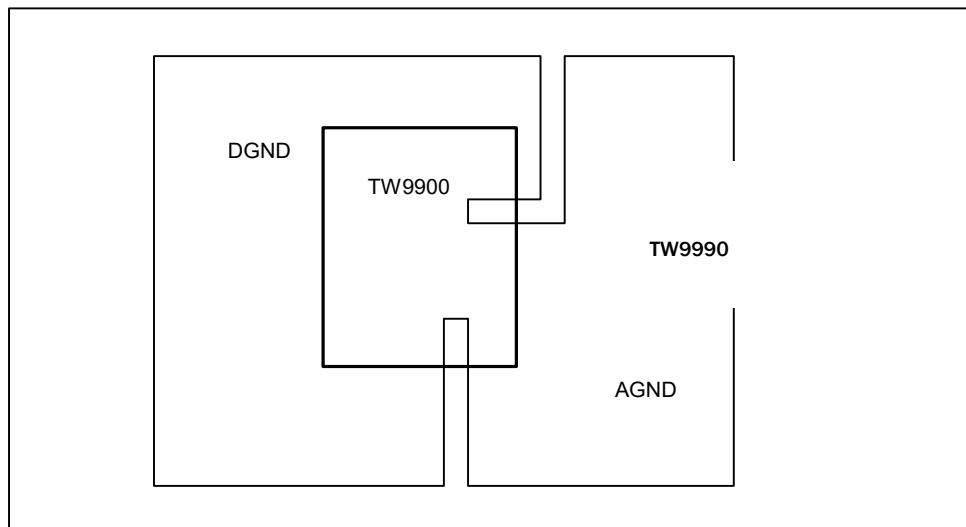
1) Chip Level Example:



PCB Layout Considerations

The PCB layout should be done to minimize the power and ground noise on the TW9990. This is done by good power decoupling with minimum lead length on the de-coupling capacitors; well-filtered and regulated analog power input shielding and ground plane isolation.

The ground plane should cover most of the PCB area with separated digital and analog ground planes surrounding the chip. These two planes should be at the same electrical potential and connected together under TW9990. The following figure shows a ground plane layout example.



To minimize crosstalk, the digital signals of TW9990 should be separated from the analog circuitry. Moreover, the digital signals should not cross over the analog power and ground plane. Parallel running of digital lines for long distance should also be avoided.

For WFQFN Package, the Exposed die pad (Ground bond) can be either floating or soldered to PCB Ground to enhance thermal performance.



Thermal Pad Consideration

Thermal Pad Land Design

The size of the thermal land should at least match the exposed die flag size. But it is necessary to avoid solder bridging between thermal pad and the perimeter pads. We recommend the clearance between thermal pad and perimeter pads is 0.15 mm.

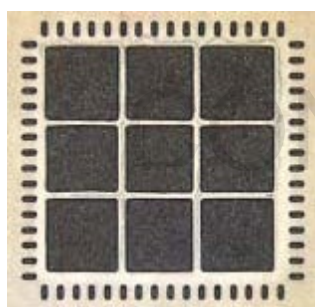
Thermal Via Design

In order to take full advantage of WFQFN thermal performance, thermal vias are needed to provide a thermal path from top to inner/bottom layers of the motherboard to remove the heat.

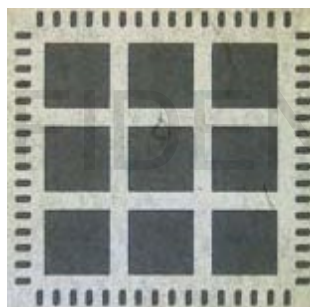
- Via size(in diameter): 0.3 ~ 0.33mm
- Via pitch: 1.0 ~ 1.2 mm
- # of thermal vias : depend on the application

Stencil Recommendation*

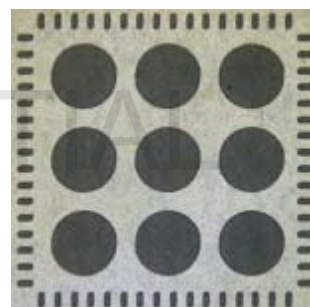
- The small multiple openings should be used in steady of one big opening.
 - 60 ~ 85% solder paste coverage
 - Rounded corners to minimize clogging
 - Positive taper with bottom opening larger than the top



DON'T RECOMMEND
COVERAGE 91%



RECOMMEND
COVERAGE 77%



RECOMMEND
COVERAGE 65%

* Note: About stencil opening pictures are for reference only, please check 32 pin WFQFN Mechanical Data for detail size information.

Control Registers

TW9990 REGISTER SUMMARY

The registers are organized in functional groups in this Register Summary

“-”: For register it means “reserved”, for reset value it means “unknown” register summary

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
00	ID					REV			00
01	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	-
02	DIFF_ENB	FC27	CVIDEO	SVIDEO	YSEL		-		40
03	MODE	LEN	LLCMD	AINC	-	OEN	TRI_SEL		24
04	-	CKHY		HSDLY					00
05	VDSEL				HSP	VSP	HVSEL		00
06	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	C_PDN	-	00
07	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
08	VDELAY_LO								12
09	VACTIVE_LO								F0
0A	HDELAY_LO								10
0B	HACTIVE_LO								D0
0C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC
0D	CLMP_LOI	TOGGLE	CUR_MODE	FULL_TIME	PRECOND	RSTR_ON	RSTR_MODE		00
0E	CONFIDENTIAL								
0F	B_CHANNEL		A_CHANNEL		SH_GND_THRESH		SH_BAT_THRESH		00
10	BRIGHTNESS								00
11	CONTRAST								64
12	SCURVE	VSF	CTI		SHARPNESS				51
13	SAT_U								80
14	SAT_V								80
15	HUE								00
16	-	SV_DET	-						00
17	SHCOR				RTSEL3	VSHP			30
18	CTCOR		CCOR		VCOR		CIF		44
19	VBI_EN	VBI_BYT	VBI_FRAM	HA_EN	-	RTSEL			58
1A	LLC_TEST	EDS_EN	-		FF_OVF	FF_EMP	CC_EDS	LO_HI	00
1B	CK2S		-			CM_GAIN_EN	CM_IN_GAIN	CM_OUT_ATTEN	00
1C	DTSTUS	STDNOW			ATREG	STANDARD			07
1D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSCM	7F
1E	NT50	-							08
1F	TEST								00

INDEX (HEX)	7	6	5	4	3	2	1	0	RESET (HEX)
20	CLPEND				CLPST				50
21	NMGAIN				WPGAIN			AGCGAIN[8]	42
22	AGCGAIN[7:0]								F0
23	PEAKWT								D8
24	CLMPLD	CLMPL							BC
25	SYNCTD	SYNCT							B8
26	MISSCNT				HSWIN				44
27	PCLAMP								2A
28	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
29	BSHT			VSHT					00
2A	CKILMAX		CKILMIN						78
2B	HTL				VTL				44
2C	CKLM	YDLY			HFLT				30
2D	HPLC	EVCNT	PALC	SDET	OPLMT	BYPASS	SYOUT	HADV	14
2E	HPM		ACCT		SPM		CBW		A5
2F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0
30	-				CSBAD	MCVSN	CSTRIPE	CTYPE	00
31	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	00
32	HFREF								-
33	FRM		YNR		CLMD		PSP		05
34	IDX		NSEN / SSEN / PSEN / WKTH						1E
35	CTEST	YCLEN	CLEN	VLEN	GTEST	VLPF	CKLY	CKLC	00
4C	CM_KILL_E	CN_FILTER_REJ		PLL_IREF	CP_SEL		BYPASS_SEL	LPRES_SEL	05
4D	ADCMD	VBIMIN							40
4E	-	HSBEGIN[2:0]			-	HSEND[2:0]			00
4F	-		WSS[19:14]						00
50	FILLDATA								A0
51	NODAEN	SYRM	SDID						22
52	ANCEN	-	VIPCFG	DID					31
53	CRCERR	WSSFLD	WSS[13:8]						80
54	WSS[7:0]								00
55	-		HAMM84	NTSC656	WBI				00
6B	HSBEGIN[10:3]								06
6C	HSEND[10:3]								24
6D	OVSDLY								00
6E	HSPIN	OFDLY			VSMODE	OVSEND			20
6F	PDNSVBI	ANCDMODE	VBIDELAY						13
AE	F1LIEN	F2LIEN	LINENUMBER						1A
AF	INTOEN	INTPOL	EN_GND_B	EN_GND_A	EN_BAT_B	EN_BAT_A	SH_LATCH	SH_CLEAR	80

0X00 – PRODUCT ID CODE REGISTER (ID)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-3	ID	R	The TW9990 Product ID code is 00000.	0
2-0	Revision	R	The revision number.	0

0X01 – CHIP STATUS REGISTER I (STATUS1)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSS	R	1 = Video not present. (Sync is not detected in number of line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Subcarrier PLL is locked to the incoming video source. 0 = Subcarrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual output vertical scanning frequency depends on the current standard invoked.	0

0X02 – INPUT FORMAT (INFORM)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DIFF_ENB	R/W	1 = Differential Mode Enable. If this mode is enabled, select YSEL = 0 or 2 for MUX0+/- or MUX2+/-, respectively. 0 = Differential Mode Disable.	0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	01 = S-video decoding 00 = Composite video decoding	0
3-2	YSEL	R/W	These two bits control the Y input video selection. 00 = Mux0 01 = Mux1 10 = Mux2 11 = Mux3	0
1-0	Reserved	R/W	Reserved	0

0X03 – OUTPUT FORMAT CONTROL REGISTER (OPFORM)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	MODE	R/W	0 = CCIR601 compatible YCrCb 4:2:2 format with separate syncs and flags. 1 = ITU-R-656 compatible data sequence format.	0
6	LEN	R/W	0 = 8-bit YCrCb 4:2:2 output format. 1 = Reserved	0
5	LLCMODE	R/W	1 = LLC output mode. 0 = Reserved	1
4	AINC	R/W	Serial interface auto-indexing control 0 = Auto-Increment 1 = Non-auto	0
3		R/W	Reserved	0
2	OEN	R/W	Output Enable together with TRI_SEL.	1
1-0	TRI_SEL	R/W	With bit OEN, there three bits select the outputs to be tri-stated(OEN, TRI_SEL[1], TRI_SEL[0]). There are three major groups that can be independently tri-stated: timing group (HSYNC, VSYNC, MPOUT), data group VD[7:0], and clock CLKX1 according to following definition. 000 = All output on. 001 = Data group and Clock group on. 010 = All output on. 011 = Reserved. 100 = All tri-state except Clock group. 101 = Data group and Clock group on. 110 = All output on. 111 = All tri-stated.	0

0X04 – COLOR KILLER HYSTERESIS AND HSYNC DELAY CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GMEN	R/W	Factory use only	0
6-5	CKHY	R/W	Color killer hysteresis. 0 – Fastest 1 – Fast 2 – Medium 3 – Slow	0
4-0	HSDLY	R/W	Factory use only	0

0X05 – OUTPUT CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VSP	R/W	0 = VSYNC pin output polarity is active low 1 = VSYNC pin output polarity is active high.	0
6-4	VSSL	R/W	VSYNC pin output control 0 = VSYNC 1 = VACT 2 = FIELD 3 - 5 = Reserved 6 = Factory test only 7 = 0	0
3	HSP	R/W	0 = HSYNC pin output polarity is active low 1 = HSYNC pin output polarity is active high.	0
2-0	HSSL	R/W	HSYNC pin output control 0 = HACT 1 = HSYNC 2 = HLOCK 3 = ASYNCW 4 - 5 = Reserved 6 = Factory test only 7 = 0	0

0X06 – ANALOG CONTROL REGISTER (ACNTL)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SRESET	W	A 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	1 = Internal voltage reference. 0 = Internal voltage reference shutdown.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = System clock in power-down mode, but the MPU INTERFACE module and output clocks (CLKX1 and CLKX2) are still active.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power-down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power-down mode.	0
0		R/W	Reserved for future use	0

0X07 – CROPPING REGISTER, HIGH (CROP_HI)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0X08 – VERTICAL DELAY REGISTER, LOW (VDELAY_LO)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09 – VERTICAL ACTIVE REGISTER, LOW (VACTIVE_LO)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0

0X0A – HORIZONTAL DELAY REGISTER, LOW (HDELAY_LO)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	10h

0X0B – HORIZONTAL ACTIVE REGISTER, LOW (HACTIVE_LO)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0X0C – CONTROL REGISTER I (CNTRL1)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Secam false color reduction mode 1 = Reduction 0 = Normal	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (Recommended) 0 = Mode 0.	1
1	YCOMB	R/W	Comb filter operation in monochrome mode 1 = Off 0 = On	0
0	PDLY	R/W	PAL delay line control 1 = Disable 0 = Enable	0

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0X0D – COMMON MODE CLAMP

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLMP_LOI	R/W	0 = Normal clamp strength 1 = Reduced clamp strength	0
6	TOGGLE	R/W	0 = Disable CM Restore from toggling each line. 1 = Enable CM Restore to toggle each line.	0
5	CUR_MODE	R/W	0 = CM Restore is in voltage mode. 1 = Enable Current Mode for CM Restore	0
4	FULL_TIME	R/W	CM Restore to be active full time for the whole line unless Reg 0x0D[6] = 1. 0 = Disable 1 = Enable	0
3	PRECOND	R/W	Set this bit HIGH will make the unused inputs to be held at mid-supply.	0
2	RSTR_ON	R/W	0 = CM Restore disabled 1 = CM Restore enabled	0
1-0	RSTR_MODE	R/W	The clamping modes for CM Restore 0 = Middle of HSYNC 1 = During the Differential Clamp 2 = After color burst 3 = During color burst	0

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0X0F – SHORT DIAGNOSTIC1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	B-CHANNEL	R/W	These bits select the input for the B-Channel diagnostic. 0 = Mux0 1 = Mux1 2 = Mux2 3 = Mux3	0
5-4	A-CHANNEL	R/W	These bits select the input for the A-Channel diagnostic. 0 = Mux0 1 = Mux1 2 = Mux2 3 = Mux3	0
3-2	SH_GND_THRESH	R/W	These bits select the level of the ground fault diagnostic threshold (as a ratio of the 1.8V power supply). 0 = 1/16 1 = 2/16 2 = 3/16 3 = 5/16	0
1-0	SH_BAT_THRESH	R/W	These bits select the level of the battery fault diagnostic threshold (as a ratio of the 1.8V power supply). 0 = 1/8 1 = 3/8 2 = 5/8 3 = 7/8	0

0X10 – BRIGHTNESS CONTROL REGISTER (BRIGHT)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BRIGHT	R/W	These bits control the brightness. They have value of -128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X11 – CONTRAST CONTROL REGISTER (CONTRAST)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% in 1% per step.	64

0X12 – SHARPNESS CONTROL REGISTER I (SHARPNESS)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SCURVE	R/W	This bit controls the sharpness filter center frequency. 0 = Normal 1 = High	0
6	VSF	R/W	This bit is for internal used.	1
5-4	CTI	R/W	CTI level selection. 0 = Lowest. 3 = Highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1

0X13 – CHROMA (U) GAIN REGISTER (SAT_U)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X14 – CHROMA (V) GAIN REGISTER (SAT_V)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X15 – HUE CONTROL REGISTER (HUE)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +36° (7Fh) to -36° (80h) with an increment of 0.28°. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC system.	00

0X16 – SV_DET

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R	Reserved	0
6	SV_DET	R	1 = Detection of color subcarrier on C-channel	0
5-0	Reserved	R	Reserved	00

0X17 – CORING

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	3
3	RTSEL3	R/W	The real time signal output	0
2-0	VSHP	R/W	Vertical peaking level. 0 = None. 7 = Highest.	0

0X18 – CORING AND IF COMPENSATION (CORING)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0X19 – VBI CONTROL REGISTER (VBICNTL)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VBI_EN	R/W	0 = VBI capture disabled. 1 = VBI capture enabled.	0
6	VBI Byte Order	R/W	0 = Pixel 2, 1, 4, 3, 6, 5.on the VD[7:0] data bus. 1 = Pixel 1, 2, 3, 4, 5, 6.on the VD[7:0] data bus.	1
5	VBI_FRAM	R/W	0 = Normal mode 1 = ADC output mode If ADCMD=0,VD[7:0] pin is 10bit Y-ADC data bit9-2 If ADCMD=1,VD[7:0] pin is 10bit C-YADC data bit9-2	0
4	HA_EN	R/W	0 = HACTIVE output is disabled during vertical blanking period. 1 = HACTIVE output is enabled during vertical blanking period.	1
3		R/W	Reserved	1
2-0	RTSEL	R/W	Register 0x17[3] RTSEL3 together with bits RTSEL control the real time signal output from the MPOUT pin. 0000 = Video loss 0001 = H-lock 0010 = S-lock 0011 = V-lock 0100 = MONO 0101 = DET50 0110 = FIELD 0111 = RTCO (Real Time Control) 1110 = Factory test only 1111 = 0	0

0X1A – ANALOG CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LLCTEST	R/W	LLC test mode	0
6	PLL_PDN	R/W	0 = LLC PLL in normal operation. 1 = PLL in power down mode.	0
5-4	Reserved	R/W	Reserved	0
3	YFLEN	R/W	Y-Ch anti-alias filter control 1 = Enable 0 = Disable	0
2	YSV	R/W	Y-Ch power saving mode 1 = Enable 0 = Disable	0
1	CFLEN	R/W	C-Ch anti-alias filter control 1 = Enable 0 = Disable	0
0	CSV	R/W	C-Ch power saving mode 1 = Enable 0 = Disable	0

0X1B – OUTPUT CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CK2S	R/W	CLKX2 pin output control. Set to "0" 0 = CLKx2, Others = Reserved	0
5-3	Reserved	R/W	Reserved	0
2	CM_GAIN_EN	R/W	1 = Enable extra gain stage 0 = Bypass extra gain stage	0
1	CM_IN_GAIN	R/W	1 = Extra gain is 12dB 0 = Extra gain is 6dB	0
0	CM_OUT_ATTEN	R/W	1 = Extra gain is reduced by 6dB 0 = Extra gain is not changed = 0dB	0

0X1C – STANDARD SELECTION (SDT)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X1D – STANDARD RECOGNITION (SDTR)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = Enable recognition of PAL60. 0 = Disable recognition.	1
5	PALN_EN	R/W	1 = Enable recognition of PAL (CN). 0 = Disable recognition.	1
4	PALM_EN	R/W	1 = Enable recognition of PAL (M). 0 = Disable recognition.	1
3	NT44_EN	R/W	1 = Enable recognition of NTSC 4.43. 0 = Disable recognition.	1
2	SEC_EN	R/W	1 = Enable recognition of SECAM. 0 = Disable recognition.	1
1	PALB_EN	R/W	1 = Enable recognition of PAL (B,D,G,H,I). 0 = Disable recognition.	1
0	NTSC_EN	R/W	1 = Enable recognition of NTSC (M). 0 = Disable recognition.	1

0X1E – RESERVED

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = Decoding format is set by register 0x1C (SDT)	0
6-0	Reserved	R	Reserved	08

0X1F – TEST CONTROL REGISTER (TEST)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	TEST	R/W	This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 1 = Analog test mode1. The Y channel 10bit ADC output can be obtained from {VD[7:0],HSYNC,VSABC}. 2 = Analog test mode2. The C channel 10bit ADC output can be obtained from {VD[7:0],HSYNC,VSABC}. 4 = Digital test mode1. This is the CVBS test mode. The 8-bit input corresponds to VD[7:0] in the order of bit 7 to 0. B = Clamp test mode. Clamp control input YU, YUX, YD, YDX, CU, CUX, CD, and CDX are mapped to VD[3:0]. YU = VD[3], YUX = VD[2], YD = VD[1], YDX = VD[0] CU = VD[3], CUX = VD[2], CD = VD[1], CDX = VD[0] C = Memory Bist test mode. Internal Memories are tested with XTI clock input and following pin outputs. VD[7] = Comb4_fail_h. VD[6] = Comb4_tst_done VD[5] = bcs_fail_h VD[4] = bcs_tst_done Other values are reserved.	0

0X20 – CLAMPING GAIN (CLMPG)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping period is determined by this and CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0X21 – INDIVIDUAL AGC GAIN (IAGC)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	4
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	This bit is the MSB of the 10-bit register that controls the AGC gain when AGC loop is disabled.	0

0X22 – AGC GAIN (AGCGAIN)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 10-bit register that controls the AGC gain when AGC loop is disabled.	F0

0X23 – WHITE PEAK THRESHOLD (PEAKWT)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' disables this function.	D8

0X24 – CLAMP LEVEL (CLMPL)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d for 60Hz field rate or 63d for 50Hz.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y-channel.	3C

0X25 – SYNC AMPLITUDE (SYNCT)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0X26 – SYNC MISS COUNT REGISTER (MISSCNT)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MISSCNT	R/W	MISSCNT[3] controls the speed of VDLOSS detection with '0' being fast and '1' being slow. MISSCNT[2:0] control the threshold of horizontal sync miss detection per field before VDLOSS is flagged.	4
3-0	HSWIN	R/W	These bits determine the VCR mode HSYNC detection window.	4

0X27 – CLAMP POSITION REGISTER (PCLAMP)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	2A

0X28 – VERTICAL CONTROL I (VCNTL1)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VLCKI	R/W	Vertical lock in time. 0 = Fastest 3 = Slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = Fastest 3 = Slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = Search mode. 0 = Vertical count down mode.	0
2	DETV	R/W	1 = Recommended for special application only. 0 = Normal Vertical sync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = Long 0 = Normal	0

0X29 – VERTICAL CONTROL II (VCNTL2)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	BSHT	R/W	Burst PLL center frequency control. Factory use only.	0
5-0	VSHT	R/W	Vertical sync output delay control in the increment of half line length.	00

0X2A – COLOR KILLER LEVEL CONTROL (CKILL)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	28

0X2B – COMB FILTER CONTROL (COMB)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	HTL	R/W	Adaptive Comb filter threshold control 1.	4
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4

0X2C – LUMA DELAY AND H FILTER CONTROL (LDLY)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKLM	R/W	Color killer mode. 0 = Normal 1 = Fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provide -4 to +3 unit delay control.	3
3-0	HFLT	R/W	Alternative peaking control. Larger value gives larger enhancement.	0

0X2D – MISCELLANEOUS CONTROL I (MISC1)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HPLC	R/W	Reserved for Internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	OPLMT	R/W	1 = Output data range are limited to 16~235 for Y and 16~240 for Cb/Cr. 0 = No limit.	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	1 = HSYNC output is disabled when video loss is detected 0 = HSYNC output is always enabled	0
0	HADV	R/W	This bit advances the HACTIVE pin output by one data clock when set.	0

0X2E – LOOP CONTROL REGISTER (LOOP)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto 1 1 = Auto2 0 = Normal	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = Slow 2 = Medium 3 = Fast	2
3-2	SPM	R/W	Burst PLL speed control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0X2F – MISCELLANEOUS CONTROL II (MISC2)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled	1
4	CBAL	R/W	0 = Normal output 1 = Special output mode	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color 0 = Black	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X30 – MACROVISION DETECTION (MVSN)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R	Reserved	0
3	CSBAD	R	Set when Macrovision color stripe detection may be un-reliable	0
2	MCVSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. Cstripe=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X31 – CHIP STATUS II (STATUS2)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCR	R	VCR signal indicator	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = 525/625 line signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	0
1	EDSDT	R	1 = EDS data detected. 0 = Not detected.	0
0	CCDET	R	1 = CC data detected. 0 = Not detected.	0

0X32 – H MONITOR (HFREF)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HFREF	R	Horizontal line frequency indicator	X

0X33 – CLAMP MODE (CLMD)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	FRM	R/W	Free run mode control 0 = Auto 2 = Default to 60Hz 3 = Default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None 1 = smallest 2 = Small 3 = Medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = Low 1 = Medium 2 = High	1

0X34 – ID DETECTION CONTROL (IDCNTL)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently be controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0X35 – CLAMP CONTROL I (CLCNTL1)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CTEST	R/W	Clamping control.	1
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled	0
5	CLEN	R/W	1 = C channel clamp disabled 0 = Enabled	0
4	VLEN	R/W	Reserved	0
3	GTEST	R/W	1 = Test. 0 = Normal operation	0
2	VLPF	R/W	Sync filter control	0
1	CKLY	R/W	Clamping current control 1	0
0	CKLC	R/W	Clamping current control 2	0

0X4C – ANAPLLCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CM_KILL_EN	R/W	1 = Enable enhanced common mode rejection function 0 = Disable	0
6-5	CM_FILTER_REJ	R/W	This controls a first order filter at the input of the AFE that works only when the extra gain is enabled. This filter is strongest when <1,1> weakest when <0,0>. The lowest bandwidth is at <1,1> and will have some effect on video bandwidth. The highest setting will not affect video bandwidth. It is recommended that this filter is set off or wideband which is <0,0>.	0
4	PLL_IREF	R/W	Current bias 0:Default, 1:33% more current	0
3-2	CP_SEL	R/W	Charge-pump current 00: 1μA, 01: 5μA, 10: 10μA, 11: 15μA	1
1	BYPASS_SEL	R/W	Test mode 0:PLL clock output, 1:PLL reference clock	0
0	LPRES_SEL	R/W	Loop-filter resistance 0:60k, 1:35k	1

0X4D – VBIMIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ADCMD	R/W	Test purpose only for ADC data output. When VBI_FRAM=1, this function is effective. 0: VD[7:0] pin output 10-bit Y-ADC data Bit9-2. 1: VD[7:0] pin output 10-bit C-ADC data Bit9-2.	0
6-0	VBIMIN	R/W	VBI Minimum Level.	40

0X4E – HSLOWCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	HSBEGIN[2:0]	R/W	HSYNC Start position Control Bit2-0.	00
3	Reserved	R		0
2-0	HSEND[2:0]	R/W	HSYNC End position Control Bit2-0.	00

0X4F – WSS3

BIT	FUNCTION	R/W	DESCRIPTION	RESET
5-0	WSS[19:14]	R	CGMS (WSS525) Bit19-14 in 525 line video system. These bits show CRC 6bits in CGMS (WSS525). These bits are only valid in 525 line video system.	0

0X50 – FILLDATA

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	FILLDATA	R/W	Filled data as dummy data in ANC Dword data packet.	A0

0X51 – SDID

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NODAEN	R/W	1: Bit7 in 4th byte of EAV/SAV code will be 0 when sync lost (No Video input.) 0: Bit7 in 4th byte of EAV/SAV is always VIPCFG register bit.	0
6	SYRM	R/W	1: Minimum value in raw VBI will be 0x10 for Sync Level remove. 0: None.	0
5-0	SDID	R/W	Secondary data ID in ANC data packet type 2	22

0X52 – DID

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ANCEN	R/W	ANC data packet output control. 1 = Enable. 0 = Disable.	0
6	Reserved	R	Reserved	0
5	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code.	1
4-0	DID	R/W	Data ID in ANC data packet type 2.	11

0X53 – WSS1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CRCERR	R	This bit is only valid in 525 line video system. 1: CGMS(WSS525) CRC error detected in current field. 0: No CRC error	1
6	WSSFLD	R	0: Current WSS data is received in Odd field. 1: Current WSS data is received in Even field.	0
5-0	WSS[13:8]	R	CGMS (WSS525) Bit13-8 in 525 line video system. Wide Screen Signaling Bit13-8 in 625 line video system.	0

0X54 – WSS2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	WSS[7:0]	R	CGMS (WSS525) Bit7-0 in 525 line video system. Wide Screen Signaling Bit7-0 in 625 line video system.	0

0X55 – VVBI

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R	Reserved	0
5	HAMM84	R/W	1: Enable 84 Hamming Code checking BI Slicer. 0: Disable.	0
4	NTSC656	R/W	1: Number of Even Field Video output line is (the number of Odd field Video output line – 1). This bit is required for ITU-R BT.656 output for 525-line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line.	0
3-0	VVBI	R/W	The number of raw VBI data output line counted from top video active line signal timing.	0

0X56~6A LCTL6~LCTL26

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	LCTLn	R/W	Set up VBI Data Slicer Decoding mode on Line-n. Value is set up by upper Bit7-4 meaning for Line-n in odd field.	0
3-0		R/W	Value is set up by below Bit3-0 meaning for Line-n in even field. 0h: Disable decoding. 1h: Teletext-B 2h: Teletext-C 3h: Teletext-D 4h: Closed Captioning and Extended Data service. (EIA-608 type). 5h: CGMS (WSS525) in 525 line system or WSS625 in 625 line system. 6h: VITC 7h: Gemstar 1x 8h: Gemstar 2x 9h: VPS (Line16 VPS type) Ah: Teletext-A Bh~Fh: reserved	0

0X6B – HSGEGIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSBEGIN[10:3]	R/W	HSYNC Start position Bit10-3.	06

0X6C – HSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HSEND[10:3]	R/W	HSYNC End position Bit10-3.	24

0X6D – OVSDLY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	OVSDLY	R/W	VSYNC start position.	00

0X6E – OVSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HSPIN	R/W	1: HSYNC output is HACTIVE. 0: HSYNC output is HSYNC.	0
6-4	OFDLY	R/W	FIELD output delay. This bit is only effective for FIELD signal on MPOUT pin output. 0h: 0H line delay FIELD output. 1h-7h: 1-H to 7-H line delay FIELD output.	2
3	VSMODE	R/W	1: VSYNC output is HACTIVE-VSYNC mode. 0: VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0X6F – VBIDELAY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PDNSVBI	R/W	1: VBI data slicer enable 0: VBI data slicer is in reset and power-down mode	0
6	ANCDMODE	R/W	0: 0xFF/0x00 data value in ANC data packet will be converted to 0xFC/0x03 value. 1: No change	0
5-0	VBIDELAY	R/W	Raw VBI output delay. Typical setting value: NTSC-M 13h, PAL 8h	13

0XAE – LINENUMBERINT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	F1LIEN	R/W	0: Disable LINE_INT during field 1. 1: Enable LINE_INT during field 1.	0
6	F2LIEN	R/W	0: Disable LINE_INT during field 2. 1: Enable LINE_INT during field 2.	0
5-0	LINENUMBER	R/W	LINE_INT register bit is "1" while video line number is more than this value. LINE_INT_CH register bit is also set to "1" at the start of this video number.	1A

0XAF – SHORT DIAGNOSTIC2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	INTOEN	R/W	0 = Enable INTREQ output 1 = Disable INTREQ output	1
6	INTPOL	R/W	0 = Negative polarity 1 = Positive polarity	0
5	EN_GND_B	R/W	Enable short-to-ground on Channel B	0
4	EN_GND_A	R/W	Enable short-to-ground on Channel A	0
3	EN_BAT_B	R/W	Enable short-to-battery on Channel B	0
2	EN_BAT_A	R/W	Enable short-to-battery on Channel A	0
1	SH_LATCH	R/W	0 = Fault signals are logically ORed and are not latched. 1 = Enable all fault signals to be latched until it is cleared.	0
0	SH_CLEAR	R/W	Set '1' and then '0' will clear the latched fault signals if 0xAF[1]=1. This bit must be manually toggled.	0

0XB0 – INT1ENABLE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SHORT_INT_ENABLE	R/W	0: Disable SHORT_INT status changed interrupt on INTREQ pin. 1: Enable SHORT_INT status changed interrupt on INTREQ pin.	0
6	GEM2XCH_ENABLE	R/W	0: Disable GEMSTAR2X status changed interrupt on INTREQ pin. 1: Enable GEMSTAR2X status changed interrupt on INTREQ pin.	0
5	VITCCH_ENABLE	R/W	0: Disable VITC status changed interrupt on INTREQ pin. 1: Enable VITC status changed interrupt on INTREQ pin.	0
4	VPSCH_ENABLE	R/W	0: Disable VPS status changed interrupt on INTREQ pin. 1: Enable VPS status changed interrupt on INTREQ pin.	0
3	WSTCH_ENABLE	R/W	0: Disable WST(Teletext) status changed interrupt on INTREQ pin. 1: Enable WST(Teletext) status changed interrupt on INTREQ pin.	0
2	WSSCH_ENABLE	R/W	0: Disable WSS status changed interrupt on INTREQ pin. 1: Enable WSS status changed interrupt on INTREQ pin.	0
1	CCF2CH_ENABLE	R/W	0: Disable CCF2 status changed interrupt on INTREQ pin. 1: Enable CCF2 status changed interrupt on INTREQ pin.	0
0	CCF1CH_ENABLE	R/W	0: Disable CCF1 status changed interrupt on INTREQ pin. 1: Enable CCF1 status changed interrupt on INTREQ pin.	0

0XB1 – INT2ENABLE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LINE_INT_CH_ENABLE	R/W	0: Disable LINE_INT_CH interrupt on INTREQ pin. 1: Enable LINE_INT_CH interrupt on INTREQ pin.	0
6	MACROCH_ENABLE	R/W	0: Disable Macrovision status changed interrupt on INTREQ pin. 1: Enable Macrovision status changed interrupt on INTREQ pin.	0
5	VDLOSSCH_ENABLE	R/W	0: Disable VDLOSS status changed interrupt on INTREQ pin. 1: Enable VDLOSS status changed interrupt on INTREQ pin.	0
4	DET50CH_ENABLE	R/W	0: Disable DET50 status changed interrupt on INTREQ pin. 1: Enable DET50 status changed interrupt on INTREQ pin.	0
3		R	Reserved	0
2	SLOCKCH_ENABLE	R/W	0: Disable SLOCK status changed interrupt on INTREQ pin. 1: Enable SLOCK status changed interrupt on INTREQ pin.	0
1	HVLOCKCH_ENABLE	R/W	0: Disable HVLOCK status changed interrupt on INTREQ pin. 1: Enable HVLOCK status changed interrupt on INTREQ pin.	0
0	VCRCH_ENABLE	R/W	0: Disable VCR status changed interrupt on INTREQ pin. 1: Enable VCR status changed interrupt on INTREQ pin.	0

0XB3 – INT1RST

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SHORT_INT_RST	R/W	0: No action. 1: Reset SHORT_INT bit to 0.	0
6	GEM2XCH_RST	R/W	0: No action. 1: Reset GEM2XCH_STATUS bit to 0.	0
5	VITCCH_RST	R/W	0: No action. 1: Reset VITCCH_STATUS bit to 0.	0
4	VPSCH_RST	R/W	0: No action. 1: Reset VPSCH_STATUS bit to 0.	0
3	WSTCH_RST	R/W	0: No action. 1: Reset WSTCH_STATUS bit to 0.	0
2	WSSCH_RST	R/W	0: No action. 1: Reset WSSCH_STATUS bit to 0.	0
1	CCF2CH_RST	R/W	0: No action. 1: Reset CCF2CH_STATUS bit to 0.	0
0	CCF1CH_RST	R/W	0: No action. 1: Reset CCF1CH_STATUS bit to 0.	0

0XB4 – INT2RST

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LINE_INT_CH_RST	R/W	0: No action. 1: Reset LINE_INT_CH_STATUS bit to 0.	0
6	MACROCH_RST	R/W	0: No action, 1: Reset MACROCH_STATUS bit to 0.	0
5	VDLOSSCH_RST	R/W	0: No action. 1: Reset VDLOSSCH_STATUS bit to 0.	0
4	DET50CH_RST	R/W	0: No action. 1: Reset DET50CH_STATUS bit to 0.	0
3		R	Reserved	0
2	SLOCKCH_RST	R/W	0: No action. 1: Reset SLOCKCH_STATUS bit to 0.	0
1	HVLOCKCH_RST	R/W	0: No action. 1: Reset HVLOCKCH_STATUS bit to 0.	0
0	VCRCH_RST	R/W	0: No action. 1: Reset VCRCH_STATUS bit to 0.	0

0XB6 – INT1RAWSTATUS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SHORT_INT_DET	R	0: Not available. 1: SHORT_INT type data is detected.	0
6	GEM2X_DET	R	0: Not available. 1: GEMSTAR2X type data is detected.	0
5	VITC_DET	R	0: Not available. 1: VITC data is detected.	0
4	VPS_DET	R	0: Not available. 1: VPS data is detected.	0
3	WST_DET	R	0: Not available. 1: WST (Teletext) data is detected.	0
2	WSS_DET	R	0: Not available. 1: WSS data is detected.	0
1	CCF2_DET	R	0: Not available. 1: CCF2 (Field2 Closed Captioning) data is detected.	0
0	CCF1_DET	R	0: Not available. 1: CCF1 (Field1 Closed Captioning) data is detected.	0

0XB7 – INT2RAWSTATUS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LINE_INT	R	0: Current Video line number is smaller than the number of LINENUMBER register. 1: Current Video line number is larger than the number of LINENUMBER register.	0
6	MACRO	R	0: Macrovision status is not changing in current field. 1: Macrovision status is changing in current field.	0
5	VDLOSS	R	This bit is same as VDLOSS in reg0x00[7]. This bit exists here for INT2STATUS and INTREQ pin interrupt. 1 = Video not present. (Sync is not detected in number of line periods specified by MISSCNT register) 0 = Video detected.	0
4	DET50	R	This bit is same as DET50 in reg0x00[0]. This bit exists here for INT2STATUS and INTREQ pin interrupt. 0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0
3		R	Reserved	0
2	SLOCK	R	This bit is same as SLOCK in reg0x00[5]. This bit exists here for INT2STATUS and INTREQ pin interrupt. 1 = Subcarrier PLL is locked to the incoming video source. 0 = Subcarrier PLL is not locked.	0
1	HVLOCK	R	0: {HLOCK,VLOCK}=2'b00. 1: {HLOCK,VLOCK} is not 2'b00.	0
0	VCR	R	This bit is same as VCR in reg0x31[7]. This bit exists here for INT2STATUS and INTREQ pin interrupt. VCR signal indicator.	0

0XB9 – INT1STATUS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GEM1X_STATUS	R	0: This status was being reset and has not been changed since then. 1: GEMSTAR1X detection status changed.	0
6	GEM2X_STATUS	R	0: This status was being reset and has not been changed since then. 1: GEMSTAR2X detection status changed.	0
5	VITC_STATUS	R	0: This status was being reset and has not been changed since then. 1: VITC detection status changed.	0
4	VPS_STATUS	R	0: This status was being reset and has not been changed since then. 1: VPS detection status changed.	0
3	WST_STATUS	R	0: This status was being reset and has not been changed since then. 1: WST (Teletext) detection status changed.	0
2	WSS_STATUS	R	0: This status was being reset and has not been changed since then. 1: WSS is detected and WSS registers are updated.	0
1	CCF2_STATUS	R	0: This status was being reset and has not been changed since then. 1: CCF2 is detected and CCF2DATA1/CCF2DATA2 registers are updated.	0
0	CCF1_STATUS	R	0: This status was being reset and has not been changed since then. 1: CCF1 is detected and CCF1DATA1/CCF1DATA2 registers are updated	0

0XBA – INT2STATUS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LINE_INT_CH	R	0: This status was being reset and has not been changed since then. 1: LINE_INT detection status changed.	0
6	MACROCH	R	0: This status was being reset and has not been changed since then. 1: Macrovision detection status changed.	0
5	VDLOSSCH	R	0: This status was being reset and has not been changed since then. 1: VDLOSS detection status changed.	0
4	DET50CH	R	0: This status was being reset and has not been changed since then. 1: DET50 detection status changed.	0
3		R	Reserved	0
2	SLOCKCH	R	0: This status was being reset and has not been changed since then. 1: SLOCK detection status changed.	0
1	HVLOCKCH	R	0: This status was being reset and has not been changed since then. 1: HVLOCK detection status changed.	0
0	VCRCH	R	0: This status was being reset and has not been changed since then. 1: VCR detection status changed.	0

0XBD – CCF1DATA1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CCF1DATA1	R	Field1 CC data 1st byte.	80

0XBE – CCF1DATA2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CCF1DATA2	R	Field1 CC data 2nd byte.	80

0XBF – CCF2DATA1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CCF2DATA1	R	Field2 CC data 1st byte.	80

0XC0 – CCF2DATA2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CCF2DATA2	R	Field2 CC data 2nd byte.	80

Life Support Policy

These products are not authorized for use as critical components in life support devices or systems.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION #	CHANGE
Jun 2, 2023	6.01	Updated Pin description for pins 2, 3, 4, and 6.
Oct 1, 2021	6.00	P1, description for Digital output, added "8-bit" P35, removed VCLK from the timing table and chart P38, remove kfactor P42, update reg 0x1B[5-3] P43, update reg 0xAF reset value P54, update description for reg 0x1B[7-6], reserved [5-4] P65, update reg 0xAF bit7 =1 reset value P73, update POD to the latest revision, changes are as follows: -Added Note 7 for Edge Protection Technology -Updated D1 and E1 dimensions in Top View changing them from 4.75 to 4.71. -Updated side view by adding Edge protection information. Removed About Intersil section.
Jan 20, 2016	5.00	Applied Intersil Standards throughout document. Added AEC Qualified to Features on page 1. Updated POD to most current revision with rev changes as follows: -Bottom View - changed left side dimension (0.50) to (0.45) - Detail "X" - removed measurement left side. -Changed Seating plane dimension from 0.08 to 0.05 +++20141002 -Detail "X" - Added dimple dimension 0.10 ±0.05 back on (left side). -Detail "X" - Changed the tolerance back (in the seating plane box) to 0.08. -Bottom View - Removed 0.15 ±0.10 this is a duplicate dim with detail A. -Bottom View - Extended the dimension line to the bottom of the exposed pad.
Feb 14, 2014	4.00	Updated Note for the Ordering Information on page 4
Dec 7, 2013	3.00	Made correction to description for register 0x02[3:2] on page 43
Aug 22, 2013	2.00	On page 1, changed bullet from "Low power consumption: <100mW typical" to "Low power consumption". On page 4 Corrected misspelled word. Changed "less than 100mW" to "110mW".
Aug 8, 2013	1.00	All references to "QFN" package changed to "WFQFN" to reflect that this is a Wettable Flank QFN package.

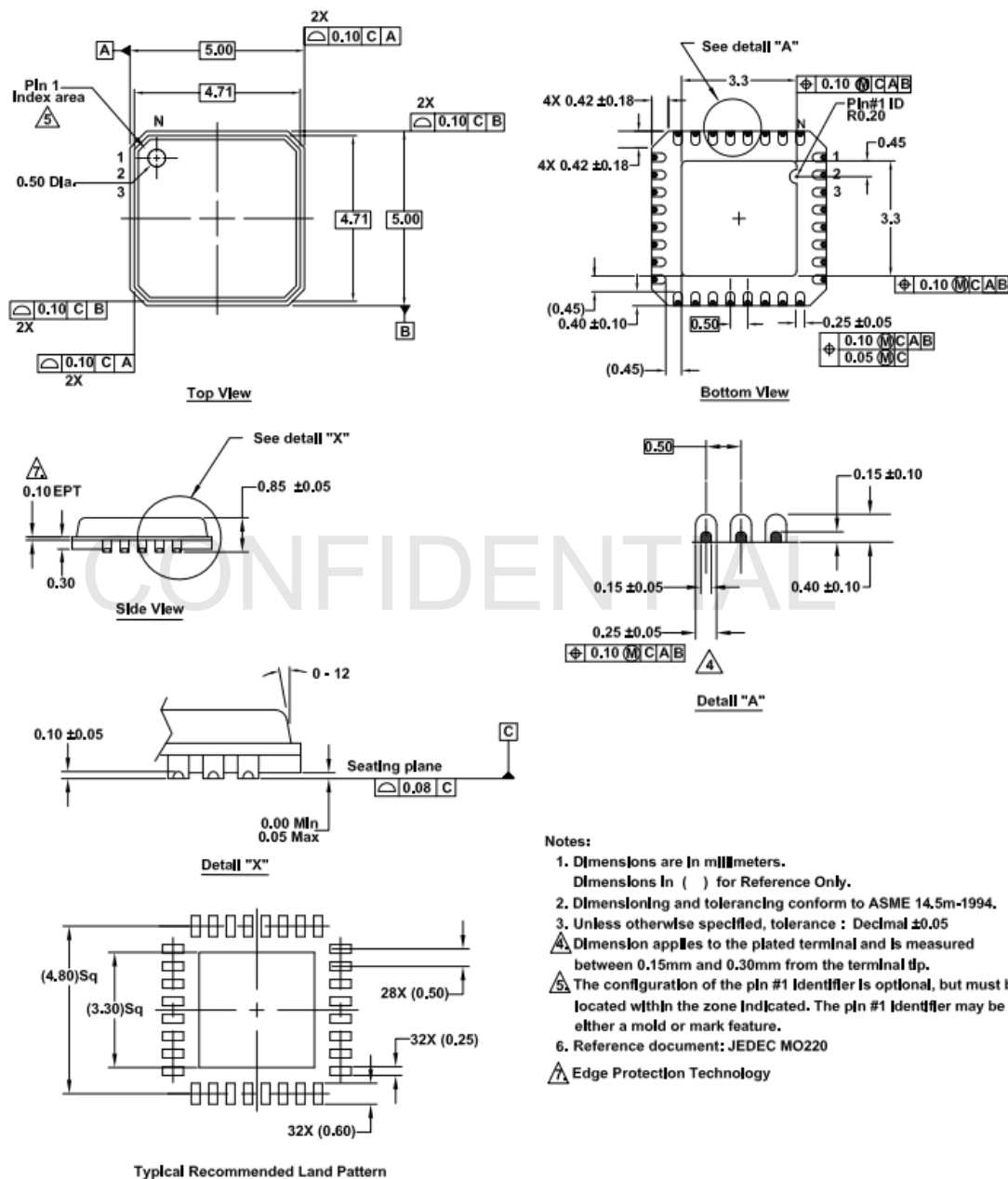
Package Outline Drawing

For the most recent package outline drawing, see [L32.5X5H](#).

L32.5x5H

32 Lead Quad Flat No-Lead Plastic Package (Punch QFN with Wettable Flank)

Rev 3, 8/2021



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