

TW9984

4-Channel Video Decoder and Video Encoder for Automotive Applications

The [TW9984](#) has four high quality NTSC/PAL/SECAM video decoders that convert analog composite video signal to digital component YCbCr data. Each channel contains a 10-bit ADC with application selectable differential or single-ended analog video input options and proprietary clamp and gain controllers. Each channel uses a 4H comb filter to separate luminance and chrominance to reduce cross noise artifacts. The TW9984 uses image enhancement techniques such as IF compensation filter, CTI, and programmable peaking. The TW9984 also includes an NTSC/PAL video encoder with a 10-bit DAC to support CVBS output.

Related Literature

UG018, "TW9984AT-NA1-GE-EVAL Evaluation Board User Guide"

For a full list of related documents, visit our website:

- [TW9984](#) device page

Features

- Accepts all NTSC (M/4.43)/PAL (B/D/G/H/I/K/L/M/N/60)/SECAM standards with auto detection
- Integrated four video analog antialiasing filters and 10-bit CMOS ADCs with differential and single-ended inputs

- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter to improve color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness, and sharpness
- Proprietary fast video locking system for non-real-time applications
- Supports the standard ITU-R BT.656 format or time multiplexed output with 54MHz/108MHz
- Supports a two-wire serial host interface
- Integrated video encoder and 10-bit video CMOS DAC
- Integrated clock PLL for 108MHz clock output
- Short-to-battery and short-to-ground detection
- Ultra low power consumption (550mW, typical)
- Single 27MHz crystal for all standards and output options
- 1.2V/3.3V power supply
- Optional 1.8V digital operation
- 10mmx10mm 68 Ld WQFN package
- [AEC-Q100](#) qualified

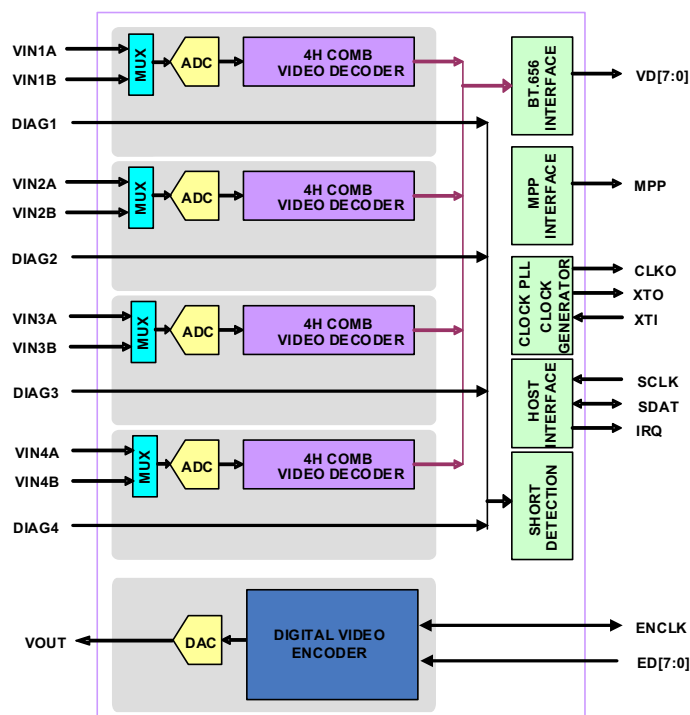


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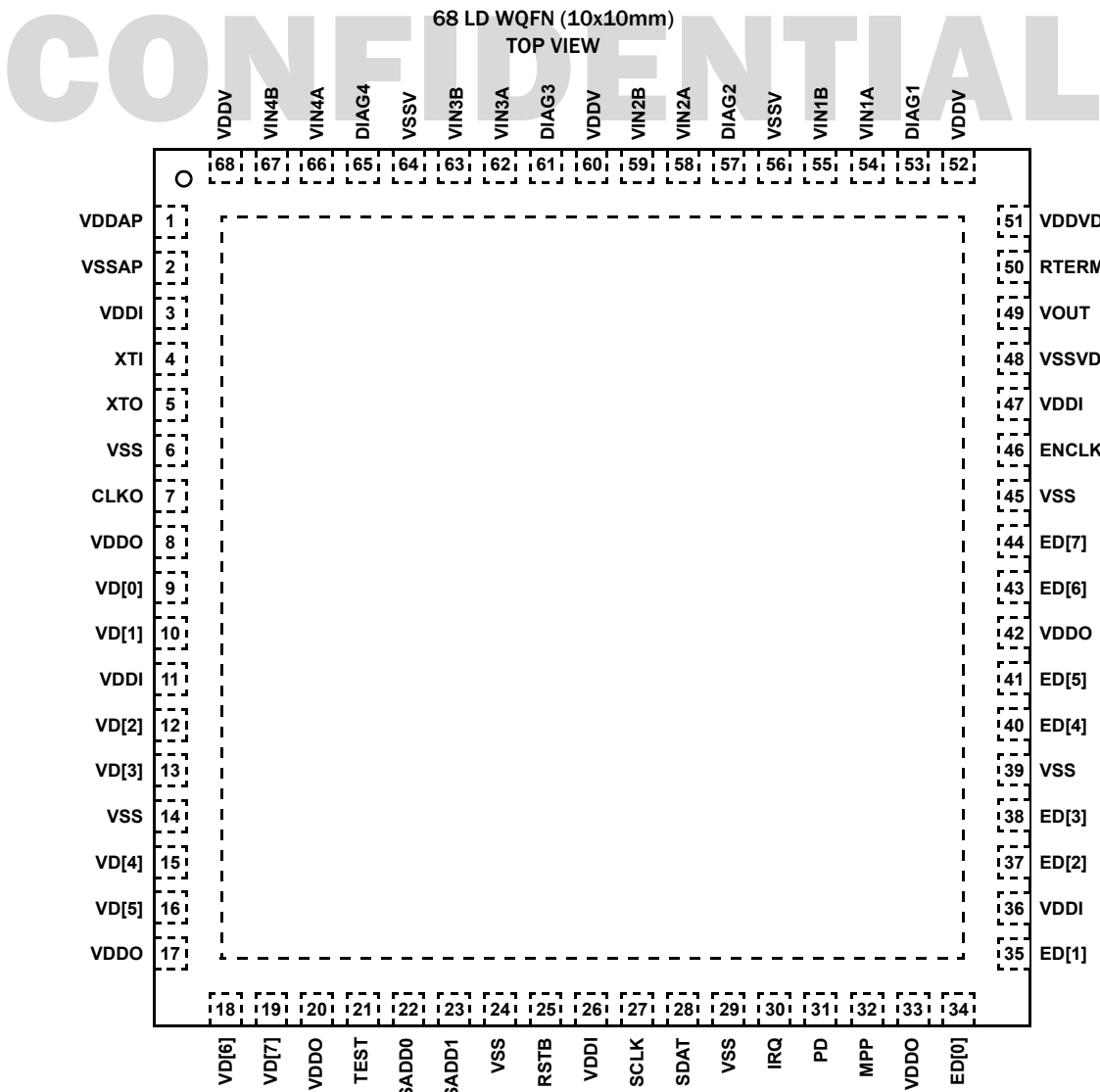
Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP RANGE
TW9984AT-NA1-GE	TW9984AT NA1-GE	68 Lead WQFN (10mmx10mm)	L68.10x10D	Tray	-40 to +105 °C
TW9984AT-NA1-GET				Reel, 1k	
TW9984AT-NA1-GE-EVAL	Evaluation Board				

NOTES:

- 1. See [TB347](#) for details about reel specifications.
- 2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- 3. For Moisture Sensitivity Level (MSL), see the [TW9984](#) device page. For more information about MSL, see [TB363](#).

Pin Configuration



Pin Descriptions

PIN#	I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION (Notes 4, 5)	RECOMMENDED CONNECTION WHEN UNUSED	STATUS AFTER HW RESET
ANALOG VIDEO INTERFACE PINS						
54	AI	VIN1A	Single-ended analog CVBS input 1A/differential CVBS positive input 1	-	Ground	-
55	AI	VIN1B	Single-ended analog CVBS input 1B/differential CVBS negative input 1	-	Ground	-
58	AI	VIN2A	Single-ended analog CVBS input 2A/differential CVBS positive input 2	-	Ground	-
59	AI	VIN2B	Single-ended analog CVBS input 2B/differential CVBS negative input 2	-	Ground	-
62	AI	VIN3A	Single-ended analog CVBS input 3A/differential CVBS positive input 3	-	Ground	-
63	AI	VIN3B	Single-ended analog CVBS input 3B/differential CVBS negative input 3	-	Ground	-
66	AI	VIN4A	Single-ended analog CVBS input 4A/differential CVBS positive input 4	-	Ground	-
67	AI	VIN4B	Single-ended analog CVBS input 4B/differential CVBS negative input 4	-	Ground	-
49	AO	VOUT	Analog CVBS output	-	Open	-
50	AI	RTERM	Analog video resistance termination	-	Ground through resistor	-
53	AI	DIAG1	Short detection input 1	-	Ground	-
57	AI	DIAG2	Short detection input 2	-	Ground	-
61	AI	DIAG3	Short detection input 3	-	Ground	-
65	AI	DIAG4	Short detection input 4	-	Ground	-
DIGITAL VIDEO INTERFACE PINS						
9	O	VD[0]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
10	O	VD[1]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
12	O	VD[2]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
13	O	VD[3]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
15	O	VD[4]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
16	O	VD[5]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
18	O	VD[6]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
19	O	VD[7]	BT.656 data output (1.8V/3.3V selectable)	-	Open	-
7	O	CLKO	27MHz/54MHz/108MHz clock output (1.8V/3.3V selectable)	-	Open	-
34	I	ED[0]	BT.656 encoder data input	Pull-down	Open	-
35	I	ED[1]	BT.656 encoder data input	Pull-down	Open	-
37	I	ED[2]	BT.656 encoder data input	Pull-down	Open	-
38	I	ED[3]	BT.656 encoder data input	Pull-down	Open	-
40	I	ED[4]	BT.656 encoder data input	Pull-down	Open	-
41	I	ED[5]	BT.656 encoder data input	Pull-down	Open	-
43	I	ED[6]	BT.656 encoder data input	Pull-down	Open	-

Pin Descriptions (Continued)

PIN#	I/O	PIN NAME	DESCRIPTION	INTERNAL CONNECTION (Notes 4, 5)	RECOMMENDED CONNECTION WHEN UNUSED	STATUS AFTER HW RESET
44	I	ED[7]	BT.656 encoder data input	Pull-down	Open	-
46	I/O	ENCLK	BT.656 encoder clock input/output	Pull-down	Open	Hi-Z
SYSTEM CONTROL PINS						
25	I	RSTB	System reset	Pull-up	-	-
4	I	XTI	Crystal 27MHz (54MHz) connection or oscillator clock input	-	-	-
5	O	XTO	Crystal 27MHz (54MHz) connection	-	Open	-
21	I	TEST	Test pin. Connect to ground	Pull-down	Ground	-
27	I	SCLK	Serial control clock line	Pull-up	-	-
28	I/O	SDAT	Serial control data line	Pull-up	-	Hi-Z
22	I	SADD0	Serial control address	Pull-down	-	-
23	I	SADD1	Serial control address	Pull-down	-	-
30	O	IRQ	Interrupt request output	-	Open	-
31	I	PD	Power-down (1: Power-down, 0: Normal operation)	Pull-down	Ground	-
32	O	MPP	Multipurpose output pin	Pull-up	Open	Hi-Z
POWER AND GROUND PINS						
3, 11, 26, 36, 47	P	VDDI	Digital core power 1.2V	-	-	-
8, 17, 20, 33, 42	P	VDDO	Digital I/O power 3.3V/1.8V	-	-	-
6, 14, 24, 29, 39, 45	P	VSS	Digital ground	-	-	-
52, 60, 68	P	VDDV	Analog video ADC power 3.3V	-	-	-
56, 64	P	VSSV	Analog video ADC ground	-	-	-
51	P	VDDVD	Analog video DAC power 3.3V	-	-	-
48	P	VSSVD	Analog video DAC ground	-	-	-
1	P	VDDAP	Analog clock PLL/Short detection power 3.3V	-	-	-
2	P	VSSAP	Analog clock PLL/Short detection ground	-	-	-

NOTES:

- For 3.3V VDDO, the pull-up resistor has a typical value of 85kΩ. The pull-down resistor has a typical value of 79kΩ.
- For 1.8V VDDO, the pull-up resistor has a typical value of 198kΩ. The pull-down resistor has a typical value of 185kΩ.

Absolute Maximum Ratings

VDDI to VSS	-0.5V to +1.6V
VDDO to VSS	-0.5V to +2.3V
VDDV to VSSV	-0.5V to +4.2V
VDDVD to VSSVD	-0.5V to +4.2V
VDDAP to VSSAP	-0.5V to +4.2V
Any Digital Pin to VSS	-0.5V to +5.5V
Any Analog Pin to AVSPLL	-0.5V to +2.3V
ESD Ratings	
Human Body Model (Tested per AEC-Q100-002E)	2kV
Machine Model (Tested per AEC-A100-003E)	200V
Charged Device Model (Tested per AEC-Q100-011C)	750V
Latch-Up (Tested per AEC-Q100-004D; Class 2, Level A)	100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
68 Ld 10x10 WQFN (Notes 6, 7)	23	1
Junction Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Ambient Temperature Range	-40°C to +105°C	
Pb-Free Reflow Profile	see TB493	

Recommended Operating Conditions

VDDI	+1.08V to +1.32V
VDDO	+1.62V to +3.6V
VDDV, VDDVD, VDDAP	+2.97V to +3.6V
Ambient Temperature Range	-40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See [TB379](#).
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Parameters

Unless otherwise noted, the typical specifications are measured at the following conditions:

VDDI = 1.2V, VDDO = VDDVD = VDDAP = 3.3V, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.

PARAMETER	SYMBOL	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
DIGITAL INPUTS					
Input High Voltage (at VDDO = 3.3V)	V_{IH}	2.0		3.6	V
Input Low Voltage (at VDDO = 3.3V)	V_{IL}	-0.3		0.8	V
Input High Voltage (at VDDO = 1.8V)	V_{IH}	1.17		1.98	V
Input Low Voltage (at VDDO = 1.8V)	V_{IL}	-0.3		0.63	V
Input Leakage Current (at $V_I = 3.3\text{V}$ or 0V)	I_L			± 10	μA
Input Capacitance	C_{IN}		6		pF
DIGITAL OUTPUTS					
Output High Voltage (at VDDO = 3.3V)	V_{OH}	2.4			V
Output Low Voltage (at VDDO = 3.3V)	V_{OL}			0.4	V
Output High Voltage (at VDDO = 1.8V)	V_{OH}	1.35			V
Output Low Voltage (at VDDO = 1.8V)	V_{OL}			0.45	V
High Level Output Current (at VDDO = 1.8V)	I_{OH}	2.4			mA
Low Level Output Current (at VDDO = 1.8V)	I_{OL}	3.5			mA
Tri-State Output Leakage Current (at $V_O = 3.3\text{V}$ or 0V)	I_{OZ}			± 10	μA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF
SUPPLY CURRENT					
Analog Video ADC Supply Current (VDDV, 3.3V)	I_{DDV}		66		mA
Analog Video DAC Supply Current (VDDVDA, 3.3V)	I_{DDVDA}		45		mA
Clock PLL Supply Current (VDDAPLL, 3.3V)	I_{DDAPLL}		3		mA
Digital Internal Supply Current (VDDI, 1.2V)	I_{DDI}		30		mA
Digital I/O Supply Current (VDDO, 3.3V)	I_{DDO}		32		mA
Total Power Dissipation	P		550		mW

XTI and Video Data/Sync Timing

PARAMETER	SYMBOL	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Hold from CLK0 to Video Data/Sync (27MHz)	2a	3			ns
Delay from CLK0 to Video Data/Sync (27MHz)	2b			7	ns
Hold from CLK0 to Video Data/Sync (54MHz)	4a	3			ns
Delay from CLK0 to Video Data/Sync (54MHz)	4b			7	ns
Hold from CLK0 to Video Data/Sync (108MHz)	6a	3			ns
Delay from CLK0 to Video Data/Sync (108MHz)	6b			7	ns

NOTE:

8. CLK0 timing is related to the CLK0_DEL register value. The timing diagram in [Figure 2](#) illustrates when CLK0_DEL is set to 0 hex and CLK0_POL is set to 0.

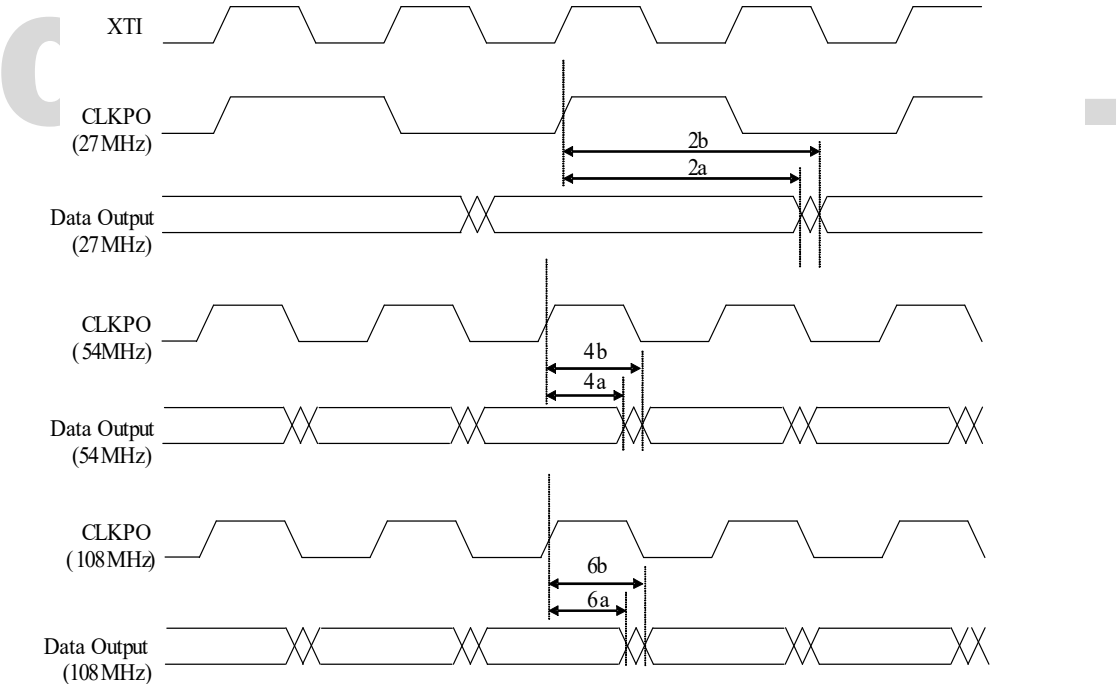


FIGURE 2. XTI AND VIDEO DATA TIMING DIAGRAM

Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Bus-Free Time Between STOP and START	t_{BF}	740			ns
SDAT Set-Up Time	t_{sSDAT}	100			ns
SDAT Hold Time (XTI 108MHz)	t_{hSDAT}	50			ns
SDAT Hold Time (XTI 54MHz)		100			ns
Set-Up Time for START Condition	t_{sSTA}	370			ns
Set-Up Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for Each Bus Line	C_{BUS}			400	pF
LOW Period of SCLK	t_{LOW}	0.5			μ s
HIGH Period of SCLK	t_{HIGH}	0.5			μ s
SCLK Clock Frequency	f_{SCLK}			800	kHz

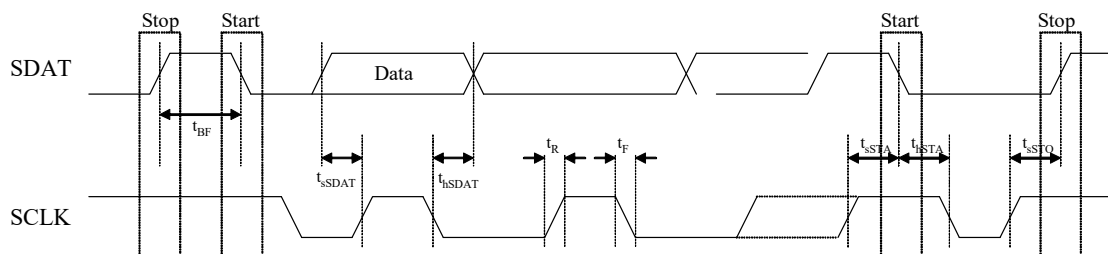


FIGURE 3. SERIAL HOST INTERFACE TIMING DIAGRAM

Video Decoder Parameter

PARAMETER	SYMBOL	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
ADCs					
ADC Resolution	ADCR		10		Bits
ADC Integral Nonlinearity	AINL		± 1		LSB
ADC Differential Nonlinearity	ADNL		± 1		LSB
ADC Clock Rate	f_{ADC}	24	27	30	MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}		15.625		kHz
Line Frequency (60Hz)	f_{LN}		15.734		kHz
Static Deviation	Δf_H			6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}		3579545		Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}		4433619		Hz
Subcarrier Frequency (PAL-M)	f_{SC}		3575612		Hz

Video Decoder Parameter (Continued)

PARAMETER	SYMBOL	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Subcarrier Frequency (PAL-N)	f_{SC}		3582056		Hz
Lock -In Range	Δf_H	± 450			Hz
CRYSTAL OSCILLATOR INPUT REQUIREMENT					
Nominal Frequency			27		MHz
Deviation				± 50	ppm
Duty Cycle				55	%
LOCK SPECIFICATION					
Sync Amplitude Range		1		200	%
Color Burst Range		5		200	%
Horizontal Lock Range		-5		5	%
Vertical Lock Range		45		65	Hz
F_{SC} Lock Range			± 450		Hz
Color Burst Position Range			± 2.2		μs
Color Burst Width Range		8	9	10	cycle
VIDEO BANDWIDTH					
B/W			6		MHz
NOISE SPECIFICATION					
SNR (Luma Flat Field)			57		dB
NONLINEAR SPECIFICATION					
Y Nonlinearity			0.5		%
Differential Phase	DP		0.4		°
Differential Gain	DG		0.6		%
CHROMA SPECIFICATION					
Hue Accuracy			1		°
Chroma ACC Range				400	%
Chroma Amplitude Error			1		%
Chroma Phase Error			0.3		%
Chroma Luma Intermodulation			0.2		%
K-FACTOR					
K2T			0.5		%
Kpulse/bar			0.5		%

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Functional Description

Video Input Formats

The TW9984 has built-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency, and frame rate to identify NTSC, PAL, and SECAM color signals. The TW9984 can identify the following standards: NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60), and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

The TW9984 supports all common video formats as shown in [Table 1](#).

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW9984

FORMAT	LINES	FIELDS	F _{sc} (MHz)	COUNTRY
NTSC-M	525	60	3.579545	U.S., many others
NTSC-Japan (Note 10)	525	60	3.579545	Japan
PAL-B, G, N	625	50	4.433619	Many
PAL-D	625	50	4.433619	China
PAL-H	625	50	4.433619	Belgium
PAL-I	625	50	4.433619	Great Britain, others
PAL-M	525	60	3.575612	Brazil
PAL-CN	625	50	3.582056	Argentina
SECAM	625	50	4.406 4.250	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619	China
NTSC (4.43)	525	60	4.433619	Transcoding

NOTE:

10. NTSC-Japan has 0 IRE setup.

Analog Front-End

The TW9984 has four 10-bit Analog-to-Digital Converters (ADCs) to digitize the analog video inputs. The ADC can be set to power-down mode by the V_ADC_PWDN register. The TW9984 also contains an antialiasing filter to prevent out-of-band frequencies in analog video input signals. No external components are required in the analog input pins except an AC coupling capacitor and termination resistor. [Figure 4](#) shows the frequency response of the antialiasing filter.

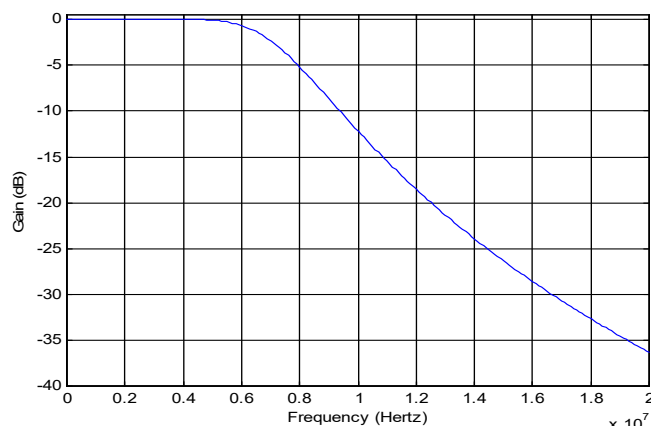


FIGURE 4. ANTIALIASING FILTER FREQUENCY RESPONSE

DECIMATION FILTER

The digitized composite video data are oversampled to simplify the analog filter design. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image when down-sampled. [Figure 5](#) shows the characteristic of the decimation filter.

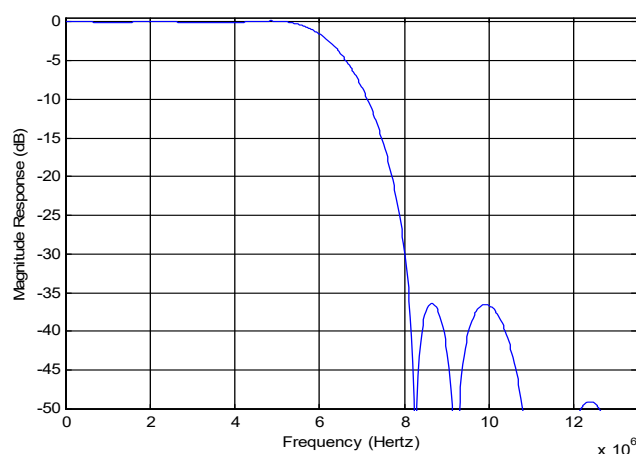


FIGURE 5. CHARACTERISTIC OF THE DECIMATION FILTER

Automatic Gain Control and Clamping

All four analog channels have a built-in clamping circuit that restores the signal DC level. The video input restores the back porch of the digitized video to a level of 60. This operation is automatic through an internal feedback loop. The video input Automatic Gain Control (AGC) adjusts input gain so that the sync tip is at an appropriate level. Programmable white peak protection logic prevents saturation in the case of abnormal signal proportion between sync and white peak level.

Sync Processing

The sync processor detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in both stable signals and unstable signals.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. The actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input.

Y/C Separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multistandard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be performed either by comb filter or notch/bandpass filter combination. For SECAM standard signals, adaptive notch/bandpass filter is used. The default selection for NTSC/PAL is comb filter.

COMB FILTER

The TW9984 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current, and next lines. This technique leads to excellent Y/C separation with small cross luma and cross color at both horizontal and vertical edges.

Due to the line buffer used in the comb filter, there is always a two line processing delay at the output, except for the component input mode, which has only one line of delay.

NOTCH/BANDPASS FILTER

The characteristics of the notch and bandpass filters are shown in [Figures 6 and 7](#).

[Figure 6](#) shows the frequency response of the notch filter for each system NTSC and PAL. [Figure 7](#) shows the frequency response of chroma bandpass filter curves.

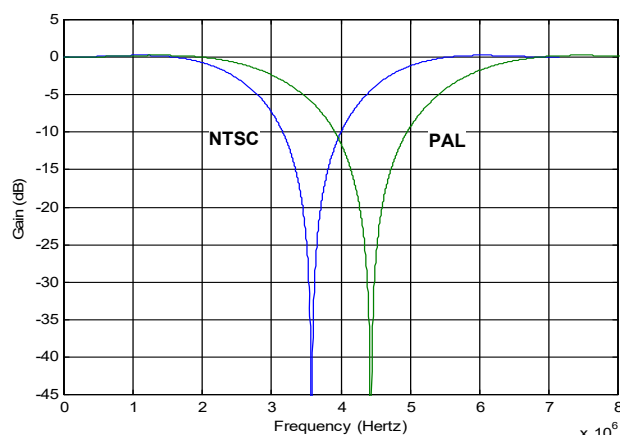


FIGURE 6. THE CHARACTERISTICS OF LUMINANCE NOTCH FILTER FOR PAL

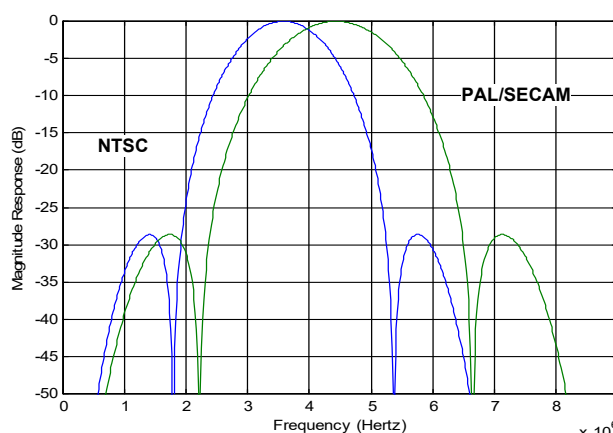


FIGURE 7. CHROMA BANDPASS FILTER CURVES

Color Decoding

CHROMINANCE DEMODULATION

NTSC and PAL standard signals are color demodulated by first quadrature mixing the chroma signal to the base band. A low-pass filter then removes the carrier signal and yields chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For PAL systems, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the color information is FM modulated onto a different carrier. The demodulation process therefore consists of FM demodulation and filter de-emphasis. During an FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The subcarrier signal for use in the color demodulator is generated by a direct digital synthesis PLL that locks onto the input subcarrier reference (color burst). This arrangement allows any substandard of NTSC and PAL to be demodulated easily with a single crystal frequency.

[Figure 8](#) shows the frequency response of chrominance low-pass filter curves.

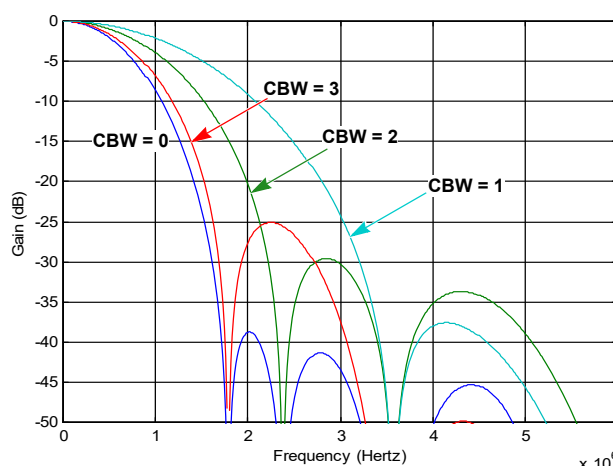


FIGURE 8. CHROMINANCE LOW-PASS FILTER CURVES

ACC (AUTOMATIC CHROMA GAIN CONTROL)

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chroma output gain. The ACC range is -6dB to +24dB.

Chrominance Processing

CHROMINANCE GAIN, OFFSET, AND HUE ADJUSTMENT

When decoding NTSC signals, the TW9984 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. The NTSC phase shift decoding can be programmed through a control register. For the PAL standard, the PAL delay line compensates any hue error; therefore, no hue adjustment is available. The color saturation can be adjusted by changing the gain of the Cb and Cr signals for all NTSC, PAL, and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

CTI (COLOR TRANSIENT IMPROVEMENT)

The TW9984's Color Transient Improvement (CTI) function further enhances the image quality. CTI enhances the color edge transient without any overshoot or undershoot.

Luminance Processing

The TW9984 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW9984 also provides a programmable peaking function that further enhances the video sharpness. The peaking control has a built-in coring function to prevent enhancement of noise.

[Figure 9](#) shows the characteristics of the peaking filter for four different gain modes and four different center frequencies.

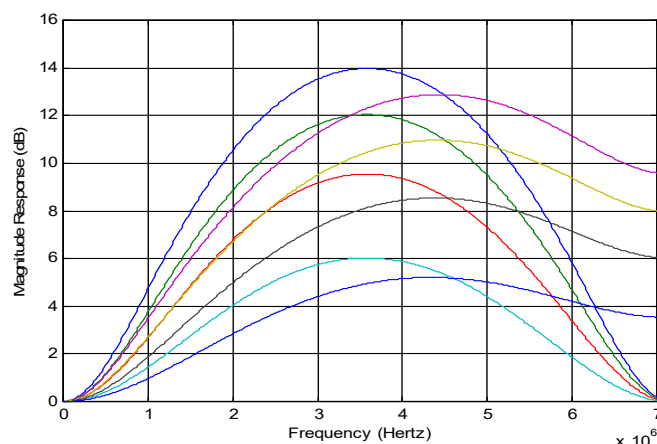


FIGURE 9. THE CHARACTERISTIC OF LUMINANCE PEAKING FILTER

Short Diagnostics

SHORT-TO-BATTERY AND SHORT-TO-GROUND

The TW9984 provides Short-to-Battery (STB) and Short-to-Ground (STG) detection capabilities. The short diagnostics module has four channels, one for each video input. Both STB and STG

support 8-step programmable threshold levels (three bits per threshold). The STG thresholds range from 1/16 to 8/16 of the 1.8V power supply. The STB thresholds range from 1/16 to 15/16 of the 1.8V power supply. STB and STG events can be detected either by polling registers or by using the interrupt pin.

Video Cropping

Cropping allows only a subsection of a video image to be output. The active video region is determined by the HDELAY, HACTIVE, VDELAY, and VACTIVE registers as illustrated in [Figure 10](#). The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field. The HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of HSYNC. The start of the active lines from the vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by the HDELAY, HACTIVE, VDELAY, and VACTIVE registers, which are eight bits wide. The lower eight bits are in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. The upper two bits share the same register, CROP_HI.

The Horizontal Delay register (HDELAY) determines the number of pixels of delay between the leading edge of HSYNC and the leading edge of HACTIVE.

Note: This value is referenced to the unscaled pixel number. The Horizontal Active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the unscaled pixel number.

Therefore, if the scaling ratio is changed, the active video region used for scaling remains unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. For cropping to work properly, [Equation 1](#) must be true.

$$\text{HDELAY} + \text{HACTIVE} < \text{Total number of pixels per line} \quad (\text{EQ. 1})$$

For NTSC output at 13.5MHz pixel rate, the total number of pixels is 858. For PAL output at 13.5MHz rate, the total number of pixels is 864. HACTIVE should be set to 720.

The Vertical Delay register (VDELAY) determines the number of lines of delay between the leading edge of the VSYNC and the start of the active video lines. VDELAY indicates the number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for 60Hz systems and 625 for 50Hz systems. The Vertical Active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register, depending on the vertical scaling ratio. For vertical cropping to work properly, [Equation 2](#) must be true.

$$\text{VDELAY} + \text{VACTIVE} < \text{Total number of lines per field} \quad (\text{EQ. 2})$$

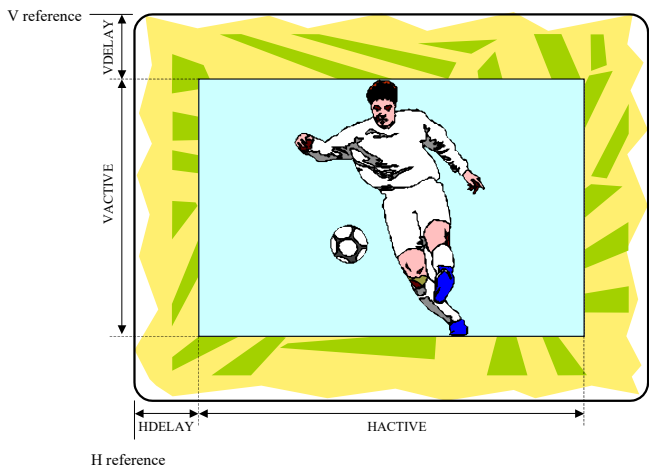


FIGURE 10. THE EFFECT OF CROPPING REGISTERS

Output Format

The TW9984 supports a standard ITU-R BT.656 format. All video data and timing signals of four channels are synchronous with the pins' CLKO output. Therefore, CLKO can be connected to 4-channel interfaces for synchronizing data. The phase of CLKO can be independently controlled by the registers CLKO_DEL (Delay) and CLKO_POL (Polarity Inverse).

ITU-R BT.656 FORMAT

In the ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. The number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 11. The SAV and EAV sequences are shown in Table 2. An optional set of 656 SAV/EAV code sequences can be enabled to identify a no-video status using the NOVID_656 bit.

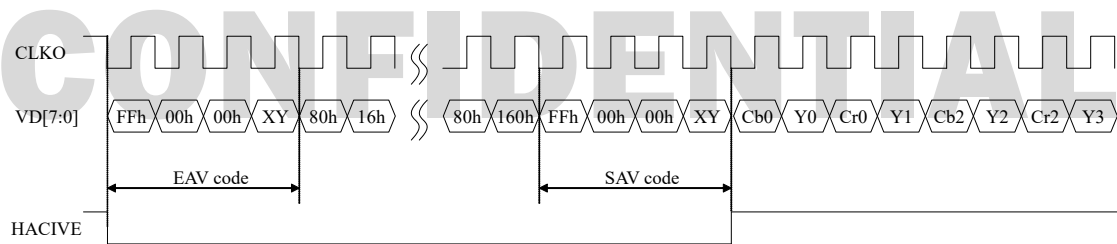


FIGURE 11. ITU-R BT.656 FORMAT TIMING DIAGRAM

TABLE 2. ITU-R BT.656 SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	FOURTH	
									NORMAL	OPTION (Note 11)
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

NOTE:
11. Option includes video loss information in ITU-R BT.656.

**TWO CHANNEL ITU-R BT.656 TIME-MULTIPLEXED
FORMAT WITH 54MHz**

The TW9984 supports a two channel ITU-R BT.656 time-multiplexed format with 54MHz that is useful for security applications requiring two channel outputs through one channel video port. The CHMD1 register enables the dual ITU-R BT.656 Time-multiplexed format and the MAINCH/SELCH register selects channel output to be multiplexed on the VD pin. To demultiplex the Time-multiplexed data in the back end chip, the channel ID

can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format are supported:

- Horizontal blanking code with channel ID
- ITU-R BT.656 sync code with channel ID

Figure 12 illustrates the logical timing diagram for CH1 and CH2 time-multiplexed output through the CH1 video output port. Figures 13 and 14 illustrate VD[7:0]/CLKO pin default timing with 54MHz and 27MHz clock output modes.

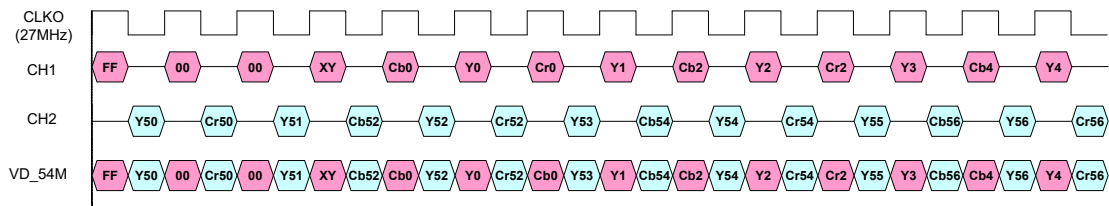


FIGURE 12. TIMING DIAGRAM OF TWO CHANNEL TIME-MULTIPLEXED FORMAT

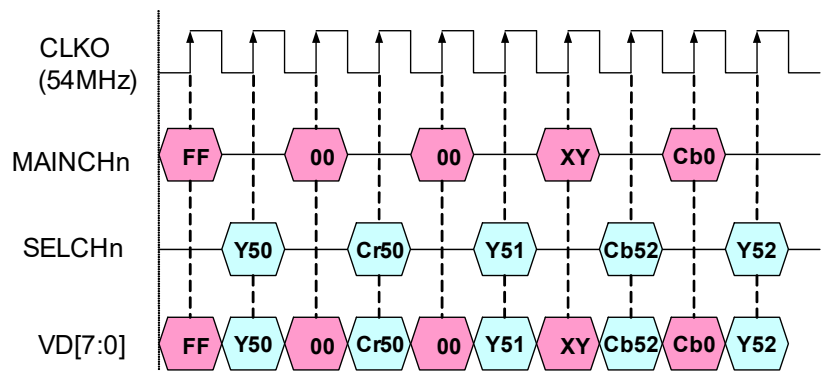


FIGURE 13. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 54MHz CLOCK

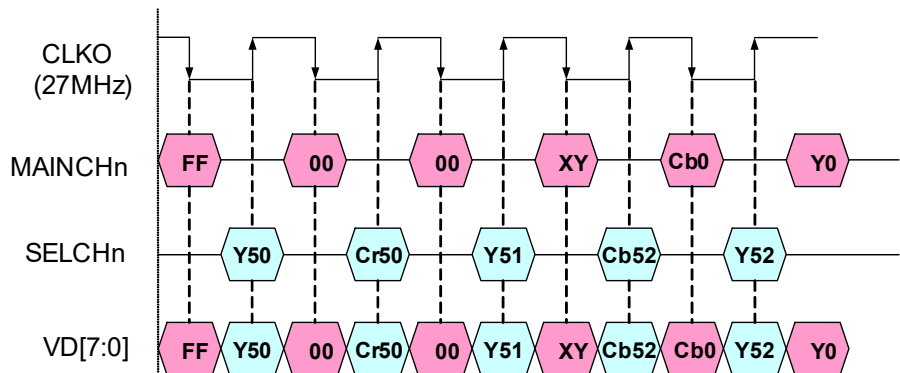


FIGURE 14. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH 27MHz CLOCK

FOUR CHANNEL D1 TIME-DIVISION-MULTIPLEXED FORMAT WITH 108MHz

The TW9984 implements four channels of D1 (720x480) at 27MHz video stream that are time-division-multiplexed at 108MHz data rate format for security surveillance applications. To reduce pin counts and thus reduce chip size, the TW9984 implements a single 8-bit bus at 4x the base band pixel clock rate of 27MHz on both the decoder's digital output port and the input port of the back end compression Codec devices. While quadrupling the data rate on a single bus to meet the new

requirement, individually, each channel data arrangement still retains the base band 27MHz ITU-R BT.656 specification. For interfaces that can accept the new 108MHz clock bus, only one single clock at 108MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for demultiplexing and separation of channel data. [Figure 15](#) depicts the temporal arrangement of the video data at the 108MHz data rate. Each channel is byte level time-division multiplexed (TDM). The main clock is 108MHz.

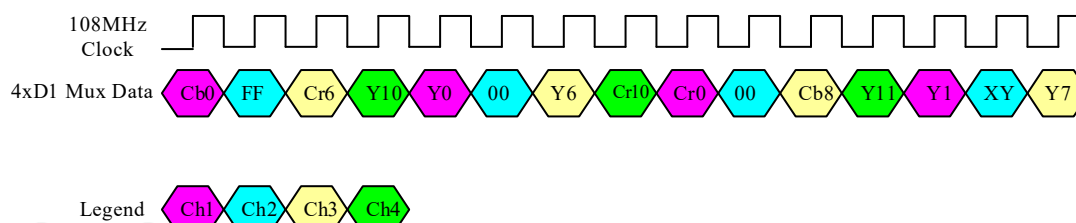


FIGURE 15. TIMING DIAGRAM OF 108MHz 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA

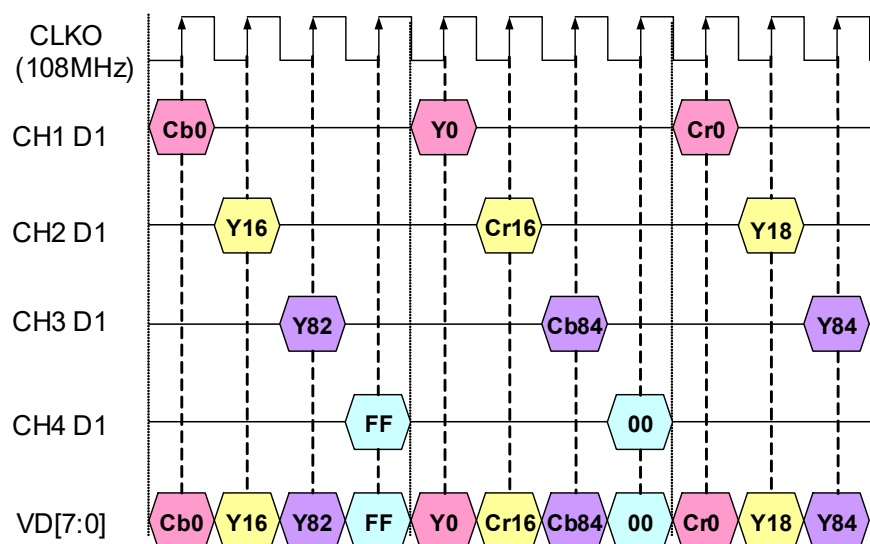


FIGURE 16. PIN OUTPUT TIMING OF 108MHz 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH 108MHz CLOCK

TABLE 3. SPECIAL FORMAT OF ITU-R BT. 656 EMBEDDED TIMING CODE AND CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
FIELD	V-TIME	H-TIME	F	V	H	FIRST	SECOND	THIRD	FOURTH			
									CH1	CH2	CH3	CH4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

OUTPUT ENABLING ACT

After power-up, the TW9984 registers have unknown values. The RSTB pin must be asserted and released to bring all registers to their default values. After reset, the TW9984 data outputs are tri-stated. The OE register should be written after reset to enable the outputs.

VIDEO OUTPUT CHANNEL SELECTION

If CHMD1[1:0] in Reg0xCA is set to 0hex, MAINCH[1:0] in Reg0xCD selects one number of video channels to be output on VD[7:0] pin as a Single Channel ITU-R BT.656(D1) format output. If CHMD[1:0] in Reg0xCA is set to 1hex, MAINCH[1:0] in Reg0xCD and SELCH[1:0] in Reg0xCC select two numbers of Video Channels to be output on the VD[7:0] pin as a Two Channel ITU-R BT.656 (D1) Time-multiplexed format output. If CHMD[1:0] in

Reg0xCA is set to 2hex, the Four Channel ITU-R BT.656 (D1) time-multiplexed format is output on the VD[7:0] pin.

EXTRA SYNC OUTPUT

The MPP pin supports additional timing information such as syncs and field flag. The video output timing is illustrated in Figures 17 and 18. The TW9984 HS/VS/FLD output function is compatible to TW9907 Video decoder HSYNC/VS/FLD output function. Start of VS timing is controlled by the VSHT register (V timing) and OVSDLY register (H timing). End of VS timing is controlled by the OVSEND register (V timing). Start of FLD timing is controlled by the OFDLY register (V timing). Start of HS timing is controlled by the HSBEGIN register and end of HS timing is controlled by the HSEND register.

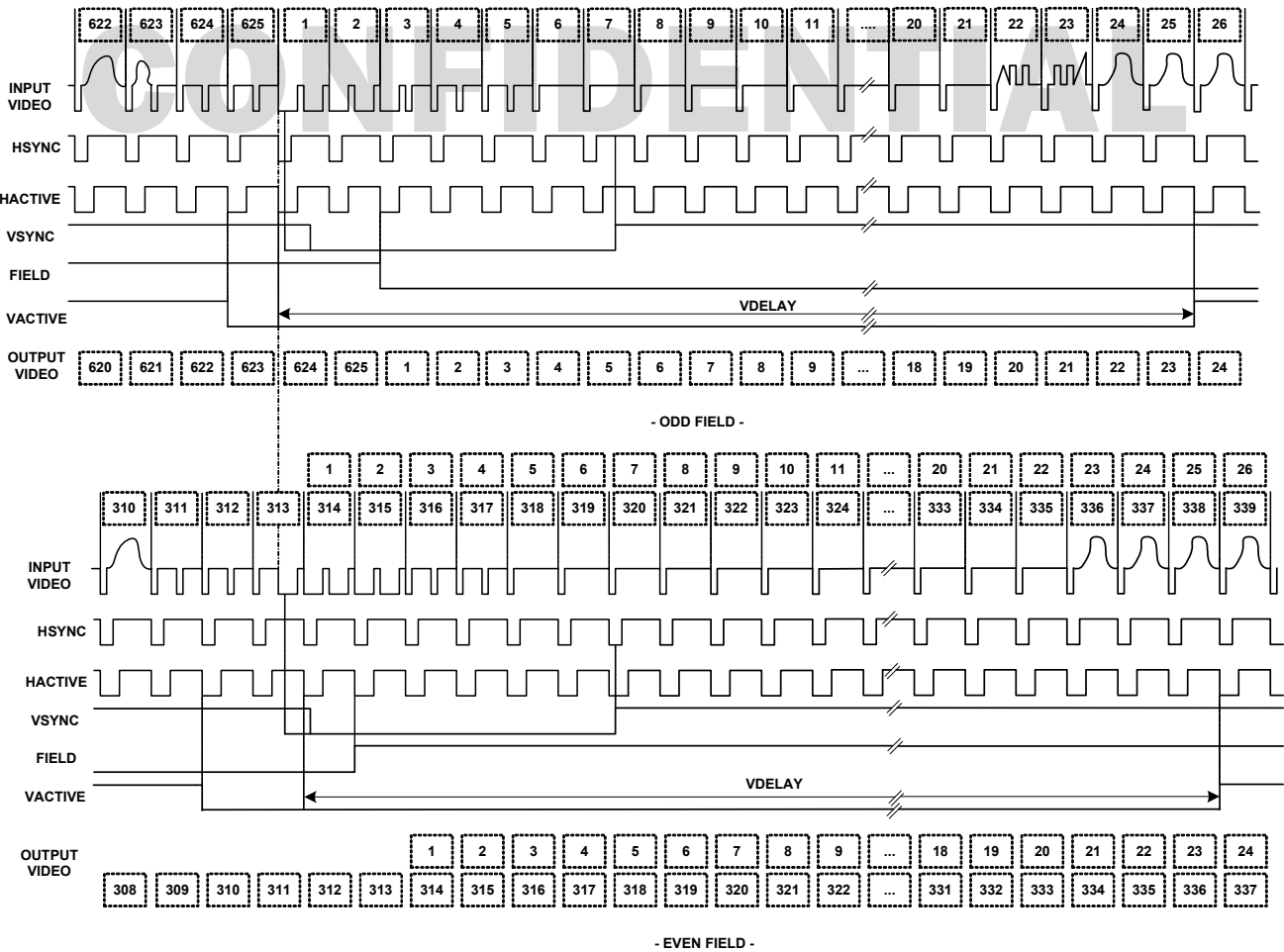


FIGURE 17. VERTICAL TIMING DIAGRAM FOR 60Hz/525 LINE SYSTEM

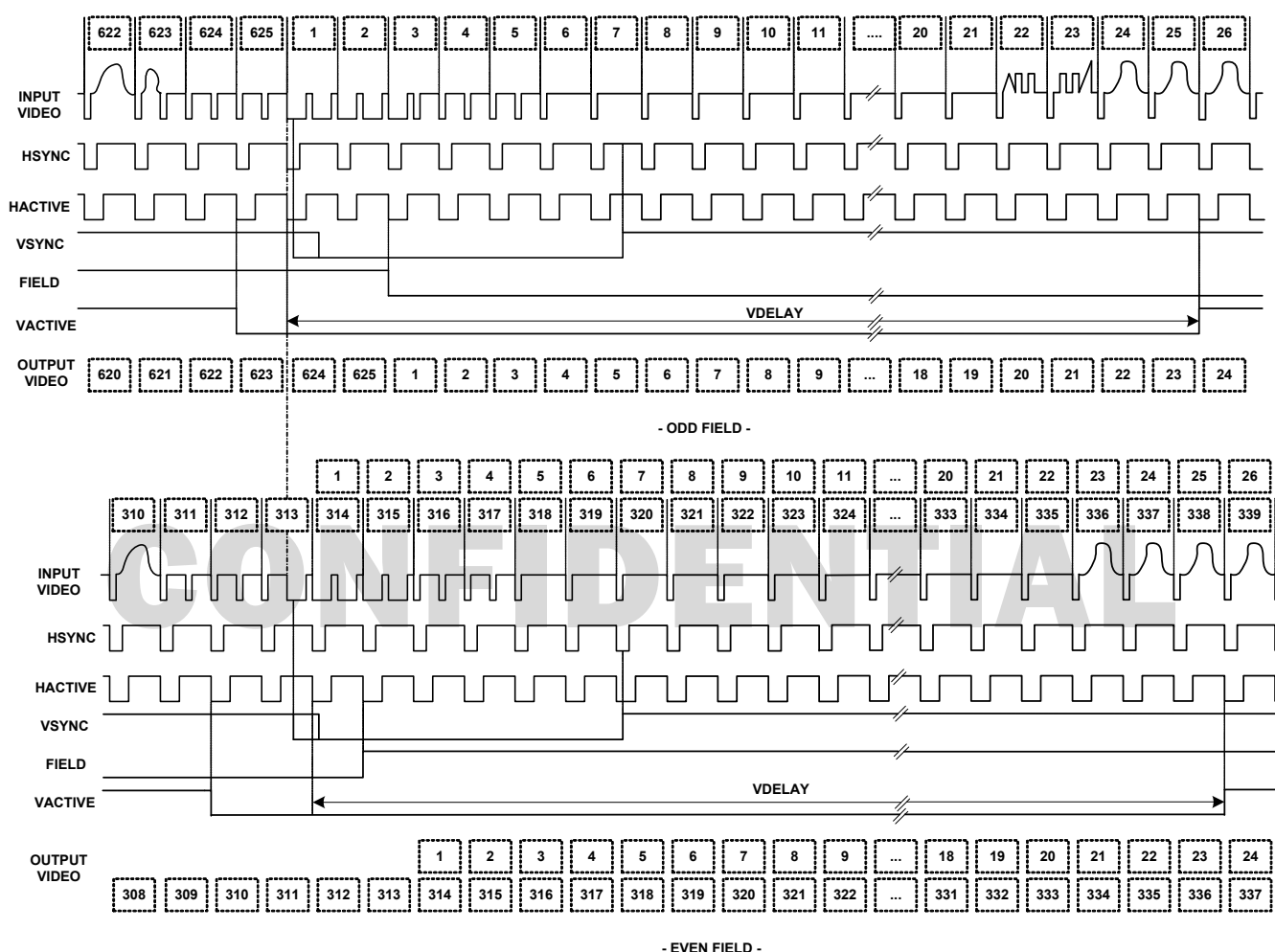


FIGURE 18. VERTICAL TIMING DIAGRAM FOR 50Hz/625 LINE SYSTEM

Video Encoder

The TW9984 has a built-in NTSC/PAL video encoder to support analog video output. It converts the standard digital ITU-R BT.656 data stream into an analog composite output through a 10-bit video DAC. The digital video data is first gain adjusted according to the format selected. The luminance signal is band-limited to 6MHz before it is interpolated to a 27MHz sampling rate. The chrominance is also band-limited to the selected bandwidth before it is modulated with the internal generated subcarrier and interpolated to a 27MHz sampling rate. These signals are finally combined with sync information before they are sent to the DAC. The encoder can operate in either master or slave clock mode. In master mode, the clock comes from the internally generated 27MHz clock. The NTSC output can be selected to include a 7.5 IRE pedestal. The luminance, chrominance, sync, and burst amplitude can be adjusted independently. The encoder also has a built-in color bar pattern generator for video adjustment. The encoder block diagram is shown in [Figure 19](#) and input timing is shown in [Figure 20](#).

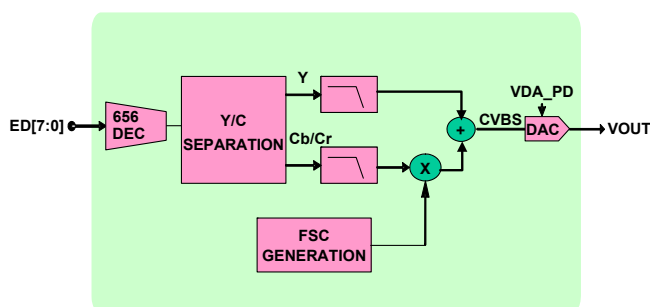
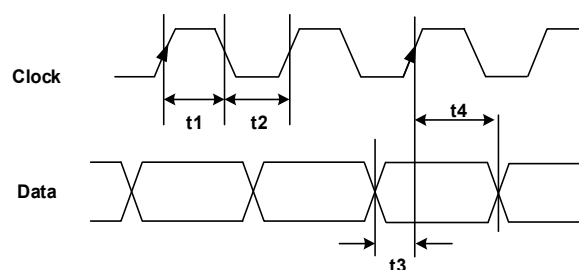


FIGURE 19. ENCODER BLOCK DIAGRAM



ITEM	SYMBOL	MIN	TYP	MAX	UNIT
CLK Cycle Time		-	27	-	MHz
Clock High Time	t_1	8	-	-	ns
Clock Low Time	t_2	8	-	-	ns
Data Setup Time	t_3	12	-	-	ns
Data Hold Time	t_4	2	-	-	ns

FIGURE 20. VIDEO ENCODER INPUT TIMING

OUTPUT STANDARD SELECTION

The TW9984 supports various video standard outputs from the HZ50 and FSCSEL, PHALT, and PED registers as described in [Table 4](#).

TABLE 4. ANALOG OUTPUT VIDEO STANDARDS

FORMAT	SPECIFICATION			REGISTER			
	LINE/Fv (Hz)	Fh (kHz)	Fsc (MHz)	HZ50	FSCSEL	PHALT (Note 12)	PED
NTSC-M	525/59.94	15.734	3.579545	0	0	0	1
NTSC-J							0
NTSC-4.43	525/59.94	15.734	4.43361875	0	1	0	1
NTSC-N	625/50	15.625	3.579545	1	0	0	0
PAL-BDGIH	625/50	15.625	4.43361875	1	1	1	0
PAL-N							1
PAL-M	525/59.94	15.734	3.57561149	0	2	1	0
PAL-NC	625/50	15.625	3.58205625	1	3	1	0
PAL-60	525/59.94	15.734	4.43361875	0	1	1	0

NOTE:

12. If the PHALT register is set to **1**, phase alternation can be reset every eight fields so that phase alternation keeps the same phase every eight fields.

Chrominance Filter

The bandwidth of the chrominance signal can be selected with the CBW register as shown in [Figure 21](#).

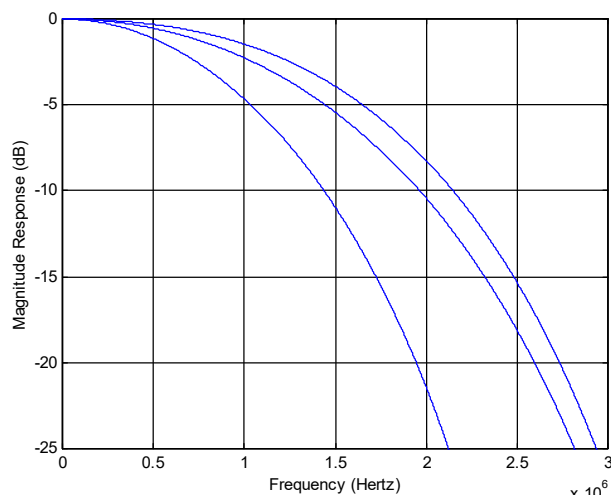


FIGURE 21. CHARACTERISTICS OF CHROMINANCE FILTER

Digital-to-Analog Converter

Digital video data from the video encoder is converted to analog video signal by the Digital-to-Analog Converter (DAC). The V_{OUT} port always outputs the CVBS signal. The DAC can be disabled by the VDA_PD register to save power. The full-scale current can be controlled by the external R_{SET} resistor.

A simple reconstruction filter is required externally to reject noise as shown in [Figure 22](#).

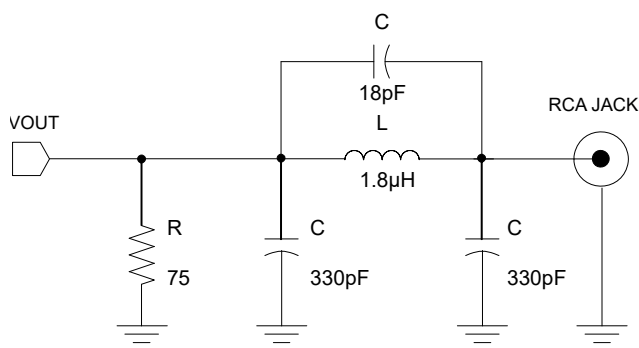


FIGURE 22. EXAMPLE OF RECONSTRUCTION FILTER

Host Interface

Serial Interface

The two-wire serial bus interface allows an external microcontroller to write to or read from the data through the TW9984 register. The SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by the resistors connected to VDD. The SADD[1:0] defines two LSBs of the slave device address by tying the SADD pins either to VDD or GND.

SLAVE ADDRESS						R/W
0	1	0	1	0	SADD[1] SADD[0]	1 = Read 0 = Write

The TW9984 supports auto index increments in write/read mode if the data are in sequential order. The data transfer rate on the bus is up to 400kbits/s.

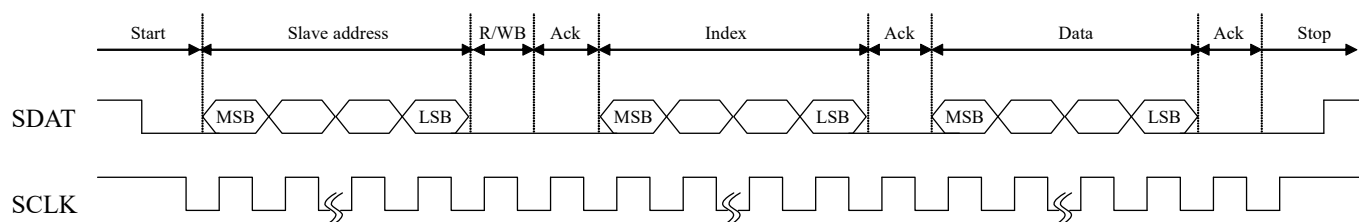


FIGURE 23A. WRITE MODE

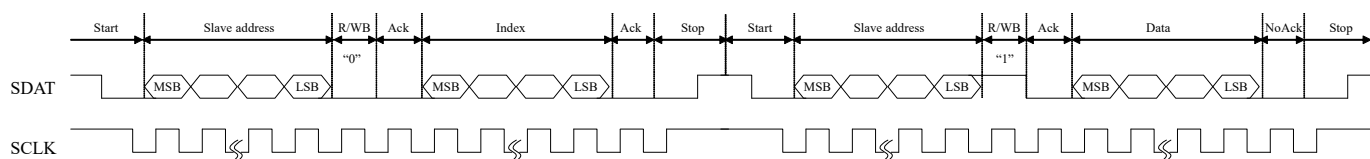


FIGURE 23B. READ MODE
FIGURE 23. TIMING CHART OF SERIAL INTERFACE

Interrupt Interface

The TW9984 provides the interrupt request function using an IRQ pin so the host does not need to waste resources to detect a video signal from the TW9984. To use the interrupt request function, enable the interrupt request with IRQENA and select the polarity of the IRQ pin with IRQPOL. Also, each video detection

channel should be enabled by the VDET_ENA and short detection should be enabled by BSDET_ENA (battery short detection enable) and GSDET_ENA (ground short detection enable). The interrupt trigger mode for video detection should be defined by the VDET_MODE. For short detection, a level trigger is used for interrupt to set the status registers VDET_STATE, BDET_STATE, and GDET_STATE. [Figure 24](#) shows the interrupt operation when

the VDET_MODE is 2 (triggered by the falling edge). The IRQ pin is cleared automatically by reading the VDET_STATE for video detection. When the VDET_MODE is 1 or 2, the status register VDET_STATE is also cleared automatically by reading the VDET_STATE register. However, when the VDET_MODE is 3, the status register VDET_STATE is not cleared automatically, but has the same value as the actual status of the video detection flag.

For STB and STG detection, the interrupt circuit always tries to detect the "High" state of the short detection result (short detected), then sets the status register and output to the IRQ pin. The short detection status output to IRQ can be masked by the BSDET_MASK and GSDET_MASK registers without affecting the contents of the status register. Each of the eight statuses can be reset individually by writing 1 to the corresponding BSDET_CLEAR and GSDET_CLEAR register bits. This operation affects both status register and IRQ output.

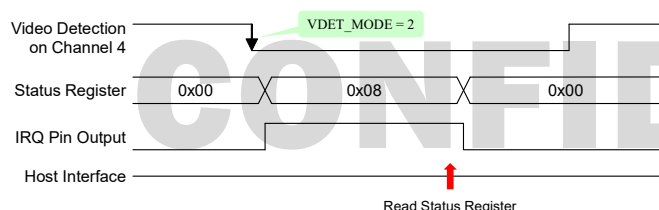


FIGURE 24A. STATUS REGISTER OF AUTOMATIC CLEARED MODE

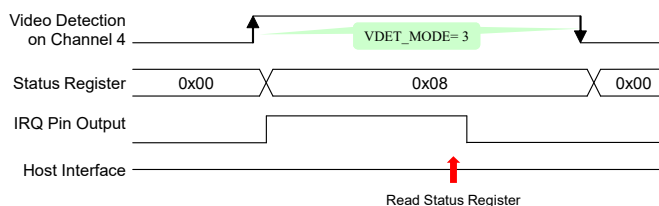


FIGURE 24B. STATUS REGISTER SAME AS VIDEO DETECTION FLAG MODE

FIGURE 24. TIMING DIAGRAM OF INTERRUPT INTERFACE (VIDEO DETECTION)

Squared Pixel Mode Operation

If the FC27 register bit is set to 0, the TW9984 operates in Squared Pixel mode. In PAL-SQ mode, the XTI pin input should be set to either 59MHz (= 29.5MHz x 2) or 29.5MHz. In NTSC-SQ mode, the XTI pin input should be either 49.086MHz (= 24.543MHz x 2) or 24.543MHz. The HACTIVE register value should be 0x300 (768dec) for PAL-SQ and 0x280 (640dec) for NTSC-SQ.

Clock PLL

The TW9984 has a built-in 2x/4x clock PLL to generate a frequency that is 2x or 4x the XTI clock. If a 54MHz crystal is connected to XTI pin, the SEL_X24 register needs to be 0 (2x mode). If a 27MHz crystal is connected to the XTI pin, the SEL_X24 register needs to be 1 (4x mode, default). The XTMD register selects which clock source is used in the system. If the analog clock PLL is not used, the XTMD register needs to be set to an adequate value to match the XTI input clock frequency.

Control Register

Register Map

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE	
CH1	CH2	CH3	CH4											
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FIELD*	VLOCK*	RESERVED*	MONO*	DET50*	–	
0x01	0x11	0x21	0x31	BRIGHT	BRIGHT								00h	
0x02	0x12	0x22	0x32	CONTRAST	CNTRST								64h	
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARP				11h	
0x04	0x14	0x24	0x34	SAT_U	SAT_U								80h	
0x05	0x15	0x25	0x35	SAT_V	SAT_V								80h	
0x06	0x16	0x26	0x36	HUE	HUE								00h	
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]	VACTIVE[9:8]			HDELAY[9:8]	HACTIVE[9:8]			12h	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]								12h	
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]								20h	
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]								0Ah	
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]								D0h	
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MVCSN*	CSTRIPE*	CTYPE*	–	
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	RESERVED			–	
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STD			-7h	
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL6_EN	PALN_EN	PALM_EN	NT44_EN	SEC_EN	PALB_EN	NTSC_EN	7Fh	
0xE4	0xE7	0xEA	0xED	RESERVED	RESERVED									
0xE5	0xE8	0xEB	0xEE	RESERVED	RESERVED									
0xE6	0xE9	0xEC	0xEF	RESERVED	RESERVED									
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH						1Ah	
0xC4	0xC5	0xC6	0xC7	HREF*	HFREF								–	
0x41				ENCCTL	HZ50	INTERLACE	FSCSEL		COFF	PHALT	PDRST	PED	40h	
0x42				ENCTEST1	YBW		CBW		CBGEN	TCSEL			90h	
0x43				ENCCLK	CKMST	ENCCCKPOL	NONSTA	FRUN	YDEL					08h
0x44				ENCOUT	CVBS_YSEL	RESERVED	ENCTMODE						00h	
0x45				SCH	SCH								38h	
0x46				ENCYGAIN	ENCYGAIN								80h	
0x47				ENCCGAIN	ENCCGAIN								80h	

Register Map (Continued)

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE	
CH1	CH2	CH3	CH4											
0x48				ENCSGAIN	ENCSGAIN								80h	
0x49				ENCBGAIN	ENCBGAIN								80h	
0x4A				ENCIREF	RESERVED				VDA_IREFY				FFh	
0x4B				ENCTEST2	ENCVDOUT	TEST_DAC	RESERVED	VDA_PD	VDAC_CKPOL	ENC_LOOP	LOOP_CH		30h	
0x4C				EVDELAY	RESERVED			EVDELAY					00h	
0x4D				EHDELAY	RESERVED			EHDELAY					00h	
0x4F				DAIN_SEL	RESERVED		ADDABP	RESERVED			BPCHSEL		00h	
0x59				PDBV	PDBV4B	PDBV3B	PDBV2B	PDBV1B	PDBV4A	PDBV3A	PDBV2A	PDBV1A	00h	
0x5A				VSAVE	AVDSMD	VREF50M_AVDS	BIAS_AVDS		PD_BIAS	VSAVE				07h
0x5B				DO_DRIVE1	RESERVED	VD_OEN	RESERVED	VD_DS	RESERVED	CK_OEN	RESERVED	CK_DS	99h	
0x5C				DO_DRIVE2	RESERVED		BGCTL	RESERVED	LS_OPT_OEN	LS_OEN	LS_OPT_DS	LS_DS	09h	
0x5D				CH2MISC2	NKILL_2	PKILL_2	SKILL_2	CBAL_2	FCS_2	LCS_2	CCS_2	BST_2	E0h	
0x5E				CH3MISC2	NKILL_3	PKILL_3	SKILL_3	CBAL_3	FCS_3	LCS_3	CCS_3	BST_3	E0h	
0x5F				CH4MISC2	NKILL_4	PKILL_4	SKILL_4	CBAL_4	FCS_4	LCS_4	ICCS_4	BST_4	E0h	
0x60				PLL1	RESERVED	PLL_PD	PLL_IREF	SEL_X24	LP_X4		CP_X4		15h	
0x61				PLL2	RESERVED			DECOSC	CKOUTSEL		XTIMD		13h	
0x65				VDOEB	RESERVED			VD4ORD	RESERVED			VD10EB	00h	
0x80				SRST	RESERVED	ENCRST	IRQRST	VOUTRST	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST	00h	
0x81				ACNTL	RESERVED	IREF	VREF	RESERVED	CLKPDN	RESERVED	YFLEN	YSV	02h	
0x82				ACNTL2	CTEST	YCLEN	CKIPOL	RESERVED	GTEST	VLPF	CKLY	RESERVED	00h	
0x83				CNTRL1	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CCh	
0x84				CKHY	GMEN	CKHY		HSDLY					00h	
0x85				SHCOR	SHCOR				VIN4	VIN3	VIN2	VIN1	80h	
0x86				CORING	CTCOR		CCOR		VCOR		CIF		44h	
0x87				CLMPG	CLPEND				CLPST				50h	
0x88				IAGC	NMGAIN				WPGAIN			RESERVED	22h	
0x8A				PEAKWT	PEAKWT								D8h	
0x8B				CLMPL	CLMPLD	CLMPL							BCh	
0x8C				SYNCT	SYNCTD	SYNCT							B8h	

Register Map (Continued)

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE	
CH1	CH2	CH3	CH4											
0x8D				MISSCNT	MISSCNT				HSWIN				44h	
0x8E				PCLAMP	PCLAMP								38h	
0x8F				VCNTL1	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00h	
0x90				VCNTL2	BSHT			VSHT					00h	
0x91				CKILL	CKILMAX		CKILMIN						78h	
0x92				COMB	COMBMD	HTL			VTL				44h	
0x93				LDLY	CKLM	YDLY			RESERVED				30h	
0x94				MISC1	HPLC	EVCNT	PALC	SDET	TBC_EN	BYPASS	SYOUT	RESERVED	14h	
0x95				LOOP	HPM	ACCT		SPM			CBW		A5h	
0x96				MISC2	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0h	
0x97				CLMD	FRM		YNR		CLMD			PSP		05h
0x98				HSLOWCTL	RESERVED	HSBEGIN[2:0]			RESERVED	HSEND[2:0]				00h
0x99				HSBEGIN	HSBEGIN[10:3]								28h	
0x9A				HSEND	HSEND[10:3]								44h	
0x9B				OVSDLY	OVSDLY								44h	
0x9C				OVSEND	HASYNC	OFDLY			VSMODE	OVSEND				20h
0x9D				HBLEN	HBLEN								90h	
0x9E				NOVID	RESERVED	FC27	CHID_MD		NOVID_656	EAVSWAP	VIPCFG	NTSC656	42h	
0x9F				CLK1MD	RESERVED				CLKO_DEL					00h
0xAA				AGCEN	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]	00h	
0xAB				AGCGAIN1	AGCGAIN1[7:0]								F0h	
0xAC				AGCGAIN2	AGCGAIN2[7:0]								F0h	
0xAD				AGCGAIN3	AGCGAIN3[7:0]								F0h	
0xAE				AGCGAIN4	AGCGAIN4[7:0]								F0h	
0xAF				VSHP21	RESERVED	VSHP2			RESERVED	VSHP1				00h
0xB0				VSHP43	RESERVED	VSHP4			RESERVED	VSHP3				00h
0xB1				NOVIDMODE	RESERVED		NOVIDMODE		RESERVED					00h
0xB2				CLMP_FINE1	RESERVED								CL_OFF[8]	00h
0xB3				CLMP_FINE2	CL_OFF[7:0]								00h	

Register Map (Continued)

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE	
CH1	CH2	CH3	CH4											
0xC8				MPP_CTL1	RESERVED	MPP_MODE2			GPP_VAL	MPP_MODE1			7Fh	
0xC9				MPP_CTL2	RESERVED	MPP_MODE4			RESERVED	MPP_MODE3			77h	
0xCA				CHMD	RESERVED						CHMD1		00h	
0xCB				CIF54M	RESERVED	MPP_CH		POLMPP	RESERVED					00h
0xCC				SELCH	RESERVED						SELCH		39h	
0xCD				MAINCH	RESERVED						MAINCH		E4h	
0xCE				ADC_CNT1	PD_BIAS	BIAS_CTRL			V_ADC_PWDN				70h	
0xCF				ADC_CNT2	FLT_EN				DIFF				F0h	
0xD0				ADC_CNT3	GAIN_SEL_4		GAIN_SEL_3		GAIN_SEL_2		GAIN_SEL_1		00h	
0xD1				ADC_CNT4	VADC_CK_POL	DCLAMP_ATTEN			DCLAMP_EN				0Fh	
0xD2				ADC_CNT5	RES_REFERENCE				PRECONDITION				00h	
0xD3				ADC_CNT6	PASSIVE_CLAMP				PASSIVE_VREF				00h	
0xD4				ADC_CNT7	ACLAMP_ATTEN		AN_TEST_SEL		AN_TEST_EN				C0h	
0xD5				CMM_CLMP	CM_CLAMP	TOGGLE_MODE	CM_CLAMP_MODE		CL_MARGIN	CM_ALWAYS_SAMPLE	CM_SAMPLE_TIME	CM_SAMPLE_MODE	00h	
0xD6				SHORT1	PD_SHORT	BAT_TRESH_SEL			RESERVED	GND_THRESH_SEL			80h	
0xD7				SHORT2	BAT_SHORT_OUT *				GND_SHORT_OUT *				-	
0xD8				SHORT_INT1	BSDET_ENA				GSDET_ENA				00h	
0xD9				SHORT_INT2	BSDET_MASK				GSDET_MASK				00h	
0xDA				SHORT_INT3	BSDET_CLEAR				GSDET_CLEAR				00h	
0xF9				VMISC	LIM16	RESERVED	YBCBR422	HA656MD	VBI_FRAM	CNTL656	VSCL_SYNC	HA_EN	11h	
0xFA				CLKOCTL	RESERVED	OE	RESERVED	CLKO_OEB	RESERVED		CLKO_MD		00h	
0xFB				AVDET_MODE	RESERVED	CLKO_POL	IRQENA	IRQPOL	SDET_MODE		VDET_MODE		0Fh	
0xFC				AVDET_ENA	RESERVED				VDET_ENA				00h	
0xFD				AVDET_STATE*	RESERVED				VDET_STATE *				00h	
0xFE				TEST	DEV_ID[6:5]*		RESERVED			TEST			00h	
0xFF				DEV_ID*	DEV_ID[4:0]*							REV_ID *	F8h	

NOTE: *Read only registers

Register Descriptions

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X00(CH1)/0X10(CH2)/0X20(CH3)/0X30(CH4) – VIDEO STATUS REGISTER				
7	VDLOSS	R	1 = Video is not present (sync is not detected in the number of consecutive line periods specified by the MISSCNT register) 0 = Video is detected	-
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source 0 = Horizontal sync PLL is not locked	-
5	SLOCK	R	1 = Subcarrier PLL is locked to the incoming video source 0 = Subcarrier PLL is not locked	-
4	FIELD	R	0 = Odd field is being decoded 1 = Even field is being decoded	-
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source 0 = Vertical logic is not locked	-
2	Reserved	R	Reserved	-
1	MONO	R	1 = No color burst signal detected 0 = Color burst signal detected	-
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	-
0X01(CH1)/0X11(CH2)/0X21(CH3)/0X31(CH4) – BRIGHTNESS CONTROL REGISTER				
7-0	BRIGHT	R/W	Controls the brightness and has a value of –128 to 127 in 2's complement form. A positive value increases brightness. A value of 0 has no effect on the data.	00h
0X02(CH1)/0X12(CH2)/0X22(CH3)/0X32(CH4) – CONTRAST CONTROL REGISTER				
7-0	CNTRST	R/W	Controls the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	64h
0X03(CH1)/0X13(CH2)/0X23(CH3)/0X33(CH4) – SHARPNESS CONTROL REGISTER				
7	SCURVE	R/W	Controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = Low 1 = Center	0h
6	VSF	R/W	Internal use only	0h
5-4	CTI	R/W	CTI level selection. 0 = None 3 = Highest	1h
3-0	SHARP	R/W	Controls the amount of sharpness enhancement on the luminance signals. There are 16 levels of control. A value of '0' has no effect on the output image. Values 1 through 15 provide sharpness enhancement with 'F' being the strongest.	1h
0X04(CH1)/0X14(CH2)/0X24(CH3)/0X34(CH4) – CHROMA (U) GAIN REGISTER				
7-0	SAT_U	R/W	Controls the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h
0X05(CH1)/0X15(CH2)/0X25(CH3)/0X35(CH4) – CHROMA (V) GAIN REGISTER				
7-0	SAT_V	R/W	Controls the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has a gain of 100%.	80h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X06(CH1)/0X16(CH2)/0X26(CH3)/0X36(CH4) – HUE CONTROL REGISTER				
7-0	HUE	R/W	Controls the color hue as a 2's complement number. Valid values are from +90° (7Fh) to -90° (80h) with increments of 2.8°. The two LSBs have no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL systems.	00h
0X07(CH1)/0X17(CH2)/0X27(CH3)/0X37(CH4) – CROPPING REGISTER, HIGH				
7-6	VDELAY_HI	R/W	Bit 9 to 8 of the 10-bit Vertical Delay register.	0h
5-4	VACTIVE_HI	R/W	Bit 9 to 8 of the 10-bit VACTIVE register. Refer to the "0X09(CH1)/0X19(CH2)/0X29(CH3)/0X39(CH4) – Vertical Active Register, Low" description for its shadow register.	1h
3-2	HDELAY_HI	R/W	Bit 9 to 8 of the 10-bit Horizontal Delay register.	0h
1-0	HACTIVE_HI	R/W	Bit 9 to 8 of the 10-bit HACTIVE register.	2h
0X08(CH1)/0X18(CH2)/0X28(CH3)/0X38(CH4) – VERTICAL DELAY REGISTER, LOW				
7-0	VDELAY_LO	R/W	Bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. This register defines the number of lines between the leading edge of VSYNC and the start of the active video.	12h
0X09(CH1)/0X19(CH2)/0X29(CH3)/0X39(CH4) – VERTICAL ACTIVE REGISTER, LOW				
7-0	VACTIVE_LO	R/W	Bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. This register defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20h
0X0A(CH1)/0X1A(CH2)/0X2A(CH3)/0X3A(CH4) – HORIZONTAL DELAY REGISTER, LOW				
7-0	HDELAY_LO	R/W	Bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. This register defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources, respectively. These registers can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0Ah
0X0B(CH1)/0X1B(CH2)/0X2B(CH3)/0X3B(CH4) – HORIZONTAL ACTIVE REGISTER, LOW				
7-0	HACTIVE_LO	R/W	Bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. This register defines the number of active pixels per line output.	D0h
0X0C(CH1)/0X1C(CH2)/0X2C(CH3)/0X3C(CH4) – MACROVISION DETECTION				
7	SF	R	Internal use	-
6	PF	R	Internal use	-
5	FF	R	Internal use	-
4	KF	R	Internal use	-
3	CSBAD	R	1 = Macrovision color stripe detection may be unreliable	-
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected	-
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected 0 = Not detected	-
0	CTYPE	R	This bit is valid only when color stripe protection is detected, that is, CSTRIPE = 1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	-

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X0D(CH1)/0X1D(CH2)/0X2D(CH3)/0X3D(CH4) – CHIP STATUS II				
7	VCR	R	VCR signal indicator.	-
6	WKAIR	R	Weak signal indicator 2.	-
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	-
4	VSTD	R	1 = Standard signal 0 = Nonstandard signal	-
3	NINTL	R	1 = Noninterlaced signal 0 = Interlaced signal	-
2-0	Reserved	R	Reserved.	-
0X0E(CH1)/0X1E(CH2)/0X2E(CH3)/0X3E(CH4) – STANDARD SELECTION				
7	DETSTUS	R	0 = Idle 1 = Detection in progress	-
6-4	STDNOW	R	Current standard invoked. 0 = NTSC(M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	-
3	ATREG	R/W	1 = Disable the shadow registers 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0h
2-0	STD	R/W	Standard selection. 0 = NTSC(M) 1 = PAL (B, D, G, H, I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7h
0X0F(CH1)/0X1F(CH2)/0X2F(CH3)/0X3F(CH4) – STANDARD RECOGNITION				
7	ATSTART	R/W	Write a 1 to this bit to manually initiate the auto format detection process. This bit is self-resetting.	0
6	PAL6_EN	R/W	1 = Enable recognition of PAL60 0 = Disable recognition	1h
5	PALN_EN	R/W	1 = Enable recognition of PAL (CN) 0 = Disable recognition	1h
4	PALM_EN	R/W	1 = Enable recognition of PAL (M) 0 = Disable recognition	1h
3	NT44_EN	R/W	1 = Enable recognition of NTSC 4.43 0 = Disable recognition	1h
2	SEC_EN	R/W	1 = Enable recognition of SECAM 0 = Disable recognition	1h
1	PALB_EN	R/W	1 = Enable recognition of PAL (B, D, G, H, I) 0 = Disable recognition	1h
0	NTSC_EN	R/W	1 = Enable recognition of NTSC (M) 0 = Disable recognition	1h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XE4(CH1)/0XE7(CH2)/0XEA(CH3)/0XED(CH4)				
7-0	Reserved	R/W	Reserved	00h
0XE5(CH1)/0XE8(CH2)/0XEB(CH3)/0XEE(CH4)				
7-0	Reserved	R/W	Reserved	11h
0XE6(CH1)/0XE9(CH2)/0XEC(CH3)/0XEF(CH4) – HORIZONTAL SCALING REGISTER, LOW				
7-0	Reserved	R/W	Reserved	00h
0XA4(CH1)/0XA5(CH2)/0XA6(CH3)/0XA7(CH4) – ID DETECTION CONTROL				
7-6	IDX	R/W	Indicates which of the four lower 6-bit registers is currently being controlled. The write sequence is a two step process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write actually writes into the register.	0h
5-0	NSEN/SSEN/PSEN/WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A/ 20/ 1C/ 2Ah
0XC4(CH1)/0XC5(CH2)/0XC6(CH3)/0XC7(CH4) – H MONITOR				
7-0	HREF	R	Horizontal line frequency indicator (for test purposes only).	-
0X80 – SOFTWARE RESET CONTROL REGISTER				
7	Reserved	R	Reserved	-
6	ENCRST	W	A “1” written to this bit resets the video encoder logic to its default state but all register content remains unchanged. This bit is self-resetting.	0h
5	IRQRST	W	A “1” written to this bit resets the IRQ logic to its default state but all register content remains unchanged. This bit is self-resetting.	0h
4	VOUTrST	W	A “1” written to this bit resets the Video data mux output logic to its default state but all register content remains unchanged. This bit is self-resetting.	0h
3	VDEC4RST	W	A “1” written to this bit resets the Video4 Decoder portion to its default state but all register content remains unchanged. This bit is self-resetting.	0h
2	VDEC3RST	W	A “1” written to this bit resets the Video3 Decoder portion to its default state but all register content remains unchanged. This bit is self-resetting.	0h
1	VDEC2RST	W	A “1” written to this bit resets the Video2 Decoder portion to its default state but all register content remains unchanged. This bit is self-resetting.	0h
0	VDEC1RST	W	A “1” written to this bit resets the Video1 Decoder portion to its default state but all register content remains unchanged. This bit is self-resetting.	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X81 – ANALOG CONTROL REGISTER				
7	Reserved	R	Reserved	-
6	IREF	R/W	0 = Internal current reference 1 1 = Increase internal current reference 30%	0h
5	VREF	R/W	0 = Internal voltage reference 1 = Internal voltage reference shut down	0h
4	Reserved	R/W	0 = Normal operation (must be 0) 1 = AIGAINTEST	0h
3	CLKPDN	R/W	0 = Normal clock operation 1 = All 4Ch Video Decoder System clocks are in power-down mode, but the MPU INTERFACE module and output clocks (CLKP and CLKN) are still active	0h
2	Reserved	R/W	0 = Normal operation (must be 0) 1 = AINSWTEST	0h
1	YFLEN	R/W	Analog Video CH1/CH2/CH3/CH4 antialias filter control. 1 = Enable 0 = Disable	1h
0	YSV	R/W	Analog Video CH1/CH2/CH3/CH4 reduced power mode. 1 = Enable 0 = Disable	0h
0X82 – ANALOG CONTROL REGISTER 2				
7	CTEST	R/W	Clamping control for debugging use (test purposes only).	0h
6	YCLEN	R/W	1 = Digital clamp disabled (test purposes only) 0 = Enable clamp pulse generation	0h
5	CKIPOL	R/W	27MHz clock output signal rise/fall timing. 0: Change by 54MHz clock output falling edge 1: Change by 54MHz clock output rising edge	0h
4	Reserved	R	Reserved	-
3	GTEST	R/W	1 = Test (test purposes only) 0 = Normal operation	0h
2	VLPF	R/W	Clamping filter control.	0h
1	CKLY	R/W	Clamping current control. 1 = No 2x clamping	0h
0	Reserved	R/W	Reserved	-
0X83 – CONTROL REGISTER I				
7	PBW	R/W	1 = Wide chroma BPF BW 0 = Normal chroma BPF BW	1h
6	DEM	R/W	Reserved	-
5	PALSW	R/W	1 = PAL switch sensitivity is low 0 = PAL switch sensitivity is normal	0h
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level 0 = The black level is the same as the blank level	0h
3	COMB	R/W	1 = Adaptive comb filter for NTSC and PAL (recommended). Not for SECAM. 0 = Notch filter, for SECAM	1h
2	HCOMP	R/W	1 = Operation mode 1 (recommended) 0 = Mode 0	1h
1	YCOMB	R/W	1 = Bypass comb filter when no burst is present 0 = No bypass	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0	PDLY	R/W	PAL delay line. 0 = Enabled 1 = Disabled	0h
0X84 – COLOR KILLER HYSTERESIS CONTROL REGISTER				
7	GMEN	R/W	Reserved	-
6-5	CKHY	R/W	Color killer hysteresis. 0 = Fastest 1 = Fast 2 = Medium 3 = Slow	0h
4-0	HSDLY	RW	Reserved for test.	00h
0X85 – VERTICAL SHARPNESS				
7-4	SHCOR	R/W	Provides the coring function for the sharpness control.	8h
3	VIN4	R/W	Ch4 Video ADC input signal select. 0: VIN4A 1: VIN4B	0h
2	VIN3	R/W	Ch3 Video ADC input signal select. 0: VIN3A 1: VIN3B	0h
1	VIN2	R/W	Ch2 Video ADC input signal select. 0: VIN2A 1: VIN2B	0h
0	VIN1	R/W	Ch1 Video ADC input signal select. 0: VIN1A 1: VIN1B	0h
0X86 – CORING CONTROL REGISTER				
7-6	CTCOR	R/W	Controls the coring for CTI.	1h
5-4	CCOR	R/W	Controls the low level coring function for the Cb/Cr output.	0h
3-2	VCOR	R/W	Controls the coring function of vertical peaking.	1h
1-0	CIF	R/W	Controls the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0h
0X87 – CLAMPING POSITION				
7-4	CLPEND	R/W	Sets the end time of the clamping pulse. Its value should be larger than the value of CLPST.	5h
3-0	CLPST	R/W	Sets the start time of the clamping. It is referenced to the PCLAMP position.	0h
0X88 – INDIVIDUAL AGC GAIN				
7-4	NMGAIN	R/W	Controls the normal AGC loop maximum correction value.	2h
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1h
0	Reserved	R	Reserved	-
0X8A – WHITE PEAK THRESHOLD				
7-0	PEAKWT	R/W	Controls the white peak detection threshold. Set FF to disable this function.	D8h
0X8B – CLAMP LEVEL				
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL 1 = Clamping level preset at 60d	1h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
6-0	CLMPL	R/W	Determines the clamping level of the video input.	3Ch
0X8C – SYNC AMPLITUDE				
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT 1 = Reference sync amplitude is preset to 38h	1h
6-0	SYNCT	R/W	Determines the standard sync pulse amplitude for AGC reference.	38h
0X8D – SYNC MISS COUNT REGISTER				
7-4	MISSCNT	R/W	Sets the threshold for horizontal sync miss count threshold.	4h
3-0	HSWIN	R/W	Determines the VCR mode detection threshold.	4h
0X8E – CLAMP POSITION REGISTER				
7-0	PCLAMP	R/W	Sets the clamping position from the PLL sync edge.	38h
0X8F – VERTICAL CONTROL I				
7-6	VLCKI	R/W	Vertical lock in time. 0 = Fastest 3 = Slowest	0h
5-4	VLCKO	R/W	Vertical lock out time. 0 = Fastest 3 = Slowest	0h
3	VMODE	R/W	Controls the vertical detection window. 1 = Search mode 0 = Vertical count down mode	0h
2	DETV	R/W	1 = Recommended for special applications only 0 = Normal VSYNC logic	0h
1	AFLD	R/W	Auto field generation control. 0 = Off 1 = On	0h
0	VINT	R/W	Vertical integration time control. 1 = Short 0 = Normal	0h
0X90 – VERTICAL CONTROL II				
7-5	BSHT	R/W	Burst PLL center frequency control.	0h
5-0	VSHT	R/W	VSYNC output delay control half line length increments.	00h
0X91 – COLOR KILLER LEVEL CONTROL				
7-6	CKILMAX	R/W	Controls the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1h
5-0	CKILMIN	R/W	Controls the color killer threshold. Larger values give lower killer levels.	38h
0X92 – COMB FILTER CONTROL				
7	COMBMD	R/W	0 = Adaptive mode 1 = Fixed comb	0h
6-4	HTL	R/W	Adaptive Comb filter threshold control 1.	4h
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4h
0X93 – LUMA DELAY AND H FILTER CONTROL				

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKLM	R/W	Color Killer mode. 0 = Normal 1 = Fast (for special applications)	0h
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides -4 to +3 unit delay control.	3h
3-0	Reserved	RW		0h
0X94 – MISCELLANEOUS CONTROL I				
7	HPLC	R/W	Reserved for internal use.	0h
6	EVCNT	R/W	1 = Even field counter in special mode 0 = Normal operation	0h
5	PALC	R/W	Reserved for future use.	0h
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1h
3	TBC_EN	R/W	1 = Internal TBC enable. Total pixels per line on the Video active line is always 858x2 for NTSC/PAL-M (60Hz) and 864x2 for PAL/SECAM (50Hz) 0 = TBC off	0h
2	BYPASS	R/W	Controls the standard detection. Set to 1 in normal use.	1h
1	SYOUT	R/W	1 = HSYNC output is disabled when video loss is detected 0 = HSYNC output is always enabled	0h
0	Reserved	R	Reserved	0h
0X95 – LOOP CONTROL REGISTER				
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal	2h
5-4	ACCT	R/W	ACC time constant. 0 = No ACC 1 = Slow 2 = Medium 3 = Fast	2h
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1h
1-0	CBW	R/W	Chroma low pass filter bandwidth control. See filter curves.	1h
0X96 – MISCELLANEOUS CONTROL II				
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode 0 = Disabled	1h
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode 0 = Disabled	1h
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode 0 = Disabled	1h
4	CBAL	R/W	0 = Normal output 1 = Special output mode	0h
3	FCS	R/W	1 = Force decoder output value determined by CCS 0 = Disabled	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
2	LCS	R/W	1 = Enable predetermined output value indicated by CCS when video loss is detected 0 = Disabled	0h
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two display colors can be selected. 1 = Blue 0 = Black	0h
0	BST	R/W	1 = Enable blue stretch 0 = Disabled	0h
0X97 – DIGITAL CLAMP MODE				
7-6	FRM	R/W	Free run mode control. 0 = Auto 2 = Default to 60Hz 3 = Default to 50Hz	0h
5-4	YNR	R/W	YHF noise reduction. 0 = None 1 = Smallest 2 = Small 3 = Medium	0h
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1h
1-0	PSP	R/W	Slice level control. 0 = Low 1 = Medium 2 = High	1h
0X98 – HSLOWCTL				
7	Reserved	R/W	Reserved	-
6-4	HSBEGIN[2:0]	R/W	HSYNC Start position Control Bit[2-0].	0h
3	Reserved	R/W	Reserved	-
2-0	HSEND[2:0]	R/W	HSYNC End position Control Bit[2-0].	0h
0X99 – HSBEGIN				
7-0	HSBEGIN[10:3]	R/W	HSYNC Start position Control Bit[10-3].	28h
0X9A – HSEND				
7-0	HSEND[10:3]	R/W	HSYNC End position Control Bit[10-3].	44h
0X9B – OVSDLY				
7-0	OVSDLY	R/W	VSYNC Start position. Control H position on VSYNC start.	44h
0X9C – OVSEND				
7	HASYNC	R/W	1: The length of EAV to SAV is set up and fixed by the HBLN registers 0: The length of SAV to EAV is set up and fixed by the HACTIVE registers	0h
6-4	OFDLY	R/W	FIELD output delay. 0h: 0H line delay FIELD output. (601 mode only) 1h-6h: 1H-6H line delay FIELD output 7h: Reserved	2h
3	VSMODE	R/W	1: VSYNC output is HACTIVE-VSYNC mode 0: VSYNC output is HSYNC-VSYNC mode	0h
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X9D – HBLN				
7-0	HBLN	R/W	Effective when the HASYNC bit is set to 1. These bits set up the length of the EAV to SAV code when the HASYNC bit is 1. Normal value is (Total pixel per line – HACTIVE). NTSC/PAL-M (60Hz): 8Ah (138dec) = 858-720 PAL/SECAM (50Hz): 90h (144dec) = 864-720 If Reg0x0E[3] (ATRIG for CH1) is set to 0, this value changes into 8Ah or 90h at auto video format detection initial time automatically according to CH1 video detection status.	90h
0X9E – NOVID				
7	Reserved	R	Reserved	-
6	FC27	R/W	1: Normal ITU-R656 operation 0: Squared Pixel mode	1h
5-4	CHID_MD	R/W	Select the Channel ID format for Time-multiplexed outputs. 0: No channel ID (default) 1: CHID with the specific ITU-R BT.656 sync code 2: CHID with the specific horizontal blanking code 3: CHID with the specific ITU-R BT.656 sync and horizontal blanking code	0h
3	NOVID_656	R/W	0: Normal ITU-R BT.656 SA/EAV (default) 1: An optional set of ITU-R BT.656 SAV/EAV codes for no-video status	0h
2	EAVSWAP	R/W	1: EAV-SAV code is swapped. 0: EAV-SAV code is not swapped (standard 656 output mode)	0h
1	VIPCFG	R/W	Set up Bit 7 in the fourth byte of the EAV/SAV code. 1: Standard ITU-R656 code format (and VIP task-A code format) 0: Old VIP task-B code format	1h
0	NTSC656	R/W	1: Number of Even Field Video output lines = (number of Odd field Video output line – 1). This bit is required for the ITU-R BT.656 output for the 525 line system standard. 0: Number of Even Field Video output lines is same as the number of Odd field Video output lines.	0h
0X41 – VIDEO ENCODER STANDARD CONTROL				
7	HZ50	R/W	1 = 50Hz field rate 0 = 60Hz field rate	0h
6	INTERLACE	R/W	1 = Interlaced output 0 = Noninterlaced output	1h
5-4	FSCSEL	R/W	FSCSEL frequency selection 00 = NTSC-M 01 = PAL-B 10 = PAL-M 11 = PAL-N	0h
3	COFF	R/W	1 = Turn off chroma output 0 = Turn on chroma output	0h
2	PHALT	R/W	1 = Alternating burst for PAL 0 = NTSC	0h
1	PDRST	R/W	1 = PAL phase reset every eight fields 0 = No phase reset	0h
0	PED	R/W	1 = Pedestal enabled (NTSC-M) 0 = Disabled	0h
0X42 – VIDEO ENCODER TEST GENERATION				
7-6	YBW	R/W	Luminance bandwidth control. 2, 3 = Normal bandwidth 1, 0 = Not available	2h
5-4	CBW	R/W	Chrominance bandwidth control. See filter diagram.	1h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
3	CBGEN	R/W	1 = Enable internal test pattern generation 0 = Disabled	0h
2-0	TCSEL	R/W	Test pattern selection. 0 = 75% color bar 1 = White 2 = Yellow 3 = Cyan 4 = Green 5 = Magenta 6 = Red 7 = Blue	0h
0X43 – VIDEO ENCODER CLOCK AND DELAY CONTROL				
7	CKMST	R/W	1 = Use the internal 27MHz clock as the encoder clock. The ENCLK pin is the clock output, for internal use only 0 = Use the input clock as the encoder clock. The ENCLK pin is the clock input	0h
6	ENCKPOL	R/W	Controls the clock polarity for latching input data.	0h
5	NONSTA	R/W	1 = Nonstandard 656 input (internal use only) 0 = Normal 656 input	0h
4	FRUN	R/W	0 = Encoder timing generation based on input 1 = Internal generated timing for built-in test pattern	0h
3-0	YDEL	R/W	Y delay adjustment relative to Cb/Cr. The center value of 8.8h should be set up normally	8h
0X44 – VIDEO ENCODER OUTPUT CONTROL				
7	CVBS_SEL	R/W	DAC output control 1 = Luma output 0 = CVBS output	0h
6	Reserved	R/W	Reserved	-
5-0	ENCTMODE	R/W	Encoder test mode. Internal use only	0h
0X45 – VIDEO ENCODER SCH				
6-0	SCH	R/W	Subcarrier phase control. Internal use only	38h
0X46 – VIDEO ENCODER YGAIN				
7-0	ENCYGAIN	R/W	Luminance amplitude gain control. The 0dB gain is 0x80	80h
0X47 – VIDEO ENCODER CGAIN				
7-0	ENCCGAIN	R/W	Chrominance amplitude gain control. The 0dB gain is 0x80	80h
0X48 – VIDEO ENCODER SGAIN				
7-0	ENCSGAIN	R/W	Sync pulse amplitude gain control. The 0dB gain is 0x80	80h
0X49 – VIDEO ENCODER BGAIN				
7-0	ENCBGAIN	R/W	Burst amplitude gain control. The 0dB gain is 0x80	80h
0X4A – VIDEO DAC CONTROL				
7-4	Reserved	R/W	Reserved	-
3-0	VDA_IREFY	R/W	Video DAC IREF control	Fh

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X4B – VIDEO DAC CONTROL				
7	ENCVDOUT	R/W	Test purposes only	0
6	TEST_DAC	R/W	Test purposes only	0
5	Reserved	R/W	Reserved	-
4	VDA_PD	R/W	1: Video DAC power-down mode 0: Normal mode	1
3	VDAC_CKPOL	R/W	1: Analog video DAC input clock polarity inverse 0: Not inverse.	0
2	ENC_LOOP	R/W	Video Decoder to Video Encoder loop test mode. 1: Video Decoder output directly connects to the Video Encoder input for test purposes only. LOOP_CH register select Video CH number to be connected to Video Encoder in this mode. This function is for internal test use only 0: Normal Video Decoder and Video Encoder operation. Video Decoder and Video Encoder are working independently	0
1-0	LOOP_CH	R/W	Selects the Video CH number to be connected to the Video Encoder directly when the ENC_LOOP register is set to 1. 0: CH1 Video Data 1: CH2 Video Data 2: CH3 Video Data 3: CH4 Video Data	0h
0X4C – VIDEO ENCODER VDELAY				
7-5	Reserved	R	Reserved	-
4-0	EVDELAY	R/W	Video Encoder output Vertical position control.	0h
0X4D – VIDEO ENCODER HDELAY				
7-5	Reserved	R	Reserved	-
4-0	EHDELAY	R/W	Video Encoder output Horizontal position control.	0h
0X4F – DAC INPUT SELECTION (OPTIONAL)				
7-6	Reserved	R	Reserved	-
5	ADDABP	R/W	1: AD to DA direct bypass mode enable 0: Disable	0
4-2	Reserved	R/W	Reserved	-
1-0	BPCHSEL	R/W	AD to DA direct bypass mode channel selection. 0: CH-1 1: CH-2 2: CH-3 3: CH-4	0h
0X9F – CLOCK OUTPUT DELAY CONTROL REGISTER				
7-4	Reserved	R/W		0h
3-0	CLKO_DEL	R/W	Controls the clock delay of the CLKO pin. 0h/1h/3h/7h/Fh values are effective. 1h: About 2ns more delay 3h: About 4ns more delay 7h: About 6ns more delay Fh: About 7ns more delay	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
Video AGC Control				
0XAA – VIDEO AGC CONTROL				
7	AGCEN4	R/W	Selects Video AGC loop function on VIN4. 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN4	0
6	AGCEN3	R/W	Selects Video AGC loop function on VIN3 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN3	0
5	AGCEN2	R/W	Selects Video AGC loop function on VIN2 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN2	0
4	AGCEN1	R/W	Selects Video AGC loop function on VIN1 0: AGC loop function enabled (recommended for most application cases). 1: AGC loop function disabled. Gain is set by AGCGAIN1	0
3	AGCGAIN4[8]	R/W	AGCGAIN4 MSB	0
2	AGCGAIN3[8]	R/W	AGCGAIN3 MSB	0
1	AGCGAIN2[8]	R/W	AGCGAIN2 MSB	0
0	AGCGAIN1[8]	R/W	AGCGAIN1 MSB	0
0XAB – VIDEO AGC CONTROL				
7-0	AGCGAIN1[7:0]	R/W	Controls the AGC Gain when the AGC loop is disabled. AGCGAIN1 Bit 7-0.	F0h
0XAC – VIDEO AGC CONTROL				
7-0	AGCGAIN2[7:0]	R/W	Controls the AGC Gain when the AGC loop is disabled. AGCGAIN2 Bit 7-0.	F0h
0XAD – VIDEO AGC CONTROL				
7-0	AGCGAIN3[7:0]	R/W	Controls the AGC Gain when the AGC loop is disabled. AGCGAIN3 Bit 7-0.	F0h
0XAE – VIDEO AGC CONTROL				
7-0	AGCGAIN4[7:0]	R/W	Controls the AGC Gain when the AGC loop is disabled. AGC GAIN4 Bit 7-0.	F0h
0XAF – VERTICAL PEAKING LEVEL CONTROL				
7	Reserved	R	Reserved	-
6-4	VSHP2	R/W	Selects the CH2 Video Vertical peaking level (Note 13). 0: None 7: Highest	0h
3	Reserved	R	Reserved	-
2-0	VSHP1	R/W	Selects the CH1 Video Vertical peaking level (Note 13). 0: None 7: Highest	0h
0XB0 – VERTICAL PEAKING LEVEL CONTROL				
7	Reserved	R	Reserved	-
6-4	VSHP4	R/W	Selects the CH4 Video Vertical peaking level (Note 13). 0: None 7: Highest	0h
3	Reserved	R	Reserved	-

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
2-0	VSHP3	R/W	Selects the CH3 Video Vertical peaking level (Note 13). 0: None 7: Highest	0h
0XB1 – NOVIDMODE				
7-6	Reserved	R	Reserved	-
5-4	NOVIDMODE	R/W	Selects the NOVID_656 output mode status. When NOVID_656 is set to 1, the NOVID_656 code is output when the following status is active in the Video Decoding logic. 0: Video lost (vdlloss) 1: No Video (novideo) 2: Video lost or No video (vdlloss or novideo) 3: NOVID_656 code is not being output at anytime	0h
3-0	Reserved	R	Reserved	-
0XB2 – CLAMP PULSE FINE ADJUSTMENT 1				
7-1	Reserved	R/W	Reserved	-
0	CL_OFF[8]	R/W	Clamp pulse position fine adjustment MSB. This value is 2's complement and accepts negative values to move the pulse location forward (to the front porch).	0h
0XB3 – CLAMP PULSE FINE ADJUSTMENT 2				
7-0	CL_OFF[7:0]	R/W	Clamp pulse position fine adjustment LSB (8 bits). This value is 2's complement and accepts negative values to move the pulse location forward (to the front porch).	00h
MPP Pin Output Mode Control				
0XC8 – MPP PIN OUTPUT MODE CONTROL 1				
7	Reserved	R/W	Reserved	-
6-4	MPP_MODE2	R/W	Selects the Channel 2 decoder status for the MPP pin. The following values describe the status when the POLMPP register is set to 0. If the POLMPP register is set to 1, the following values have an inversed status. 0: Horizontal sync output. Low is H-sync active 1: Vertical sync output. Low is V-sync active 2: Field flag output. Low is field1 (Odd), High is field2 (Even) 3: Horizontal active signal output. High is H-active 4: Vertical active and horizontal active signal output. High is VH-active 5: No video flag. High is No-video, Low is Video 6: VDLOSS 7: GPP_VAL. Same as the GPP_VAL register value	7h
3	GPP_VAL	R/W	Selects the general purpose value through the MPP pin. 0: "0" value 1: "1" value	1h
2-0	MPP_MODE1	R/W	Selects the Channel 1 decoder status for the MPP pin. The following values describe the status when the POLMPP register is set to 0. If the POLMPP register is set to 1, the following values have an inversed status. 0: Horizontal sync output. Low is H-sync active 1: Vertical sync output. Low is V-sync active 2: Field flag output. Low is field1 (Odd), High is field2 (Even) 3: Horizontal active signal output. High is H-active 4: Vertical active and horizontal active signal output. High is VH-active 5: No video flag. High is No-video, Low is Video 6: VDLOSS 7: GPP_VAL. Same as the GPP_VAL register value	7h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XC9 – MPP PIN OUTPUT MODE CONTROL 2				
7	Reserved	R/W	Reserved	0h
6-4	MPP_MODE4	R/W	Selects the Channel 4 decoder status for the MPP pin. The following values describe the status when the POLMPP register is set to 0. If the POLMPP register is set to 1, the following values have an inversed status. 0: Horizontal sync output. Low is H-sync active 1: Vertical sync output. Low is V-sync active 2: Field flag output. Low is field1 (Odd), High is field2 (Even) 3: Horizontal active signal output. High is H-active 4: Vertical active and horizontal active signal output. High is VH-active 5: No video flag. High is No-video, Low is Video 6: VDLOSS 7: GPP_VAL. Same as the GPP_VAL register value	7h
3	Reserved	R/W	Reserved	0h
2-0	MPP_MODE3	R/W	Selects the Channel 3 decoder status for the MPP pin. The following values describe the status when the POLMPP register is set to 0. If each POLMPP register is set to 1, the following values have an inversed status. 0: Horizontal sync output. Low is H-sync active 1: Vertical sync output. Low is V-sync active 2: Field flag output. Low is field1 (Odd), High is field2 (Even) 3: Horizontal active signal output. High is H-active 4: Vertical active and horizontal active signal output. High is VH-active 5: No video flag. High is no video, Low is video 6: VDLOSS 7: GPP_VAL. Same as the GPP_VAL register value	7h
0XCA – VIDEO CHANNEL OUTPUT CONTROL				
7-2	Reserved	R/W	Reserved	0h
1-0	CHMD1	R/W	Selects the video bus output mode on the 8-bit VD[7:0] pin. 0: Single channel ITU-R BT.656 format output 1: Two channel ITU-R BT.656 Time-multiplexed format output 2: Four channel ITU-R BT.656 Time-multiplexed format output	0h
0XCB – MPP PIN OUTPUT MODE CONTROL 3				
7	Reserved	R/W	Reserved	-
6-5	MPP_CH	R/W	Selects the decoder channel for the MPP pin decoder status output. 0: CH1 1: CH2 2: CH3 3: CH4	0h
4	POLMPP	R/W	Selects the MPP pin output polarity. 0: Normal 1: Inverse polarity	0h
3-0	Reserved	R/W	Reserved	-
0XCC – 2ND CHANNEL SELECTION				
7-2	Reserved	R/W	Reserved	-
1-0	SELCH	R/W	Selects the second video output channel for the Two Channel ITU-R BT.656 Time-multiplexed Format on the VD pin. 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	1h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XCD – 1ST CHANNEL SELECTION				
7-2	Reserved	R/W	Reserved	-
1-0	MAINCH	R/W	Selects the first video output channel for the Two Channel ITU-R BT.656 Time-multiplexed Format on the VD pin. 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output	0h
0XCE – VIDEO ADC CONTROL 1				
7	PD_BIAS	R/W	Band-gap power-down control shared by all four channels.	0h
6-4	BIAS_CTRL	R/W	Shared ADC bias control for all four channels. Always set to 3h.	7h
3-0	V_ADC_PWDN	R/W	Power down the video ADC. V_ADC_PWDN[3:0] stands for CH4 to CH1. 0: Normal operation 1: Power-down	0h
0XCF – VIDEO ADC CONTROL 2				
7-4	FLT_EN	R/W	Antialiasing filter enable for each channel.	Fh
3-0	DIFF	R/W	Differential mode enable on AFE for each channel.	0h
0XD0 – VIDEO ADC CONTROL 3				
7-6	GAIN_SEL_4	R/W	Preamplifier gain control for Channel 4. 0: 1x 1: 2x 2: 4x 3: 4x	0h
5-4	GAIN_SEL_3	R/W	Preamplifier gain control for Channel 3.	0h
3-2	GAIN_SEL_2	R/W	Preamplifier gain control for Channel 2.	0h
1-0	GAIN_SEL_1	R/W	Preamplifier gain control for Channel 1.	0h
0XD1 – VIDEO ADC CONTROL 4				
7	VADC_CK_POL	R/W	Video ADC clock polarity.	0h
6-4	DCLAMP_ATTEN	R/W	Attenuates digital clamp current. Register shared by all four channels. 1x current is: 0: 15μA 1: 7.5μA 2: 5μA 3: 3.75μA 4: 3μA 5: 2.5μA 6: 2.1μA 7: 1.9μA	0h
3-0	DCLAMP_EN	R/W	1: Enables taking the output clamp pulse of the digital clamp for each channel.	Fh
0XD2 – VIDEO ADC CONTROL 5				
7-4	RES_REFERENCE	R/W	1: Uses an alternate resistor divider in the analog common-mode/DC restore block.	0h
3-0	PRECONDITION	R/W	1: Enables the input common-mode preconditioning circuit.	0h
0XD3 – VIDEO ADC CONTROL 6				
7-4	PASSIVE_CLAMP	R/W	1: Uses resistors for differential common-mode restore. 0: Uses OTA common-mode restore.	0h
3-0	PASSIVE_VREF	R/W	1: Uses unbuffered ADC V _{REF} .	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0XD4 – VIDEO ADC CONTROL 7				
7-6	ACLAMP_ATTEN	R/W	Attenuates the analog clamp current. These bits are shared by all four channels. 0: 5 μ A 1: 6.7 μ A 2: 10 μ A 3: 20 μ A	3h
5-4	AN_TEST_SEL	R/W	Shared selection for ADC internal test multiplexers. 0: PGA/AAF (pos) 1: REFP 2: COM 3: REFM	0h
3-0	AN_TEST_EN	R/W	1: Enables test multiplexers. See separate table for output pins.	0h
0XD5 – COMMON MODE CLAMP CONTROL 1				
7	CM_CLAMP	R/W	When in clamp test mode (0xFE[2:0]: TEST = 5), this register value overrides the internally generated common-mode clamp pulse.	0h
6	TOGGLE_MODE	R/W	1: Enables toggle-mode, which eliminates systematic offsets between two output phases of the common-mode restore amplifier by swapping them from line to line.	0h
5-4	CM_CLAMP_MODE	R/W	Selects between four modes of operation for the common-mode restore. 0: Clamp counter 1: Blanking period 2: Burst period 3: Back-porch counter	0h
3	CL_MARGIN	R/W	Adjusts timing spacing between two non-overlapping clocks that operate in the toggle-mode. 0: Three clock periods at 27MHz 1: Six clock periods at 27MHz	0h
2	CM_ALWAYS_SAMPLE	R/W		0h
1	CM_SAMP_TIME	R/W		0h
0	CM_SAMP_MODE	R/W		0h
0XD6 – SHORT DIAGNOSIS 1				
7	PD_SHORT	R/W	1: Power-down short diagnosis	1h
6-4	BAT_THRESH_SEL	R/W	Short-to-battery detection threshold selection 0 = AVDAD*(20/152) 1 = AVDAD*(26/152) 2 = AVDAD*(32/152) 3 = AVDAD*(38/152) 4 = AVDAD*(44/152) 5 = AVDAD*(50/152) 6 = AVDAD*(56/152) 7 = AVDAD*(62/152)	0h
3	Reserved	R/W	Reserved	-
2-0	GND_THRESH_SEL	R/W	Short-to-ground detection threshold selection. 0 = AVDAD*(1/152) 1 = AVDAD*(2/152) 2 = AVDAD*(3/152) 3 = AVDAD*(4/152) 4 = AVDAD*(5/152) 5 = AVDAD*(6/152) 6 = AVDAD*(7/152) 7 = AVDAD*(8/152)	0h
0XD7 – SHORT DIAGNOSIS 2				
7-4	BAT_SHORT_OUT	R	Level triggered battery short detection result. These statuses can be reset by writing 0xDA.	-

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
3-0	GND_SHORT_OUT	R	Level triggered ground short detection result. These statuses can be reset by writing 0xDA.	-
0XD8 – SHORT DIAGNOSIS INTERRUPT 1				
7-4	BSDET_ENA	R/W	Battery short detection enable for Channel 4 ~ 1. 1: Enable	0h
3-0	GSDET_ENA	R/W	Ground short detection enable for Channel 4 ~ 1. 1: Enable	0h
0XD9 – SHORT DIAGNOSIS INTERRUPT 2				
7-4	BSDET_MASK	R/W	Battery short detection mask for Channel 4 ~ 1. 0: Masked for IRQ output.	0h
3-0	GSDET_MASK	R/W	Ground short detection mask for Channel 4 ~ 1. 0: Masked for IRQ output.	0h
0XDA – SHORT DIAGNOSIS INTERRUPT 3				
7-4	BSDET_CLEAR	R/W	Battery short detection status reset for Channel 4 ~ 1. Writing “1” resets the corresponding status bit. These bits return to “0” automatically.	0h
3-0	GSDET_CLEAR	R/W	Ground short detection status reset for Channel 4 ~ 1. Writing “1” resets the corresponding status bit. These bits return to “0” automatically.	0h
0XF9 – VIDEO MISCELLANEOUS FUNCTION CONTROL				
7	LIM16	R/W	0: Output ranges are limited to 2~254 1: Output ranges are limited to 16~235 for Y and 16~239 for CbCr	0h
6	Reserved	R/W	Reserved	-
5	YCBCR422	R/W	Control YCbCr 4:2:2 output mode 0: Normal 4:2:2 output mode 1: Averaging 4:2:2 output mode	0h
4	HA656MD	R/W	Controls the HACTIVE signal output in H-Down Scaling output mode. 0: HACTIVE signal is always the HACTIVE register's length. 1: HACTIVE signal is the same as the DVALID signal in H-Down Scaled video output.	1h
3	VBI_FRAM	R/W	Test purposes only.	0h
2	CNTL656	R/W	Select invalid data value. 0: 0x80 and 0x10 code are output as invalid data during the active video line 1: 0x00 code is output as invalid data during the active video line	0h
1	VSCL_SYNC	R/W	Enables the optional ITU-R.656 sync code format. 0: Skip ITU-R BT.656 sync code for non-valid vertical lines 1: Standard ITU-R BT.656 sync code on any vertical line	0h
0	HA_EN	R/W	Controls the HACTIVE output during the vertical blanking period. 0: HACTIVE output is disabled during vertical blanking period 1: HACTIVE output is enabled during vertical blanking period	1h
Output Enable Control and Clock Output Control				
0XFA – OUTPUT ENABLE CONTROL AND CLOCK OUTPUT CONTROL				
7	Reserved	R/W	Reserved	0h
6	OE	R/W	Controls the tri-state of the output pin. 0: Outputs are tri-stated, except the CLK0 pin 1: Outputs are enabled	0h
5	Reserved	R/W	Reserved	0h
4	CLKO_OEB	R/W	Controls the tri-state of the CLK0 pin. 0: Output is enabled 1: Output is tri-stated	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
3-2	Reserved	R/W	Reserved	0h
1-0	CLKO_MD	R/W	Controls the clock frequency of the CLKO pin. 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: Always 0	0h

Interrupt and Clock Polarity Control

0XFB – INTERRUPT AND CLOCK POLARITY CONTROL

7	Reserved	R/W	Reserved	0h
6	CLKO_POL	R/W	Polarity inverse control on the output CLKO signal just before the CLKO pin. 0: Not inverted. Good for 27MHz/54MHz clock output 1: Polarity inverse	0h
5	IRQENA	R/W	Enables/disables the interrupt request through the IRQ pin. 0: Disable 1: Enable	0h
4	IRQPOL	R/W	Selects the polarity of the interrupt request through the IRQ pin. 0: Falling edge requests the interrupt and keeps its state until cleared 1: Rising edge requests the interrupt and keeps its state until cleared	0h
3-2	SDET_MODE	R/W	Defines the polarity of the trigger for the interrupt request for short detection. 0: No interrupt request by the short detection 1: Make the interrupt request only when the short detection signal rises 2: Make the interrupt request only when the short detection signal falls 3: Make the interrupt request when the short detection signal either rises or falls	3h
1-0	VDET_MODE	R/W	Defines the polarity of the trigger for the interrupt request for video detection. 0: No interrupt request by the video detection 1: Make the interrupt request rising only when the video signal comes in 2: Make the interrupt request falling only when the video signal goes out 3: Make the interrupt request rising and falling when the video comes in and goes out	3h

Enable Video Detection

0XFC – ENABLE VIDEO DETECTION

7-4	Reserved	R/W	Reserved	-
3-0	VDET_ENA	R/W	Enables state register updating and interrupt request of video detection for each input. [0] : Video input VIN1A/B [1] : Video input VIN2A/B [2] : Video input VIN3A/B [3] : Video input VIN4A/B 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request	0h

Status of Video and Short Detection

0XFD – STATUS OF VIDEO DETECTION

7-4	Reserved	R	Reserved	-
3-0	VDET_STATE	R	State of Video detection. These bits are activated according to VDET_MODE. [0]: Video input VIN1A/B [1]: Video input VIN2A/B [2]: Video input VIN3A/B [3]: Video input VIN4A/B 0: Not detected 1: Detected	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
Device ID and Revision ID Flag				
0XFE – DEVICE ID AND REVISION ID FLAG				
7-6	DEV_ID[6:5]	R	Bit 6-5 of Device ID. Together with 0xFF[7:3], they indicate the TW9984 product ID code. DEV_ID = 7'h19	0h
5-3	Reserved	R	Reserved	-
2-0	TEST	R/W	Production test purposes only. This must be 0 in normal mode.	0h
0XFF – DEVICE ID AND REVISION ID FLAG				
7-3	DEV_ID[4:0]	R	Bit 4-0 of the Device ID.	1Fh
2:0	REV_ID	R	Revision number.	0h
0X60 – CLOCK PLL CONTROL				
7	Reserved	R	Reserved	-
6	PLL_PD	R/W	Clock PLL Power-down control. 0: Clock PLL normal mode 1: Clock PLL power-down mode	0h
5	PLL_IREF	R/W	Clock PLL Current bias reference. 0: Reference 0 1: Reference 1	0h
4	SEL_X24	R/W	Clock PLL output mode. 0: 2x XTI input frequency. 54MHz clock input mode 1: 4x XTI input frequency. 27MHz clock input mode	1h
3-2	LP_X4	R/W	PLL loop resistor. 0: 80.5kΩ 1: 35.5kΩ 2: 25.5kΩ 3: 20.5kΩ	1h
1-0	CP_X4	R/W	PLL. charge-pump current. 0: 1μA 1: 5μA 2: 10μA 3: 15μA	1h
0X61 – 108MHZ CLOCK SELECT				
7-5	Reserved	R	Reserved	-
4	DECOSC	R/W	Video Decoder system clock selector. 0: Analog Clock PLL output 108MHz/4 clock is selected 1: System clock generated by XTI input crystal clock If 108MHz clock is connected, system clock is XTI/4 If 54MHz clock is connected, system clock is XTI/2 If 27MHz clock is connected, system clock is XTI	1h
3-2	CKOUTSEL	R/W	Analog Clock PLL output 108MHz selector. 0: 108MHz Clock output - in phase 1: 108MHz Clock output - 90° phase shift 2: 108MHz Clock output - 180° phase shift 3: 108MHz Clock output - 270° phase shift	0h
1-0	XTIMD	R/W	XTI pin input clock process control. If XTIMD = 0/1/2, the Analog Clock PLL Output clock is not used for internal logic processes. 0: 27MHz XTI input clock is used for all clock sources 1: 54MHz XTI input clock is used for all clock sources 2: 108MHz XTI input clock is used for all clock sources 3: Analog Clock PLL 108MHz output is used for all system clock sources	3h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X65 – VIDEO BUS TRI-STATE CONTROL				
7-5	Reserved	R	Reserved	-
4	VD4ORD	R/W	Selects the video channel output order in 4xD1 output mode. 0: CH1->CH2->CH3->CH4->CH1->CH2->CH3->....(increase) 1: CH4->CH3->CH2->CH1->CH4->CH3->CH2->....(decrease)	0h
3-1	Reserved	R/W	Reserved	-
0	VD10EB	R/W	VD[7:0] output tri-state control. 1: Tri-state output VD[7:0] 0: Normal output VD[7:0]	0h
0X59 – AVDS POWER CONTROL (TEST PURPOSE ONLY)				
7	PDBV4B	R/W	0: VIN4B AVDS power-down 1: VIN4B AVDS normal operation	0h
6	PDBV3B	R/W	0: VIN3B AVDS power-down 1: VIN3B AVDS normal operation	0h
5	PDBV2B	R/W	0: VIN2B AVDS power-down 1: VIN2B AVDS normal operation	0h
4	PDBV1B	R/W	0: VIN1B AVDS power-down 1: VIN1B AVDS normal operation	0h
3	PDBV4A	R/W	0: VIN4A AVDS power-down 1: VIN4A AVDS normal operation	0h
2	PDBV3B	R/W	0: VIN3A AVDS power-down 1: VIN3A AVDS normal operation	0h
1	PDBV2B	R/W	0: VIN2A AVDS power-down 1: VIN2A AVDS normal operation	0h
0	PDBV1B	R/W	0: VIN1A AVDS power-down 1: VIN1A AVDS normal operation	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X5A – VSAVE				
7	AVDSMD	R/W	AVDS module PDB input select (test purposes only). 0: PDBV4B input = PDBV4B register PDBV3B input = PDBV3B register PDBV2B input = PDBV2B register PDBV1B input = PDBV1B register PDBV4A input = PDBV4A register PDBV3A input = PDBV3A register PDBV2A input = PDBV2A register PDBV1A input = PDBV1A register 1: PDBV4B input = inversed VIN4 register PDBV3B input = inversed VIN3 register PDBV2B input = inversed VIN2 register PDBV1B input = inversed VIN1 register PDBV4A input = VIN4 register PDBV3A input = VIN3 register PDBV2A input = VIN2 register PDBV1A input = VIN1 register	0h
6	VREF50M_AVDS	R/W	AVDS V_{REF} selection (test purposes only). 0 = 100mV 1 = 50mV	0h
5-4	BIAS_AVDS	R/W	AVDS BIAS selection (test purposes only). 00 = 1.0 μ A 01 = 2.0 μ A 10 = 8.0 μ A 11 = 8.0 μ A	0h
3	PD_BIAS	R/W	Video ADC PD_BIAS	0h
2-0	VSAVE	R/W	Video ADC power save	7h
0X5B– VIDEO OUTPUT PIN DRIVE (Note 14)				
7	Reserved	R/W	VD[7:0] pin optional buffer output enable (not available).	1h
6	VD_OEN	R/W	VD[7:0] pin output enable. 0: Enable output 1: Hi-Z	0h
5	Reserved	R/W	VD[7:0] pin optional buffer drive strength (not available).	0h
4	VD_DS	R/W	VD[7:0] pin drive strength. 0: Low-drive 1: High-drive	1h
3	Reserved	R/W	CLK0 pin optional buffer output enable (not available).	1h
2	CK_OEN	R/W	CLK0 pin output enable. 0: Enable output 1: Hi-Z	0h
1	Reserved	R/W	CLK0 pin optional buffer drive strength (not available).	0h
0	CK_DS	R/W	CLK0 pin drive strength. 0: Low-drive 1: High-drive	1h
0X5C– VIDEO OUTPUT PIN DRIVE (Note 14)				
7	Reserved	R	Reserved	0h
5	BGCTL	R/W	0: Reg96[7:0] control all CH1/CH2/CH3/CH4 video. 1: Reg96[7:0] control only CH1 video Reg5D[7:0] control only CH2 video Reg5E[7:0] control only CH3 video Reg5F[7:0] control only CH4 video	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
4	Reserved	R/W		0h
3	Reserved	R/W	Low speed output pins optional buffer output enable (not available).	1h
2	LS_OEN	R/W	Low speed output pins output enable. 0: Enable output 1: Hi-Z	0h
1	Reserved	R/W	Low speed output pins optional buffer drive strength (not available).	0h
0	LS_DS	R/W	Low speed output pins drive strength. 0: Low-drive 1: High-drive	1h

0X5D – CH2 MISCELLANEOUS CONTROL II ON BGCTL = 1

7	NKILL_2	R/W	1 = Enable noisy signal color killer function in NTSC mode 0 = Disabled	1h
6	PKILL_2	R/W	1 = Enable automatic noisy color killer function in PAL mode 0 = Disabled	1h
5	SKILL_2	R/W	1 = Enable automatic noisy color killer function in SECAM mode 0 = Disabled	1h
4	CBAL_2	R/W	0 = Normal output 1 = Special output mode	0h
3	FCS_2	R/W	1 = Force decoder output value determined by CCS 0 = Disabled	0h
2	LCS_2	R/W	1 = Enable predetermined output value indicated by CCS when video loss is detected 0 = Disabled	0h
1	CCS_2	R/W	When FCS is set high or a video loss condition is detected when LCS is set high, one of two display colors can be selected. 1 = Blue 0 = Black	0h
0	BST_2	R/W	1 = Enable blue stretch 0 = Disabled	0h

0X5E – CH3 MISCELLANEOUS CONTROL II ON BGCTL = 1

7	NKILL_3	R/W	1 = Enable noisy signal color killer function in NTSC mode 0 = Disabled	1h
6	PKILL_3	R/W	1 = Enable automatic noisy color killer function in PAL mode 0 = Disabled	1h
5	SKILL_3	R/W	1 = Enable automatic noisy color killer function in SECAM mode 0 = Disabled	1h
4	CBAL_3	R/W	0 = Normal output 1 = Special output mode	0h
3	FCS_3	R/W	1 = Force decoder output value determined by CCS 0 = Disabled	0h
2	LCS_3	R/W	1 = Enable predetermined output value indicated by CCS when video loss is detected 0 = Disabled	0h
1	CCS_3	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two display colors can be selected. 1 = Blue 0 = Black	0h
0	BST_3	R/W	1 = Enable blue stretch 0 = Disabled	0h

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X5F – CH4 MISCELLANEOUS CONTROL II ON BGCTL = 1				
7	NKILL_4	R/W	1 = Enable noisy signal color killer function in NTSC mode 0 = Disabled	1h
6	PKILL_4	R/W	1 = Enable automatic noisy color killer function in PAL mode 0 = Disabled	1h
5	SKILL_4	R/W	1 = Enable automatic noisy color killer function in SECAM mode 0 = Disabled	1h
4	CBAL_4	R/W	0 = Normal output 1 = Special output mode	0h
3	FCS_4	R/W	1 = Force decoder output value determined by CCS 0 = Disabled	0h
2	LCS_4	R/W	1 = Enable predetermined output value indicated by CCS when video loss is detected 0 = Disabled	0h
1	CCS_4	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two display colors can be selected. 1 = Blue 0 = Black	0h
0	BST_4	R/W	1 = Enable blue stretch 0 = Disabled	0h]

NOTES:

13. VSHP must be set to '0' if Reg0x83 COMB = 0.

14. For 0x5B[7:4], 0x5B[3:0] and 0x5C[3:0], the following output driving current is achieved for each 4-bit setting if optional pads are bonded.

[Low speed] 3: 12mA, 1: 10mA, 2, 9, B: 8mA, 0: 6mA, 6, 7, 8, A: 4mA, 4, 5: 2mA, C, D, E, F: 0mA

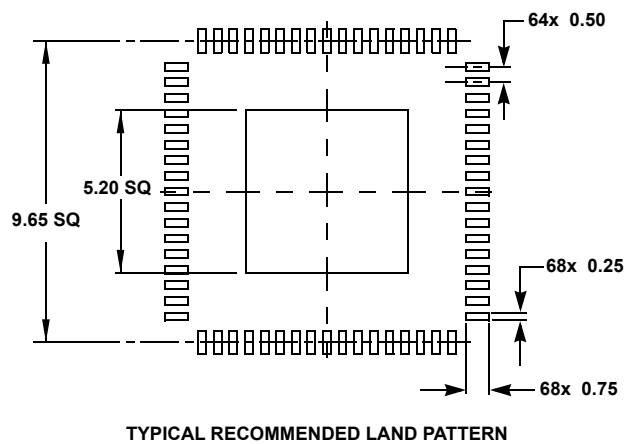
[CLK0 and VD] 3: 16mA, 1, 2: 12mA, 0, 6, 7, 9, B: 8mA, 4, 5, 8, A: 4mA, C, D, E, F: 0mA

Revision History

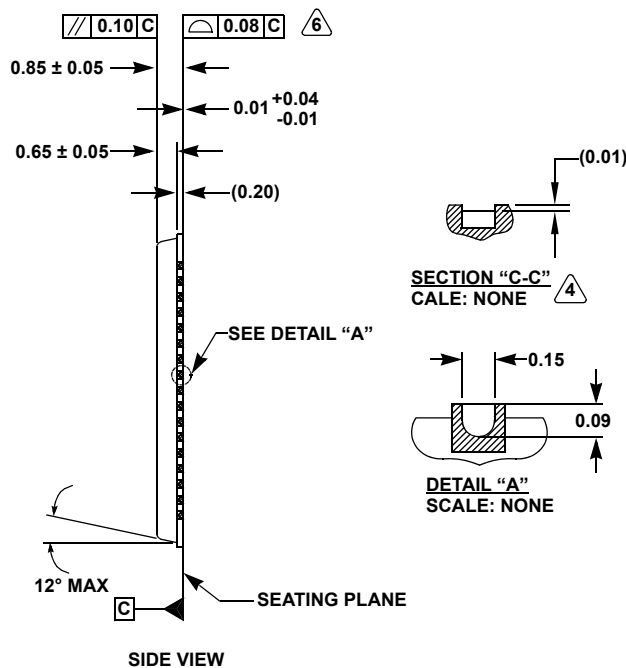
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Apr 8, 2024	4.02	Updated Video Encoder section.
Feb 12, 2024	4.01	Updated Ordering Information table formatting. Updated Pin 32 description. Updated Figure 19.
Feb 15, 2019	4.00	Updated Related Literature section on page 1. Added Tape and Reel (Units) column to Ordering Information table on page 4. Added values for Color Burst Width Range specification on page 10. Updated description of register 0x6E[6:4] on page 40 to "Shared ADC bias control for all four channels. Always set to 3h." Removed "About Intersil" section. Updated disclaimer.
April 7, 2016	3.00	Added AEC-Q100 features bullet. Added Related Literature on page 1. Updated register 0xD6 descriptions for Bits [6:4] and Bits [2:0] on page 42.
May 28, 2015	2.00	Ordering Information table on page 4, added Note: "Add "T" suffix for tape and reel. Please refer to TB347 for details on reel specifications." Thermal Information on page 7, updated Theta JA and JC notes from: 6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details. 7. For θ_{JC} , the "case temp" location is taken at the package top center. To: 6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379. 7. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
January 14, 2015	1.00	- Corrected temperature range in the ordering information table on page 4, from "-40 to +85" to "-40 to +105". - Corrected heading in the Electrical Specification table on page 7 from "Unless otherwise noted, the typical specifications are measured at the following conditions: VDD18=AVDAD=AVDPLL=1.8V, VDD33=VDDO=3.3V, unless otherwise noted. Typical values are at TA = +25 °C. Boldface limits apply across the operating temperature range, -40 °C to +85 °C" to "Unless otherwise noted, the typical specifications are measured at the following conditions: VDDI = 1.2V, VDDO = VDDVD = VDDAP = 3.3V, unless otherwise noted. Typical values are at TA = +25 °C."
December 16, 2014	0.00	Initial Release

Rev 0. 03/14



4. Dimension applies to plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The Pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
6. Unilateral coplanarity zone applies to the exposed pad as well as the terminals.



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