DATASHEET

TW2802, TW2804

Multiple Video Decoder for Security Applications

FN7732
Rev. 1.00
May 19, 2017

The TW280X includes four high quality NTSC/ PAL video decoders, which convert analog composite to digital component YCbCr for security application. The TW280X contains four 10-bit A/D and proprietary digital gain/clamp controllers and uses proprietary techniques for separating luminance and chrominance to reduce both cross-luminance and cross-chrominance artifacts. The high performance dual scalers in each channel offer two differently scaled video outputs with 54MHz ITU-R BT.656 format for security system design. Four built-in motion detectors can also increase the feature of security system.

Applications

Security systems

Device Options

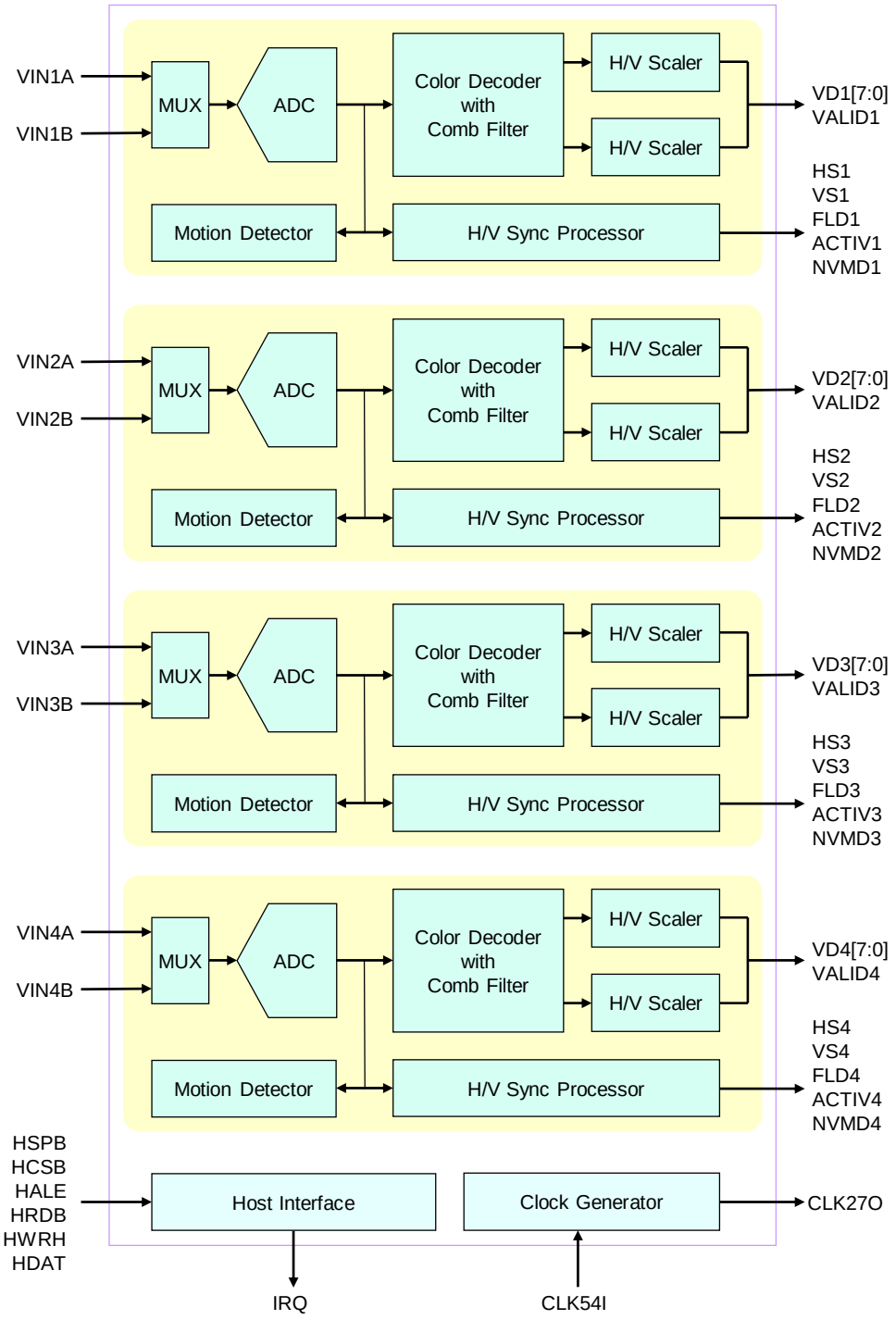
Device Name	Features
TW2802	Two-Channel Video Decoder
TW2804	Four-Channel Video Decoder

Features

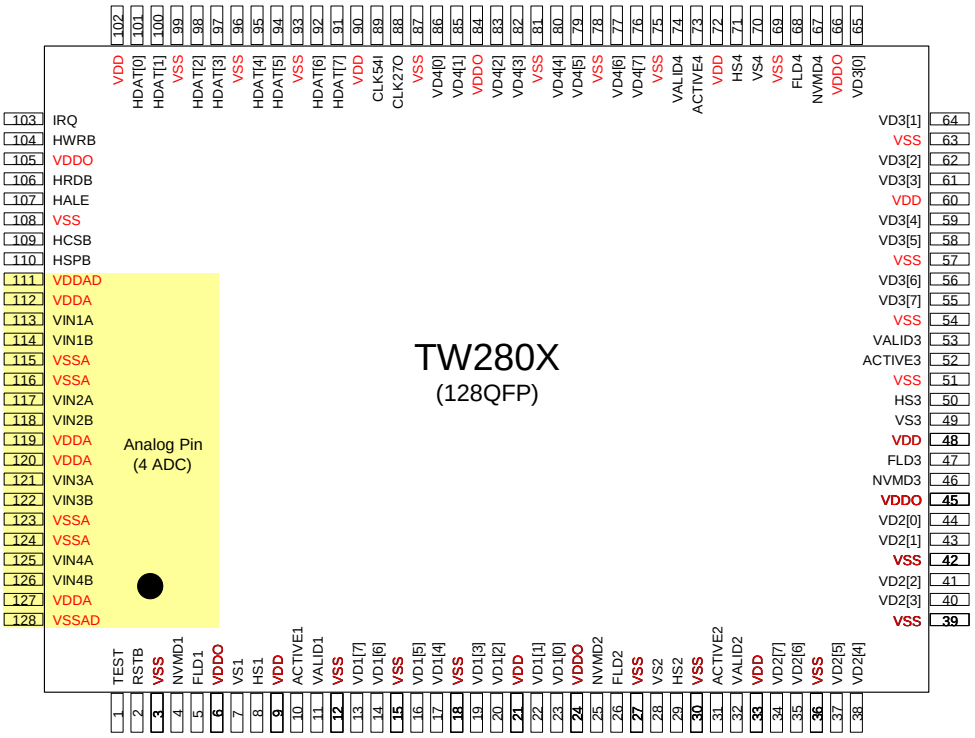
- Accepts all NTSC (M/N/4.43) / PAL (B/D/G/H/I/K/L/M/N/60) standard formats with auto detection
- Four 10-bit video CMOS analog to digital converters
- Adjust video level with proprietary automatic clamp and gain control system
- Proprietary architecture for locking to weak, noisy, or unstable signals
- High performance adaptive comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- PAL delay lines for correcting PAL phase errors
- Programmable hue, saturation, contrast, brightness and sharpness
- Dual high quality horizontal and vertical down scaler for each channel
- Four built-in motion detectors for security system
- Supports the standard ITU-R BT.656/8-bit ITU-R BT.601 format
- Supports two differently scaled output mode with 54MHz ITU-R BT.656 format
- Supports a two-wire serial or parallel interface
- Low power consumption
- 128 PQFP package

Table of Contents

Block Diagram



Pin Configuration



Pin Description

Analog Interface Pins

Name	Number	Type	Description
VIN1A	113	A	Composite video input A of Channel 1. Must be connected through 2.2uF cap to input.
VIN1B	114	A	Composite video input B of Channel 1. Must be connected through 2.2uF cap to input.
VIN2A	117	A	Composite video input A of Channel 2. Must be connected through 2.2uF cap to input.
VIN2B	118	A	Composite video input B of Channel 2. Must be connected through 2.2uF cap to input.
VIN3A	121	A	Composite video input A of Channel 3. Must be connected through 2.2uF cap to input.
VIN3B	122	A	Composite video input B of Channel 3. Must be connected through 2.2uF cap to input.
VIN4A	125	A	Composite video input A of Channel 4. Must be connected through 2.2uF cap to input.
VIN4B	126	A	Composite video input B of Channel 4. Must be connected through 2.2uF cap to input.

Digital Data Interface Pins

Name	Number	Type	Description
VD1 [7:0]	13,14,16,17, 19,20,22,23	O	Dual scaled video data output for Channel 1.
VD2 [7:0]	34,35,37,38, 40,41,43,44	O	Dual scaled video data output for Channel 2.
VD3 [7:0] *	55,56,58,59, 61,62,64,65	O	Dual scaled video data output for Channel 3.
VD4 [7:0] *	76,77,79,80, 82,83,85,86	O	Dual scaled video data output for Channel 4.
VALID1	11	O	Valid data indicator for Channel 1.
VALID2	32	O	Valid data indicator for Channel 2.
VALID3*	53	O	Valid data indicator for Channel 3.
VALID4*	74	O	Valid data indicator for Channel 4.
HS1	8	O	Horizontal sync output for Channel 1.
HS2	29	O	Horizontal sync output for Channel 2.
HS3*	50	O	Horizontal sync output for Channel 3.
HS4*	71	O	Horizontal sync output for Channel 4.
VS1	7	O	Vertical sync output for Channel 1.
VS2	28	O	Vertical sync output for Channel 2.
VS3*	49	O	Vertical sync output for Channel 3.
VS4*	70	O	Vertical sync output for Channel 4.
FLD1	5	O	Even/odd field flag output for Channel 1.
FLD2	26	O	Even/odd field flag output for Channel 2.
FLD3*	47	O	Even/odd field flag output for Channel 3.
FLD4*	68	O	Even/odd field flag output for Channel 4.
ACTIVE1	10	O	Active flag output for Channel 1.
ACTIVE2	31	O	Active flag output for Channel 2.
ACTIVE3*	52	O	Active flag output for Channel 3.
ACTIVE4*	73	O	Active flag output for Channel 4.
NVMD1	4	O	Video loss or Motion detection flag for Channel 1.
NVMD2	25	O	Video loss or Motion detection flag for Channel 2.
NVMD3*	46	O	Video loss or Motion detection flag for Channel 3.
NVMD4*	67	O	Video loss or Motion detection flag for Channel 4.

Notes: * Disabled for TW2802

System Control Pins

Name	Number	Type	Description
RSTB	2	I	System reset.
CLK54I	89	I	54MHz system clock input.
CLK27O	88	O	27MHz Clock output.
TEST	1	I	Test pin. Connect to ground.
HSPB	110	I	Select Serial/Parallel host interface.
HCSB	109	I	Chip select for parallel interface. Slaver address [0] for serial interface.
HALE	107	I	Address line enable for parallel interface. Serial clock for serial interface.
HRDB	106	I	Read enable for parallel interface. Ground for serial interface.
HWRB	104	I	Write enable for parallel interface. Ground for serial interface.
HDAT [7:0]	91,92,94,95, 97,98,100,101	I/O	Data bus for parallel interface. HDAT [7] is serial data for serial interface. HDAT [6:1] is slaver address [6:1] for serial interface. HCSB is slaver address [0].
IRQ	103	O	Interrupt request by video loss and Motion detection

Power/Ground Pins

Name	Number	Type	Description
VDD	9,21,33,48,60, 72,90,102	P	Digital power for internal logic. 2.5V.
VDDO	6,24,45, 66,84,105	P	Digital power for output driver. 3.3V.
VSS	3,12,15,18, 27, 30,36,39,42,51, 54,57,63,69,75, 78,81,87,93,96, 99,108	G	Digital ground.
VDDA	112,119,120,127	P	Analog power. 2.5V.
VSSA	115,116,123,124	G	Analog ground.
VDDAD	111	P	Analog digital power. 2.5V.
VSSAD	128	G	Analog digital ground.

Functional Description

Video Input Formats

The TW280X supports all NTSC/PAL standard formats and has built-in automatic standard detection circuit. The following Table 1 shows the identified standards. Automatic standard detection can be overridden by writing the value into the IFMTMAN and IFORMAT register (0x01, 0x41, 0x81, 0xC1). Even in no-video status, the device can be forced to free-run in a particular video standard mode for fast locking by programming IFORMAT register.

Table 1 Input Video Format Supported

Format	Line/Fv (Hz)	Fh (KHz)	Fsc (MHz)
NTSC-M* NTSC-J	525/59.94	15.734	3.579545
NTSC-4.43*	525/59.94	15.734	4.43361875
NTSC-N	625/50	15.625	3.579545
PAL-BDGHI PAL-N*	625/50	15.625	4.43361875
PAL-M*	525/59.94	15.734	3.57561149
PAL-NC	625/50	15.625	3.58205625
PAL-60	525/59.94	15.734	4.43361875

Notes: * 7.5 IRE Setup

Analog-to-Digital Converter

The TW280X contains four 10-bit Analog to Digital converters that digitizes the analog video inputs. As the inputs are digitized at greater than two times that of the Nyquist sampling rate, only simple external anti-aliasing LPF are needed to prevent out-of-band frequencies. Each ADC has two analog switches that are controlled by ANA_SW (0x22, 0x62, 0xA2, 0xE2) registers. The A/D converters can also be put into power-down mode by the ADC_PWDN (0x78) registers.

Sync Processing

The sync processor of TW280X detects horizontal synchronization and vertical synchronization signals in the composite. The TW280X uses proprietary technology for locking to weak, noisy, or unstable signals such as those from on air signal and fast forward or backward of VCR system.

Video Level Adjustment

A patented digital gain and clamp control circuit restores the ac coupled video signal to a fixed DC level. The clamping circuit provides line-by-line restoration of the video pedestal level to a fixed DC reference voltage. In no AGC mode, the gain control circuit adjusts only the video sync gain to achieve desired sync amplitude so that the active video is bypassed regardless of the gain control. But when AGC mode is enabled, both active video and sync are adjusted by the gain control. The range of AGC is from –6dB to 18dB approximately.

Horizontal Sync Processing

The horizontal synchronization processing contains a sync separator, a PLL and the related decision logic. The horizontal sync separator detects the horizontal sync by examining low-pass filtered video input whose level is lower than a threshold. Additional logic is also used to avoid false detection on glitches. The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. In case the horizontal sync is missing, the PLL is on free running status that matches the standard raster frequency.

Vertical Sync Processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field.

Color Decoding

Decimation Filter

The digitized composite video data at 2X pixel clock rate first passes through decimation filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image. Fig 1 shows the characteristic of the decimation filter.

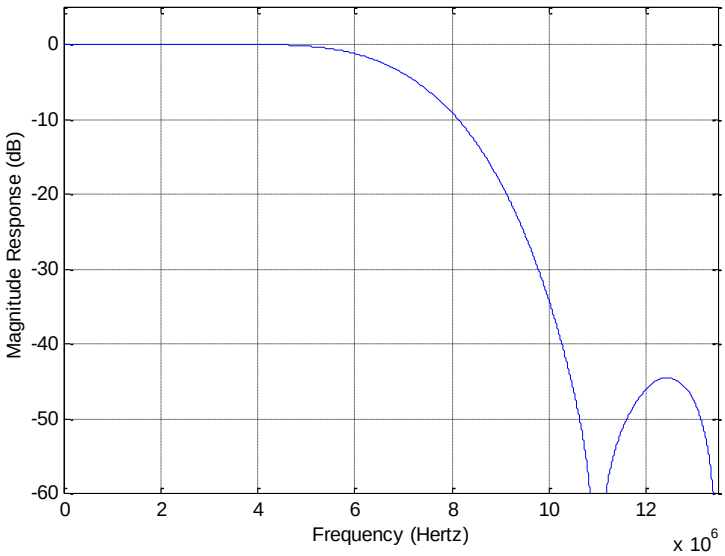


Fig 1 The Characteristic of the Decimation Filter

Y/C Separation

The adaptive comb filter is used for high quality luminance/chrominance separation from NTSC/PAL composite video signals. The comb filter improves the luminance resolution and reduces noise such as cross-luminance and cross-color. The adaptive algorithm eliminates most of errors without introducing new artifacts or noise. To accommodate some viewing preferences, additional chrominance trap filters are also available in the luminance path. Fig. 2 and Fig 3 show the frequency response of notch filter for each system NTSC and PAL.

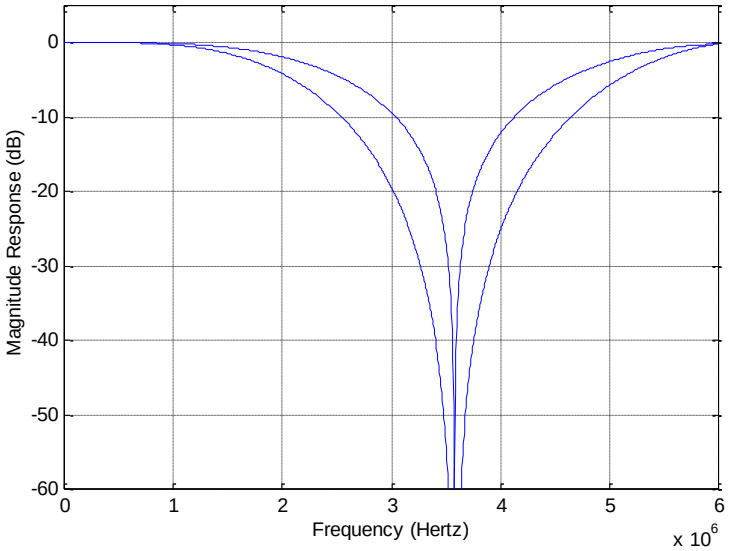


Fig. 2 The Characteristics of Luminance Notch Filter for NTSC

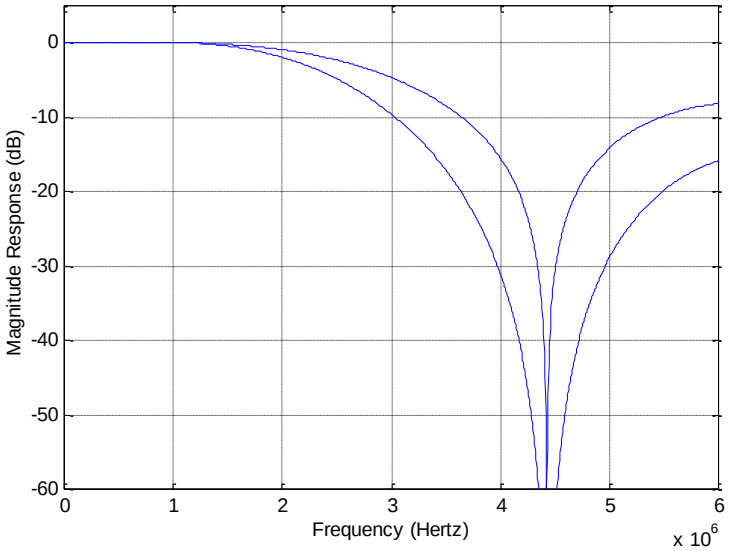


Fig 3 The Characteristics of Luminance Notch Filter for PAL

Luminance Processing

The luminance signal is separated by adaptive comb or trap filter is then fed to a peaking circuit. The peaking filter enhances the high frequency components of the luminance signal via the Y_PEAK (0x14, 0x54 0x94, 0xD4) register. Fig. 4 shows the characteristics of the peaking filter for four different gain modes. The picture contrast and brightness adjustment is provided through CONT (0x11, 0x51, 0x91, 0xD1) and BRT (0x12, 0x52, 0x92, 0xD2) registers. The contrast adjustment range is from approximately 0 to 200 percent, and the brightness adjustment is in the range of ±25 IRE. Moreover, a high frequency coring function is also embedded in TW280X to minimize a high frequency noise. The coring level is adjustable through the Y_H_CORE (0xF8) register.

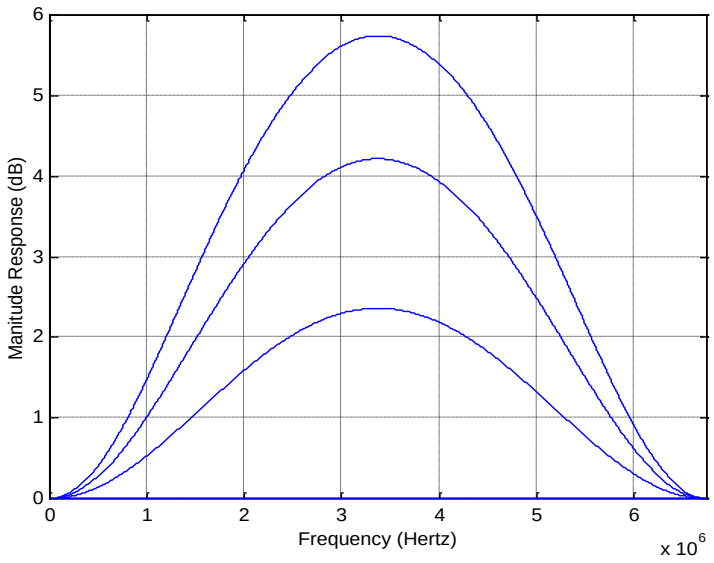


Fig. 4. The Characteristic of Luminance Peaking filter

Chrominance Processing

Chrominance Demodulation

The chrominance demodulation is done by first quadrature mixing for NTSC and PAL. The mixing frequency is equal to the sub-carrier frequency of NTSC and PAL. After the mixing, a LPF is used to remove 2X carrier signal and yield chrominance components. The LPF characteristic can be selected for optimized transient color performance. In case of a mistuned IF source, IF compensation filter makes up for any attenuation at higher frequencies or asymmetry around the color sub-carrier. The gain for the upper chrominance side band is controlled by IFCMP_MD (0x13, 0x53, 0x93, 0xD3) register. Fig. 5 and Fig. 6 show the frequency response of IF-compensation filter and chrominance LPF.

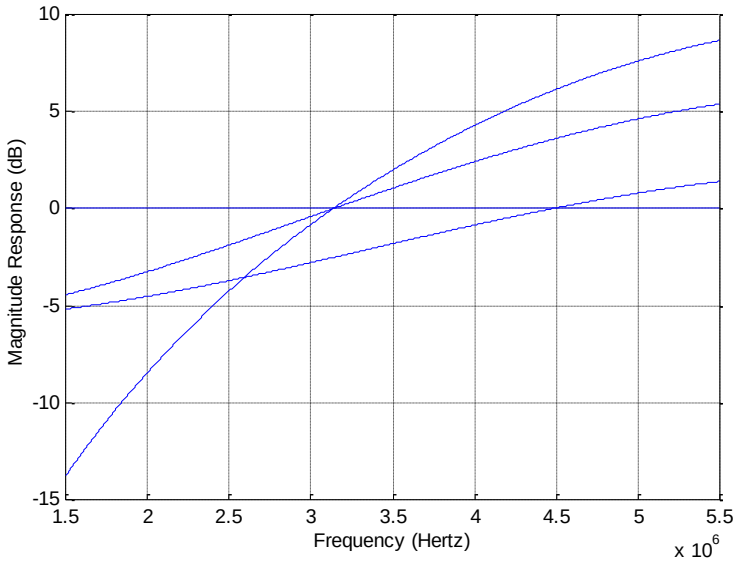


Fig. 5 The Characteristics of IF-compensation Filter

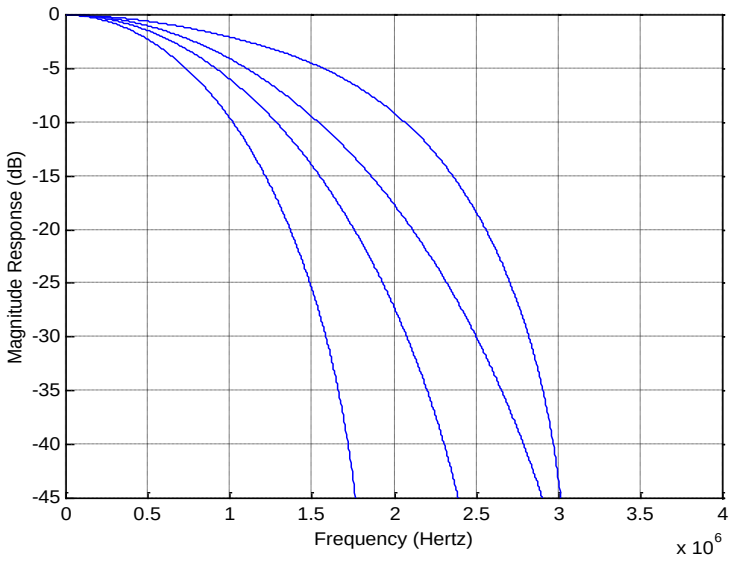


Fig. 6 The Characteristics of Chrominance Low Pass Filter

ACC (Automatic Color gain control)

The ACC (Automatic Color gain Control) compensates for reduced amplitudes caused by high frequency suppression in video signal. The range of ACC is from –6dB to 30dB approximately. For black and white video or very weak and noisy signals, the color will be off by the internal color killing circuit. The color killer function can also be always enabled or disabled by programming CKIL (0x14, 0x54, 0x94, 0xD4) register.

Chrominance Gain, Offset and Hue Adjustment

The color saturation can be adjusted by changing the register SAT (0x10, 0x50, 0x90, 0xD0). The Cb and Cr gain can be also adjusted independently by programming UGAIN (0x3C) and VGAIN (0x3D) register. Likewise, the Cb and Cr offset can be programmed through U_OFF (0x3E) and V_OFF (0x3F) registers. Hue control is achieved with phase shift of the digitally controlled oscillator. The phase shift can be programmed through HUE (0x0F, 0x4F, 0x8F, 0xCF) register.

Video Scaling and Cropping

The TW280X provides two methods to reduce the amount of video pixel data, scaling and cropping. The scaling function provides video image at lower resolution while the cropping function supplies only a portion of the video image.

Video Scaling

The TW280X includes a high quality horizontal and vertical down scaler. The video images can be downscaled in both horizontal and vertical direction to an arbitrary size. The luminance horizontal scaler includes an anti-aliasing filter to reduce image artifacts in the resized image and a 32 poly-phase filter to accurately interpolate the value of a pixel. This results in more aesthetically pleasing video as well as higher compression ratios in bandwidth-limited applications. Fig 7 shows the frequency response of anti-aliasing filter for horizontal scaling and Fig 8 shows the 32 poly-phase filter characteristics. Similarly, the vertical scaler also contains an anti-aliasing filter and 16 poly-phase filter for down scaling. The filter characteristics are shown in Fig. 9.

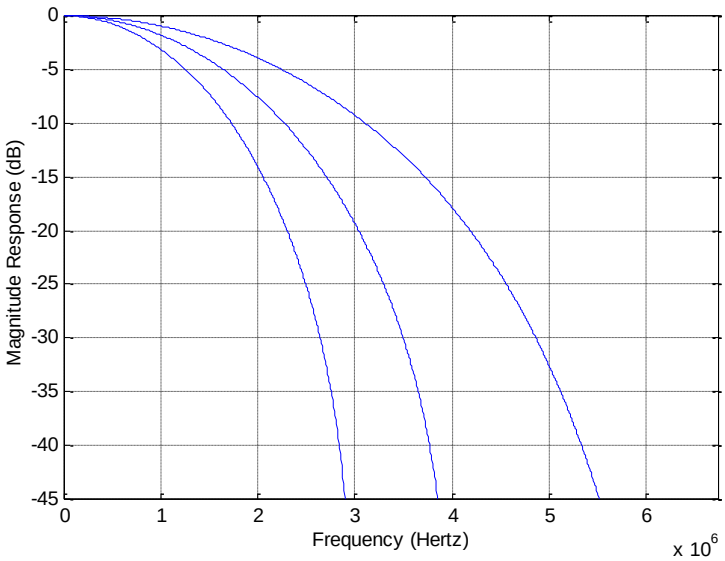


Fig 7 The Characteristics of Anti-aliasing filter for horizontal luminance scaling

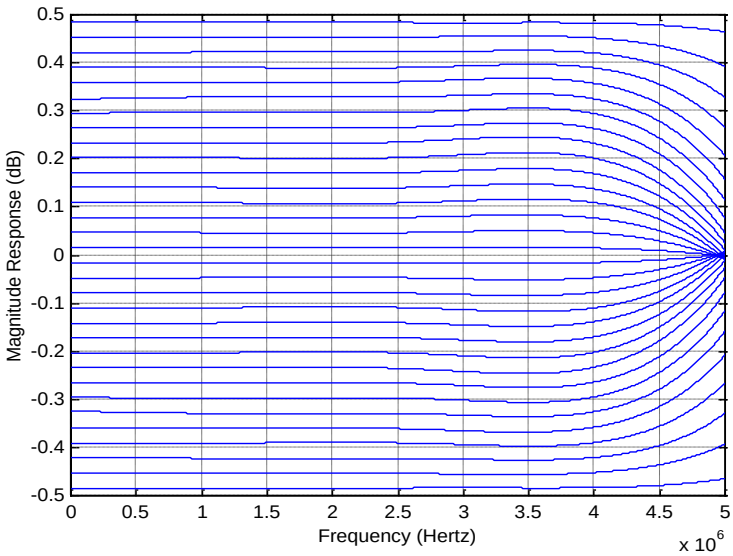


Fig 8 The Characteristics of Group delay for horizontal luminance scaling

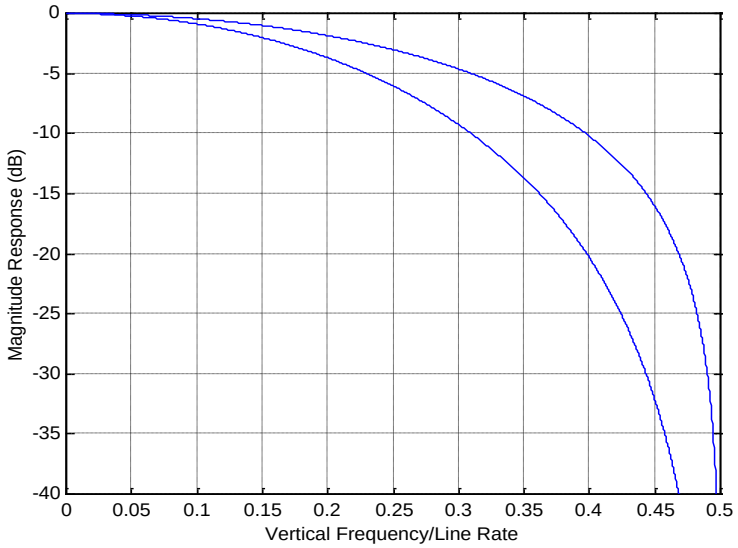


Fig. 9 The Characteristics of Anti-aliasing filter for vertical luminance scaling

Down scaling is achieved by programming the horizontal scaling register (HSCALE) and vertical scaling register (VSCALE). When no scaled video image, the TW280X will output the number of pixels per line as specified by the HACTIVE register. If the number of output pixels required is smaller than the number specified by the HACTIVE register, the 16-bit HSCALE register is used to reduce the output pixels to the desired number.

Following equation is used to determine the horizontal scaling ratio to be written into the 16-bit HSCALE register.

HSCALE = [$N_{pixel\_desired}$/ HACTIVE] * (2^16 – 1)
Where $N_{pixel\_desired}$ is the desired number of active pixels per line

For example, to scale full picture (HACTIVE is 720) to CIF (360 pixels), the HSCALE value can be found as:

HSCALE = [360/720] * (2^16 – 1) = 0x7FFF

Following equation is used to determine the vertical scaling ratio to be written into the 16-bit VSCALE register.

VSCALE = [$N_{line\_desired}$ / VACTIVE] * (2^16 - 1)
Where $N_{line\_desired}$ is the desired number of active lines per field

For example, to scale full picture (VACTIVE is 240or288) to CIF (120/144 lines), the VSCALE value can be found as:

VSCALE = [120 / 240] * (2^16 – 1) = 0x7FFF for 60Hz
VSCALE = [144 / 288] * (2^16 – 1) = 0x7FFF for 50Hz

The scaling ratios of popular case are listed in Table 2

Table 2 HSCALE and VSCALE value for some popular video formats

Scaling Ratio	Format	Output Resolution	HSCALE	VSCALE
1	NTSC PAL	720x480 720x576	0xFFFF 0xFFFF	0xFFFF 0xFFFF
1/2 (CIF)	NTSC PAL	360x240 360x288	0x7FFF 0x7FFF	0x7FFF 0x7FFF
1/4 (QCIF)	NTSC PAL	180x120 180x144	0x3FFF 0x3FFF	0x3FFF 0x3FFF

Video Cropping

The cropping function allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Fig 10. The first active line is defined by the VDELAY register and the first active pixel is defined by the HDELAY register. The VACTIVE register can be programmed to define the number of active lines in a video field, and the HACTIVE register can be programmed to define the number of active pixels in a video line.

The horizontal delay register HDELAY determines the number of pixel delays between the horizontal reference and the leading edge of the active region. The horizontal active register HACTIVE determines the number of active pixels to be processed. Note that these values are referenced to the pixel number before scaling. Therefore, even if the scaling ratio is changed, the active video region used for scaling remains unchanged as set by the HDEALY and HACTIVE register. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line
Where the total number of pixels per line is 858 for 60Hz and 864 for 50Hz

To process full size region, the HDELAY should be set to 32 and HACTIVE set to 720 for both 60Hz and 50Hz system.

The vertical delay register (VDELAY) determines the number of line delays from the vertical reference to the start of the active video lines. The vertical active register (VACTIVE) determines the number of lines to be processed. These values are referenced to the incoming scan lines before the vertical scaling. In order for the vertical cropping to work properly, the following equation should be satisfied.

VDELAY + VACTIVE < Total number of lines per field
Where the total number of lines per field is 262 for 60Hz and 312 for 50Hz

To process full size region, the VDELAY should be set to 7 and VACTIVE set to 240 for 60Hz and the VDELAY should be also set to 4 and VACTIVE set to 288 for 50Hz.

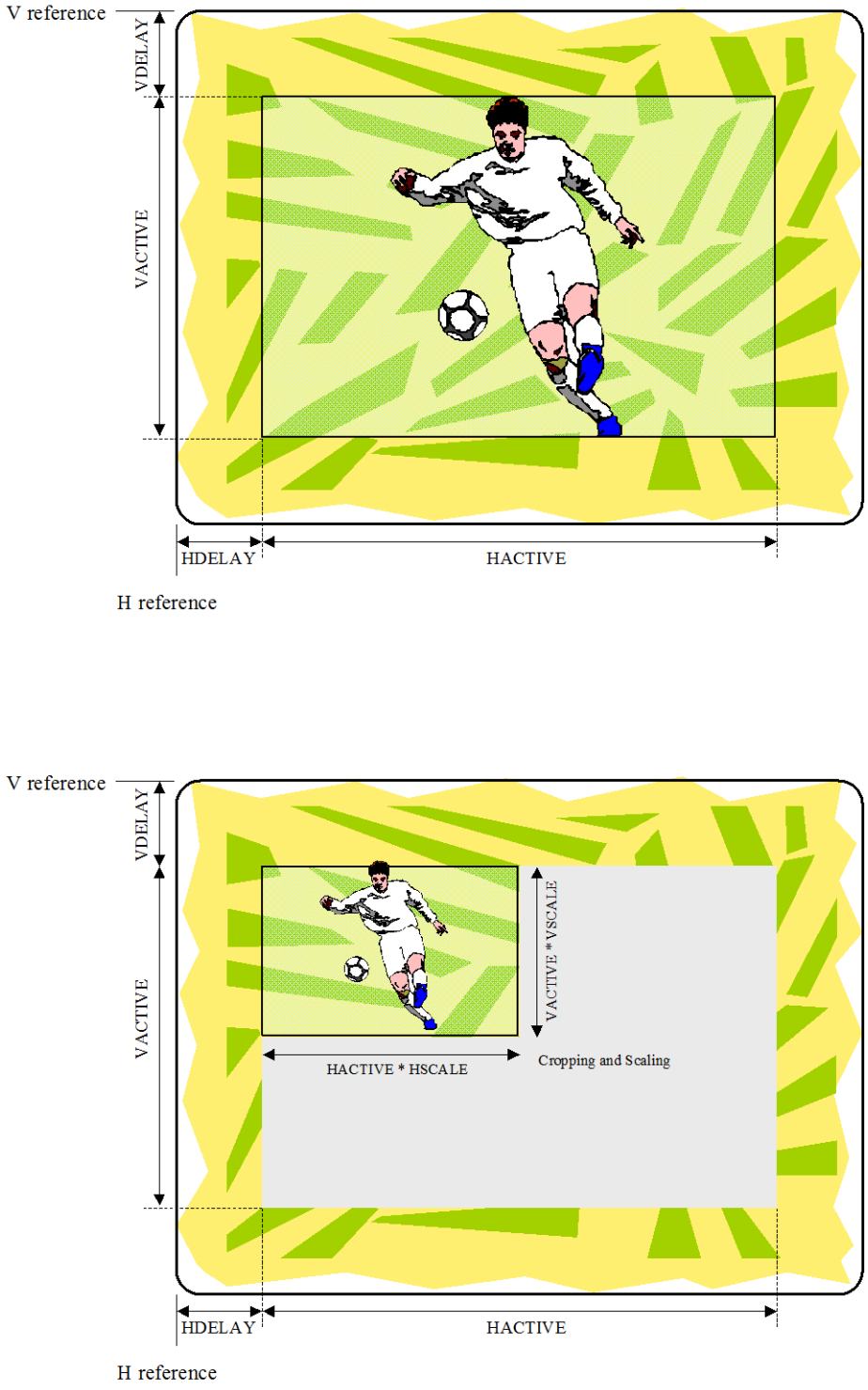


Fig 10 The Effect of Cropping and Scaling Active Registers

Motion Detector

The TW280X supports hardware motion detector for four channels individually. The motion detection algorithm built in the TW280X uses difference between two luminance levels of the adjacent two fields. Motion is detected for full screen image and each channel has 144(12x12) mask regions, which enable or disable motion detection for that region. The motion detection has several attributes, sensitivity and velocity of motion detector controlled by programming the register. The Host takes the result of motion detection via IRQ or NVMD pin. Refer to the host Interface for the detail.

Sensitivity Control

The motion detector has three sensitivity control parameters. One is level sensitivity control parameter (LVLSENS), another is spatial sensitivity control parameter (SPTSENS), and a third is temporal sensitivity control parameter (TMPSENS). The recommended values of sensitivity control parameters for a proper operation are listed in Table 3.

LVLSENS (Level Sensitivity)

In built-in motion detection algorithm, motion is detected when luminance level difference between two fields is greater than the value, which is defined by LVLSENS. The smaller LVLSENS value makes the motion detector sense more sensitively, and the larger is the opposite. When LVLSENS is too small, the motion detector can be weak in noise.

SPTSENS (Spatial Sensitivity)

Motion detection from only luminance level difference between two fields is very weak in spatial random noise. To remove the fake motion detection from the random noise, spatial filter is used. SPTSENS adjusts the window size of the spatial filter to control the spatial sensitivity so that the large SPTSENS value increases the immunity of spatial random noise.

TMPSENS (Temporal Sensitivity)

Likewise, temporal filter is used to remove the fake motion detection from the temporal random noise. TMPSENS regulates the number of taps in the temporal filter to control the temporal sensitivity so that the large TMPSENS value increases the immunity of temporal random noise.

Table 3 The recommended values of sensitivity parameters for a proper operation

TMPSENS	SPTSENS	LVLSENS		
		More Sensitive		Less Sensitive
0	0	7	~	10
	1	3	~	9
	2	2	~	8
	3	2	~	7
1	0	3	~	9
	1	2	~	8
	2	2	~	7
	3	2	~	6
2	0	3	~	8
	1	2	~	7
	2	1	~	6
	3	1	~	5
3	0	3	~	7
	1	1	~	6
	2	1	~	5
	3	1	~	4

Velocity Control

Motion has various velocities. That is, in a fast motion an object appears and disappears rapidly between the adjacent fields while in a slow motion it is to the contrary. As the built-in motion detection algorithm uses the luminance level difference between two adjacent fields, a slow motion is inferior in detection rate to a fast motion. To compensate this weakness, the MDPERIOD parameter is used. MDPERIOD parameter adjusts the field interval in which the luminance level is compared. Thus, for detection of a fast motion a small value is needed and for a slow motion a large value is required. The parameter MDPERIOD value should be greater than TMPSENS value.

Mask Detection Region

The motion in the specific area can be ignored by the control of mask area. The full screen image is divided into 144 (12x12) mask areas. If the mask bit in specific area is programmed into high, the specific area is ignored in operation of motion detector, as illustrated in Fig. 11. But for proper operation, more than four mask areas should be enabled in any case.

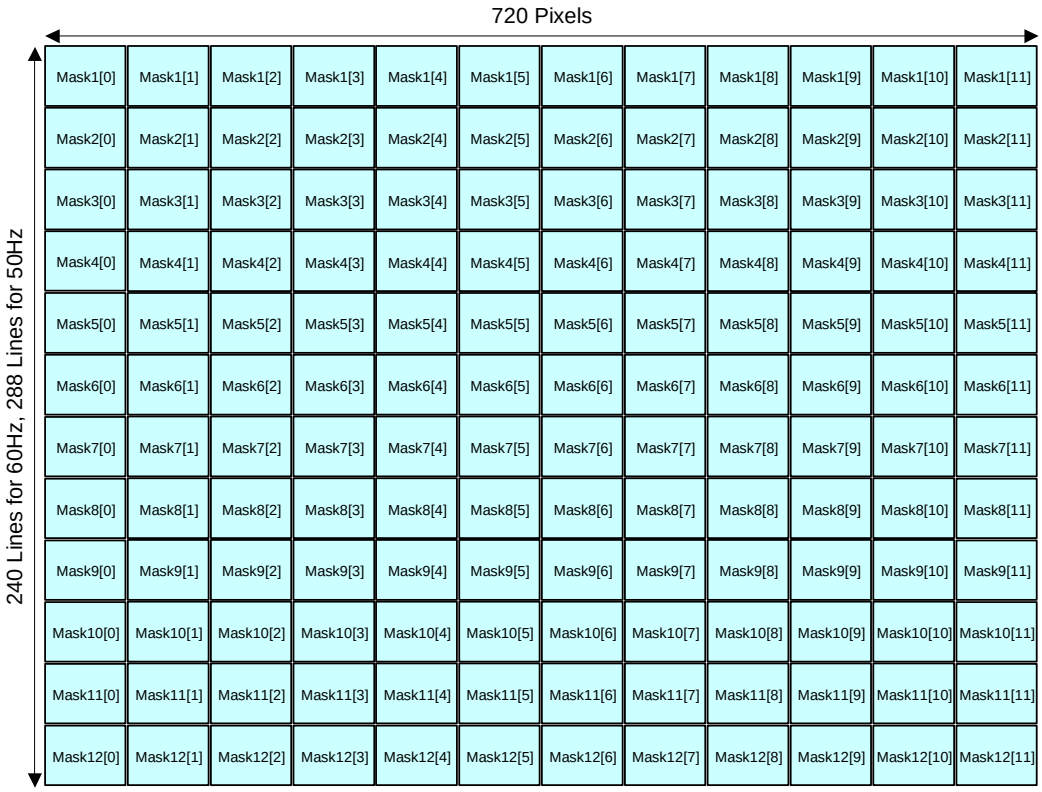


Fig. 11 Motion detection mask windows

Output Format

The TW280X supports three 8-bit output formats, ITU-R BT.656, 8-bit ITU-R BT.601, and Dual ITU-R BT.656 with 54MHz data format. The output data is synchronous with rising or falling edge of CLK27O for ITU-R BT.656 and 8-bit ITU-R BT.601 format and with rising edge of CLK54I for Dual ITU-R BT.656 with 54MHz format. The polarity of CLK27O is controlled by the CK27O_POL register (0x3B). For Dual ITU-R BT.656 with 54MHz format, two kinds of scaled image are time-multiplexed with 54MHz. The output formats are selected by the OUT_FMT register (0x22, 0x62, 0xA2, 0xE2).

ITU-R BT.656 Format

In ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. During the blanking time, the YCbCr outputs have a value 0x00 for Y, Cr and Cb. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. If scaling is used, the number of active pixels per line is constant with invalid pixel indicated by the blanking code 0x00. The output timing is illustrated in Fig. 12. The SAV and EAV sequences are shown in Table 4. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit (0x22, 0x62, 0xA2, 0xE2).

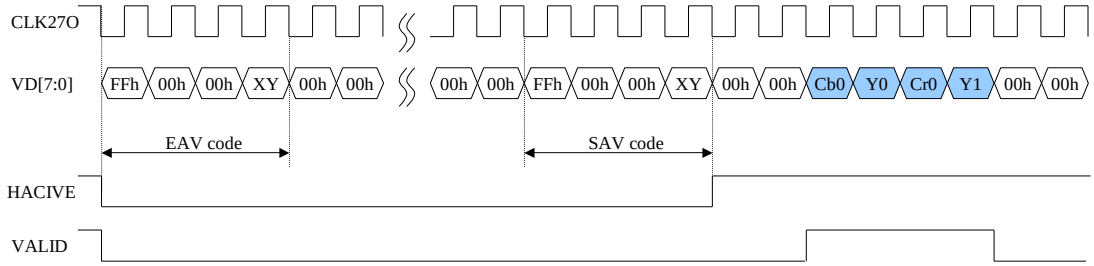


Fig. 12 Timing Diagram of ITU-R BT.656 format on HSCALE = 16'h7FFF

Table 4 ITU-R 656 SAV and EAV Code Sequence

Condition			656 FVH Value			SAV/EAV Code Sequence				
Field	Vertical	Horizontal	F	V	H	First	Second	Third	Fourth	
									Normal	Option (Novideo)
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

8-bit ITU-R BT.601 Format

8-bit ITU-R BT.601 format is 8-bit YCbCr 4:2:2 data stream with additional timing information such as syncs and field flag. The video output timing is illustrated in Fig 13 and Fig 14.

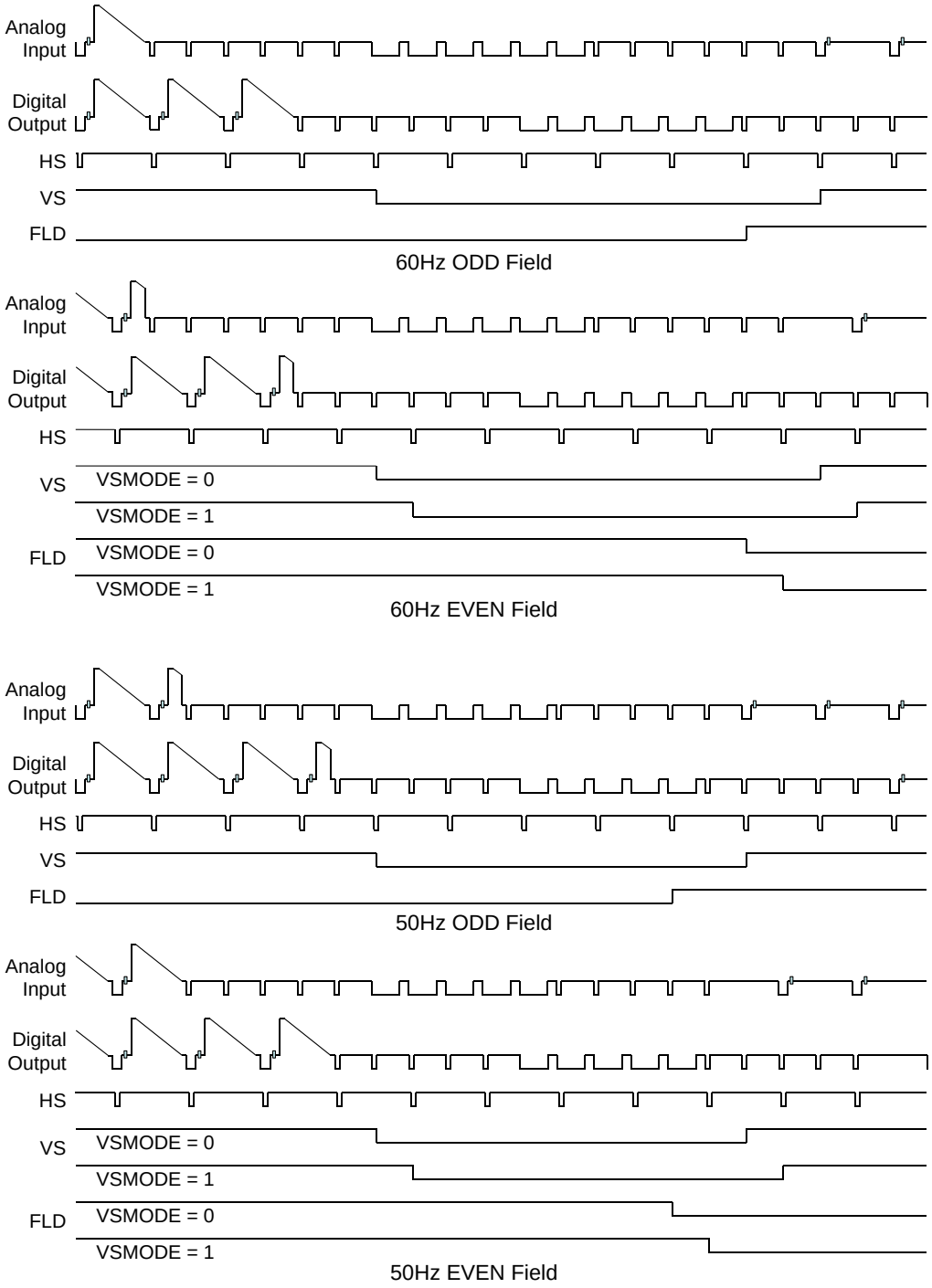
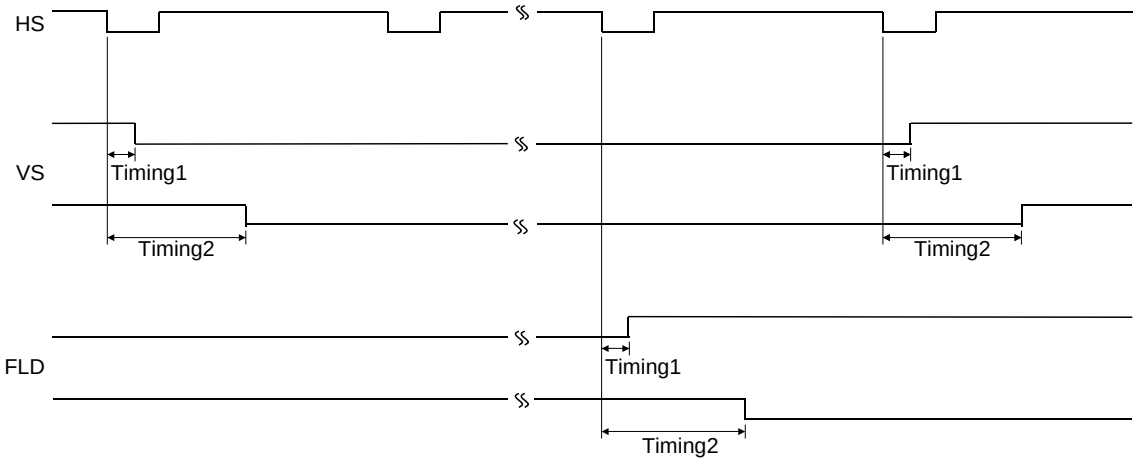


Fig 13 Vertical Timing for 60Hz / 50Hz Video



Timing1 : 40 system clock(54MHz) for the Even field with VSMODE=1 or Odd field
Timing2 : 1760 system clock(54MHz) for the Even field with VSMODE=0

Fig 14 Horizontal and Vertical Timing in Video Output

Dual ITU-R BT.656 Format in 54MHz

Dual ITU-R BT.656 format in 54MHz is very useful to the security applications, which need two independently scaled video images for display and record purpose. In the case of HSCALE_X = 16'h7FFF and HSCALE_Y = 16'hFFFF, the timing diagram of video output is illustrated in Fig 15.

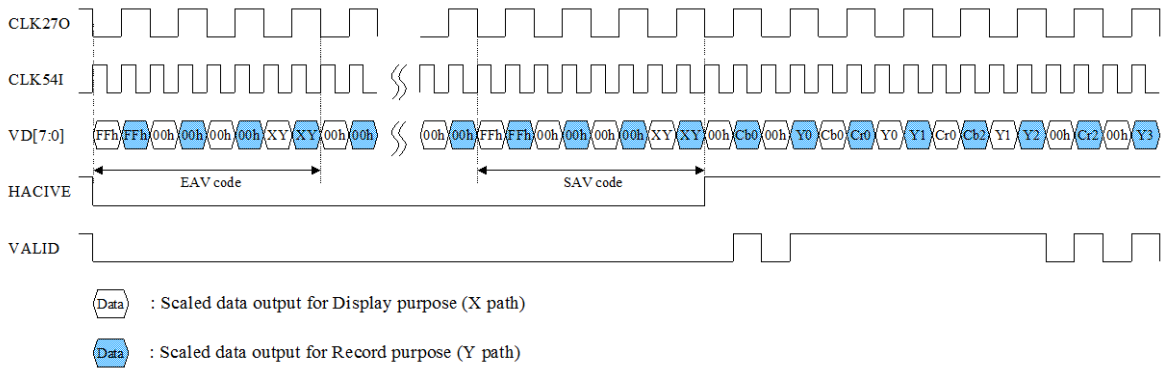


Fig 15 Timing Diagram in Dual ITU-R BT.656 with 54MHz format

Host Interface

The TW280X provides serial and parallel interfaces that can be selected by HSPB pin. When HSPB is low, the parallel interface is selected, the serial interface for high. Some of the interface pins serve a dual purpose depending on the working mode. The pins HALE and HDAT[7] in parallel mode become SCLK and SDAT pins in serial mode respectively. Each interface protocol is shown in the following figure.

Table 5 Pin Assignment for Serial/Parallel Interface

Pin Name	Serial Mode	Parallel Mode
HSPB	HIGH	LOW
HALE	SCLK	AEN
HRDB	Not Used	RENB
HWRB	Not Used	WENB
HCSB	Slave Address[0]	CSB
HDAT[0]	Not Used	PDATA[0]
HDAT[1]	Slave Address[1]	PDATA[1]
HDAT[2]	Slave Address[2]	PDATA[2]
HDAT[3]	Slave Address[3]	PDATA[3]
HDAT[4]	Slave Address[4]	PDATA[4]
HDAT[5]	Slave Address[5]	PDATA[5]
HDAT[6]	Slave Address[6]	PDATA[6]
HDAT[7]	SDAT	PDATA[7]

Serial Interface

HDAT[6:1] and HCSB pins define slave address. Therefore, any slave address can be assigned for full flexibility. TW2804 also supports auto index increments in write/read mode if the data are in sequential order. Data transfer rate on the bus is up to 400 Kbits/s.

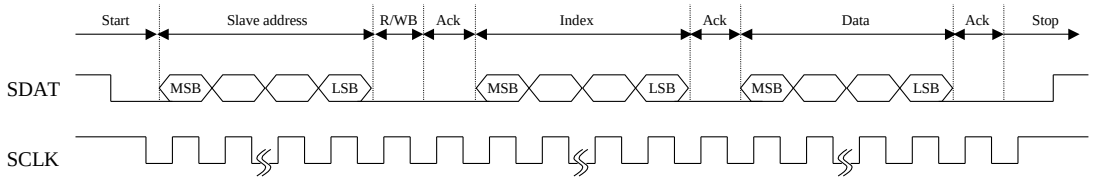


Fig 16 Write mode in Serial Interface

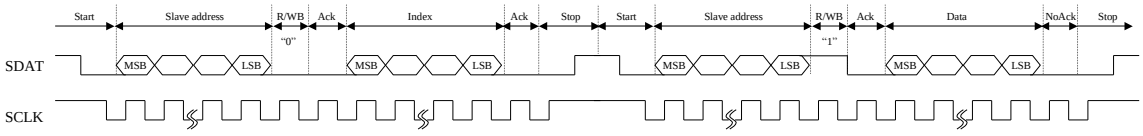


Fig 17 Read mode in Serial Interface

Parallel Interface

The following figures show the write/read timing chart of parallel interface. The parallel interface supports auto index increment after each byte of data is sent with WENB. Therefore, the host can write multiple bytes to the slave without additional address if they are in sequential order. The host completes the transfer cycle with CSB which is Low to High transition. Auto index increment is also supported in read mode.

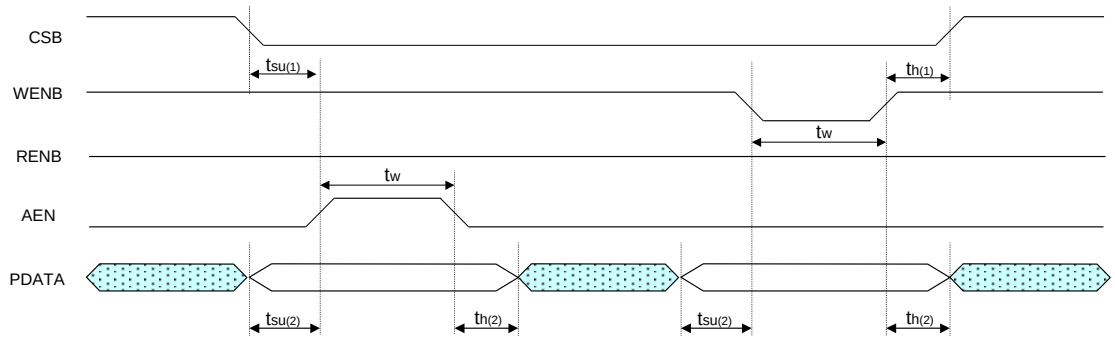


Fig 18 Write mode in Parallel interface

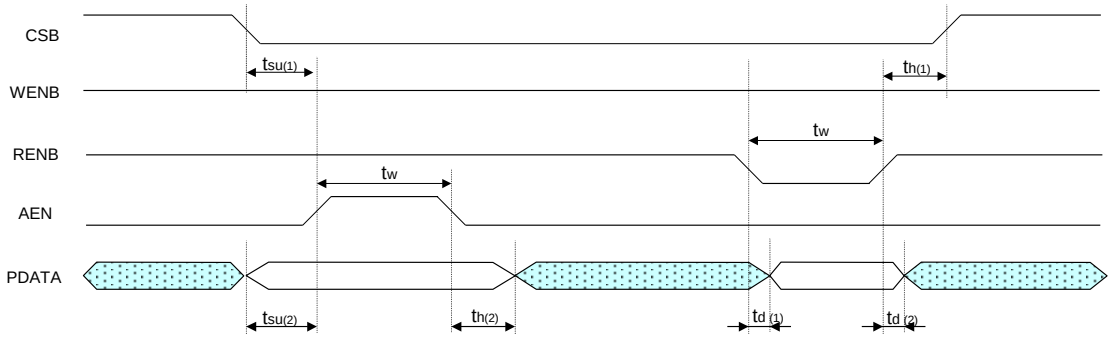


Fig 19 Read mode in Parallel interface

Table 6 Parallel Interface Timing Parameter

Parameter	Symbol	Min	Typ	Max	Units
CSB setup until AEN active	$t_{su\ (1)}$	10			ns
PDATA setup until AEN, WENB active	$t_{su\ (2)}$	10			ns
AEN, WENB, RENB active pulse width	t_w	40			ns
CSB hold after WENB, RENB inactive	$t_{h\ (1)}$	60			ns
PDATA hold after AEN, WENB inactive	$t_{h\ (2)}$	60			ns
PDATA delay after RENB active	$t_{d\ (1)}$			12	ns
PDATA delay after RENB inactive	$t_{d\ (2)}$			12	ns

Interrupt Interface

The TW280X provides the interrupt request function via an IRQ pin. Any video loss detection or motion detection will make the IRQ pin high until cleared via register IRQCLR (0x39) by the host. The host processor will read the interrupt status register DET_NVMD (0x38) to find out which channel has sensed motion or video loss. Writing high to the corresponding bit of the interrupt clear register IRQCLR (0x39) will clear the interrupt request. Each interrupt status bit also has its mask bit (0x3A) to disable the interrupt for that function. This sequence is described in Fig 20.

The TW280X also provides the video loss detection or motion detection flag of individual channel via NVMD pins. Four NVMD pins have respective channel information of motion or video loss so that host takes status information directly by reading these pins. Its mode is controlled by NVMD (0x3B) that is set “0” for video loss flag and “1” for motion detection flag.

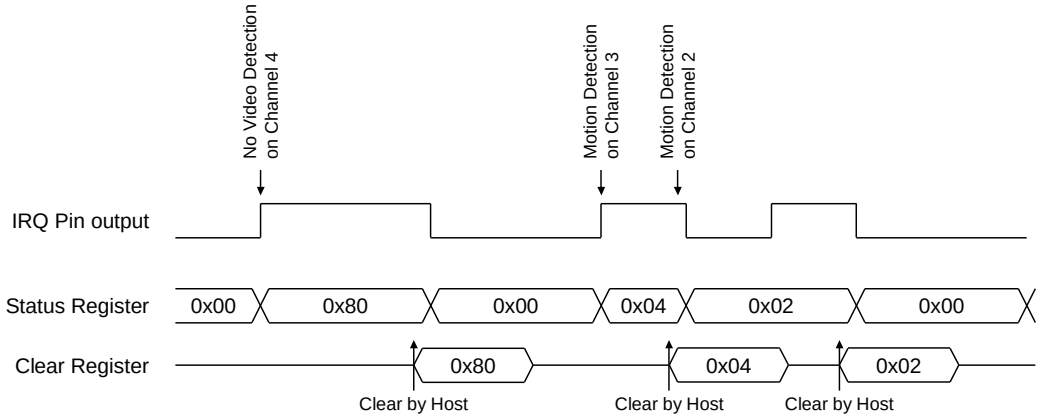


Fig 20 Timing Diagram of Interrupt Interface

Control Register

Register Map

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x00	0x40	0x80	0xC0	VIDSTAT *	DET_FORMAT			DET_COLOR	LOCK_COLOR	LOCK_GAIN	LOCK_OFFSET	LOCK_HPLL
0x01	0x41	0x81	0xC1	FORMAT	IFMTMAN	IFORMAT			0	1	DET_NONSTD *	DET_FLD60 *
0x02	0x42	0x82	0xC2	AGC_PLL	AGC	PEDEST	0		GNTIME		OSTIME	
0x03	0x43	0x83	0xC3	HDELAY_X	HDELAY_X [7:0]							
0x04	0x44	0x84	0xC4	HACTIVE_X	HACTIVE_X [7:0]							
0x05	0x45	0x85	0xC5	HDELAY_Y	HDELAY_Y [7:0]							
0x06	0x46	0x86	0xC6	HACTIVE_Y	HACTIVE_Y [7:0]							
0x07	0x47	0x87	0xC7	MSB_ACTV	HACTIVE_Y [9:8]		HDELAY_Y [9:8]		HACTIVE_X [9:8]		HDELAY_X [9:8]	
0x08	0x48	0x88	0xC8	HSWIDTH	0		HSWIDTH					
0x09	0x49	0x89	0xC9	VDELAY_X	VDELAY_X [7:0]							
0x0A	0x4A	0x8A	0xCA	VACTIVE_X	VACTIVE_X [7:0]							
0x0B	0x4B	0x8B	0xCB	VDELAY_Y	VDELAY_Y [7:0]							
0x0C	0x4C	0x8C	0xCC	VACTIVE_Y	VACTIVE_Y [7:0]							
0x0D	0x4D	0x8D	0xCD	HPLL	HPLLMAN	HPLLTIME			VACTVE_Y [8]	VDELAY_Y [8]	VACTVE_X [8]	VDELAY_X [8]
0x0E	0x4E	0x8E	0xCE	SYNCPOL	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0
0x0F	0x4F	0x8F	0xCF	HUE	HUE							
0x10	0x50	0x90	0xD0	SAT	SAT							
0x11	0x51	0x91	0xD1	CONT	CONT							
0x12	0x52	0x92	0xD2	BRT	BRT							
0x13	0x53	0x93	0xD3	CFILTER	IFCOMP		CLPF		ACCMODE		APCMODE	
0x14	0x54	0x94	0xD4	PEAKCKIL	YPEAK_Y		YPEAK_X		0		CKILL	
0x15	0x55	0x95	0xD5	SCLFLT	VLPF_Y		VLPF_X		HLPF_Y		HLPF_X	
0x16	0x56	0x96	0xD6	TRAP_X	YBWI_X	COMBMD_X		0				
0x17	0x57	0x97	0xD7	TRAP_Y	YBWI_Y	COMBMD_Y		0				
0x18	0x58	0x98	0xD8	VSCLMSB_X	VSCALE_X [15:8]							
0x19	0x59	0x99	0xD9	VSCLLSB_X	VSCALE_X [7:0]							
0x1A	0x5A	0x9A	0xDA	VSCLMSB_Y	VSCALE_Y [15:8]							
0x1B	0x5B	0x9B	0xDB	VSCLLSB_Y	VSCALE_Y [7:0]							
0x1C	0x5C	0x9C	0xDC	HSCLMSB_X	HSCALE_X [15:8]							
0x1D	0x5D	0x9D	0xDD	HSCLLSB_X	HSCALE_X [7:0]							
0x1E	0x5E	0x9E	0xDE	HSCLMSB_Y	HSCALE_Y [15:8]							
0x1F	0x5F	0x9F	0xDF	HSCLLSB_Y	HSCALE_Y [7:0]							
0x20	0x60	0xA0	0xE0	VSCLCON_X	0	VFLT_MD_X	VBW_X		PALDLY_X	ODD_EN_X	EVEN_EN_X	1
0x21	0x61	0xA1	0xE1	VSCLCON_Y	0	VFLT_MD_Y	VBW_Y		PALDLY_Y	ODD_EN_Y	EVEN_EN_Y	1
0x22	0x62	0xA2	0xE2	OUTFMT	BGND_EN	BGND_COLR	NOVID_656	LIM_16	SW_RESET	ANA_SW	OUT_FMT	
0x23	0x63	0xA3	0xE3	RESERVED	1	0	0	1	0	0	0	1
0x24	0x64	0xA4	0xE4	SENSCTL	LVLSENS				TMPSENS		SPTSENS	
0x25	0x65	0xA5	0xE5	MPERIOD	0			MDPERIOD				
0x26	0x66	0xA6	0xE6	MDMASK1	MDMASK1[7:0]							
0x27	0x67	0xA7	0xE7	MDMASK12	MDMASK2[11:8]				MDMASK1[11:8]			
0x28	0x68	0xA8	0xE8	MDMASK2	MDMASK2[7:0]							
0x29	0x69	0xA9	0xE9	MDMASK3	MDMASK3[7:0]							
0x2A	0x6A	0xAA	0xEA	MDMASK34	MDMASK4[11:8]				MDMASK3[11:8]			
0x2B	0x6B	0xAB	0xEB	MDMASK4	MDMASK4[7:0]							
0x2C	0x6C	0xAC	0xEC	MDMASK5	MDMASK5[7:0]							
0x2D	0x6D	0xAD	0xED	MDMASK56	MDMASK6[11:8]				MDMASK5[11:8]			

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x2E	0x6E	0xAE	0xEE	MDMASK6	MDMASK6[7:0]							
0x2F	0x6F	0xAF	0xEF	MDMASK7	MDMASK7[7:0]							
0x30	0x70	0xB0	0xF0	MDMASK78	MDMASK8[11:8]				MDMASK7[11:8]			
0x31	0x71	0xB1	0xF1	MDMASK8	MDMASK8[7:0]							
0x32	0x72	0xB2	0xF2	MDMASK9	MDMASK9[7:0]							
0x33	0x73	0xB3	0xF3	MDMASK9A	MDMASK10[11:8]				MDMASK9[11:8]			
0x34	0x74	0xB4	0xF4	MDMASKA	MDMASK10[7:0]							
0x35	0x75	0xB5	0xF5	MDMASKB	MDMASK11[7:0]							
0x36	0x76	0xB6	0xF6	MDMASKBC	MDMASK12[11:8]				MDMASK11[11:8]			
0x37	0x77	0xB7	0xF7	MDMASKC	MDMASK12[7:0]							
0x38				DET_NVMD *	DET_NOVID4	DET_NOVID3	DET_NOVID2	DET_NOVID1	DET_MOTION4	DET_MOTION3	DET_MOTION2	DET_MOTION1
0x39				IRQCLR	IRQCLR							
0x3A				IRQENA	IRQENA							
0x3B				MISC	OE	NVMD	ACTIVE_MODE		0	CK27_POL	IRQPOL	IRQRPT
0x3C				U_GAIN	U_GAIN							
0x3D				V_GAIN	V_GAIN							
0x3E				U_OFF	U_OFF							
0x3F				V_OFF	V_OFF							
0x78				ADC_PWDN	0	0	0	0	ADC_PWDN4	ADC_PWDN3	ADC_PWDN2	ADC_PWDN1
0x79				RESERVED	1	0	0	0	0	0	0	0
0x7A				RESERVED	0	0	0	0	0	0	0	0
0x7B				FLDOFST	FLD_OFST_4Y	FLD_OFST_4X	FLD_OFST_3Y	FLD_OFST_3X	FLD_OFST_2Y	FLD_OFST_2X	FLD_OFST_1Y	FLD_OFST_1X
0x7C				RESERVED	0	0	0	0	0	0	0	0
0x7D				RESERVED	0	0	0	0	0	0	0	0
0xB8				RESERVED	0	0	0	0	0	0	0	0
0xF8				CORE	HAV_VALID	0	0	0	C_CORE		Y_H_CORE	
0xF9				COMBCDEL	0	CDEL			0	FLD_656	1	0
0xFA				RESERVED	0	0	1	1	1	1	0	0
0xFB				RESERVED	0	0	0	1	0	0	0	0
0xFC				RESERVED	0	0	0	0	0	0	0	0
0xFD				RESERVED	0	0	0	0	0	0	0	0

Notes: ① * : Read only register

② : Modified in TW2804 RevC

③ : Modified in TW2804 RevD

Recommended Value

Address				Mnemonic	NTSC			PAL		
CH1	CH2	CH3	CH4		FULL	CIF	QCIF	FULL	CIF	QCIF
0x00	0x40	0x80	0xC0	VIDSTAT	8'h00			8'h00		
0x01	0x41	0x81	0xC1	FORMAT	C4			84		
0x02	0x42	0x82	0xC2	AGC_PLL	A5			A5		
0x03	0x43	0x83	0xC3	HDELAY_X	20			20		
0x04	0x44	0x84	0xC4	HACTIVE_X	D0			D0		
0x05	0x45	0x85	0xC5	HDELAY_Y	20			20		
0x06	0x46	0x86	0xC6	HACTIVE_Y	D0			D0		
0x07	0x47	0x87	0xC7	MSB_ACTV	88			88		
0x08	0x48	0x88	0xC8	HSWIDTH	20			20		
0x09	0x49	0x89	0xC9	VDELAY_X	07			04		
0x0A	0x4A	0x8A	0xCA	VACTIVE_X	F0			20		
0x0B	0x4B	0x8B	0xCB	VDELAY_Y	07			04		
0x0C	0x4C	0x8C	0xCC	VACTIVE_Y	F0			20		
0x0D	0x4D	0x8D	0xCD	HPLL	40			4A		
0x0E	0x4E	0x8E	0xCE	SYNCPOL	D2			D2		
0x0F	0x4F	0x8F	0xCF	HUE	80			80		
0x10	0x50	0x90	0xD0	SAT	80			80		
0x11	0x51	0x91	0xD1	CONT	80			80		
0x12	0x52	0x92	0xD2	BRT	80			80		
0x13	0x53	0x93	0xD3	CFILTER	2F			2F		
0x14	0x54	0x94	0xD4	PEAKCKIL	00	10		00	10	00
0x15	0x55	0x95	0xD5	SCLFLT	00	21	33	00	20	33
0x16	0x56	0x96	0xD6	TRAP_X	00			40	C0	
0x17	0x57	0x97	0xD7	TRAP_Y	00			40		
0x18	0x58	0x98	0xD8	VSCLMSB_X	FF	7F	3F	FF	7F	3F
0x19	0x59	0x99	0xD9	VSCLLSB_X	FF			FF		
0x1A	0x5A	0x9A	0xDA	VSCLMSB_Y	FF			FF		
0x1B	0x5B	0x9B	0xDB	VSCLLSB_Y	FF			FF		
0x1C	0x5C	0x9C	0xDC	HSCLMSB_X	FF	7F	3F	FF	7F	3F
0x1D	0x5D	0x9D	0xDD	HSCLLSB_X	FF			FF		
0x1E	0x5E	0x9E	0xDE	HSCLMSB_Y	FF			FF		
0x1F	0x5F	0x9F	0xDF	HSCLLSB_Y	FF			FF		
0x20	0x60	0xA0	0xE0	VSCLCON_X	07	07	67	0F	07	67
0x21	0x61	0xA1	0xE1	VSCLCON_Y	07			0F		
0x22	0x62	0xA2	0xE2	OUTFMT	00			00		
0x23	0x63	0xA3	0xE3	RESERVED	91			91		
0x24	0x64	0xA4	0xE4	SENSCTL	51			51		
0x25	0x65	0xA5	0xE5	MPERIOD	03			03		
0x26	0x66	0xA6	0xE6	MDMSKL1	00			00		
0x27	0x67	0xA7	0xE7	MDMSKM12	00			00		
0x28	0x68	0xA8	0xE8	MDMSKL2	00			00		
0x29	0x69	0xA9	0xE9	MDMSKL3	00			00		
0x2A	0x6A	0xAA	0xEA	MDMSKM34	00			00		
0x2B	0x6B	0xAB	0xEB	MDMSKL4	00			00		
0x2C	0x6C	0xAC	0xEC	MDMSKL5	00			00		
0x2D	0x6D	0xAD	0xED	MDMSKM56	00			00		
0x2E	0x6E	0xAE	0xEE	MDMSKL6	00			00		
0x2F	0x6F	0xAF	0xEF	MDMSKL7	00			00		
0x30	0x70	0xB0	0xF0	MDMSKM78	00			00		
0x31	0x71	0xB1	0xF1	MDMSKL8	00			00		
0x32	0x72	0xB2	0xF2	MDMSKL9	00			00		
0x33	0x73	0xB3	0xF3	MDMSKM9A	00			00		
0x34	0x74	0xB4	0xF4	MDMSKLA	00			00		
0x35	0x75	0xB5	0xF5	MDMSKLB	00			00		

Address				Mnemonic	NTSC			PAL		
CH1	CH2	CH3	CH4		FULL	CIF	QCIF	FULL	CIF	QCIF
0x36	0x76	0xB6	0xF6	MDMSKMBC	00			00		
0x37	0x77	0xB7	0xF7	MDMSKLC	00			00		
0x38				DET_NVMD	00			00		
0x39				IRQCLR	00			00		
0x3A				IRQENA	FF			FF		
0x3B				MISC	84			84		
0x3C				U_GAIN	80			80		
0x3D				V_GAIN	80			80		
0x3E				U_OFF	82			82		
0x3F				V_OFF	82			82		
0x78				ADC_PWDN	00			00		
0x79				RESERVED	80			80		
0x7A				RESERVED	00			00		
0x7B				FLDOFST	00			00		
0x7C				RESERVED	00			00		
0x7D				RESERVED	00			00		
0xB8				RESERVED	00			00		
0xF8				CORE	0A			0A		
0xF9				COMBCDEL	42			42		
0xFA				RESERVED	3C			3C		
0xFB				RESERVED	10			10		
0xFC				RESERVED	00			00		
0xFD				RESERVED	00			00		

Note : ① Blanks : Indicate the same value as full size

② : Modified in TW2804 RevC

③ : Modified in TW2804 RevD

Register Description

CH	Index	Video Status Flag *(Read only)*							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x00	DET_FORMAT			DET_COLOR	LOCK_COLOR	LOCK_GAIN	LOCK_OFST	LOCK_PLL
2	0x40								
3	0x80								
4	0xC0								

DET_FORMAT — Status of video standard detection
- 0 PAL-B/D
- 1 PAL-M
- 2 PAL-N
- 3 PAL-60
- 4 NTSC-M
- 5 NTSC-4.43
- 6 NTSC-N

DET_COLOR — Status of color detection
- 0 Color is not detected
- 1 Color is detected

LOCK_COLOR — Status of locking for color demodulation loop
- 0 Color demodulation loop is not locked
- 1 Color demodulation loop is locked

LOCK_GAIN — Status of locking for AGC loop
- 0 AGC loop is not locked
- 1 AGC loop is locked

LOCK_OFST — Status of locking for clamping loop
- 0 Claming loop is not locked
- 1 Claming loop is locked

LOCK_PLL — Status of locking for horizontal PLL
- 0 Horizontal PLL is not locked
- 1 Horizontal PLL is locked

CH	Index	Input Video Format							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x01	IFMTMAN	IFORMAT			0	1	DET_ NONSTD *	DET_ FLD60 *
2	0x41								
3	0x81								
4	0xC1								

Notes: * Read only register

IFMTMAN Setting video standard manually with IFORMAT
- 0 Detect video standard automatically according to incoming video signal (default)
- 1 Video standard is selected with IFORMAT

IFORMAT Force the device to operate in a particular video standard when IFMTMAN is high or to free-run in a particular video standard on no-video status when IFMTMAN is low
- 0 PAL-B/D (default)
- 1 PAL-M
- 2 PAL-N
- 3 PAL-60
- 4 NTSC-M
- 5 NTSC-4.43
- 6 NTSC-N

DET_NONSTD Status of non-standard video detection *(Read only)*
- 0 The incoming video source is standard
- 1 The incoming video source is non-standard

DET_FLD60 Status of field frequency of incoming video *(Read only)*
- 0 50Hz field frequency
- 1 60Hz field frequency

CH	Index	Gain and Offset Tracking							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x02	AGC	PEDEST	1	0	GNTIME		OSTIME	
2	0x42								
3	0x82								
4	0xC2								

AGC — Enable the AGC
- 0 Disable the AGC (default)
- 1 Enable the AGC

PEDEST — Enable gain correction for 7.5 IRE black (pedestal) level
- 0 No pedestal level (0 IRE is ITU-R BT.656 code 16) (default)
- 1 7.5 IRE setup level (7.5 IRE is ITU-R BT.656 code 16)

GNTIME — Control the time constant of gain tracking loop
- 0 Slower
- 1 Slow (default)
- 2 Fast
- 3 Faster

OSTIME — Control the time constant of offset tracking loop
- 0 Slower
- 1 Slow (default)
- 2 Fast
- 3 Faster

CH	Index	Horizontal Delay Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x07							HDELAY[9:8]	
	0x03	HDELAY[7:0]							
2	0x47							HDELAY[9:8]	
	0x43	HDELAY[7:0]							
3	0x87							HDELAY[9:8]	
	0x83	HDELAY[7:0]							
4	0xC7							HDELAY[9:8]	
	0xC3	HDELAY[7:0]							

CH	Index	Horizontal Delay Control for Path Y							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x07			HDELAY[9:8]					
	0x05	HDELAY[7:0]							
2	0x47			HDELAY[9:8]					
	0x45	HDELAY[7:0]							
3	0x87			HDELAY[9:8]					
	0x85	HDELAY[7:0]							
4	0xC7			HDELAY[9:8]					
	0xC5	HDELAY[7:0]							

HDELAY — This 10-bit register defines the starting location of horizontal active pixel. A unit is 1 pixel. HDELAY1 and HDELAY2 define the different starting location of horizontal active pixel for dual scaler output. The default value is decimal 32.

CH	Index	Horizontal Active Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x07					HACITIVE[9:8]			
	0x04	HACTIVE[7:0]							
2	0x47					HACITIVE[9:8]			
	0x44	HACTIVE[7:0]							
3	0x87					HACITIVE[9:8]			
	0x84	HACTIVE[7:0]							
4	0xC7					HACITIVE[9:8]			
	0xC4	HACTIVE[7:0]							

CH	Index	Horizontal Active Control for Path Y							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x07	HACTIVE[9:8]							
	0x06	HACTIVE[7:0]							
2	0x47	HACTIVE[9:8]							
	0x46	HACTIVE[7:0]							
3	0x87	HACTIVE[9:8]							
	0x86	HACTIVE[7:0]							
4	0xC7	HACTIVE[9:8]							
	0xC6	HACTIVE[7:0]							

HACTIVE — This 10-bit register defines the number of horizontal active pixel. A unit is 1 pixel. HACTIVE1 and HACTIVE2 define the different number of horizontal active pixels for dual scaler output. The default value is decimal 720.

CH	Index	Horizontal Sync Pulse Width Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x08	0	0	HSWIDTH					
2	0x48								
3	0x88								
4	0xC8								

HSWIDTH — This 6-bit register defines the width of horizontal sync output. A unit is 1 pixel. The default value is decimal 32

CH	Index	Vertical Delay Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0D								VDELAY[8]
	0x09	VDELAY[7:0]							
2	0x4D								VDELAY[8]
	0x49	VDELAY[7:0]							
3	0x8D								VDELAY[8]
	0x89	VDELAY[7:0]							
4	0xCD								VDELAY[8]
	0xC9	VDELAY[7:0]							

CH	Index	Vertical Delay Control for Path Y							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0D						VDELAY[8]		
	0x0B	VDELAY[7:0]							
2	0x4D						VDELAY[8]		
	0x4B	VDELAY[7:0]							
3	0x8D						VDELAY[8]		
	0x8B	VDELAY[7:0]							
4	0xCD						VDELAY[8]		
	0xCB	VDELAY[7:0]							

VDELAY — This 9-bit register defines the starting location of vertical active. A unit is 1 line. VDELAY1 and VDELAY2 define the different starting location of vertical active line for dual scaler output. The default value is decimal 6.

CH	Index	Vertical Active Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0D							VACTIVE[8]	
	0x0A	VACTIVE[7:0]							
2	0x4D							VACTIVE[8]	
	0x4A	VACTIVE[7:0]							
3	0x8D							VACTIVE[8]	
	0x8A	VACTIVE[7:0]							
4	0xCD							VACTIVE[8]	
	0xCA	VACTIVE[7:0]							

CH	Index	Vertical Active Control for Path Y							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0D					VACTIVE[8]			
	0x0C	VACTIVE[7:0]							
2	0x4D					VACTIVE[8]			
	0x4C	VACTIVE[7:0]							
3	0x8D					VACTIVE[8]			
	0x8C	VACTIVE[7:0]							
4	0xCD					VACTIVE[8]			
	0xCC	VACTIVE[7:0]							

VACTIVE — This 9-bit register defines the number of vertical active lines. A unit is 1 line. VACTIVE1 and VACTIVE2 define the different number of vertical active lines for dual scaler output. The default value is decimal 240.

CH	Index	Horizontal PLL Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0D	HPLLMAN	HPLLTIME						
2	0x4D								
3	0x8D								
4	0xCD								

HPLLMAN Set horizontal PLL time constant with HPLLTIME.
0 Automatic horizontal tracking mode (default)
1 Horizontal PLL time constant is fixed with HPLLTIME

HPLLTIME Control the time constant of horizontal PLL when HPLLMAN is high
0 Slow
: :
4 Typical (default)
: :
7 Fast

CH	Index	Sync Pulse Polarity Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0E	FLDMODE		VSMODE	FLDPOL	HSPOL	VSPOL	1	0
2	0x4E								
3	0x8E								
4	0xCE								

FLDMODE Select the field flag generation mode
0 Field flag is detected from incoming video (default)
1 Field flag is generated from small accumulator of detected field
2 Field flag is generated from medium accumulator of detected field
3 Field flag is generated from large accumulator of detected field

VSMODE Control the VS and field flag timing
0 VS and field flag is aligned with vertical sync of incoming video (default)
1 VS and field flag is aligned with HS

FLDPOL Select the FLD polarity
0 Odd field is high (default)
1 Even field is high

HSPOL Select the HS polarity
0 Low for sync duration (default)
1 High for sync duration

VSPOL Select the VS polarity
0 Low for sync duration (default)
1 High for sync duration

CH	Index	Hue Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x0F	HUE							
2	0x4F								
3	0x8F								
4	0xCF								

HUE Control the hue information. The resolution is 1.4° / LSB.

0	-180°
:	:
128	0° (default)
:	:
255	180°

CH	Index	Saturation Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x10	SAT							
2	0x50								
3	0x90								
4	0xD0								

SAT Control the color saturation. The resolution is 0.8% / LSB.

0	0 %
:	:
128	100 % (default)
:	:
255	200 %

CH	Index	Contrast Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x11	CONT							
2	0x51								
3	0x91								
4	0xD1								

CONT Control the contrast. The resolution is 0.8% / LSB.
0 0 %
: :
128 100 % (default)
: :
255 200 %

CH	Index	Brightness Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x12	BRT							
2	0x52								
3	0x92								
4	0xD2								

BRT Control the brightness. The resolution is 0.2IRE / LSB.
0 -25 IRE
: :
128 0 (default)
: :
255 25 IRE

CH	Index	Color Filter Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x13	IFCOMP		CLPF		ACCMODE		APCMODE	
2	0x53								
3	0x93								
4	0xD3								

IFCOMP — Select the IF-compensation filter mode
- 0 No compensation (default)
- 1 +1 dB/ MHz
- 2 +2 dB/ MHz
- 3 +3 dB/ MHz

CLPF — Select the Color LPF mode
- 0 550KHz bandwidth
- 1 750KHz bandwidth (default)
- 2 950KHz bandwidth
- 3 1.1MHz bandwidth

ACCMODE — Control the time constant of auto color control loop
- 0 Slower
- 1 Slow
- 2 Fast
- 3 Faster (default)

APCMODE — Control the time constant of auto phase control loop
- 0 Slower
- 1 Slow
- 2 Fast
- 3 Faster (default)

CH	Index	Peaking and Color Killer Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x14	YPEAK_Y		YPEAK_X		0	0	CKIL	
2	0x54								
3	0x94								
4	0xD4								

YPEAK_Y Control the luminance peaking for SCALER Y path
0 No peaking (default)
1 31.25%
2 62.5%
3 93.75%

YPEAK_X Control the luminance peaking for SCALER X path
0 No peaking (default)
1 31.25%
2 62.5%
3 93.75%

CKIL Control the color killing mode
0,1 Auto detection mode (default)
2 Color is always alive
3 Color is always killed

CH	Index	Scaler Filter Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x15	VLPF_Y		VLPF_X		SCLFLT_Y		SCLFLT_X	
2	0x55								
3	0x95								
4	0xD5								

VLPF_Y Select the vertical anti-aliasing filter mode for VSCALER Y
0,1 Full bandwidth (default)
2 0.25 Line-rate bandwidth
3 0.18 Line-rate bandwidth

VLPF_X Select the vertical anti-aliasing filter mode for VSCALER X
0,1 Full bandwidth (default)
2 0.25 Line-rate bandwidth
3 0.18 Line-rate bandwidth

SCLFLT_Y Select the horizontal anti-aliasing filter mode for HSCALER Y
0 Full bandwidth (default)
1 2 MHz bandwidth
2 1.5 MHz bandwidth
3 1 MHz bandwidth

SCLFLT_X Select the horizontal anti-aliasing filter mode for HSCALER X
0 Full bandwidth (default)
1 2 MHz bandwidth
2 1.5 MHz bandwidth
3 1 MHz bandwidth

CH	Index	Trap Filter Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x16	YBWI	COMBMD		0	0	0	0	0
2	0x56								
3	0x96								
4	0xD6								

CH	Index	Trap Filter Control for Path Y							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x17	YBWI	COMBMD		0	0	0	0	0
2	0x57								
3	0x97								
4	0xD7								

YBWI — Select the luminance trap filter mode
- 0 Narrow bandwidth trap filter mode (default)
- 1 Wide bandwidth trap filter mode

COMBMD — Select the adaptive comb filter mode
- 0,1 Adaptive comb filter mode (default)
- 2 Force trap filter mode
- 3 Not supported

CH	Index	Vertical Scaler Ratio Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x18	VSCALE[15:8]							
	0x19	VSCALE[7:0]							
2	0x58	VSCALE[15:8]							
	0x59	VSCALE[7:0]							
3	0x98	VSCALE[15:8]							
	0x99	VSCALE[7:0]							
4	0xD8	VSCALE[15:8]							
	0xD9	VSCALE[7:0]							

CH	Index	Vertical Scaler Ratio Control for Path Y							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x1A	VSCALE[15:8]							
	0x1B	VSCALE[7:0]							
2	0x5A	VSCALE[15:8]							
	0x5B	VSCALE[7:0]							
3	0x9A	VSCALE[15:8]							
	0x9B	VSCALE[7:0]							
4	0xDA	VSCALE[15:8]							
	0xDB	VSCALE[7:0]							

VSCALE — The 16-bit register defines a vertical scaling ratio. The actual vertical scaling ratio is VSCALE[15:0] / (2^16 – 1). VSCALE1 and VSCALE2 define the different vertical scaling ratio for dual scaler. The default value is 16 bit 0xFFFF.

CH	Index	Horizontal Scaler Ratio Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x1C	HSCALE[15:8]							
	0x1D	HSCALE[7:0]							
2	0x5C	HSCALE[15:8]							
	0x5D	HSCALE[7:0]							
3	0x9C	HSCALE[15:8]							
	0x9D	HSCALE[7:0]							
4	0xDC	HSCALE[15:8]							
	0xDD	HSCALE[7:0]							

CH	Index	Horizontal Scaler Ratio Control for Path Y							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x1E	HSCALE[15:8]							
	0x1F	HSCALE[7:0]							
2	0x5E	HSCALE[15:8]							
	0x5F	HSCALE[7:0]							
3	0x9E	HSCALE[15:8]							
	0x9F	HSCALE[7:0]							
4	0xDE	HSCALE[15:8]							
	0xDF	HSCALE[7:0]							

HSCALE — The 16-bit register defines a horizontal scaling ratio. The actual horizontal scaling ratio is HSCALE[15:0] / (2^16 – 1). HSCALE1 and HSCALE2 define the different horizontal scaling ratio for dual scaler. The default value is 16 bit 0xFFFF.

CH	Index	Vertical Scaler Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x20	0	VFLT_MD	VBW		PALDLY	ODD_EN	EVEN_EN	1
2	0x60								
3	0xA0								
4	0xE0								

CH	Index	Vertical Scaler Control for Path X							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x21	0	VFLT_MD	VBW		PALDLY	ODD_EN	EVEN_EN	1
2	0x61								
3	0xA1								
4	0xE1								

VFLT_MD — Select the vertical scaling filter mode
- 0 Vertical poly-phase filter mode is selected (default)
- 1 Vertical bandwidth control mode is selected with VBW bits

VBW — Control the vertical bandwidth only if VFLT_MD bit is high
- 0,1 Not supported (default)
- 2 Wide
- 3 Narrow

PAL_DLY — Select the PAL delay line mode
- 0 Normal vertical scaling operation in chroma path (default)
- 1 PAL delay line mode is selected in chroma path

ODD_EN — Control valid signal in ODD field
- 0 Valid signal is always disabled in ODD field
- 1 Normal operation (default)

EVEN_EN — Control valid signal in EVEN field
- 0 Valid signal is always disabled in EVEN field
- 1 Normal operation (default)

CH	Index	Output Formatter							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x22	BGNDEN	BGNDCLR	NOVID_656	LIM_16	SW_ RESET	ANA_SW	OUT_FMT	
2	0x62								
3	0xA2								
4	0xE2								

BGNDEN — Control the background color on/off
- 0 Background color is disabled (default)
- 1 Background color is enabled

BGNDCLR — Select the background color mode only if BGNDEN bit is high
- 0 Blue color mode (default)
- 1 Black color mode

NOVID_656 — Select the optional set of 656 SAV/EAV code sequence for no-video status
- 0 Normal 656 SAV/EAV code sequence (default)
- 1 An optional set of 656 SAV/EAV code sequence for no-video status

LIM_16 — Control the output range
- 0 Output ranges are limited to 2 ~ 254 (default)
- 1 Output ranges are limited to 16 ~ 239

SW_RESET — Reset the system by software except control registers.
This bit is self-clearing in a few clocks after enabled
- 0 Normal operation (default)
- 1 Enable soft reset

ANA_SW — Control the analog input channel switch
- 0 VIN_A channel is selected (default)
- 1 VIN_B channel is selected

OUT_FMT — Select the output format
- 0 ITU-R BT.656 format (default)
- 1 8-bit ITU-R BT.601 format
- 2 Dual ITU-R BT.656 with 54MHz format
- 3 Not supported

CH	Index	Reserved							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x23	1	0	0	1	0	0	0	1
2	0x63								
3	0xA3								
4	0xE3								

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

CH	Index	Motion Detection Sensitivity							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x24	LVLSENS				TMPSENS		SPTSENS	
2	0x64								
3	0xA4								
4	0xE4								

LVLSENS Control the level sensitivity of motion detector (default : 3)
0 More sensitive
: :
15 Less sensitive

TMPSENS Control the temporal sensitivity of motion detector (default : 1)
0 More sensitive
: :
3 Less sensitive

SPTSENS Control the spatial sensitivity of motion detector (default : 1)
0 More sensitive
: :
3 Less sensitive

CH	Index	Motion Detection Control							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x25	0			MDPERIOD				
2	0x65								
3	0xA5								
4	0xE5								

MDPERIOD Control the velocity of motion detector (default : 3)
0 No field interval
1 1 field interval
: :
31 31 field interval

CH	Index	Masking Motion Detection Area MASK1							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x27					MDMASK1[11:8]			
	0x26	MDMASK1[7:0]							
2	0x67					MDMASK1[11:8]			
	0x66	MDMASK1[7:0]							
3	0xA7					MDMASK1[11:8]			
	0xA6	MDMASK1[7:0]							
4	0xE7					MDMASK1[11:8]			
	0xE6	MDMASK1[7:0]							

CH	Index	Masking Motion Detection Area MASK2							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x27	MDMASK2[11:8]							
	0x28	MDMASK2[7:0]							
2	0x67	MDMASK2[11:8]							
	0x68	MDMASK2[7:0]							
3	0xA7	MDMASK2[11:8]							
	0xA8	MDMASK2[7:0]							
4	0xE7	MDMASK2[11:8]							
	0xE8	MDMASK2[7:0]							

CH	Index	Masking Motion Detection Area MASK3							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x2A					MDMASK3[11:8]			
	0x29	MDMASK3[7:0]							
2	0x6A					MDMASK3[11:8]			
	0x69	MDMASK3[7:0]							
3	0xAA					MDMASK3[11:8]			
	0xA9	MDMASK3[7:0]							
4	0xEA					MDMASK3[11:8]			
	0xE9	MDMASK3[7:0]							

CH	Index	Masking Motion Detection Area MASK4							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x2A	MDMASK4[11:8]							
	0x2B	MDMASK4[7:0]							
2	0x6A	MDMASK4[11:8]							
	0x6B	MDMASK4[7:0]							
3	0xAA	MDMASK4[11:8]							
	0xAB	MDMASK4[7:0]							
4	0xEA	MDMASK4[11:8]							
	0xEB	MDMASK4[7:0]							

CH	Index	Masking Motion Detection Area MASK5							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x2D					MDMASK5[11:8]			
	0x2C	MDMASK5[7:0]							
2	0x6D					MDMASK5[11:8]			
	0x6C	MDMASK5[7:0]							
3	0xAD					MDMASK5[11:8]			
	0xAC	MDMASK5[7:0]							
4	0xED					MDMASK5[11:8]			
	0xEC	MDMASK5[7:0]							

CH	Index	Masking Motion Detection Area MASK6							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x2D	MDMASK6[11:8]							
	0x2E	MDMASK6[7:0]							
2	0x6D	MDMASK6[11:8]							
	0x6E	MDMASK6[7:0]							
3	0xAD	MDMASK6[11:8]							
	0xAE	MDMASK6[7:0]							
4	0xED	MDMASK6[11:8]							
	0xEE	MDMASK6[7:0]							

CH	Index	Masking Motion Detection Area MASK7							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x30					MDMASK7[11:8]			
	0x2F	MDMASK7[7:0]							
2	0x70					MDMASK7[11:8]			
	0x6F	MDMASK7[7:0]							
3	0xB0					MDMASK7[11:8]			
	0xAF	MDMASK7[7:0]							
4	0xF0					MDMASK7[11:8]			
	0xEF	MDMASK7[7:0]							

CH	Index	Masking Motion Detection Area MASK8							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x30	MDMASK8[11:8]							
	0x31	MDMASK8[7:0]							
2	0x70	MDMASK8[11:8]							
	0x71	MDMASK8[7:0]							
3	0xB0	MDMASK8[11:8]							
	0xB1	MDMASK8[7:0]							
4	0xF0	MDMASK8[11:8]							
	0xF1	MDMASK8[7:0]							

CH	Index	Masking Motion Detection Area MASK9							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x33					MDMASK9[11:8]			
	0x32	MDMASK9[7:0]							
2	0x73					MDMASK9[11:8]			
	0x72	MDMASK9[7:0]							
3	0xB3					MDMASK9[11:8]			
	0xB2	MDMASK9[7:0]							
4	0xF3					MDMASK9[11:8]			
	0xF2	MDMASK9[7:0]							

CH	Index	Masking Motion Detection Area MASK10							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x33	MDMASK10[11:8]							
	0x34	MDMASK10[7:0]							
2	0x73	MDMASK10[11:8]							
	0x74	MDMASK10[7:0]							
3	0xB3	MDMASK10[11:8]							
	0xB4	MDMASK10[7:0]							
4	0xF3	MDMASK10[11:8]							
	0xF4	MDMASK10[7:0]							

CH	Index	Masking Motion Detection Area MASK11							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x36					MDMASK11[11:8]			
	0x35	MDMASK11[7:0]							
2	0x76					MDMASK11[11:8]			
	0x75	MDMASK11[7:0]							
3	0xB6					MDMASK11[11:8]			
	0xB5	MDMASK11[7:0]							
4	0xF6					MDMASK11[11:8]			
	0xF5	MDMASK11[7:0]							

CH	Index	Masking Motion Detection Area MASK12							
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0x36	MDMASK12[11:8]							
	0x37	MDMASK12[7:0]							
2	0x76	MDMASK12[11:8]							
	0x77	MDMASK12[7:0]							
3	0xB6	MDMASK12[11:8]							
	0xB7	MDMASK12[7:0]							
4	0xF6	MDMASK12[11:8]							
	0xF7	MDMASK12[7:0]							

MDMASK1~12 Select mask area of motion detector. An active region is divided into 12x12 mask areas as illustrated in Fig. 11. If the mask bit in specific area is programmed into high, the specific area is ignored in operation of motion detector. But for proper operation, more than 4 mask areas should be enabled in any case. (default : 0x00)

Index	No video and Motion Detection Flag *(Read only)*							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x38	DET_ NOVID4	DET_ NOVID3	DET_ NOVID2	DET_ NOVID1	DET_ MOTION4	DET_ MOTION3	DET_ MOTION2	DET_ MOTION1

DET_NOVID4 Status for detection of video loss in Channel 4
0 Video is alive
1 Video loss is detected

DET_NOVID3 Status for detection of video loss in Channel 3
0 Video is alive
1 Video loss is detected

DET_NOVID2 Status for detection of video loss in Channel 2
0 Video is alive
1 Video loss is detected

DET_NOVID1 Status for detection of video loss in Channel 1
0 Video is alive
1 Video loss is detected

DET_MOTION4 Status for detection of motion in Channel 4
0 No motion
1 Motion is detected

DET_MOTION3 Status for detection of Motion in Channel 3
0 No motion
1 Motion is detected

DET_MOTION2 Status for detection of Motion in Channel 2
0 No motion
1 Motion is detected

DET_MOTION1 Status for detection of Motion in Channel 1
0 No motion
1 Motion is detected

Index	Clear Interrupt Flag							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x39	CLEAR_ NOVID4	CLEAR_ NOVID3	CLEAR_ NOVID2	CLEAR_ NOVID1	CLEAR_ MOTION4	CLEAR_ MOTION3	CLEAR_ MOTION2	CLEAR_ MOTION1

IRQCLR Setting high to bits clears interrupt requests of corresponding bits. This bit is self-clearing in a few clocks after setting high (default : 0x00)

Index	Enable Interrupt Flag							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3A	EN_ NOVID4	EN _ NOVID3	EN_ NOVID2	EN _ NOVID1	EN _ MOTION4	EN_ MOTION3	EN_ MOTION2	EN_ MOTION1

IRQENA Enable the corresponding (0x38, 0x39) interrupt register bit (default : 0x00)

Index	Miscellaneous Control Register							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3B	OE	NVMD	ACTIVE_MODE[1:0]		0	CK27_POL	IRQPOL	IRQRPT

OE — Control the tri-state of output pin
- 0 Outputs are Tri-state (default)
- 1 Outputs are enabled

NVMD — Select the output mode of NVMD pin
- 0 Video loss flag (default)
- 1 Motion detection flag

ACTIVE_MODE — Select the output mode of ACTIVE pin
- 0 HACTIVE (default)
- 1 VACTIVE
- 2 Horizontal valid pixel indicator
- 3 Vertical valid line indicator

CK27_POL — Select the CLK27O polarity
- 0 ITU-R BT.656 data outputs at the rising edge of CLK27O (default)
- 1 ITU-R BT.656 data outputs at the falling edge of CLK27O

IRQPOL — Select the IRQ polarity
- 0 Active high (default)
- 1 Active low

IRQRPT — Select the IRQ mode
- 0 IRQ maintains the state until the interrupt request is cleared (default)
- 1 IRQ toggles the state at regular intervals until the interrupt request is cleared

Index	U Gain							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3C	U_GAIN[7:0]							

U_GAIN Adjust gain for U (or Cb) component. The resolution is 0.8% / LSB.

0	0 %
:	:
128	100 % (default)
:	:
255	200 %

Index	V Gain							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3D	V_GAIN[7:0]							

V_GAIN Adjust gain for V (or Cr) component. The resolution is 0.8% / LSB.

0	0 %
:	:
128	100 % (default)
:	:
255	200 %

Index	U Offset							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3E	U_OFF[7:0]							

U_OFF U (or Cb) offset adjustment register. The resolution is 0.4% / LSB.

0	-50 %
:	:
128	0 % (default)
:	:
255	50 %

Index	V Offset							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3F	V_OFF[7:0]							

V_OFF V (or Cr) offset adjustment register. The resolution is 0.4% / LSB.

0	-50 %
:	:
128	0 % (default)
:	:
255	50 %

Index	ADC Power Down							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x78	0	0	0	0	ADC_ PWDN4	ADC_ PWDN3	ADC_ PWDN2	ADC_ PWDN1

ADC_PWDN4 Power down the ADC of Channel 4
0 Normal (default)
1 Power down

ADC_PWDN3 Power down the ADC of Channel 3
0 Normal (default)
1 Power down

ADC_PWDN2 Power down the ADC of Channel 2
0 Normal (default)
1 Power down

ADC_PWDN1 Power down the ADC of Channel 1
0 Normal (default)
1 Power down

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x79	1	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7A	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Field Offset Control							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7B	FLD_OFST_4Y	FLD_OFST_4X	FLD_OFST_3Y	FLD_OFST_3X	FLD_OFST_2Y	FLD_OFST_2X	FLD_OFST_1Y	FLD_OFST_1X

FLD_OFST_4Y Remove the field offset between ODD and EVEN for Y path of Channel 4
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

FLD_OFST_4X Remove the field offset between ODD and EVEN for X path of Channel 4
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

FLD_OFST_3Y Remove the field offset between ODD and EVEN for Y path of Channel 3
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

FLD_OFST_3X Remove the field offset between ODD and EVEN for X path of Channel 3
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

FLD_OFST_2Y Remove the field offset between ODD and EVEN for Y path of Channel 2
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

FLD_OFST_2X Remove the field offset between ODD and EVEN for X path of Channel 2
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

FLD_OFST_1Y Remove the field offset between ODD and EVEN for Y path of Channel 1
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

FLD_OFST_1X Remove the field offset between ODD and EVEN for X path of Channel 1
0 Normal operation (default)
1 Remove the field offset between ODD and EVEN field

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7C	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x7D	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB8	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Luma and Chroma Coring							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF8	HAV_VALID	0	0	0	C_CORE[1:0]		Y_H_CORE[1:0]	

HAV_VALID — Select VALID output mode
- 0 Valid data indicator only for active data (default)
- 1 Valid data indicator for both active data and ITU-R 656 timing codes

C_CORE — Coring to reduce the noise in the chrominance
- 0 No coring
- 1 Coring value is within 128 +/- 1 range
- 2 Coring value is within 128 +/- 2 range (default)
- 3 Coring value is within 128 +/- 4 range

Y_H_CORE — Coring to reduce the high frequency noise in the luminance
- 0 No coring
- 1 Coring value is within +/- 1 range
- 2 Coring value is within +/- 2 range (default)
- 3 Coring value is within +/- 4 range

Index	Chroma Delay and Comb Filter Correlation Reference							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xF9	0	CDEL[2:0]			0	FLD_656	1	0

CDEL — Adjust the group delay of chrominance path relative to luminance
0 -2.0 pixel
1 -1.5 pixel
2 -1.0 pixel
3 -0.5 pixel
4 0.0 pixel (default)
5 0.5 pixel
6 1.0 pixel
7 1.5 pixel

FLD_656 — Control the field polarity mode in ITU-R 656 timing codes
0 Fixed field polarity according to ITU-R 656 format (default)
1 Controllable field polarity by FLDPOL register (0x0E,0x4E,0x8E,0xCE)

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFA	0	0	1	1	1	1	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFB	0	0	0	1	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFC	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Index	Reserved							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFD	0	0	0	0	0	0	0	0

This control register is reserved for putting the part into test mode. For normal operation, the above value should be set in this register.

Parametric Information

DC Electrical Parameters

Table 7 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VDDA (measured to VSSA)	VDD_{AM}			3.5	V
VDD (measured to VSS)	VDD_{IM}			3.5	V
VDDO (measured to VSS)	VDD_{OM}			4.6	V
Voltage on any signal pin (See the note below)	-	VSS–0.5		6.0	V
Analog Input Voltage	-	VDD_{AM}–0.5		VDD_{AM}+0.5	V
Storage Temperature	T_S	– 65		150	° C
Junction Temperature	T_J	0		125	° C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}			220	° C

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition.

Table 8 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
VDDA (measured to VSSA)	VDD_A	2.25	2.5	2.75	V
VDD (measured to VSS)	VDD_I	2.25	2.5	2.75	V
VDDO (measured to VSS)	VDD_O	3.0	3.3	3.6	V
Maximum $\|VDD_I – VDD_A\|$				0.3	V
Maximum $\|VDD_O – VDD_A\|$				1.05	V
Maximum $\|VDD_O – VDD_I\|$				1.05	V
Analog VIN Amplitude Range (AC coupling required)		0.5	1.0	2.0	V
Ambient Operating Temperature	T_A	0		85	° C

NOTE: Power On/Off sequence should keep the following rule.

- Apply power to VDD, VDDA and VDDO at the same time
- If it is difficult to apply the power to these pins at the same time, apply the power to VDDO first and to VDD/VDDA later.
- Cut the power of VDD, VDDA and VDDO at the same time
- If it is difficult to cut the power of these pins at the same time, cut the power of VDD/VDDA first and of VDDO later.

Table 9 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0		5.5	V
Input Low Voltage (TTL)	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I=2.5V or 0V)	I_L			±1	uA
Input Capacitance	C_{IN}		6		pF
Digital Outputs					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current (@V_{OH}=2.4V)	I_{OH}	5.7	11.6	18.6	mA
Low Level Output Current (@V_{OL}=0.4V)	I_{OL}	4.1	6.7	8.2	mA
Tri-state Output Leakage Current (@V_O=2.5V or 0V)	I_{OZ}			±1	uA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF

Table 10 Supply Current and Power Dissipation

Parameter	Symbol	Min	Typ	Max	Units
Analog Supply Current (2.5V)	I_{DDA}		50	55	mA
Digital Internal Supply Current (2.5V)	I_{DDI}		400	440	mA
Digital I/O Supply Current (3.3V)	I_{DDO}		10	11	mA
Total Power Dissipation	P		1.16	1.27	W

AC Electrical Parameters

Table 11 Clock and Data Timing

Parameter	Symbol	Min	Typ	Max	Units
Delay from CLK54I to CLK27O	1	5		12	ns
Hold from CLK27O to Data	2a	16			ns
Delay from CLK27O to Data	2b			19	ns
Hold from CLK54I to Data	3a	5			ns
Delay from CLK54I to Data	3b			12	ns

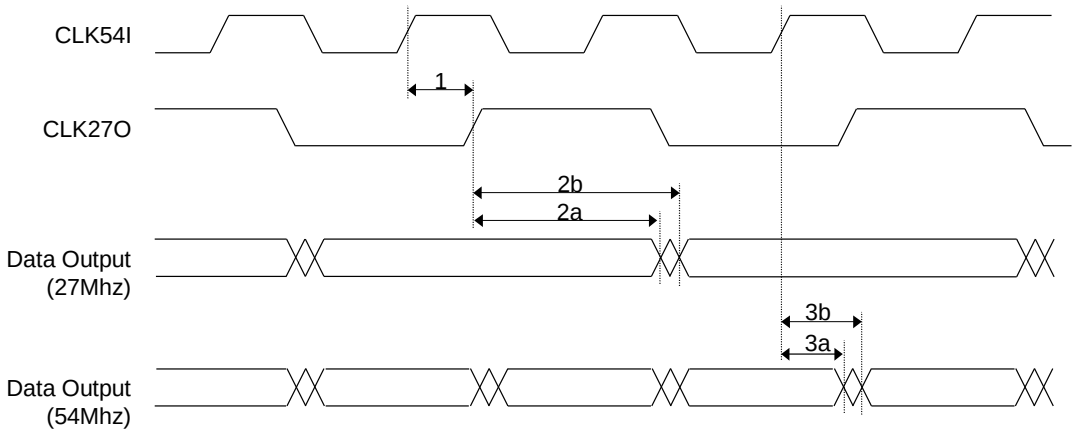


Fig 21 Clock and Data Timing Diagram

Table 12. Serial Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time between STOP and START	t_{BF}	1.3			us
SDAT setup time	t_{sSDAT}	100			ns
SDAT hold time	t_{hSDAT}	0		0.9	us
Setup time for START condition	t_{sSTA}	0.6			us
Setup time for STOP condition	t_{sSTOP}	0.6			us
Hold time for START condition	t_{hSTA}	0.6			us
Rise time for SCLK and SDAT	t_R			300	ns
Fall time for SCLK and SDAT	t_F			300	ns
Capacitive load for each bus line	C_{BUS}			400	pF
SCLK clock frequency	f_{SCLK}			400	KHz

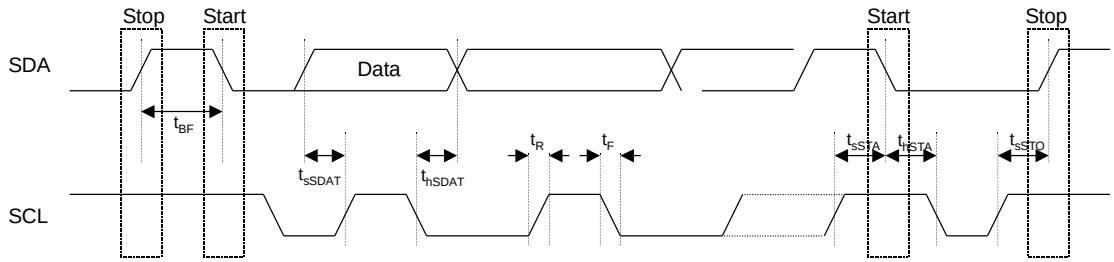


Fig 22. Serial Interface Timing Diagram

Table 13. Parallel Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
CSB setup until AEN active	$t_{su\ (1)}$	10			ns
PDATA setup until AEN, WENB active	$t_{su\ (2)}$	10			ns
AEN, WENB, RENB active pulse width	t_w	40			ns
CSB hold after WENB, RENB inactive	$t_{h\ (1)}$	60			ns
PDATA hold after AEN, WENB inactive	$t_{h\ (2)}$	60			ns
PDATA delay after RENB active	$t_{d\ (1)}$			12	ns
PDATA delay after RENB inactive	$t_{d\ (2)}$			12	ns

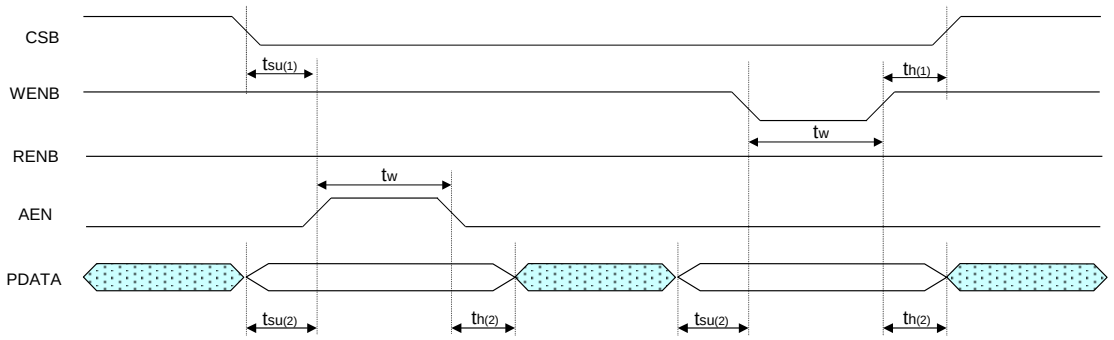


Fig 23. Write Timing Diagram in Parallel Interface

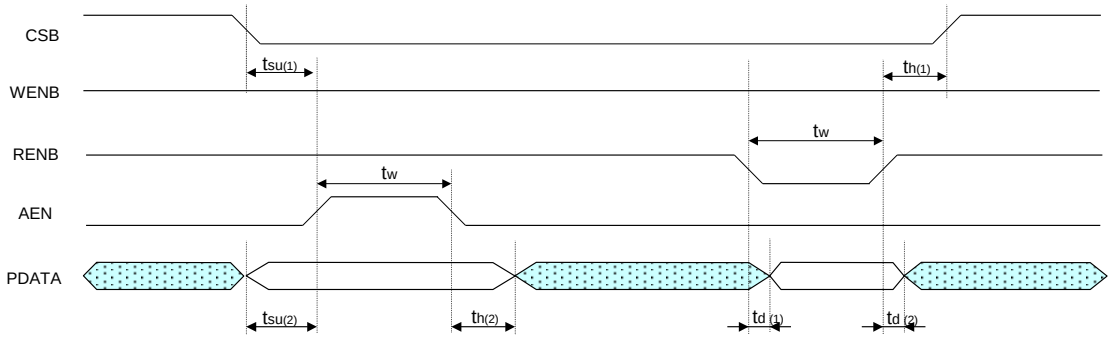
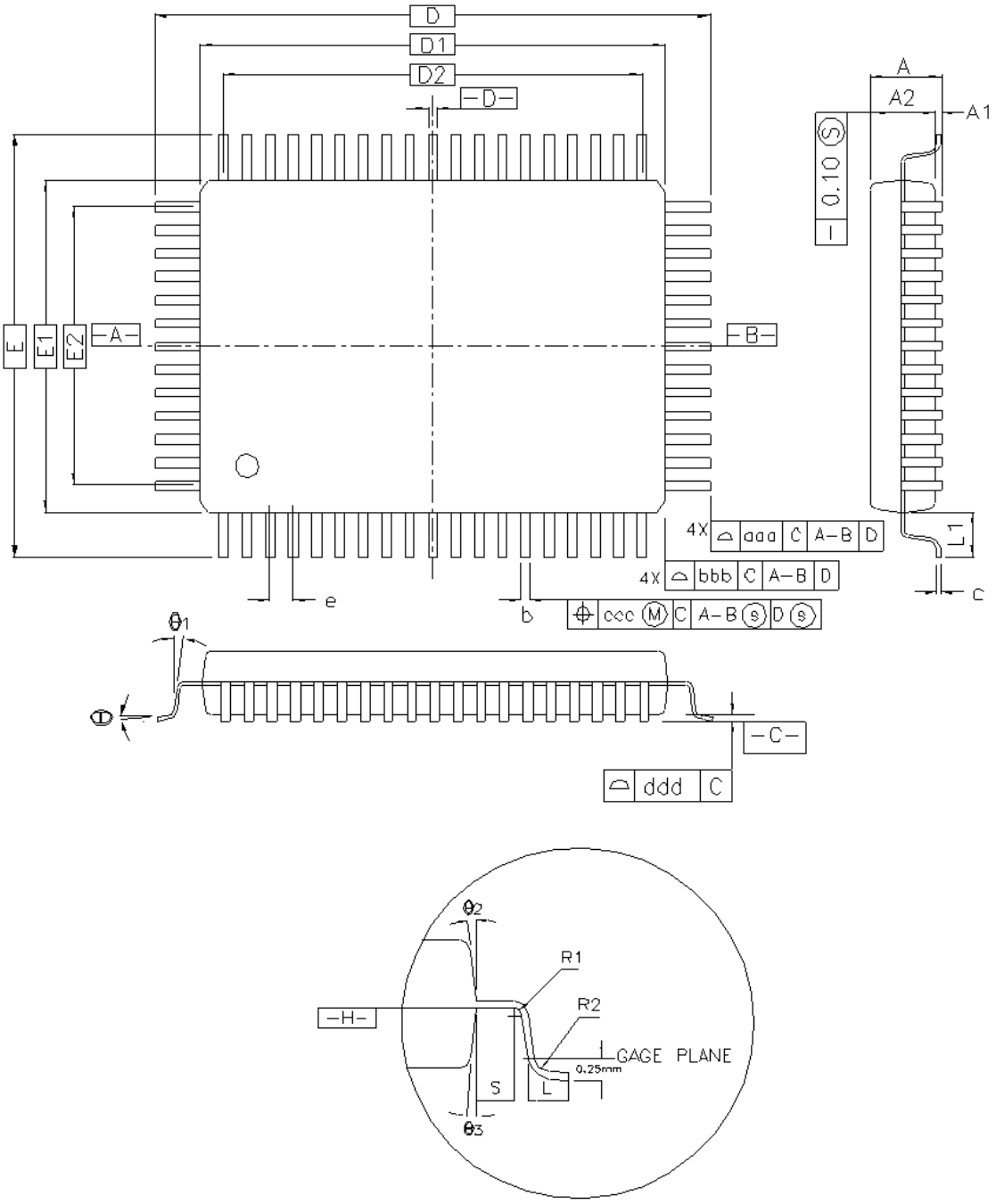


Fig 24. Read Timing Diagram in Parallel Interface

Table 14.Decoder Performance Parameter

Parameter	Symbol	Min	Typ	Max	Units
Analog characteristics					
Differential gain	D_G			3	%
Differential phase	D_P			2	deg
Channel Cross-talk	α_{ct}			-50	dB
Bandwidth (at –3dB)	BW		7		MHz
Horizontal PLL					
Line frequency (60Hz)	f_H		15.734		KHz
Line frequency (50Hz)	f_H		15.625		KHz
Permissible static deviation	Δf_H			±6	%
Subcarrier PLL					
Subcarrier frequency (NTSC-M)	f_{SC}		3.579545		MHz
Subcarrier frequency (PAL-BDGHI)	f_{SC}		4.433619		MHz
Subcarrier frequency (PAL-M)	f_{SC}		3.575612		MHz
Subcarrier frequency (PAL-N)	f_{SC}		3.582056		MHz
Lock in range	Δf_{SC}	±800			Hz
AGC (Auto Gain Control)					
Range	AGC	-6		18	dB
ACC (Auto Color Gain Control)					
Range	ACC	-6		30	dB
Oscillator Input					
Nominal frequency	f_{OSC}		54		MHz
Permissible frequency deviation	$\Delta f_{OSC}/f_{OSC}$			±100	ppm
Duty cycle	dt_{OSC}			60	%

Package Dimension



SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	—	0.08	—	—	0.003	—
ddd	—	0.08	—	—	0.003	—

COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A_1	0.25	—	—	0.010	—	—
A_2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D_1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E_1	14.00 BASIC			0.551 BASIC		
R_2	0.13	—	0.30	0.005	—	0.012
R_1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ_1	0°	—	—	0°	—	—
ALLOY 42 L/F θ_2, θ_3	7° REF			7° REF		
COPPER L/F θ_2, θ_3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

Application Information

Video Input Interface

TW2804 has a built-in 2:1 input MUX for software controllable input selections. This MUX can be used to select two composite video sources. For a typical application, a video input requires an analog low-pass filter for alias reduction. An illustration is shown in the following application schematic.

Clamping / AGC

TW2804 has built-in clamping and AGC circuitry. The analog inputs must be AC coupled through an external 2.2uF capacitor. Without it, no extra external component is needed for this operation. The clamping and AGC tracking time constant can be controlled through register setting.

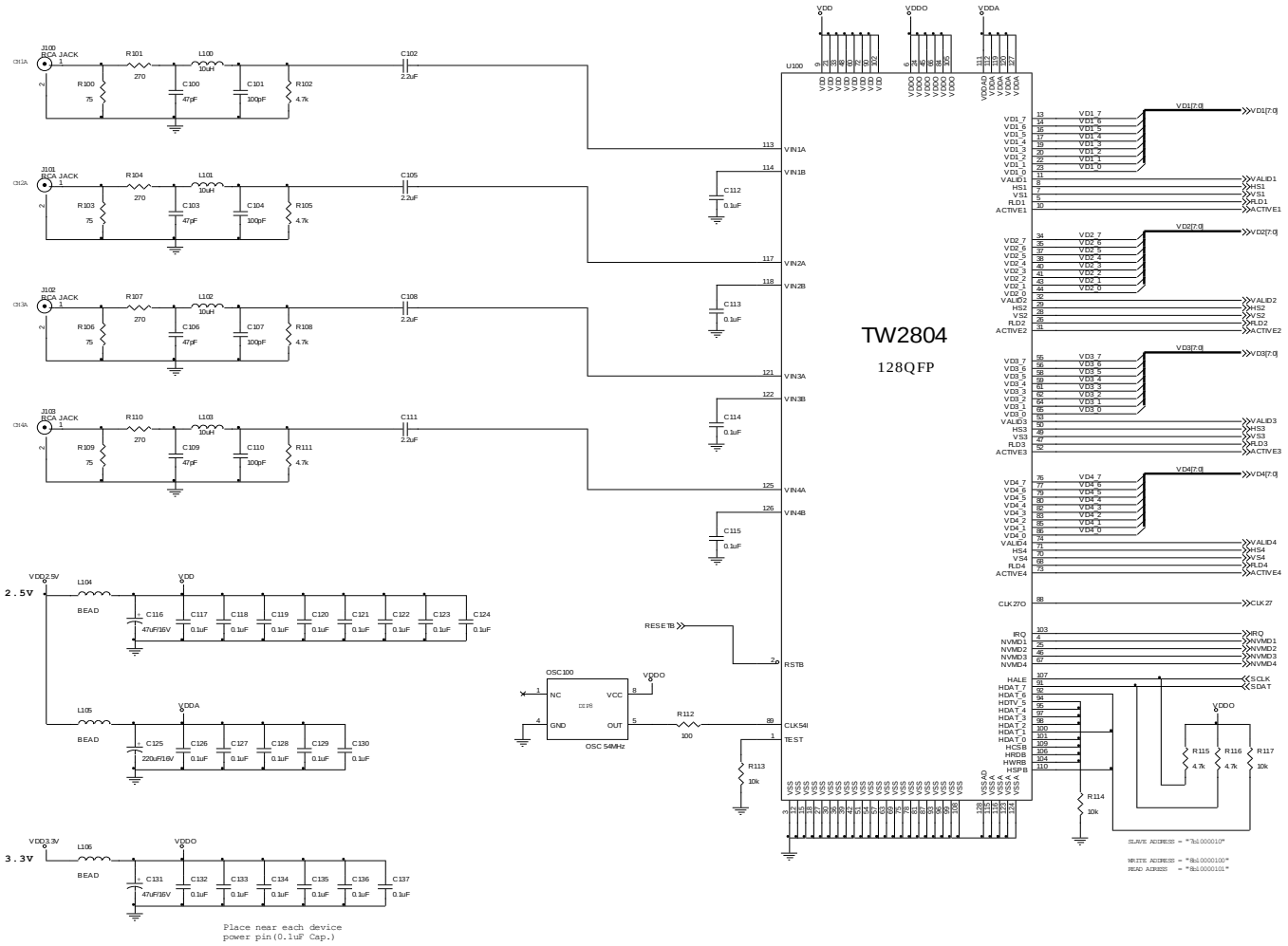
Video Output Interface

All video data and sync outputs of four channels are synchronous to pin CLK27O. Therefore, pin CLK27O should be connected to four channel interfaces for synchronizing data.

Power-Up

After power-up, TW2804 registers have unknown values. The RSTB pin must be asserted and released to bring all registers to its default values. After reset, TW2804 data outputs are tri-stated. The OE (0x3B) register should be written after reset to enable outputs desired.

Application Schematic



Revision History

Table 15 Datasheet Revision History

Revision	Date	Description	Product Code
0.9	Oct / 01 / 2002	Engineering Release	E BAHB (Eng RevB)
1.0	Dec / 11 / 2002	(1) Update Application Schematic (P.77) (2) Update Recommended Value of Control Register Map (P.31~32)	E BAHB (Eng RevB)
1.1	Jan / 29 / 2003	(1) Update Control Register Map (Read only description is added) (P.29~30, P.33~34, P.58)	E BAHB (Eng RevB)
1.2	Feb / 04 / 2003	(1) Update Application Schematic (P.77) (2) Update Recommended Value of Control Register Map (P.31~32)	E BAHB (Eng RevB)
1.3	Feb / 17 / 2003	(1) Update Control Register Map (Default value is added) (P.34, P.40, P.45, P.47, P.60) (2) Update Fig.14 (P.25)	E BAHB (Eng RevB)
2.0	Feb / 19 / 2003	(1) Change Pin Diagram (P.5~7) (2) Update Application Schematic (P.76)	E BAHC (Eng RevC)
2.1	Apr / 25 / 2003	(1) Update Fig 4 and Fig 9 (P.12, P.16) (2) Update Table 4 (P.23) (3) Update Control Register Map and Recommended Value (P.29~32, P.35, P.40, P.45~47, P.50~51, P.60, P.63~70) (4) Fix FLDPOL and NVMD mode (P.41, P.60)	E BAHC (Eng RevC)
2.2	Jul / 21 / 2003	(1) Update Fig 19 (P.27)	E BAHC (Eng RevC)
2.3	Aug / 16 / 2003	(1) Change digital power(Pin 111) and ground pin(Pin 128) to analog power and ground pin (P.5 ~ 7) (2) Change Recommended Value of Control Register 0xFB (P.69) (2) Update parallel interface timing diagram (P.27) (3) Update Application Schematic (P.77)	E BAHD (Eng RevD)
2.4	Sep / 09 / 2003	(1) Update Supply Current and Power Dissipation information (P.72) (2) Update Application Information (P.76) (3) Update Application Schematic (P.77)	E BAHD (Eng RevD)
2.5	Nov / 11 / 2003	(1) Update Fig 12 and Fig 15 (P.23, P.25) (2) Update Control Register Map (P.65) (3) Update Decoder Performance Parameter (P.74) (4) Update Application Schematic (P.78)	E BAHE (Eng RevE)
2.6	Dec / 26 / 2003	(1) Update Register Description for VBW bits (P.50) (2) Update Serial and Parallel Interface Timing Parameter (P.74,75) (3) Update Analog Characteristics (P.76)	E BAHE (Eng RevE)

2.7	Apr / 08 / 2004	(1) Update Recommended Value of Control Register Map (P.31~32) (2) Update Application Schematic (P.80)	BAHE (RevE)
2.8	May / 04 / 2004	(1) Update Application Schematic (P.80)	BAHE (RevE)
2.9	Jul / 14 / 2004	(1) Update Supply Current and Power Dissipation information (P.72) (2) Update Application Schematic (P.80)	BAHE (RevE)
3.0	Jul / 16 / 2005	(1) Update the Ambient Operating Temperature (P.71) (2) Update the Power On/Off sequence (P.71)	BAHE (RevE)
FN7732.0	Jan / 31 / 2011	Assigned file number FN7732.0 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. No changes to datasheet content.	
FN7732.1	May 8, 2017	Applied header/footer. Moved Introduction, Features and applications to page 1.	

Table 16. List of Revision Point in TW2804 RevC

No.	Issue	TW2804 RevB	TW2804 RevC
1	Cross-talk	Cross-talk between adjacent input channels	Remove cross-talk by modifying analog circuit and changing analog pin location
2	100% amplitude, 100% saturation Color bar pattern	Clipping the yellow and cyan pattern	Fixed by adjusting data range
3	Contrast range	Biased toward upper range	Fixed by adjusting contrast range
4	Background color pattern	Not supported	Supported with Blue and Black pattern
5	Vertical scaling filter	A little aliasing noise is remained	Rejected perfectly by improving vertical scaling filter
6	IRQ polarity	Only active high is supported	Both active high and low are supported
7	Optional ITU –R 656 code set	Not supported	Optional No-video and non-valid code set are supported
8	Peaking filter	Common mode in Scaling X and Y path	Separate mode in Scaling X and Y path

Table 17 List of Revision Point in TW2804 RevD

No.	Issue	TW2804 RevC	TW2804 RevD
1	ADC Linearity	Not good in ADC linearity	Improve ADC linearity

Table 18 List of Revision Point in TW2804 RevE

No.	Issue	TW2804 RevD	TW2804 RevE
1	ADC Linearity	Improve ADC linearity	Improve ADC linearity more
2	Field Offset Control	Not supported	Supports the field offset control for speeding up the field rate in analog switching mode