

TP70H480G4JSG

700V SuperGaN® GaN FET in PQFN (source tab)

Description

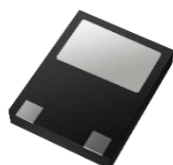
The TP70H480G4JSG 700V, 480mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low-voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

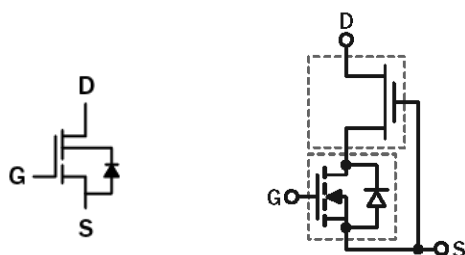
Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Easy to drive with commonly used gate drivers

Product/Schematic Diagrams



TP70H480G4JSG PQFN



Cascode Schematic Symbol

Cascode Device Structure

(MOSFET has integrated ESD Protection Circuit)

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Robust design, defined by
 - Transient over-voltage capability
 - Operation with E-mode Gate drivers without need for Zener protection
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging
- 2kV HBM ESD rating

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting



Key Specifications

V _{DS} (V)	700
V _{DSS(TR)} (V)	800
R _{DS(on)} (mΩ) maximum ^[1]	560
Q _{oss} (nC) typical	9.2
Q _G (nC) typical	5.2

1. Dynamic RDS(on); see Figure 21 and Figure 22.

Contents

1. Pin Information	3
1.1 Pin Assignments	3
1.2 Pin Descriptions	3
2. Specifications	4
2.1 Absolute Maximum Ratings	4
2.2 Thermal Specifications	4
2.3 Circuit Implementation	5
2.4 Electrical Specifications – Forward Device	6
2.5 Electrical Specifications – Reverse Device	7
3. Typical Performance Graphs	8
4. Test Circuits and Waveforms	11
5. Package Outline Drawings	12
6. Design Considerations	13
7. Related Information	13
8. Ordering Information	13
9. Revision History	13

Figures

Figure 1. Pin Assignments – Bottom View	3
Figure 2. Simplified Half-Bridge Schematic	5
Figure 3. Simplified Single-Ended Schematic	5
Figure 4. Typical Output Characteristics, $T_J = 25^{\circ}\text{C}$	8
Figure 5. Typical Output Characteristics, $T_J = 150^{\circ}\text{C}$	8
Figure 6. Typical Transfer Characteristics	8
Figure 7. Normalized On-resistance	8
Figure 8. Typical Capacitance	8
Figure 9. Typical C_{OSS} Stored Energy	8
Figure 10. Typical Q_{OSS}	9
Figure 11. Typical Gate Charge	9
Figure 12. Power Dissipation	9
Figure 13. Current Derating	9
Figure 14. Forward Characteristics of Rev. Diode	9
Figure 15. Transient Thermal Resistance	9
Figure 16. Safe Operating Area $T_C = 25^{\circ}\text{C}$	10
Figure 17. Switching Time Test Circuit	11
Figure 18. Switching Time Waveform	11
Figure 19. Diode Characteristics Test Circuit	11
Figure 20. Diode Recovery Waveform	11
Figure 21. Dynamic $R_{DS(on)eff}$ Test Circuit	11
Figure 22. Dynamic $R_{DS(on)eff}$ Waveform	11

1. Pin Information

1.1 Pin Assignments

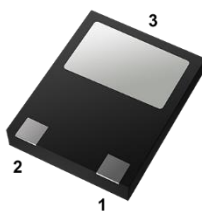


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1	G	Gate.
2	D	Drain.
3	S	Source.

2. Specifications

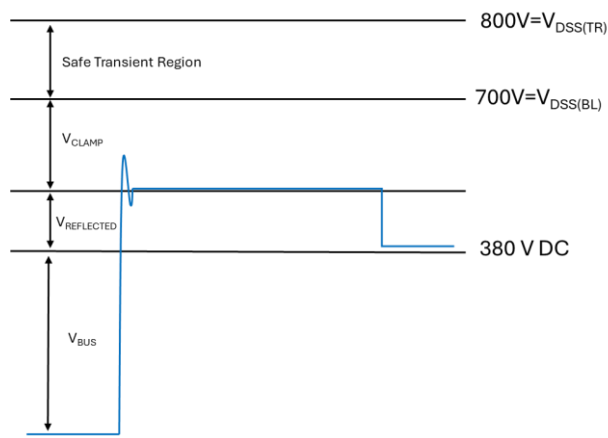
2.1 Absolute Maximum Ratings

($T_c = 25^\circ\text{C}$ unless otherwise stated.)

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter		Minimum	Maximum	Unit
V_{DS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)		-	700	V
$V_{DS(TR)}$, non-repetitive	Transient drain to source voltage, non-repetitive ^[1]		-	800	
$V_{DS(TR)}$, repetitive	Transient drain to source voltage, repetitive ^[2]		-	750	
V_{GS}	Gate to source voltage		-12	+12	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$		-	25	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$ ^[3]		-	5	A
	Continuous drain current at $T_c = 100^\circ\text{C}$ ^[3]		-	3.1	A
I_{DM}	Pulsed drain current (pulse width: 10 μs)		-	30	A
T_c	Operating temperature	Case	-55	+150	$^\circ\text{C}$
T_J		Junction	-55	+150	$^\circ\text{C}$
T_s	Storage temperature		-55	+150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature ^[4]		-	260	$^\circ\text{C}$

1. In off-state, spike duration < 30 μs , non-repetitive.
2. Off-state, spike duration < 5 μs .
3. For increased stability at high current operation, see "Circuit Implementation".
4. Reflow MSL3.



2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	5	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient ^[1]	50	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm² copper area and 70 μm thickness).

2.3 Circuit Implementation

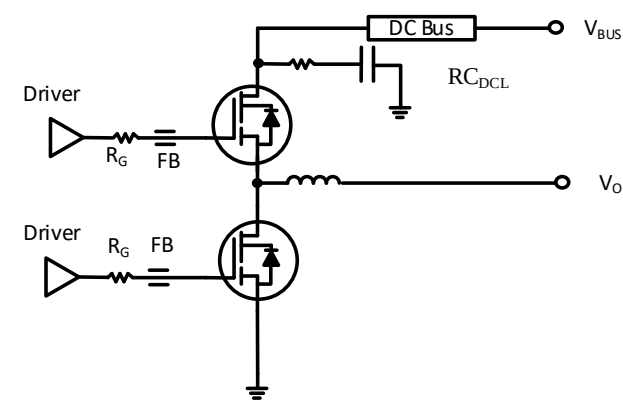


Figure 2. Simplified Half-Bridge Schematic

Recommended gate drive: (0V, 6V) with $R_{G(tot)} = 20\Omega$ ^[1]

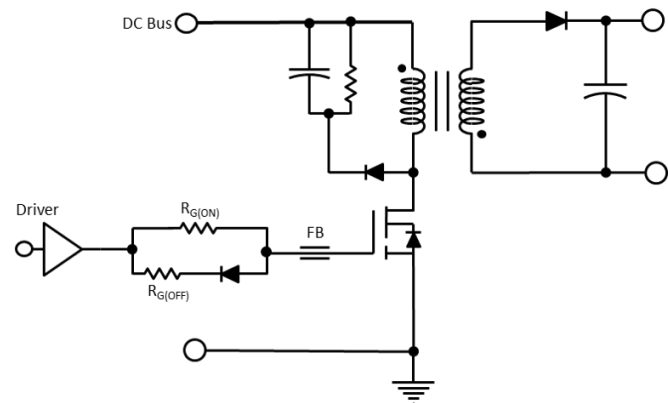


Figure 3. Simplified Single-Ended Schematic

Recommended gate drive:

Gate drive: (0V, 6V): $R_{G(ON)} = 65$ to 150Ω ; $R_{G(OFF)} = 0$ to 10Ω
Gate drive*: (-6V, 6V): $R_{G(ON)} = 65$ to 100Ω ; $R_{G(OFF)} = 0$ to 20Ω

Gate Ferrite Bead (FB1)	Recommended DC Link RC Snubber (RC_{DCL}) ^[2]
120 Ω at 100MHz	4.7nF + 5 Ω

1. For bridge topologies only. R_G could be much smaller in single ended topologies.
2. RC_{DCL} should be placed as close as possible to the drain pin.

For additional driver configurations/options, see application note [Recommended External Circuitry for Renesas GaN FETs](#).

2.4 Electrical Specifications – Forward Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	$V_{GS} = 0V$	700	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 0.5mA$	1.5	2.0	2.5	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-5.8	-	mV/ $^\circ\text{C}$
$R_{DS(on)eff}$	Drain-source on-resistance ^[1]	$V_{GS} = 6V, I_D = 3A$	-	480	560	m Ω
		$V_{GS} = 6V, I_D = 3A, T_J = 150^\circ\text{C}$	-	1000	-	
I_{DSS}	Drain-to-source leakage current	$V_{DS} = 700V, V_{GS} = 0V$	-	1	10	μA
		$V_{DS} = 700V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	-	5	-	
I_{GSS}	Gate-to-source forward leakage current ^[2]	$V_{GS} = 12V$	-	-	10	μA
	Gate-to-source reverse leakage current ^[2]	$V_{GS} = -12V$	-	-	-10	
I_{GSS}	Gate-to-source forward leakage current ^[2]	$V_{GS} = 6V$	-	-	0.1	μA
	Gate-to-source reverse leakage current ^[2]	$V_{GS} = -6V$	-	-	-0.1	
C_{ISS}	Input capacitance	$V_{GS} = 0V, V_{DS} = 400V, f = 1MHz$	-	465	-	pF
C_{OSS}	Output capacitance		-	8	-	
C_{RSS}	Reverse transfer capacitance		-	1.2	-	
$C_{O(er)}$	Output capacitance, energy related ^[3]	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	11.6	-	pF
$C_{O(tr)}$	Output capacitance, time related ^[4]		-	23	-	
Q_G	Total gate charge	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 6V, I_D = 3A$	-	5.2	-	nC
Q_{GS}	Gate-source charge		-	1.3	-	
Q_{GD}	Gate-drain charge		-	2.1	-	
Q_{OSS}	Output charge	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	9.2	-	nC
$t_{D(on)}$	Turn-on delay	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 6V, I_D = 3A, R_G = 20\Omega, Z_{FB} = 120\Omega \text{ at } 100MHz \text{ (see Figure 17)}$	-	23.2	-	ns
t_R	Rise time		-	3	-	
$t_{D(off)}$	Turn-off delay		-	53.6	-	
t_F	Fall time		-	10	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 17 and Figure 18 for conditions.
2. Including leakage current of the integrated ESD protection circuit.
3. Equivalent capacitance to give same stored energy from 0V to 400V.
4. Equivalent capacitance to give same charging time from 0V to 400V.

2.5 Electrical Specifications – Reverse Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	$V_{GS} = 0V$, $T_C = 100^\circ\text{C}$, $\leq 25\%$ duty cycle	-	-	2.3	A
V_{SD}	Reverse voltage ^[1]	$V_{GS} = 0V$, $I_S = 1.3A$	-	1.3	-	V
		$V_{GS} = 0V$, $I_S = 2.6A$	-	1.8	-	
t_{RR}	Reverse recovery time	$I_S = 3A$, $V_{DD} = 400V$, $di/dt = 1000A/\mu s$	-	27.6	-	ns
Q_{RR}	Reverse recovery charge ^[2]		-	0	-	nC

1. Includes dynamic $R_{DS(on)}$ effect.
2. Excludes Q_{oss} .

3. Typical Performance Graphs

$T_c = 25^\circ\text{C}$ unless otherwise stated.

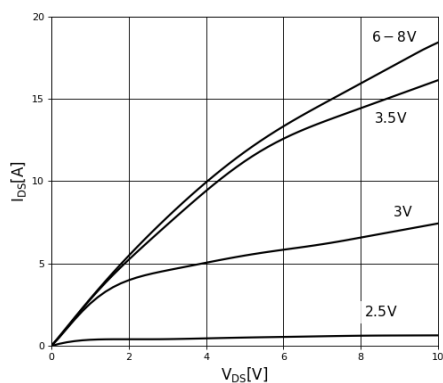


Figure 4. Typical Output Characteristics, $T_J = 25^\circ\text{C}$
Parameter: V_{GS}

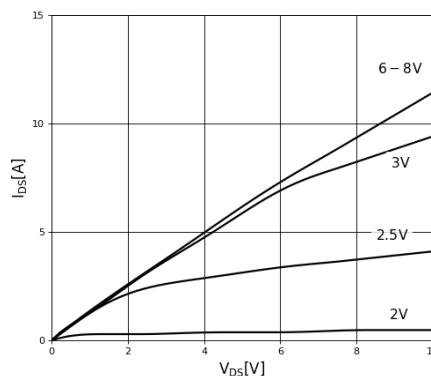


Figure 5. Typical Output Characteristics, $T_J = 150^\circ\text{C}$
Parameter: V_{GS}

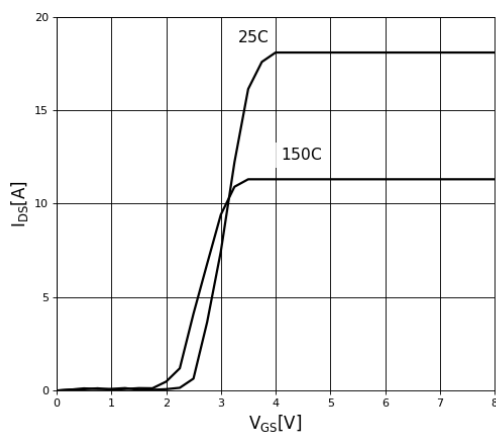


Figure 6. Typical Transfer Characteristics
 $V_{DS} = 10\text{V}$, parameter: T_J

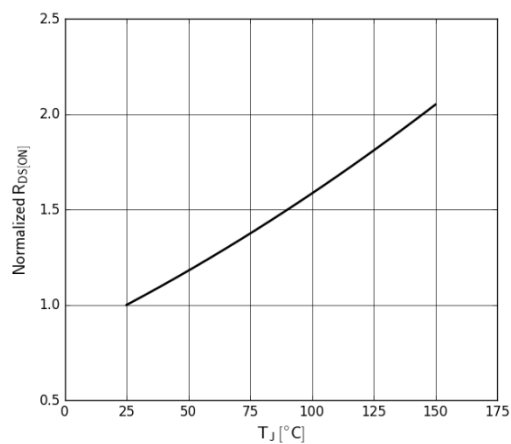


Figure 7. Normalized On-resistance
 $I_D = 3\text{A}$, $V_{GS} = 6\text{V}$

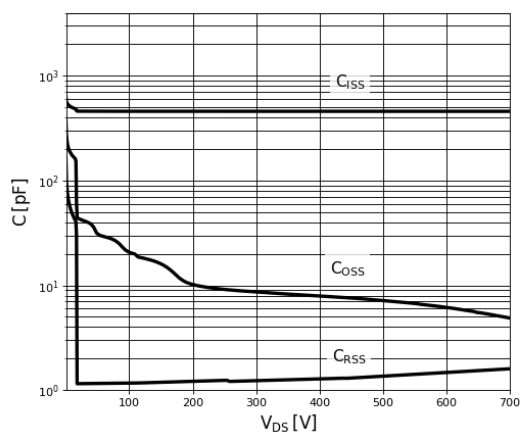


Figure 8. Typical Capacitance
 $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$

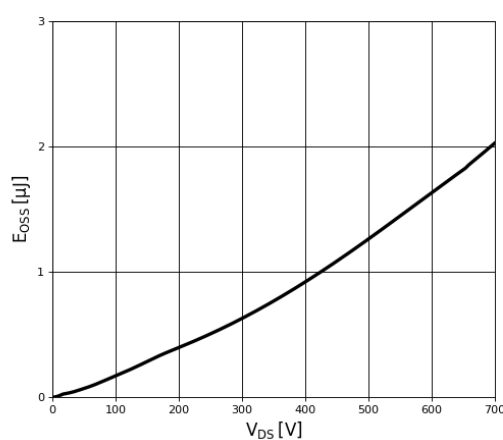


Figure 9. Typical C_{OSS} Stored Energy

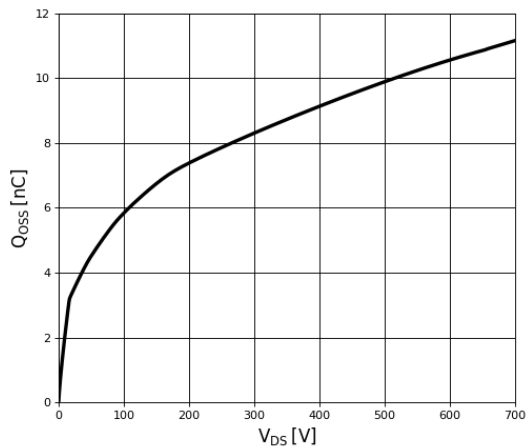


Figure 10. Typical Qoss

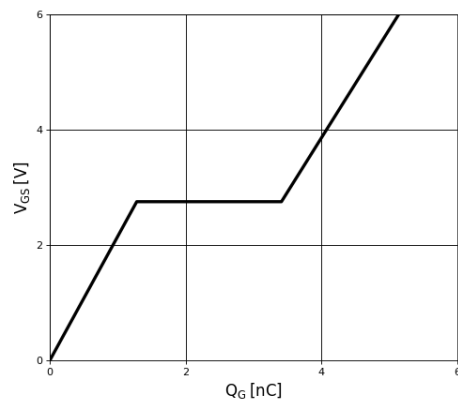


Figure 11. Typical Gate Charge

$I_{DS} = 3A$, $V_{DS} = 400V$

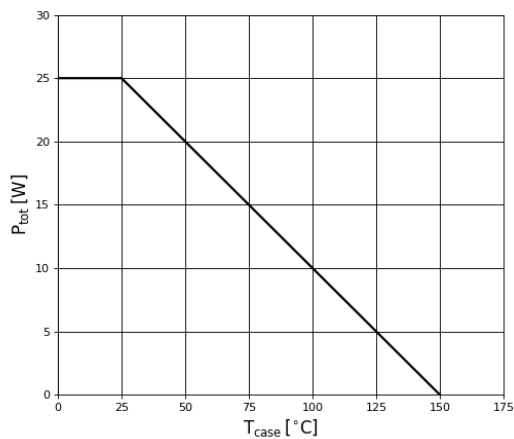


Figure 12. Power Dissipation

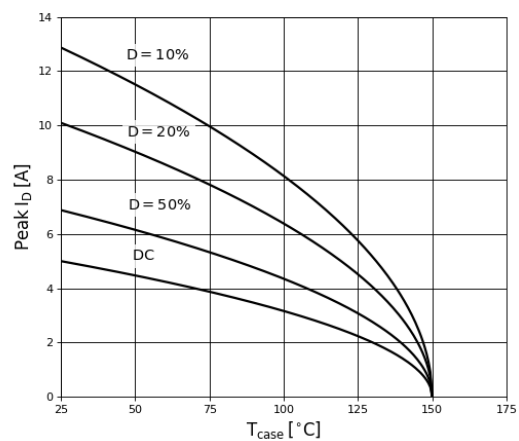


Figure 13. Current Derating

Pulse width $\leq 10\mu s$, $V_{GS} \geq 6V$

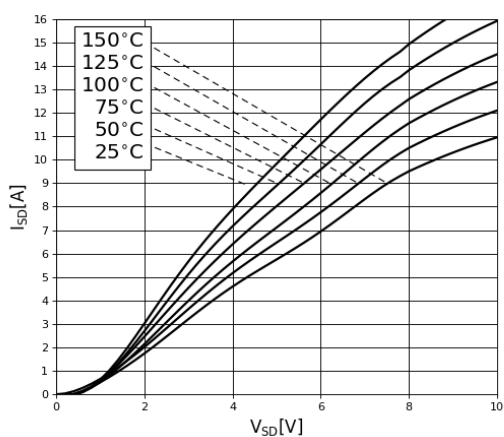


Figure 14. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, parameter: T_J

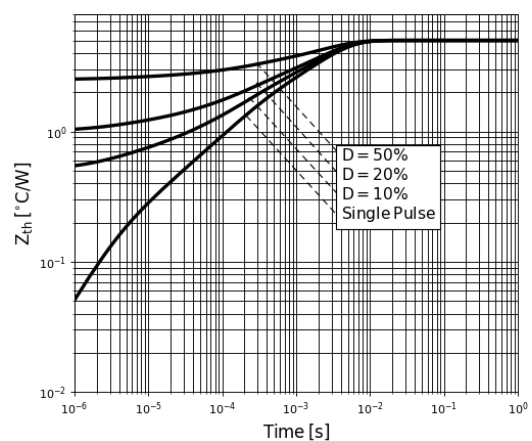


Figure 15. Transient Thermal Resistance

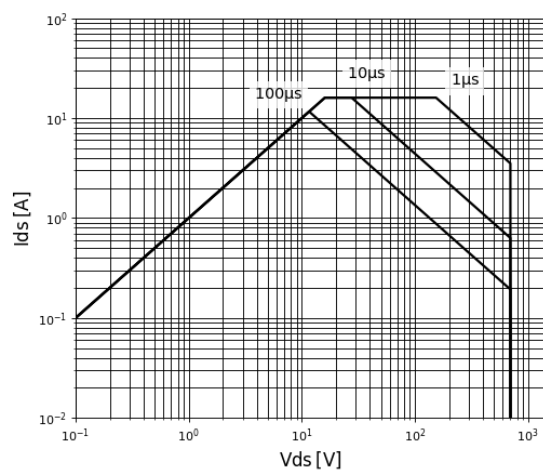


Figure 16. Safe Operating Area $T_C = 25^\circ\text{C}$

4. Test Circuits and Waveforms

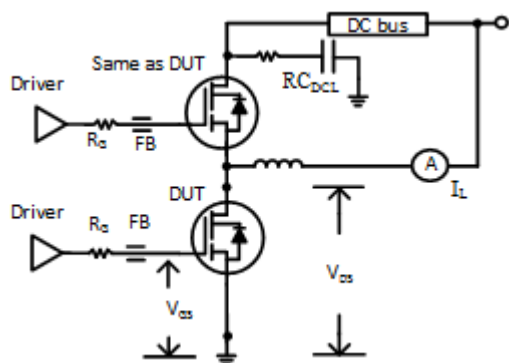


Figure 17. Switching Time Test Circuit

(For methods to ensure clean switching, see "Circuit Implementation")

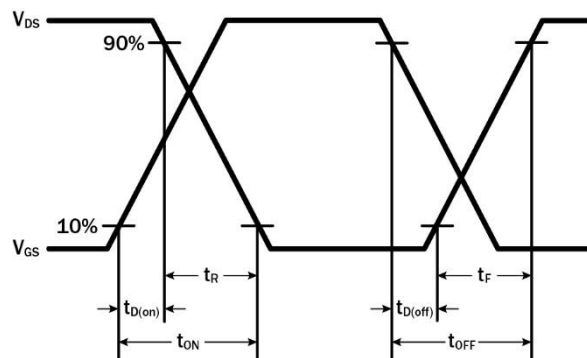


Figure 18. Switching Time Waveform

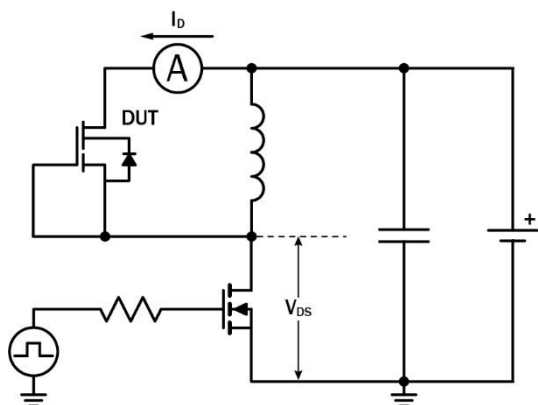


Figure 19. Diode Characteristics Test Circuit

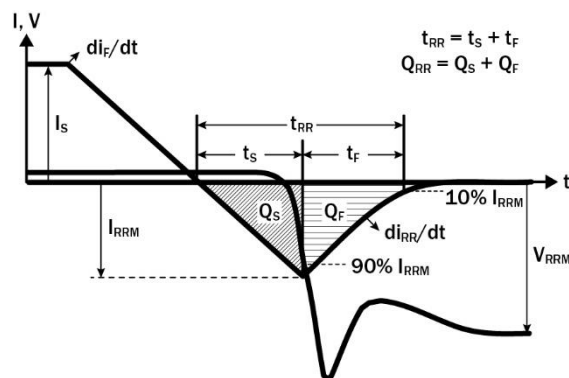


Figure 20. Diode Recovery Waveform

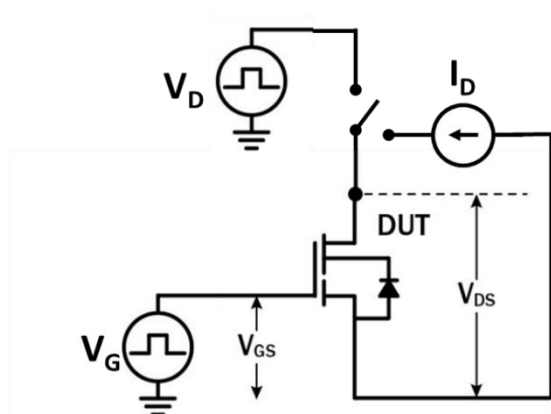


Figure 21. Dynamic $R_{DS(on)eff}$ Test Circuit

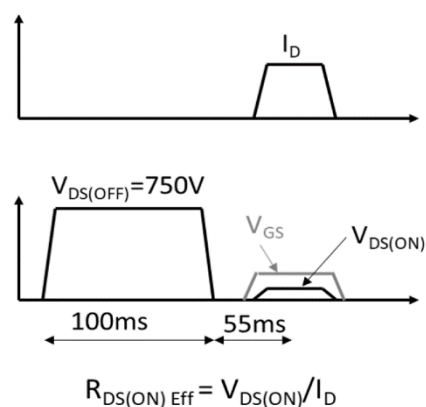
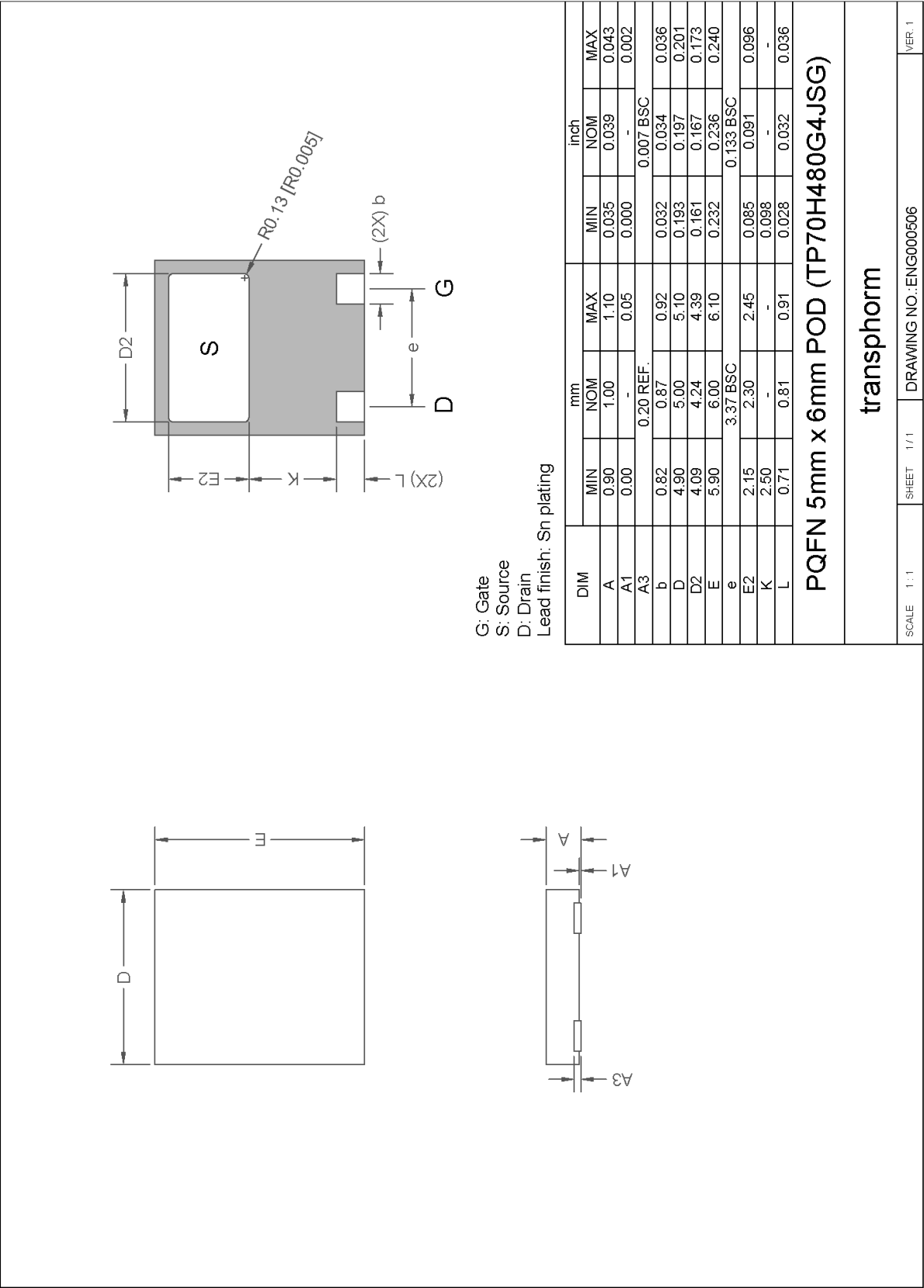


Figure 22. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high-frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas's GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The following table provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:	
DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop.	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout.
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB.	Use long traces in drive circuit, long lead length of the devices.
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points.	Use differential mode probe or probe ground clip with long wire.

7. Related Information

The complete technical library of GaN design tools can be found at [Renesas](#):

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Specific resources include:

- [Printed Circuit Board Layout and Probing for Gan Power Switches](#)
- [Recommendations for Vapor Phase Reflow](#)
- [Recommended External Circuitry for GaN FETs](#)
- [PQFN Tape and Reel Information](#)

8. Ordering Information

Part Number	Package Description	Package Configuration
TP70H480G4JSG-TR ^[1]	5 × 6 PQFN	Source

1. "-TR" suffix refers to tape and reel.

9. Revision History

Revision	Date	Description
1.00	Apr 10, 2025	Initial release.

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