TP65H300G4LSGBE

650V SuperGaN® GaN FET in PQFN (source tab)

Description

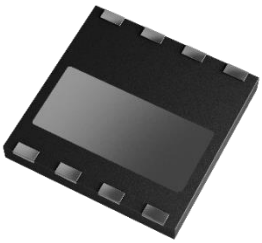
The TP65H300G4LSGBE 650V, 240mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

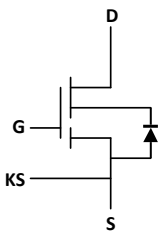
Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly used gate drivers

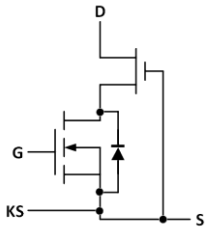
Product/Schematic Diagrams



TP65H300G4LSGBE PQFN



Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Robust design, defined by
  - Transient over-voltage capability
  - Operation with E-mode Gate drivers without need for Zener protection
- Very low QRR
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	312
Q_{OSS} (nC) typical	19
Q_G (nC) typical	12.7

1. Dynamic $R_{DS(on)}$; see Figure 21 and Figure 22.

Contents

Figures

1. Pin Information

1.1 Pin Assignments

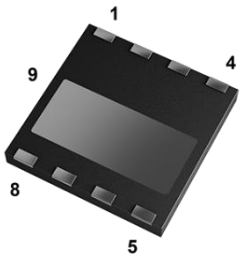


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4	D	Drain.
5, 6	S	Source.
7	KS	Kelvin source.
8	G	Gate.
9	S	Source.

2. Specifications

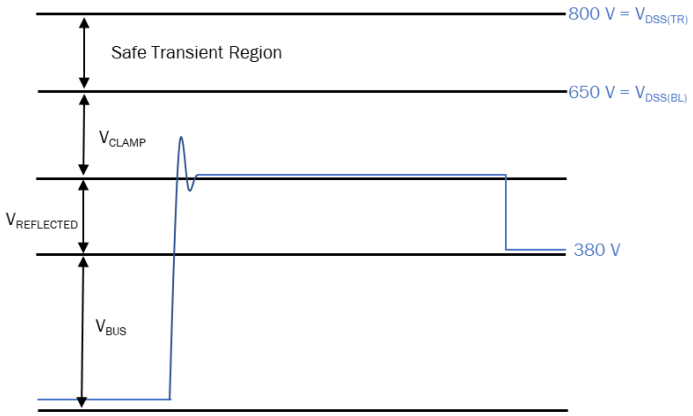
2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter		Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		-	650	V
$V_{DSS(TR)}$, non-repetitive	Transient drain to source voltage, non-repetitive [1]		-	800	
$V_{DSS(TR)}$, repetitive	Transient drain to source voltage, repetitive [2]		-	750	
V_{GSS}	Gate to source voltage		-20	+20	
P_D	Maximum power dissipation at T_C = 25°C		-	31.5	W
I_D	Continuous drain current at T_C = 25°C [3]		-	8	A
	Continuous drain current at T_C = 100°C [3]		-	5	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		-	30	A
T_C	Operating temperature	Case	-55	+150	°C
T_J		Junction	-55	+150	°C
T_S	Storage temperature		-55	+150	°C
T_{SOLD}	Reflow soldering temperature [4]		-	260	°C

1. In off-state, spike duration < 30µs, non-repetitive.
2. Off-state, spike duration < 5µs.
3. For increased stability at high current operation, see “Circuit Implementation”.
4. Reflow MSL3.



Primary Switch Voltage Stress (264 V AC)

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	4	°C/W
$R_{\theta JA}$	Junction-to-ambient [1]	50	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm2 copper area and 70µm thickness).

2.3 Circuit Implementation

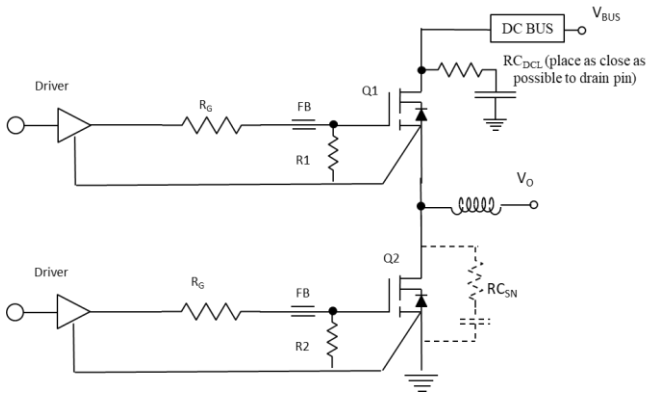


Figure 2. Simplified Half-Bridge Schematic

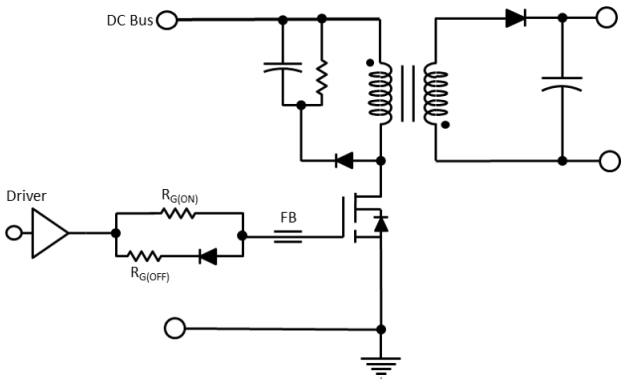


Figure 3. Simplified Single-Ended Schematic

Recommended gate drive: (0V, 6V) with $R_{G(tot)}$ = 15Ω [1]

Recommended gate drive:

Gate drive: (0V, 6V): $R_{G(ON)}$ = 50 to 150 Ω; $R_{G(OFF)}$ = 0 to 10 Ω
Gate drive*: (-6V, 6V): $R_{G(ON)}$ = 50 to 100 Ω; $R_{G(OFF)}$ = 0 to 20 Ω

Gate Ferrite Bead (FB1)	Recommended DC Link RC Snubber (RC_{DCL}) [2]
120Ω at 100MHz	4.7nF + 5Ω

1. For bridge topologies only. R_G could be much smaller in single-ended topologies.
2. RC_{DCL} should be placed as close as possible to the drain pin.

For additional driver configurations/options, see application note Recommended External Circuitry for Renesas GaN FETs.

2.4 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.5mA	1.2	1.6	2	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-5.8	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 6V, I_D = 5A, T_J = 25°C	-	240	312	mΩ
		V_{GS} = 6V, I_D = 5A, T_J = 150°C	-	492	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C	-	1.2	12	µA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	8	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-	-	100	nA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	1225	-	pF
C_{OSS}	Output capacitance		-	16.7	-	
C_{RSS}	Reverse transfer capacitance		-	3.4	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	23.7	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	48	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 6V, I_D = 5A	-	12.7	-	nC
Q_{GS}	Gate-source charge		-	3	-	
Q_{GD}	Gate-drain charge		-	4.6	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	19	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 6V, I_D = 5A, R_{G_on} = 15Ω, R_{G_off} = 5Ω, Z_{FB} = 120Ω at 100MHz (see Figure 17)	-	33	-	ns
t_R	Rise time		-	5.6	-	
$t_{D(off)}$	Turn-off delay		-	68	-	
t_F	Fall time		-	10	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 21 and Figure 22 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.5 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100 °C, ≤25% duty cycle	-	-	5	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 10A	-	3	-	V
		V_{GS} = 0V, I_S = 5A	-	1.9	-	
t_{RR}	Reverse recovery time	I_S = 5A, V_{DD} = 400V, di/dt = 1000A/us	-	29	-	ns
Q_{RR}	Reverse recovery charge [2]		-	0	-	nC

1. Includes dynamic $R_{DS(on)}$ effect.
2. Excludes Q_{OSS}.

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

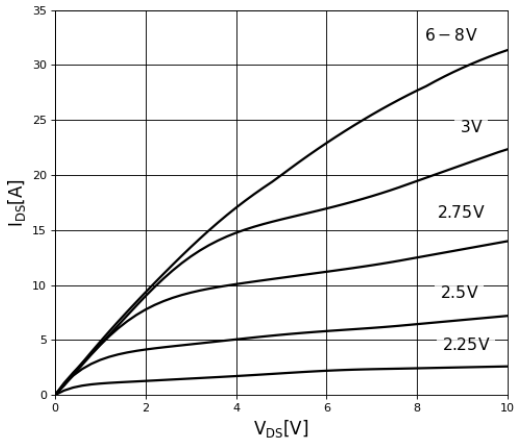


Figure 4. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

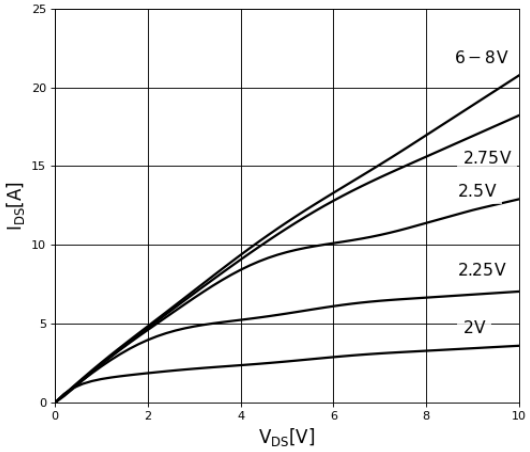


Figure 5. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

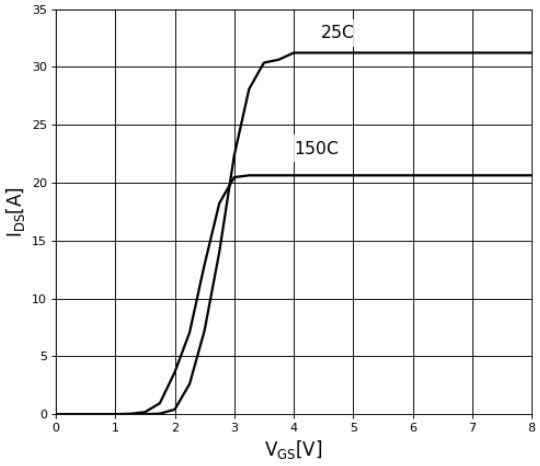


Figure 6. Typical Transfer Characteristics

V_{DS} = 10V, parameter: T_J

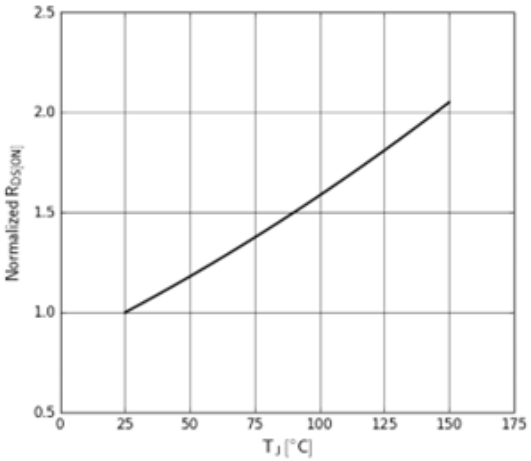


Figure 7. Normalized On-resistance

I_D = 5A, V_{GS} = 6V

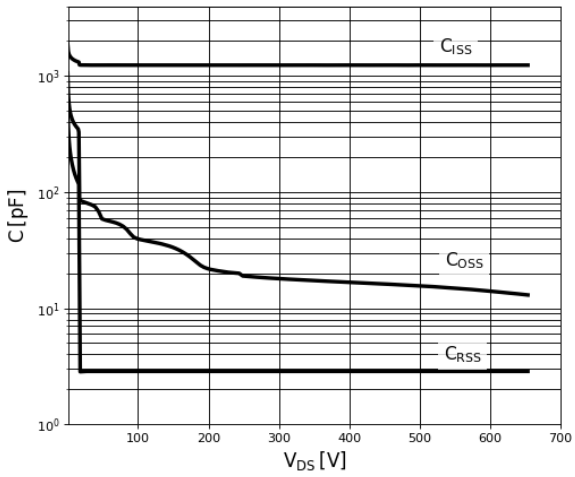


Figure 8. Typical Capacitance

V_{GS} = 0V, f = 1MHz

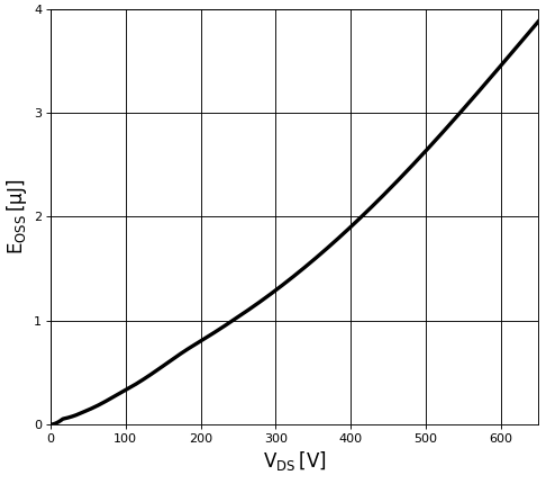


Figure 9. Typical C_{OSS} Stored Energy

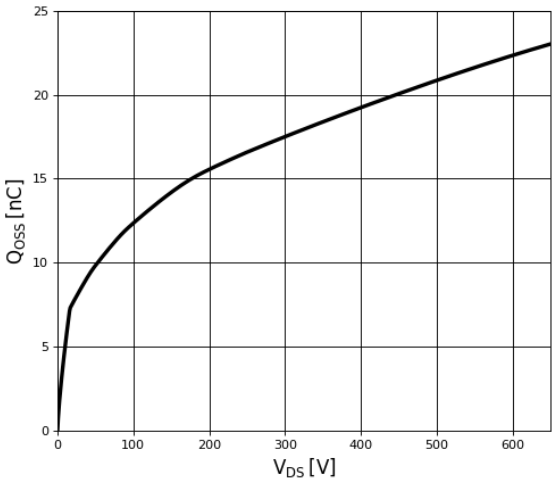


Figure 10. Typical Q_{OSS}

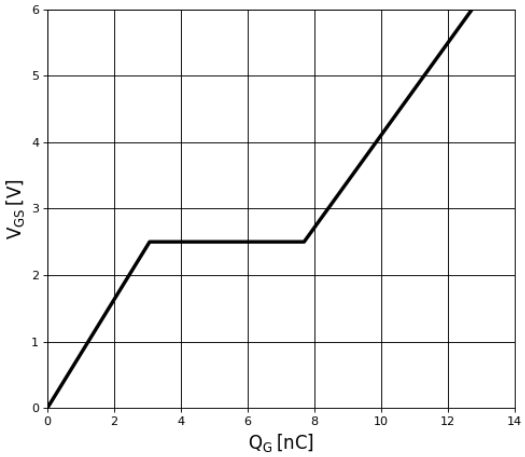


Figure 11. Typical Gate Charge

I_{DS} = 5A, V_{DS} = 400V

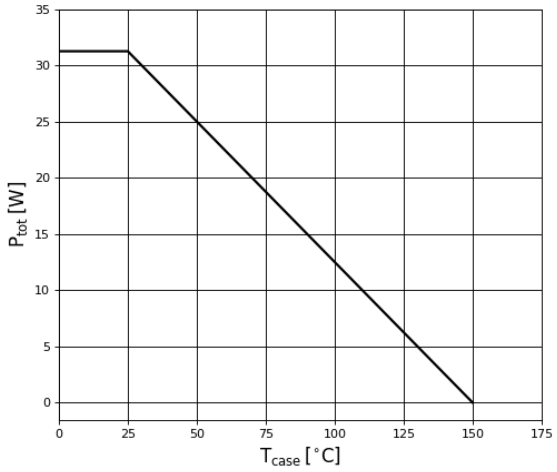


Figure 12. Power Dissipation

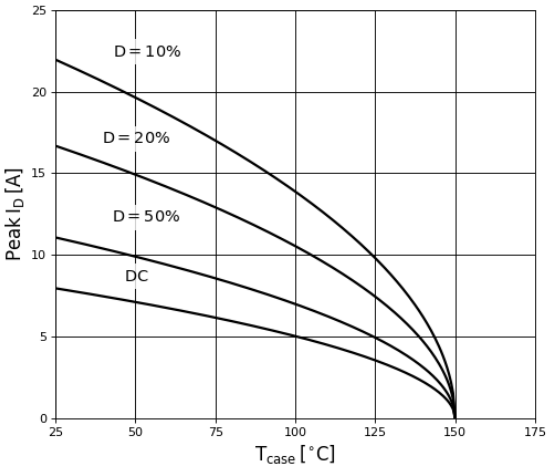


Figure 13. Current Derating

Pulse width ≤ 10µs, V_{GS} ≥ 6V

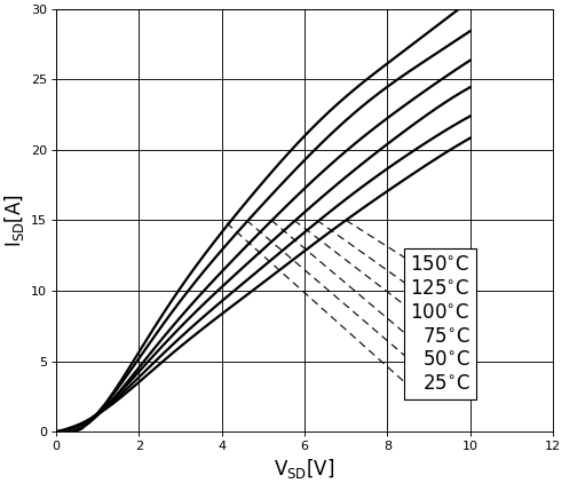


Figure 14. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, parameter: T_J

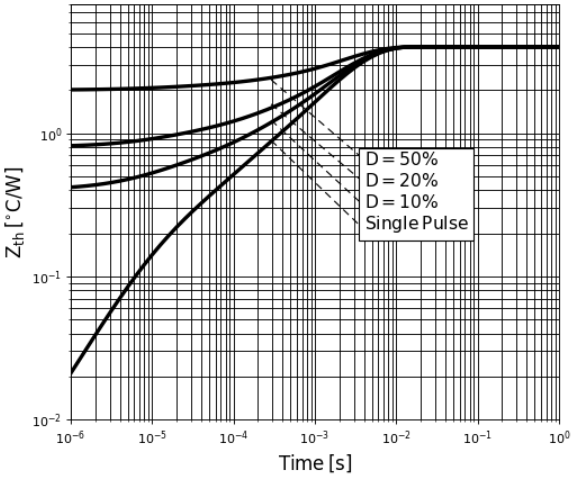


Figure 15. Transient Thermal Resistance

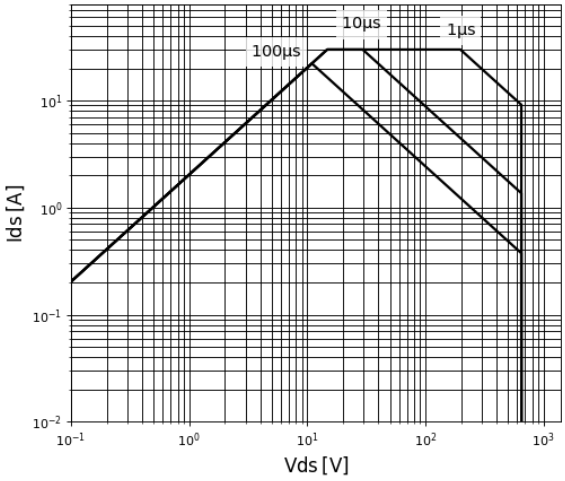


Figure 16. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

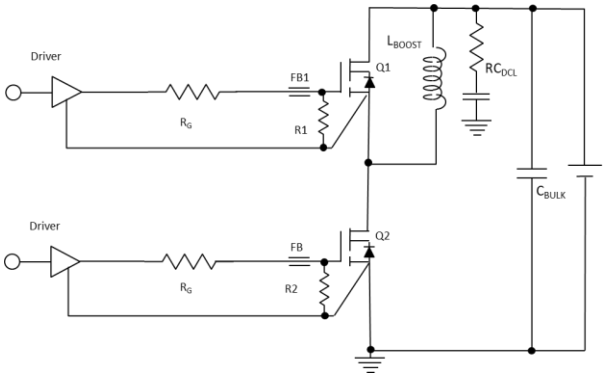


Figure 17. Switching Time Test Circuit

(For methods to ensure clean switching, see “Circuit Implementation”)

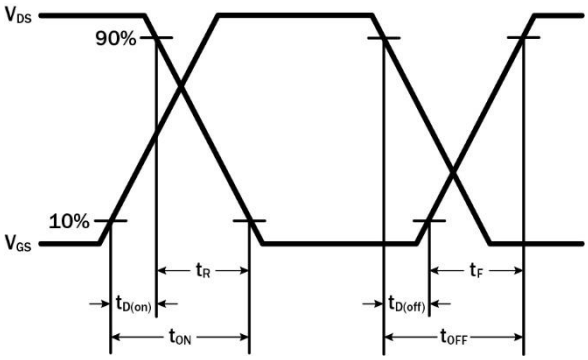


Figure 18. Switching Time Waveform

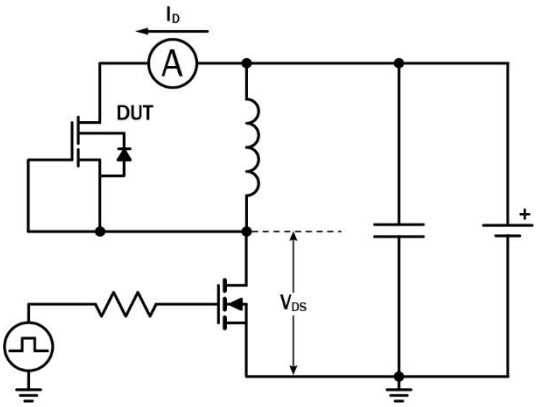


Figure 19. Diode Characteristics Test Circuit

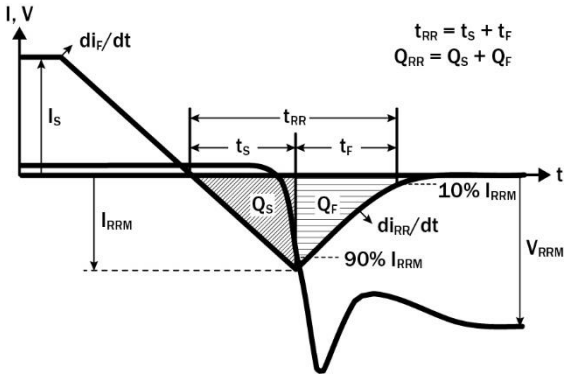


Figure 20. Diode Recovery Waveform

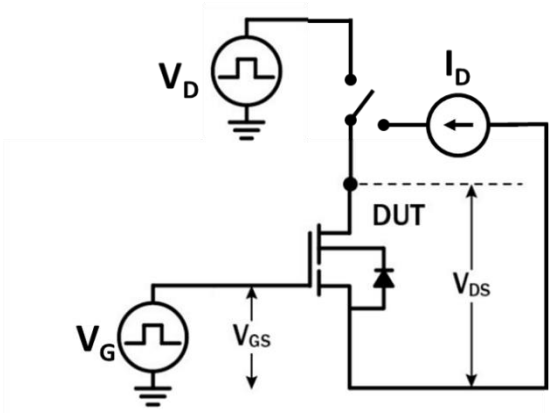


Figure 21. Dynamic $R_{DS(on)eff}$ Test Circuit

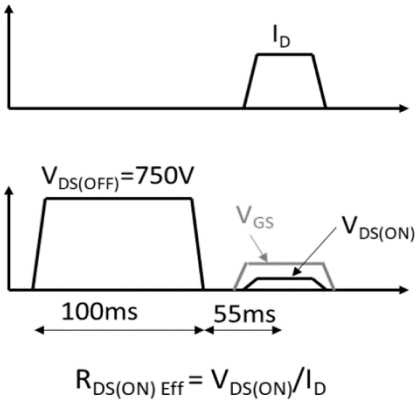
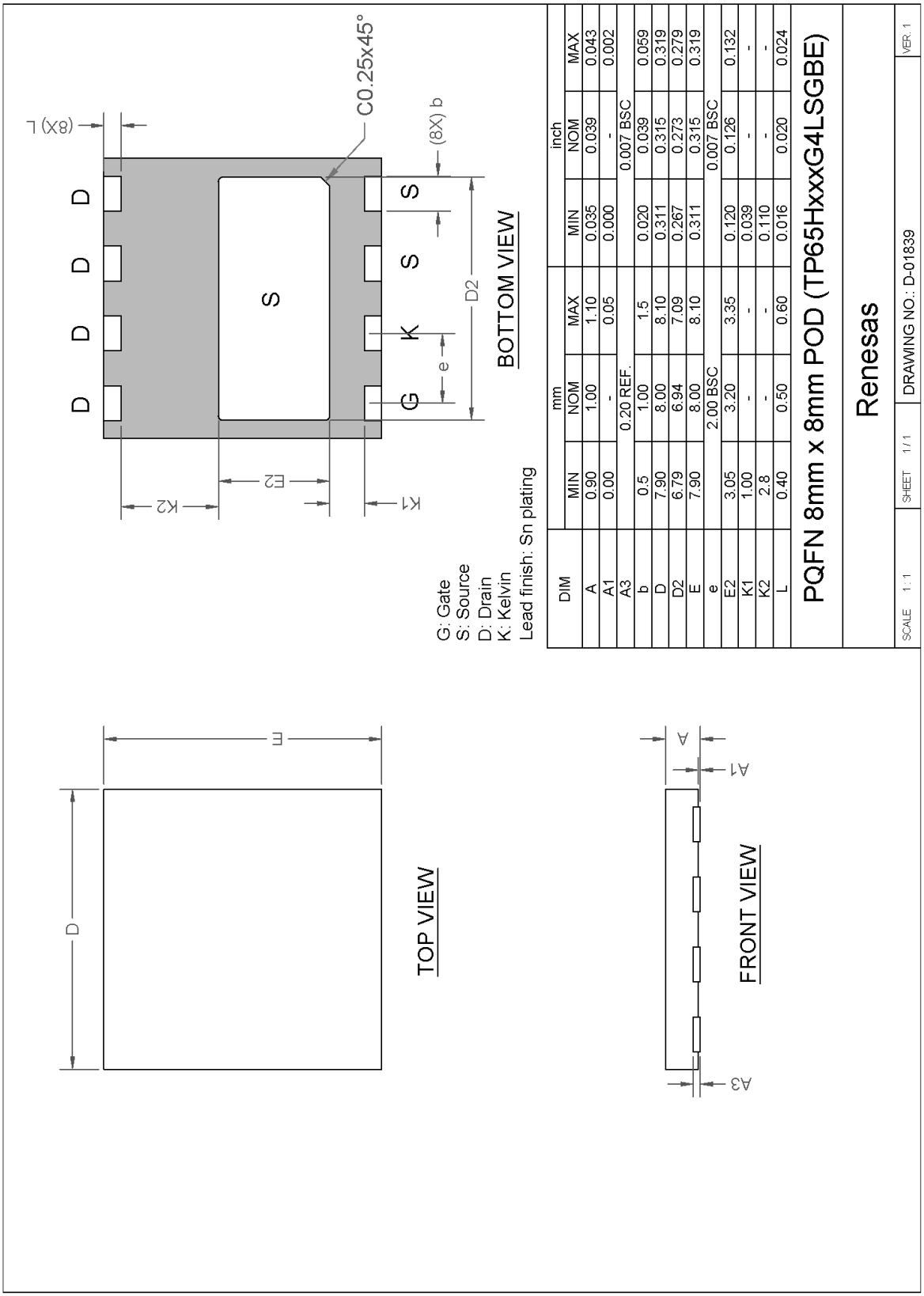


Figure 22. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3		0.20 REF.			0.007 BSC	
b	0.5	1.00	1.5	0.020	0.039	0.059
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.79	6.94	7.09	0.267	0.273	0.279
E	7.90	8.00	8.10	0.311	0.315	0.319
e		2.00 BSC			0.007 BSC	
E2	3.05	3.20	3.35	0.120	0.126	0.132
K1	1.00	-	-	0.039	-	-
K2	2.8	-	-	0.110	-	-
L	0.40	0.50	0.60	0.016	0.020	0.024

6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high-frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note *Printed Circuit Board Layout and Probing for GaN Power Switches*. The following table provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:	
DO	**DO NOT**
Minimize circuit inductance by keeping traces short, both in the drive and power loop.	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout.
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB.	Use long traces in drive circuit, long lead length of the devices.
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points.	Use differential mode probe or probe ground clip with long wire.

7. Related Information

The complete technical library of GaN design tools can be found at Renesas:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Specific resources include:

- *Printed Circuit Board Layout and Probing for Gan Power Switches*
- *Recommendations for Vapor Phase Reflow*
- *Recommended External Circuitry for GaN FETs*
- *PQFN Tape and Reel Information*

8. Ordering Information

Part Number	Package Description	Package Configuration
TP65H300G4LSGBE-TR [1]	8 × 8 PQFN	Source

1. "-TR" suffix refers to tape and reel.

9. Revision History

Revision	Date	Description
1.00	Apr 9, 2025	Initial release.

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