TP65H050G4WS

650V SuperGaN® FET in TO-247-3 (source tab)

Description

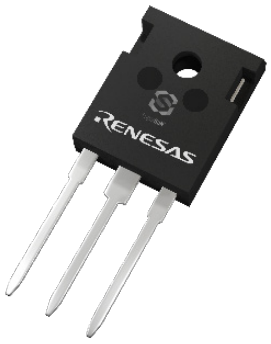
The TP65H050G4WS 650V, 50mΩ gallium nitride (GaN) FET is a normally-off device using Renesas's Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

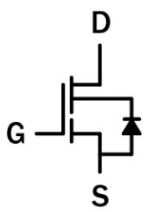
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

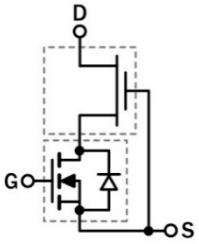
Product and Schematic Diagrams



TP65H050G4WS TO-247-3



Cascode Schematic Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV GaN technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Reduced crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- E-mobility charging
- PV inverter
- UPS
- BESS

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	60
Q_{OSS} (nC) typical	120
Q_G (nC) typical	15.3

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)

Contents

Figures

1. Pin Information

1.1 Pin Assignments

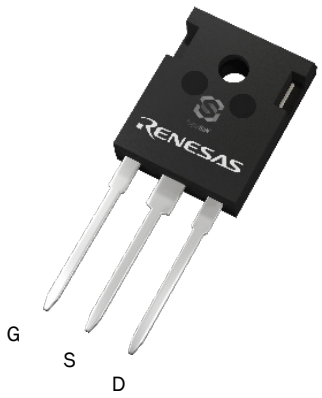


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Name	Description
D	Drain.
S	Source.
G	Gate.

2. Specifications

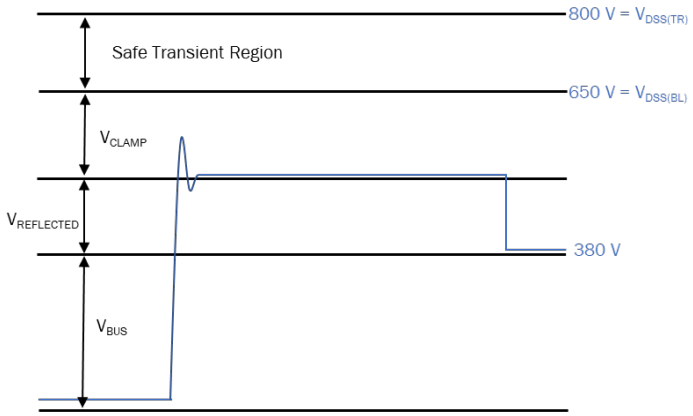
2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	650	V
$V_{DSS(TR)}$	Transient drain to source voltage [1]	800	
V_{GSS}	Gate to source voltage	+20	
P_D	Maximum power dissipation at T_C = 25°C	119	W
I_D	Continuous drain current at T_C = 25°C	34	A
	Continuous drain current at T_C = 100°C	22	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	150	A
T_J	Junction operating temperature	-55 to +150	°C
T_S	Storage temperature	-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [2]	260	°C
-	Mounting torque	80	N cm

1. In off-state, spike duty cycle D < 0.01, spike duration < 30µs, non-repetitive.
2. For 10 sec., 1.6mm from the case.



Primary Switch Voltage Stress (264 V AC)

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	1.05	°C/W
$R_{\Theta JA}$	Junction-to-ambient	40	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.7mA	3.3	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-6.2	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 10V, I_D = 22A, T_J = 25°C	-	50	60	mΩ
		V_{GS} = 10V, I_D = 22A, T_J = 150°C	-	105	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C	-	4	40	μA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	15	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-	-	100	nA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	1000	-	pF
C_{OSS}	Output capacitance		-	110	-	
C_{RSS}	Reverse transfer capacitance		-	6	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	164	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	280	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A	-	15.3	-	nC
Q_{GS}	Gate-source charge		-	6	-	
Q_{GD}	Gate-drain charge		-	5	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	120	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 22A, R_G = 45Ω, Z_{FB} = 240Ω at 100MHz (see Figure 15)	-	49.2	-	ns
t_R	Rise time		-	11.3	-	
$t_{D(off)}$	Turn-off delay		-	88.3	-	
t_F	Fall time		-	10.9	-	

1. Dynamic $R_{DS(on)}$ 100% tested; see Figure 17 and Figure 18 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle	-	-	22	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 22A	-	2.2	-	V
		V_{GS} = 0V, I_S = 11A	-	1.6	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology.

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

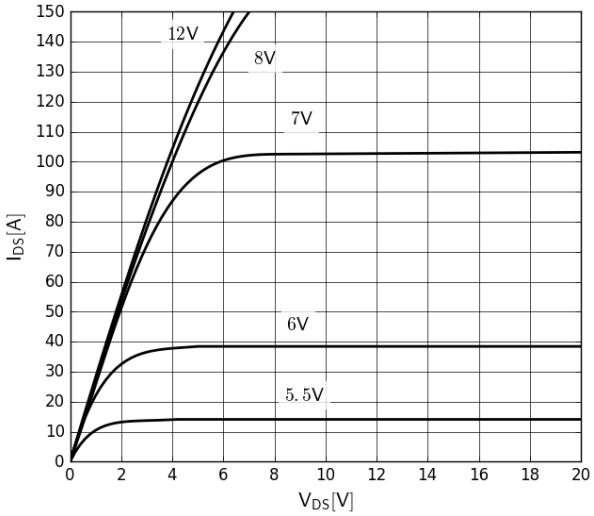


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

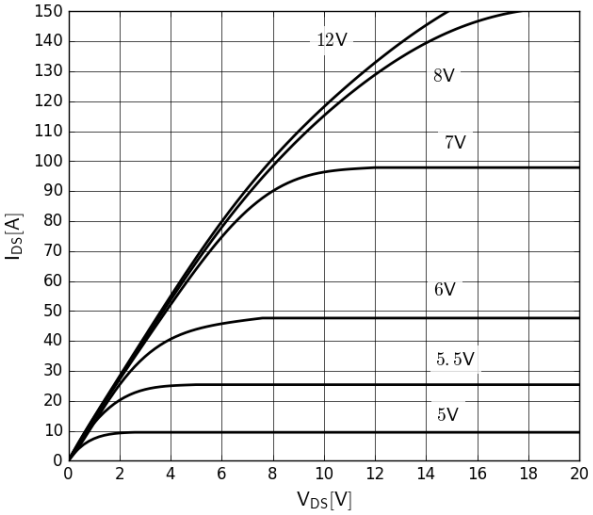


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

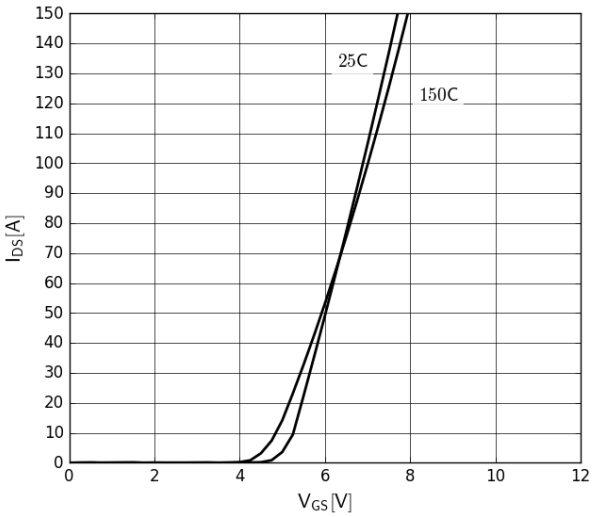


Figure 4. Typical Transfer Characteristics

V_{DS} = 20V, Parameter: T_J

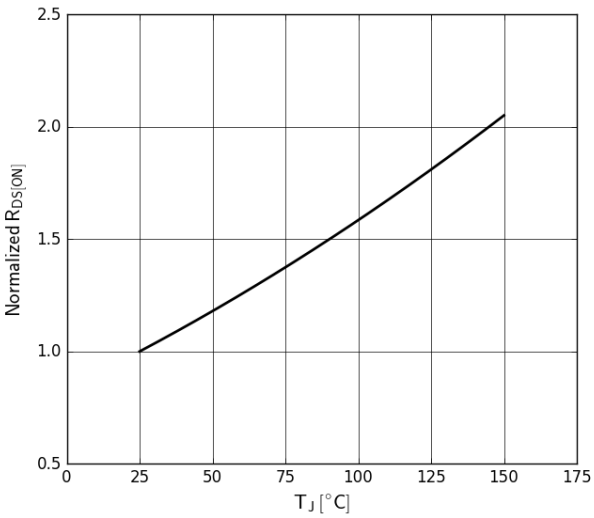


Figure 5. Normalized On-resistance

I_D = 22A, V_{GS} = 10V

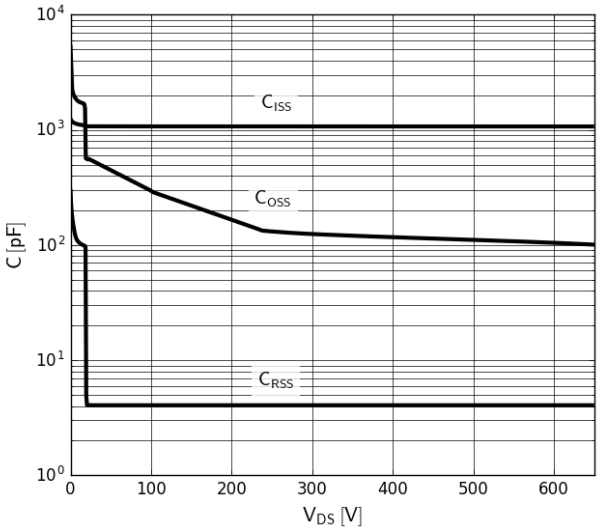


Figure 6. Typical Capacitance

V_{GS} = 0V, f = 1MHz

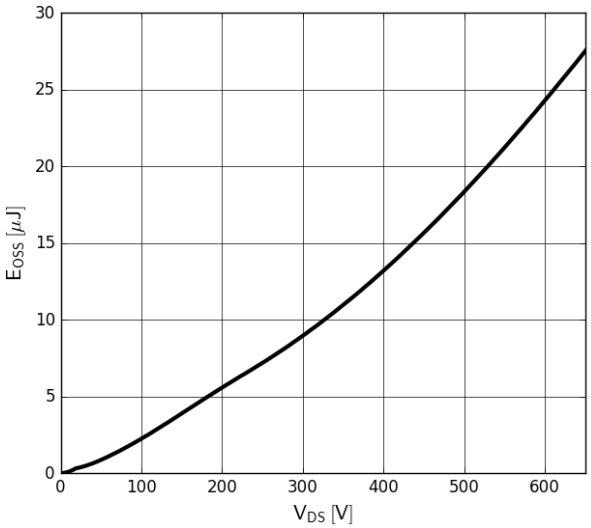


Figure 7. Typical C_{OSS} Stored Energy

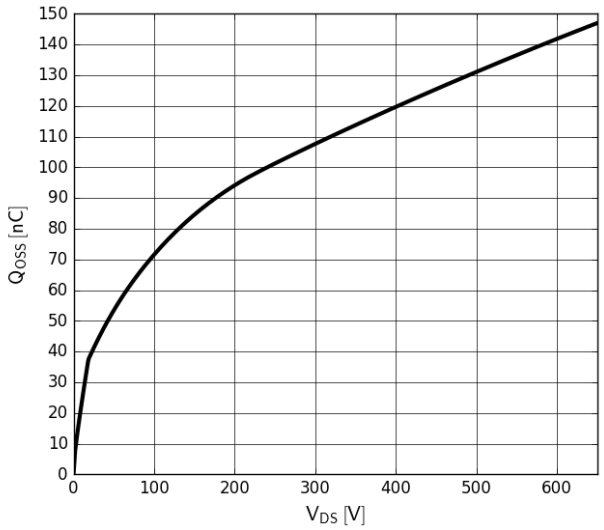


Figure 8. Typical Q_{OSS}

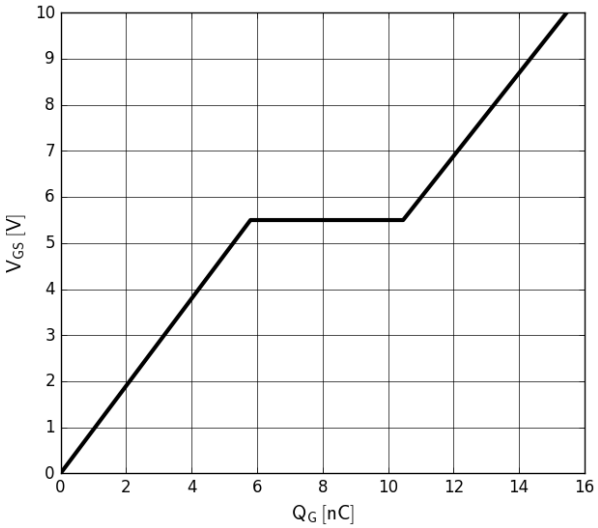


Figure 9. Typical Gate Charge

I_{DS} = 22A, V_{DS} = 400V

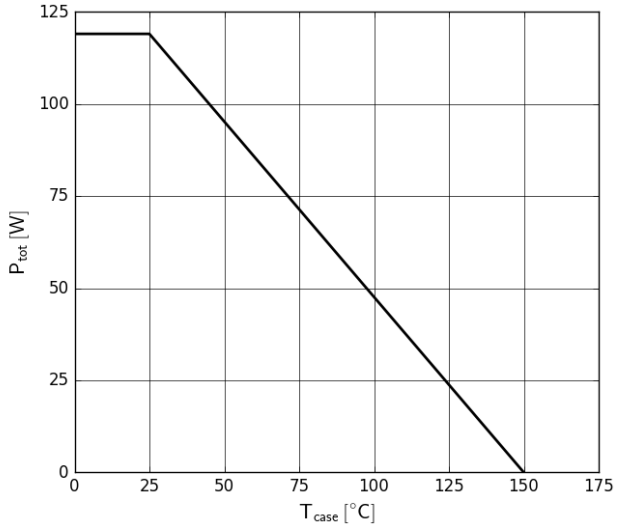


Figure 10. Power Dissipation

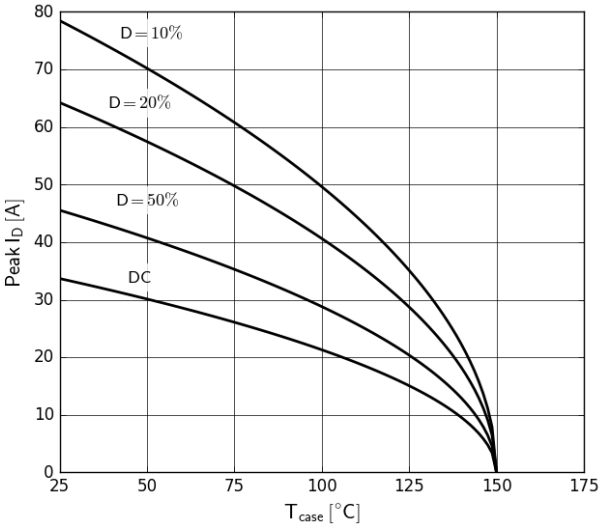


Figure 11. Current Derating

Pulse width ≤ 10µs, V_{GS} ≥ 10V

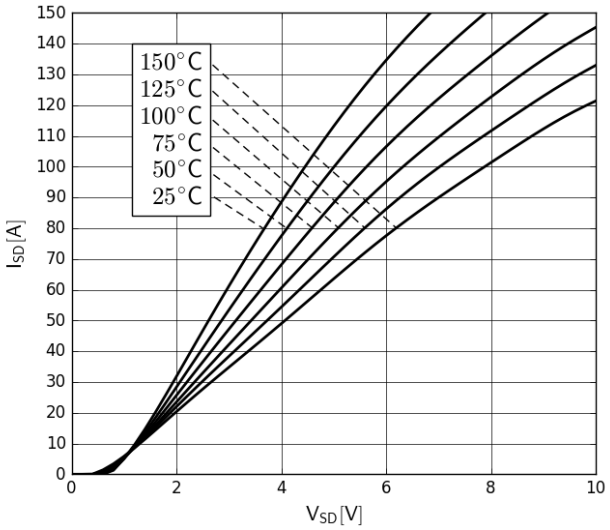


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

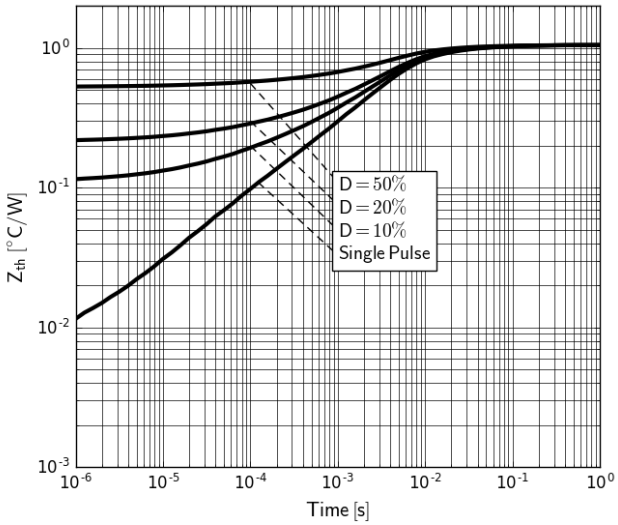


Figure 13. Transient Thermal Resistance

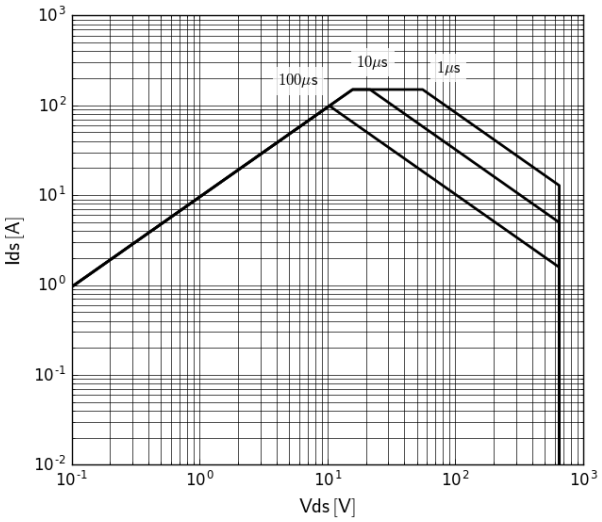


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

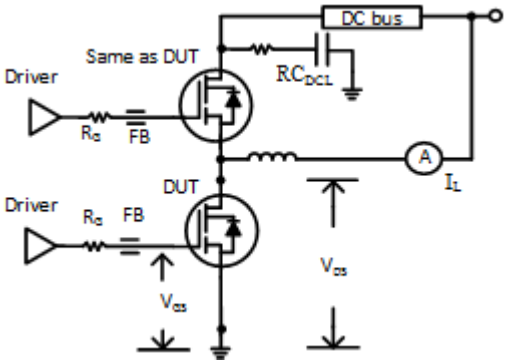


Figure 15. Switching Time Test Circuit

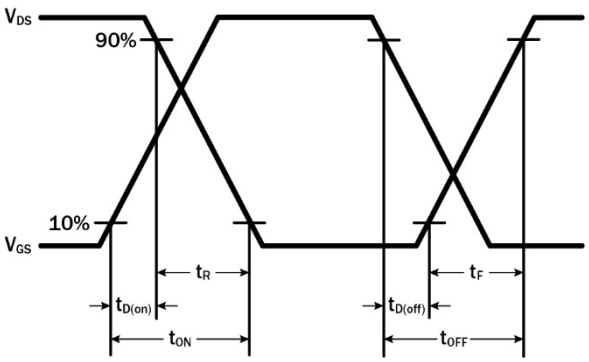


Figure 16. Switching Time Waveform

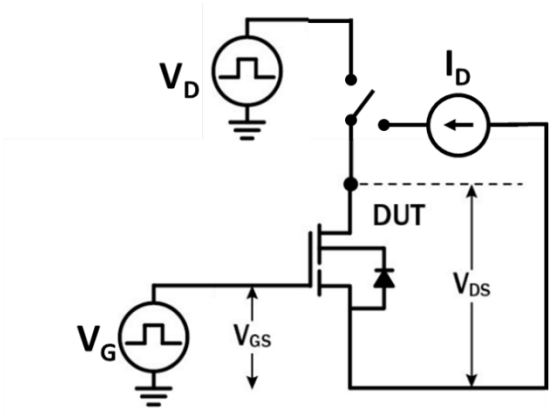


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

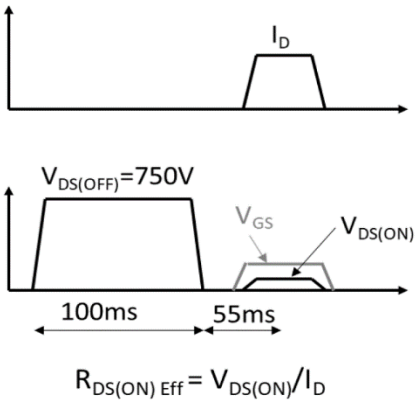
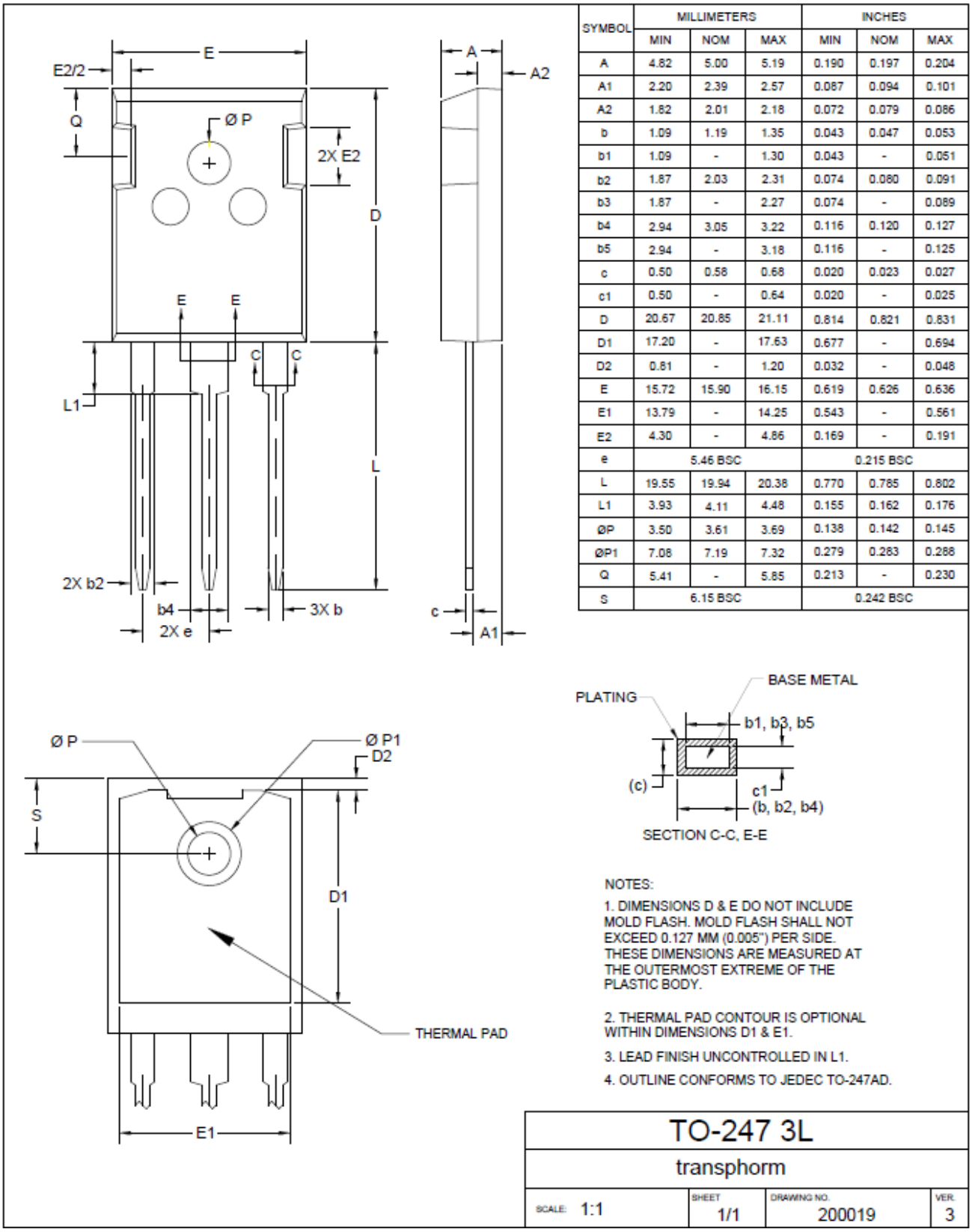


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.82	5.00	5.19	0.190	0.197	0.204
A1	2.20	2.39	2.57	0.087	0.094	0.101
A2	1.82	2.01	2.18	0.072	0.079	0.086
b	1.09	1.19	1.35	0.043	0.047	0.053
b1	1.09	-	1.30	0.043	-	0.051
b2	1.87	2.03	2.31	0.074	0.080	0.091
b3	1.87	-	2.27	0.074	-	0.089
b4	2.94	3.05	3.22	0.116	0.120	0.127
b5	2.94	-	3.18	0.116	-	0.125
c	0.50	0.58	0.68	0.020	0.023	0.027
c1	0.50	-	0.64	0.020	-	0.025
D	20.67	20.85	21.11	0.814	0.821	0.831
D1	17.20	-	17.63	0.677	-	0.694
D2	0.81	-	1.20	0.032	-	0.048
E	15.72	15.90	16.15	0.619	0.626	0.636
E1	13.79	-	14.25	0.543	-	0.561
E2	4.30	-	4.86	0.169	-	0.191
e	5.46 BSC			0.215 BSC		
L	19.55	19.94	20.38	0.770	0.785	0.802
L1	3.93	4.11	4.48	0.155	0.162	0.176
ØP	3.50	3.61	3.69	0.138	0.142	0.145
ØP1	7.08	7.19	7.32	0.279	0.283	0.288
Q	5.41	-	5.85	0.213	-	0.230
S	6.15 BSC			0.242 BSC		

NOTES:

1. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 MM (0.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
2. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS D1 & E1.
3. LEAD FINISH UNCONTROLLED IN L1.
4. OUTLINE CONFORMS TO JEDEC TO-247AD.

TO-247 3L			
transphorm			
SCALE: 1:1	SHEET 1/1	DRAWING NO. 200019	VER. 3

Figure 19. TO-247-3 Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H050G4WS	TO-247-3	Source tab

8. Revision History

Revision	Date	Description
2.00	Nov 26, 2025	Updated the document's formatting; no technical changes were completed.
1.00	Mar 6, 2022	Initial release.

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