

TP65H050G4QS

650V SuperGaN® FET in TOLL (source tab)

Description

The TP65H050G4QS 650V, 50mΩ gallium nitride (GaN) FET is a normally-off device using Renesas’s Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

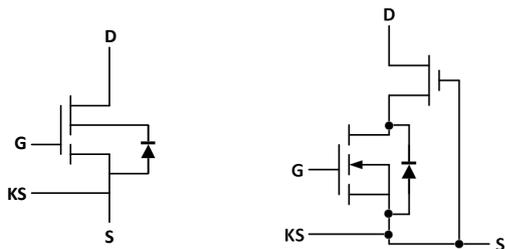
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

Product and Schematic Diagrams



TP65H050G4QS TOLL



Cascode Schematic Symbol

Cascode Device Structure

Features

- Ultra-fast switching Gen IV GaN technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Reduced crossover loss
- Negligible Q_{rr}
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- E-mobility charging
- PV inverter
- UPS
- BESS



Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	60
Q_{OSS} (nC) typical	120
Q_G (nC) typical	15.3

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)

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1. Pin Information

1.1 Pin Assignments

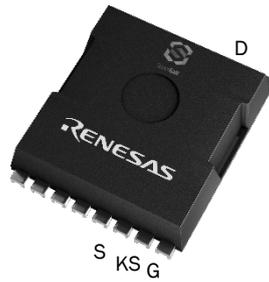


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Name	Description
D	Drain.
S	Source.
G	Gate.
KS	Kelvin source.

2. Specifications

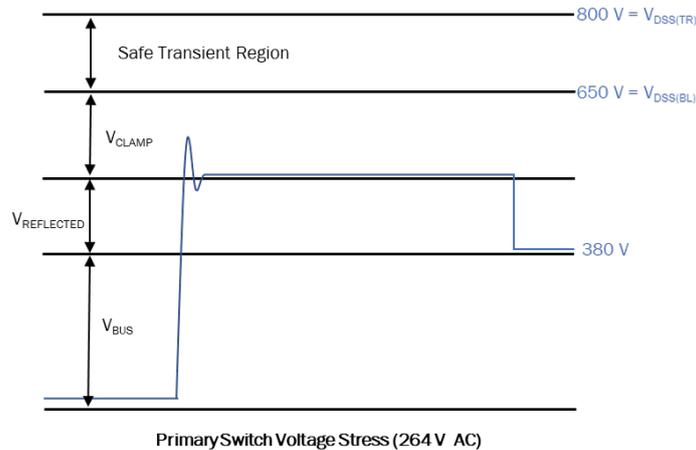
2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Limit Value	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650	V
$V_{DSS(TR)}$	Transient drain to source voltage ^[1]	800	
V_{GSS}	Gate to source voltage	+20	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$	119	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$	34	A
	Continuous drain current at $T_c = 100^\circ\text{C}$	22	A
I_{DM}	Pulsed drain current (pulse width: $10\mu\text{s}$)	150	A
T_J	Junction operating temperature	-55 to +150	$^\circ\text{C}$
T_S	Storage temperature	-55 to +150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature ^[2]	260	$^\circ\text{C}$

1. In off-state, spike duty cycle $D < 0.01$, spike duration $< 30\mu\text{s}$, non-repetitive.
2. For 10 sec., 1.6mm from the case.



2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	1.05	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient	45	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V _{DSS(BL)}	Maximum drain-source voltage	V _{GS} = 0V	650	-	-	V
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 0.7mA	3.3	4	4.8	V
ΔV _{GS(th)} /T _J	Gate threshold voltage temperature coefficient		-	-6.2	-	mV/°C
R _{DS(on)eff}	Drain-source on-resistance ^[1]	V _{GS} = 10V, I _D = 22A, T _J = 25°C	-	50	60	mΩ
		V _{GS} = 10V, I _D = 22A, T _J = 150°C	-	105	-	
I _{DSS}	Drain-to-source leakage current	V _{DS} = 650V, V _{GS} = 0V, T _J = 25°C	-	4	40	μA
		V _{DS} = 650V, V _{GS} = 0V, T _J = 150°C	-	15	-	
I _{GSS}	Gate-to-source forward leakage current	V _{GS} = 20V	-	-	100	nA
	Gate-to-source reverse leakage current	V _{GS} = -20V	-	-	-100	
C _{ISS}	Input capacitance	V _{GS} = 0V, V _{DS} = 400V, f = 1MHz	-	1000	-	pF
C _{OSS}	Output capacitance		-	110	-	
C _{RSS}	Reverse transfer capacitance		-	6	-	
C _{O(er)}	Output capacitance, energy related ^[2]	V _{GS} = 0V, V _{DS} = 0V to 400V	-	164	-	pF
C _{O(tr)}	Output capacitance, time related ^[3]		-	280	-	
Q _G	Total gate charge	V _{DS} = 400V, V _{GS} = 0V to 10V, I _D = 22A	-	15.3	-	nC
Q _{GS}	Gate-source charge		-	6	-	
Q _{GD}	Gate-drain charge		-	5	-	
Q _{OSS}	Output charge	V _{GS} = 0V, V _{DS} = 0V to 400V	-	120	-	nC
t _{D(on)}	Turn-on delay	V _{DS} = 400V, V _{GS} = 0V to 10V, I _D = 22A, R _G = 45Ω, Z _{FB} = 240Ω at 100MHz (see Figure 15)	-	49.2	-	ns
t _R	Rise time		-	11.3	-	
t _{D(off)}	Turn-off delay		-	88.3	-	
t _F	Fall time		-	10.9	-	

1. Dynamic R_{DS(on)}, 100% tested; see Figure 17 and Figure 18 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	$V_{GS} = 0V$, $T_C = 100^\circ\text{C}$, $\leq 25\%$ duty cycle	-	-	22	A
V_{SD}	Reverse voltage ^[1]	$V_{GS} = 0V$, $I_S = 22A$	-	2.2	-	V
		$V_{GS} = 0V$, $I_S = 11A$	-	1.6	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology.

3. Typical Performance Graphs

$T_c = 25^\circ\text{C}$ unless otherwise stated.

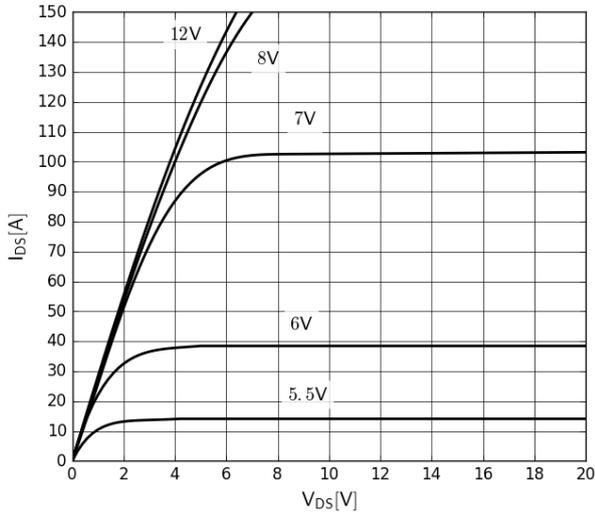


Figure 2. Typical Output Characteristics, $T_J = 25^\circ\text{C}$
Parameter: V_{GS}

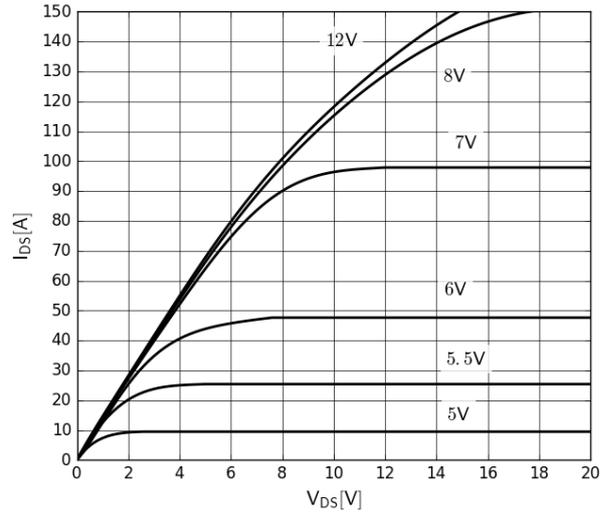


Figure 3. Typical Output Characteristics, $T_J = 150^\circ\text{C}$
Parameter: V_{GS}

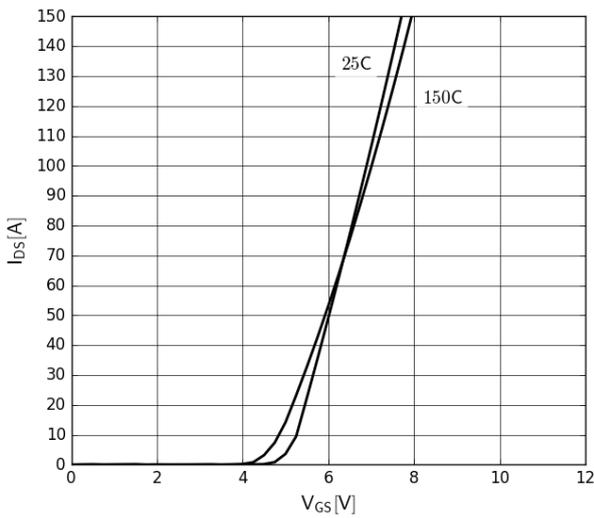


Figure 4. Typical Transfer Characteristics
 $V_{DS} = 20\text{V}$, Parameter: T_J

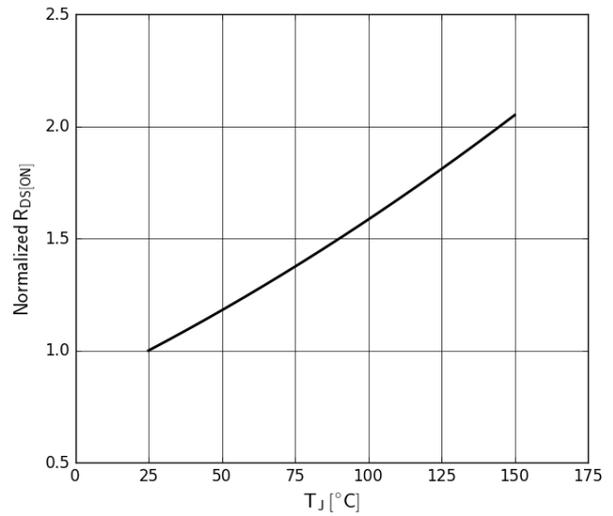


Figure 5. Normalized On-resistance
 $I_D = 22\text{A}$, $V_{GS} = 10\text{V}$

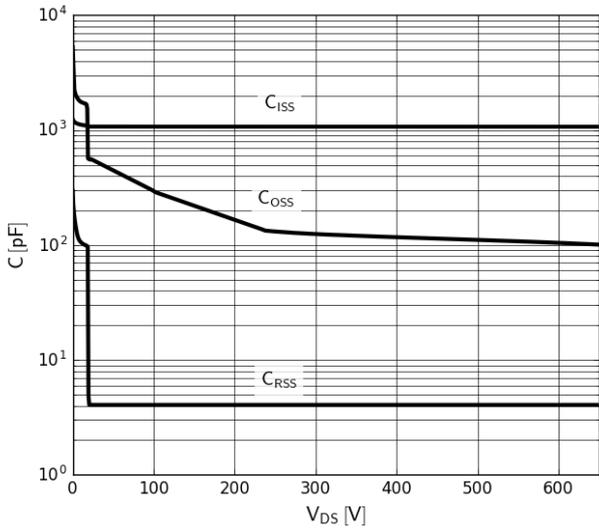


Figure 6. Typical Capacitance

V_{GS} = 0V, f = 1MHz

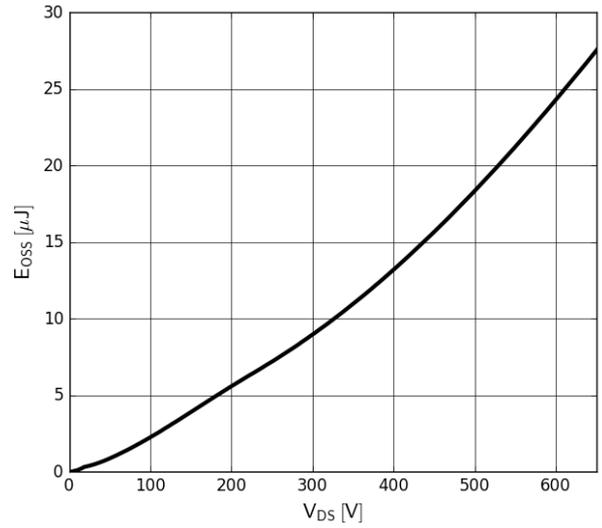


Figure 7. Typical C_{OSS} Stored Energy

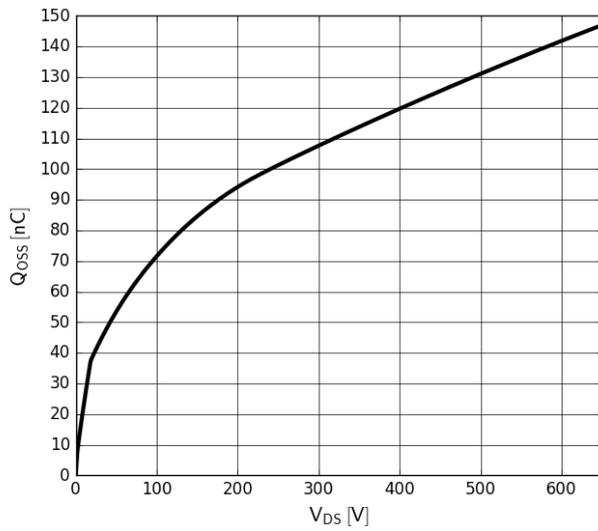


Figure 8. Typical Q_{OSS}

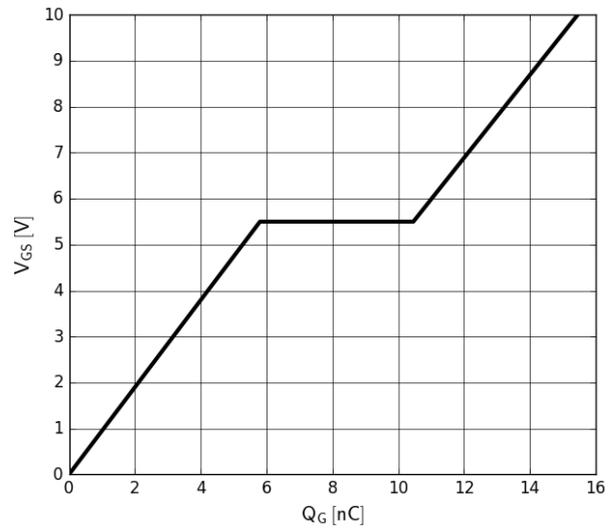


Figure 9. Typical Gate Charge

I_{DS} = 22A, V_{DS} = 400V

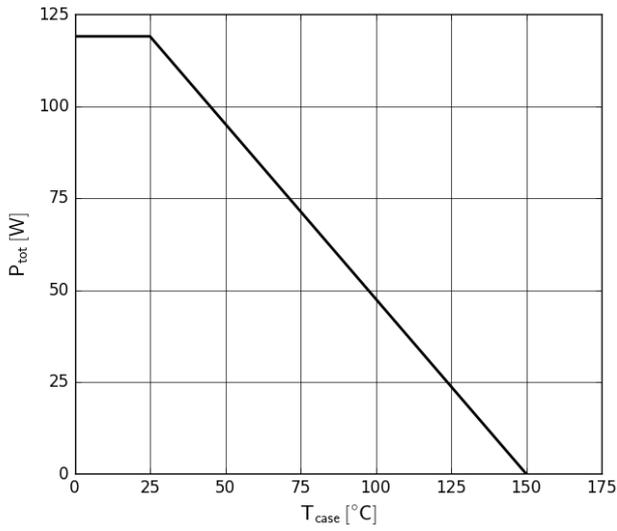


Figure 10. Power Dissipation

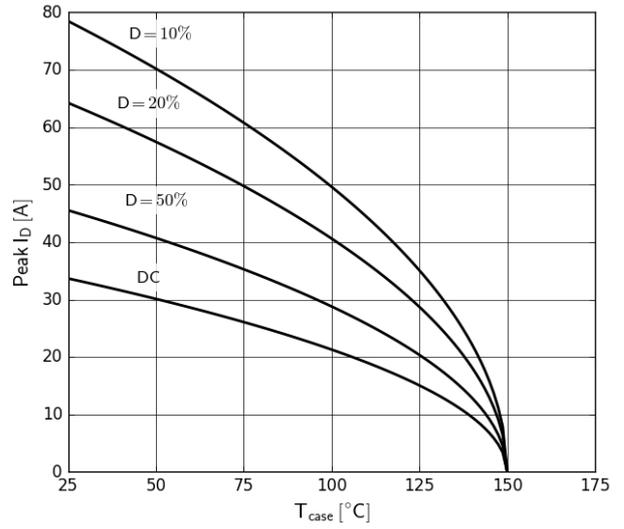


Figure 11. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 10V

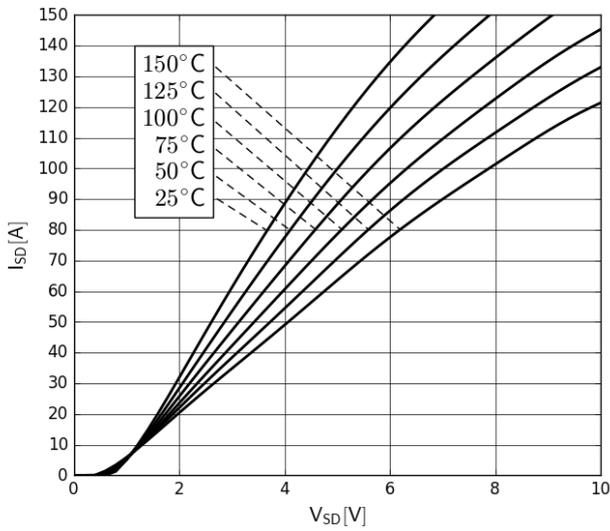


Figure 12. Forward Characteristics of Rev. Diode

I_S = f(V_{SD}), Parameter: T_J

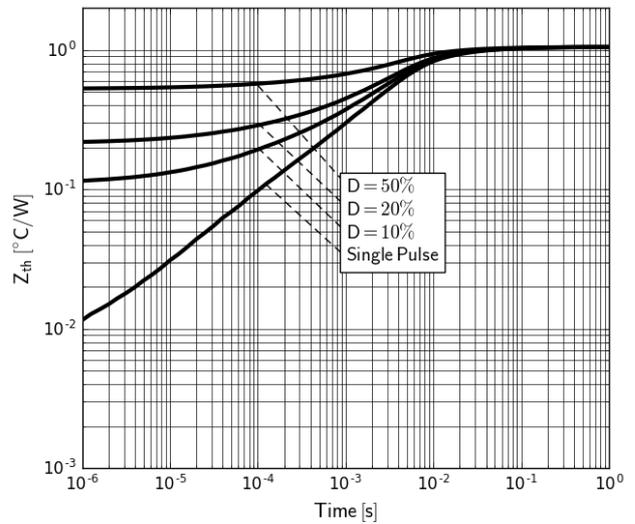


Figure 13. Transient Thermal Resistance

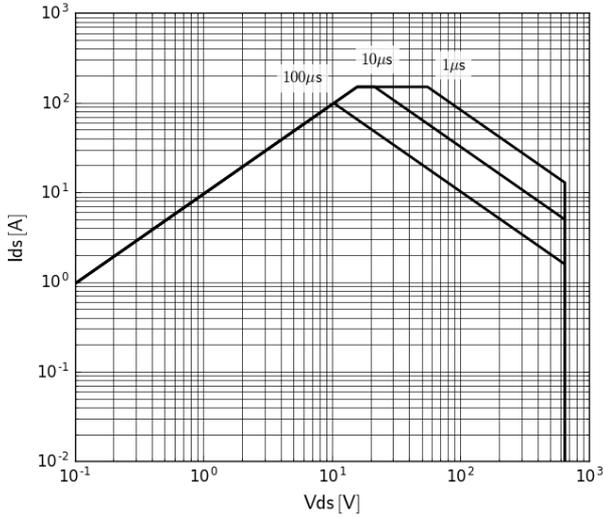


Figure 14. Safe Operating Area $T_c = 25^\circ\text{C}$

4. Test Circuits and Waveforms

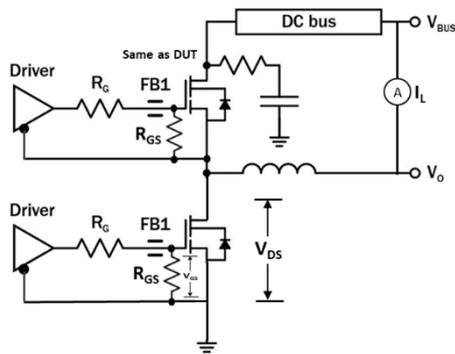


Figure 15. Switching Time Test Circuit

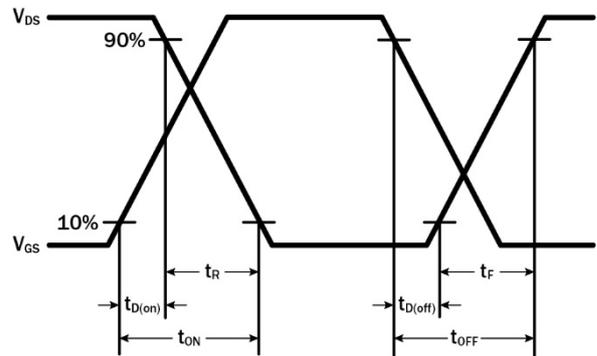


Figure 16. Switching Time Waveform

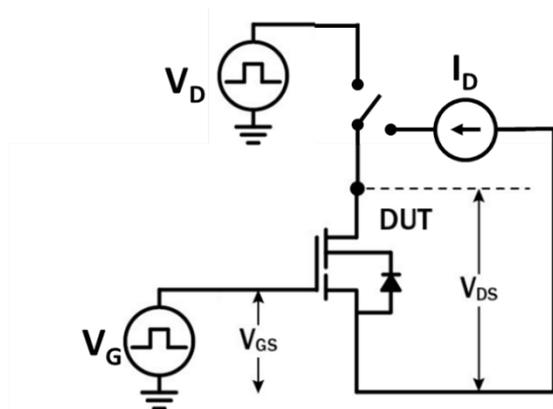


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

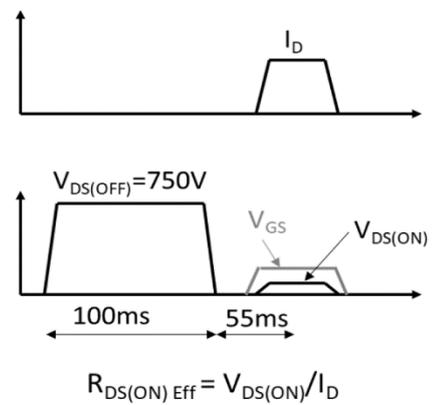


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings

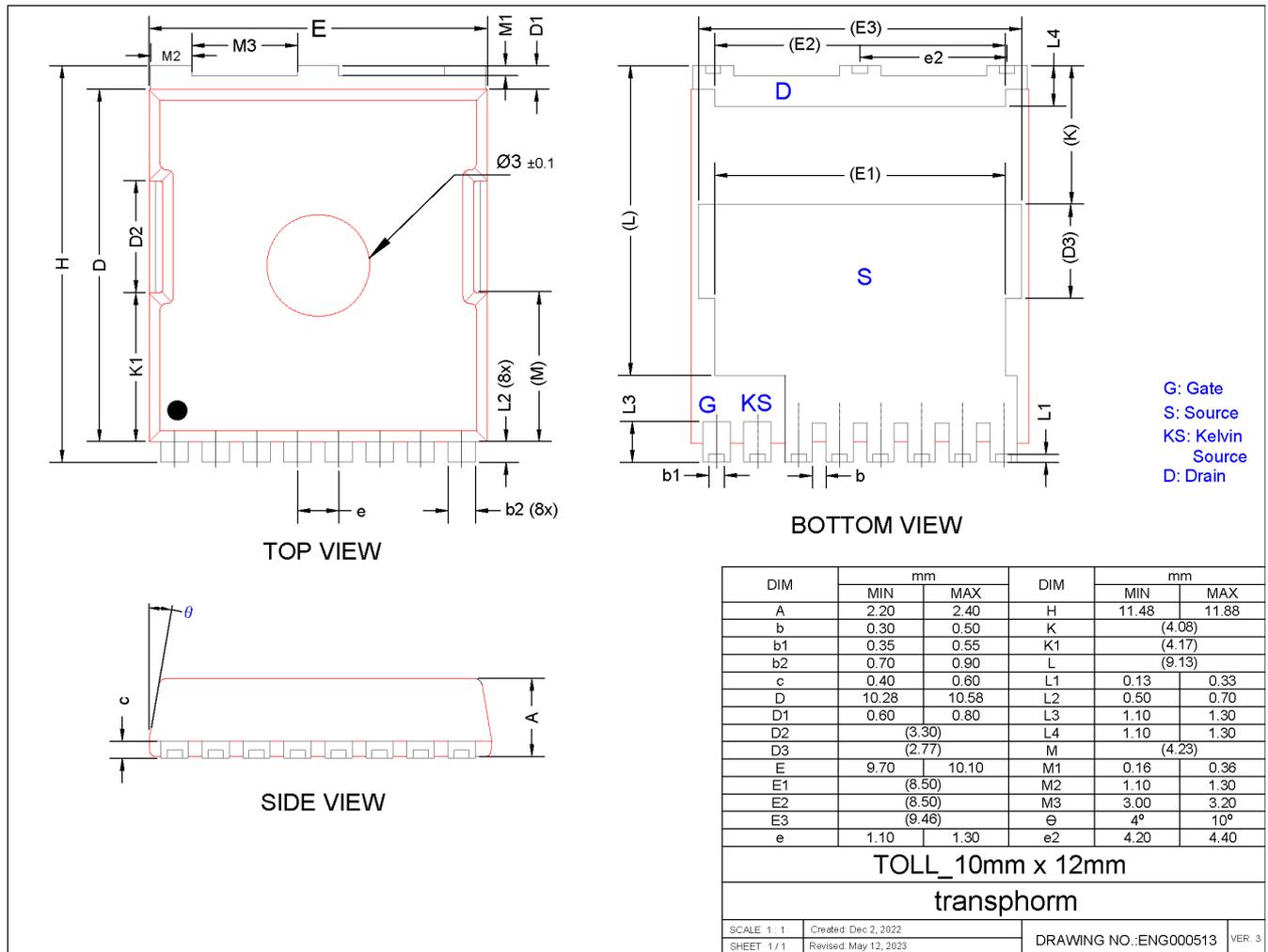


Figure 19. 10 × 12 mm TOLL Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the [GaN Power Solutions](#) page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H050G4QS	TOLL	Source tab

8. Revision History

Revision	Date	Description
2.00	Nov 26, 2025	Updated the document's formatting; no technical changes were completed.
1.00	Jan 5, 2024	Updated datasheet.

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