

TP65H030G4PRS

650V SuperGaN® GaN FET in TOLT (source tab)

Description

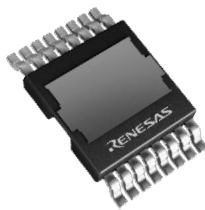
The TP65H030G4PRS 650V, 30mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV plus platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

The Gen IV plus SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

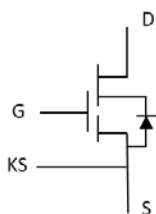
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

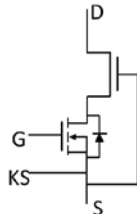
Product and Schematic Diagrams



TP65H030G4PRS TOLT



Cascode Schematic Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Reduced crossover loss
- Negligible Q_{rr}
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- E-mobility charging
- PV inverter
- UPS
- BESS



Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	37
Q_{OSS} (nC) typical	135
Q_G (nC) typical	24.5

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)

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1. Pin Information

1.1 Pin Assignments

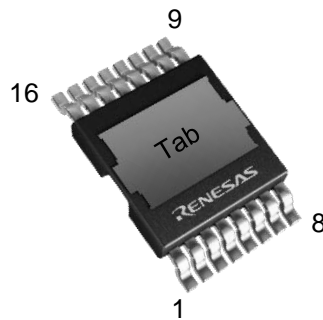


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4, 5, 6, 7, 8	D	Drain.
9	G	Gate.
10	KS	Kelvin Source.
11, 12, 13, 14, 15, 16	S	Source.
Tab	S	Source.

2. Specifications

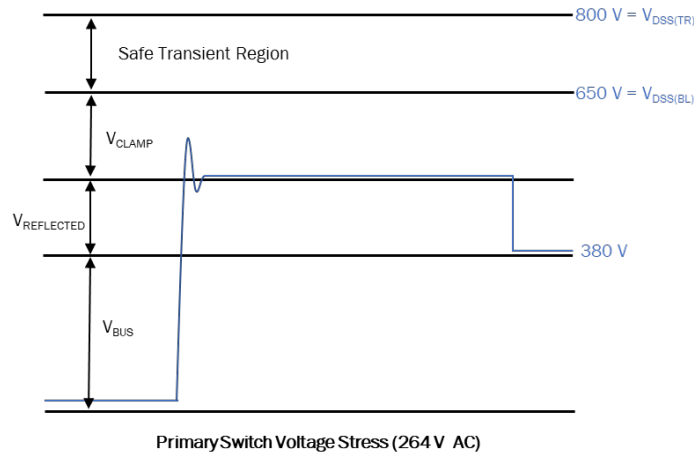
2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	-	650	V
$V_{DSS(TR)}$	Transient drain to source voltage ^[1]	-	800	
$V_{DSS(TR), \text{pulsed}}$	Drain to source voltage, pulsed ^[2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$	-	192	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$	-	55.7	A
	Continuous drain current at $T_c = 100^\circ\text{C}$	-	35	A
I_{DM}	Pulsed drain current (pulse width: 10 μs)	-	230	A
T_J	Operating temperature junction	-55	+150	$^\circ\text{C}$
T_S	Storage temperature	-55	+150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature ^[3]	-	260	$^\circ\text{C}$

- $V_{GS} = 0\text{V}$, $\leq 10\mu\text{s}$, $\leq 1\%$ Duty Cycle, cumulative 60s (60 million pulses).
- $V_{GS} = 0\text{V}$, $\leq 1\mu\text{s}$, $\leq 1\%$ Duty Cycle, cumulative 10h (36 billion pulses).
- Reflow MSL3.



2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	0.65	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient	40	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V _{DSS(BL)}	Maximum drain-source voltage	V _{GS} = 0V	650	-	-	V
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 1mA	3.3	4	4.8	V
ΔV _{GS(th)} /T _J	Gate threshold voltage temperature coefficient		-	-6.5	-	mV/°C
R _{DS(on)eff}	Drain-source on-resistance ^[1]	V _{GS} = 12V, I _D = 30A, T _J = 25°C	-	30	37	mΩ
		V _{GS} = 12V, I _D = 30A, T _J = 150°C	-	62	-	
I _{DSS}	Drain-to-source leakage current	V _{DS} = 650V, V _{GS} = 0V, T _J = 25°C	-	3	30	μA
		V _{DS} = 650V, V _{GS} = 0V, T _J = 150°C	-	20	-	
I _{GSS}	Gate-to-source forward leakage current	V _{GS} = 20V	-	-	400	nA
	Gate-to-source reverse leakage current	V _{GS} = -20V	-	-	-400	
C _{ISS}	Input capacitance	V _{GS} = 0V, V _{DS} = 400V, f = 1MHz	-	1500	-	pF
C _{OSS}	Output capacitance		-	127	-	
C _{RSS}	Reverse transfer capacitance		-	4.6	-	
C _{O(er)}	Output capacitance, energy related ^[2]	V _{GS} = 0V, V _{DS} = 0V to 400V	-	183	-	pF
C _{O(tr)}	Output capacitance, time related ^[3]		-	339	-	
Q _G	Total gate charge	V _{DS} = 400V, V _{GS} = 0V to 12V, I _D = 30A	-	24.5	-	nC
Q _{GS}	Gate-source charge		-	8.4	-	
Q _{GD}	Gate-drain charge		-	6.6	-	
Q _{OSS}	Output charge	V _{GS} = 0V, V _{DS} = 0V to 400V	-	135	-	nC
t _{D(on)}	Turn-on delay	V _{DS} = 400V, V _{GS} = 0V to 12V, R _{G(on)} = 10Ω, R _{G(off)} = 30Ω, I _D = 30A, Z _{FB} = 180Ω at 100MHz (see Figure 15)	-	26.4	-	ns
t _R	Rise time		-	6.4	-	
t _{D(off)}	Turn-off delay		-	63.6	-	
t _F	Fall time		-	5.2	-	

1. Dynamic R_{DS(on)}, 100% tested; see Figure 17 and Figure 18 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	$V_{GS} = 0V$, $T_C = 100^\circ\text{C}$, $\leq 25\%$ duty cycle	-	-	32	A
V_{SD}	Reverse voltage ^[1]	$V_{GS} = 0V$, $I_S = 32A$	-	1.8	-	V
		$V_{GS} = 0V$, $I_S = 16A$	-	1.3	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology

3. Typical Performance Graphs

$T_c = 25^\circ\text{C}$ unless otherwise stated.

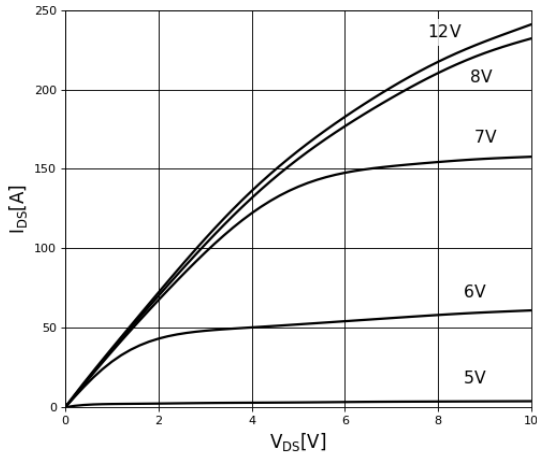


Figure 2. Typical Output Characteristics, $T_J = 25^\circ\text{C}$
Parameter: V_{GS}

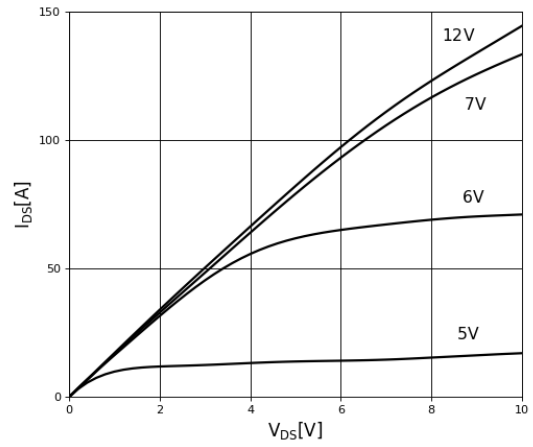


Figure 3. Typical Output Characteristics, $T_J = 150^\circ\text{C}$
Parameter: V_{GS}

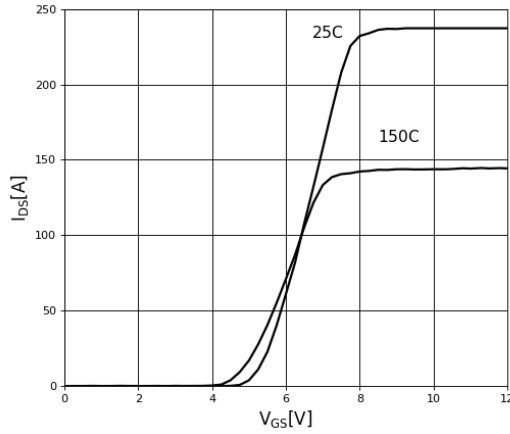


Figure 4. Typical Transfer Characteristics
 $V_{DS} = 10\text{V}$, Parameter: T_J

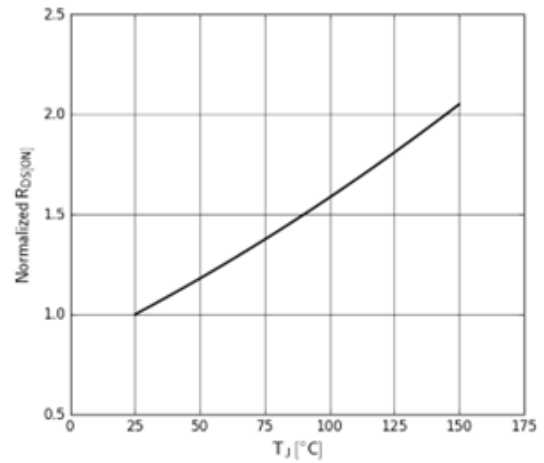


Figure 5. Normalized On-resistance
 $I_D = 30\text{A}$, $V_{GS} = 12\text{V}$

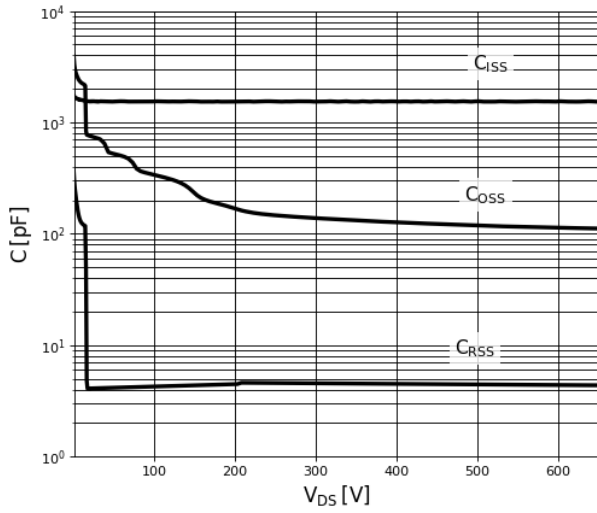


Figure 6. Typical Capacitance
 $V_{GS} = 0V, f = 1MHz$

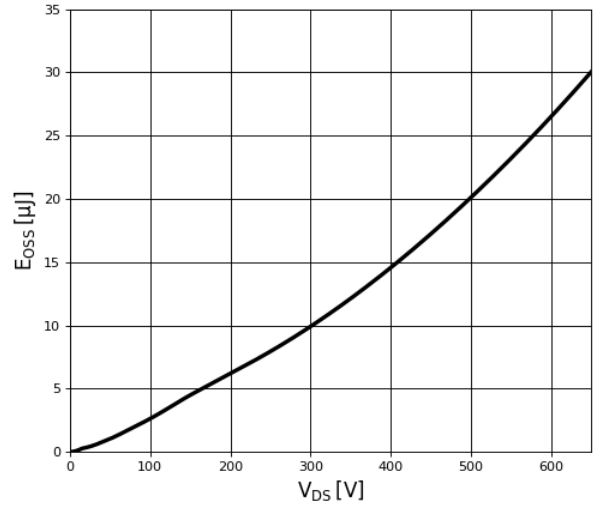


Figure 7. Typical Coss Stored Energy

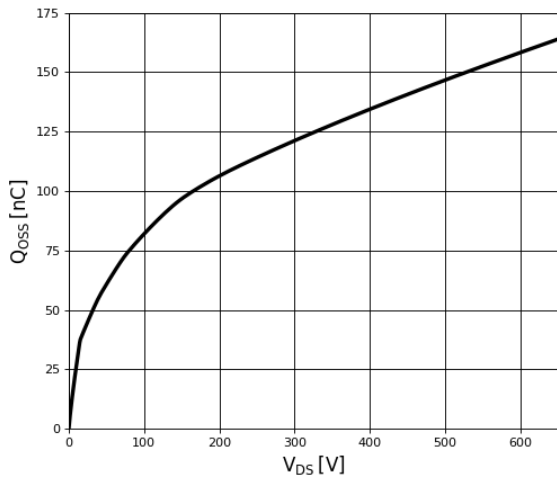


Figure 8. Typical Qoss

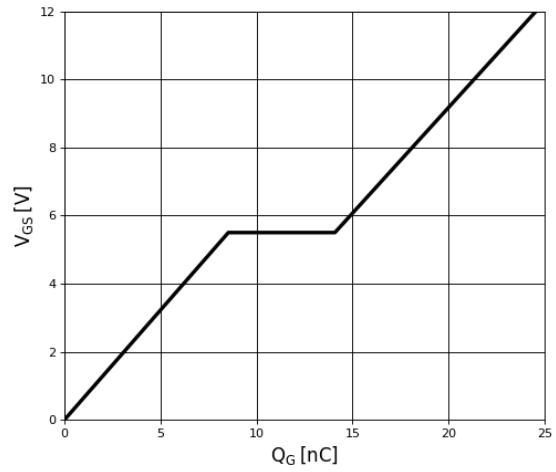


Figure 9. Typical Gate Charge
 $I_{DS} = 30A, V_{DS} = 400V$

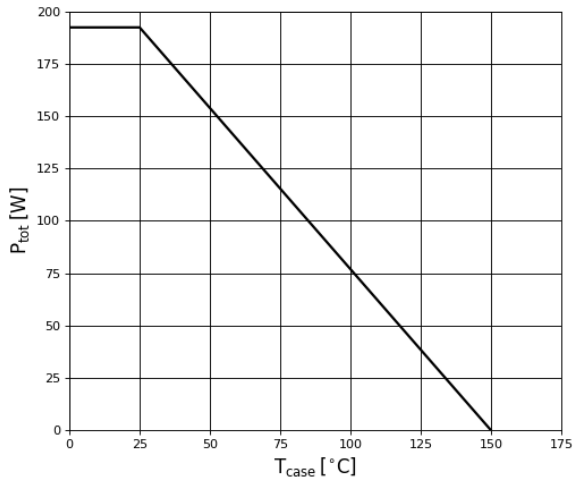


Figure 10. Power Dissipation

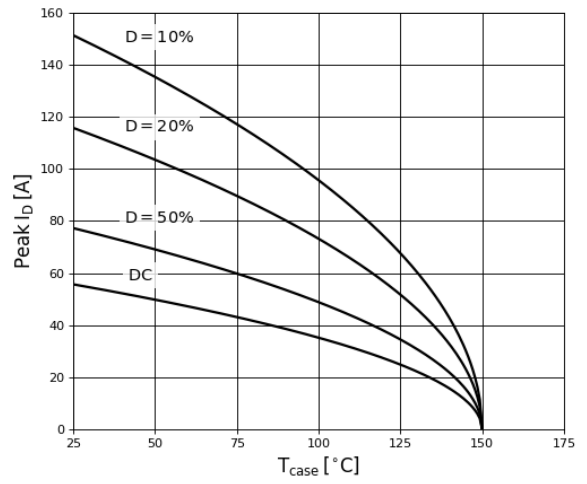


Figure 11. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 12V

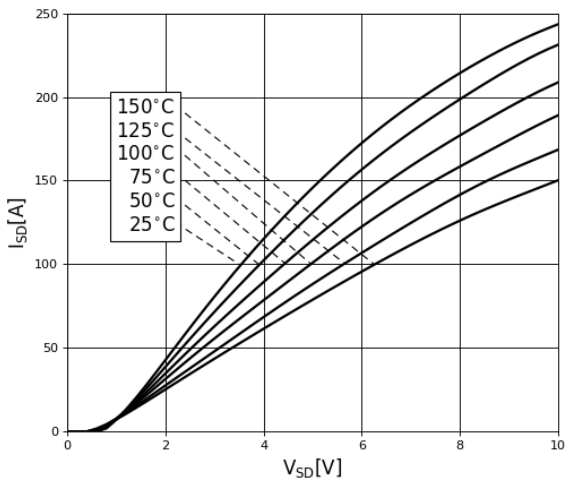


Figure 12. Forward Characteristics of Rev. Diode

I_S = f(V_{SD}), Parameter: T_J

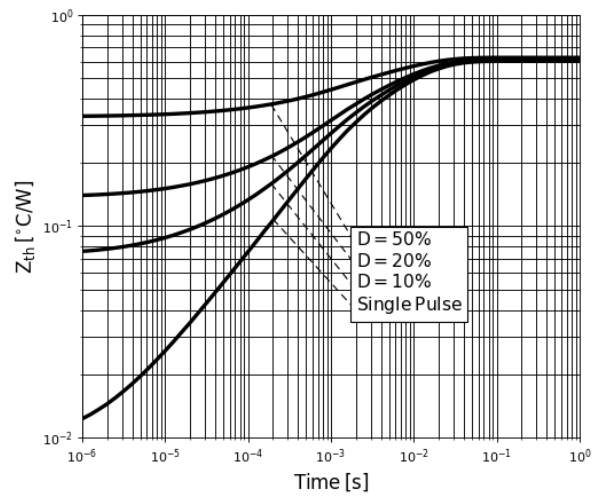


Figure 13. Transient Thermal Resistance

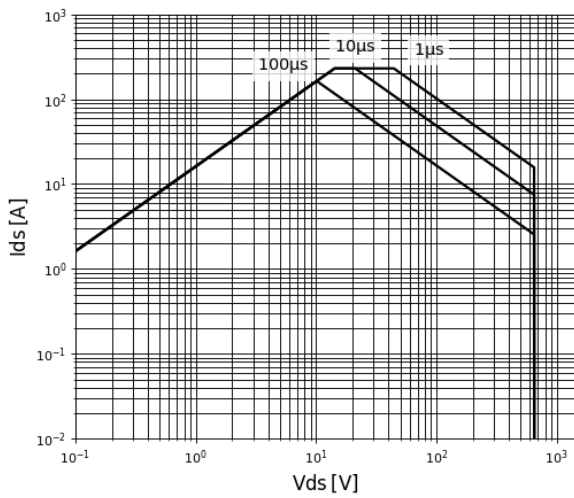


Figure 14. Safe Operating Area T_c = 25°C

4. Test Circuits and Waveforms

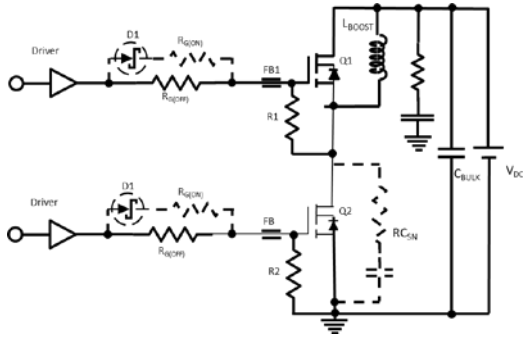


Figure 15. Switching Time Test Circuit

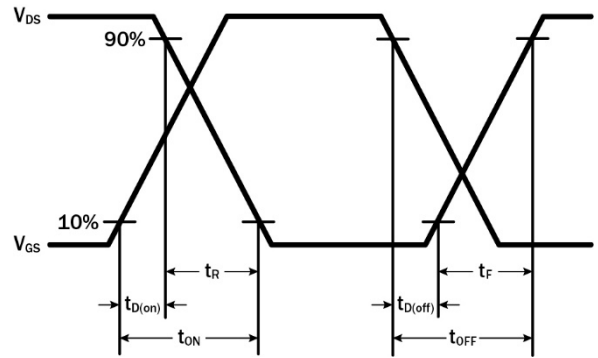


Figure 16. Switching Time Waveform

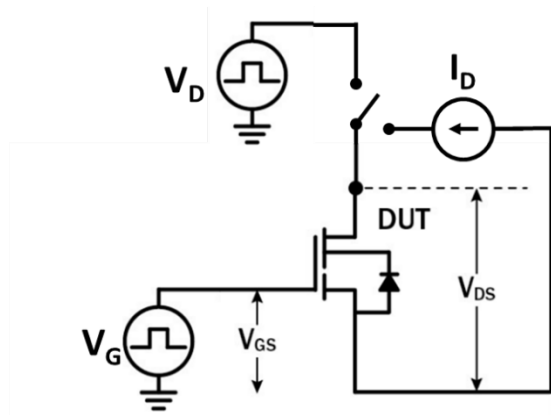


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

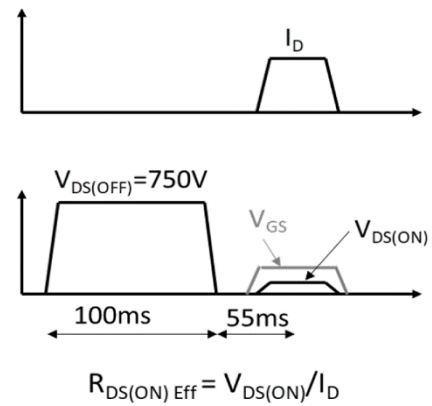


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



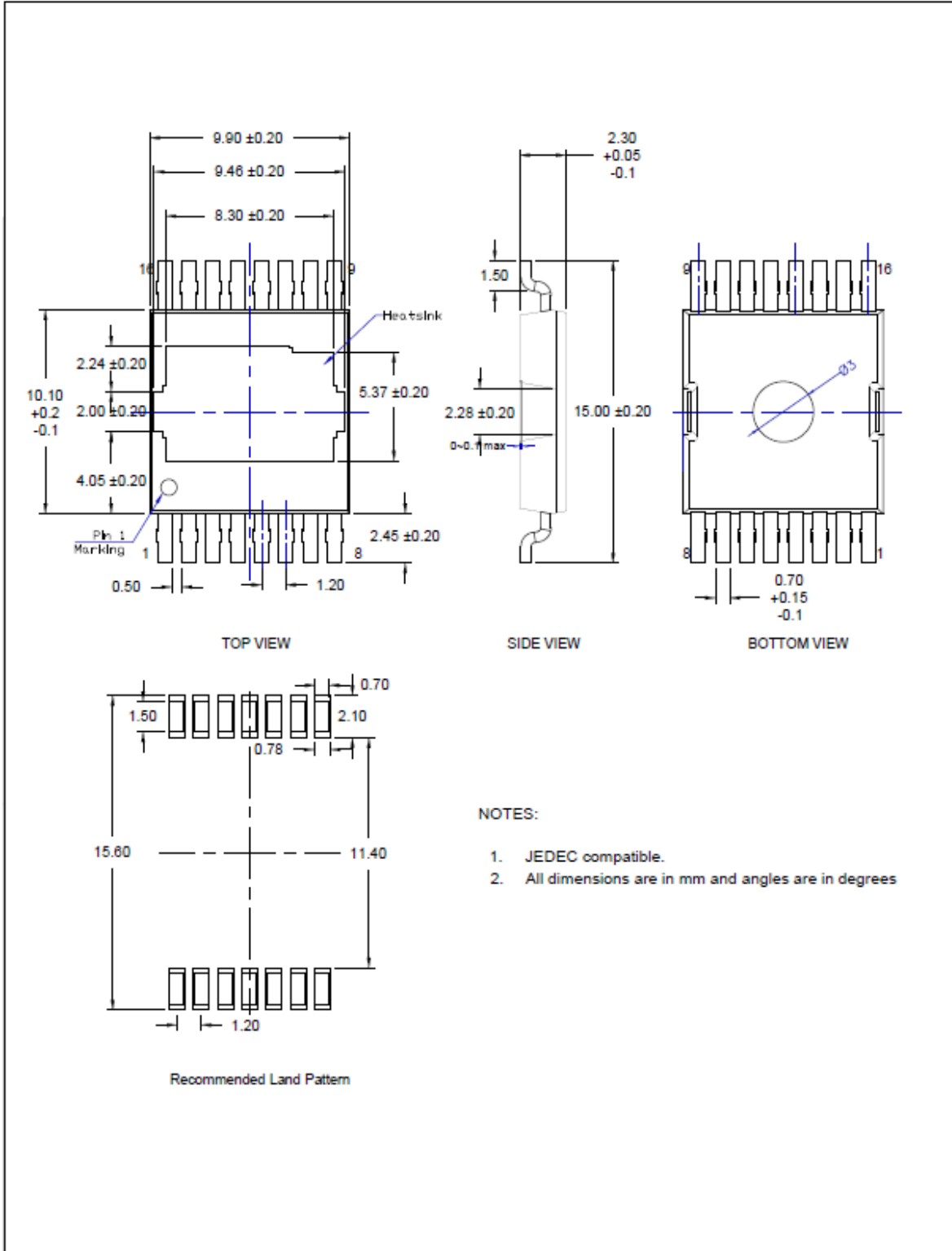
Package Outline Drawing

PSC-5184-01

TN0016AA

16-TOLT 10.1 x 9.9 x 2.3 mm Body, 1.2 mm Pitch (ePad Top Side: 8.3 x 5.37 mm)

Rev.00, Sep 16, 2025



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Figure 19. 16-TOLT 10.1 x 9.9 mm Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the [GaN Power Solutions](#) page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H030G4PRS	TOLT	Source tab

8. Revision History

Revision	Date	Description
2.02	Jun 29, 2026	Updated maximum Rds(on) specification and transient voltage test conditions.
2.01	Dec 2, 2025	Updated the document's formatting; no technical changes were completed.
2.00	Nov 6, 2025	Final release
1.01	Jul 10, 2025	Revision update
1.00	Jun 25, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
TP65H030G4PRS	16	TOLT	TN0016AA/PSC-5184-01

A.2 Symbol Pin Information

A.2.1 16-TOLT

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	D	Passive	-
2	D	Passive	-
3	D	Passive	-
4	D	Passive	-
5	D	Passive	-
6	D	Passive	-
7	D	Passive	-
8	D	Passive	-
9	G	Passive	-
10	KS	Passive	-
11	S	Passive	-
12	S	Passive	-
13	S	Passive	-
14	S	Passive	-
15	S	Passive	-
16	S	Passive	-

A.3 Symbol Parameters

Orderable Part Number	Qualification	Mounting Type	Min Operating Temperature	Max Operating Temperature	Max Power Dissipation	Gate Charge (Qg)	RoHS	Rds(on) Max	Drain-to-Source Voltage (Vdss)	Continuous Drain Current (Id)
TP65H030G4PRS	Industrial	SMD	-40 °C	150 °C	192 W	24.5 nC	Compliant	41 mΩ	650 V	55.7 A

A.4 Footprint Design Information

A.4.1 16-TOLT

IPC Footprint Type	Package Code/ POD number	Number of Pins
SOP	TN0016AA/PSC-5184-01	16

Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	14.80	<p>Bottom View</p> <p>Side View</p>
Maximum lead span (horizontal side)	Hmax	15.20	
Minimum body span (pin1 side)	Dmin	9.70	
Maximum body span (pin1 side)	Dmax	10.10	
Minimum body span	Emin	10.00	
Maximum body span	Emax	10.30	
Minimum Lead Width	Bmin	0.60	
Maximum Lead Width	Bmax	0.85	
Minimum Lead Length	Lmin	1.50	
Maximum Lead Length	Lmax	1.50	
Maximum Height	Amax	2.35	
Minimum Standoff Height	A1min	0.01	
Minimum Lead Thickness	cmin	0.50	
Maximum Lead Thickness	cmax	0.50	
Total number of pin positions (including absent pins)	PinCount	16	
Distance between the center of any two adjacent pins	Pitch	1.20	
Minimum thermal pad size (pin1 side)	D2min	8.10	
Maximum thermal pad size (pin1 side)	D2max	8.50	
Minimum thermal pad size	E2min	5.17	
Maximum thermal pad size	E2max	5.57	

Recommended Land Pattern			Diagram
Description	Dimension	Value (mm)	<p>PCB Top View</p>
Distance between left pad toe to right pad toe	Z	15.60	
Distance between left pad heel to right pad heel	G	11.40	
Row spacing. Distance between pad centers	C	13.50	
Pad Width	X	0.78	
Pad Length	Y	2.10	

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