TP65B110HRU

650V Bi-Directional Switch (BDS) in TOLT

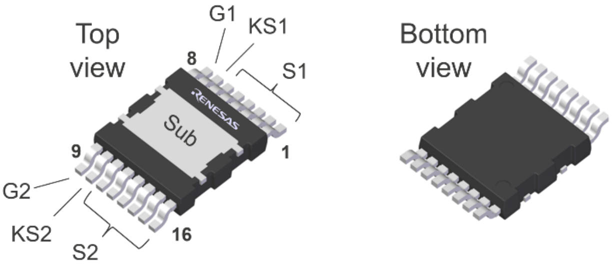
Description

The TP65B110HRU is a 650V 110mΩ common-drain Bi-Directional Switch (BDS) based on Renesas' SuperGaN® Bi-Directional platform. It conducts and blocks current in both directions with smallest footprint and a best-in-class switching figure of merit. The product combines a bidirectional, high-voltage, depletion-mode GaN with two normally-off low-voltage silicon MOSFETs to provide superior performance, with high threshold for standard gate-drive compatibility, easy integration, and robust reliability for advanced power applications.

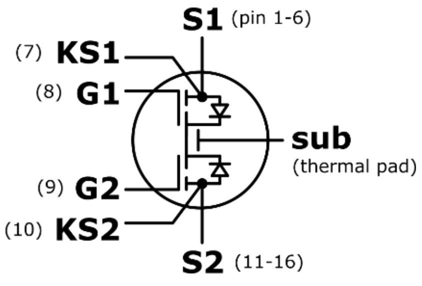
Benefits

- Ultra-fast switching for high efficiency, high power-density converters
- Smaller footprint and lower cost versus back-to-back unidirectional switches
- High noise immunity and easy to drive, with no negative voltage required
- Reliable under the widest range of operating conditions, including AC and DC
- Facilitates cost-effective GaN adoption, reducing system size, weight, and costs

Product Diagrams



TP65B110HRU TOLT



Symbol

Features

- Insulated gate with high threshold
- Built-in freewheeling diode with low voltage drop
- Negligible reverse recovery charge
- Low Qg and low Q_{OSS}
- High dv/dt immunity
- Soft- and hard-switching capability
- Transient over-voltage capability
- DC bias withstand capability
- 2kV ESD capability (HBM and CDM)
- JEDEC qualified
- RoHS compliant and Halogen-free packaging

Applications

- PV inverters
- Battery chargers
- Motor drives
- AI datacenter and telecom power supplies
- UPS

Specifications

V_{SS} (V)	±650
$V_{SS(TR)}$ (V)	±800
$V_{GS(TH)}$ (V)	3
$R_{SS(on)}$ (mΩ) typical	110
Q_{OSS} (nC) typical	54
Q_G (nC) typical	6.8

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1. Pin Information

1.1 Pin Assignments

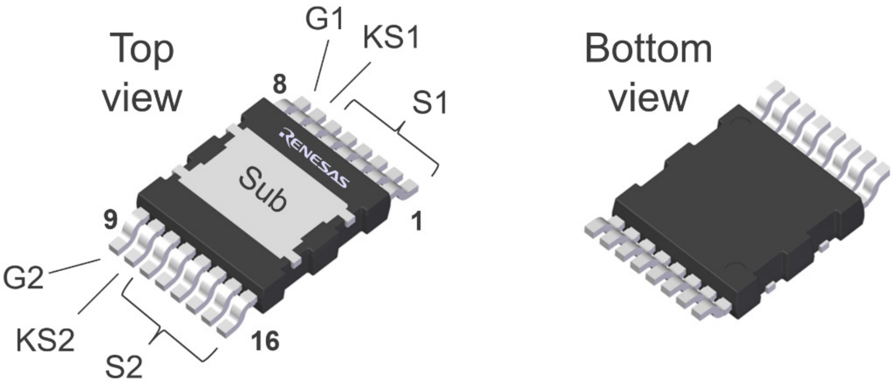


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1–6	S1	Source 1
7	KS1	Kelvin Source 1
8	G1	Gate 1
9	G2	Gate 2
10	KS2	Kelvin Source 2
11–16	S2	Source 2
Tab	Sub	GaN HEMT Substrate (Thermal path)

2. Specifications

2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter		Limit Value	Unit
$V_{SS(AC)}$	Off-state Continuous AC Voltage between S1 and S2 (T_J = -55°C to 150°C)		650	Vpk
$V_{SS(DC)}$	Off-state Continuous DC Voltage between S1 and S2 (T_J = -55°C to 150°C)		±650	V
$V_{SS(TR)}$	Off-state Transient Voltage between S1 and S2 [1]		±800	
$V_{GS,max}$	Continuous Gate to Source Voltage		±12	
$V_{GS,max\ (TR)}$	Transient Gate to Source Voltage		±20	
P_D	Maximum Power Dissipation at T_C = 25°C		156	W
I_{SS}	Continuous Source Current at T_C = 25°C [2]		±24	A
	Continuous Source Current at T_C = 100°C [2]		±15	
I_{SSM}	Pulsed Source Current (pulse width: 10µs)		±110	
T_C	Operating Temperature Junction	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage Temperature		-55 to +150	°C
T_{SOLD}	Reflow Soldering Temperature [3]		260	°C

1. < 10µs events, 60s cumulative.
2. Both gates on.
3. Reflow MSL3.

2.2 Thermal Specifications

Symbol	Parameter	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	0.8	°C/W
$R_{\Theta JA}$	Junction-to-ambient	50	

2.3 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$V_{GS,off}$	Off-State Gate Voltage	-	0	0	V
$V_{GS,on}$	On-State Gate Voltage	7	9	-	

2.4 Gate Characteristics

T_J = 25°C, Opposite gate on at 9V, unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{GS(th)}$	Gate Threshold Voltage	I_{SS} = 0.5mA	2.6	3	3.4	V
$\Delta V_{GS(th)}/T_j$	Threshold Voltage Temperature Coefficient	I_{SS} = 0.5mA	-	-4	-	mV/°C
gm	Gate Transconductance	V_{SS} = 20V, I_{SS} = 10A	-	35	-	S
Q_G	Total Gate Charge	V_{GS} = 0V to 7V V_{SS} = 400V I_{SS} = 5A	-	6.8	-	nC
Q_{GS}	Gate-Source Charge		-	3	-	
Q_{GD}	Gate-Drain Charge		-	1.5	-	
I_G	Gate-to-Source Leakage Current	V_{GS} = 9V	-	0.1	1	µA
		V_{GS} = -9V	-	0.1	1	
		V_{GS} = 20V	-	6	-	
		V_{GS} = -20V	-	6	-	
$R_{G,int}$	Internal Gate Resistor	-	-	1.8	-	Ω

2.5 On-State Characteristics

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$R_{SS,on}$	On-State Resistance between S1 and S2	Both gates on (V_{G1S1} = 9V, V_{G2S2} = 9V) I_{SS} = 10A	-	110	140	mΩ
		Both gates on (V_{G1S1} = 9V, V_{G2S2} = 9V) I_{SS} = 10A, T_J = 150°C	-	230	-	mΩ

2.6 Off-State Characteristics

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$I_{SS,OFF}$	Off-State Source Leakage Current	V_{SS} = ±650V V_{G1S1} = 0V, V_{G2S2} = 0V	-	±2	±20	µA
		V_{SS} = ±650V V_{G1S1} = 0V, V_{G2S2} = 0V T_J = 150°C	-	±20	-	µA

2.7 Dynamic Characteristics

T_J = 25°C, G1 blocking, unless otherwise stated.

Symbol	Parameter	Test Conditions	G2 On (V_{G2S2} = 9V) Typical	G2 Off (V_{G2S2} = 0V) Typical	Unit
C_{ISS}	Input Capacitance	V_{G1S1} = 0V V_{S2S1} = 400V f = 1MHz	810	777	pF
C_{OSS}	Output Capacitance		63	65	
C_{RSS}	Reverse Transfer Capacitance		0.9	0.7	
$C_{O(er)}$	Output Capacitance, Energy Related [1]	V_{G1S1} = 0V V_{S2S1} = 0V to 400V	80	81	pF
$C_{O(tr)}$	Output Capacitance, Time Related [2]		156	134	
Q_{OSS}	Output Charge	V_{G1S1} = 0V V_{S2S1} = 0V to 400V	62	54	nC
$t_{D(on)}$	Turn-on Delay	V_{G1S1} = 0 to 9V V_{S2S1} = 400 I_{S2S1} = 5A $R_{g,on}$ = 27Ω $R_{g,off}$ = 3.3Ω	23.5	-	ns
t_R	Rise Time		2.6	-	
$t_{D(off)}$	Turn-off Delay		19.2	-	
t_F	Fall Time		15.4	-	

1. Equivalent capacitance to give same stored energy from 0V to 400V.
2. Equivalent capacitance to give same charging time from 0V to 400V.

2.8 Diode Characteristics

T_J = 25°C unless otherwise stated.

Symbol	Parameter [1]	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{SS,FW}$	Free-Wheeling Voltage Drop	G1 off (V_{G1S1} = 0V) G2 on (V_{G2S2} = 9V) I_{S1S2} = 10A	-	1.9	-	V

1. Negligible reverse recovery charge due to low-voltage Silicon MOSFET technology.

3. Typical Characteristics

T_C = 25°C unless otherwise stated.

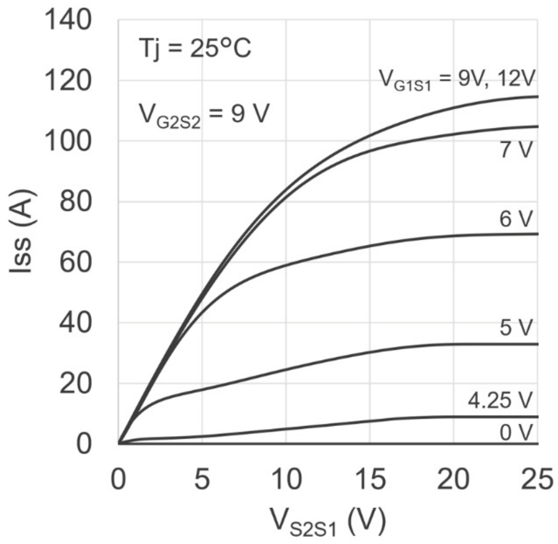


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{G1S1}

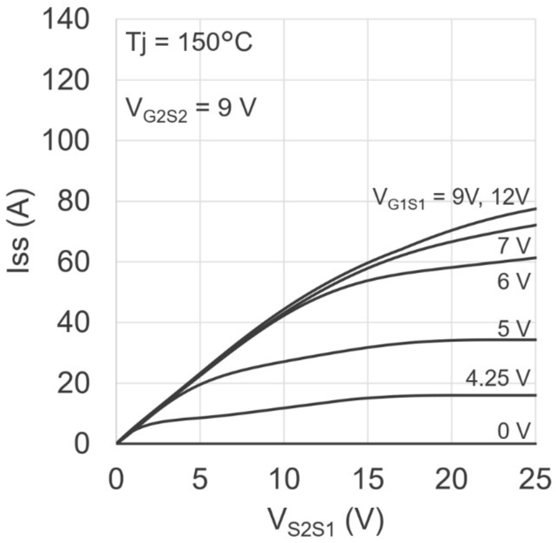


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{G1S1}

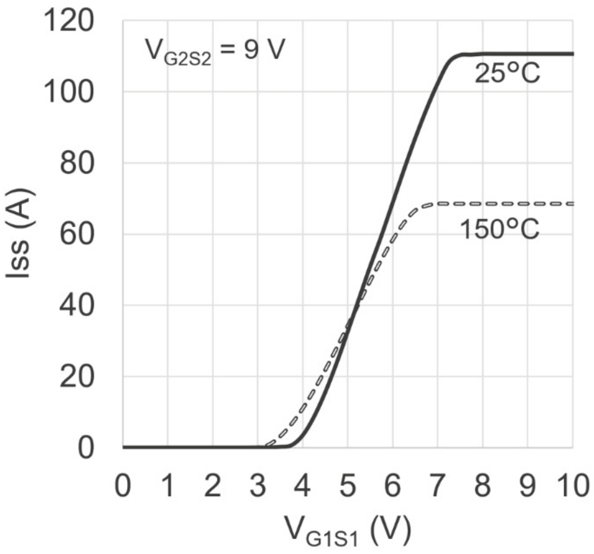


Figure 4. Typical Transfer Characteristics,

Parameter: T_J

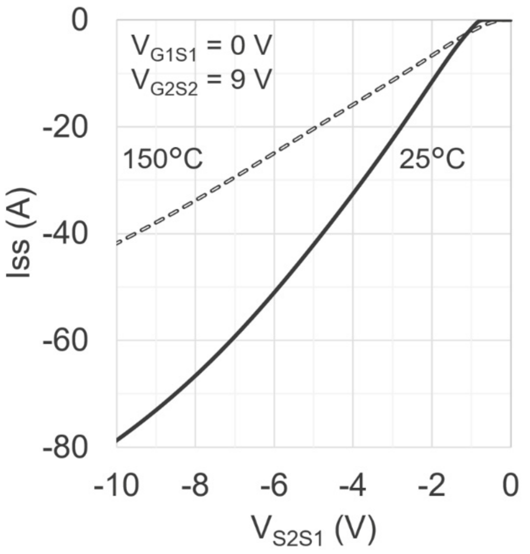


Figure 5. Typical Reverse Conduction Characteristics,

Parameter: T_J

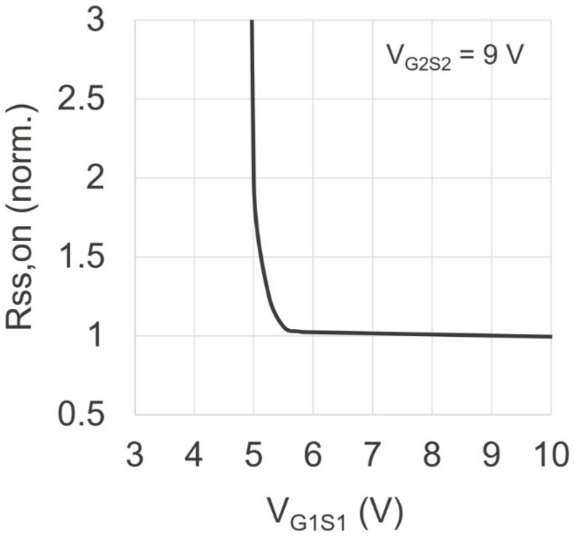


Figure 6. Typical On-State Resistance vs Gate-Source Voltage

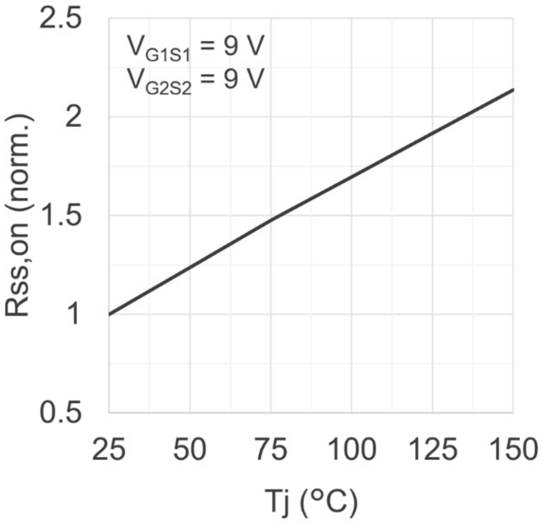


Figure 7. Typical On-State Resistance vs Junction Temperature, Normalized at 25°C

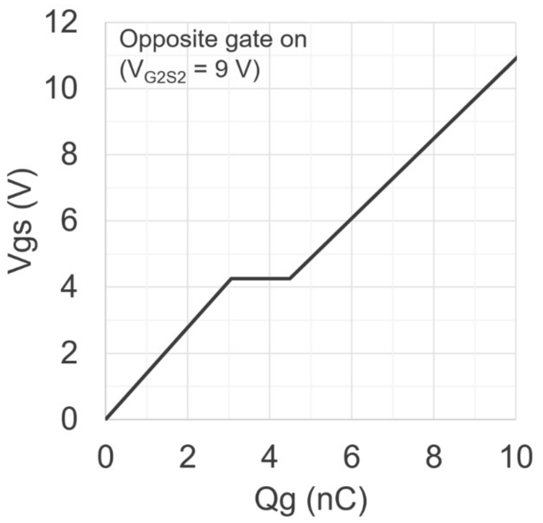


Figure 8. Typical Gate Charge Characteristics

I_{SS} = 5A, V_{SS} = 400V

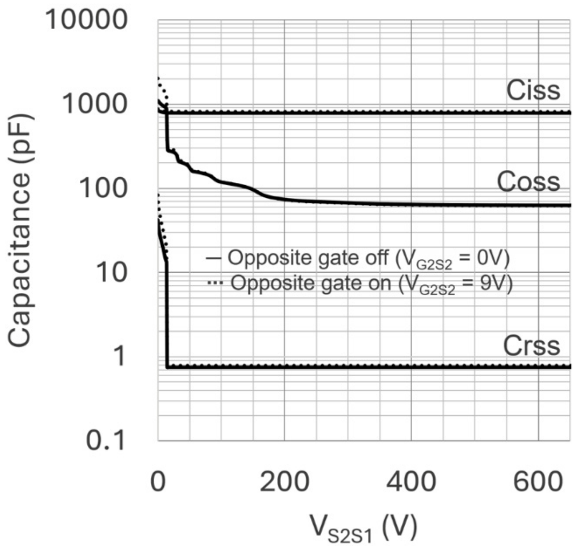


Figure 9. Typical Capacitance Characteristics with Single Gate Off and Both Gates Off,

f = 1MHz

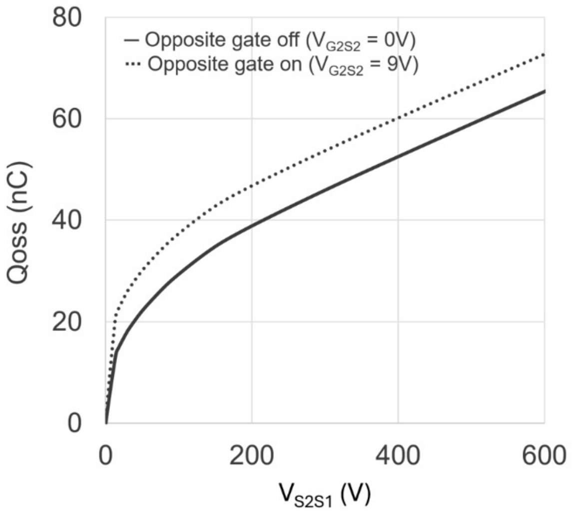


Figure 10. Output Charge vs Voltage

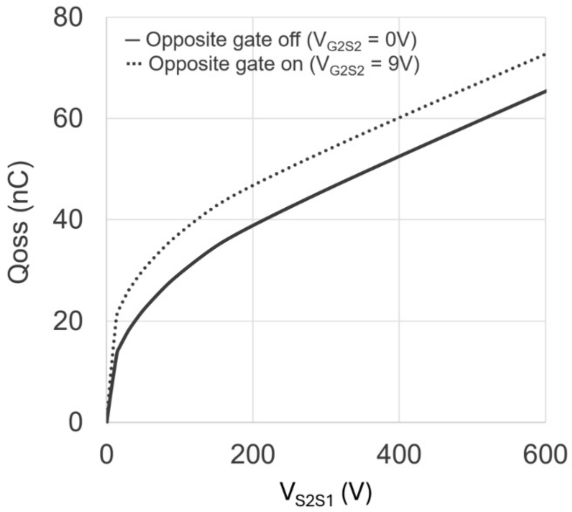


Figure 11. Output Energy vs Voltage

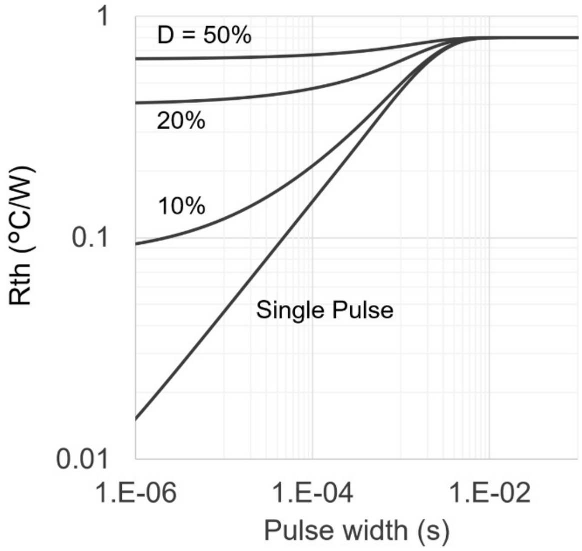


Figure 12. Thermal Resistance vs Pulse Width (single pulse).

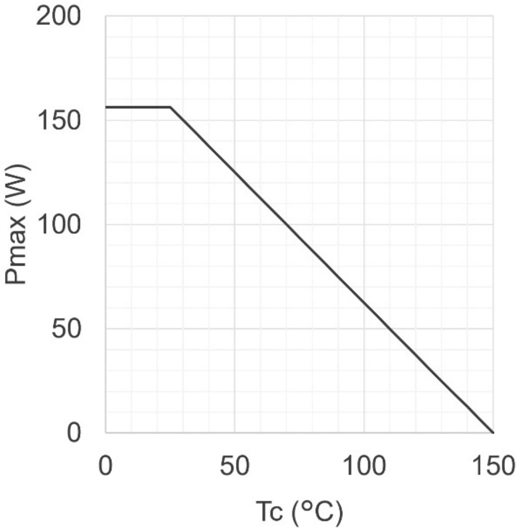


Figure 13. Max Power Dissipation vs Case Temperature

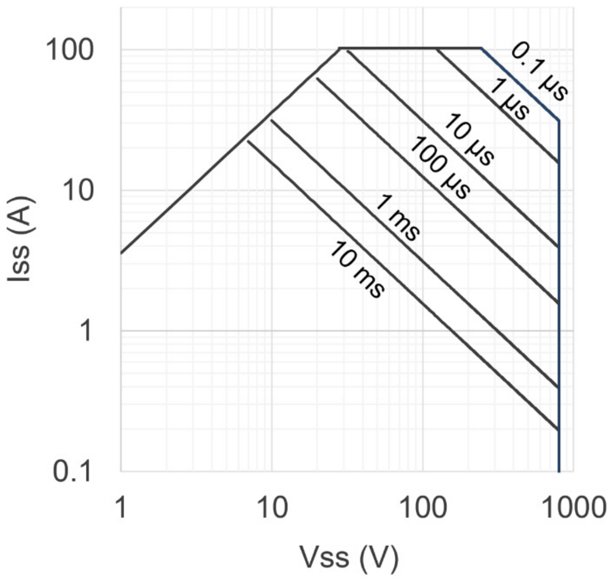


Figure 14. Safe Operating Area, Parameter Pulse Width

4. Test Circuits and Waveforms

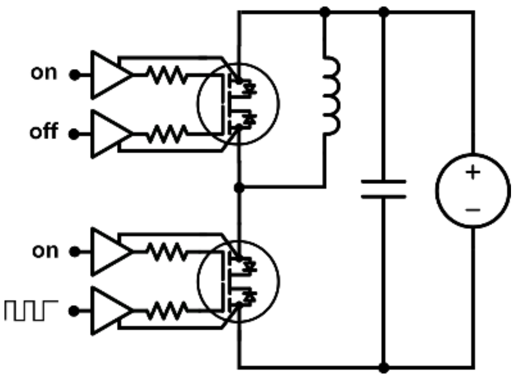


Figure 15. Switching Time Test Circuit

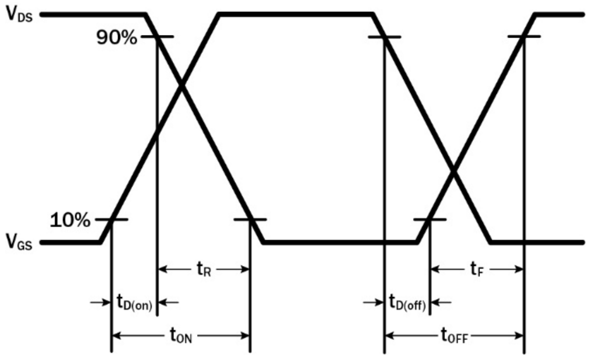


Figure 16. Switching Time Waveform

5. Modes of Operation

The GaN BDS has three modes of operation:

- Both gates off
- Both gates on
- Single gate on

When **both gates are on**, the device conducts current in both directions with the lowest on-state resistance. Use this mode during conduction time to ensure lowest conduction losses.

When a **single gate is on**, the device rectifies, conducting current in one direction and blocking it in the other. Use this mode during deadtime periods to ensure a free-wheeling path for inductive currents while preventing shoot-through in half-bridge legs.

When **both gates are off**, the device blocks current in both directions. No free-wheeling path is available in neither direction. Use this mode with caution: unclamped inductive switching at high voltage may push the device beyond maximum ratings.

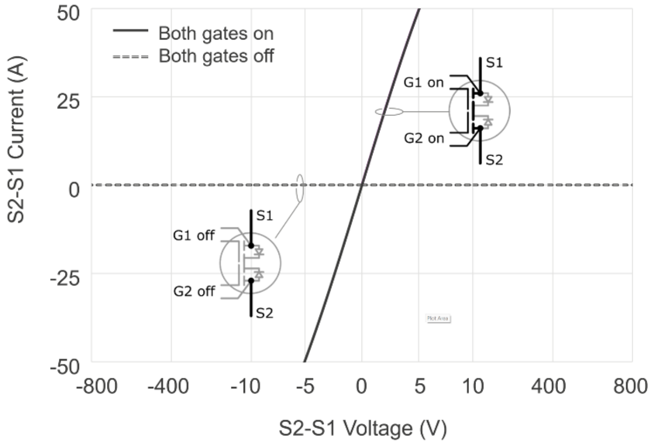


Figure 17. Both Gates On/Off

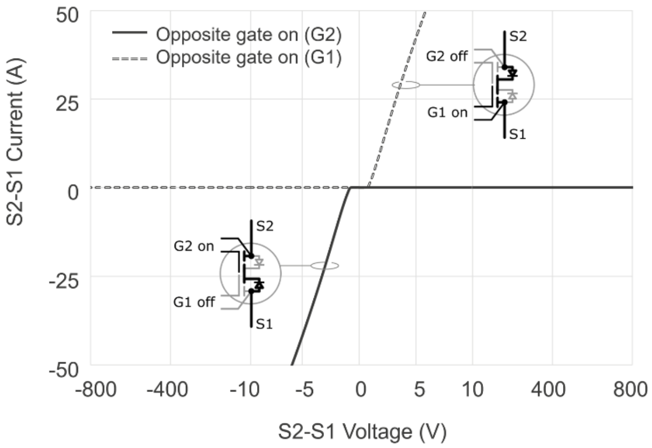


Figure 18. Opposite Gate On

6. Device Architecture

The GaN BDS consists of a high-voltage **D-mode GaN HEMT** connected in cascode configuration with two low-voltage silicon MOSFETs. The D-mode GaN HEMT monolithically integrates the high-voltage bidirectional voltage blocking capability in common-drain configuration for smallest footprint and highest switching figure of merit. The **low-voltage silicon MOSFETs** ensure high gate threshold, high gate robustness and efficient reverse conduction. Because of the cascode architecture, the BDS product is capable of both soft-switching and hard-switching with high di/dt and dv/dt immunity, and no internal or external substrate bias circuitry is required.

The substrate of the GaN die is directly connected to the **package tab** for highest thermal performance. The substrate terminal is at high electrical impedance and requires no electrical connection.

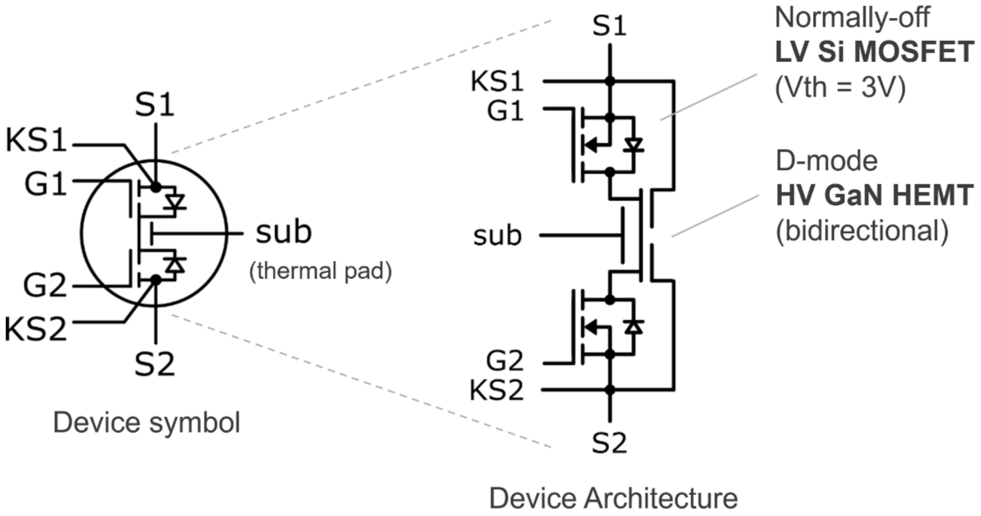
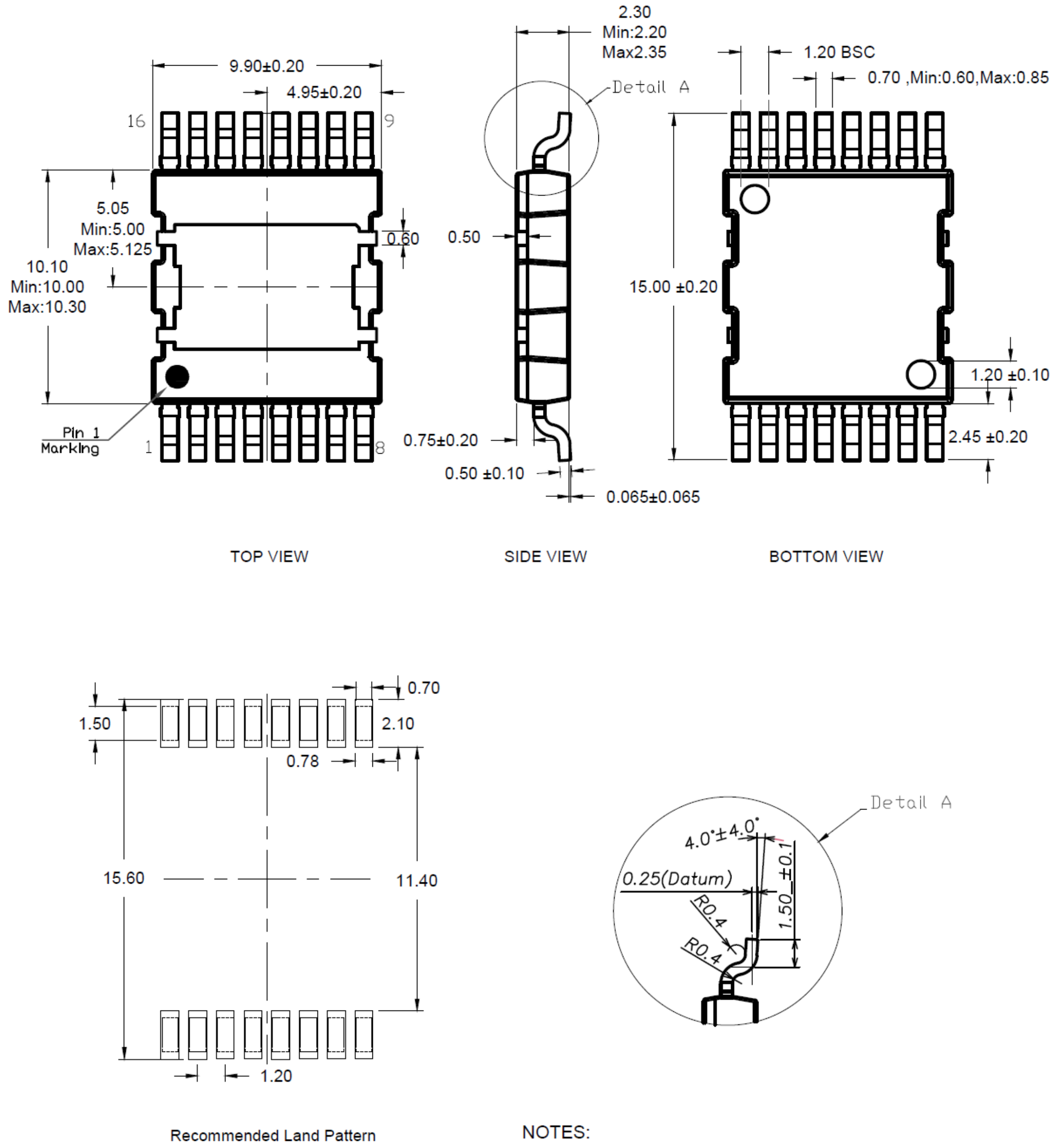


Figure 19. Device Symbol and Device Architecture

7. Design Considerations

If a heatsink is used, a thermal insulating material should be inserted between the package tab and the heatsink to ensure proper electrical isolation.

8. Package Outline Drawings



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.

Figure 20. Package Outline Drawing – 16-TOLT 10.1 × 9.9 × 2.3 mm Body

9. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

10. Ordering Information

Part Number	Package Description	Package Configuration
TP65B110HRU-TR [1]	16-TOLT 10.1 × 9.9 × 2.3 mm	Bi-directional, Common Drain

1. “-TR” suffix refers to tape and reel.

11. Revision History

Revision	Date	Description
1.00	Mar 10, 2026	Initial release.

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