PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

µPD66702, µPD66703

System-on-Chip Lite+
Extended ARM7TDMI-S™-based, Customizable Microcontroller
32-Bit RISC CPU Core

DESCRIPTION

System-on-Chip Lite+ is based on standard ASIC technology and consists of two blocks: an ARM7TDMI-S based subsystem and a sea-of-gates area. The ARM subsystem is fully designed and verified as a super-macro. It frees the user from the task of developing a complete RISC computer system. The sea-of-gates area allows the user to implement custom logic or special peripheral functions.
System-on-Chip Lite+ is designed for embedded control applications. To maintain flexibility, System-on-Chip Lite+ is not realized as an ASSP (Application Specific Standard Product); consequently it can be used for a wide range of different applications. Once the customer's functions are implemented into the sea-of-gates block, it becomes a custom SoC.
The ARM7TDMI-S based subsystem of System-on-Chip Lite+ offers an extended combination of general purpose peripheral functions, like dynamic and static memory interface, 10/100 Mbps Ethernet MAC with MII interface, a serial communication interface (UART), Timer (32-bit), Interrupt Controller, Watchdog, internal RAM and ROM.

Detailed functions are described in the following user's manuals. Be sure to read these manuals when you design your systems.

User's Manual System-on-Chip Lite+ : A17158EE2V0UM00

FEATURES

- ARM7TDMI-S core (Rev. 4.2) with max. 60 MHz ARM and THUMB instruction set supported
- 3 KBytes internal ROM, 8 KBytes internal RAM
- External memory interface supports SDRAM (max. 100 MHz). SyncFlash, (Page) ROM, (Page) Flash, SRAM and I/O devices
- 16/32 bit configurable bus width for dynamic memories and 8/16/32 bit for static memories and I/O
- 10/100 Mbps Ethernet MAC integrated with high-speed AHB bus to external memory
- User-defined logic (UDL) complexity of max. 250,000 raw gates for µPD66702 and 440,000 raw gates for µPD66703
- Max. 50 I/O pins (76, if 16-bit memory interface is used) on µPD66702 and max. 76 (102, if 16-bit memory interface is used) on µPD66703
- APB, AHB master and AHB slave interfaces between ARM subsystem and UDL
- 1 channel serial interface (UART)
- Integrated USB 1.1 compatible buffers
- 32-bit timer and 12-bit watchdog timer
- Integrated oscillator and PLL to generate all internally required clocks
- Interrupt Controller for 32 prioritized interrupt sources with nested interrupt capabilities
- On-chip debug functionality via JTAG
- Boundary scan support
- 2.5 V (logic) and 3.3 V (I/O) power supply
- Temperature Range: T_A = - 40 to + 85°C
- Compact packages: 240FPBGA for µPD66702 and 256PBGA for µPD66703
- 0.25 µm CMOS technology

ORDERING INFORMATION

Part Number	Package	UDL complexity
µPD66702F1-Yxx-HN3	240FPBGA	250,000 raw gates
µPD66703F1-Yxx-GN4	256PBGA	440,000 raw gates

The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production.
Not all products and/or types are availabe in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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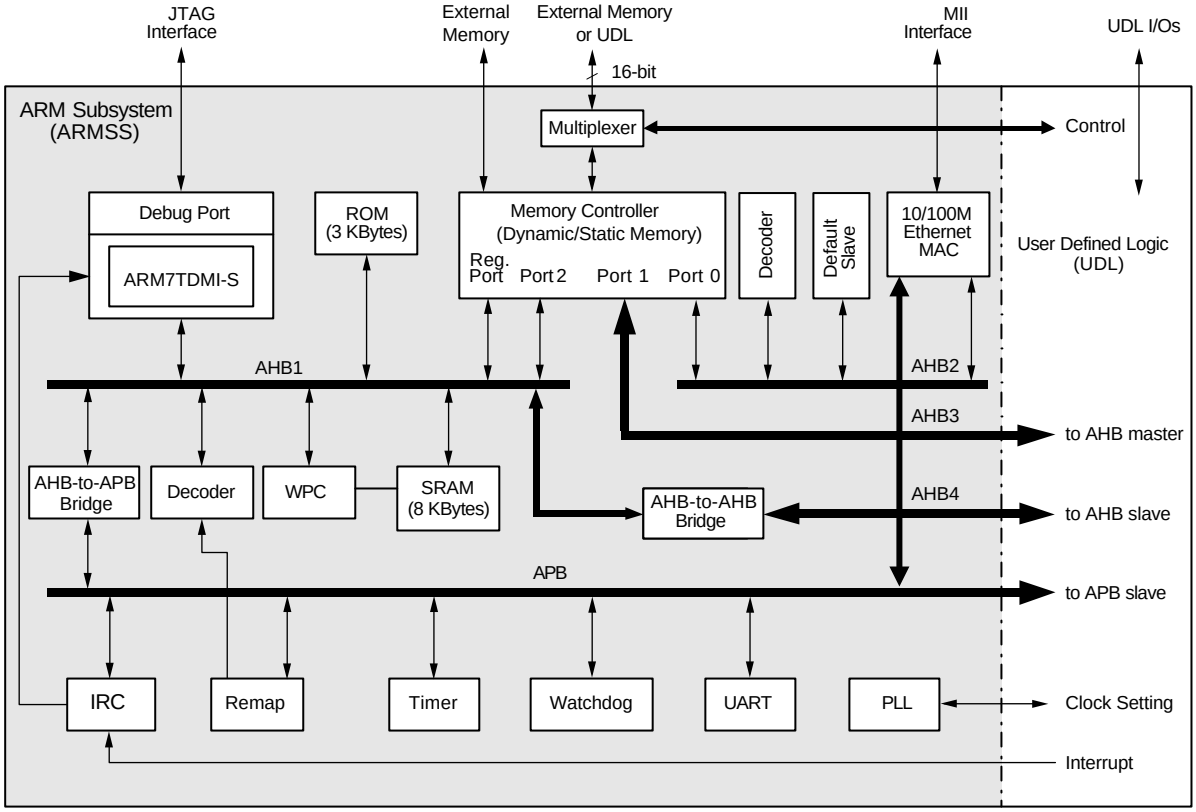
INTERNAL BLOCK DIAGRAM

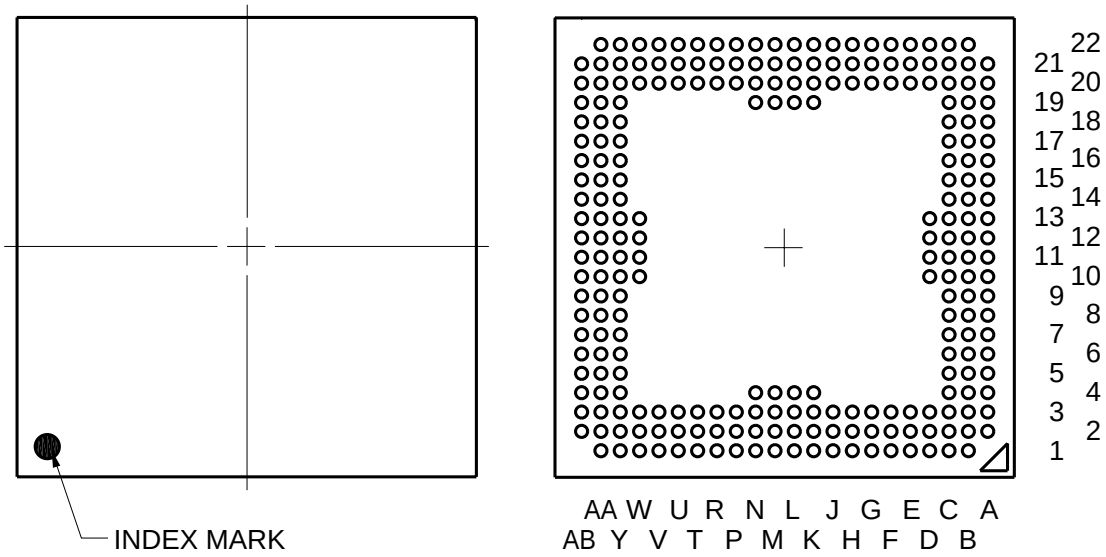


PIN IDENTIFICATION

XADDR(27:0)	Address bus	RX_ER	: MII receive error
XDATA(31:0)	Data bus	RXCLK	: MII receive clock
nXOE	Output enable	RX_DV	: MII receive data valid
nXWEN	Write Enable	CRS	: MII carrier sense detection
CKEOUT(3:0)	SDRAM/SyncFlash clock enable	MDC	: MII management data synchronization clock
CLKOUT(3:0)	SDRAM/SyncFlash clock	MDIO	: MII management data input/output
FBCLKIN(3:0)	SDRAM/SyncFlash feed-back clock input	DBGEN	: Debug enable
DQMOUT(3:0)	Data mask output to SDRAM/ SyncFlash	JTAG_TDI	: JTAG data in
nCASOUT	Column address strobe to SDRAM/ SyncFlash	JTAG_TDO	: JTAG data out
nRASOUT	Row address strobe to SDRAM/ SyncFlash	JTAG_TCK	: JTAG clock
nXCSD(3:0)	Chip Select to SDRAM/SyncFlash	JTAG_RTCK	: JTAG return clock
nRPOUT	Reset power down to SyncFlash memory	JTAG_TMS	: JTAG mode select
nXBLS(3:0)	Byte lane select	JTAG_TRST	: JTAG reset
nXCSS(3:0)	Chip Select to static memories	AV_{DD}	: 2.5 V analog power supply for PLL
RXD	UART Receive Data Input	DV_{DD}	: 2.5 V digital power supply for PLL
TXD	UART Transmit Data Output	AGND	: Analog Ground for PLL
D+	USB data (+)	DGND	: Digital Ground for PLL
D-	USB data (-)	V_{DD1}	: 2.5 V power supply voltage
TX_ER	MII transmit coding error	V_{DD2}	: 3.3 V power supply voltage
TXD(3:0)	MII transmit data (to PHY)	GND	: Ground
TX_EN	MII transmit enable	XT1	: Oscillator input
TXCLK	MII transmit clock	XT2	: Oscillator output
COL	MII collision detection		
RXD(3:0)	MII receive data	UDL(49:0)	: User defined logic
		UDL(101:76)	User defined logic (only on μPD66703)

PIN CONFIGURATION (for μPD66702)

- 240-Pin FPBGA (for μPD66702)



Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A2	FBCLKIN1	A18	XADDR6	B13	XADDR16	C7	DQMOUT1
A3	FBCLKIN0	A19	NC[Note 1]	B14	GND	C8	CLKOUT0
A4	nXCSS0	A20	NC[Note 1]	B15	XADDR13	C9	nXWEN
A5	nXCSD1	A21	GND	B16	XADDR8	C10	VDD1
A6	nRASOUT	B1	VDD2	B17	XADDR5	C11	XADDR23
A7	CLKOUT1	B2	GND	B18	XADDR3	C12	XADDR20
A8	nXOE	B3	GND	B19	XADDR1	C13	VDD1
A9	VDD2	B4	NC[Note 1]	B20	XADDR0	C14	XADDR14
A10	XADDR25	B5	NC[Note 1]	B21	VDD2	C15	XADDR11
A11	XADDR22	B6	nXBLS0	B22	CLKOUT3	C16	XADDR10
A12	GND	B7	nCASOUT	C1	NC[Note 1]	C17	XADDR7
A13	XADDR18	B8	DQMOUT0	C2	XDATA0	C18	XADDR4
A14	VDD2	B9	GND	C3	VDD1	C19	XADDR2
A15	XADDR15	B10	XADDR27	C4	nXCSS1	C20	GND
A16	XADDR12	B11	XADDR24	C5	nXBLS1	C21	VDD1
A17	XADDR9	B12	XADDR19	C6	nXCSD0	C22	CLKOUT2

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
D1	NC[Note 1]	J1	VDD2	N19	TXD3	W1	DQMOUT2
D2	XDATA1	J2	GND	N20	VDD2	W2	NC
D3	XDATA2	J3	XDATA14	N21	TXD2	W3	DQMOUT3
D10	XADDR26	J20	IC[Note 2]	N22	TX_EN	W10	UDL11
D11	XADDR21	J21	GND	P1	VDD2	W11	UDL16
D12	VDD2	J22	VDD2	P2	GND	W12	UDL17
D13	XADDR17	K1	D+	P3	AVDD	W13	UDL22
D20	CKEOUT3	K2	FBCLKIN2	P20	TXD0	W20	UDL42
D21	NC[Note 1]	K3	VDD1	P21	VDD1	W21	UDL41
D22	CKEOUT2	K4	FBCLKIN3	P22	TXD1	W22	NC[Note 1]
E1	XDATA6	K19	CRS	R1	DVDD	Y1	nXCSD2
E2	XDATA3	K20	VDD1	R2	XDATA24	Y2	VDD1
E3	XDATA4	K21	MDC	R3	AGND	Y3	GND
E20	CKEOUT1	K22	RX_DV	R20	RXD	Y4	nXCSS2
E21	NC[Note 1]	L1	VDD2	R21	TX_ER	Y5	UDL0
E22	nRPOUT	L2	D-	R22	GND	Y6	UDL3
F1	XDATA9	L3	GND	T1	DGND	Y7	UDL6
F2	XDATA5	L4	XDATA16	T2	XDATA26	Y8	UDL7
F3	XDATA7	L19	RXD2	T3	XDATA25	Y9	XT1
F20	JTAG_TRST	L20	RX_ER	T20	NC[Note 1]	Y10	VDD1
F21	CKEOUT0	L21	RXCLK	T21	UDL48	Y11	UDL14
F22	JTAG_TMS	L22	RXD3	T22	TXD	Y12	UDL19
G1	XDATA12	M1	XDATA18	U1	XDATA27	Y13	VDD1
G2	XDATA8	M2	XDATA20	U2	XDATA30	Y14	UDL25
G3	XDATA10	M3	XDATA19	U3	XDATA28	Y15	UDL26
G20	JTAG_TCK	M4	XDATA17	U20	UDL47	Y16	UDL29
G21	JTAG_RTCK	M19	RXD1	U21	UDL45	Y17	UDL32
G22	JTAG_TDI	M20	COL	U22	UDL49	Y18	UDL35
H1	XDATA15	M21	TXCLK	V1	XDATA29	Y19	UDL37
H2	XDATA13	M22	RXD0	V2	NC[Note 1]	Y20	VDD1
H3	XDATA11	N1	XDATA21	V3	XDATA31	Y21	UDL40
H20	DBGEN	N2	XDATA23	V20	UDL44	Y22	NC[Note 1]
H21	JTAG_TDO	N3	VDD1	V21	UDL43	AA1	nXCSD3
H22	MDIO	N4	XDATA22	V22	UDL46	AA2	VDD2

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
AA3	nXBLS2	AA13	UDL23	AB2	GND	AB12	UDL18
AA4	nXBLS3	AA14	GND	AB3	NC[Note 1]	AB13	UDL21
AA5	nXCSS3	AA15	UDL28	AB4	NC[Note 1]	AB14	VDD2
AA6	UDL1	AA16	UDL30	AB5	UDL2	AB15	UDL24
AA7	UDL4	AA17	UDL34	AB6	UDL5	AB16	UDL27
AA8	UDL9	AA18	NC[Note 1]	AB7	UDL8	AB17	UDL31
AA9	GND	AA19	NC[Note 1]	AB8	XT2	AB18	UDL33
AA10	UDL10	AA20	GND	AB9	VDD2	AB19	UDL36
AA11	UDL13	AA21	GND	AB10	UDL12	AB20	UDL38
AA12	UDL20	AA22	VDD2	AB11	UDL15	AB21	UDL39

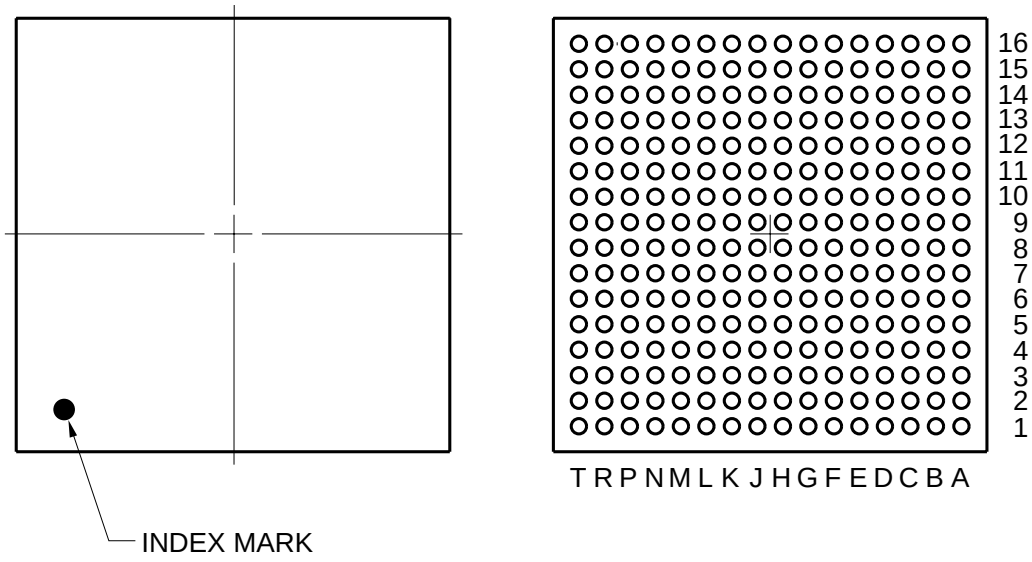
Notes: 1. Not connected

2. Internally connected, must always be pulled low.

Remark: Unused UDL pins must be internally connected to GND by using appropriate UDL-code.

PIN CONFIGURATION (for μPD66703)

- 256-Pin PBGA (for μPD66703)



Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	FBCLKIN0	B1	XDATA1	C1	XDATA4	D1	XDATA7
A2	nXCSS1	B2	XDATA0	C2	XDATA2	D2	XDATA3
A3	nXBLS1	B3	FBCLKIN1	C3	NC[Note 1]	D3	XDATA6
A4	nXBLS0	B4	nXCSS0	C4	nXCSD1	D4	VDD1
A5	DQMOUT0	B5	nCASOUT	C5	nXCSD0	D5	nRASOUT
A6	nXWEN	B6	DQMOUT1	C6	CLKOUT1	D6	XADDR27
A7	XADDR24	B7	CLKOUT0	C7	nXOE	D7	XADDR25
A8	XADDR19	B8	XADDR23	C8	XADDR22	D8	XADDR18
A9	XADDR16	B9	XADDR12	C9	GND	D9	XADDR13
A10	XADDR10	B10	XADDR6	C10	XADDR7	D10	XADDR14
A11	XADDR5	B11	XADDR3	C11	XADDR4	D11	XADDR8
A12	XADDR2	B12	XADDR1	C12	CLKOUT2	D12	VDD1
A13	XADDR0	B13	CKEOUT2	C13	CLKOUT3	D13	VDD1
A14	CKEOUT3	B14	CKEOUT1	C14	NC	D14	DBGEN
A15	CKEOUT0	B15	nRPOUT	C15	JTAG_TRST	D15	JTAG_TDO
A16	JTAG_TMS	B16	JTAG_TCK	C16	JTAG_TDI	D16	JTAG_RTCK

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
E1	FBCLKIN2	G1	XDATA15	J1	XDATA22	L1	XDATA28
E2	XDATA8	G2	XDATA11	J2	DVDD	L2	DQMOUT2
E3	XDATA5	G3	XDATA12	J3	XDATA25	L3	XDATA30
E4	VDD1	G4	XDATA17	J4	XDATA21	L4	XDATA26
E5	VDD1	G5	XDATA18	J5	VDD2	L5	DGND
E6	XADDR26	G6	XDATA20	J6	VDD2	L6	UDL19
E7	XADDR21	G7	GND	J7	GND	L7	UDL25
E8	VDD2	G8	GND	J8	GND	L8	VDD2
E9	VDD2	G9	GND	J9	GND	L9	VDD2
E10	XADDR15	G10	GND	J10	GND	L10	UDL29
E11	XADDR9	G11	TXD1	J11	VDD2	L11	UDL97
E12	VDD1	G12	TXD2	J12	VDD2	L12	UDL95
E13	MDIO	G13	COL	J13	UDL99	L13	UDL94
E14	IC[Note 2]	G14	RXD2	J14	TXD	L14	UDL90
E15	MDC	G15	RX_ER	J15	UDL98	L15	UDL89
E16	RX_DV	G16	TXCLK	J16	NC[Note 1]	L16	UDL91
F1	XDATA10	H1	XDATA19	K1	AVDD	M1	XDATA31
F2	FBCLKIN3	H2	D-	K2	XDATA29	M2	DQMOUT3
F3	XDATA9	H3	GND	K3	XDATA27	M3	nXCSD3
F4	XDATA13	H4	XDATA16	K4	AGND	M4	nXCSD2
F5	XDATA14	H5	VDD2	K5	XDATA24	M5	VDD1
F6	D+	H6	VDD2	K6	XDATA23	M6	UDL17
F7	XADDR20	H7	GND	K7	GND	M7	UDL23
F8	VDD2	H8	GND	K8	GND	M8	VDD2
F9	VDD2	H9	GND	K9	GND	M9	VDD2
F10	XADDR17	H10	GND	K10	GND	M10	UDL30
F11	XADDR11	H11	VDD2	K11	RXD	M11	UDL35
F12	RXD0	H12	VDD2	K12	UDL101	M12	VDD1
F13	RXD1	H13	TX_ER	K13	UDL100	M13	VDD1
F14	RXCLK	H14	TXD3	K14	UDL93	M14	UDL84
F15	CRS	H15	TX_EN	K15	UDL92	M15	UDL87
F16	RXD3	H16	TXD0	K16	UDL96	M16	UDL88

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
N1	nXBLS3	P1	nXCSS2	R1	UDL0	T1	UDL1
N2	nXCSS3	P2	UDL2	R2	UDL3	T2	UDL4
N3	nXBLS2	P3	NC[Note 1]	R3	UDL5	T3	UDL7
N4	VDD1	P4	UDL9	R4	UDL6	T4	UDL10
N5	VDD1	P5	UDL8	R5	UDL11	T5	UDL12
N6	UDL16	P6	XT2	R6	XT1	T6	UDL13
N7	UDL22	P7	UDL15	R7	UDL14	T7	UDL18
N8	UDL21	P8	UDL26	R8	UDL20	T8	UDL24
N9	UDL27	P9	UDL31	R9	UDL32	T9	UDL28
N10	UDL34	P10	UDL37	R10	UDL39	T10	UDL33
N11	UDL36	P11	UDL40	R11	UDL42	T11	UDL38
N12	UDL44	P12	UDL45	R12	UDL43	T12	UDL41
N13	VDD1	P13	UDL46	R13	UDL49	T13	UDL47
N14	UDL85	P14	NC	R14	UDL78	T14	UDL48
N15	UDL82	P15	UDL81	R15	UDL79	T15	UDL76
N16	UDL86	P16	UDL83	R16	UDL80	T16	UDL77

Notes: 1. Not connected.

2. Internally connected, must always be pulled low.

Remark: Unused UDL pins must be internally connected to GND by using appropriate UDL-code

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1. Pin Functions

1.1 List of Pin and Signal Functions

1.1.1 External pins

(1) Memory interface

Table 1-1: Memory Interface Pins

Pin Name	I/O	Function	Alternate Function
XADDR(27:0)	O	28-bit address bus for external memory	
XDATA(15:0)	I/O	lower 16-bit of data bus for external memory	
XDATA(31:16)	I/O	upper 16-bit of data bus for external memory	UDL(65:50)
CKEOUT(3:0)	O	SDRAM and SyncFlash clock enable	
CLKOUT(1:0)	O	SDRAM and SyncFlash clock output	
CLKOUT(3:2)	O**Note 1**	SDRAM and SyncFlash clock output	UDL(71:70)
FBCLKIN(3:0)	I	SDRAM and SyncFlash feedback clock input	
DQMOUT(1:0)	O	Data mask output to SDRAM and SyncFlash	
DQMOUT(3:2)	O**Note 2**	Data mask output to SDRAM and SyncFlash	UDL(73:72)
nXCSD(1:0)	O	Chip select signal output for SDRAMs	
nXCSD(3:2)	O**Note 2**	Chip select signal output for SDRAMs	UDL(75:74)
nRASOUT	O	Row address strobe output to SDRAM and SyncFlash	
nCASOUT	O	Column address strobe output to SDRAM and SyncFlash	
nRPOUT	O	Reset power down to SyncFlash memory	
nXOE	O	Data output enable	
nXWEN	O	Write enable signal output	
nXCSS(1:0)	O	Chip select signal output for static memory and I/O devices	
nXCSS(3:2)	O**Note 2**	Chip select signal output for static memory and I/O devices	UDL(69:68)
nXBLS0	O	Byte lane select signal output for XDATA(7:0)	
nXBLS1	O	Byte lane select signal output for XDATA(15:8)	
nXBLS2	O**Note 2**	Byte lane select signal output for XDATA(23:16)	UDL66
nXBLS3	O**Note 2**	Byte lane select signal output for XDATA(31:24)	UDL67

Notes: 1. Input, if configured as UDL pin

2. I/O, if configured as UDL pin

(2) UART

Table 1-2: UART Pins

Pin Name	I/O	Function	Alternate Function
RXD	I	Serial receive data input	
TXD	O	Serial transmit data output	

(3) USB buffer

Table 1-3: USB Buffer Pins

Pin Name	I/O	Function	Alternate Function
D+	I/O	USB data (+)	
D-	I/O	USB data (-)	

(4) MII interface

Table 1-4: MII Interface Pins

Pin Name	I/O	Function	Alternate Function
TX_ER	O	MII transmit error output	
TXD(3:0)	O	MII transmit data output	
TX_EN	O	MII transmit enable output	
TXCLK	I	MII transmit clock input	
COL	I	MII collision detection input	
RX_ER	I	MII receive error input	
RXD(3:0)	I	MII receive data input	
RX_DV	I	MII receive data valid input	
RXCLK	I	MII receive clock input	
CRS	I	MII carrier sense detection input	
MDC	O	MII management data synchronization clock output	
MDIO	I/O	MII management data input/output	

(5) Debug interface

Table 1-5: Debug Interface Pins

Pin Name	I/O	Function	Alternate Function
DBGEN[Note]	I	Debug enable input that selects between boundary scan or ARM debug operation low: enable boundary scan operation high: enable ARM debug operation	
JTAG_TDI	I	Data in for debugging or boundary scan	
JTAG_TDO	O	Data out for debugging or boundary scan	
JTAG_TCK	I	Clock input for debugging or boundary scan	
JTAG_RTCK	I/O	JTAG return clock	
JTAG_TMS	I	Mode select input for debugging or boundary scan	
JTAG_TRST	I	Reset input for debugging or boundary scan	

Note: Must be kept unchanged during operation

(6) User defined logic (UDL)

Table 1-6: UDL Pins

Pin Name	I/O	Function	Alternate Function
UDL(7:0)	I/O	User defined logic input/output	
UDL8	I/O	User defined logic input/output	GND, if internal oscillator is used (only on μPD66702)
UDL9	I/O	User defined logic input/output	$V_{DD1,}$ if internal oscillator is used (only on μPD66702)
UDL10	I/O	User defined logic input/output	
UDL11	I/O	User defined logic input/output	GND, if internal oscillator is used (only on μPD66703)
UDL12	I/O	User defined logic input/output	$V_{DD1,}$ if internal oscillator is used (only on μPD66703)
UDL(49:13)	I/O	User defined logic input/output	
UDL(65:50)	I/O	User defined logic input/output	XDATA(31:16)
UDL(67:66)	I/O[Note 1]	User defined logic input/output	nXBLS(3:2)
UDL(69:68)	I/O[Note 1]	User defined logic input/output	nXCSS(3:2)
UDL(71:70)	I[Note 1]	User defined logic input	CLKOUT(3:2)
UDL(73:72)	I/O[Note 1]	User defined logic input/output	DQMOUT(3:2)
UDL(75:74)	I/O[Note 1]	User defined logic input/output	nXCSD(3:2)
UDL(101:76)	I/O[Note 2]	User defined logic input/output	
XT1	I	Oscillator input	
XT2	O	Oscillator output	

Notes: 1. Output, if not configured as UDL pin

2. only available on μPD66703

(7) Power supply

Table 1-7: Power Supply Pins

Pin Name	Function	Alternate Function
AV_{DD}	2.5 V analog power supply for PLL	
DV_{DD}	2.5 V digital power supply for PLL	
AGND	Analog ground for PLL	
DGND	Digital ground for PLL	
V_{DD1}	2.5 V power supply voltage	UDL9 (on μPD66702) or UDL12 (on μPD66703) **Note 1**, if internal oscillator is unused
V_{DD2}	3.3 V power supply voltage	
GND	Ground	UDL8 (on μPD66702) or UDL11 (on μPD66703) **Note 2**, if internal oscillator is unused

Notes: 1. UDL9 is available at pin AA8 on μPD66702; UDL12 is available at pin T5 on μPD66703

2. UDL8 is available at pin AB7 on μPD66702; UDL11 is available at pin R5 on μPD66703

1.1.2 Internal signals

(1) AHB4 (AHB Master interface) signals

Table 1-8: AHB4 Signals

Pin Name	Direction	Function
AHB4_HBUSREQ	to UDL	Bridge request to arbiter of AHB4
AHB4_HGRANT	from UDL	Bridge is granted AHB4 by arbiter
AHB4_HLOCK	to UDL	Bridge requires locked access on AHB4
AHB4_HADDR(31:0)	to UDL	32-bit system address bus
AHB4_HREADY	from UDL	Extension of bus transfer
AHB4_HTRANS(1:0)	to UDL	Type of current transfer
AHB4_HWRITE	to UDL	High = Write transfer; Low = Read transfer
AHB4_HSIZE(2:0)	to UDL	Size of transfer
AHB4_HBURST(2:0)	to UDL	Indicated part of burst
AHB4_HPROT(3:0)	to UDL	Protection control
AHB4_HRESP(1:0)	from UDL	Response from slave
AHB4_HWDATA(31:0)	to UDL	Write data bus
AHB4_HRDATA(31:0)	from UDL	Read data bus

(2) AHB3 (AHB Slave interface) signals

Table 1-9: AHB3 Signals

Pin Name	Direction	Function
AHB3_HADDR(27:0)	from UDL	28-bit system address bus
AHB3_HSELMPMCG	from UDL	AHB slave select (general chip select to MPMC)
AHB3_HSELMPMCCS(7:0)	from UDL	AHB slave select (chip selects for memory)
AHB3_HMASTLOCK	from UDL	Master request for locked transfer
AHB3_HREADYIN	from UDL	Extension of bus transfer
AHB3_HREADYOUT	to UDL	Extension of bus transfer
AHB3_HTRANS(1:0)	from UDL	Type of current transfer
AHB3_HWRITE	from UDL	High = Write transfer; Low = Read transfer
AHB3_HSIZE(2:0)	from UDL	Size of transfer
AHB3_HBURST(2:0)	from UDL	Indicate part of burst
AHB3_HRESP(1:0)	to UDL	Response from slave
AHB3_HWDATA(31:0)	from UDL	Write data bus
AHB3_HRDATA(31:0)	to UDL	Read data bus

(3) APB signals

Table 1-10: APB Signals

Pin Name	Direction	Function
PADDR_UDL(28:0)	to UDL	29-bit APB address bus
PWRITE_UDL	to UDL	High = Write transfer; Low = Read transfer
PSELUDL_UDL	to UDL	APB slave select
PENABLE_UDL	to UDL	Strobe signal
PRDATA_UDL(31:0)	from UDL	Read data bus
PWDATA_UDL(31:0)	to UDL	Write data bus

(4) Signals for control of UDL pins shared with external memory interface

Table 1-11: UDL Pin Control Signals

Pin Name	Direction	Function
EXTIN_UDL(75:50)	to UDL	Input from UDL pins that are shared with external memory interface
EXTOUT_UDL(69:50) EXTOUT_UDL(75:72)**Note**	from UDL	Output to UDL pins that are shared with external memory interface
EXTEN_UDL(69:50) EXTEN_UDL(75:72)**Note**	from UDL	Direction control for UDL pins that are shared with external memory interface

Note: EXTOUT_UDL(71:70) and EXTEN_UDL(71:70) do not exist, because UDL(71:70) can only be used as inputs.

(5) USB buffer signals

Table 1-12: USB Buffer Signals

Pin Name	Direction	Function
USB_Y1	to UDL	Data output
USB_ISE	to UDL	Single end zero output
USB_CNA	to UDL	Plus connect/disconnect
USB_CNB	to UDL	Minus connect/disconnect
USB_A	from UDL	Data input
USB_OEN	from UDL	Input enable
USB_OSE	from UDL	Single end zero input
USB_FL	from UDL	Last bit, high speed input
USB_IEN	from UDL	Enable input (for IDDQ test)
USB_PS	from UDL	Power save mode

(6) Configuration signals

Table 1-13: Configuration Signals

Pin Name	Direction	Function
MPMCSTCSMW(1:0)	from UDL	Memory width selection for nXCSS1 of MPMC and external memory interface bus width
MPMCSTCS(3:0)POL	from UDL	Polarity of nXCSS(3:0) signals
MPMCSTCS1PB	from UDL	Byte lane state selection
BIGENDIAN	from UDL	Endianess selection
EA(1:0)	from UDL	Boot source selection
CLKRATIO	from UDL	Memory to AMBA clock ratio

(7) PLL signals

Table 1-14: PLL Signals

Pin Name	Direction	Function
PLL_M(4:0)	from UDL	PLL divider settings, M-value
PLL_N(6:0)	from UDL	PLL divider settings, N-value
PLL_P(2:0)	from UDL	PLL divider settings, P-value
PLL_S(1:0)	from UDL	PLL VCO frequency selection
PLL_MB	from UDL	PLL operation mode control
PLL_MODE	from UDL	PLL operation mode control
XCLK	from UDL	Input clock for PLL
FCLK	to UDL	Output clock from PLL

(8) Additional signals

Table 1-15: Additional Signals

Pin Name	Direction	Function
IRQ_UDL(27:0)	from UDL	Interrupt lines to interrupt controller
NFIQ_UDL	from UDL	FIQ directly connected to ARM CPU
nRST	from UDL	Reset signal from UDL to ARM subsystem
MPMCNPOR	from UDL	Reset signal from UDL to MPMC
HRESETN	to UDL	Reset signal from ARM subsystem
SCLK	from UDL	System clock into ARM subsystem
DBGACK	to UDL	Acknowledge debug state of ARM7
DBGREQ	from UDL	Request to ARM7 to enter debug state
MASK_DBGEN	from UDL	Disable the possibility to set ARM7 to debug state
BS_TCK	to UDL	Shared JTAG clock signal for boundary scan in the UDL
BS_TMS	to UDL	Shared JTAG mode select signal for boundary scan in the UDL

1.2 Pin Status and Recommended Connection Examples

1.2.1 External pins

Table 1-16: External Pins (1/2)

Pin Name	I/O	Nominal drive strength	Input type	I/O during Reset	Level during Reset
XADDR(27:0)	O	9 mA	-	O	L
XDATA(15:0)	I/O	9 mA	LVTTL	Hi-Z	-
XDATA(31:16)	I/O	9 mA	LVTTL	Hi-Z Note 3	- Note 3
CKEOUT(3:0)	O	9 mA	-	O	H
CLKOUT(1:0)	O	9 mA	-	O	SCLK signal
CLKOUT(3:2)	O Note 1	9 mA	LVTTL	O Note 3	SCLK signal Note 3
FBCLKIN(3:0)	I	-	LVTTL	I	-
DQMOUT(1:0)	O	9 mA	-	O	H
DQMOUT(3:2)	O Note 2	9 mA	LVTTL	O Note 3	H Note 3
nXCSD(1:0)	O	9 mA	-	O	H
nXCSD(3:2)	O Note 2	9 mA	LVTTL	O Note 3	H Note 3
nRASOUT	O	9 mA	-	O	H
nCASOUT	O	9 mA	-	O	H
nRPOUT	O	9 mA	-	O	L
nXOE	O	9 mA	-	O	H
nXWEN	O	9 mA	-	O	H
nXCSS(1:0)	O	9 mA	-	O	H
nXCSS(3:2)	O Note 2	9 mA	LVTTL	O Note 3	H Note 3
nXBLS(1:0)	O	9 mA	-	O	H
nXBLS(3:2)	O Note 2	9 mA	LVTTL	O Note 3	H Note 3
RXD	I	-	LVTTL	I	-
TXD	O	6 mA	-	O	H
D+	I/O		USB	Hi-Z Note 4	- Note 4
D-	I/O		USB	Hi-Z Note 4	- Note 4
TX_ER	O	6 mA	-	O	L
TXD(3:0)	O	6 mA	-	O	L
TX_EN	O	6 mA	-	O	L
TXCLK	I	-	LVTTL	I	-
COL	I	-	LVTTL	I	-
RX_ER	I	-	LVTTL	I	-
RXD(3:0)	I	-	LVTTL	I	-
RX_DV	I	-	LVTTL	I	-
RXCLK	I	-	LVTTL	I	-
CRS	I	-	LVTTL	I	-
MDC	O	6 mA	-	O	L

Table 1-16: External Pins (2/2)

Pin Name	I/O	Nominal drive strength	Input type	I/O during Reset	Level during Reset
MDIO	I/O	6 mA	LVTTL	Hi-Z	-
DBGEN	I	-	internal pull down	I	-
JTAG_TDI	I	-	LVTTL	I	-
JTAG_TDO	O	6 mA	-	Hi-Z	-
JTAG_TCK	I	-	LVTTL	I	-
JTAG_RTCK	I/O	6 mA	LVTTL	O	L
JTAG_TMS	I	-	LVTTL	I	-
JTAG_TRST	I	-	LVTTL	I	-
XT1	I				
XT2	O				

Notes: 1. Input, if configured as UDL pin

2. I/O, if configured as UDL pin

3. Implementation dependent, if configured as UDL pin

4. Implementation dependent; USB buffers will be Hi-Z, if their OEN input is kept active during Reset

1.2.2 Internal signals

Table 1-17: Internal Signals (1/2)

Signal Name	Direction	Status during Reset
AHB4_HBUSREQ	to UDL	L
AHB4_HGRANT	from UDL	-
AHB4_HLOCK	to UDL	L
AHB4_HADDR(31:0)	to UDL	L
AHB4_HREADY	from UDL	-
AHB4_HTRANS(1:0)	to UDL	L
AHB4_HWRITE	to UDL	L
AHB4_HSIZE(2:0)	to UDL	L
AHB4_HBURST0	to UDL	H
AHB4_HBURST(2:1)	to UDL	L
AHB4_HPROT(3:0)	to UDL	L
AHB4_HRESP(1:0)	from UDL	-
AHB4_HWDATA(31:0)	to UDL	L
AHB4_HRDATA(31:0)	from UDL	-
AHB4_HBUSREQ	to UDL	L
AHB4_HGRANT	from UDL	-
AHB4_HLOCK	to UDL	L
AHB4_HADDR(31:0)	to UDL	L
AHB3_HADDR(27:0)	from UDL	-
AHB3_HSELMPMCG	from UDL	-
AHB3_HSELMPMCCS(7:0)	from UDL	-
AHB3_HMASTLOCK	from UDL	-
AHB3_HREADYIN	from UDL	-
AHB3_HREADYOUT	to UDL	H
AHB3_HTRANS(1:0)	from UDL	-
AHB3_HWRITE	from UDL	-
AHB3_HSIZE(2:0)	from UDL	-
AHB3_HBURST(2:0)	from UDL	-
AHB3_HRESP(1:0)	to UDL	L
AHB3_HWDATA(31:0)	from UDL	-
AHB3_HRDATA(31:0)	to UDL	L
PADDR_UDL(28:0)	to UDL	L
PWRITE_UDL	to UDL	L
PSELUDL_UDL	to UDL	L
PENABLE_UDL	to UDL	L
PRDATA_UDL(31:0)	from UDL	-
PWDATA_UDL(31:0)	to UDL	L
EXTIN_UDL(75:72)	to UDL	L
EXTIN_UDL(71:70)	to UDL	SCLK signal

Table 1-17: Internal Signals (2/2)

Signal Name	Direction	Status during Reset
EXTIN_UDL(69:66)	to UDL	L
EXTIN_UDL(65:50)	to UDL	undefined
EXTOUT_UDL(75:72)	from UDL	-
EXTOUT_UDL(69:50)	from UDL	-
EXTEN_UDL(75:72)	from UDL	-
EXTEN_UDL(69:50)	from UDL	-
USB_Y1	to UDL	undefined
USB_ISE	to UDL	undefined
USB_CNA	to UDL	undefined
USB_CNB	to UDL	undefined
USB_A	from UDL	-
USB_OEN	from UDL	-
USB_OSE	from UDL	-
USB_FL	from UDL	-
USB_IEN	from UDL	-
USB_PS	from UDL	-
PLL_M(4:0)	from UDL	-
PLL_N(6:0)	from UDL	-
PLL_P(2:0)	from UDL	-
PLL_S(1:0)	from UDL	-
PLL_MB	from UDL	-
PLL_MODE	from UDL	-
XCLK	from UDL	-
FCLK	to UDL	undefined
IRQ_UDL(27:0)	from UDL	-
NFIQ_UDL	from UDL	-
nRST	from UDL	-
MPMCNPOR	from UDL	-
HRESETN	to UDL	L (i.e. HRESETN active)
SCLK	from UDL	-
DBGACK	to UDL	L
DBGREQ	from UDL	-
MASK_DBGEN	from UDL	-
BS_TCK	to UDL	undefined
BS_TMS	to UDL	undefined
BS_TRST	to UDL	undefined

2. Electrical Specifications

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage	2.5 V supply	V_{DD1}		-0.5 to +3.6	V
	3.3 V supply	V_{DD2}		-0.5 to 4.6	V
	PLL supply	AV_{DD},DV_{DD}		-0.5 to +3.6	V
I/O voltage		V_I, V_O	V_I, V_O < V_{DD2} + 0.5 V	-0.5 to 4.6	V
Output current		I_O	I_{OL} = 3 mA	10	mA
			I_{OL} = 6 mA	20	mA
			I_{OL} = 9 mA	30	mA
			I_{OL} = 12 mA	40	mA
			I_{OL} = 18 mA	55	mA
			I_{OL} = 24 mA	70	mA
Operating temperature		T_A		-40 to +85	°C
Storage temperature		T_{STG}		-65 to +150	°C

Caution: Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark: Except for buffers with a fail-safe function, always apply 2.5 V or 3.3 V voltage to I/O pins after applying the power supply voltage.

2.2 Operating Conditions

Table 2-2: Recommended Operating Conditions

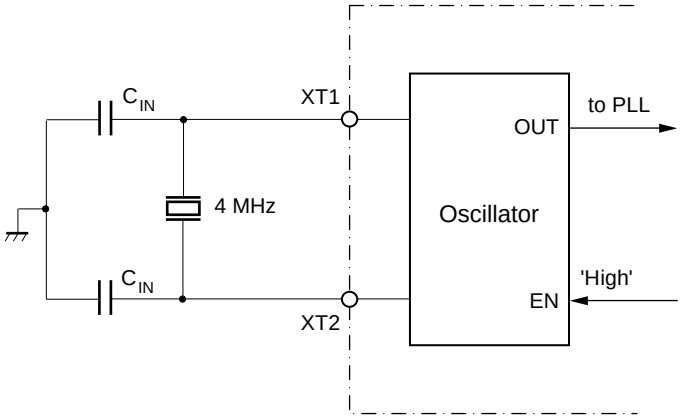
Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	2.5 V supply	V_{DD1}		2.3	2.5	2.7	V
	3.3 V supply	V_{DD2}		3.0	3.3	3.6	V
	PLL supply	AV_{DD}, DV_{DD}		2.3	2.5	2.7	V
Ambient temperature		T_A		-40		+85	°C
Input voltage high		V_{IH}		2		V_{DD2}	V
Input voltage low		V_{IL}		0		0.8	V
Input voltage high for XT1 input		V_{IHXT1}		1.7		V_{DD1}	V
Input voltage low for XT1 input		V_{ILXT1}		0		0.7	V
Positive trigger voltage	Schmitt input	V_P		1.3		2.4	V
Negative trigger voltage		V_N		0.8		1.7	V
Hysteresis voltage		V_H		0.2		1.0	V
Input rise time	Normal input	t_{RI}		0		200	ns
Input fall time		t_{FI}		0		200	ns
Input rise time	Schmitt input	t_{RI}		0		10	ms
Input fall time		t_{FI}		0		10	ms
Operation Clock Frequencies		$f_{CRYSTAL}$			4		MHz
		$f_{Ext. Osc.}$		2		16	MHz
		f_{HCLK}				60	MHz
		f_{SCLK}				100	MHz

Remark: When inputting a slow signal with a long rise / fall time, noise on a signal line may affect the operation. Therefore use a Schmitt trigger input buffer.

2.3 Oscillator Characteristics

(1) Crystal resonator connection

Figure 2-1: Crystal Resonator Connection



(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-3: Oscillator Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	$f_{CRYSTAL}$	V_{DD1} = 2.3 V ~ 2.7 V V_{DD2} = 3.0 V ~ 3.6 V	3.96	4	4.04	MHz
Oscillation stabilization time	t_{OST}			10		ms

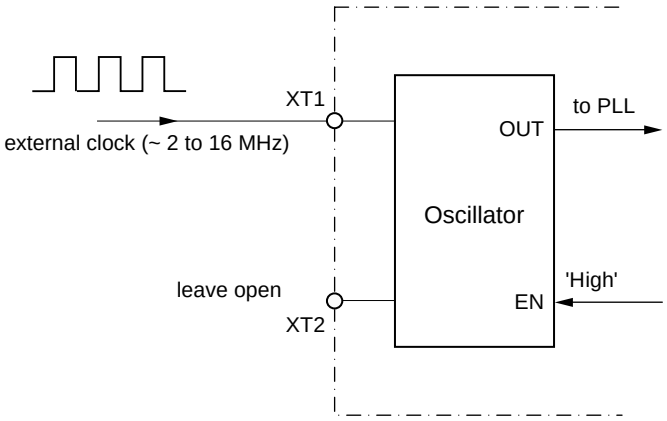
Note: The value of the oscillation stabilization time is just a typical value. It greatly depends on the application (external components, PCB layout).

Caution: Ensure that the duty cycle of oscillation waveform is between 45% and 55%.

Remark: PCB layout recommendations are listed in sub-chapter **(3) on page 29**.

(2) External clock input

Figure 2-2: External Clock Input



The external clock shall be connected to the XT1 input leaving XT2 open.

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-4: Oscillator Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	$f_{Ext. Osc.}$	V_{DD1} = 2.3 V ~ 2.7 V V_{DD2} = 3.0 V ~ 3.6 V	2		16	MHz

Caution: The XT1 input is a 2.5 V input; the voltage level of the clock signal that is attached to XT1 must not exceed the limits given in Table 2-2.

(3) Recommendations for PCB layout

Since crystal oscillators are very EMI sensitive, it is strongly recommended to design the PCB board for the oscillator part very carefully according to the below listed recommendations.

The oscillator consists of an inverter inside System-on-Chip Lite+, that is normally connected to a quartz-crystal. The inverter is bridged by an internal feedback resistor. The inverter within System-on-Chip Lite+ has a high input impedance (XT1 pin) and high output impedance (XT2 pin). The output pin XT2 has a low drive capability in order not to overdrive or damage the crystal. Internally, the oscillator signal is fed via a Schmitt-trigger buffer to an input divider inside the PLL.

In case of a poor PCB layout, noise injection into the on-chip oscillator may cause unintended noise spikes at the output of the internal oscillator buffer stage. The spiky signal will be divided at the PLL input and then further be filtered by the PLL characteristics. In case of an injected noise spike, a slowly decaying frequency disturbance at the PLL output would be observable.

The PCB layout recommendations for the oscillator part are as follows:

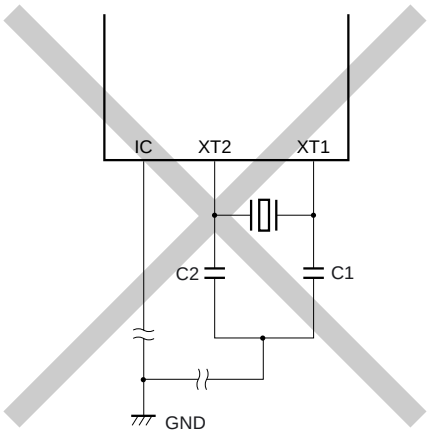
- Ground path distance between the capacitors C1 and C2 and the ground pin GND should be as short as possible.
- The oscillator must not share its ground trace with other signals (please refer to Figure **2-3**).
- Place the crystal resonator and the capacitors C1 and C2 as close as possible to the XT1 and XT2 pins.
- Keep the wiring lengths as short as possible.
- Ensure that no other signals cross or/and accompany the crystal wiring (please refer to Figure **2-3 b/c**).
- Enclose the oscillator circuitry with a ground guard ring as much as possible. Even a very thin guard ring due to PCB routing restrictions, is much better than having no guard ring at all.
- Apply an as complete as possible ground shielding to XT1 and XT2 oscillator signals. Shielding tracks on both sides of XT1 and XT2 oscillator signals must be connected to the ground plane at both ends and at least every 5 to 10 mm. Further, a local ground plane on the adjacent layers may be required.
- Keep any fast switching and/or high fluctuating current flows away from the oscillator lines.
- Do not fetch signals directly from the oscillator (please refer to Figure **2-3 e**)
- As starting value, C1 should be chosen equal to C2. It must be ensured by appropriate measurements that the XT1 input signal does not exceed the maximum ratings. The input level can be decreased, by increasing C1 appropriately. Please contact your crystal vendor for that purpose for further details.

NEC strongly recommends to prove the effectiveness of these measures after E/S silicon availability in an early stage of the project.

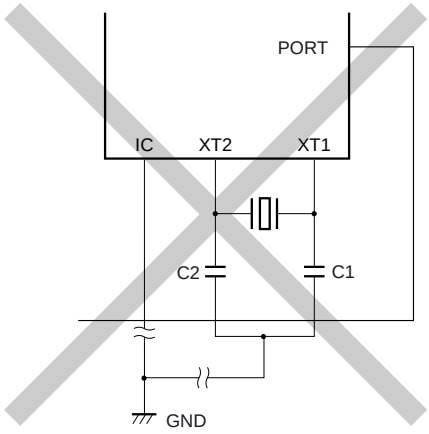
If your system is sensitive to sporadic frequency disturbances due to injected noise, we recommend to use an external crystal oscillator instead (see Figure **2-2**). Keep the wiring between external oscillator and XT1 pin short.

Figure 2-3: Examples of Incorrect Resonator Connection (1/2)

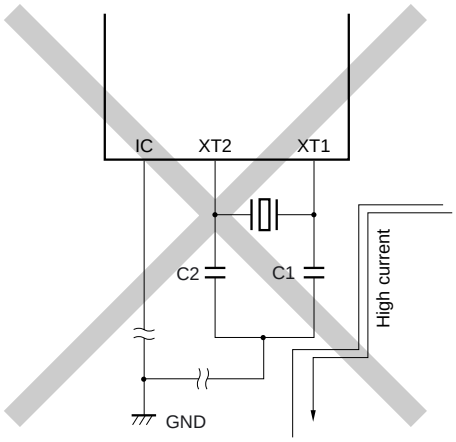
(a) Too long wiring



(b) Crossed signal line



(c) Wiring near high alternating current



(d) Current flowing through ground line of oscillator (potential at points A, B and C fluctuates)

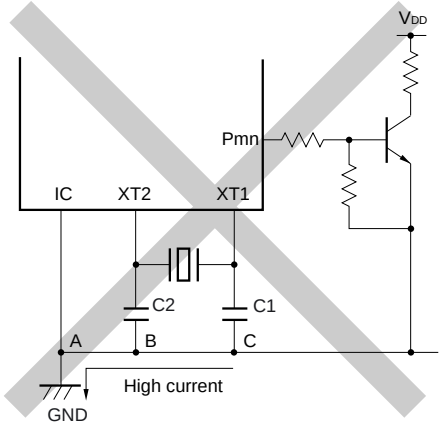
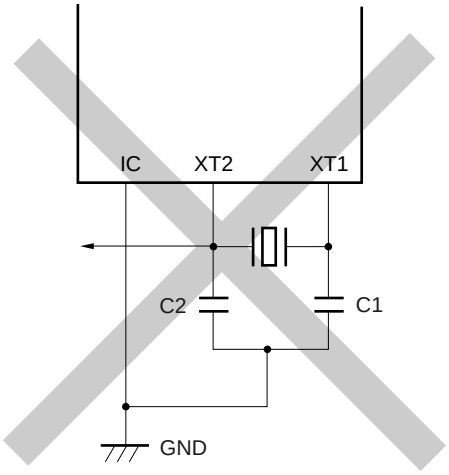


Figure 2-3: Examples of Incorrect Resonator Connection (2/2)

(e) Signals are fetched



2.4 PLL Characteristics

(T_A = -40 to +85°C, AV_{DD} = 2.3 V ~ 2.7 V, DV_{DD} = 2.3 V ~ 2.7 V)

Table 2-5: PLL Recommended Operation Range

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Analog supply voltage	AV_{DD}		2.3	2.5	2.7	V
Digital supply voltage	DV_{DD}		2.3	2.5	2.7	V
PLL input frequency	f_{XCLK}		2		160	MHz
PFD input frequency			1		80	MHz
Input duty ratio			30		70	%
Input rise time	t_r	From 10% to 90% of DV_{DD}			1.6	ns
Input fall time	t_f	From 90% to 10% of DV_{DD}			1.6	ns
Input high pulse width			1.4			ns
Input low pulse width			1.4			ns
Divide ratio	m	Multiplication rate = n / (m*p)	2		32	
	n		2		128	
	p		1 **Note**		8 **Note**	

Note: Only the following settings are allowed for p: 1, 2, 4 and 8.

(T_A = -40 to +85°C, AV_{DD} = 2.3 V ~ 2.7 V, DV_{DD} = 2.3 V ~ 2.7 V)

Table 2-6: PLL AC Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{ADD}	Operation			20	mA
	I_{ADDS}	Standby			10	μA
VCO output frequency	f_{VCO}	Selected frequency range using S (1:0)	60		270	MHz
Output duty ratio		p = 1	40		60	%
		p = 2, 4, 8	45		55	%
Output period jitter	t_{pj}	peak to peak			0.4	ns
Output long term jitter	t_{lj}	peak to peak			2.0	ns
Lock up time	t_{lo}			300	1000	μs

2.5 DC Characteristics

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-7: DC Characteristics

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Output voltage high	2.5 or 3.3 V output	V_{OH}	I_{OH} = 0 mA	V_{DD} - 0.1 V			V
Output voltage low	2.5 or 3.3 V output	V_{OL}	I_{OL} = 0 mA			0.1	V
OFF-state output current	2.5 or 3.3 V output	I_{OZ}	V_O = V_{DD} or GND			±10	μA
Output short-circuit current**Note 1**		I_{OS}	V_O = GND			-250	mA
Input leakage current (3.3 V I/O buffer)	Normal input	I_I	V_I = V_{DD} or GND		$\pm 10^{-4}$	±10	μA
	With pull-up resistor (50 kΩ)	I_I	V_I = GND	24	72	180	μA
	With pull-up resistor (5 kΩ)	I_I	V_I = GND	200	600	1440	μA
	With pull-down resistor (50 kΩ)	I_I	V_I = V_{DD}	24	72	180	μA
Pull-up resistor**Note 2**	50 kΩ	R_{PU}	V_I = V_{DD}	20	45	125	kΩ
	5 kΩ			2.5	5.5	15	kΩ
Pull-down resistor**Note 2**	50 kΩ	R_{PD}	V_I = GND	20	45	125	kΩ
Low-level output current (3.3V I/O buffer)**Note 3**	3 mA type	I_{OL}	V_{OL} = 0.4 V	3			mA
	6 mA type			6			mA
	9 mA type			9			mA
	12 mA type			12			mA
Low-level output current	USB buffer	I_{OL}	V_{OL} = 0.4 V	18			mA
High-level output current (3.3V I/O buffer)**Note 3**	3 mA type	I_{OH}	V_{OH} = 2.4 V	3			mA
	6 mA type			6			mA
	9 mA type			9			mA
	12 mA type			12			mA
High-level output current	USB buffer	I_{OH}	V_{OH} = 2.4 V	24			mA
Supply Current**Note 4**	SCLK = 60 MHz CLKRATIO = 1:1	I_{DD1}**Note 5**			225	450	mA
		I_{DD2}**Note 5**			55	110	mA
	SCLK = 100 MHz CLKRATIO = 2:1	I_{DD1}**Note 5**			210	420	mA
		I_{DD2}**Note 5**			60	120	mA

Notes: 1. The output short-circuit time is 1 second or less per pin of the device.

2. The pull-up and pull-down resistances vary depending on the input and output voltages.

3. All buffers with the same output drive capability have the same specifications.

4. Supply currents refer only to the ARM subsystem. The current contribution of the UDL is customer specific and needs to be determined by the customer.

5. I_{DD1} refers to the 2.5 V supply voltage; I_{DD2} refers to the 3.3 V supply voltage

Remark: The + and - signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by -.

2.6 AC Characteristics

2.6.1 General

Table 2-8: Conditions for AC Characteristics

	UDL Signals	External Signals (Pins)
Ambient temperature	T_A = -40 to +85°C	
Operating voltages	V_{DD1} = 2.5 V ± 0.2 V, V_{SS} = 0 V V_{DD2} = 3.3 V ± 0.3 V	
Input signal rise/fall time	ideal (= 0 ns)	
Output signal load capacitance	C_L = 1 pF	C_L = 50 pF

Figure 2-4: AC Test Input Measurement Points (external signals)

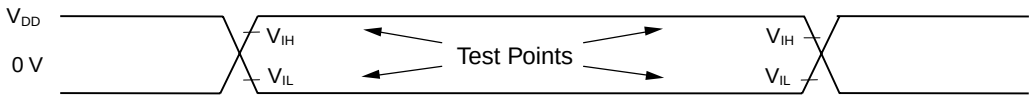


Figure 2-5: AC Test Output Measurement Points (external signals)

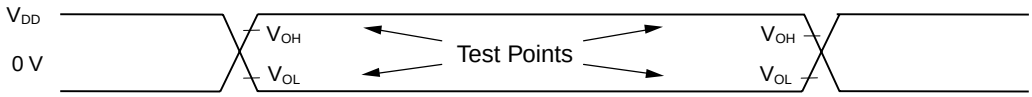
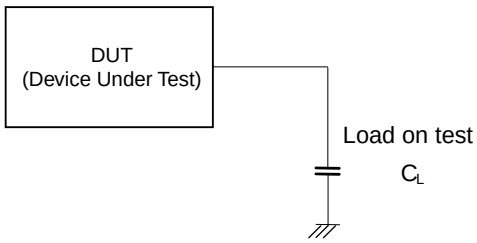


Figure 2-6: AC Test Load Condition



Caution: If the load capacitance of external signals (pins) exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

Remark: A minimum capacitive load of 10 pf is required on the FBCLKIN(3:0) inputs.

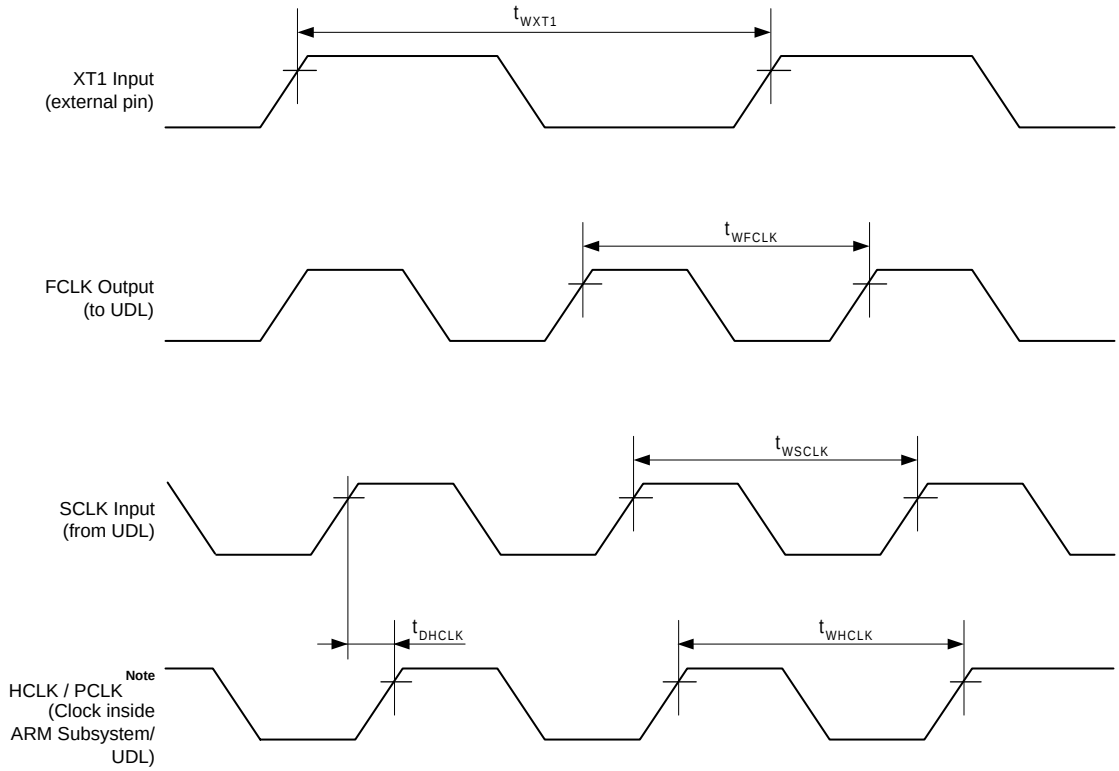
2.6.2 Clock timing

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-9: Clock AC Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
XT1 input cycle	t_{WXT1}	Crystal	247.52	250	252.52	ns
		External oscillator	62.5		500	ns
XT1 input clock duty cycle			45		55	%
FCLK output cycle	t_{WFCLK}		3.906			ns
FCLK clock duty cycle		p = 2,4,8	45		55	%
		p = 1	40		60	%
SCLK input cycle	t_{WSCLK}	CLKRATIO = 1	10			ns
		CLKRATIO = 0	16.67			ns
SCLK clock duty cycle			45		55	%
HCLK output cycle	t_{WHCLK}	CLKRATIO = 1	20			ns
		CLKRATIO = 0	16.67			ns
HCLK clock duty cycle			45		55	%
delay time from SCLK to HCLK	t_{DHCLK}	for μPD66702	2.9		7.8	ns
		for μPD66703	3.4		9	ns

Figure 2-7: Clock Waveforms



2.6.3 Static memory interface

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-10: Static Memory Interface Timing Parameters for μPD66702 (1/2)

	Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Read	Address valid time before nXCSS↓	$t_{VXADDR1}$			-1.01	ns
	Delay time from nXCSS↓ to nXOE↓	t_{DnXOE1}		WAITOEN × T + 0.18	WAITOEN × T + 0.63	ns
	Delay time from nXCSS↑ to nXOE↑	t_{DnXOE2}		0.35		ns
	nXCSS low level width (single read)	$t_{WnXCSS1}$		(WAITRD+1) × T - 0.72		ns
	nXCSS low level width (page mode)	$t_{WnXCSS2}$		(WAITRD + 4 × WAIT-PAGE + 5) × T		ns
	Data input valid after nXOE↓ (single read)	$t_{VXDATA1}$			WAITRD × T + 2.95	ns
	Data input valid after address (burst read)	$t_{VXDATA2}$			WAITRD × T + 2.57	ns
	Data input valid after nXOE↓ (1st read in page mode)	$t_{VXDATA3}$			WAITRD × T + 2.95	ns
	Data input valid after address (inside page)	$t_{VXDATA4}$			WAITPAGE × T + 2.57	ns
	Data input hold time (after nXCSS↑)	$t_{HXDATA1}$		0		ns
Write	Delay time from nXCSS↓ to nXWEN↓	t_{DnXWEN}		(WAITWEN+1) × T - 0.96		ns
	Delay time from nXCS↓ to nXBLS↓	$t_{DnXBLS1}$		(WAITWEN+1) × T - 0.5		ns
	nXWEN low level width	t_{WnXWEN}		(WAITWR - WAITWEN + 1) × T - 0.34		ns
	nXBLS low level width	t_{WnXBLS}		(WAITWR - WAITWEN + 1) × T - 1.7		ns
	Delay time from nXWEN↑ to nXCSS↑ **Note 1**	$t_{DnXCSS1}$		T + 0.14		ns
	Delay time from nXBLS↑ to nXCSS↑ **Note 1**	$t_{DnXCSS2}$		T - 1.88		ns
	Address valid time before nXWEN↓	$t_{VXADDR2}$		T - 0.5		ns
	Data valid time before nXWEN↓	$t_{VXDATA5}$		T - 0.4		ns
	Data output hold time (from nXWEN↑) **Note 1**	$t_{HXDATA2}$		T- 2.29		ns
	Data output hold time (from nXBLS↑) **Note 1**	$t_{HXDATA3}$		T - 3.46		ns
	nXCSS low level width **Note 2**	$t_{WnXCSS3}$		(WAITWR - WAITWEN + 3) × T - 0.72		ns
	Delay time from nXWEN↓ / nXBLS↓ to next nXWEN↓ / nXBLS↓	t_{DSWE}		(5 + WAITWR) × T		ns

Table 2-10: Static Memory Interface Timing Parameters for μPD66702 (2/2)

	Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Write	Address hold time (from nXWEN↑) **Note 1**	$t_{HXADDR1}$		T - 1.87		ns
	Address hold time (from nXBLS↑) **Note 1**	$t_{HXADDR2}$		T - 3.04		ns
Turn around	nXCSS high level width (turn around inside the same memory bank, read before write)	$t_{WnXCSS4}$		(WAITTR + 1) × T - 0.81 (for WAITTR > 2)		ns
	nXCSS high level width (turn around inside the same memory bank, write before read)	$t_{WnXCSS5}$		2 × T - 0.81		ns
	nXCSS high level width (turn around to a different memory bank)	$t_{WnXCSS6}$		(WAITTR +2) × T - 0.5		ns

Notes: 1. Write access inside the same memory bank.

2. Consecutive write access to a different memory bank.

Remarks: 1. T: Clock period of SCLK

2. WAITOEN: corresponds to the content of the WAITOEN field in the respective MPMCStaticWaitOen register

3. WAITRD: corresponds to the content of the WAITRD field in the respective MPMCStaticWaitRd register

4. WAITWEN: corresponds to the content of the WAITWEN field in the respective MPMCStaticWaitWen register

5. WAITWR: corresponds to the content of the WAITWR field in the respective MPMCStaticWaitWr register

6. WAITTR: corresponds to the content of the WAITTR field in the respective MPMCStaticWaitTurn register

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V

Table 2-11: Static Memory Interface Timing Parameters for μPD66703 (1/2)

	Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Read	Address valid time before nXCSS↓	$t_{VXADDR1}$			-0.7	ns
	Delay time from nXCSS↓ to nXOE↓	t_{DnXOE1}		WAITOEN × T + 0.3	WAITOEN × T + 0.5	ns
	Delay time from nXCSS↑ to nXOE↑	t_{DnXOE2}		0.38		ns
	nXCSS low level width (single read)	$t_{WnXCSS1}$		(WAITRD+1) × T - 0.42		
	nXCSS low level width (page mode)	$t_{WnXCSS2}$		(WAITRD + 4 × WAIT-PAGE + 5) × T		ns
	Data input valid after nXOE↓ (single read)	$t_{VXDATA1}$			WAITRD × T + 2.69	ns
	Data input valid after address (burst read)	$t_{VXDATA2}$			WAITRD × T + 2.49	ns
	Data input valid after nXOE↓ (1st read in page mode)	$t_{VXDATA3}$			WAITRD × T + 2.69	ns
	Data input valid after address (inside page)	$t_{VXDATA4}$			WAITPAGE × T + 2.49	ns
	Data input hold time (after nXCSS↑)	$t_{HXDATA1}$		0		ns
Write	Delay time from nXCSS↓ to nXWEN↓	t_{DnXWEN}		(WAITWEN + 1) × T - 0.64		ns
	Delay time from nXCS↓ to nXBLS↓	$t_{DnXBLS1}$		(WAITWEN + 1) × T - 1.4		ns
	nXWEN low level width	t_{WnXWEN}		(WAITWR - WAITWEN + 1) × T - 0.24		ns
	nXBLS low level width	t_{WnXBLS}		(WAITWR - WAITWEN + 1) × T - 0.16		ns
	Delay time from nXWEN↑ to nXCSS↑ **Note 1**	$t_{DnXCSS1}$		T - 1.2		ns
	Delay time from nXBLS↑ to nXCSS↑ **Note 1**	$t_{DnXCSS2}$		T - 1.88		ns
	Address valid time before nXWEN↓	$t_{VXADDR2}$		T - 0.5		ns
	Data valid time before nXWEN↓	$t_{VXDATA5}$		T - 0.4		ns
	Data output hold time (from nXWEN↑) **Note 1**	$t_{HXDATA2}$		T- 2.4		ns
	Data output hold time (from nXBLS↑) **Note 1**	$t_{HXDATA3}$		T - 3.08		ns
	nXCSS low level width **Note 2**	$t_{WnXCSS3}$		(WAITWR - WAITWEN + 3) × T - 0.42		ns
	Delay time from nXWEN↓ / nXBLS↓ to next nXWEN↓ / nXBLS↓	t_{DSWE}		(5 + WAITWR) × T		ns

Table 2-11: Static Memory Interface Timing Parameters for μPD66703 (2/2)

	Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Write	Address hold time (from nXWEN↑) **Note 1**	$t_{HXADDR1}$		T - 1.89		ns
	Address hold time (from nXBLS↑) **Note 1**	$t_{HXADDR2}$		T - 2.57		ns
Turn Around	nXCSS high level width (turn around inside the same memory bank, read before write)	$t_{WnXCSS4}$		(WAITTR + 1) × T - 0.81 (for WAITTR > 2)		ns
	nXCSS high level width (turn around inside the same memory bank, write before read)	$t_{WnXCSS5}$		2 × T - 0.81		ns
	nXCSS high level width (turn around to a different memory bank)	$t_{WnXCSS6}$		(WAITTR +2) × T - 0.5		ns

Notes: 1. Write access inside the same memory bank.

2. Consecutive write access to a different memory bank.

Remarks: 1. T: Clock period of SCLK

2. WAITOEN: corresponds to the content of the WAITOEN field in the respective MPMCStaticWaitOen register

3. WAITRD: corresponds to the content of the WAITRD field in the respective MPMCStaticWaitRd register

4. WAITWEN: corresponds to the content of the WAITWEN field in the respective MPMCStaticWaitWen register

5. WAITWR: corresponds to the content of the WAITWR field in the respective MPMCStaticWaitWr register

6. WAITTR: corresponds to the content of the WAITTR field in the respective MPMCStaticWaitTurn register

Figure 2-8: Static Memory Single Read Cycle Example

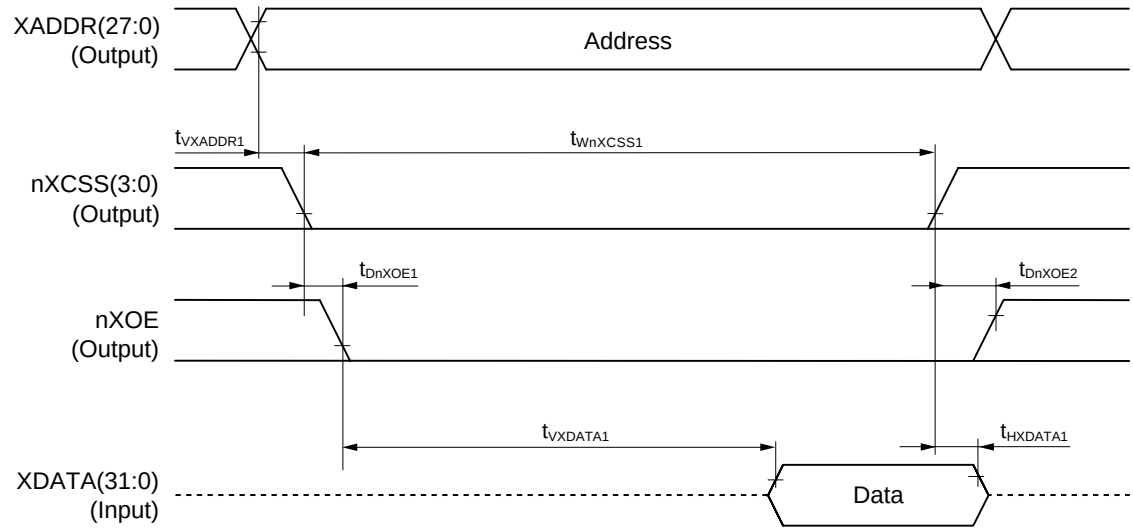


Figure 2-9: Static Memory Burst Read Cycle Example

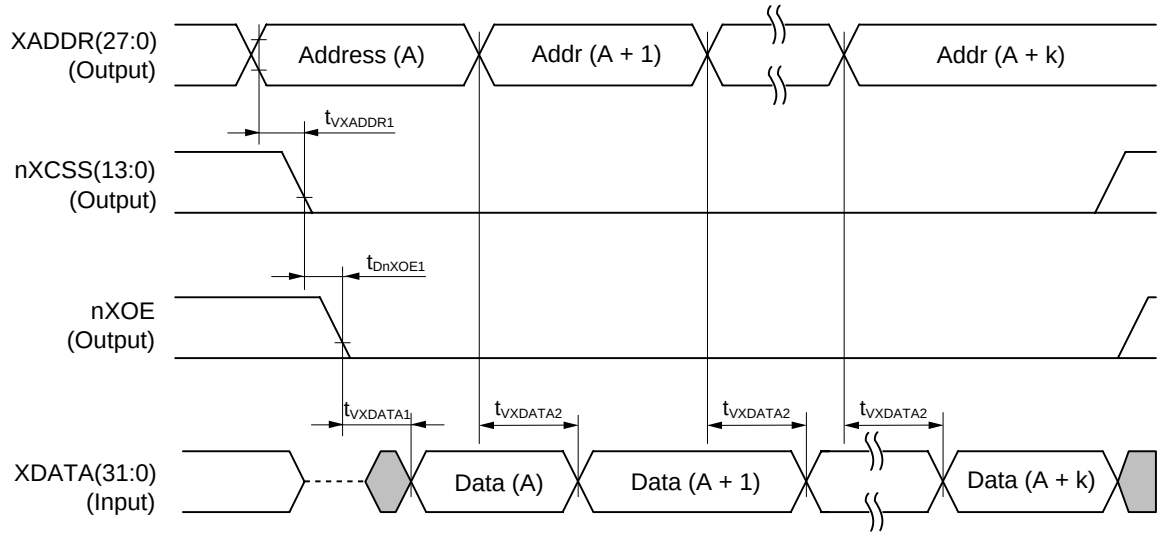


Figure 2-10: Static Memory Page Mode Read Cycle Example

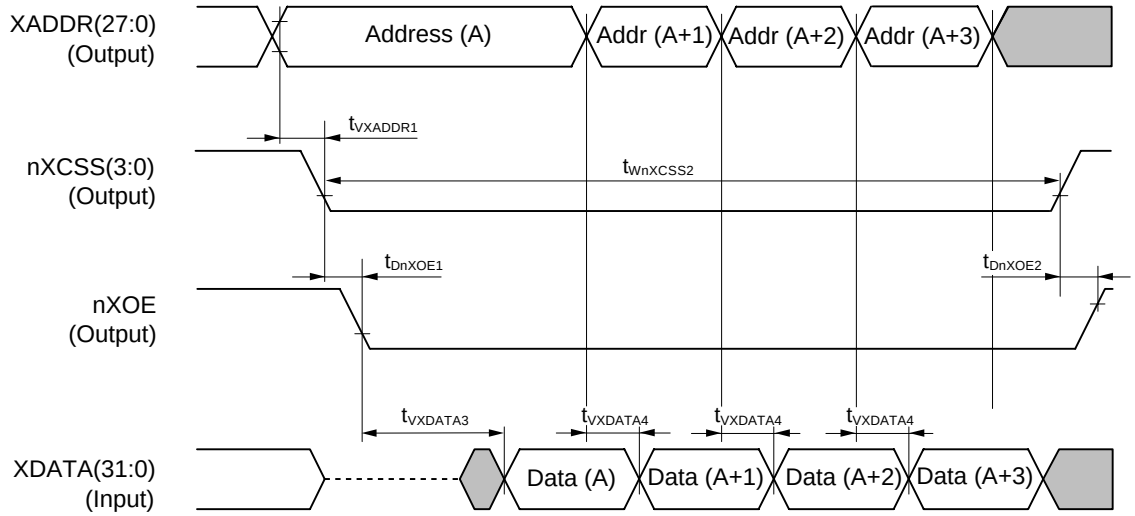
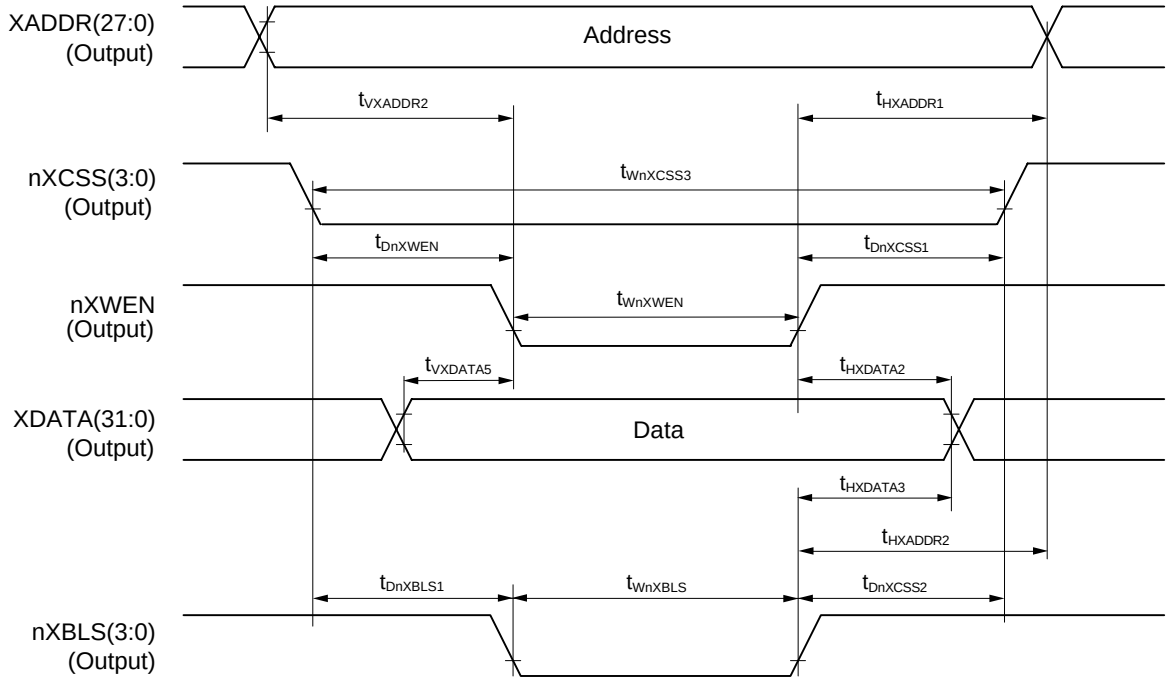


Figure 2-11: Static Memory Single Write Cycle Example (nXWEN controlled)



Remark: Write accesses to static memory are always nXWEN-controlled.

Figure 2-12: Static Memory Single Write Cycles to different Memory Banks (Example)

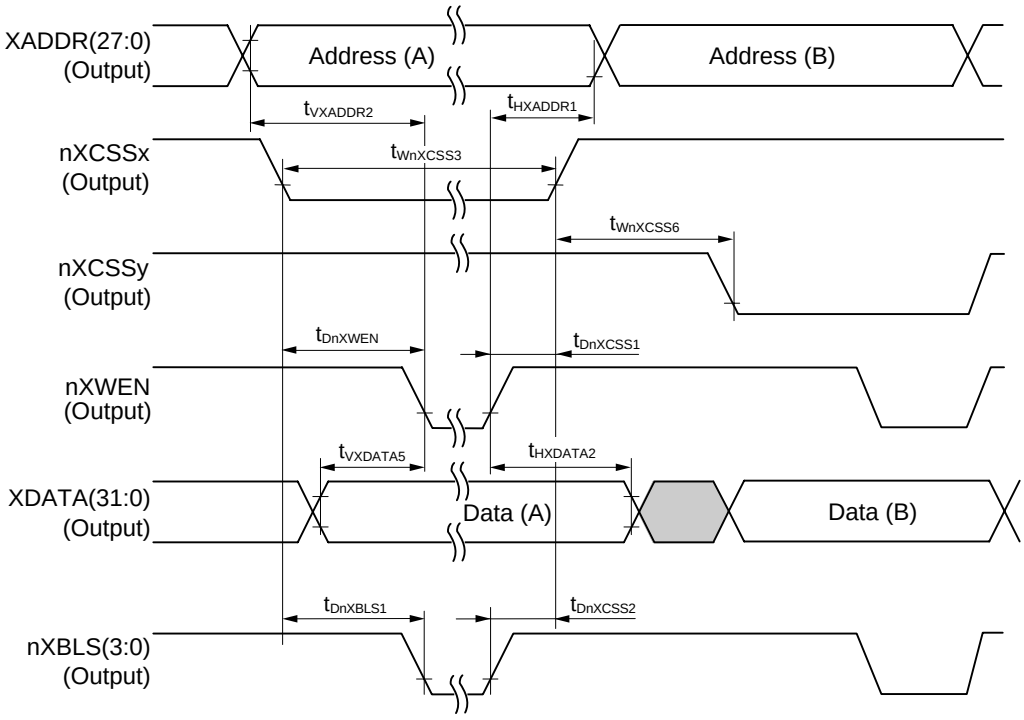


Figure 2-13: Static Memory Single Read before Single Write Cycle (Example)

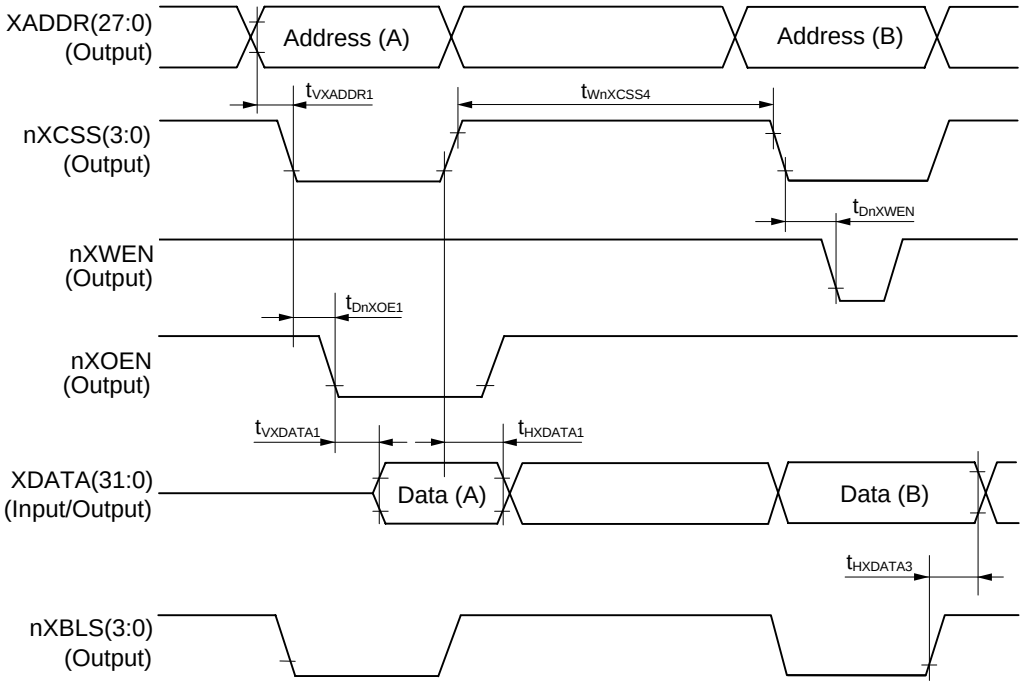
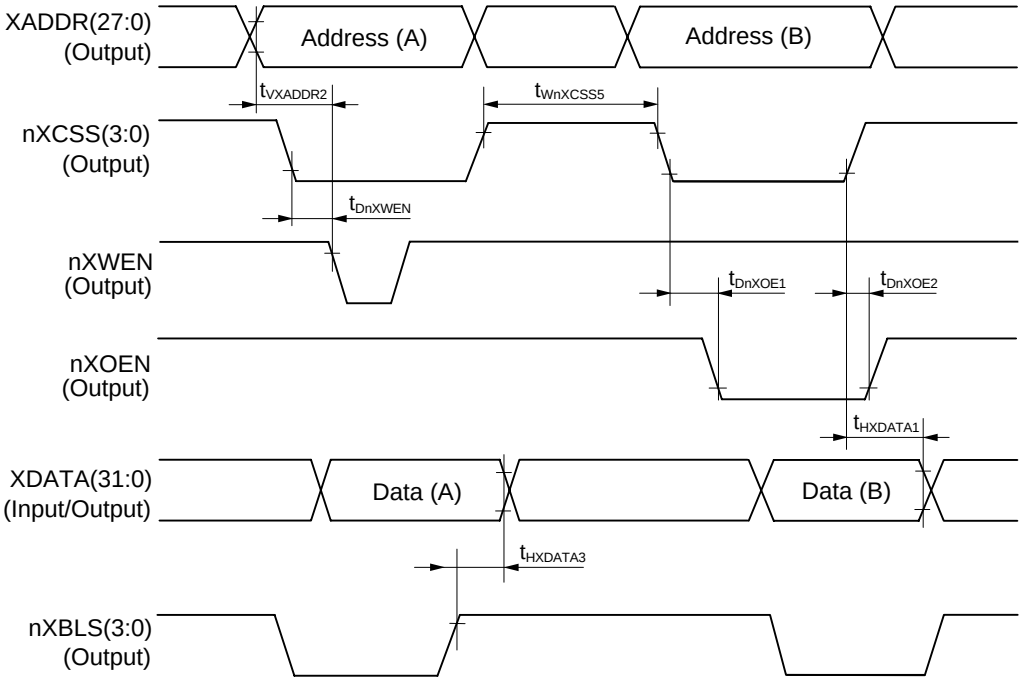


Figure 2-14: Static Memory Single Write before Single Read Cycle (Example)



2.6.4 Dynamic memory interface

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-12: Dynamic Memory Interface Timing Parameters for μPD66702

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
XDATA delay time from CLKOUT↑	t_{DXDATA}			T/2 + 3.15	ns
XADDR delay time from CLKOUT↑	t_{DXADDR}			T/2 + 2.43	ns
CKEOUT delay time from CLKOUT↑	$t_{DCKEOUT}$			T/2 + 1.88	ns
DQMOUT delay time from CLKOUT↑	$t_{DDQMOUT}$			T/2 + 1.95	ns
nXCSD delay time from CLKOUT↑	t_{DnXCSD}			T/2 + 1.92	ns
nRASOUT delay time from CLKOUT↑	$t_{DnRASOUT}$			T/2 + 1.02	ns
nCASOUT delay time from CLKOUT↑	$t_{DnCASOUT}$			T/2 + 0.82	ns
nXWEN delay time from CLKOUT↑	t_{DnXWEN}			T/2 + 1.15	ns
XDATA input setup time	t_{SXDATA}		1.56	-	ns
XDATA input hold time	t_{HXDATA}		0.81	-	ns
FBCLKIN cycle time	-		10		ns
Mode register set to ACT command**Note**	t_{MRD}		1	16	clocks
ACT to REF/ACT command period (Operation)**Note**	t_{RC}		1	32	clocks
Auto-refresh period**Note**	t_{RFC}		1	32	clocks
ACT to PRE command period**Note**	t_{RAS}		1	16	clocks
PRE to ACT command period**Note**	t_{RP}		1	16	clocks
ACT (one) to ACT (another) command period**Note**	t_{RRD}		1	16	clocks
Self-refresh exit time**Note**	t_{SREX}		1	16	clocks
Last data-in to active command time**Note**	t_{DAL}		0	15	clocks
Last data-out to active command time**Note**	t_{APR}		1	16	clocks
Write recovery time**Note**	t_{WR}		1	16	clocks
Exit self-refresh to active command time**Note**	t_{XSR}		1	32	clocks

Note: This parameter is software configurable using a control register of the System-on-Chip Lite+ memory controller. Please consult the user's manual for details.

Remark: T/2 corresponds to a half period of the CLKOUT(3:0) signal.

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-13: Dynamic Memory Interface Timing Parameters for μPD66703

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
XDATA delay time from CLKOUT↑	t_{DXDATA}			T/2 + 3.48	ns
XADDR delay time from CLKOUT↑	t_{DXADDR}			T/2 + 2.84	ns
CKEOUT delay time from CLKOUT↑	$t_{DCKEOUT}$			T/2 + 2.27	ns
DQMOUT delay time from CLKOUT↑	$t_{DDQMOUT}$			T/2 + 2.11	ns
nXCSD delay time from CLKOUT↑	t_{DnXCSD}			T/2 + 2.32	ns
nRASOUT delay time from CLKOUT↑	$t_{DnRASOUT}$			T/2 + 1.42	ns
nCASOUT delay time from CLKOUT↑	$t_{DnCASOUT}$			T/2 + 1.22	ns
nXWEN delay time from CLKOUT↑	t_{DnXWEN}			T/2 + 1.57	ns
XDATA input setup time	t_{SXDATA}		0.8	-	ns
XDATA input hold time	t_{HXDATA}		1.04	-	ns
FBCLKIN cycle time	-		10		ns
Mode register set to ACT command**Note**	t_{MRD}		1	16	clocks
ACT to REF/ACT command period (Operation)**Note**	t_{RC}		1	32	clocks
Auto-refresh period**Note**	t_{RFC}		1	32	clocks
ACT to PRE command period**Note**	t_{RAS}		1	16	clocks
PRE to ACT command period**Note**	t_{RP}		1	16	clocks
ACT (one) to ACT (another) command period**Note**	t_{RRD}		1	16	clocks
Self-refresh exit time**Note**	t_{SREX}		1	16	clocks
Last data-in to active command time**Note**	t_{DAL}		0	15	clocks
Last data-out to active command time**Note**	t_{APR}		1	16	clocks
Write recovery time**Note**	t_{WR}		1	16	clocks
Exit self-refresh to active command time**Note**	t_{XSR}		1	32	clocks

Note: This parameter is software configurable using a control register of the System-on-Chip Lite+ memory controller. Please consult the user's manual for details.

Remark: T/2 corresponds to a half period of the CLKOUT(3:0) signal.

Figure 2-15: Example of 32-bit Dynamic Memory Read Cycle Example (CAS Latency of 3)

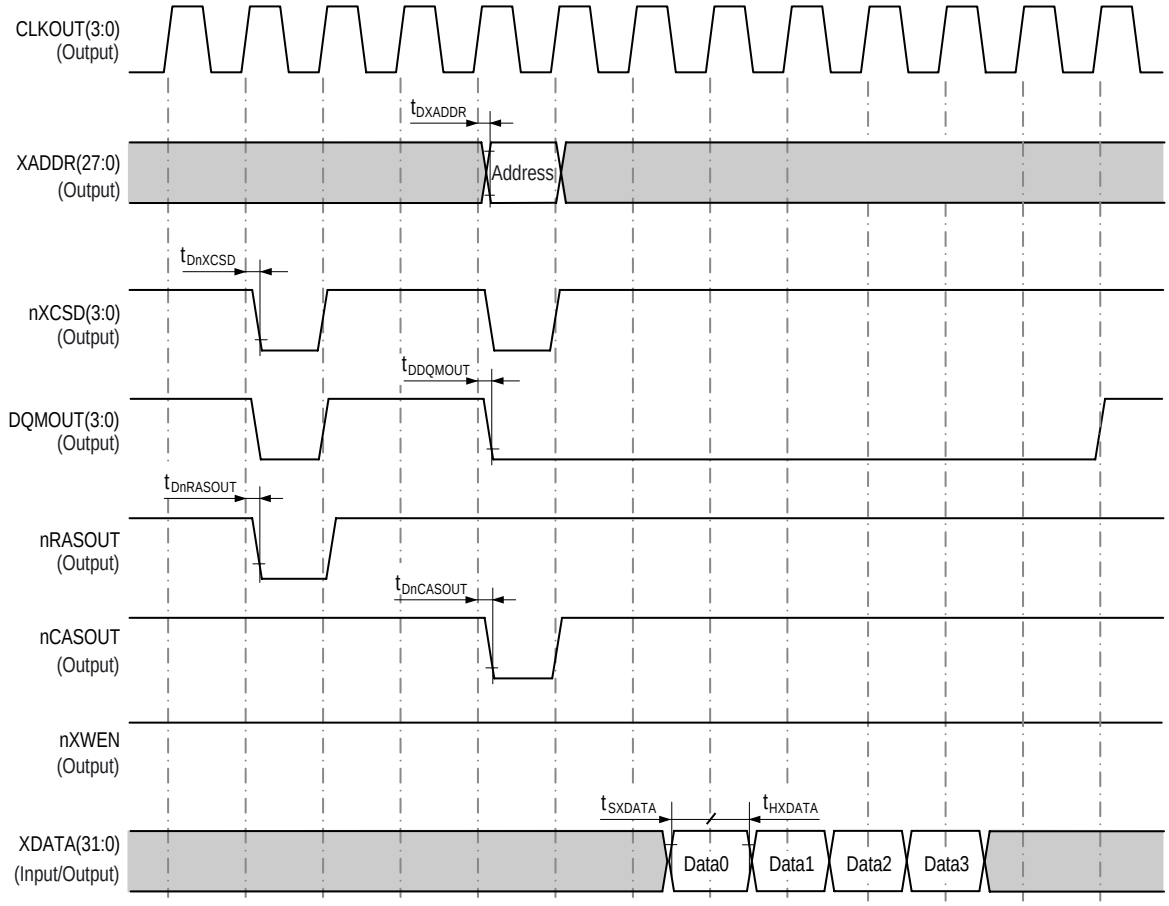


Figure 2-16: Example of 16-bit Dynamic Memory Read Cycle Example (CAS Latency of 3)

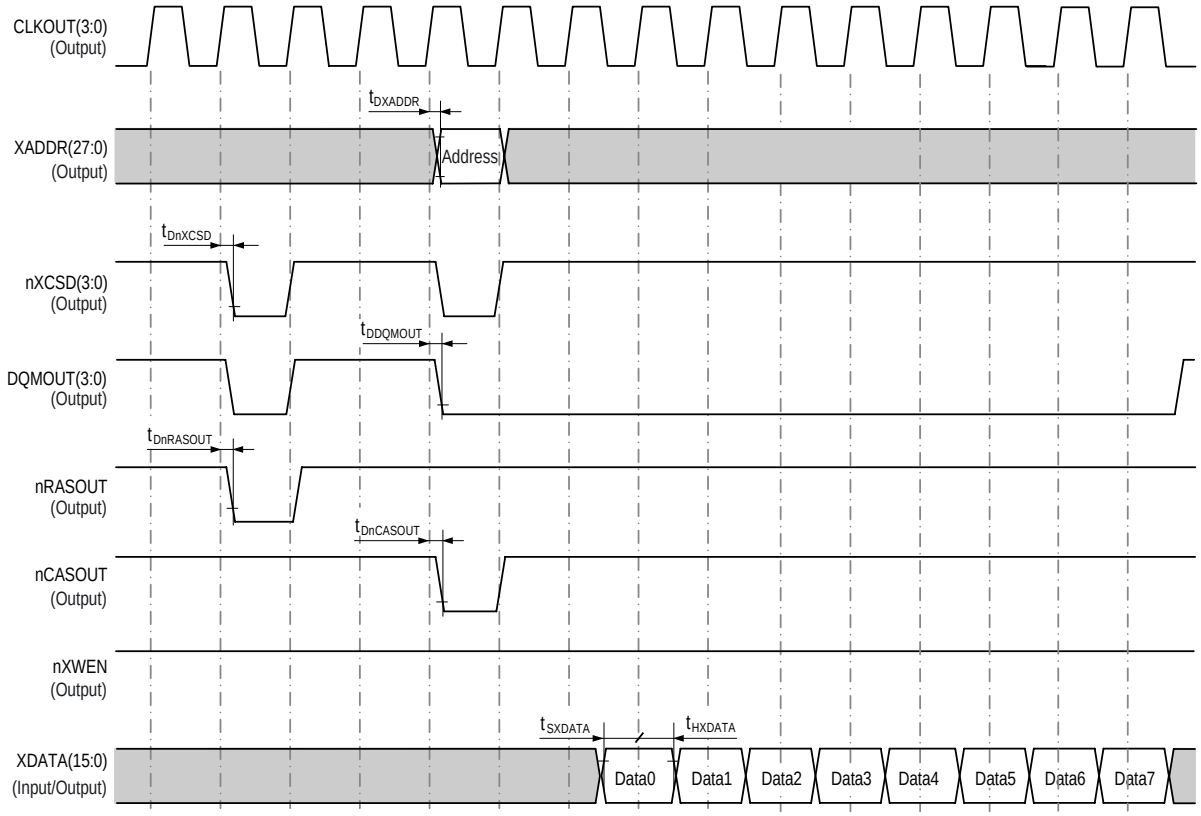


Figure 2-17: Example of 32-bit Dynamic Memory Write Cycle Example (CAS Latency of 3)

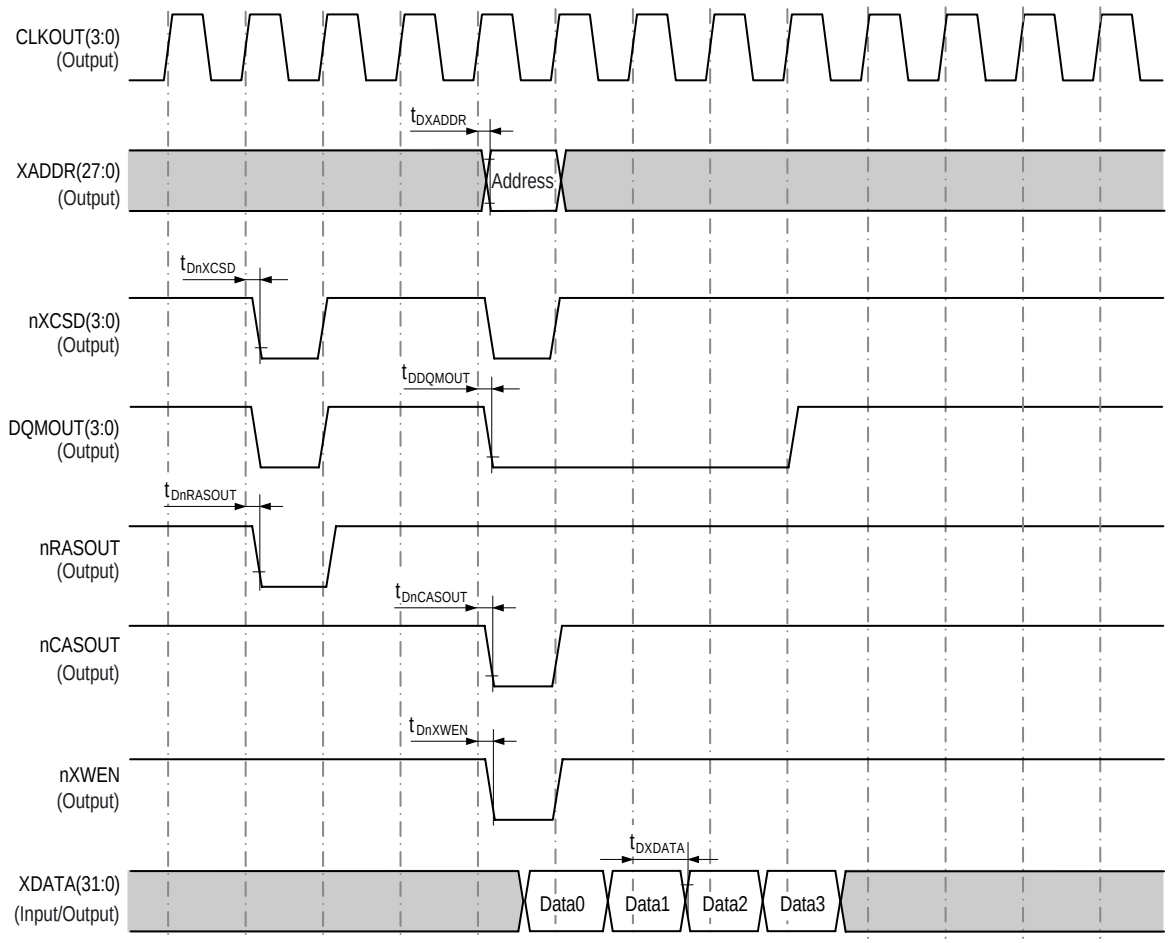
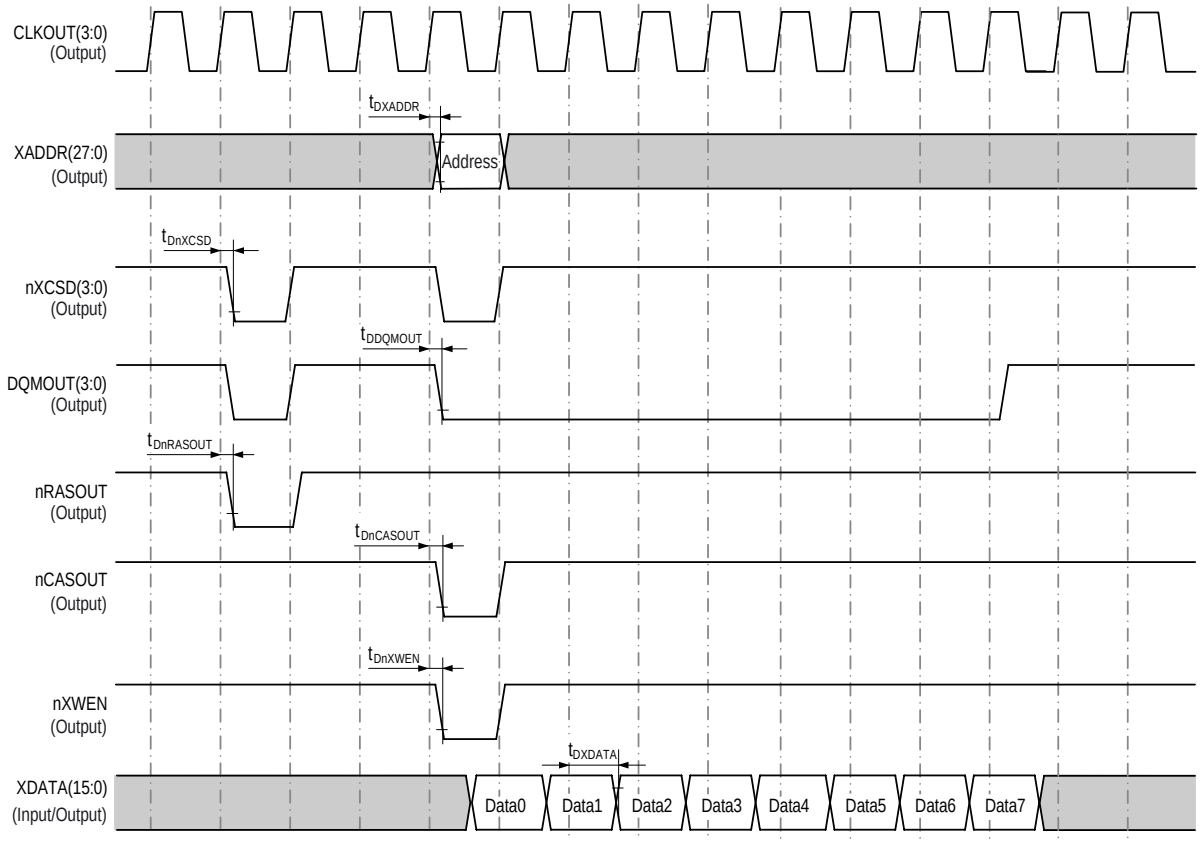


Figure 2-18: Example of 16-bit Dynamic Memory Write Cycle Example (CAS Latency of 3)



2.6.5 Ethernet (MII) interface parameters

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-14: Ethernet (MII) Interface Parameters for μPD66702

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
TXCLK period		10 Mbps operation	400			ns
		100 Mbps operation	40			ns
TXCLK duty cycle		10/100 Mbps operation	40		60	%
TXEN output delay	t_{DTXEN}				8.56	ns
TXER output delay	t_{DTXER}				8.2	ns
TXD(3:0) output delay	t_{DTXD}				9.37	ns
COL setup time	t_{SCOL}		0.75			ns
COL hold time	t_{HCOL}		2.1			ns
RXCLK period		10 Mbps operation	400			ns
		100 Mbps operation	40			ns
RXCLK duty cycle		10/100 Mbps operation	40		60	%
RXDV setup time	t_{SRXDV}		-0.12			ns
RXDV hold time	t_{HRXDV}		2.22			ns
RXD(3:0) setup time	t_{SRXD}		0.07			ns
RXD(3:0) hold time	t_{HRXD}		3.1			ns
RXER setup time	t_{SRXER}		-0.06			ns
RXER hold time	t_{HRXER}		2.5			ns
CRS setup time	t_{SCRS}		0.13			ns
CRS hold time	t_{HCRS}		1.73			ns
MDC period			400			ns
MDIO output delay	t_{DMDIO}				14.91	ns
MDIO setup time	t_{SMDIO}		5.3			ns
MDIO hold time	t_{HMDIO}		5.62			ns

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-15: Ethernet (MII) Interface Parameters for μPD66703

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
TXCLK period		10 Mbps operation	400			ns
		100 Mbps operation	40			ns
TXCLK duty cycle		10/100 Mbps operation	40		60	%
TXEN output delay	t_{DTXEN}				9.9	ns
TXER output delay	t_{DTXER}				9.86	ns
TXD(3:0) output delay	t_{DTXD}				10.34	ns
COL setup time	t_{SCOL}		0.01			ns
COL hold time	t_{HCOL}		2.14			ns
RXCLK period		10 Mbps operation	400			ns
		100 Mbps operation	40			ns
RXCLK duty cycle		10/100 Mbps operation	40		60	%
RXDV setup time	t_{SRXDV}		0.17			ns
RXDV hold time	t_{HRXDV}		2.55			ns
RXD(3:0) setup time	t_{SRXD}		-0.26			ns
RXD(3:0) hold time	t_{HRXD}		3.01			ns
RXER setup time	t_{SRXER}		-0.34			ns
RXER hold time	t_{HRXER}		3.03			ns
CRS setup time	t_{SCRS}		-0.08			ns
CRS hold time	t_{HCRS}		1.33			ns
MDC period			400			ns
MDIO output delay	t_{DMDIO}				16.42	ns
MDIO setup time	t_{SMDIO}		-1.75			ns
MDIO hold time	t_{HMDIO}		7.18			ns

Figure 2-19: Transmit Interface Block Timing

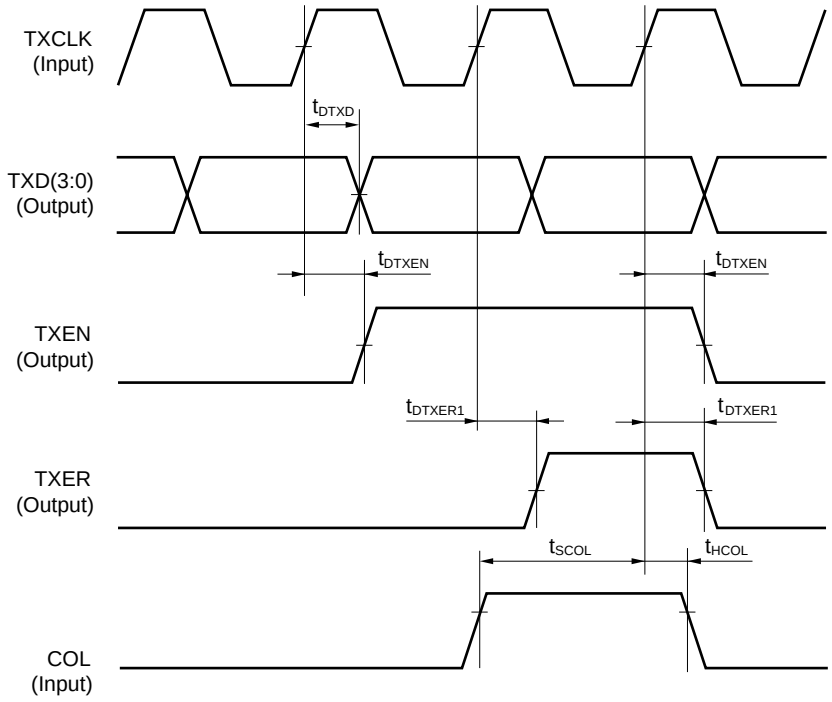


Figure 2-20: Receive Interface Block Timing

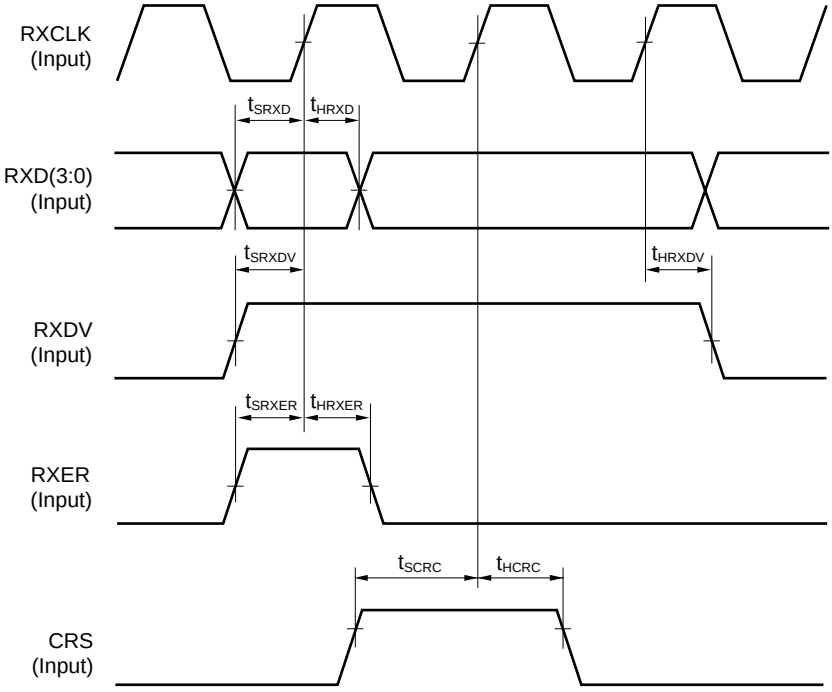
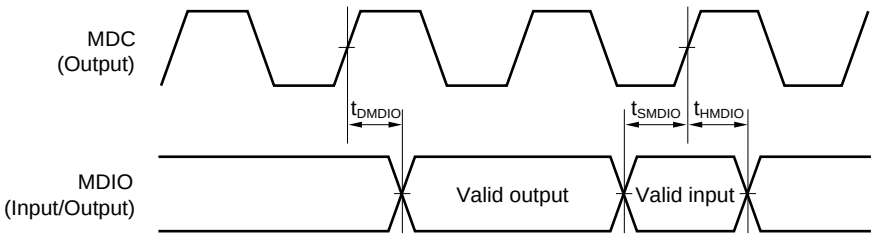


Figure 2-21: Management Interface Block Timing



2.6.6 Reset timing

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-16: Reset AC Characteristics

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
nRST low-level width	t_{WnRST1}	power on reset	1.03		ms
MPMCNPOR low-level width	$t_{WMPMCNPOR}$		1.03		ms
nRST low-level width	t_{WnRST2}	warm reset	4		ns
HRESETn delay from nRST falling edge	$t_{DHRESETn1}$			9	ns
HRESETn delay from nRST rising edge	$t_{DHRESETn2}$			$8 \times T_{SCLK}$	ns

Remark: T_{SCLK}: Clock period of SCLK.

Figure 2-22: Reset Cycle (1/2)

(a) Power-on Reset

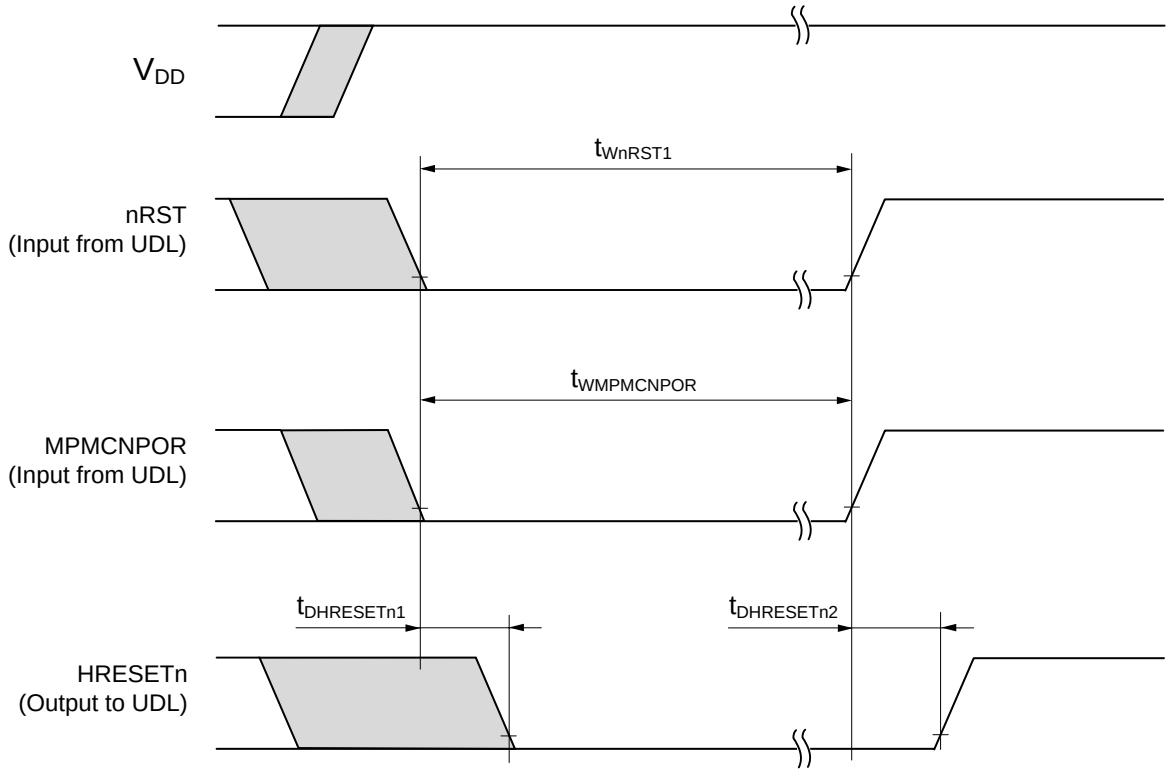
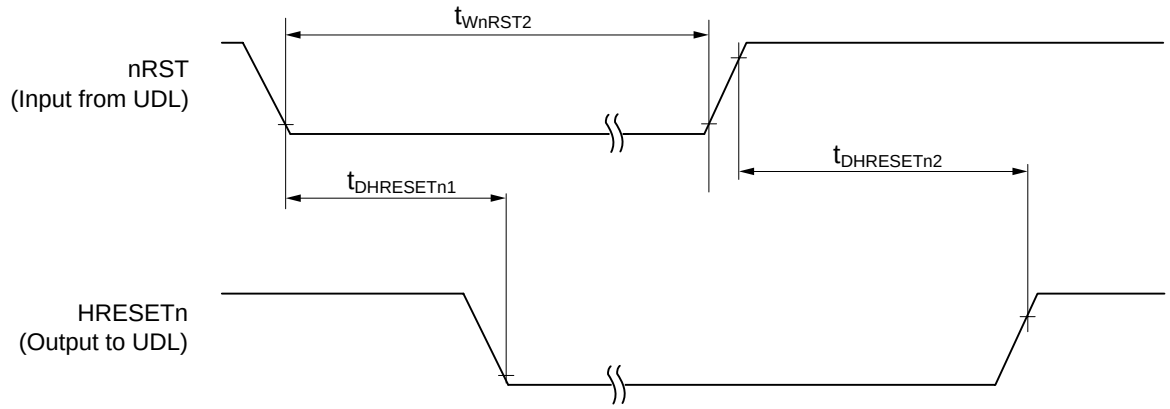


Figure 2-22: Reset Cycle (2/2)

(b) Warm Reset



2.6.7 Interrupt timing

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-17: Interrupt AC Characteristics for μPD66702

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
IRQ_UDL input setup time	t_{SIRQ_UDL}		0.01		ns
IRQ_UDL input hold time	t_{HIRQ_UDL}		6.71		ns
NFIQ_UDL input setup time	t_{SNFIQ_UDL}		-0.21		ns
NFIQ_UDL input hold time	t_{HNFIQ_UDL}		4.06		ns
DBGREQ input setup time	$t_{SDBGREQ}$		-0.08		ns
DBGREQ input hold time	$t_{HDBGREQ}$		3.93		ns
DBGACK delay from SCLK↑	$t_{DDBGACK}$			16.6	ns

Remark: The min. and max. values are related to SCLK.

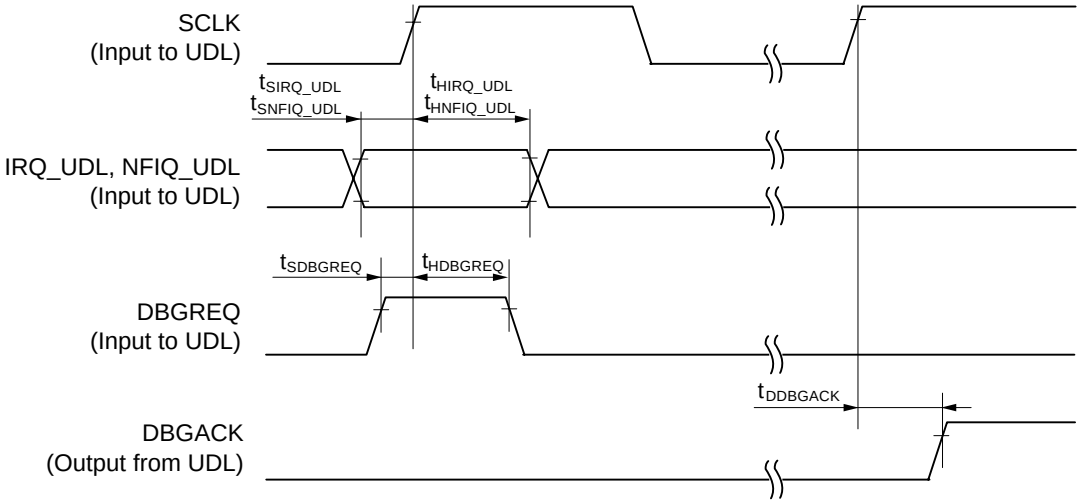
(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-18: Interrupt AC Characteristics for μPD66703

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
IRQ_UDL input setup time	t_{SIRQ_UDL}		-1.06		ns
IRQ_UDL input hold time	t_{HIRQ_UDL}		8.94		ns
NFIQ_UDL input setup time	t_{SNFIQ_UDL}		-0.89		ns
NFIQ_UDL input hold time	t_{HNFIQ_UDL}		5.7		ns
DBGREQ input setup time	$t_{SDBGREQ}$		-0.52		ns
DBGREQ input hold time	$t_{HDBGREQ}$		5.44		ns
DBGACK delay from SCLK↑	$t_{DDBGACK}$			17.98	ns

Remark: The min. and max. values are related to SCLK.

Figure 2-23: Interrupt Timing



2.6.8 APB bus timing

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-19: APB Bus Timing Parameters for μPD66702

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
PWRITE_UDL output delay	$t_{DPWRITE}$				10.84	ns
PWDATA_UDL output delay	$t_{DPWDATA}$				10.65	ns
PSELUDL_UDL output delay	$t_{DPSELUDL}$				9.47	ns
PENABLE_UDL output delay	$t_{DPENABLE}$				10.47	ns
PADDR_UDL output delay	t_{DPADDR}				10.18	ns
PRDATA_UDL setup time	$t_{SPRDATA}$		0.07			ns
PRDATA_UDL hold time	$t_{HPRDATA}$		1.85			ns

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-20: APB Bus Timing Parameters for μPD66703

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
PWRITE_UDL output delay	$t_{DPWRITE}$				12.54	ns
PWDATA_UDL output delay	$t_{DPWDATA}$				12.21	ns
PSELUDL_UDL output delay	$t_{DPSELUDL}$				10.56	ns
PENABLE_UDL output delay	$t_{DPENABLE}$				12.55	ns
PADDR_UDL output delay	t_{DPADDR}				11.65	ns
PRDATA_UDL setup time	$t_{SPRDATA}$		-1.26			ns
PRDATA_UDL hold time	$t_{HPRDATA}$		3.28			ns

Figure 2-24: APB Read Cycle

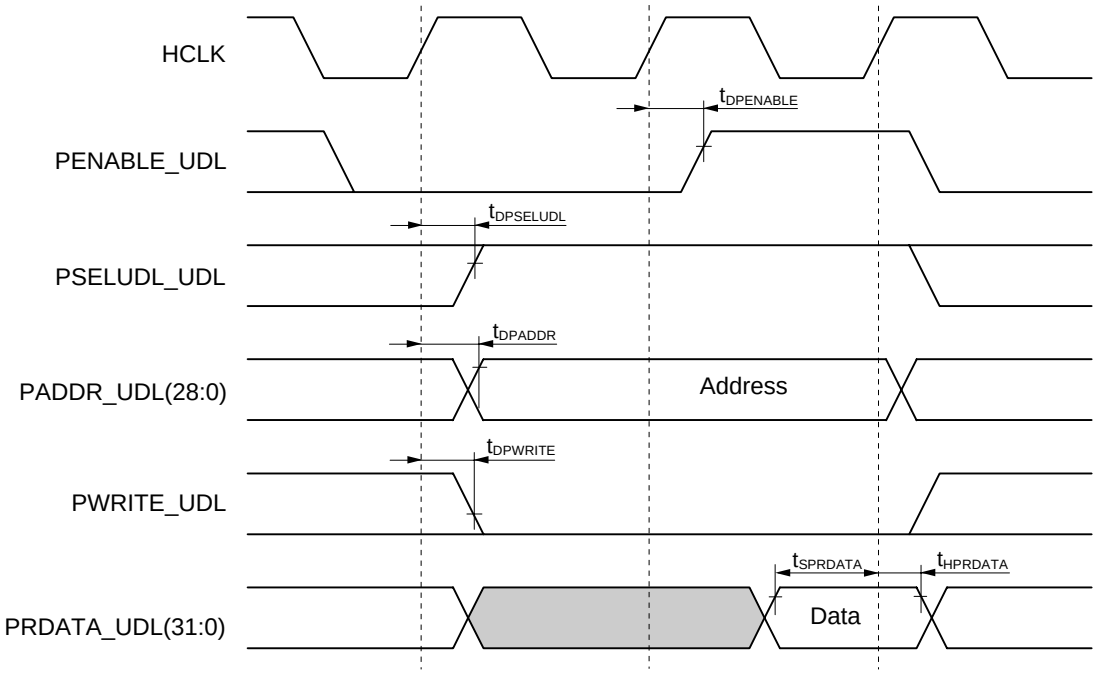
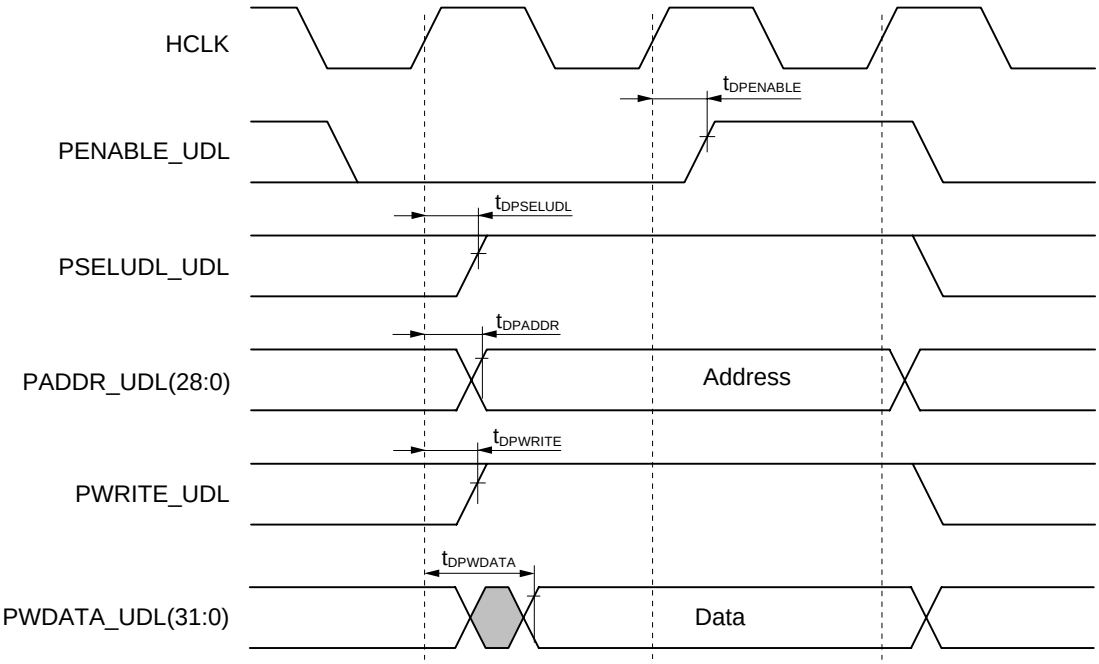


Figure 2-25: APB Write Cycle



2.6.9 AHB Master bus (AHB4) timing

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-21: AHB4 Bus Timing Parameters for μPD66702

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
AHB4_HWRITE output delay	t_{DAHB4_HWRITE}				11.6	ns
AHB4_HWDATA output delay	t_{DAHB4_HWDATA}				10.51	ns
AHB4_HTRANS output delay	t_{DAHB4_HTRANS}				13.75	ns
AHB4_HSIZE output delay	t_{DAHB4_HSIZE}				11.87	ns
AHB4_HPROT output delay	t_{DAHB4_HPROT}				11.38	ns
AHB4_HLOCK output delay	t_{DAHB4_HLOCK}				12.52	ns
AHB4_HBUSREQ output delay	$t_{DAHB4\_HBUSREQ}$				12.03	ns
AHB4_HBURST output delay	t_{DAHB4_HBURST}				12.48	ns
AHB4_HADDR output delay	t_{DAHB4_HADDR}				12.17	ns
AHB4_HRESP setup time	t_{SAHB4_HRESP}		0.59			ns
AHB4_HRESP hold time	t_{HAHB4_HRESP}		7.36			ns
AHB4_HREADY setup time	t_{SAHB4_HREADY}		0.61			ns
AHB4_HREADY hold time	t_{HAHB4_HREADY}		7.31			ns
AHB4_HRDATA setup time	t_{SAHB4_HRDATA}		-2.1			ns
AHB4_HRDATA hold time	t_{HAHB4_HRDATA}		8.05			ns
AHB4_HGRANT setup time	t_{SAHB4_HGRANT}		-1.67			ns
AHB4_HGRANT hold time	t_{HAHB4_HGRANT}		7.43			ns

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-22: AHB4 Bus Timing Parameters for μPD66703

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
AHB4_HWRITE output delay	t_{DAHB4_HWRITE}				12.56	ns
AHB4_HWDATA output delay	t_{DAHB4_HWDATA}				11.75	ns
AHB4_HTRANS output delay	t_{DAHB4_HTRANS}				14.75	ns
AHB4_HSIZE output delay	t_{DAHB4_HSIZE}				12.8	ns
AHB4_HPROT output delay	t_{DAHB4_HPROT}				12.61	ns
AHB4_HLOCK output delay	t_{DAHB4_HLOCK}				13.65	ns
AHB4_HBUSREQ output delay	$t_{DAHB4\_HBUSREQ}$				12.26	ns
AHB4_HBURST output delay	t_{DAHB4_HBURST}				13.26	ns
AHB4_HADDR output delay	t_{DAHB4_HADDR}				12.7	ns
AHB4_HRESP setup time	t_{SAHB4_HRESP}		-0.61			ns
AHB4_HRESP hold time	t_{HAHB4_HRESP}		8.35			ns
AHB4_HREADY setup time	t_{SAHB4_HREADY}		-0.44			ns
AHB4_HREADY hold time	t_{HAHB4_HREADY}		8.45			ns
AHB4_HRDATA setup time	t_{SAHB4_HRDATA}		-2.67			ns
AHB4_HRDATA hold time	t_{HAHB4_HRDATA}		8.96			ns
AHB4_HGRANT setup time	t_{SAHB4_HGRANT}		-2.29			ns
AHB4_HGRANT hold time	t_{HAHB4_HGRANT}		8.74			ns

Figure 2-26: AHB4 Bus Timing Parameters (Read and Write Burst Cycle Example)

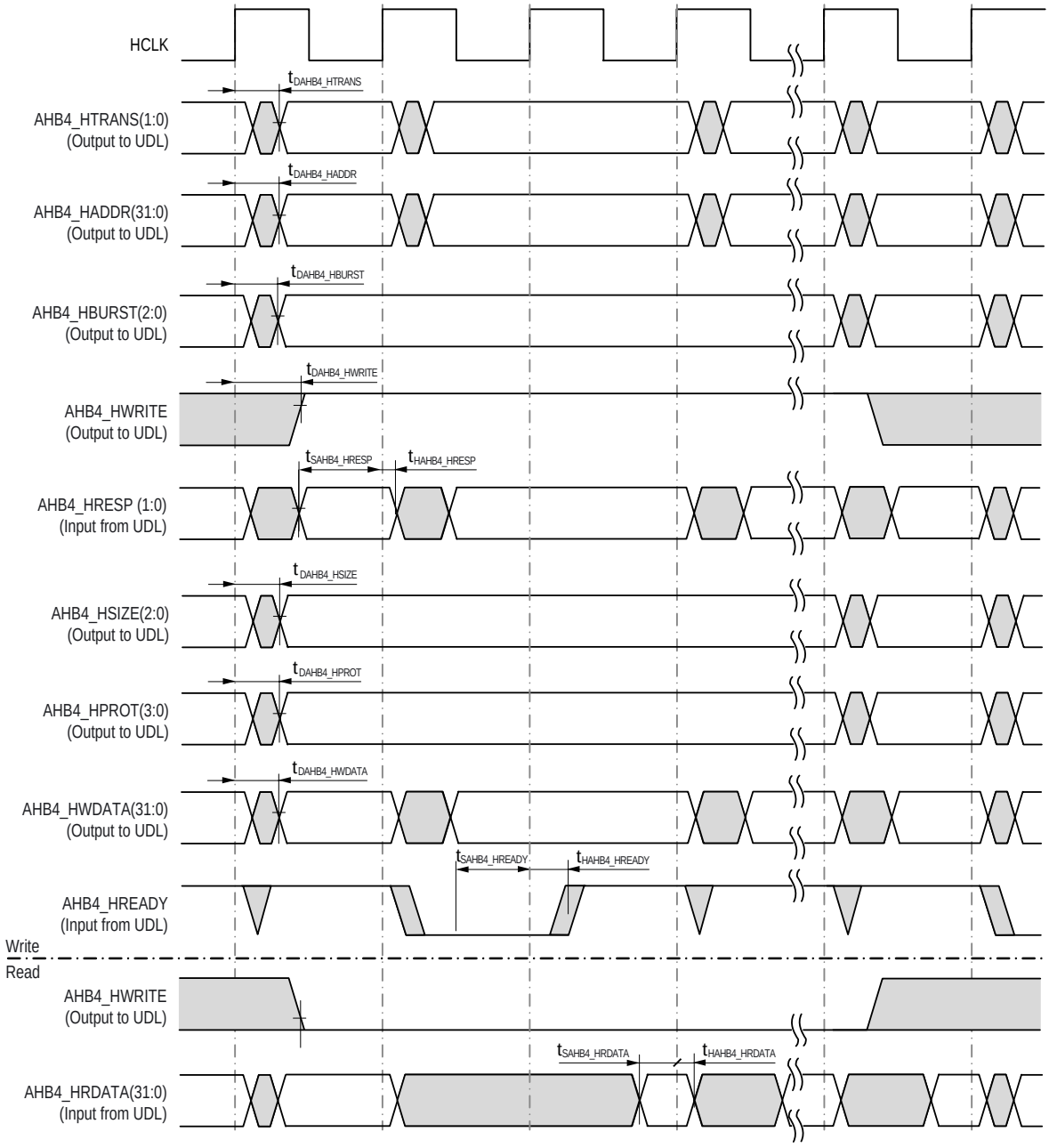
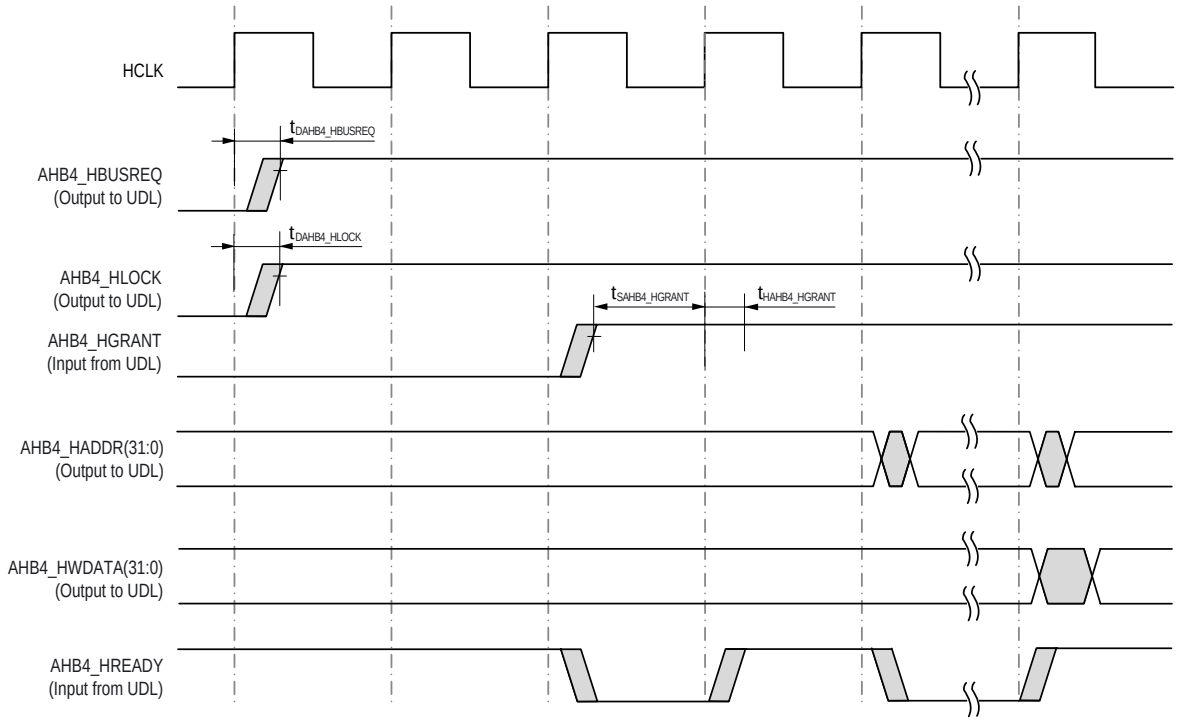


Figure 2-27: AHB4 Bus Timing Parameters (Bus Master Handover Example)



2.6.10 AHB Slave bus (AHB3) timing

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-23: AHB3 Bus Timing Parameters for μPD66702

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
AHB3_HRESP output delay	t_{DAHB3_HRESP}				11.91	ns
AHB3_HREADYOUT output delay	$t_{DAHB3\_HREADYOUT}$				15.03	ns
AHB3_HRDATA output delay	t_{DAHB3_HRDATA}				15.03	ns
AHB3_HMPMCG setup time	t_{SAHB3_HMPMCG}		-0.46			ns
AHB3_HMPMCG hold time	t_{HAHB3_HMPMCG}		5.51			ns
AHB3_HMPMCCS setup time	$t_{SAHB3\_HMPMCCS}$		-0.46			ns
AHB3_HMPMCCS hold time	$t_{HAHB3\_HMPMCCS}$		5.51			ns
AHB3_HWRITE setup time	t_{SAHB3_HWRITE}		-1.25			ns
AHB3_HWRITE hold time	t_{HAHB3_HWRITE}		5.4			ns
AHB3_HWDATA setup time	t_{SAHB3_HWDATA}		-1.55			ns
AHB3_HWDATA hold time	t_{HAHB3_HWDATA}		5.73			ns
AHB3_HTRANS setup time	t_{SAHB3_HTRANS}		-0.73			ns
AHB3_HTRANS hold time	t_{HAHB3_HTRANS}		5.8			ns
AHB3_HSIZE setup time	t_{SAHB3_HSIZE}		-1.4			ns
AHB3_HSIZE hold time	t_{HAHB3_HSIZE}		5.68			ns
AHB3_HREADYIN setup time	$t_{SAHB3\_HREADYIN}$		-0.44			ns
AHB3_HREADYIN hold time	$t_{HAHB3\_HREADYIN}$		4.17			ns
AHB3_HMASTLOCK setup time	$t_{SAHB3\_HMASTLOCK}$		-1.62			ns
AHB3_HMASTLOCK hold time	$t_{HAHB3\_HMASTLOCK}$		5.44			ns
AHB3_HBURST setup time	t_{SAHB3_HBURST}		-1.02			ns
AHB3_HBURST hold time	t_{HAHB3_HBURST}		5.59			ns
AHB3_HADDR setup time	t_{SAHB3_HADDR}		-0.79			ns
AHB3_HADDR hold time	t_{HAHB3_HADDR}		5.67			ns

(T_A = -40 to +85°C, V_{DD1} = 2.3 V ~ 2.7 V, V_{DD2} = 3.0 V ~ 3.6 V)

Table 2-24: AHB3 Bus Timing Parameters for μPD66703

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
AHB3_HRESP output delay	t_{DAHB3_HRESP}				13.3	ns
AHB3_HREADYOUT output delay	$t_{DAHB3\_HREADYOUT}$				15.58	ns
AHB3_HRDATA output delay	t_{DAHB3_HRDATA}				17.11	ns
AHB3_HMPMCG setup time	t_{SAHB3_HMPMCG}		-0.69			ns
AHB3_HMPMCG hold time	t_{HAHB3_HMPMCG}		5.89			ns
AHB3_HMPMCCS setup time	$t_{SAHB3\_HMPMCCS}$		-0.69			ns
AHB3_HMPMCCS hold time	$t_{HAHB3\_HMPMCCS}$		5.89			ns
AHB3_HWRITE setup time	t_{SAHB3_HWRITE}		-1.97			ns
AHB3_HWRITE hold time	t_{HAHB3_HWRITE}		6.66			ns
AHB3_HWDATA setup time	t_{SAHB3_HWDATA}		-1.8			ns
AHB3_HWDATA hold time	t_{HAHB3_HWDATA}		6.62			ns
AHB3_HTRANS setup time	t_{SAHB3_HTRANS}		-1.33			ns
AHB3_HTRANS hold time	t_{HAHB3_HTRANS}		6.6			ns
AHB3_HSIZE setup time	t_{SAHB3_HSIZE}		-2.03			ns
AHB3_HSIZE hold time	t_{HAHB3_HSIZE}		6.72			ns
AHB3_HREADYIN setup time	$t_{SAHB3\_HREADYIN}$		-1.02			ns
AHB3_HREADYIN hold time	$t_{HAHB3\_HREADYIN}$		4.73			ns
AHB3_HMASTLOCK setup time	$t_{SAHB3\_HMASTLOCK}$		-2.15			ns
AHB3_HMASTLOCK hold time	$t_{HAHB3\_HMASTLOCK}$		6.34			ns
AHB3_HBURST setup time	t_{SAHB3_HBURST}		-1.64			ns
AHB3_HBURST hold time	t_{HAHB3_HBURST}		6.5			ns
AHB3_HADDR setup time	t_{SAHB3_HADDR}		1.46			ns
AHB3_HADDR hold time	t_{HAHB3_HADDR}		6.63			ns

Figure 2-28: AHB3 Bus Timing Parameters (32-bit Read/Write Example)

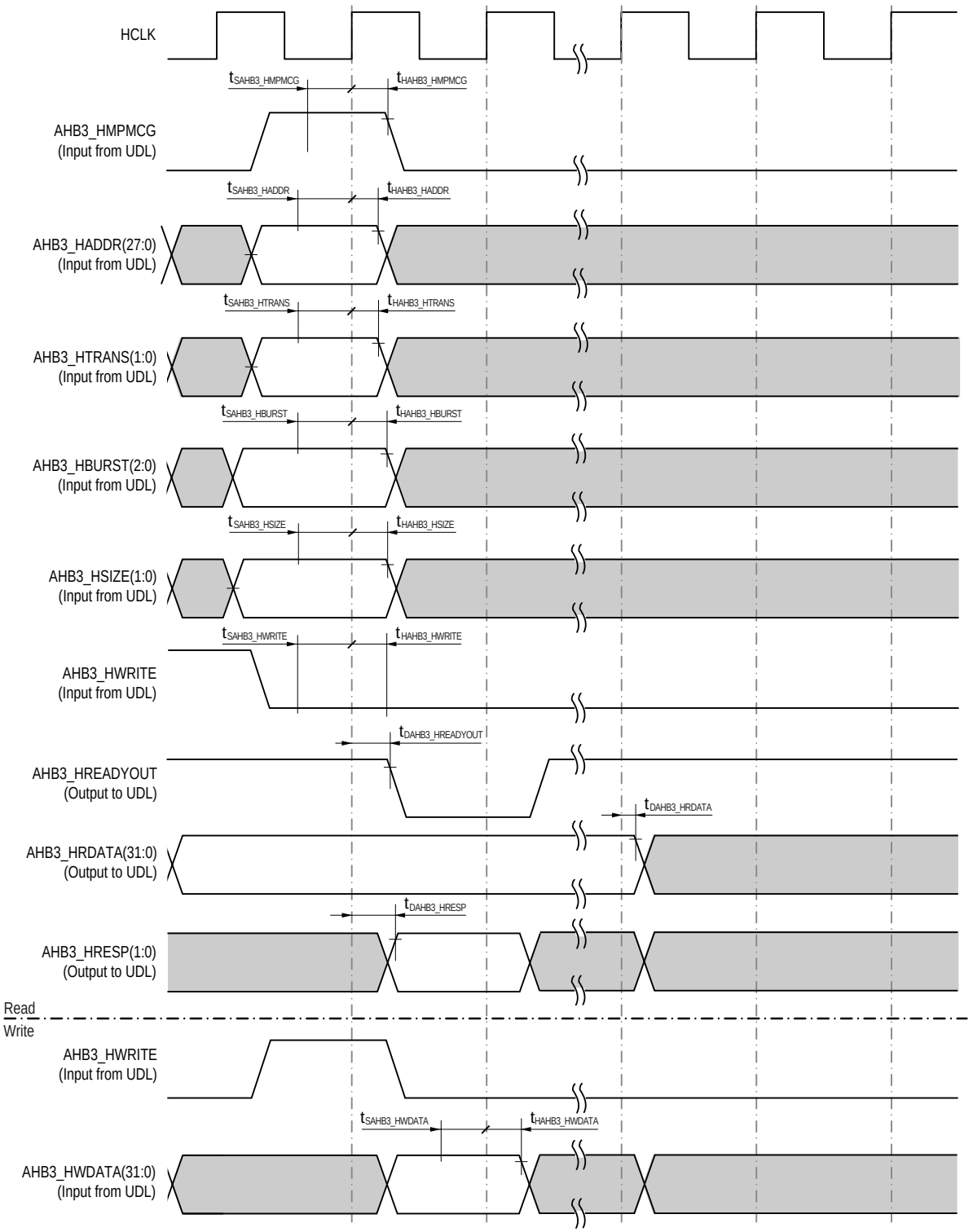


Figure 2-29: AHB3 Bus Timing Parameters (HREADY Signal Handshake Example)

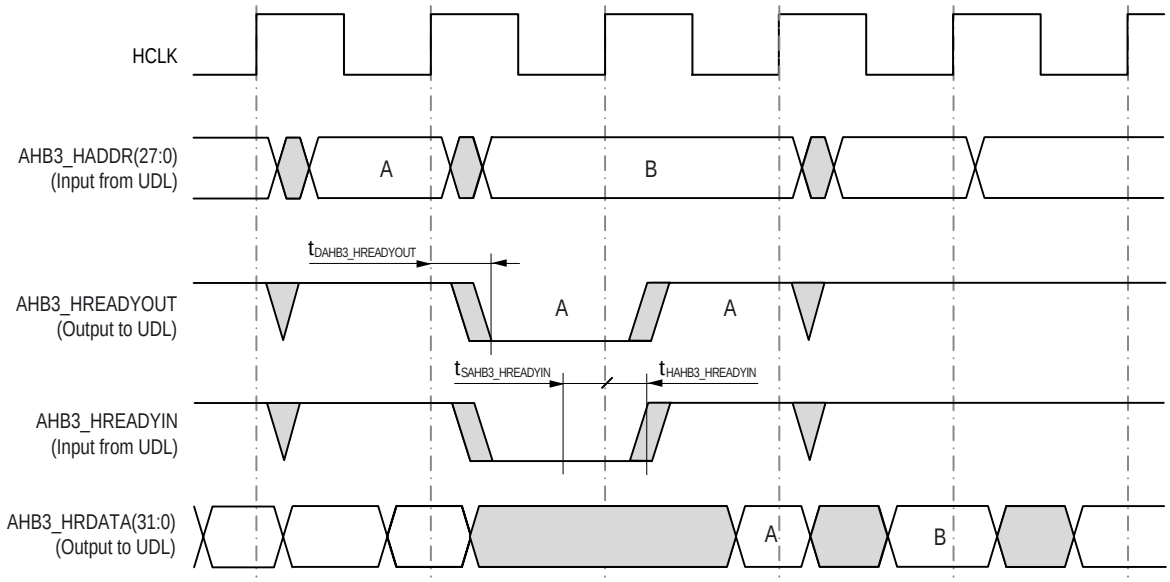
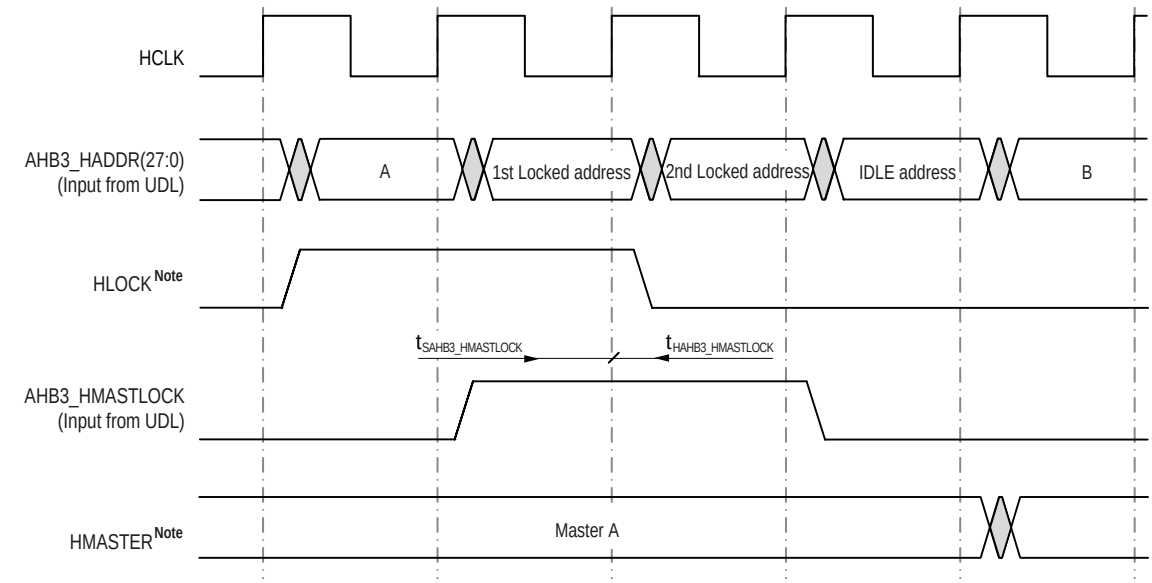


Figure 2-30: AHB3 Bus Timing Parameters (Locked Bus Cycle Example)



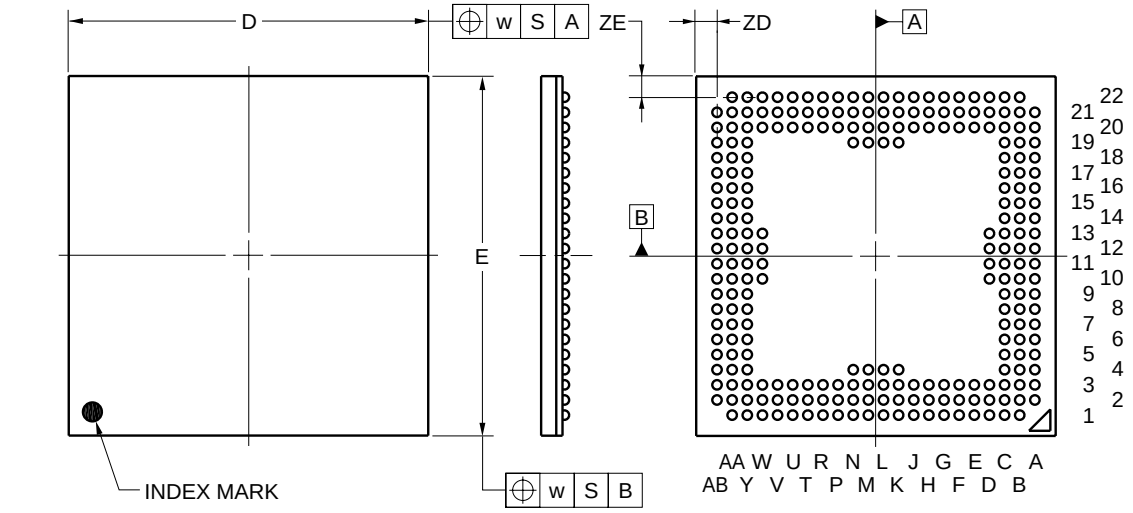
Note: HLOCK and HMASTER are UDL-internal signals, that are controlled by the actual AHB arbiter in the UDL.

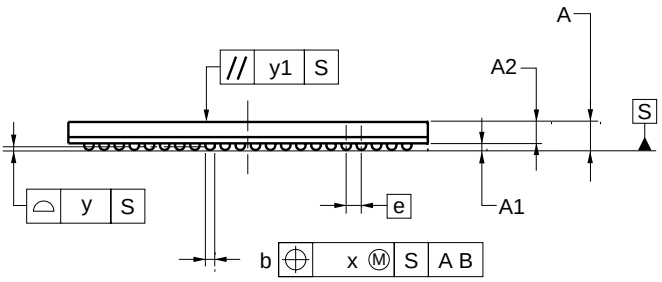
3. Package Drawing

3.1 Package Drawing for μPD66702

Figure 3-1: Package Drawing for μPD66702

240-PIN PLASTIC FBGA (19x19)





(UNIT:mm)

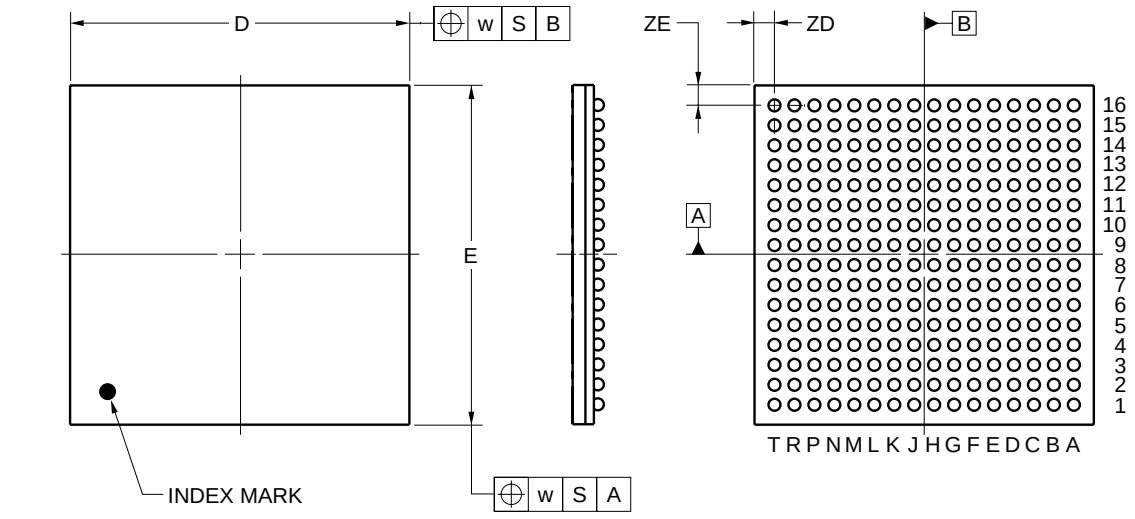
ITEM	DIMENSIONS
D	19.00 0.10
E	19.00 0.10
w	0.20
e	0.80
A	1.48 0.10
A1	0.35 0.06
A2	1.13
b	0.50 $^{0.05}_{0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.10
ZE	1.10

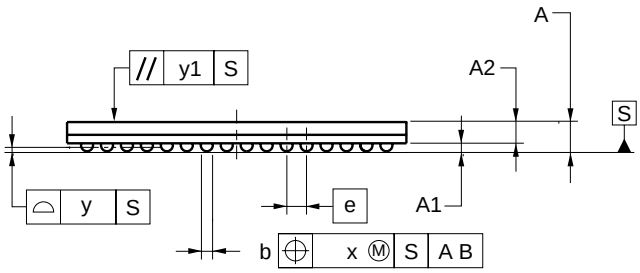
P240F1-80-HN3

3.2 Package Drawing for μPD66703

Figure 3-2: Package Drawing for μPD66703

256-PIN PLASTIC BGA (17x17)





(UNIT:mm)

ITEM	DIMENSIONS
D	17.00 0.20
E	17.00 0.20
w	0.30
e	1.00
A	1.83 0.20
A1	0.50 0.10
A2	1.33
b	0.60 0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P256F1-100-GN4

4. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended please consult NEC.

Table 4-1: Soldering Conditions for μPD66702 and μPD66703

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235°C, Time of temperature higher than 210°C: 30 seconds max. Number of reflows: 3 max. Number of storage days after opening of dry pack: 3 **Note**	IR35-107-3

After that, prebaking is necessary at 125°C for 10 hours.
The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

5. Revision History

Page	Chapter	Description
p.33	Chapter 2.7	Table 2-7: DC Characteristics Supply current values had been changed

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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