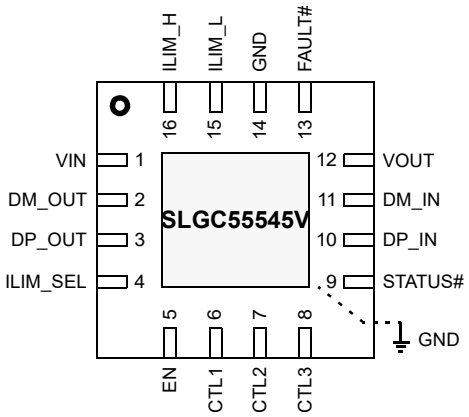
General Description

Renesas SLGC55545V is a combination of current-limited USB port power switch with a USB 2.0 high-speed data line (D+/D-) switch and USB charging port identification circuit. Applications include notebook PCs and other intelligent USB host devices. The wide bandwidth (2.6 GHz) data-line switch also features low capacitance and low on resistance, allowing signals to pass with minimum edge and phase distortion. The SLGC55545V monitors D+ and D-, providing the correct hand-shaking protocol with compliant client devices.

Features

- Meets Battery Charging Specification BC1.2 for DCP and CDP
- Meets Chinese Telecommunications Industry Standard YD/T 1591-2009
- Supports Non-BC 1.2 charging modes via Automatic selection
  - DM/DP Divider Modes 2.7 V/2.0 V (1 A) & 2.0 V/2.7 V (2 A)
  - DM/DP 1.2 V Mode
- Compatible with USB 2.0/3.0 power switch requirements
- 73 mΩ (typ) high side MOSFET
- Adjustable Current Limit up to 3.0 A (typ)
- Pb-Free / RoHS Compliant
- Halogen-Free
- TQFN-16 Package
  - UL Listed and CB File No. E468659

Pin Configuration



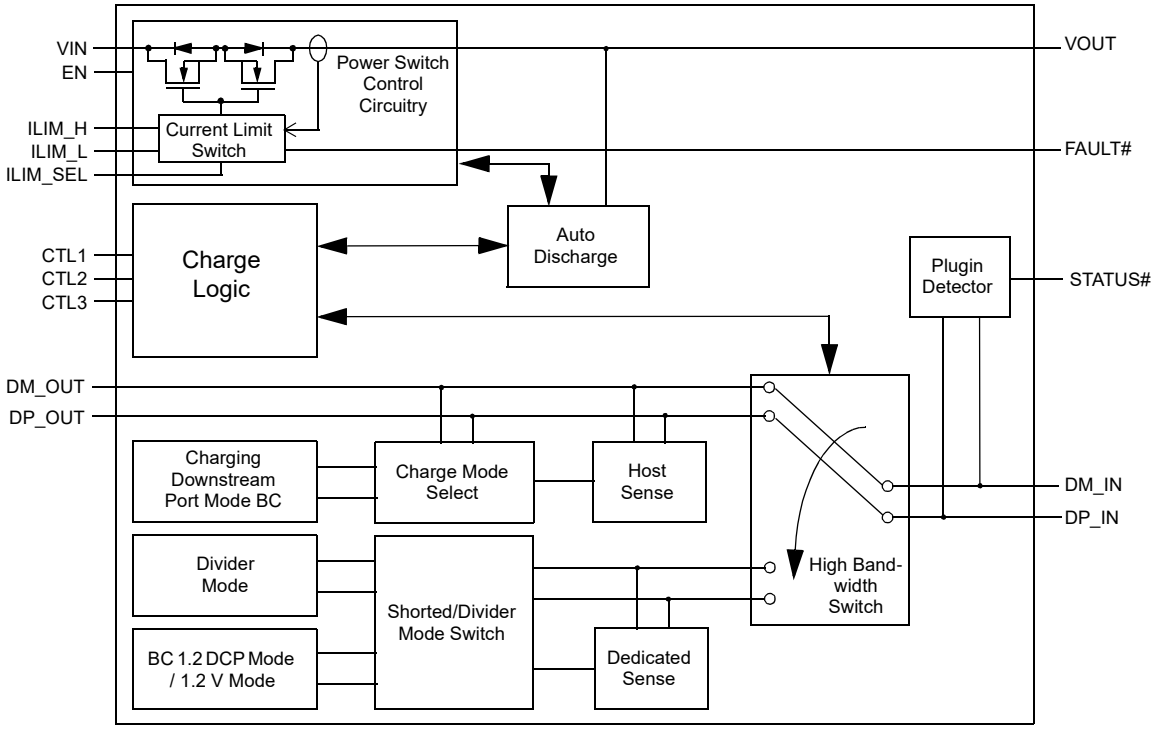
16-pin TQFN

(Top View)

Applications

- USB Ports/Hubs
- Notebook PCs
- Universal Wall Charging Adapter

Block Diagram



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Pin Description

Pin #	Pin Name	Type	Pin Description
1	VIN	PWR	Input voltage, connect a 0.1µF or greater ceramic capacitor from IN to GND as close to the device as possible
2	DM_OUT	Input/Output	D- data line to USB host controller
3	DP_OUT	Input/Output	D+ data line to USB host controller
4	ILIM_SEL	Input	Logic level input signal used to dynamically change power switch current-limit threshold; logic LOW selects ILIM_L, logic HIGH selects ILIM_H
5	EN	Input	Logic level control input for turning the power switch and the signal switches on/off. When EN is LOW, the device is disabled, the signal and power switches are OFF.
6	CTL1	Input	Logic level control inputs for controlling the charging mode and the signal switches. The “000” configuration is used to force and discharge of the output (VOUT) capacitor.
7	CTL2	Input	
8	CTL3	Input	
9	STATUS#	Output	Active Low open drain output, asserted while charge limit occur by Power Wake or Port Power Management functions.
10	DP_IN	Input/Output	D+ data line to connector, input/output used for hand-shaking with portable equipment
11	DM_IN	Input/Output	D- data line to connector, input/output used for hand-shaking with portable equipment
12	VOUT	PWR	Power switch output
13	FAULT#	Output	Active low open drain output, asserted during over-temperature or current-limit conditions
14	GND	GND	Ground
15	ILIM_L	Input	External resistor used to set current-limit threshold when ILIM_SEL is LOW. See current limit setting in detailed description.
16	ILIM_H	Input	External resistor used to set current-limit threshold when ILIM_SEL is HIGH. See current limit setting in detailed description.
--	Thermal Pad	GND	Ground

Ordering Information

Part Number	Type	Production Flow
SLGC55545V	TQFN-16	Industrial, -40 °C to 85 °C
SLGC55545VTR	TQFN-16 - Tape and Reel	Industrial, -40 °C to 85 °C

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Absolute Maximum Ratings

Parameter	Description	Min.	Max.	Unit
Supply Voltage range	VIN	-0.3	7	V
Input Voltage range	EN, ILIM_L, ILIM_H, ILIM_SEL, CTL1, CTL2, CTL3	-0.3	7	V
Output Voltage range	VOUT, FAULT#, STATUS# [2]	-0.3	7	V
Output Voltage range	VIN to VOUT	-7	7	V
Voltage range	DP_IN, DM_IN, DP_OUT, DM_OUT	-0.3	VIN+0.3 or 5.7	V
Input Clamp current	DP_IN, DM_IN, DP_OUT, DM_OUT	--	±20	mA
Continuous current in SDP or CDP mode	DP_IN to DP_OUT or DM_IN to DM_OUT	--	±100	mA
Continuous current in BC1.2 DCP mode	DP_IN to DM_IN	--	±35	mA
Continuous output current		Internally limited		
Continuous output sink current	FAULT#, STATUS#	--	25	mA
Continuous output source current	ILIM_L, ILIM_H	--	1	mA
Continuous total power dissipation		Internally limited		
ESD Rating, Human Body Model (HBM)	VIN, EN, ILIM_L, ILIM_H, ILIM_SEL, CTL1, CTL2, CTL3, VOUT, FAULT#	2	--	kV
ESD Rating, Human Body Model (HBM)	DP_IN, DM_IN, DP_OUT, DM_OUT	8	--	kV
ESD Rating, Charged Device Model		500	--	V
Operating Temperature Range		-40	85	°C
Storage Temperature Range		-65	165	°C

Note:
1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Do not apply external voltage sources directly

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Thermal Information [1]

Parameter		Typ.	Unit
θ_{JA}	Junction-to-ambient thermal resistance [2]	53.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance [3]	51.4	°C/W
θ_{JB}	Junction-to-board thermal resistance [4]	17.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter [5]	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter [6]	20.7	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance [7]	3.9	°C/W

Note:
1. For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
2. The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
3. The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
4. The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
5. The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
6. The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
7. The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Electrical Characteristics

Conditions are -40 ≤ T_J ≤ 125 °C unless otherwise noted. V_{EN} = V_{IN} = 5 V, $R_{FAULT\#}$ = $R_{STATUS\#}$ = 10 kΩ, R_{ILIM_L} = 80 kΩ, R_{ILIM_H} = 20 kΩ, ILIM_SEL = V_{IN}, CTL1 = CTL2 = CTL3 = V_{IN}, unless otherwise noted. Positive currents are into pins. Typical values are at 25 °C. All voltages are with respect to GND unless otherwise noted.

Electrical Characteristics - Power Switch

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
RDS_{ON}	Static drain-source ON-state VOUT	I_{OUT} = 2 A, V_{ILIM_SEL} = Logic High	--	73	--	mΩ
		I_{OUT} = 100 mA, V_{ILIM_SEL} = Logic Low	--	73	--	mΩ
		-40 °C ≤ T_A = T_J ≤ 85 °C, I_{OUT} = 2 A, V_{ILIM_SEL} = Logic High	--	73	--	mΩ
		T_A = T_J = 25 °C, I_{OUT} = 2 A, V_{ILIM_SEL} = Logic HIgh	--	7	--	mΩ
T_R	Rise Time, Output	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω	0.7	1.50	1.6	ms
T_F	Fall Time, Output	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω	0.2	0.35	0.5	ms
R_{DIS}	VOUT Discharge Resistance		337	498	681	Ω
T_{DIS}	Out Discharge Hold Time		--	2	--	s
I_{REV}	Reverse Leakage Current	V_{OUT} = 5.5 V, V_{IN} = V_{EN} = 0 V, T_J = 25 °C	--	--	2	µA

Electrical Characteristics - Input EN

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{EN}	Enable pin Turn on/off Threshold, falling		--	1.08	--	V

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Electrical Characteristics - Input EN

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{EN_HYS}	EN Hysteresis		--	230[1]	--	mV
	Input Current	V_{EN} = 0 V or 5.5 V	-0.5	--	0.5	µA
T_{ON}	Turn On Time	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω	--	2.7	4.0	ms
T_{OFF}	Turn Off Time	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω	--	1.7	3.0	ms
Note: 1. Typical value for reference only, not 100% tested.						

Electrical Characteristics - Current Limit

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{ILIM_SEL}	ILIM_SEL turn on/off threshold, falling		--	1.08	--	V
V_{ILIM_HYS}	ILIM_SEL Hysteresis		--	230[1]	--	mV
I_{EN}	ILIM_SEL Input Current	V_{ILIM_HYS} = 0 V or 5.5 V	-0.5	--	0.5	µA
I_{SHORT}	Maximum DC Output Current from VIN to VOUT	V_{ILIM_SEL} = Logic Low R_{ILIM_L} = 210 kΩ	0.22	0.26	0.30	A
		V_{ILIM_SEL} = Logic Low R_{ILIM_L} = 80.6 kΩ, -40 °C ≤ T_J ≤ 85 °C	0.60	0.66	0.72	A
		V_{ILIM_SEL} = Logic Low R_{ILIM_L} = 22.1 kΩ	2.120	2.275	2.430	A
		V_{ILIM_SEL} = Logic High R_{ILIM_H} = 20 kΩ	2.340	2.510	2.685	A
		V_{ILIM_SEL} = Logic High R_{ILIM_H}= 16.9 kΩ	2.77	2.97	3.17	A
T_{IOS}	Response Time to Short Circuit	V_{IN} = 5 V	--	6.65[1]	--	µs
Note: 1. Typical value for reference only, not 100% tested.						

Electrical Characteristics - Supply Current

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{CCL}	Supply Current, switch disabled	V_{EN} = 0 V, VOUT grounded, -40 °C ≤ T_J ≤ 85 °C	--	0.1	2	µA
I_{CCH}	Supply Current, operating	V_{EN} = V_{IN}	--	215	270	µA

Electrical Characteristics - Undervoltage Lockout

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{UVLO}	Low level input voltage, IN	V_{IN} rising	3.9	4.1	4.3	V
V_{IN_HYS}	Hysteresis, IN			100[1]		mV
Note: 1. Typical value for reference only, not 100% tested.						

Electrical Characteristics - FAULT#

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	Output Low voltage, FAULT#	$I_{FAULT\#}$ = 1 mA	--	--	100	mV
I_{LEAK}	Off-state Leakage	$V_{FAULT\#}$ = 5.5 V	--	--	1	µA

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Electrical Characteristics - FAULT#

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
	FAULT# Deglitch	FAULT# assertion or de-assertion due to over-current condition	--	8.6	--	ms

Electrical Characteristics - CTL Inputs

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{CTL}	CTL pins turn on/off threshold, falling		--	1.08	--	V
V_{CTL_HYS}	Hysteresis, CTL		--	230[1]	--	mV
	Input Current	V_{CTL}= 0 V or 5.5 V	-0.5	--	0.5	µA
Note: 1. Typical value for reference only, not 100% tested.						

Electrical Characteristics - Thermal Shutdown

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
	Thermal shutdown threshold		155	--	--	°C
	Thermal shutdown threshold in current-limit		135	--	--	°C
	Hysteresis			20[1]		°C
Note: 1. Typical value for reference only, not 100% tested.						

Electrical Characteristics - Analog Switch

V_{IN} = 5.0 V, T_A = 25 °C (unless specified otherwise)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DP_IN}, V_{DM_IN}	Analog signal Range		0	--	V_{DD}	V
R_{ON}	On Resistance DP_OUT/DM_OUT Switch	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = 30 mA	--	2	4	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = -15 mA	--	3	6	Ω
ΔR_{ON}	On Resistance Mismatch between channels DP_OUT/DM_OUT Switch	V_{IN} = 5 V V_{DP_IN} = V_{DM_IN}= 400 mV I_{DP_IN} = I_{DM_IN} = 10 mA	--	0.1	--	Ω
R_{FLAT}	On Resistance flatness DP_OUT/DM_OUT Switch	V_{IN} = 5.0 V V_{DP_IN} = V_{DM_IN} = 0 V to V_{IN} I_{DP_IN} = I_{DM_IN} = 10 mA	--	0.5	--	Ω
R_{SHORT}	On Resistance of DP_OUT/DM_OUT Short	V_{CB} = 0 V V_{DP_IN} = 1 V I_{DP_IN} = I_{DM_IN}= 10 mA	--	100	150	Ω
$I_{DP\_OUT\_OFF}$, I_{DM_OUTOFF}	Off-Leakage Current	V_{IN} = 3.6 V V_{DP_IN} = V_{DM_IN} = 0.3 V to 3.3 V V_{DP_OUT} = V_{DM_OUT} = 3.3 V to 0.3 V, V_{EN} = 0 V	-250	--	250	nA
$I_{DP\_IN\_OFF}$, $I_{DM\_IN\_OFF}$	Off-Leakage Current	V_{IN} = 3.6 V V_{DP_IN} = V_{DM_IN} = 3.3 V to 0.3 V V_{EN} = V_{IN}	-250	--	250	nA

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Electrical Characteristics - Dynamic Performance

V_{DD} = 5.0 V, T_A = 25 °C (unless specified otherwise)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
T_{ON}	Turn On Time	V_{DP_OUT} or V_{DM_OUT} = 1.5 V R_{LOAD} = 300 Ω C_{LOAD} = 35 pF	--‘	20	100	µs
T_{OFF}	Turn Off Time	V_{DP_OUT} or V_{DM_OUT} = 1.5 V R_{LOAD} = 300 Ω C_{LOAD} = 35 pF	--‘	1	5	µs
T_{PLH}, T_{PHL}	DP_OUT/DM_OUT Switch Propagation Delay	R_{LOAD} = R_S = 50 Ω	--	60	--	µs
T_{SKEW}	Output Skew	Skew between DP_IN and DM_IN when connected to DP_OUT and DM_OUT R_{LOAD} = R_S = 50 Ω	--	40	--	ps
C_{OFF}	DP_OUT/DM_OUT Off-Capacitance	f = 1 MHz	--‘	2.0	--	pF
C_{ON}	DP_IN/DM_IN On-Capacitance	f = 240 MHz	--‘	4.0	5.5	pF
BW	-3dB Bandwidth	R_{LOAD} = R_S = 50 Ω	--	1000	--	MHz
V_{ISO}	Off-Isolation	V_{DP_OUT}, V_{DP_IN} = 0 dBm R_{LOAD} = R_S =50 Ω f = 250 MHz	--	-20	--	dB
V_{CT}	Crosstalk	V_{DP_OUT}, V_{DP_IN} = 0 dBm R_{LOAD} = R_S = 50 Ω f = 250 MHz	--	-25	--	dB

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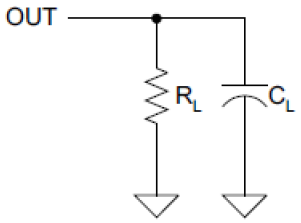
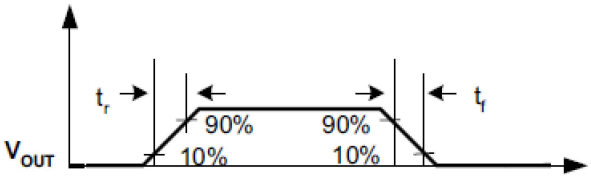
Parameter Measurement Information

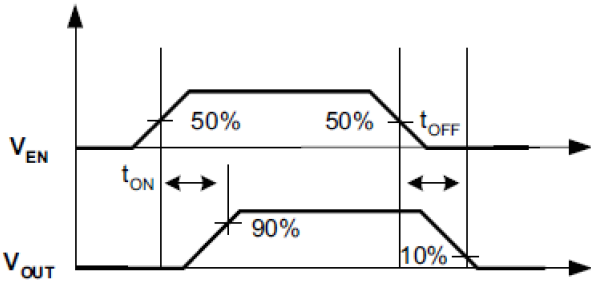
Test Circuit



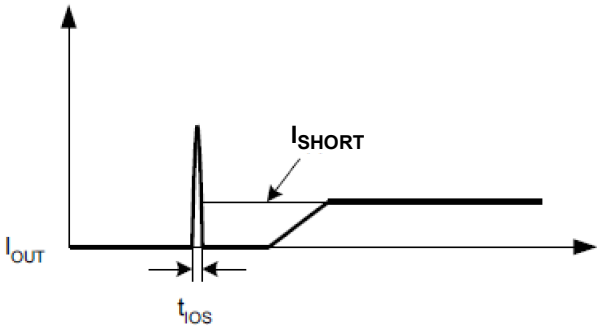
Voltage Waveform



Voltage Waveforms



Response Time to Short-Circuit Waveforms



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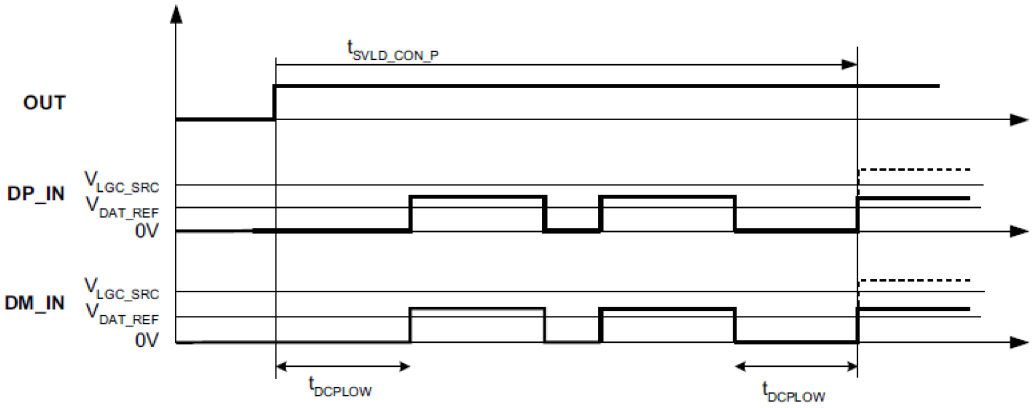
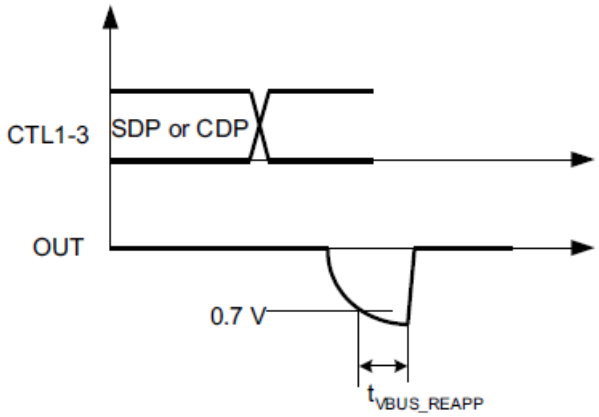
DCP BC1.2 Operation



VOUT Discharge During CTL Lines Change



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Overview

The following overview references various industry standards. It is always recommended to consult the most up-to-date standard to ensure the most recent and accurate information. Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are a convenient location for charging because of an available 5 V power source. Universally accepted standards are required to make sure host and client-side devices operate together in a system to ensure power management requirements are met. Traditionally, USB host ports following the USB 2.0 specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate its power allotment from the host to ensure the total current draw does not exceed 500 mA. In general, each USB device is granted 100 mA and may request more current in 100 mA unit steps up to 500 mA. The host may grant or deny based on the available current.

Additionally, the success of USB has made the mini-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector. One common difficulty has resulted from this. As USB charging has gained popularity, the 500 mA minimum defined by USB 2.0 has become insufficient for many handset and personal media players which need a higher charging rate. On the other hand, wall adapters can provide much more current than 500 mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500 mA minimum defined by USB 2.0 while still using a single micro-USB input connector.

The SLGC55545V supports three of the most common protocols:

- USB 2.0 Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider Mode

All three methods have similarities and differences, but the biggest commonality is that all three define three types of charging ports that provide charging current to client-side devices. These charging ports are defined as:

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

BC1.2 defines a Charging Port as a downstream facing USB port that provides power for charging portable equipment. The table below shows the differences between these ports according to BC1.2 (draft).

Operating Modes

Port Type	Supports USB 2.0 Communication	Maximum Allowable Current Draw By Portable Equipment (A)
SDP (USB 2.0)	Yes	0.5
SDP (USB 3.0)	Yes	0.9
CDP	Yes	1.5
DCP	No	1.5

BC1.2 (draft) defines the protocol necessary to allow portable equipment to determine what type of port it is connected to so that it can allot its maximum allowable current draw. The hand-shaking process has two steps. During step one, the primary detection, the portable equipment outputs a nominal 0.6-V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3 V and less than 0.8 V. The second step, the secondary detection, is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V and less than 0.8 V.

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Standard Downstream Port (SDP)

An SDP is a traditional USB port that follows USB 2.0/3.0 and supplies a maximum of 500 mA per port for USB 2.0 and 900 mA per port for USB 3.0. USB 2.0 communications is supported, and the host controller must be active to allow charging.

Charging Downstream Port (CDP)

A CDP is a USB port that follows USB 2.0/3.0 BC1.2 (draft) and supplies a minimum of 1.5 A per port. It provides power and meets USB 2.0/3.0 requirements for device enumeration. USB 2.0/3.0 communications is supported, and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 (draft) client device and allows for additional current draw by the client device.

The CDP hand-shaking process is two steps. During step one the portable equipment outputs a nominal 0.6 V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

The second step is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V and less than 0.8 V.

Dedicated Charging Port (DCP)

A DCP is a special type of wall-adapter used in charging applications that uses a micro-B connector to connect to portable devices. A DCP only provides power and does not support data connection to an upstream port. As shown in following sections, a DCP is identified by the electrical characteristics of its data lines. The SLGC55545V emulates DCP in two charging states, namely DCP Forced and DCP Auto. In DCP Forced state the device will support one of the following two DCP charging schemes: Divider1 or Shorted. In DCP Auto state, the SLGC55545V charge detection state machine is enabled which will selectively implement charging schemes involved with the Shorted, Divider1, Divider2, and 1.2 V modes.

Shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009,

Divider and 1.2V modes are used to charge devices that do not comply with BC1.2 DCP standard.

High-Bandwidth Data Line Switch

The SLGC55545V passes the D+ and D- data lines through the device to enable monitoring and handshaking while supporting charging operation. A wide bandwidth signal switch is used, allowing data to pass through the device without corrupting signal integrity. The data line switches are turned on in any of CDP or SDP operating modes. The EN input also needs to be at logic High for the data line switches to be enabled.

Note:
1. While in CDP mode, the data switches are ON even while CDP handshaking is occurring.
2. The data line switches are OFF if EN is low, or if in DCP mode (BC1.2 (draft), Divider mode or Auto-detect). They are not automatically turned off if the power switch (VIN to VOUT) is doing current limiting. With SLGC55545V, the data line switches are also off when in “000” mode.
3. The data switches are for USB 2.0 differential pair only. In the case of a USB 3.0 host, the super speed differential pairs must be routed directly to the USB connector without passing through the SLGC55545V.

Logic Control Modes

The SLGC55545V supports the listed standards above for the SDP, CDP and DCP modes using the CTL1, CTL2, and CTL3 logic I/O control pins, although their truth tables are different as shown below. The different CTLx settings correspond to the different types of charge modes. Also, using the Auto-Detect Mode, the Divider Mode or BC1.2 (draft) / YD/T 1591-2009 can be automatically selected without external user interaction

Note:

With the SLGC55545V, if the “000” mode is selected, the power switch will be turned off and an output discharge resistor will be connected, while the data line switches will be turned off.

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SLGC55545V Control Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Settings	Status Output	Note
0	0	0	0	Discharge	N/A	OFF	Output held LOW
0	0	0	1	Discharge	N/A	OFF	Output held LOW
0	0	1	0	DCP Auto	ILIM_H	OFF	Data Lines Disconnected
0	0	1	1	DCP Auto	I_{OS_PW} & ILIM_H[1]	DCP Load Present[2]	Data Lines Disconnected & Power Wake Function Active
0	1	0	0	SDP1	ILIM_L	OFF	Data Lines Connected
0	1	0	1	SDP1	ILIM_H	OFF	Data Lines Connected
0	1	1	0	DCP Auto	ILIM_H	OFF	Data Lines Disconnected
0	1	1	1	DCP Auto	ILIM_H	DCP Load Present[3]	Data Lines Disconnected & Port Power Management Function Active
1	0	0	0	DCP Shorted	ILIM_L	OFF	Device forced to stay in DCP BC 1.2 charging mode
1	0	0	1	DCP Shorted	ILIM_H	OFF	Device forced to stay in DCP BC 1.2 charging mode
1	0	1	0	DCP / Divider1	ILIM_L	OFF	Device forced to stay in DCP Divider1 charging mode
1	0	1	1	DCP / Divider1	ILIM_H	OFF	Device forced to stay in DCP Divider1 charging mode
1	1	0	0	SDP1	ILIM_L	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_H	OFF	Data Lines Connected
1	1	1	0	SDP2[4]	ILIM_L	OFF	Data Lines Connected
1	1	1	1	CDP[4]	ILIM_H	CDP Load Present[5]	Data Lines Connected & Port Power Management Active

Notes:

1. Current Limit (I_{OS}) is automatically switched between I_{OS_PW} and the value set by ILIM_H according to the Power Wake Functionality.

2. DCP Load present governed by the “Power Wake” limits.

3. DCP Load present governed by the “Non-Power Wake” limits.

4. No VOUT discharge when charging between 1111 and 1110.

5. CDP Load present governed by the “Non-Power Wake” limits.

Output Discharge

To allow a charging port to renegotiate current with a portable device, SLGC55545V uses the VBUS discharge function. It proceeds by turning off the power switch while discharging VOUT, then turning back ON the power switch to reassert the VOUT voltage. This discharge function is automatically applied when a change at the CTLx lines results in any of the following mode transitions.

- Any transition to and from CDP
- Any transition to and from SDP

In addition to this, can be achieved using the mode “000”.

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Overcurrent Protection

When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before VIN has been applied.

The SLGC55545V senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for nominally one to two microseconds before the current-limit circuit can react. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device will remain off until the junction temperature cools approximately 10°C and will then re-start. The device will continue to cycle on/off until the over-current condition is removed.

FAULT# Response

The FAULT# open-drain output is asserted (active low) during an over-temperature or current limit condition. The output remains asserted until the fault condition is removed. The SLGC55545V is designed to eliminate false FAULT# reporting by using an internal deglitch circuit for current limit conditions without the need for external circuitry. This ensures that FAULT# is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Over-temperature conditions are not deglitched and assert the FAULT# signal immediately.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

Thermal Sense

The SLGC55545V protects itself with two independent thermal sensing circuits that monitor the operating temperature of the power distribution switch and disables operation if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an over-current condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135 °C and the part is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155 °C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 10 °C. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output FAULT# is asserted (active low) during an over-temperature shutdown condition.

Power Wake

The SLGC55545V monitors charging current at the VOUT pin and provide sa mechanism via the STATUS# pin to switch out the high power DC-DC and switch to a low power LDO when charging current requirement is < 45 mA (typ). This saves system power in S4/S5 state while the port has no peripheral device connected. The function is specified in the truth table setting “0011”

Power Management

When a connected peripheral device request high current charge for their battery, the system may not be able to support to enough current for every USB port. In this situation, the SLGC55545V supports a port power management function to help the system designer to control their USB port power. STATUS# trip point is based on ILIM_L current limit value to set the point. When a connected peripheral device requires port power charge current higher than ILIM_L+60 mA 200 ms then the STATUS# pin will automatically output LOW to let system know. When the charge current is below ILIM_L + 60 mA, 3 s then STATUS# return back to HIGH. This function works via truth table setting “0111” DCP_Auto mode and “1111” CDP mode.

Application and Layout Guidelines

- The designed power supply range is from 4.5 V to 5.5 V. If the input supply is located more than a few inches from the device, an input bypass capacitor larger than 0.1 µF is recommended.
- The trace routing from the upstream regulator to the VIN pin must be as short as possible to reduce the voltage drop and parasitic inductance.
- The trace routing from the Current-Limit Set Resistors to the device must be as short as possible to reduce parasitic effects on Current-Limit accuracy.

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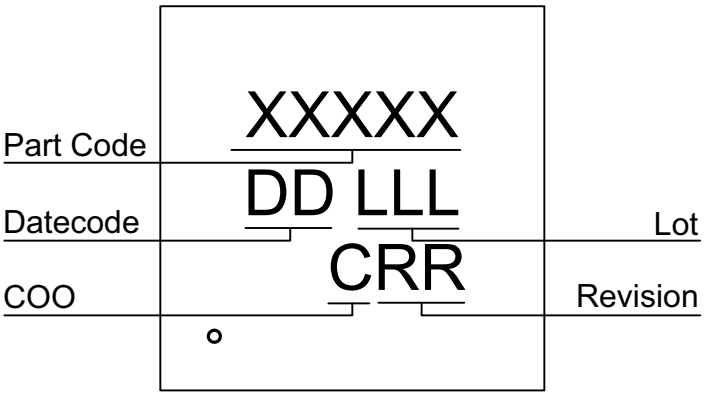
Package Top Marking System Definition



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

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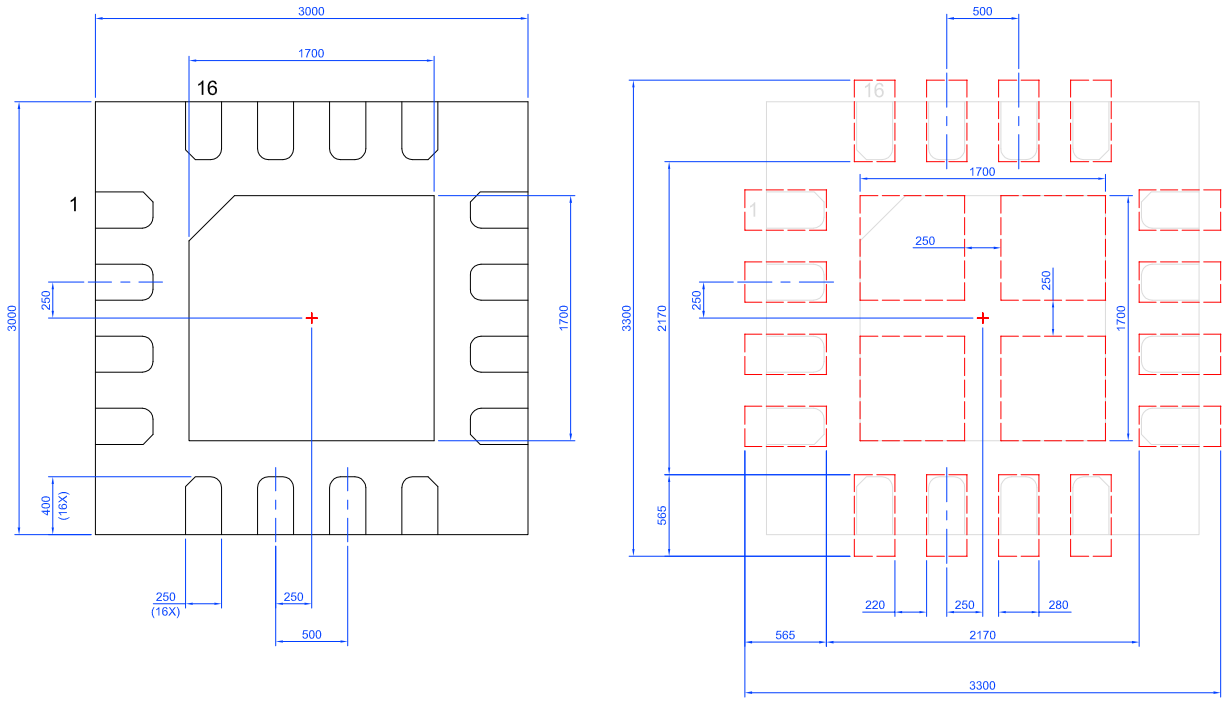
PCB Landing Pattern

Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)



Marking View

UNIT: um

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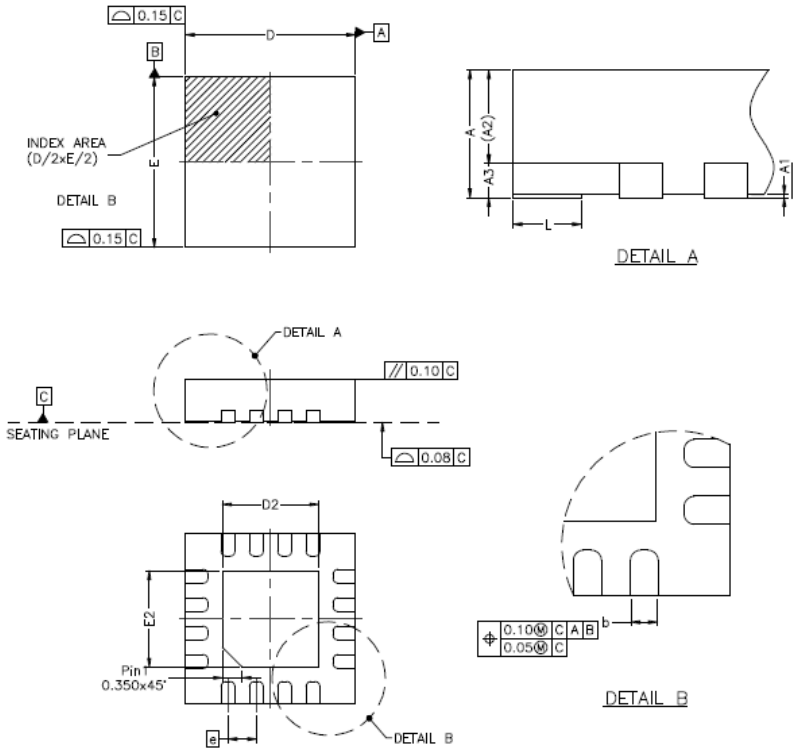
Package Drawing and Dimensions

16 Lead TQFN Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	2.90	3.00	3.10	114	118	122
D1		–			–	
D2	1.60	1.70	1.80	63	67	71
E	2.90	3.00	3.10	114	118	122
E1		–			–	
E2	1.60	1.70	1.80	63	67	71
e	0.50 BSC			20 BSC		
L	0.35	0.40	0.45	14	16	18

NOTE :

1. REFER TO JEDEC STD: MO–220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

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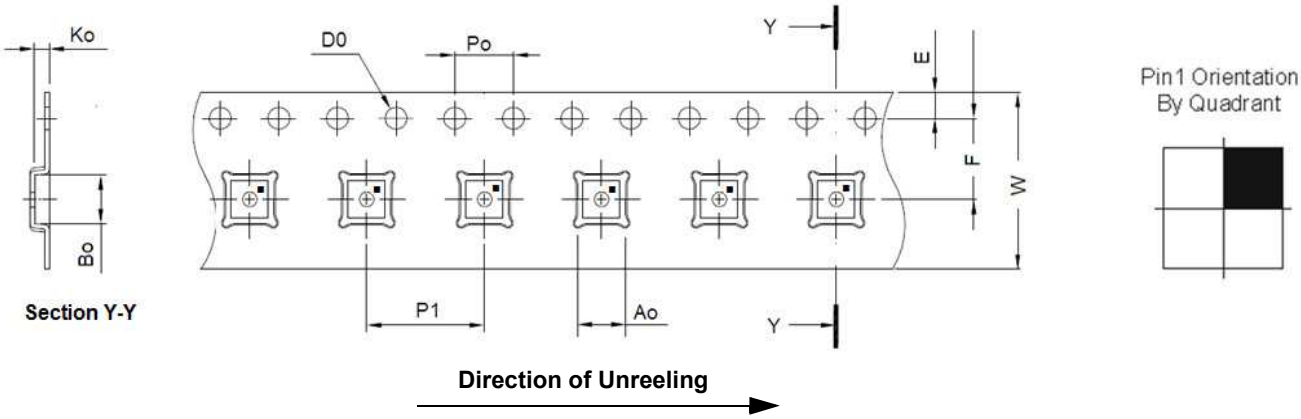
Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TQFN 16L 3x3mm Green	16	3 x 3 x 0.75	5,000	10,000	330 / 100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TQFN 16L 3X3mm Green	3.3	3.3	1.0	4.0	8.0	1.55	1.75	5.5	12.0



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 6.75 mm^3 (nominal). More information can be found at www.jedec.org.

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Revision History

Date	Version	Change
2/8/2022	1.04	Updated Company name and logo Fixed typos
3/5/2020	1.03	Updated Style and formatting
3/13/2019	1.02	Added Landing Pattern
7/11/2017	1.01	Added Application and Layout Guidelines
3/27/2017	1.00	Production Release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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