SLG7RN47363

GreenPAK™ Sun tracker. Linear motor driving with optical positioning system

Description

Renesas SLG7RN47363 is a low power and small form device. The SoC is housed in a 3 mm x 3 mm STQFN package which is optimal for using with small devices.

This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations visit the GreenPAK website.

Click here to download the GreenPAK file for the SLG7RN47363 design.

Email GreenPAKSupport@renesas.com for more information and GreenPAK design support.

Features

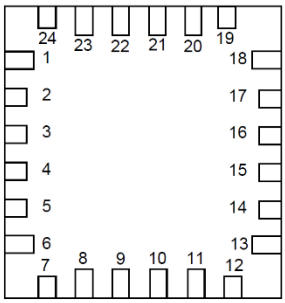
- Low power consumption
- Pb-free/RoHS compliant/Halogen-free
- 24-pin STQFN

Output Summary

- 2 Outputs – 3-State Output 2X

1. Pin Information

1.1 Pin Assignments



(Top View)
STQFN-24

Figure 1. Pin Assignments – Top View

1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Number	Pin Name
1	VDDA	13	VDD
2	AGND	14	GND
3	OP0_IN-	15	CLK
4	OP0_IN+	16	UP(LEFT)
5	OP0_OUT	17	SW1_OUT_A
6	RH0_A	18	SW1_OUT_B
7	RH0_B	19	SW0_OUT_B
8	RH1_A	20	SW0_OUT_A
9	RH1_B	21	Up/nDown
10	SCL	22	OP1_OUT
11	SDA	23	OP1_IN+
12	DOWN(RIGHT)	24	OP1_IN-

Table 2. Functional Pin Description

Pin Number	Pin Name	Type	Pin Description	Internal Resistors
1	VDDA	Analog Power Supply	Analog Power Supply	--
2	AGND	AGND	Ground	--
3	OP0_IN-	Analog Input/Output	Analog Input/Output	floating
4	OP0_IN+	Analog Input/Output	Analog Input/Output	floating
5	OP0_OUT	Analog Input/Output	Analog Input/Output	floating
6	RH0_A	Analog Input/Output	Analog Input/Output	floating
7	RH0_B	Analog Input/Output	Analog Input/Output	floating
8	RH1_A	Analog Input/Output	Analog Input/Output	floating
9	RH1_B	Analog Input/Output	Analog Input/Output	floating
10	SCL	Digital Input	Digital Input without Schmitt trigger	floating
11	SDA	Digital Input	Digital Input without Schmitt trigger	floating
12	DOWN(RIGHT)	Digital Output	3-State Output 2X	floating
13	VDD	PWR	Supply Voltage	--
14	GND	GND	Ground	--
15	CLK	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
16	UP(LEFT)	Digital Output	3-State Output 2X	floating
17	SW1_OUT_A	Analog Input/Output	Analog Input/Output	floating
18	SW1_OUT_B	Analog Input/Output	Analog Input/Output	floating
19	SW0_OUT_B	Analog Input/Output	Analog Input/Output	floating
20	SW0_OUT_A	Analog Input/Output	Analog Input/Output	floating
21	Up/nDown	Digital Input	Digital Input without Schmitt trigger	floating
22	OP1_OUT	Analog Input/Output	Analog Input/Output	floating
23	OP1_IN+	Analog Input/Output	Analog Input/Output	floating
24	OP1_IN-	Analog Input/Output	Analog Input/Output	floating

2. Specifications

2.1 Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
V_{DD} to GND, V_{DDA} to AGND (Note 1)		-0.3	7	V
Maximum Slew Rate of V_{DDA}		--	2	V/µs
Voltage at Input Pin		GND-0.3	V_{DD}+0.3	V
Current at Input Pin		-1.0	1.0	mA
Maximum Average or DC Current through V_{DDA} or AGND Pin (Per chip side)	T_J = +85 °C	--	110	mA
	T_J = +110 °C	--	50	mA
Maximum Average or DC Current through V_{DD} or GND Pin (Per chip side)	T_J = +85 °C	--	100	mA
	T_J = +110 °C	--	50	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Note 1: V_{DDA} must be equal to V_{DD}

2.2 IO Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		3	5	5.5	V
Operating Temperature	T_A		-40	+25	+85	°C
Input Capacitor at V_{DD} pin	C_{VDD}		0.1	--	--	µF
Input Capacitance	C_{IN}	PINs 10, 11	--	2.9	--	pF
		PIN 12	--	3.6	--	pF
		PINs 15, 16	--	3.8	--	pF
		PINs 17, 18, 19	--	10.2	--	pF
		PIN 20	--	27.8	--	pF
		PIN 21	--	5.7	--	pF
Quiescent Current	I_Q	Static inputs and floating outputs PIN#10 and PIN#11 are HIGH, PIN#21 is LOW	--	90	--	µA
Maximal Voltage Applied to any PIN in High-Impedance State	V_O		--	--	V_{DD}+0.3	V
HIGH-Level Input Voltage	V_{IH}	Logic Input (Note 1)	0.7xV_{DD}	--	V_{DD}+0.3	V
LOW-Level Input Voltage	V_{IL}	Logic Input (Note 1)	GND-0.3	--	0.3xV_{DD}	V
HIGH-Level Output Voltage	V_{OH}	Push-Pull 2X, I_{OH} = 3 mA at V_{DD} = 3.3 V (Note 1)	3.171	--	--	V
		Push-Pull 2X, I_{OH} = 5 mA at V_{DD} = 5.0 V (Note 1)	4.845	--	--	V
LOW-Level Output Voltage	V_{OL}	Push-Pull 2X, I_{OL} = 3 mA, at V_{DD} = 3.3 V (Note 1)	--	--	0.102	V
		Push-Pull 2X, I_{OL} = 5 mA, at V_{DD} = 5.0 V (Note 1)	--	--	0.136	V
HIGH-Level Output Current (Note 2)	I_{OH}	Push-Pull 2X, V_{OH} = 2.4V at V_{DD} = 3.3 V (Note 1)	16.34	--	--	mA
		Push-Pull 2X, V_{OH} = 2.4V at V_{DD} = 5.0 V (Note 1)	47.07	--	--	mA
LOW-Level Output Current (Note 2)	I_{OL}	Push-Pull 2X, V_{OL}= 0.4V, at V_{DD} = 3.3 V (Note 1)	10.63	--	--	mA
		Push-Pull 2X, V_{OL} = 0.4V, at V_{DD} = 5.0 V (Note 1)	13.79	--	--	mA
Internal Pull-Down Resistance	R_{PULL_D}	Pull down on PIN 15 (Note 1)	--	1	--	MΩ
Delay1 Time	T_{DLY1}	At temperature +25 °C	147.0	151.3	155.7	ms
		At temperature -40 °C to +85 °C (Note 3)	146.8	151.3	164.9	ms
Delay2 Time	T_{DLY2}	At temperature +25°C	244.5	250.9	256.9	ms
		At temperature -40 °C to +85 °C (Note 3)	244.0	250.9	272.0	ms
Delay3 Time	T_{DLY3}	At temperature +25 °C	244.5	250.9	256.9	ms
		At temperature -40 °C to +85 °C (Note 3)	244.0	250.9	272.0	ms
Analog Comparator0 Threshold Voltage	V_{ACMP0}	Low to High transition, at temperature +25 °C	V_{DDA} * 0.015 - 20	--	V_{DDA} * 0.016 + 9	mV
		Low to High transition, at temperature -40 °C to +85 °C (Note 3)	V_{DDA} * 0.015 - 22	--	V_{DDA} * 0.016 + 8	mV
		High to Low transition, at temperature +25°C	V_{DDA} * 0.015 - 20	--	V_{DDA} * 0.016 + 9	mV
		High to Low transition, at temperature -40 °C to +85 °C (Note 3)	V_{DDA} * 0.015 - 22	--	V_{DDA} * 0.016 + 8	mV
Analog Comparator1 Threshold Voltage	V_{ACMP1}	Low to High transition, at temperature +25 °C	V_{DDA} * 0.156 - 19	--	V_{DDA} * 0.157 + 9	mV
		Low to High transition, at temperature -40 °C to +85 °C (Note 3)	V_{DDA} * 0.156 - 21	--	V_{DDA} * 0.157 + 8	mV
		High to Low transition, at temperature +25 °C	V_{DDA} * 0.125 - 19	--	V_{DDA} * 0.125 + 9	mV

		High to Low transition, at temperature -40 °C to +85 °C (Note 3)	V_{DDA} * 0.125 - 21	--	V_{DDA} * 0.125 + 8	mV
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	1.9	2.7	ms
Power-On Threshold	PON_{THR}	V_{DD} Level Required to Start Up the Chip	1.63	--	2.04	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level Required to Switch Off the Chip	0.96	--	1.54	V

Note 1: No hysteresis.
Note 2: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 3: Guaranteed by Design.

2.3 Operational Amplifier0,1 Electrical Characteristics

V_{DDA} = 2.4 V to 5.5 V, V_{CM} = V_{DDA} /2, V_{OUT} ≈ V_{DDA} /2, R_L=100 kΩ to V_{DDA} /2, C_L= 50 pF, T_A = 25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	Guaranteed by PSRR Test	2.4	--	5.5	V
Gain Bandwidth Product	GBW	R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF, G = +1V/V, BW = 128 kHz	--	124	--	kHz
Input Offset Voltage	V_{OFFSET}	BW = 128 kHz	--	69	500	µV
		BW = 128 kHz, T_A = -40°C to +85 °C	--	69	930	µV
Input Common-Mode Voltage Range	V_{CMR}	T_A = - 40 °C to +85 °C	-0.2	--	V_{DD}+0.2	V
Common-Mode Rejection Ratio	CMRR	All Op Amps, GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T_A = -40 °C to +85 °C	73.5	102	--	dB
		All Op Amps, GND < V_{CM} < GND + 0.8 V or V_{DD} - 0.8V < V_{CM} < V_{DD}	69.7	101	--	dB
Power Supply Rejection Ratio	PSRR	V_{CM} = V_{DD}/2, T_A = -40 °C to +85 °C	80	101	--	dB
		V_{CM} = GND, T_A = -40 °C to +85 °C	83	102	--	dB
Input Bias Current	I_B	T_A = +25 °C	--	1.9	±9	pA
		T_A = +85 °C		1.9	±258	pA
Input Offset Current	I_{OFFSET}	T_A = +25°C	--	--	3.2	pA
		T_A = +85 °C	--	--	210	pA
Common-Mode Input Resistance	R_{CM}		--	$3*10^{12}$	--	Ω
Differential Input Resistance	R_{DIFF}		--	10^{13}	--	Ω
DC Open Loop Gain	A_{OL}	R_{LOAD} = 1 MΩ, GND + 0.1V < V_{OUT} < V_{DD} - 0.1V, T_A =-40°C to +85 °C	103.3	125	--	dB
		R_{LOAD} = 50 kΩ, GND + 0.5V < V_{OUT} < V_{DD} - 0.5V, T_A =-40°C to +85 °C	103.4	125	--	dB
Slew Rate	SR	R_{LOAD} = 50 kΩ, C_{LOAD} = 85 pF, BW = 128 kHz, T_A = -40°C to +85 °C	--	0.09	--	V/µs

Note 1: AGND = GND, unless otherwise noted.
Note 2: Equivalent offset voltage of the amplifier after user's trim using digital rheostat. Gain of the amplifier is G=200 and the zero output voltage level Vzero = V_{DD}/2.
Note 3: Op amps analog supporting blocks are always turned on.

2.4 Analog Switch0/Voltage Regulator EC

T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted.

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum Voltage at Pins	V_{AS}	Voltage between any Analog Switch pin to AGND	0	--	V_{DD}+0.3	V
Maximum Switching Frequency	f_{MAX}	Pull Up	2.5	--	--	MHz
		Pull Up, V_{DD} = 2.4 V	3.9	--	--	MHz
		Pull Down	363	--	--	kHz

		Pull Down, V_{DD} = 2.4 V	363	--	--	kHz
ON Resistance	R_{ON}	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T = +25°C	--	30	53	Ω
		V_{DD} = 3.3 V, V_{IN} > V_{DD} - 1.2, P-ch FET, T = +25°C	--	2	3	Ω
OFF Leakage Current	I_{PWROFF}	Switch OFF; from IN to OUT V_A = V_{DD} or V_B = V_{DD}	--	--	17	nA
Maximum ON-state Switch Current	I_{SW_MAX}	V_A = V_{DD}, load connected to ground, V_{AB} =0.4 V	--	--	300	mA
Maximum Pulse Current Through Switch	I_{SW_PULSE}	Pulse duration = 1 ms, Duty cycle < 5 %	--	--	500	mA

2.5 Analog Switch1/Current Sink EC

T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted.

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum Voltage at Pins	V_{AS}	Voltage between any Analog Switch pin to AGND	0	--	V_{DD}+0.3	V
Maximum Switching Frequency	f_{MAX}	Pull Up	1.6	--	--	MHz
		Pull Up, V_{DD} = 2.4 V	1.6	--	--	MHz
		Pull Down	5	--	--	kHz
		Pull Down, V_{DD} = 2.4 V	5	--	--	kHz
ON Resistance	R_{ON}	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T = +25°C	--	0.8	1.5	Ω
		V_{DD} = 3.3 V, V_{IN}>V_{DD}-1.2, P-ch FET, T = +25°C	--	53.4	204	Ω
OFF Leakage Current	I_{PWROFF}	Switch OFF; from IN to OUT V_A = V_{DD} or V_B = V_{DD}	--	--	34	nA
Maximum ON-state Switch Current	I_{SW_MAX}	V_A = V_{DD}, load connected to ground, V_{AB} =0.4 V	--	--	300	mA
Maximum Pulse Current Through Switch	I_{SW_PULSE}	Pulse duration = 1 ms, Duty cycle < 5 %	--	--	500	mA

2.6 100K Digital Rheostat EC

V_A = V_{DD}, V_B = GND, T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Rheostat Pin Voltage Range	V_{DR}	Voltage between any (A or B) pins and AGND	AGND	--	V_{DDA}	V
Digital Rheostat Resistance	R_{DR}	Full resistance with all switches open (Note 1)	94.426	101.582	113.741	kΩ
Minimal Rheostat Resistance	R_{DR_MIN}	Code = 0x00	43.679	--	84.779	Ω
Number of taps	N_{TAPS}		--	--	1024	
Rs* Resistance (Initial data)	Calculated resistance RH0	Code=10	--	0.99	--	kΩ
Rs* Resistance (Initial data)	Calculated resistance RH1	Code=10	--	0.99	--	kΩ
Step Resistance	R_S	V_{DD} = (2.4 V; 3.3 V; 5.5 V), V_{DDA} = (1 V; -1 V). T = (-40 °C; +25 °C; +85 °C)	--	99.236	--	Ω
Max current through Rheostat	I_{DR_MAX}	T = +25°C	--	--	2	mA

Note 1: User can calculate actual Digital Rheostat value using calibration data from NVM.
Note 2: Includes internal timing. External circuit should be counted separately.

2.7 I²C Specification

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Clock Frequency, SCL	f_{SCL}		--	--	1000	kHz
Clock Pulse Width, LOW	t_{LOW}		500	--	--	ns
Clock Pulse Width, HIGH	t_{HIGH}		260	--	--	ns
Input Filter Spike Suppression (SCL, SDA)	t_I		--	--	50	ns
Clock LOW to Data Out Valid	t_{AA}		--	--	450	ns
Bus Free Time between STOP and START	t_{BUF}		500	-	--	ns
Start Hold Time	t_{HD_STA}		260	--	--	ns
Start Set-up Time	t_{SU_STA}		260	--	--	ns
Data Hold Time	t_{HD_DAT}	Logic Input with Schmitt Trigger	0	--	--	ns
Data Set-up Time	t_{SU_DAT}	Logic Input with Schmitt Trigger	50	--	--	ns
Inputs Rise Time	t_R		--	--	120	ns
Inputs Fall Time	t_F		--	--	120	ns
STOP Set-up Time	t_{SU_STO}		260	--	--	ns
Data Out Hold Time	t_{DH}		50	--	--	ns

3. Chip Address

HEX	BIN	DEC
0x08	0001000	8

4. I²C Description

4.1 I²C Basic Command Structure

Each command to the I²C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 2. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1019:1016>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 2 shows this basic command structure.

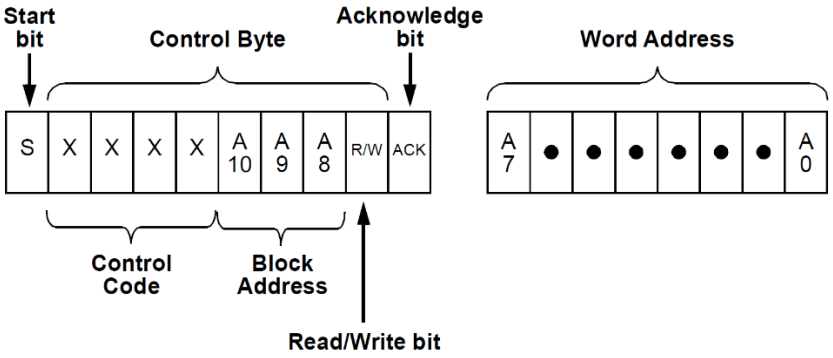


Figure 2. I²C Basic Command Structure

4.2 I²C Serial General Timing

Shown in Figure 3 is the general timing characteristics for the I²C Serial Communications block.

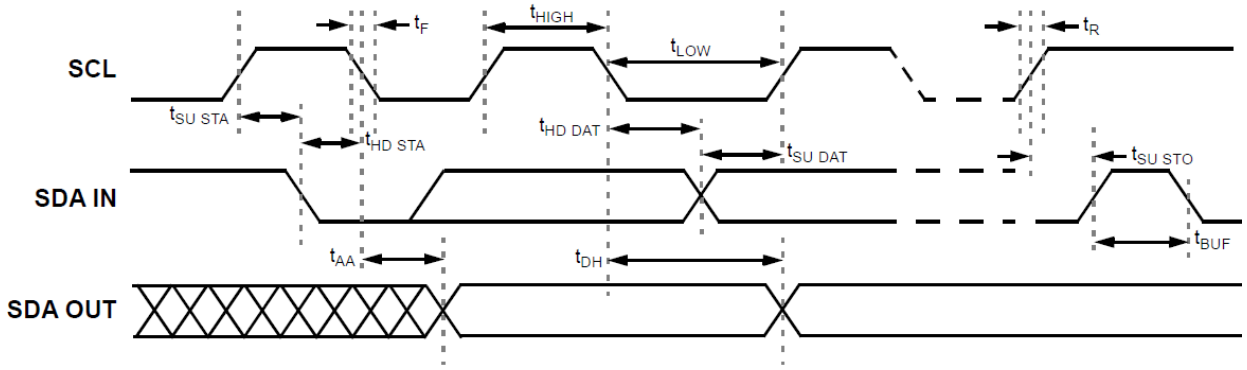


Figure 3. I²C Serial General Timing

4.3 I²C Serial Communications: Read and Write Commands

Following the Start condition from the Controller, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), are placed onto the bus by the Bus Controller. After the I²C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the Controller is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN47363 to the correct data byte to be written. After the SLG7RN47363 sends another Acknowledge bit, the Bus Controller will transmit the data byte to be written into the addressed memory location. The SLG7RN47363 again provides an Acknowledge bit and then the Bus Controller generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN47363 generates the Acknowledge bit.

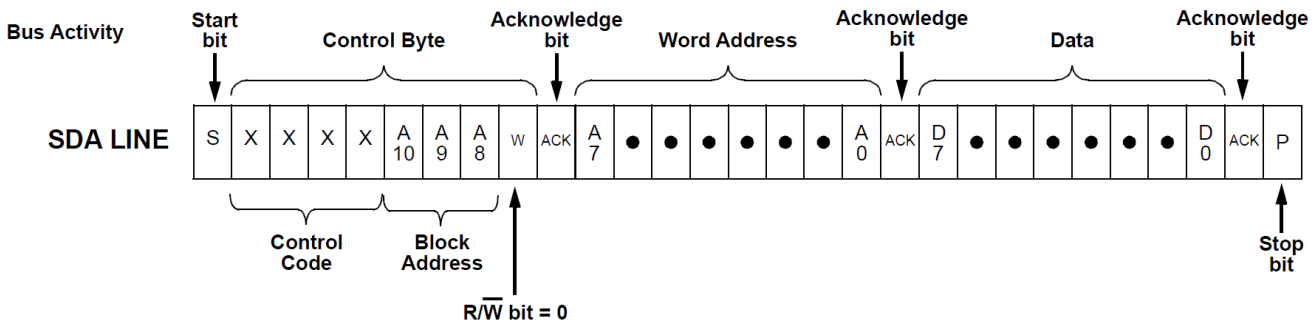


Figure 4. I²C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Controller issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7RN47363 issues an Acknowledge bit, followed by the requested eight data bits.

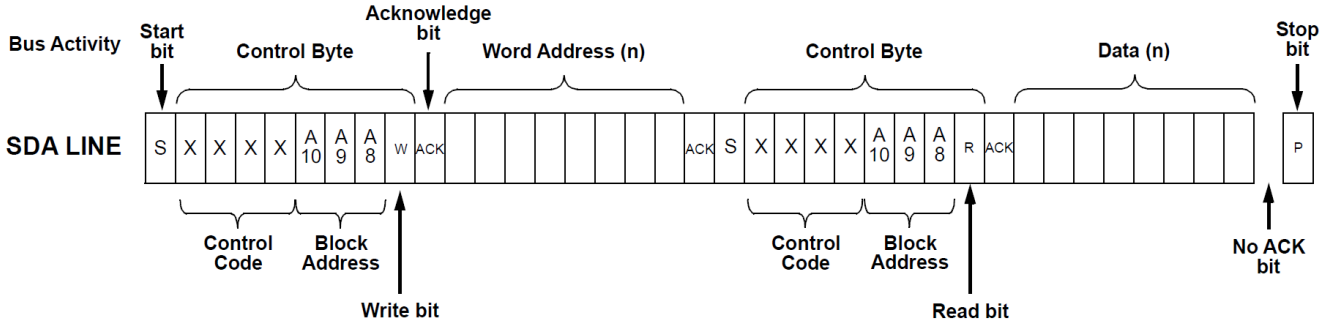
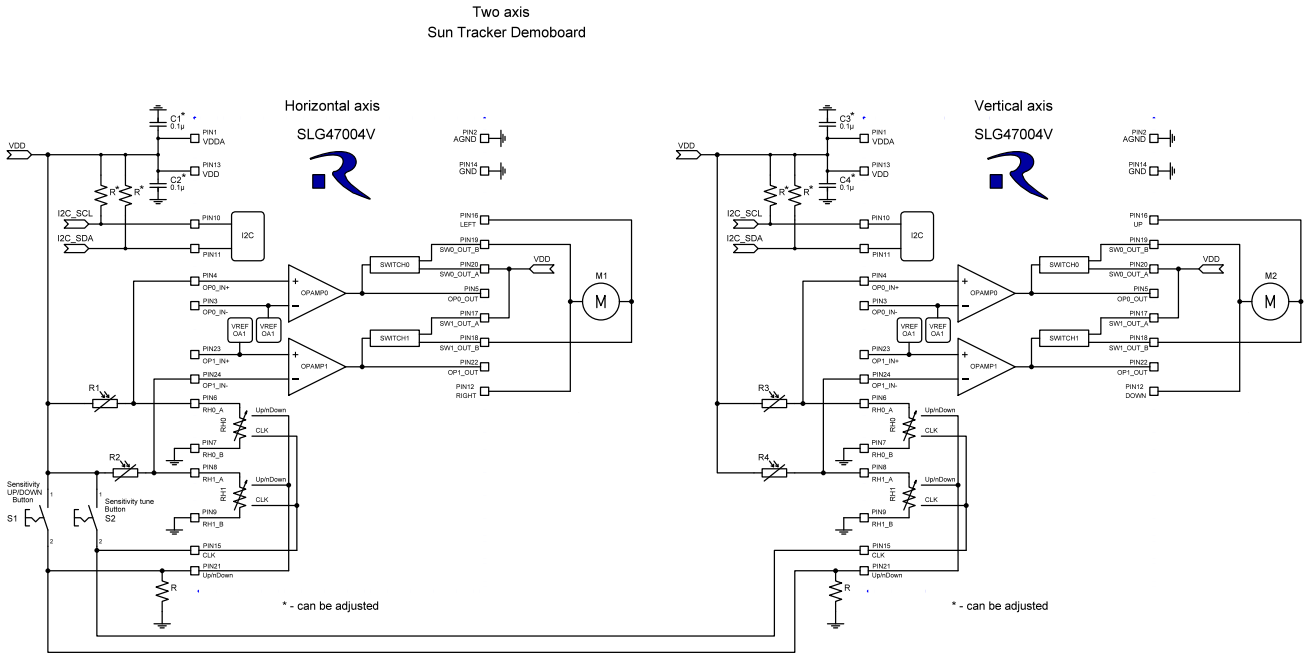


Figure 5. I²C Random Read Command

4.4 Chip reconfiguration

SLG7RN47363 has an ISP capability. This means that the chip internal blocks configuration may be changed on the fly or even re-programmed via I²C. If there is a need for temporary change of the chip configuration (it will be reset to the programmed configuration after the chip is reset or power on again) one should use Registers (A10, A9, A8 = “000”). To reprogram a configuration via I²C NVM should be accessed with A10, A9, A8 = “010”. Please keep in mind that random byte write procedure is not supported, this may lead to incorrect chip configuration. Only page write procedure is supported.

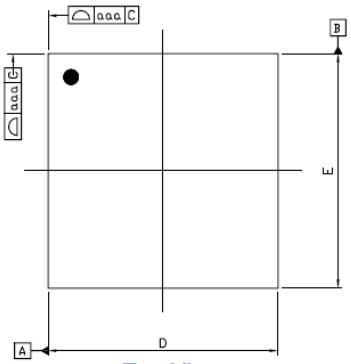
5. Typical Application Circuit



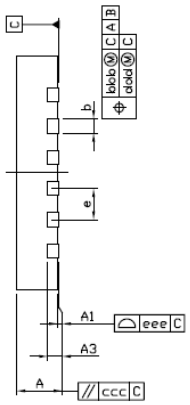
6. Package Information

6.1 Package Outline Drawing for STQFN-24

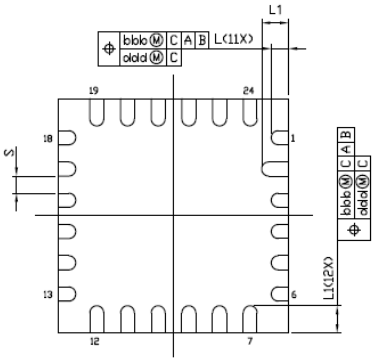
JEDEC MO-220
IC Net Weight: 0.0116 g



Top View



Side View



Bottom View

PKG CODE	UQFN					
SYMBOLS	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
b	0.13	0.18	0.23	0.005	0.007	0.009
D	2.95	3.00	3.05	0.116	0.118	0.120
E	2.95	3.00	3.05	0.116	0.118	0.120
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.30	0.35	0.40	0.012	0.014	0.016
S	0.22 REF.			0.009 REF.		
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

"A1" MAX LEAD COPLANARITY 0.05mm
STANDARD TOLERANCE : ±0.05

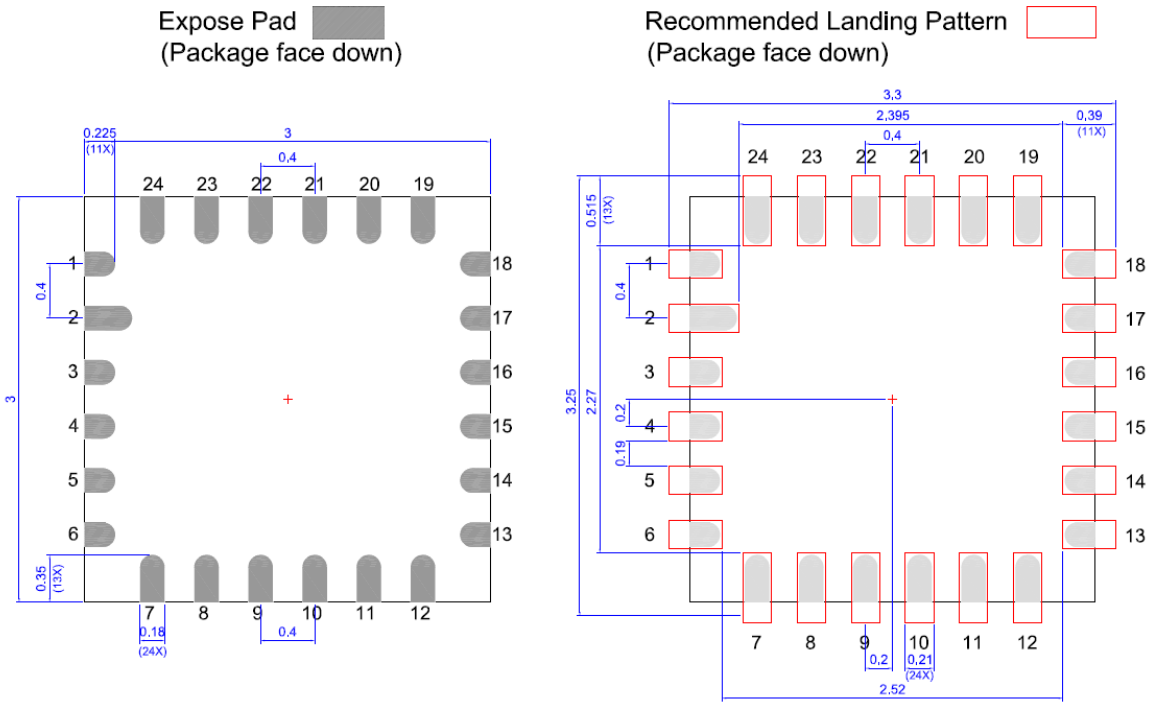
PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

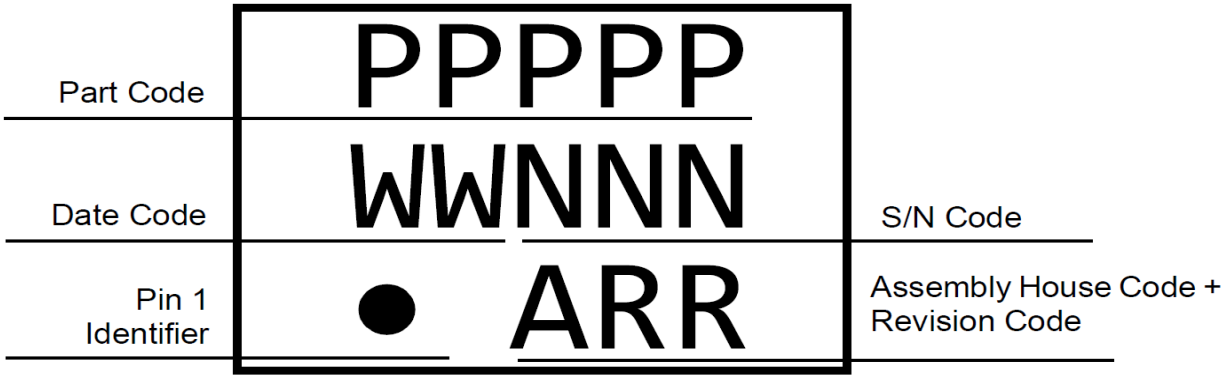
6.2 Recommended Reflow Soldering Profile

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from www.jedec.org.

6.3 Layout Guidelines



7. Marking Diagram



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	U	0x1F04387E			02/14/2024

Table 3. Memory Lock Options

Registers		NVM	
√	Unlocked	√	Unlocked
	Partly lock read		Read lock
	Partly lock write		Write/Erase lock
	Partly lock read and write		Lock read and write/erase

	Partly lock read and lock write	**Protect entire lock configuration**	
	Lock read and partly lock write		Enable
	Read lock	√	Disable
	Write lock		
	Lock read and write		
EEPROM			
√	Unlocked		
	Upper quarter of emulated EEPROM is write protected		
	Upper half of emulated EEPROM is write protected		
	Upper 3/4 of emulated EEPROM is write protected		
	Entire emulated EEPROM is write protected		
Rheostat 0 protect (NVM Configuration data)		**Rheostat 1 protect (NVM Configuration data)**	
√	Unprotected for read and write/erase	√	Unprotected for read and write/erase
	Fully protected for read		Fully protected for read
	Fully protected for write/erase		Fully protected for write/erase
	Fully protected for read and write/erase		Fully protected for read and write/erase

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

8. Ordering Information

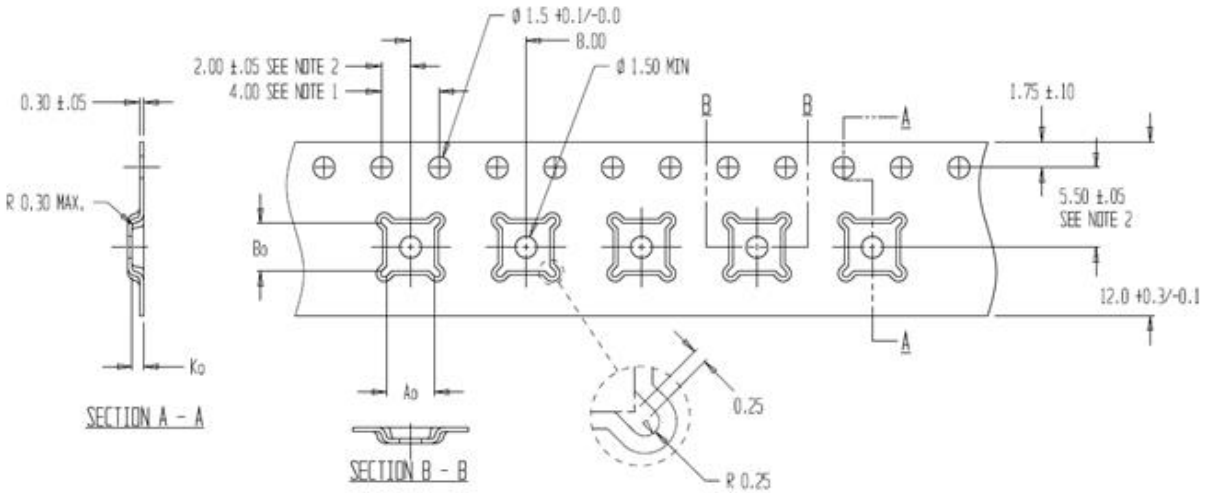
Part Number	Package Description
SLG7RN47363V	24-pin STQFN - Tape and Reel (5k units)

8.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader [min]		Trailer [min]		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 24L 3 mm x 3mm 0.4P FC Green	24	3 x 3 x 0.55	5000	100000	330 / 100	42	336	42	336	12	8

8.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 24L 3mmx3mm 0.4P FC Green	3.3	3.3	0.8	4	8	1.55	1.75	5.5	12



Notes:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. A0 AND B0 ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant1).

9. Revision History

Revision	Date	Description
1.00	Nov 21, 2025	Initial release Updated title
0.11	Nov 20, 2025	Reformatted according to Renesas template
0.10	Jun 6, 2024	New Design