SLG7RN46137

GreenPAK ™

CN363 Smart Power on/off Sequence Controller

General Description

Renesas SLG7RN46137 is a low power and small form device. The SoC is housed in a 1.6mm x 1.6mm STQFN package which is optimal for using with small devices.

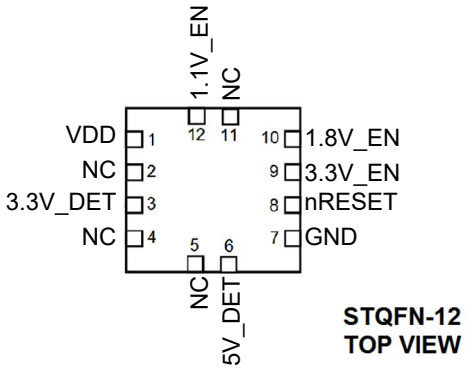
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package

Output Summary

1 Output - Open Drain NMOS 2X
3 Outputs - Push Pull 2X

Pin Configuration



STQFN-12
TOP VIEW

Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	3.3V_DET	Analog Input/Output	Analog Input/Output	floating
4	NC	--	Keep Floating or Connect to GND	--
5	NC	--	Keep Floating or Connect to GND	--
6	5V_DET	Analog Input/Output	Analog Input/Output	floating
7	GND	GND	Ground	--
8	nRESET	Digital Output	Open Drain NMOS 2X	floating
9	3.3V_EN	Digital Output	Push Pull 2X	floating
10	1.8V_EN	Digital Output	Push Pull 2X	floating
11	NC	--	Keep Floating or Connect to GND	--
12	1.1V_EN	Digital Output	Push Pull 2X	floating

Ordering Information

Part Number	Package Type
SLG7RN46137V	V=STQFN-12
SLG7RN46137VTR	STQFN-12 – Tape and Reel (3k units)

1. Use SLG7RN46137V to order. Shipments are automatically in Tape and Reel.
2. “TR” suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 2x	--	17	mA
	OD 2x	--	28	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	° C
Junction Temperature		--	150	° C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

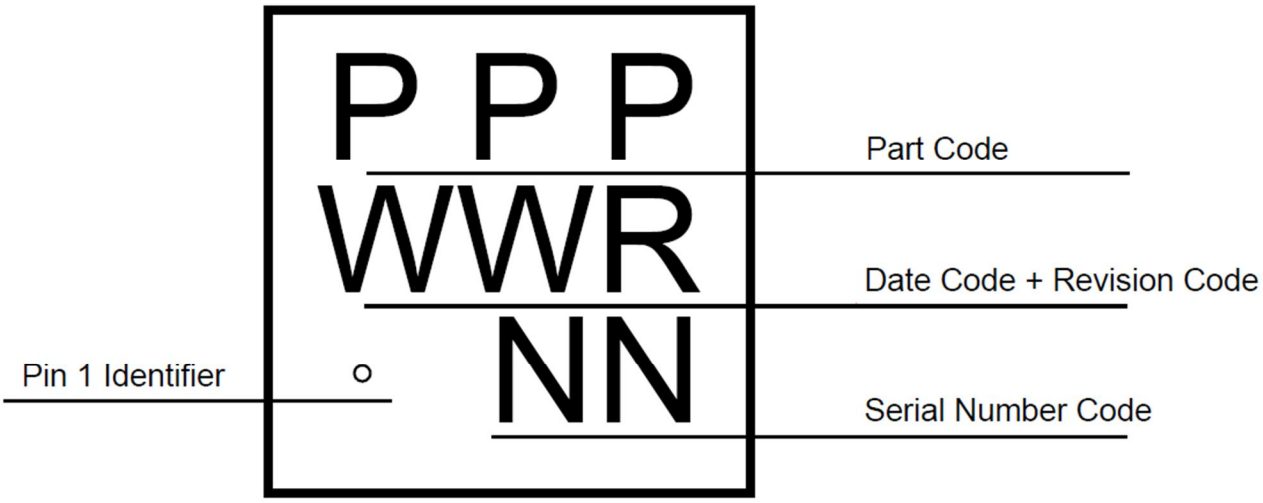
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2	5	5.5	V
T_A	Operating Temperature		-40	25	85	° C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	72	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=100µA, at VDD=1.8V	1.702	1.8	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=3mA, at VDD=3.3V	2.87	3.19	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=5mA, at VDD=5.0V	4.3	4.86	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 2X, I_{OL}=100µA, at VDD=1.8V	--	0.01	0.02	V
		Push-Pull 2X, I_{OL}=3mA, at VDD=3.3V	--	0.09	0.13	V
		Push-Pull 2X, I_{OL}=5mA, at VDD=5.0V	--	0.12	0.16	V
		Open Drain NMOS 2X, I_{OL}=100µA, at VDD=1.8V	--	0.01	0.01	V
		Open Drain NMOS 2X, I_{OL}=3mA, at VDD=3.3V	--	0.05	0.07	V
		Open Drain NMOS 2X, I_{OL}=5mA, at VDD=5.0V	--	0.07	0.09	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=VDD-0.2V, at VDD=1.8V	2.15	2.71	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=3.3V	11.264	19.66	--	mA

		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=5.0V	40.598	56.08	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 2X, V_{OL}=0.15V, at VDD=1.8V	1.52	2.66	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=3.3V	8.13	12.36	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=5.0V	11.59	19.46	--	mA
		Open Drain NMOS 2X, V_{OL}=0.15V, at VDD=1.8V	3.06	5.13	--	mA
		Open Drain NMOS 2X, V_{OL}=0.4V, at VDD=3.3V	16.26	22.9	--	mA
		Open Drain NMOS 2X, V_{OL}=0.4V, at VDD=5.0V	19.12	35.621	--	mA
T_{DLY1}	Delay1 Time	At temperature 25°C	185.9	200	232.1	µs
		At temperature -40 +85°C (Note 3)	179.7	200	326.3	µs
T_{DLY2}	Delay2 Time	At temperature 25°C	185.9	200	232.1	µs
		At temperature -40 +85°C (Note 3)	179.7	200	326.3	µs
T_{DLY3}	Delay3 Time	At temperature 25°C	185.9	200	232.1	µs
		At temperature -40 +85°C (Note 3)	179.7	200	326.3	µs
T_{CNT0}	Counter0 Period	At temperature 25°C	1.87	2	2.25	ms
		At temperature -40 +85°C (Note 3)	1.8	2	3.18	ms
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	1173	--	1273	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1143	--	1283	mV
		High to Low transition, at temperature 25°C	1135	--	1224	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1104	--	1235	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	1173	--	1269	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1145	--	1278	mV
		High to Low transition, at temperature 25°C	1132	--	1231	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1100	--	1237	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (Note 3)	ACMP 0 at temperature 25°C	--	50	--	mV
		ACMP 0 at temperature -40 +85°C	--	50	--	mV
		ACMP 1 at temperature 25°C	--	50	--	mV
		ACMP 1 at temperature -40 +85°C	--	50	--	mV
T_{SU}	Startup Time	From VDD rising past 1.35 V	--	0.27	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.11	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.
3. Guaranteed by Design.

Package Top Marking

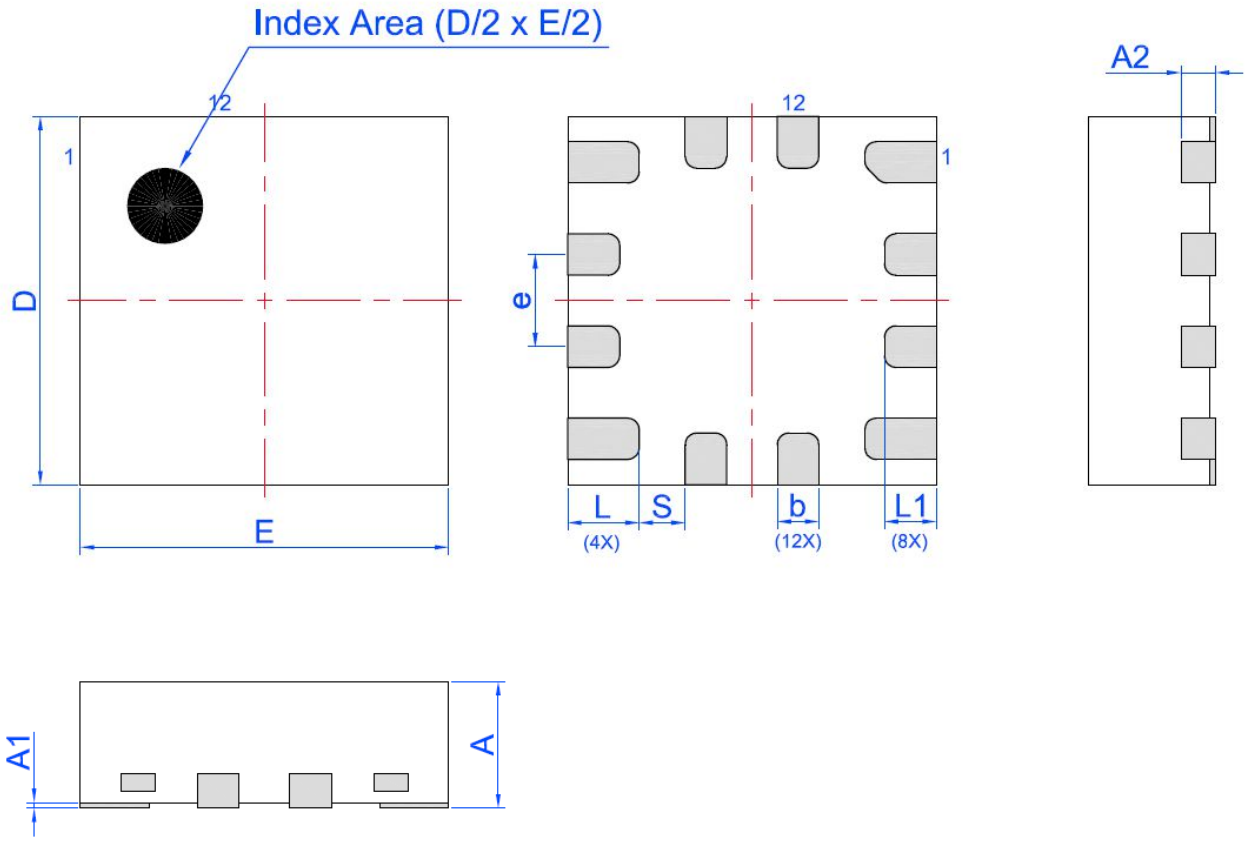


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	002	L	0xF73C6A3C	1AN	B	12/12/2022

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

12 Lead STQFN FC Package 1.6 x 1.6 mm
IC net weight: 0.0028 g



Unit: mm

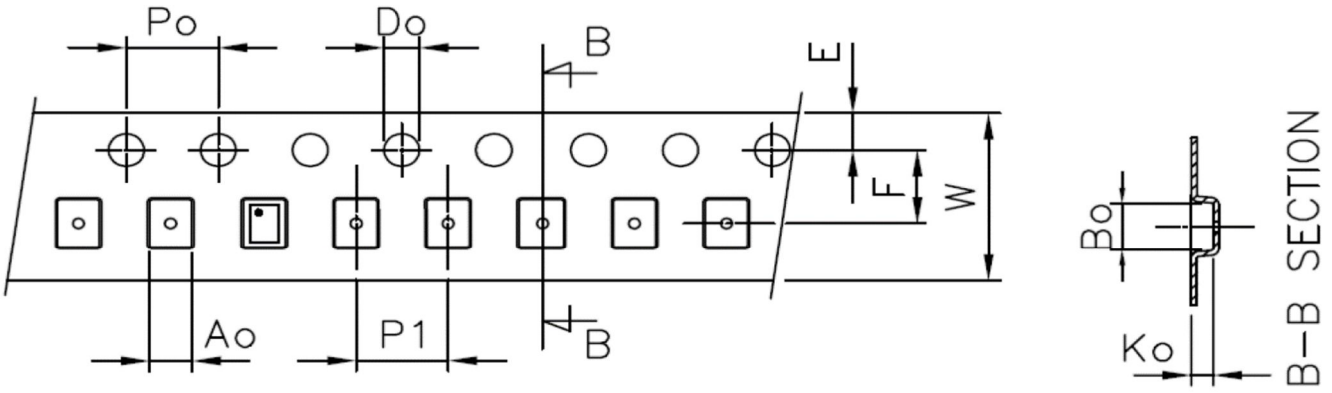
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FC 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

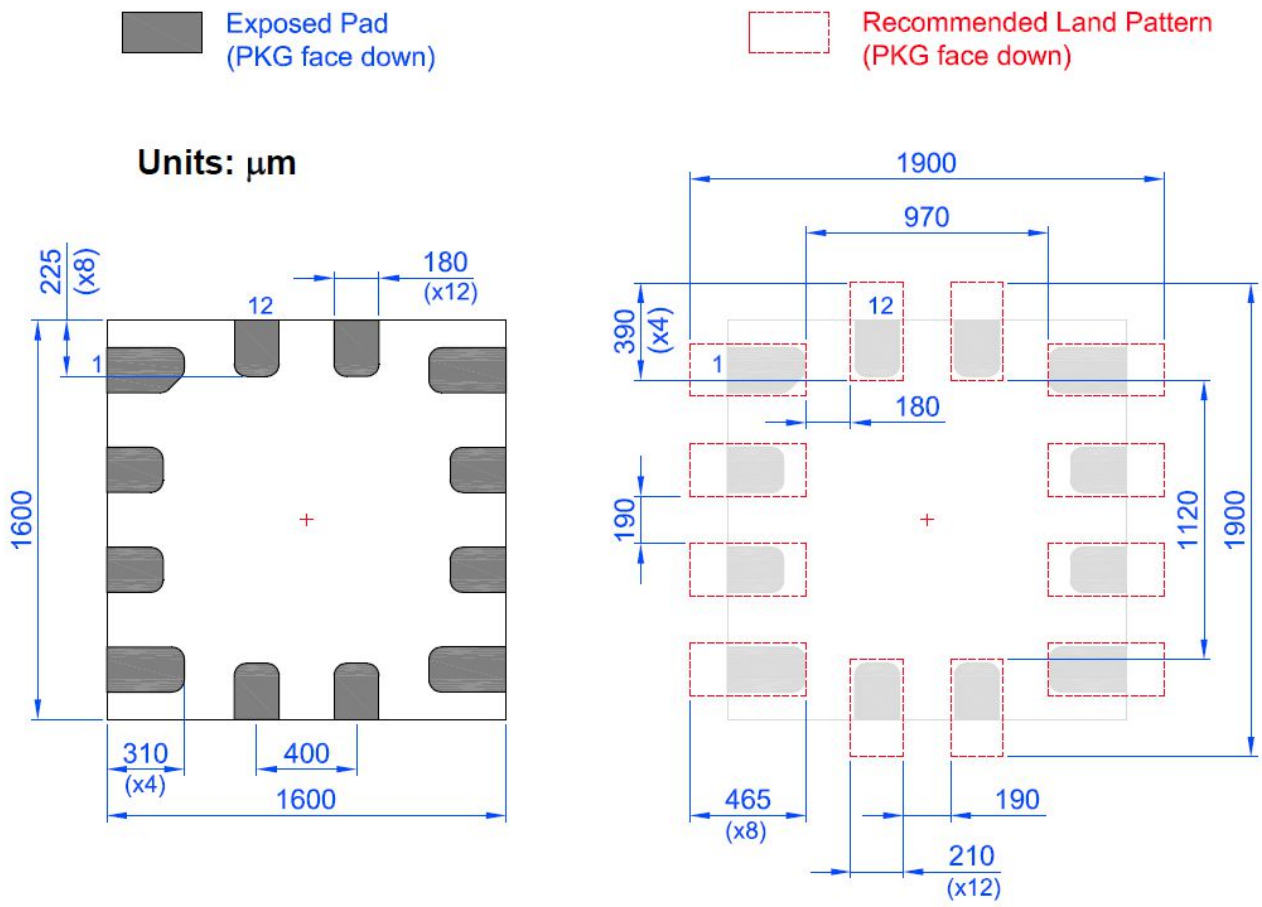
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FC 0.4P Green	1.8±0.05	1.8±0.05	±0.7	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern



Datasheet Revision History

Date	Version	Change
11/09/2022	0.10	New design for SLG46110 chip
11/14/2022	0.11	Updated Device Revision Table
11/18/2022	0.12	Change VDD range to 2.0~5.5V
11/17/2022	0.13	Updated Device Revision Table
12/12/2022	1.00	Production Release

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