## General Description

Renesas SLG7RN46131 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

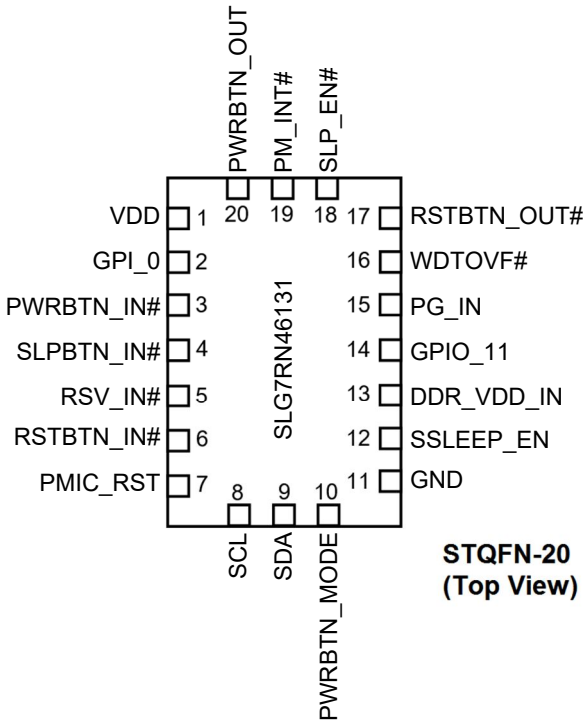
## Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

## Output Summary

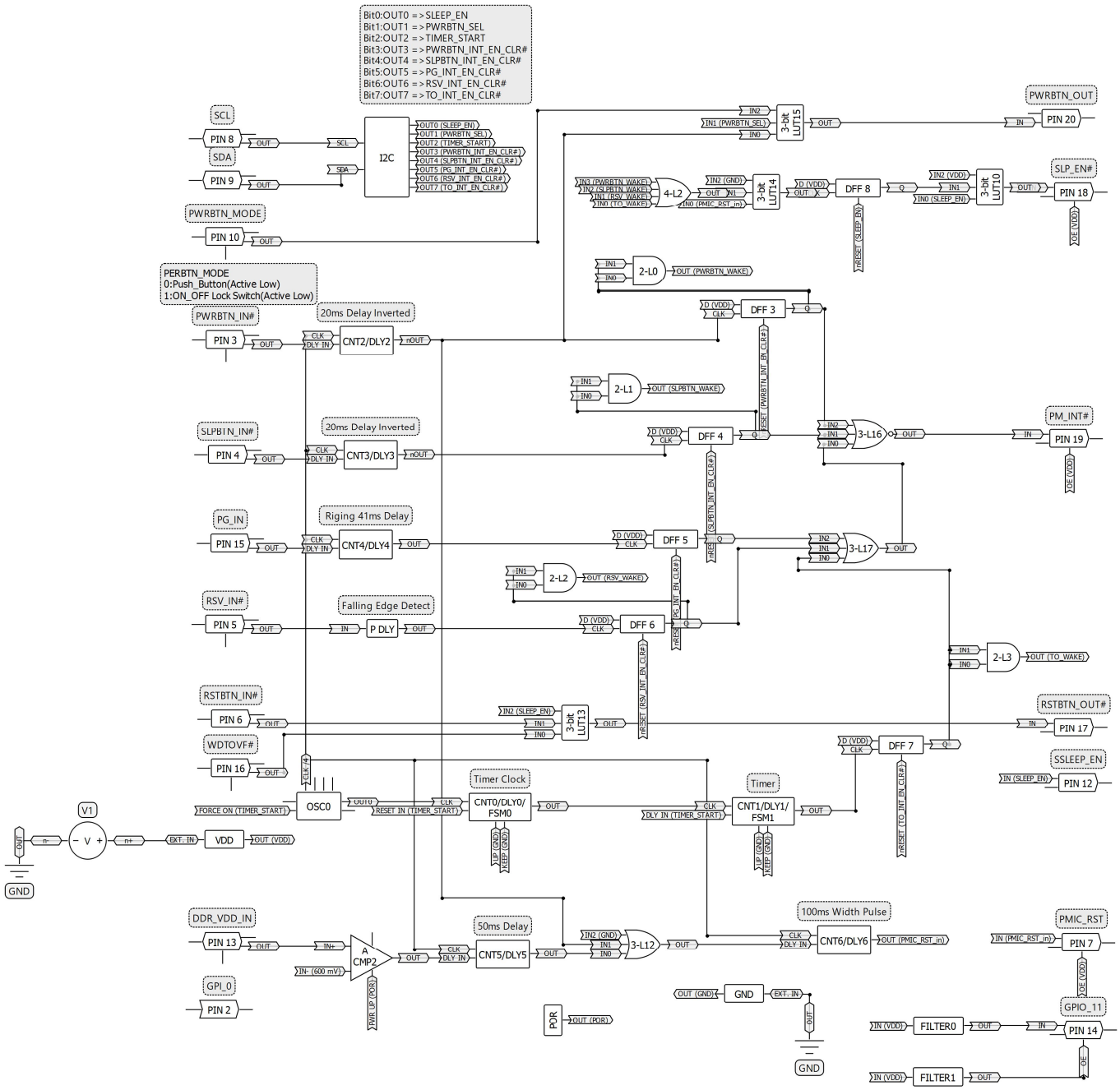
5 Outputs - Open Drain NMOS 1X
2 Outputs - Push Pull 1X

## Pin Configuration




**STQFN-20**
**(Top View)**

## Block Diagram



## Pin Configuration

| Pin # | Pin Name | Type | Pin Description | Internal Resistor |
|---|---|---|---|---|
| 1 | VDD | PWR | Supply Voltage | -- |
| 2 | GPI_0 | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 3 | PWRBTN_IN# | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 4 | SLPBTN_IN# | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 5 | RSV_IN# | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 6 | RSTBTN_IN# | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 7 | PMIC_RST | Digital Output | Push Pull 1X | floating |
| 8 | SCL | Digital Input | Low Voltage Digital Input | floating |
| 9 | SDA | Digital Input | Low Voltage Digital Input | floating |
| 10 | PWRBTN_MODE | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 11 | GND | GND | Ground | -- |
| 12 | SSLEEP_EN | Digital Output | Push Pull 1X | floating |
| 13 | DDR_VDD_IN | Analog Input/Output | Analog Input/Output | 1MΩ pulldown |
| 14 | GPIO_11 | Bi-directional | Low Voltage Digital Input / Open Drain NMOS 1X | 1MΩ pulldown |
| 15 | PG_IN | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 16 | WDTOVF# | Digital Input | Low Voltage Digital Input | 1MΩ pulldown |
| 17 | RSTBTN_OUT# | Digital Output | Open Drain NMOS 1X | floating |
| 18 | SLP_EN# | Digital Output | Open Drain NMOS 1X | floating |
| 19 | PM_INT# | Digital Output | Open Drain NMOS 1X | floating |
| 20 | PWRBTN_OUT | Digital Output | Open Drain NMOS 1X | floating |

## Ordering Information

| Part Number | Package Type |
|---|---|
| SLG7RN46131V | 20-pin STQFN |
| SLG7RN46131VTR | 20-pin STQFN - Tape and Reel (3k units) |

## Absolute Maximum Conditions

| Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage on VDD relative to GND | | -0.5 | 7 | V |
| DC Input Voltage | | GND - 0.5V | VDD + 0.5V | V |
| Maximum Average or DC Current (Through pin) | Push-Pull 1x | -- | 11 | mA |
| | OD 1x | -- | 11 | |
| Current at Input Pin | | -1.0 | 1.0 | mA |
| Input leakage (Absolute Value) | | -- | 1000 | nA |
| Storage Temperature Range | | -65 | 150 | °C |
| Junction Temperature | | -- | 150 | °C |
| ESD Protection (Human Body Model) | | 2000 | -- | V |
| ESD Protection (Charged Device Model) | | 1300 | -- | V |
| Moisture Sensitivity Level | | 1 | | |

## Electrical Characteristics

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 1.71 | 1.8 | 5.5 | V |
| $T_A$ | Operating Temperature | | -40 | 25 | 85 | °C |
| $C_{VDD}$ | Capacitor Value at VDD | | -- | 0.1 | -- | µF |
| $C_{IN}$ | Input Capacitance | | -- | 4 | -- | pF |
| $I_Q$ | Quiescent Current | Static inputs and floating outputs | -- | 56 | -- | µA |
| $V_O$ | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | VDD | V |
| $I_{VDD}$ | Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2) | $T_J$ = 85°C | -- | -- | 45 | mA |
| | | $T_J$ = 110°C | -- | -- | 22 | mA |
| $I_{GND}$ | Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2) | $T_J$ = 85°C | -- | -- | 86 | mA |
| | | $T_J$ = 110°C | -- | -- | 41 | mA |
| $V_{IH}$ | HIGH-Level Input Voltage | Low-Level Logic Input at VDD=1.8V | 0.94 | -- | VDD | V |
| | | Low-Level Logic Input at VDD=3.3V | 1.06 | -- | VDD | V |
| | | Low-Level Logic Input at VDD=5.0V | 1.15 | -- | VDD | V |
| $V_{IL}$ | LOW-Level Input Voltage | Low-Level Logic Input at VDD=1.8V | 0 | -- | 0.52 | V |
| | | Low-Level Logic Input at VDD=3.3V | 0 | -- | 0.67 | V |
| | | Low-Level Logic Input at VDD=5.0V | 0 | -- | 0.77 | V |
| $V_{OH}$ | HIGH-Level Output Voltage | Push-Pull 1X, $I_{OH}$=100µA, at VDD=1.8V | 1.69 | 1.79 | -- | V |
| | | Push-Pull 1X, $I_{OH}$=3mA, at VDD=3.3V | 2.7 | 3.12 | -- | V |
| | | Push-Pull 1X, $I_{OH}$=5mA, at VDD=5.0V | 4.15 | 4.76 | -- | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW-Level Output Voltage | Push-Pull 1X, $I_{OL}$=100µA, at VDD=1.8V | -- | 0.009 | 0.013 | V |
| | | Push-Pull 1X, $I_{OL}$=3mA, at VDD=3.3V | -- | 0.13 | 0.23 | V |
| | | Push-Pull 1X, $I_{OL}$=5mA, at VDD=5.0V | -- | 0.19 | 0.24 | V |
| | | Open Drain NMOS 1X, $I_{OL}$=100µA, at VDD=1.8V | -- | 0.006 | 0.009 | V |
| | | Open Drain NMOS 1X, $I_{OL}$=3mA, at VDD=3.3V | -- | 0.08 | 0.15 | V |
| | | Open Drain NMOS 1X, $I_{OL}$=5mA, at VDD=5.0V | -- | 0.12 | 0.16 | V |
| $I_{OH}$ | HIGH-Level Output Current (Note 1) | Push-Pull 1X, $V_{OH}$=VDD-0.2V, at VDD=1.8V | 1.07 | 1.7 | -- | mA |
| | | Push-Pull 1X, $V_{OH}$=2.4V, at VDD=3.3V | 6.05 | 12.08 | -- | mA |
| | | Push-Pull 1X, $V_{OH}$=2.4V, at VDD=5.0V | 22.08 | 34.04 | -- | mA |
| $I_{OL}$ | LOW-Level Output Current (Note 1) | Push-Pull 1X, $V_{OL}$=0.15V, at VDD=1.8V | 0.92 | 1.69 | -- | mA |
| | | Push-Pull 1X, $V_{OL}$=0.4V, at VDD=3.3V | 4.88 | 8.24 | -- | mA |
| | | Push-Pull 1X, $V_{OL}$=0.4V, at VDD=5.0V | 7.22 | 11.58 | -- | mA |
| | | Open Drain NMOS 1X, $V_{OL}$=0.15V, at VDD=1.8V | 1.38 | 2.53 | -- | mA |
| | | Open Drain NMOS 1X, $V_{OL}$=0.4V, at VDD=3.3V | 7.31 | 12.37 | -- | mA |
| | | Open Drain NMOS 1X, $V_{OL}$=0.4V, at VDD=5.0V | 10.82 | 17.38 | -- | mA |
| $R_{PULL\_DOWN}$ | Internal Pull Down Resistance | Pull down on PINs 2, 3, 4, 5, 6, 10, 13, 14, 15, 16 | -- | 1 | -- | MΩ |
| $T_{DLY1}$ | Delay1 Time | At temperature 25°C | 9.28 | 10.53 | 11.6 | s |
| | | At temperature -40 +85°C (Note 3) | 8.42 | 10.53 | 12.71 | s |
| $T_{DLY2}$ | Delay2 Time | At temperature 25°C | 19.26 | 21.1 | 22.91 | ms |
| | | At temperature -40 +85°C (Note 3) | 17.48 | 21.1 | 25.09 | ms |
| $T_{DLY3}$ | Delay3 Time | At temperature 25°C | 19.26 | 21.1 | 22.91 | ms |
| | | At temperature -40 +85°C (Note 3) | 17.48 | 21.1 | 25.09 | ms |
| $T_{DLY4}$ | Delay4 Time | At temperature 25°C | 38.61 | 41.58 | 44.44 | ms |
| | | At temperature -40 +85°C (Note 3) | 35.03 | 41.58 | 48.66 | ms |
| $T_{DLY5}$ | Delay5 Time | At temperature 25°C | 47.08 | 50.54 | 53.85 | ms |
| | | At temperature -40 +85°C (Note 3) | 42.7 | 50.54 | 58.97 | ms |
| $T_{DLY6}$ | Delay6 Time | At temperature 25°C | 95.46 | 101.74 | 107.65 | ms |
| | | At temperature -40 +85°C (Note 3) | 86.58 | 101.74 | 117.88 | ms |
| $T_{CNT0}$ | Counter0 Period | At temperature 25°C | 0.92 | 1 | 1.06 | s |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | At temperature -40 +85°C (Note 3) | 0.84 | 1 | 1.16 | s |
| $V_{ACMP2}$ | Analog Comparator2 Threshold Voltage | Low to High transition, at temperature 25°C | 588 | -- | 612 | mV |
| | | Low to High transition, at temperature -40 +85°C (Note 3) | 587 | -- | 612 | mV |
| | | High to Low transition, at temperature 25°C | 390 | -- | 411 | mV |
| | | High to Low transition, at temperature -40 +85°C (Note 3) | 389 | -- | 411 | mV |
| $V_{HYST}$ | Analog Comparator Hysteresis Voltage (Note 3) | ACMP 2 at temperature 25°C | -- | 200 | -- | mV |
| | | ACMP 2 at temperature -40 +85°C | -- | 200 | -- | mV |
| $T_{SU}$ | Startup Time | From VDD rising past $PON_{THR}$ | 0.67 | 1.38 | 2.03 | ms |
| $PON_{THR}$ | Power On Threshold | $V_{DD}$ Level Required to Start Up the Chip | 1.39 | 1.55 | 1.68 | V |
| $POFF_{THR}$ | Power Off Threshold | $V_{DD}$ Level Required to Switch Off the Chip | 1.01 | 1.17 | 1.35 | V |

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. PINs 1, 2, 3, 4, 5, 6, 7, 8, and 19 are connected to one side, PINs 11, 12, 13, 14, 15, 17, 18, 21 and 22 to another.
3. Guaranteed by Design.

## I²C Specifications

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{SCL}$ | Clock Frequency, SCL | $V_{DD}$ = (1.71...5.5) V | -- | -- | 400 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | $V_{DD}$ = (1.71...5.5) V | 1300 | -- | -- | ns |
| $t_{HIGH}$ | Clock Pulse Width High | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_I$ | Input Filter Spike Suppression (SCL, SDA) | $V_{DD}$ = 1.8V ± 5% | -- | -- | 30.0 | ns |
| | | $V_{DD}$ = 3.3V ± 10% | -- | -- | 60.1 | ns |
| | | $V_{DD}$ = 5.0V ± 10% | -- | -- | 85.4 | ns |
| $t_{AA}$ | Clock Low to Data Out Valid | $V_{DD}$ = (1.71...5.5) V | -- | -- | 900 | ns |
| $t_{BUF}$ | Bus Free Time between Stop and Start | $V_{DD}$ = (1.71...5.5) V | 1300 | -- | -- | ns |
| $t_{HD\_STA}$ | Start Hold Time | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_{SU\_STA}$ | Start Set-up Time | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_{HD\_DAT}$ | Data Hold Time | $V_{DD}$ = (1.71...5.5) V | 0 | -- | -- | ns |
| $t_{SU\_DAT}$ | Data Set-up Time | $V_{DD}$ = (1.71...5.5) V | 100 | -- | -- | ns |
| $t_R$ | Inputs Rise Time | $V_{DD}$ = (1.71...5.5) V | -- | -- | 300 | ns |
| $t_F$ | Inputs Fall Time | $V_{DD}$ = (1.71...5.5) V | -- | -- | 300 | ns |
| $t_{SU\_STO}$ | Stop Set-up Time | $V_{DD}$ = (1.71...5.5) V | 600 | -- | -- | ns |
| $t_{DH}$ | Data Out Hold Time | $V_{DD}$ = (1.71...5.5) V | 50 | -- | -- | ns |

## Chip address

| HEX | BIN | DEC |
|---|---|---|
| 0x38 | 0111000 | 56 |

## I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1867:1864>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

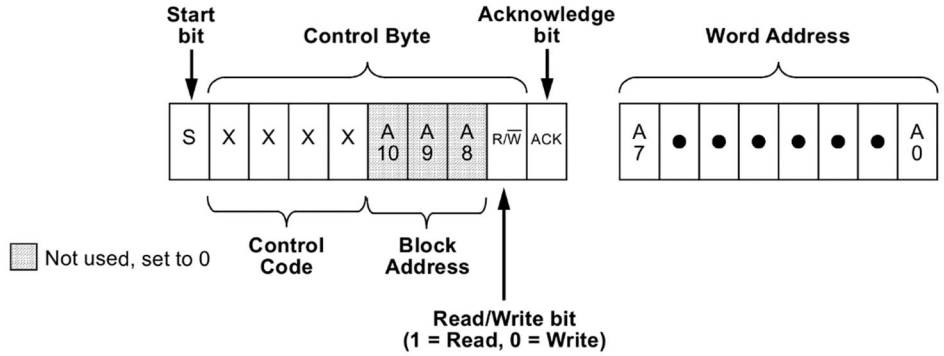



Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

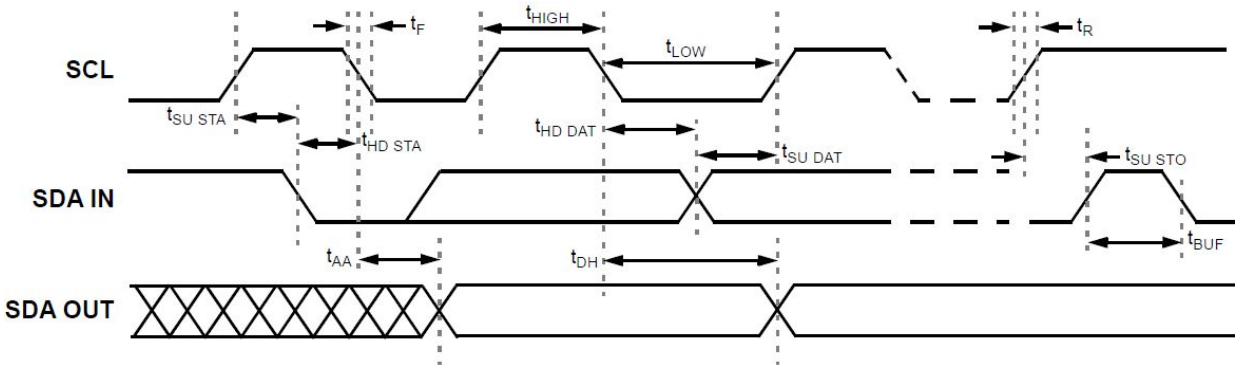



Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN46131 to the correct data byte to be written. After the SLG7RN46131 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN46131 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN46131 generates the Acknowledge bit.

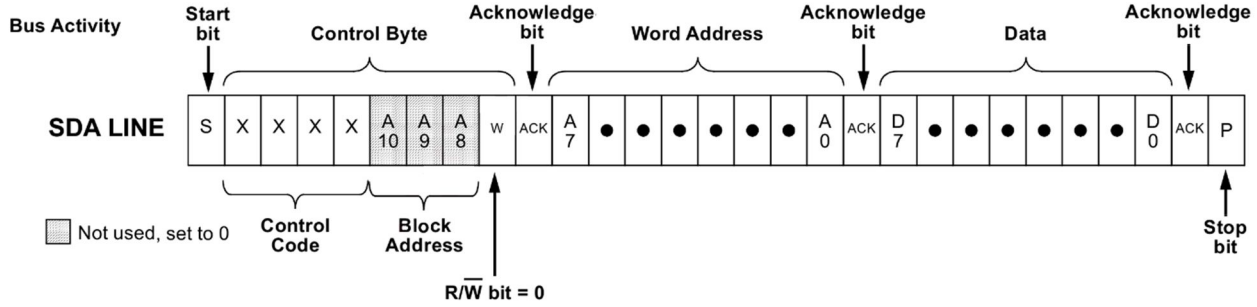



Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7RN46131 issues an Acknowledge bit, followed by the requested eight data bits.

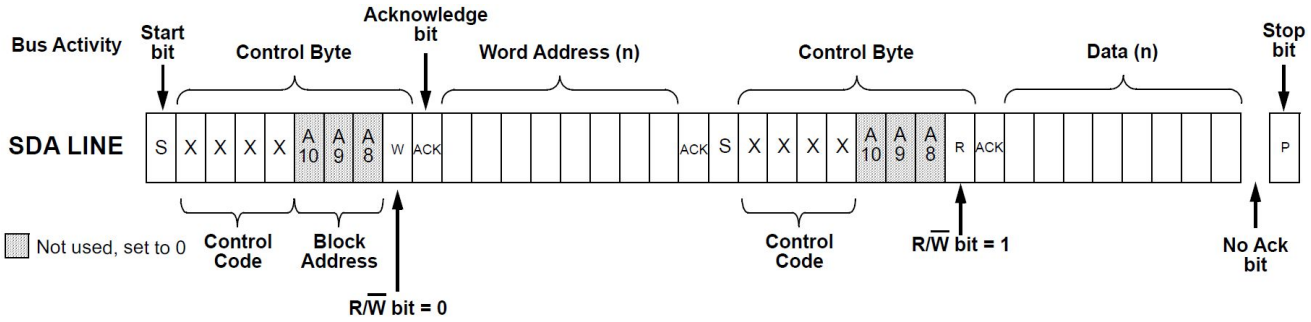


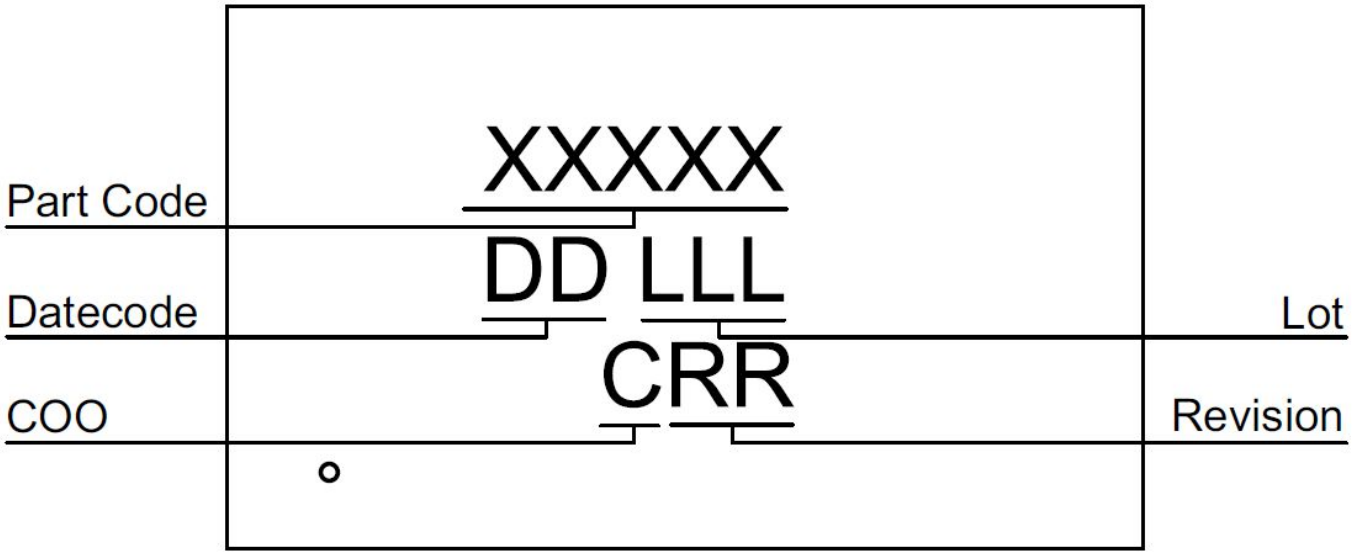

Figure4. I2C Random Read Command

4. I2C register control data

| Address Byte | Register Bit | Block | Function |
|---|---|---|---|
| 0xF4 | reg<1952> | Virtual Input <0> | Control SLEEP_EN signal Default is 0 |
| | reg<1953> | Virtual Input <1> | Control PWRBTN_SEL signal Default is 0 |
| | reg<1954> | Virtual Input <2> | Control TIMER_START signal Default is 0 |
| | reg<1955> | Virtual Input <3> | Control PWRBTN_INT_EN_CLR# signal Default is 0 |
| | reg<1956> | Virtual Input <4> | Control SLPBTN_INT_EN_CLR# signal Default is 0 |
| | reg<1957> | Virtual Input <5> | Control PG_INT_EN_CLR# signal Default is 0 |
| | reg<1958> | Virtual Input <6> | Control RSV_INT_EN_CLR# signal Default is 0 |
| | reg<1959> | Virtual Input <7> | Control TO_INT_EN_CLR# signal Default is 0 |
| 0xB6 | reg<1458> | Filter_1 output polarity | Control Filter_1 polarity Default is 0 |

| | | | |
|---|---|---|---|
| 0xB6 | reg<1462> | Filter_0 output polarity | Control Filter_0 polarity Default is 0 |

## Package Top Marking




XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|---|---|---|---|---|---|---|
| 0.11 | 001 | U | 0x3B0562DD | 46131 | AA | 11/11/2022 |

Lock coverage for this part is indicated by √, from one of the following options:

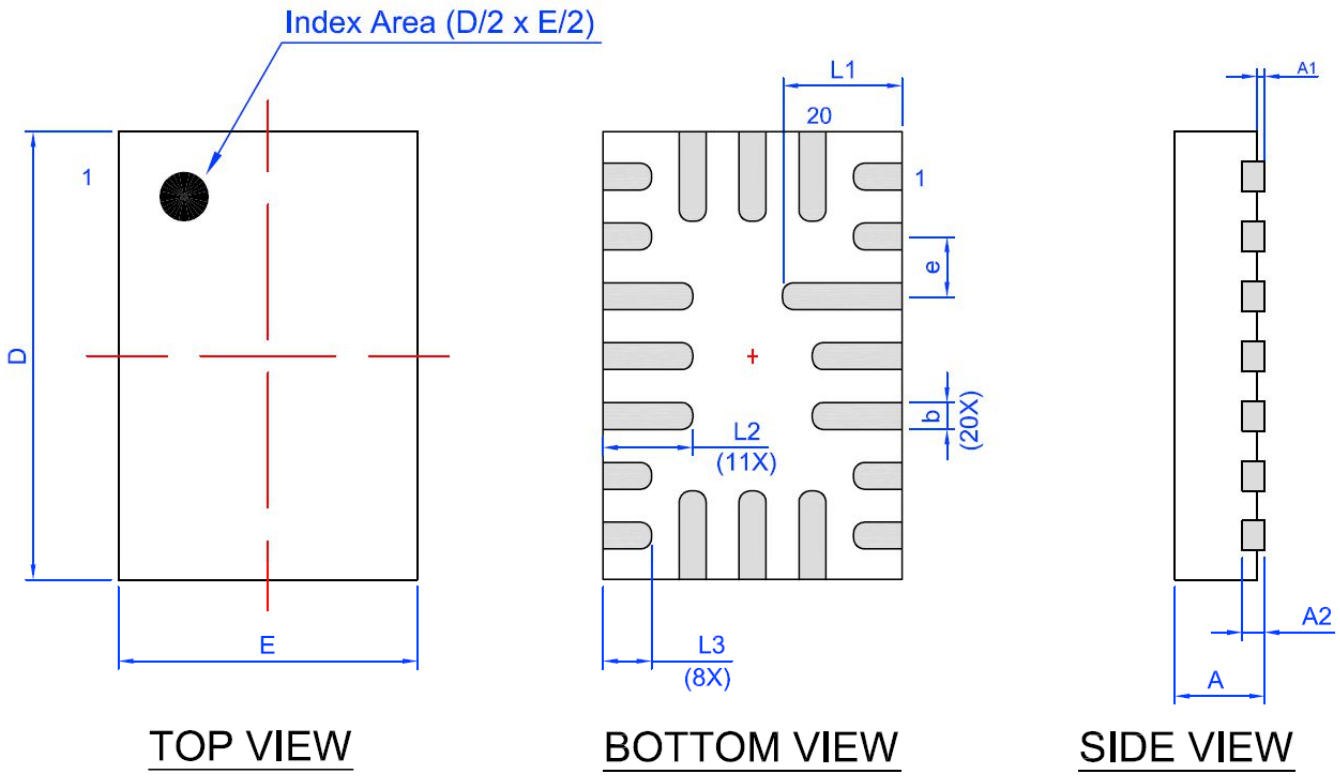
| | |
|---|---|
| √ | Unlocked |
| | Locked for read, bits <1535:0> |
| | Locked for write, bits <1535:0> |
| | Locked for write all bits |
| | Locked for read and write bits <1535:0> |
| | Locked for read bits <1535:0> and write of all bits |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

## Package Drawing and Dimensions

**STQFN 20L 2x3mm 0.4P COL Package**

**JEDEC MO-220**




Unit: mm

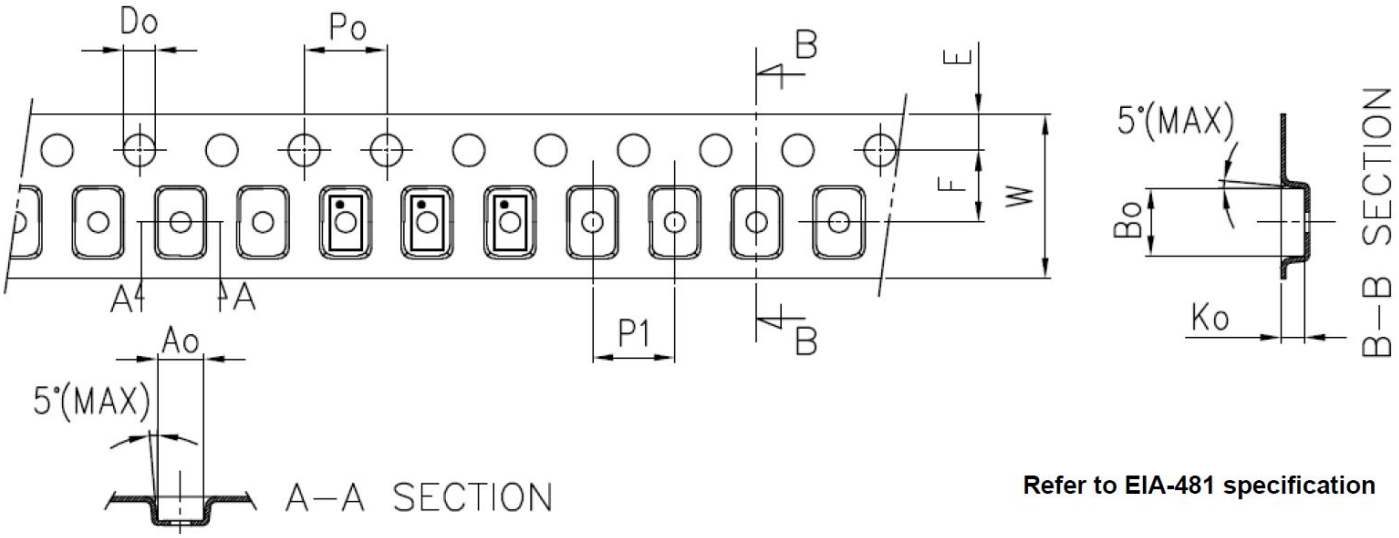
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|---|---|---|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.050 | E | 1.95 | 2.00 | 2.05 |
| A2 | 0.10 | 0.15 | 0.20 | L1 | 0.75 | 0.80 | 0.85 |
| b | 0.13 | 0.18 | 0.23 | L2 | 0.55 | 0.60 | 0.65 |
| e | 0.40 BSC | | | L3 | 0.275 | 0.325 | 0.375 |

## Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 20L 2x3 mm 0.4P COL | 20 | 2x3x0.55 | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

## Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 20L 2x3 mm 0.4P COL | 2.2 | 3.15 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |




**Refer to EIA-481 specification**

## Recommended Reflow Soldering Profile

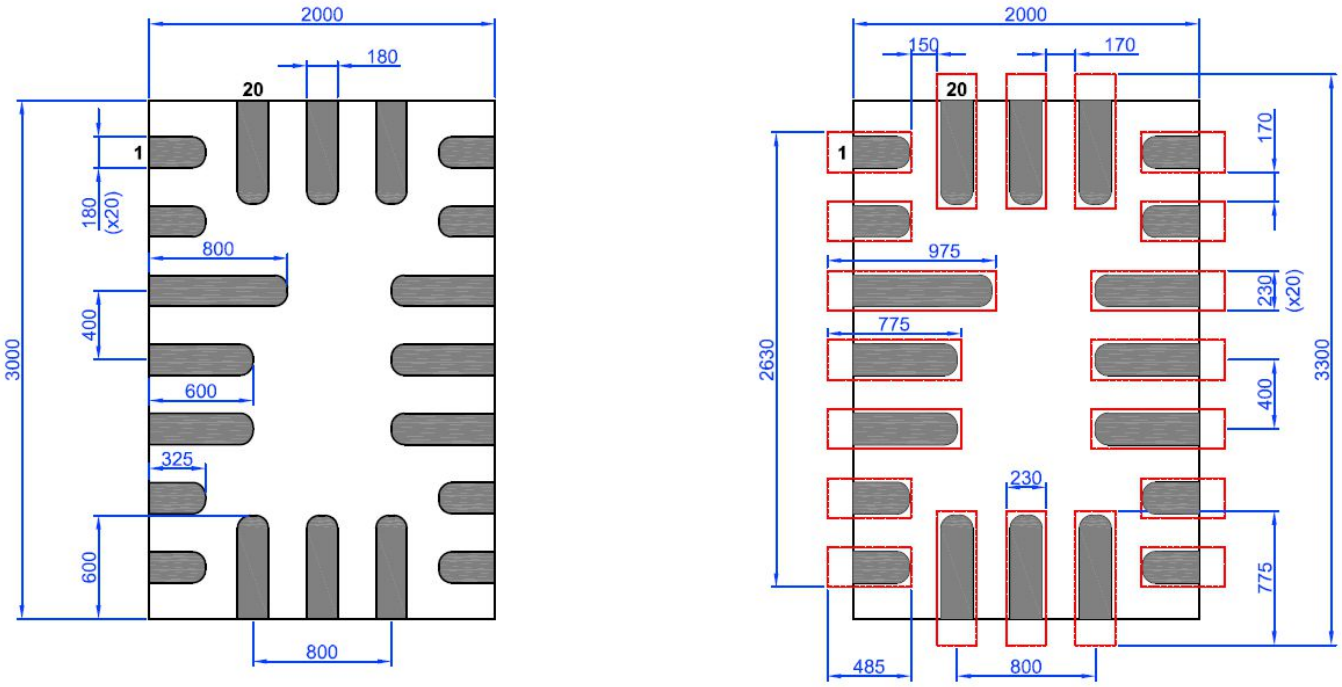
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 $mm^3$ (nominal). More information can be found at www.jedec.org.

## Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

**Units: µm**



## Datasheet Revision History

| Date | Version | Change |
|---|---|---|
| 11/07/2022 | 0.10 | New design for SLG46533V chip |
| 11/11/2022 | 0.11 | Updated Device Revision Table |

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