SLG7RN45560

GreenPAK ™

I/O Expander

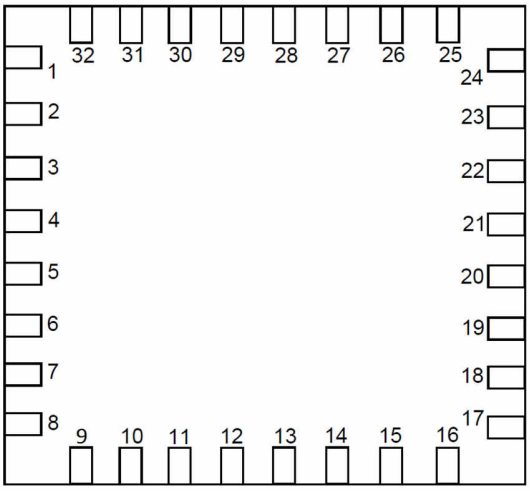
General Description

Renesas SLG7RN45560 is a low power and small form device. The SoC is housed in a 4mm x 4mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 32 Package

Pin Configuration



STQFN-32 (Top view)

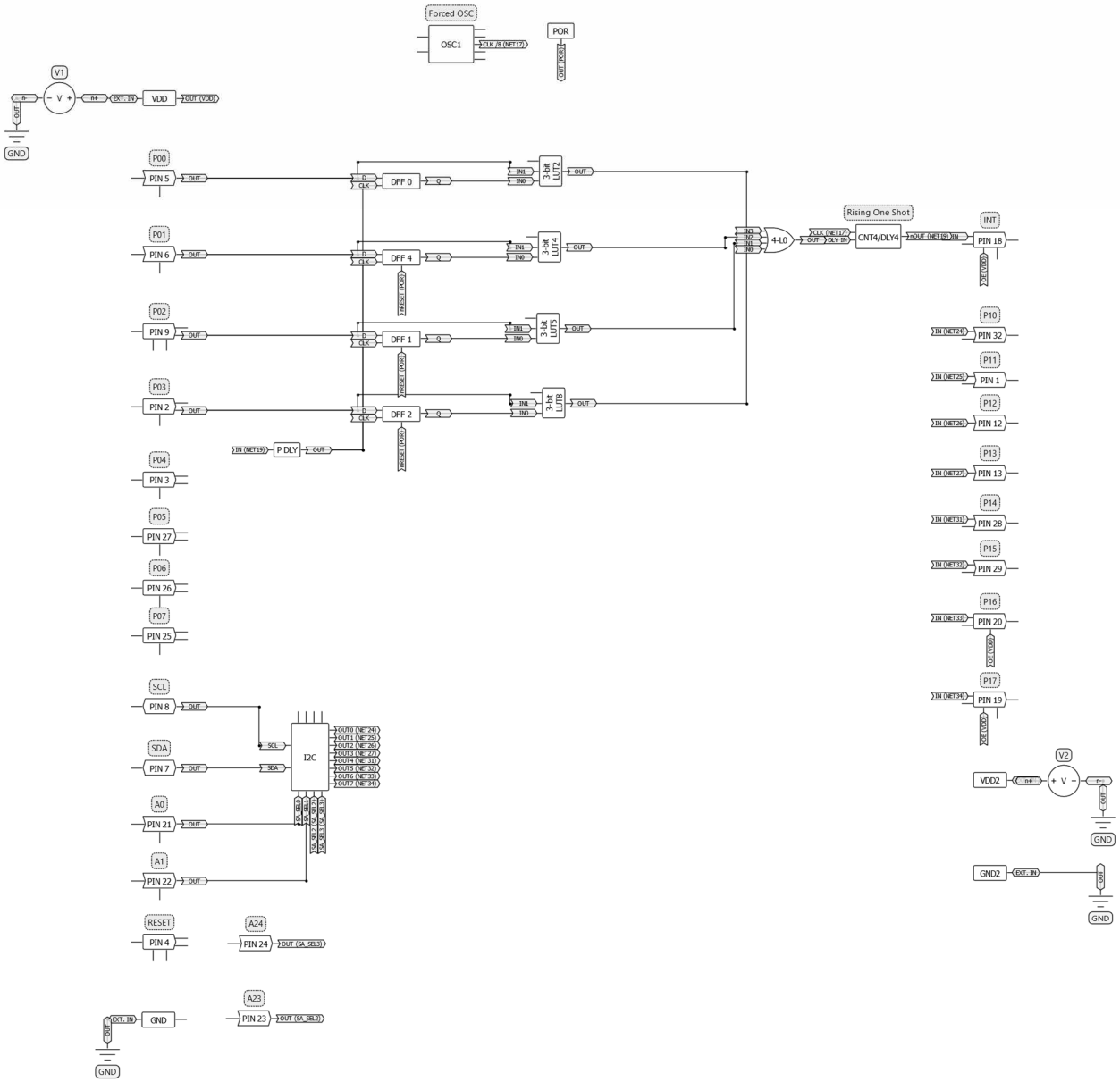
Output Summary

1 Output - Open Drain NMOS 1X
8 Outputs - Push Pull 1X

Pin name

Pin #	Pin name	Pin #	Pin name
1	P11	17	NC
2	P03	18	INT
3	P04	19	P17
4	RESET	20	P16
5	P00	21	A0
6	P01	22	A1
7	SDA	23	A23
8	SCL	24	A24
9	P02	25	P07
10	NC	26	P06
11	NC	27	P05
12	P12	28	P14
13	P13	29	P15
14	GND	30	GND
15	VDD2	31	VDD
16	NC	32	P10

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	P11	Digital Output	Push Pull 1X	floating
2	P03	Digital Input	Digital Input without Schmitt trigger	floating
3	P04	Digital Input	Digital Input without Schmitt trigger	floating
4	RESET	Digital Input	Digital Input without Schmitt trigger	floating
5	P00	Digital Input	Digital Input without Schmitt trigger	floating
6	P01	Digital Input	Digital Input without Schmitt trigger	floating
7	SDA	Digital Input	Digital Input without Schmitt trigger	floating
8	SCL	Digital Input	Digital Input without Schmitt trigger	floating
9	P02	Digital Input	Digital Input without Schmitt trigger	floating
10	NC	--	Keep Floating or Connect to GND	--
11	NC	--	Keep Floating or Connect to GND	--
12	P12	Digital Output	Push Pull 1X	floating
13	P13	Digital Output	Push Pull 1X	floating
14	GND	GND	Ground	--
15	VDD2	PWR	Supply Voltage	--
16	NC	--	Keep Floating or Connect to GND	--
17	NC	--	Keep Floating or Connect to GND	--
18	INT	Digital Output	Open Drain NMOS 1X	floating
19	P17	Digital Output	Push Pull 1X	floating
20	P16	Digital Output	Push Pull 1X	floating
21	A0	Digital Input	Digital Input without Schmitt trigger	floating
22	A1	Digital Input	Digital Input without Schmitt trigger	floating
23	A23	Digital Input	Digital Input without Schmitt trigger	floating
24	A24	Digital Input	Digital Input without Schmitt trigger	floating
25	P07	Digital Input	Digital Input without Schmitt trigger	floating
26	P06	Digital Input	Digital Input without Schmitt trigger	floating
27	P05	Digital Input	Digital Input without Schmitt trigger	floating
28	P14	Digital Output	Push Pull 1X	floating
29	P15	Digital Output	Push Pull 1X	floating
30	GND	GND	Ground	--
31	VDD	PWR	Supply Voltage	--
32	P10	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN45560V	32-pin STQFN - Tape and Reel (5k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	GND-0.5V	VDD+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
Current at Input Pin	-1.0	1.0	mA
Input leakage Current (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD} (Note 4)	Supply Voltage		2.4	3.3	5	V
V_{DD2} (Note 4)	Supply Voltage		2.3	3.3	5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		0.1	--	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PINs7, 8 are HIGH, PINs2, 3, 4, 5, 6, 9,21,22,23,24,25,26,27 are LOW	--	32	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3 (Note 1)	V
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 2)	0.7xVDD (Note 1)	--	VDD+0.3 (Note 1)	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 2)	GND-0.3	--	0.3xVDD (Note 1)	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=100µA at VDD=2.5V (Note 1)	2.286	2.292	--	V
		Push-Pull 1X, I_{OH}=3mA at VDD=3.3V (Note 1)	2.704	2.790	--	V
		Push-Pull 1X, I_{OH}=5mA at VDD=5.0V (Note 1)	4.154	4.247	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=100µA, at VDD=2.5V (Note 1)	--	0.006	0.025	V
		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V (Note 1)	--	0.158	0.217	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V (Note 1)	--	0.212	0.297	V
		Open Drain NMOS 1X, I_{OL}=100µA, at VDD=2.5V (Note 1)	--	0.003	0.011	V

		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V (Note 1)	--	0.063	0.087	V
		Open Drain NMOS 1X, I_{OL}=5mA, at VDD=5.0V (Note 1)	--	0.079	0.114	V
I_{OH}	HIGH-Level Output Current (Note 3)	Push-Pull 1X, VOH=VDD-0.2V at VDD=2.5V (Note 1)	1.55	2.14	--	mA
		Push-Pull 1X, VOH=2.4V at VDD=3.3V (Note 1)	5.54	7.48	--	mA
		Push-Pull 1X, VOH=2.4V at VDD=5.0V (Note 1)	19.89	24.83	--	mA
I_{OL}	LOW-Level Output Current (Note 3)	Push-Pull 1X, V_{OL}=0.15V, at VDD=2.5V (Note 1)	1.66	2.19	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V (Note 1)	5.26	7.00	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V (Note 1)	7.15	9.76	--	mA
		Open Drain NMOS 1X, V_{OL}=0.15V, at VDD=2.5V (Note 1)	4.15	5.38	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V (Note 1)	12.90	17.14	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=5.0V (Note 1)	16.98	23.70	--	mA
T_{DLY4}	Delay4 Time	At temperature 25°C	0.98	1.00	1.02	ms
		At temperature -40 +85°C (Note 4)	0.97	1.00	1.04	ms
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.13	1.72	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.64	1.84	2.11	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.98	1.25	1.49	V

Note 1 GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7 are powered from V_{DD} and GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4 are powered from V_{DD2}.
Note 2 No hysteresis.
Note 3 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 4 Guaranteed by Design.

I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (2.3...5.5) V	--	--	1000	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (2.3...5.5) V	500	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (2.3...5.5) V	260	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.5V ± 8%	--	--	168	ns
		V_{DD} = 3.3V ± 10%	--	--	157	ns
		V_{DD} = 5.0V ± 10%	--	--	156	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (2.3...5.5) V	--	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (2.3...5.5) V	500	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (2.3...5.5) V	260	--	--	ns

t_{SU_STA}	Start Set-up Time	V_{DD} = (2.3...5.5) V	260	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (2.3...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (2.3...5.5) V	50	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (2.3...5.5) V	--	--	120	ns
t_F	Inputs Fall Time	V_{DD} = (2.3...5.5) V	--	--	120	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (2.3...5.5) V	260	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (2.3...5.5) V	170.70	--	--	ns
Note 1 Timing diagram can be found in the Figure 2.						

Chip address

HEX	BIN	DEC
0x08	0001000	8

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<4083:4080>. The address source is selected by reg<4087>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read ("1") or written ("0") by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

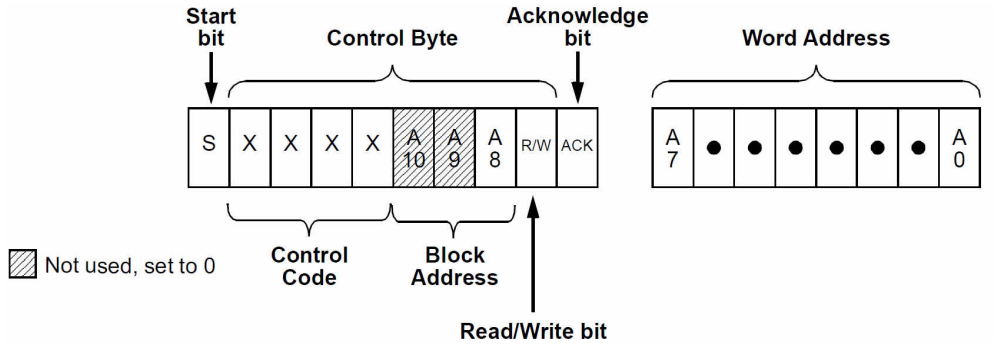


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

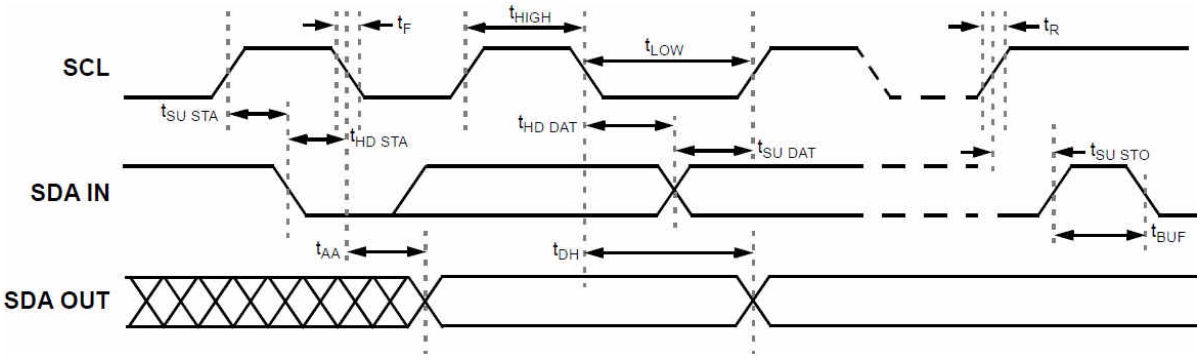


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN45560 to the correct data byte to be written. After the SLG7RN45560 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN45560 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN45560generates the Acknowledge bit.

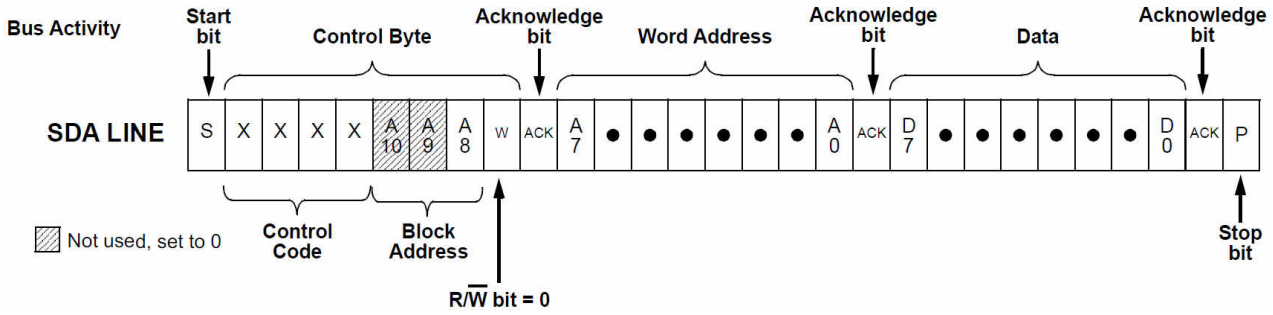


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7RN45560 issues an Acknowledge bit, followed by the requested eight data bits.

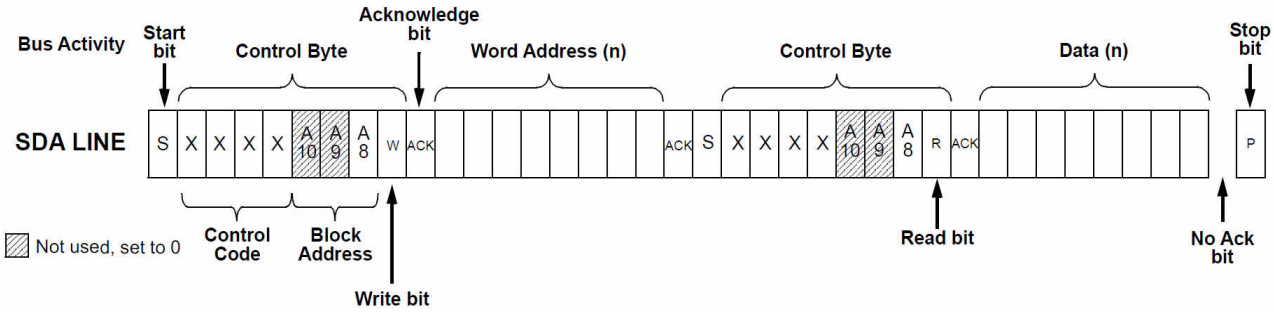


Figure4. I2C Random Read Command

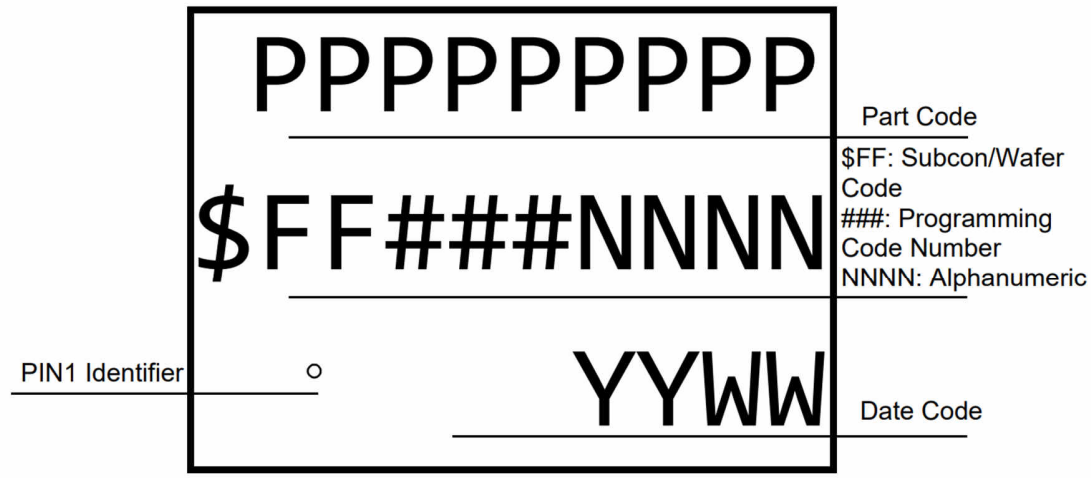
4. I2C register control data

Address Byte	Register Bit	Block	Function
0x1DB	reg<3800:3807>	Virtual Input <1>	Enable (OUT0….OUT7 = 1).

5. I2C Commands:

1. [start] [0x08] [w] [0x1DB] [0xFF] [stop] // enable (OUT0….OUT7 = 1).

Package Top Marking



Note: For this package type, Revision code is not marked on the part but may be present on labels and other materials. Instead, Wafer Code and Programming Code Number are marked on the part.

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	001	U	0x487AC902			07/12/2023

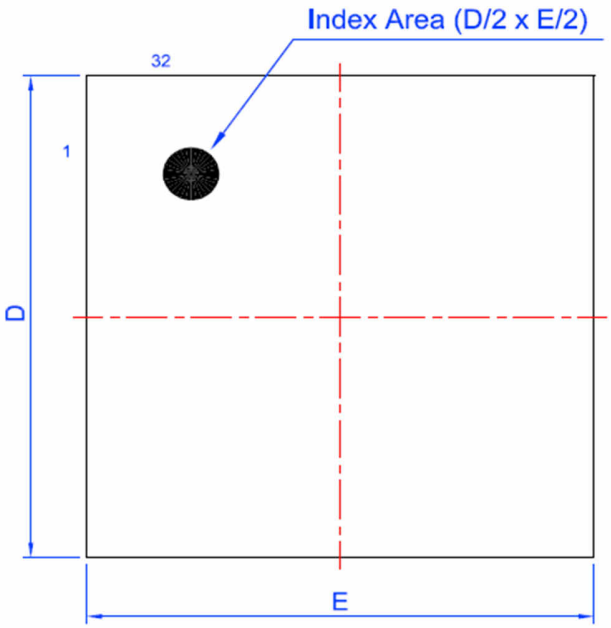
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

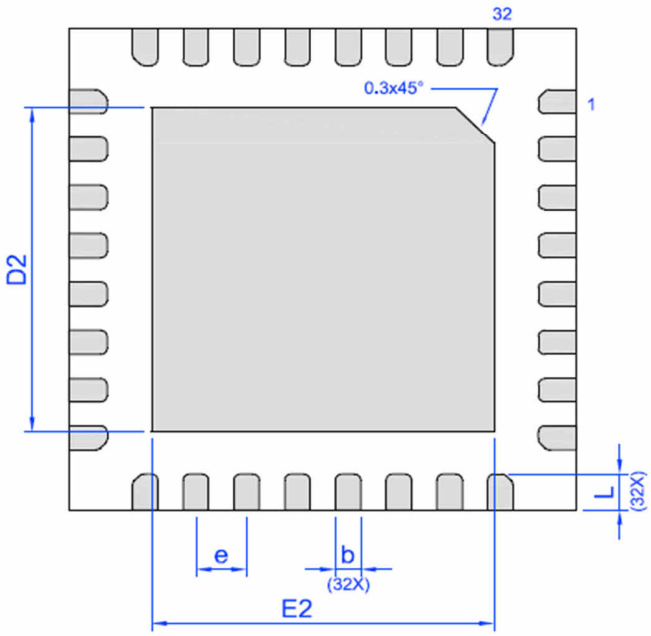
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

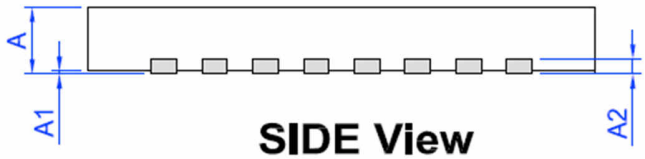
STQFN 32L 4x4mm 0.4P Package
IC Net Weight: 0.028 g



Marking View



BTM View



SIDE View

Unit: mm

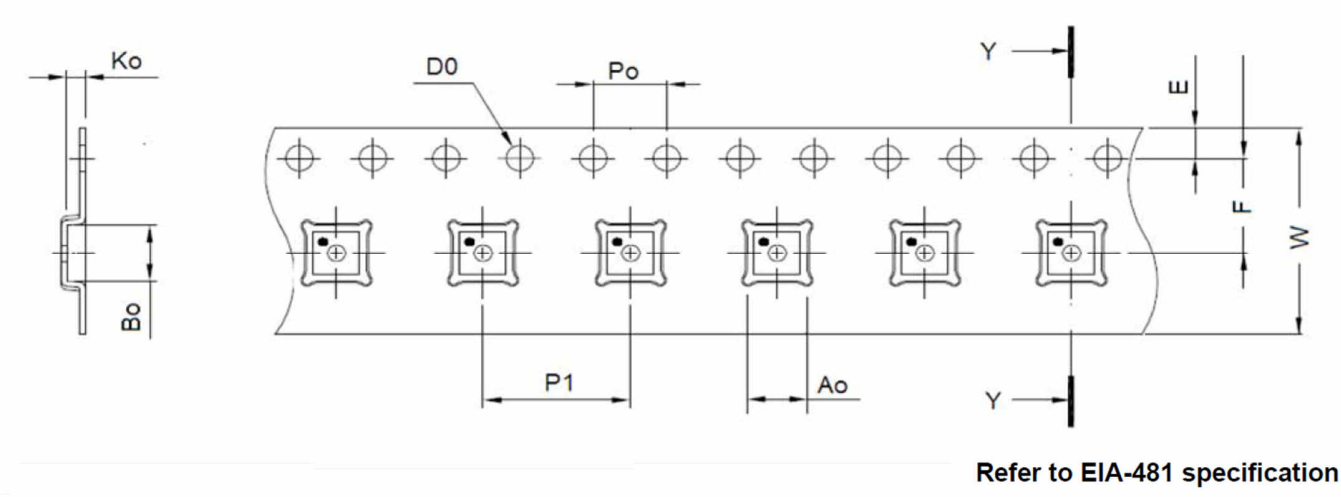
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	3.950	4.000	4.050
A1	0.00	-	0.050	E	3.950	4.000	4.050
A2	0.150 REF			D2	2.650	2.700	2.750
b	0.150	0.200	0.250	E2	2.650	0.270	2.750
e	0.400 BSC			L	0.250	0.300	0.350

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 32L 4x4 mm 0.4P Green	32	4 x 4 x 0.55	5000	10000	330/100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 32L 4x4 mm 0.4P Green	4.25	4.25	0.75	4	8	1.5	1.75	5.5	12

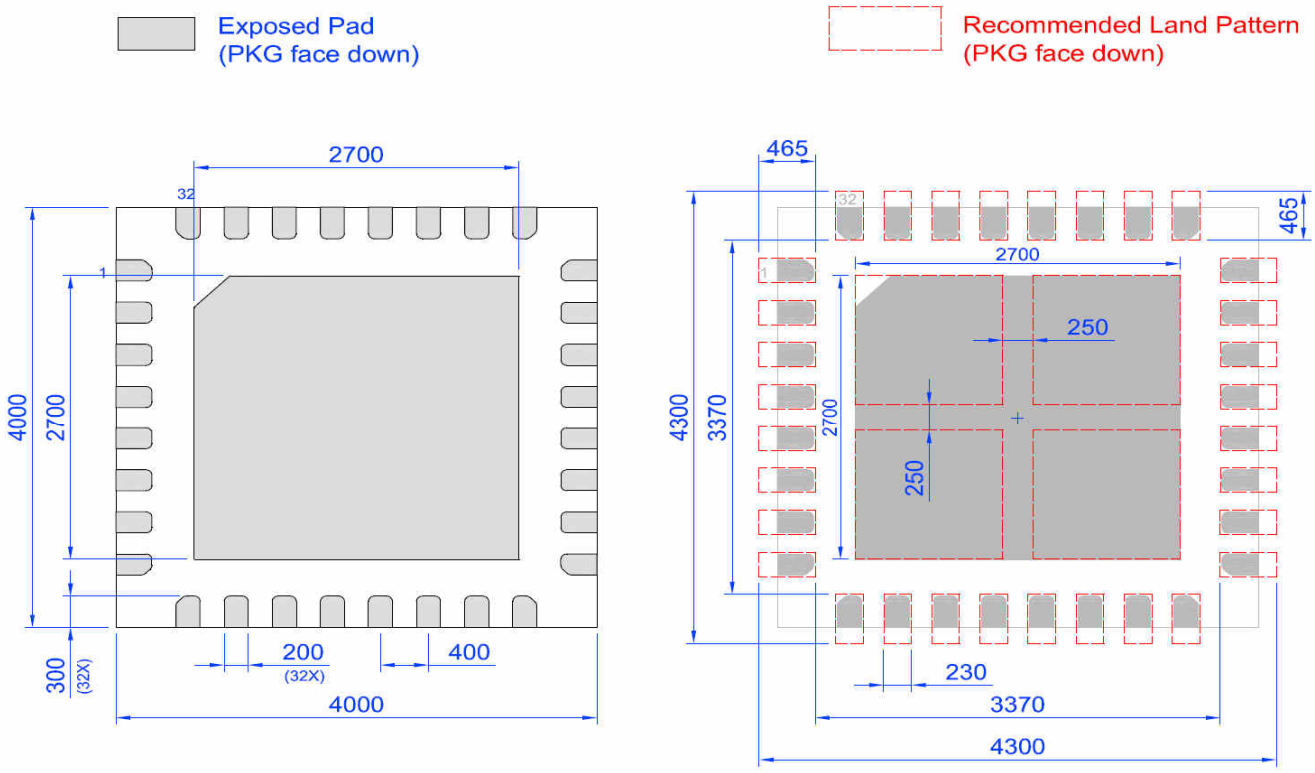


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

Layout Guidelines



Units: µm

Datasheet Revision History

Date	Version	Change
01/27/2022	0.10	New design
07/12/2023	0.11	Moved to Renesas template

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.