# SLG7MD47668

PWM Low Voltage H-Bridge Driver

The SLG7MD47668 offers a compact and efficient integrated solution for low-voltage and battery-powered motor control applications, making it ideal for small devices where space and power efficiency are essential.

Driver FETs and FET control circuitry are integrated into the SLG7MD47668 and therefore help to reduce the component count in motor driver systems. The device features a PWM interface (IN1 and IN2) for precise control of outputs, along with a low power sleep mode that can be activated using the nSLEEP pin, significantly reducing power consumption when the device is not in use.

Additionally, the SLG7MD47668 includes crucial protection features such as undervoltage lockout, overcurrent protection, and thermal shutdown.

**This is a pre-configured device. The configuration of this device can be modified to meet specific requirements at no additional NRE costs. Other functions and features may also be added. For more information on custom configurations, visit the [GreenPAK website](#).**

**Click [here](#) to download the GreenPAK file for the SLG7MD47668 design.**

**Email [GreenPAKSupport@renesas.com](#) for more information and GreenPAK design support.**

## Features

- Four high voltage high current drive GPOs
- Current up to 1.5 A RMS per GPO/H-Bridge
- Low power consumption
- Pb-free/RoHS compliant
- Halogen-free
- STQFN-20 package

## Applications

- Cameras
- DSLR lenses
- Toys
- Robotics
- Medical devices
- Motor control

## Output Summary

- High Voltage High Current Drive GPO

# Contents

# Figures
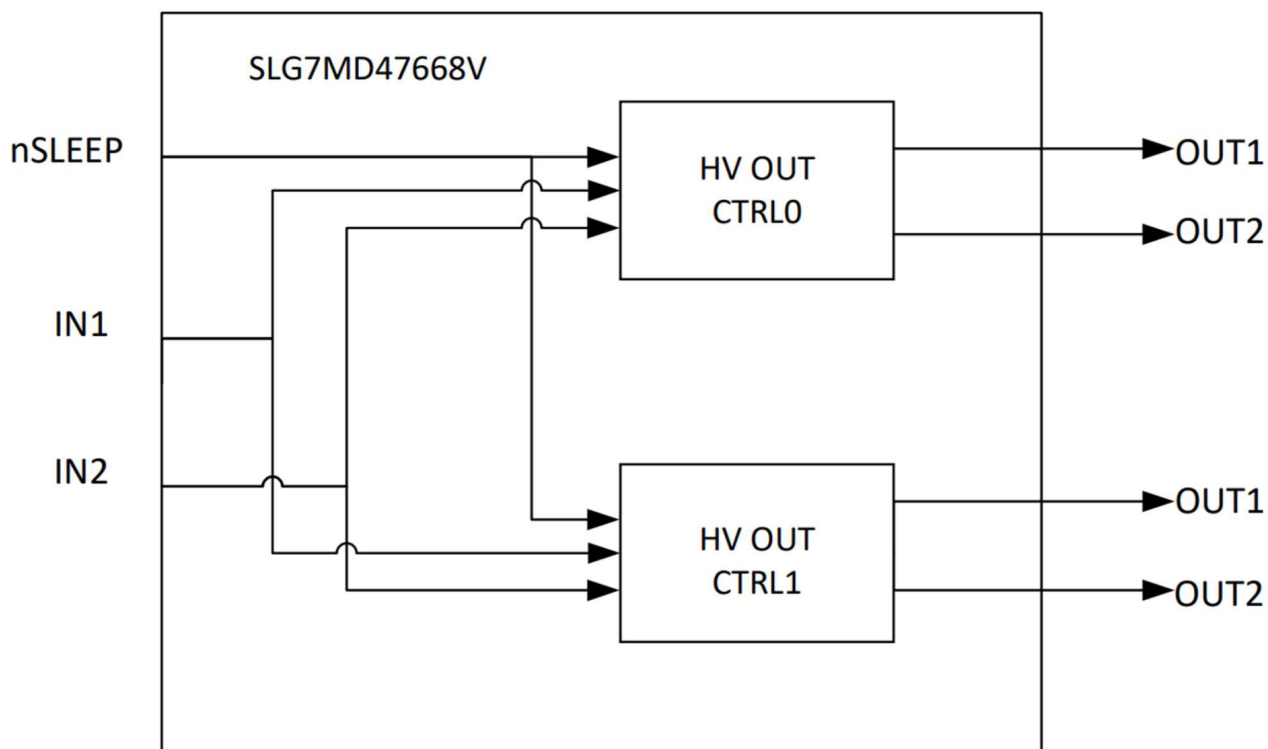
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# 1. Block Diagram
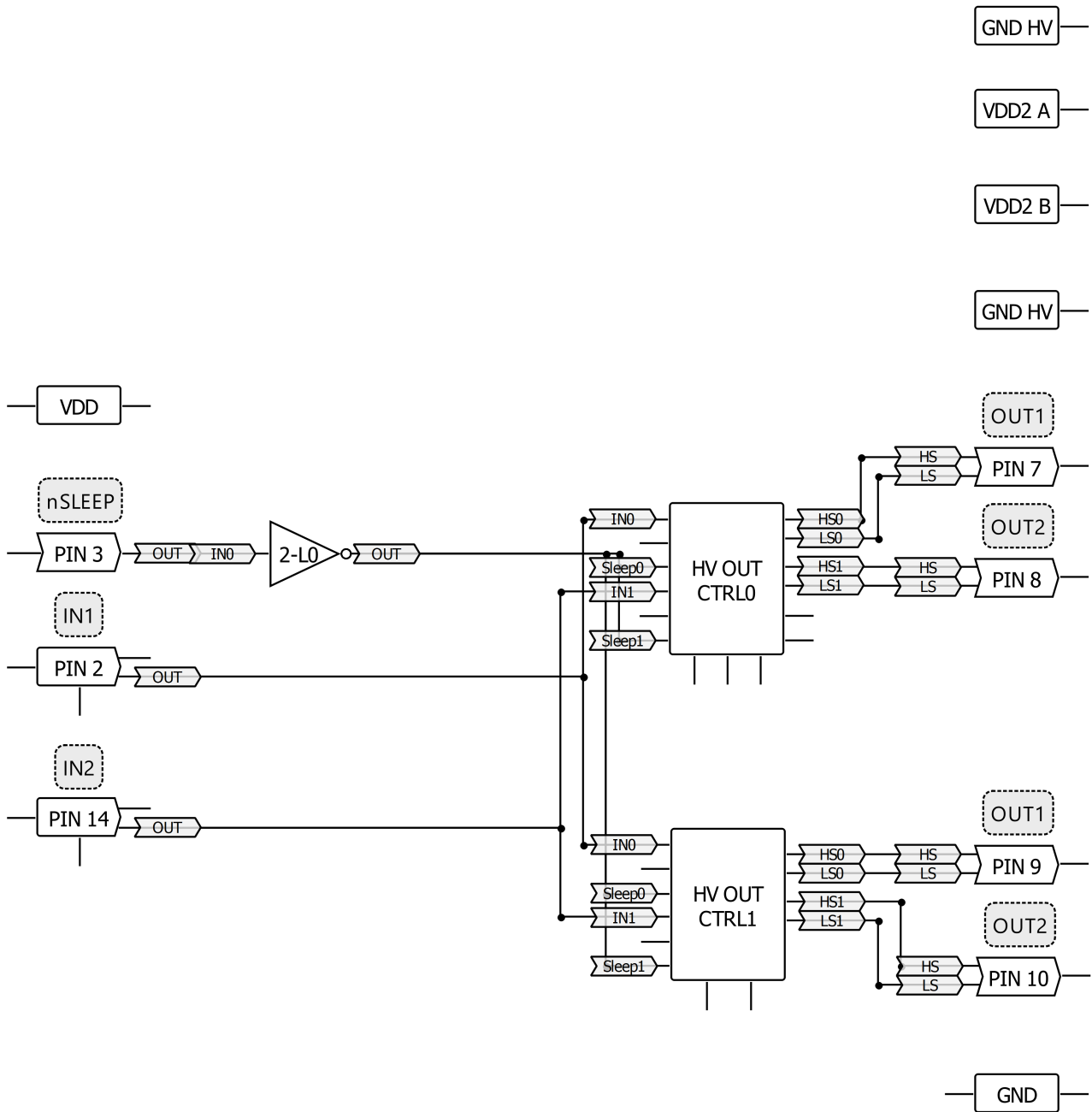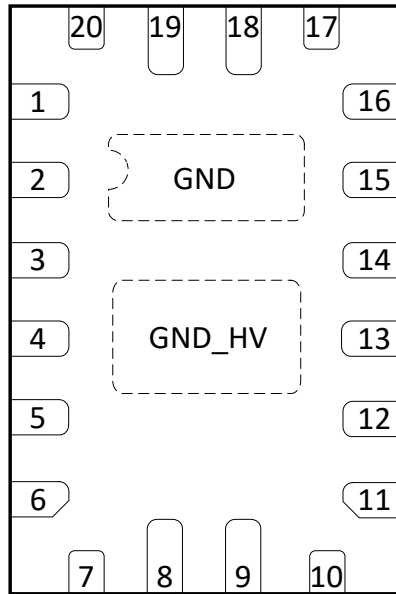


**Figure 1. Functional Diagram**

**Figure 2. Block Diagram**

# 2. Pin Information

## 2.1 Pin Assignments



**STQFN-20L**
**(Top View)**

Figure 3. Pin Assignments – Top View

## 2.2 Pin Descriptions

| Pin # | Pin Name | Type | Description | Internal Resistor |
|-------|----------|------|-------------|-------------------|
| 1 | $V_{DD}$ | PWR | Supply Voltage | -- |
| 2 | IN1 | Digital Input | Digital Input without Schmitt Trigger | 1 MΩ Pull-Down |
| 3 | nSLEEP | Digital Input | Digital Input without Schmitt Trigger | 1 MΩ Pull-Down |
| 4 | GND_HV | GND | Ground | -- |
| 5 | NC | Analog Input/Output | Analog Input/Output | Floating |
| 6 | $V_{DD2\_A}$ | PWR | Supply Voltage | -- |
| 7 | OUT1 | High Drive Output | High Drive Push-Pull | Floating |
| 8 | OUT2 | High Drive Output | High Drive Push-Pull | Floating |
| 9 | OUT1 | High Drive Output | High Drive Push-Pull | Floating |
| 10 | OUT2 | High Drive Output | High Drive Push-Pull | Floating |
| 11 | $V_{DD2\_B}$ | PWR | Supply Voltage | -- |
| 12 | NC | Analog Input/Output | Analog Input/Output | Floating |
| 13 | GND_HV | GND | Ground | -- |

| Pin # | Pin Name | Type | Description | Internal Resistor |
|-------|----------|------|-------------|-------------------|
| 14 | IN2 | Digital Input | Digital Input without Schmitt Trigger | 1 MΩ Pull-Down |
| 15 | NC | -- | Keep Floating or Connect to GND | -- |
| 16 | NC | -- | Keep Floating or Connect to GND | -- |
| 17 | NC | -- | Keep Floating or Connect to GND | -- |
| 18 | GND | GND | Ground | -- |
| 19 | NC | -- | Keep Floating or Connect to GND | -- |
| 20 | NC | -- | Keep Floating or Connect to GND | -- |

# 3. Specifications

## 3.1 Absolute Maximum Ratings

| Parameter | | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage on $V_{DD}$ relative to GND | | | -0.3 | 7.0 | V |
| Supply Voltage on $V_{DD2}$ relative to GND | | | -0.3 | 18 | V |
| DC Input Voltage | | | GND - 0.5 | $V_{DD}$ + 0.5 | V |
| Maximum $V_{DD}$ Average or DC Current | | (Through $V_{DD}$ or GND Pin) for $V_{DD}$ Group | -- | 120 | mA |
| Maximum $V_{DD2}$ Average or DC Current | | Through each $V_{DD2\_A}$, $V_{DD2\_B}$, SENSE_A or SENSE_B Pin | -- | 2000 | mA |
| Maximum Average or DC Current ($V_{DD2}$ Power Supply) | Push-Pull/ Half Bridge | Through $V_{DD2}$ High Current Group Pins | -- | 1500 | mA |
| Maximum Pulsed Current Sink/Sourced per HV HD Pin | | Pulse Width < 0.5 ms; Duty Cycle < 2 % | -- | Internally limited by OCP | mA |
| Current at Input Pin | | Through $V_{DD}$ Group Pin | -0.1 | 1.0 | mA |
| Input Leakage Current (Absolute Value) | | | -- | 1000 | nA |
| Storage Temperature Range | | | -65 | 150 | °C |
| Junction Temperature | | | -- | 150 | °C |
| ESD Protection (Human Body Model) | | | 4000 | -- | V |
| ESD Protection (Charged Device Model) | | | 1300 | -- | V |
| Moisture Sensitivity Level | | | 1 | | |

## 3.2 Thermal Information

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\Theta_{JA}$ | 4L JEDEC PCB | -- | -- | 65 | °C/W |
| | | 4L JEDEC PCB with a thermal vias that connect thermal pad through all layers of the PCB | -- | -- | 46 | °C/W |
| Junction-to-case (top) Thermal Resistance | $\Theta_{JC(top)}$ | | -- | 23.50 | -- | °C/W |
| Junction-to-board Thermal Resistance | $\Theta_{JB}$ | | -- | 25.51 | -- | °C/W |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Junction-to-case (top) Characterization Parameter | $\Psi_{JC(top)}$ | | -- | 6.80 | -- | °C/W |
| Junction-to-board Characterization Parameter | $\Psi_{JB}$ | | -- | 24.44 | -- | °C/W |

## 3.3   Electrical Specifications

| Parameter | Symbol | Condition/Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.3 | 3.3 | 5.5 | V |
| Supply Voltage | $V_{DD\_A}$ | | 3 | 12 | 13.2 | V |
| Supply Voltage | $V_{DD\_B}$ | | 3 | 12 | 13.2 | V |
| Operating Temperature | $T_A$ | | -40 | 25 | 85 | °C |
| Capacitor Value at $V_{DD}$ | $C_{VDD}$ | | 0.1 | -- | -- | µF |
| Input Capacitance | $C_{IN}$ | | -- | 4 | -- | pF |
| Quiescent Current $V_{DD}$ Side | $I_{Q\_VDD}$ | Static inputs and floating outputs | -- | 1 | -- | µA |
| Quiescent Current $V_{DD2\_A}$ Side | $I_{Q\_VDD2\_A}$ | Static inputs and floating outputs | -- | -- | -- | µA |
| Quiescent Current $V_{DD2\_B}$ Side | $I_{Q\_VDD2\_B}$ | Static inputs and floating outputs | -- | -- | -- | µA |
| HIGH-Level Input Voltage [3] | $V_{IH}$ | Logic Input [1] | 0.7 x $V_{DD}$ | -- | $V_{DD}$ + 0.3 | V |
| LOW-Level Input Voltage [3] | $V_{IL}$ | Logic Input [1] | GND - 0.3 | -- | 0.3 x $V_{DD}$ | V |
| HIGH-Level Output Voltage for $V_{DD2}$ High Current Group | $V_{OH2}$ | Push-Pull, $V_{DD}$ = 5 ± 10 %, $I_{OH2}$ = 10 mA | 4.496 | -- | -- | V |
| | | Push-Pull, $V_{DD}$ = 9 V ± 10 %, $I_{OH2}$ = 10 mA | 8.097 | -- | -- | V |
| | | Push-Pull, $V_{DD}$ = 12 V ± 10 %, $I_{OH2}$ = 10 mA | 10.797 | -- | -- | V |
| LOW-Level Output Voltage for $V_{DD2}$ High Current Group | $V_{OL2}$ | Push-Pull, $V_{DD}$ = 5 ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| | | Push-Pull, $V_{DD}$ = 9 V ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| | | Push-Pull, $V_{DD}$ = 12 V ± 10 %, $I_{OL2}$ = 10 mA | -- | -- | 0.004 | V |
| Pull-Down Resistance $T_J$ = -40 °C to 85 °C | $R_{PULL\_DOWN}$ | Pull-down on PINs 2, 3, 14 | -- | 1000 | -- | kΩ |
| Pull-Down Resistance $T_J$ = -40 °C to 150 °C | | Pull-down on PINs 2, 3, 14 | -- | 1000 | -- | kΩ |
| Startup Time | $T_{SU}$ | From $V_{DD}$ rising past $PON_{THR}$ | -- | 1 | 2 | ms |

| Parameter | Symbol | Condition/Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power-On Threshold | PON$_{THR}$ | V$_{DD}$ Level Required to Start Up the Chip | 1.8 | 1.98 | 2.16 | V |
| Power-Off Threshold | POFF$_{THR}$ | V$_{DD}$ Level Required to Switch Off the Chip | 1.33 | 1.55 | 1.83 | V |

**[1]** No hysteresis.
**[2]** DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
**[3]** ESD resistor should be taken into consideration when using pull-up/pull-down resistors. It may affect V$_{IH}$ and V$_{IL}$.
**[4]** Guaranteed by Design.

## 3.4 HV Output Electrical Specifications (Full Bridge or Half Bridge Modes)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rise Time HV OUT | t$_R$ | V$_{DD2}$ = 5 V, 16 Ω to GND, 10 % to 90 % V$_{DD2}$, T$_J$ = -40 °C to 150 °C | 81 | 116 | 156 | ns |
| Fall Time HV OUT | t$_F$ | V$_{DD2}$ = 5 V, 16 Ω to GND, 90 % to 10 % V$_{DD2}$, T$_J$ = -40 °C to 85 °C | 80 | 115 | 198 | ns |
| | | V$_{DD2}$ = 5 V, 16 Ω to GND, 90 % to 10 % V$_{DD2}$, T$_J$ = -40 °C to 150 °C | 80 | 115 | 225 | ns |
| Dead Band Time of HV_GPOx_HD in Pre-driver Mode (not for Driver Mode) (Break before Making for Full Bridge and Half Bridge Modes) | T$_{DEAD}$ | V$_{DD2}$ = 3 V, T$_J$ = -40 °C to 150 °C | -- | 337 | -- | ns |
| | | V$_{DD2}$ = 5 V, T$_J$ = -40 °C to 150 °C | -- | 75 | -- | ns |
| | | V$_{DD2}$ = 13.2 V, T$_J$ = -40 °C to 150 °C | -- | 91 | -- | ns |
| Dead Band Time, Generated by PWM Block | PWM_t$_{DEAD}$ | Configured in PWM block | | 0; 1·Tclk; 2·Tclk; 3·Tclk; | | Clk time |
| HS FET on Resistance (SENSE, GND_HV, and GND Pins are Connected Together) | R$_{DS(ON)}$ | V$_{DD2}$ = 13.2 V, I$_O$ = 500 mA, T$_J$ = 25 °C | -- | 170 | -- | mΩ |
| | | V$_{DD2}$ = 13.2 V, I$_O$ = 500 mA, T$_J$ = 150 °C | -- | -- | 295 | mΩ |
| | | V$_{DD2}$ = 9.0 V, I$_O$ = 500 mA, T$_J$ = 25 °C | -- | 170 | -- | mΩ |
| | | V$_{DD2}$ = 9.0 V, I$_O$ = 500 mA, T$_J$ = 150 °C | -- | -- | 295 | mΩ |
| | | V$_{DD2}$ = 5.0 V, I$_O$ = 500 mA, T$_J$ = 25 °C | -- | 176 | -- | mΩ |
| | | V$_{DD2}$ = 5.0 V, I$_O$ = 500 mA, T$_J$ = 150 °C | -- | -- | 304 | mΩ |
| | | V$_{DD2}$ = 3.0 V, I$_O$ = 500 mA, T$_J$ = 25 °C | -- | 255 | -- | mΩ |
| | | V$_{DD2}$ = 3.0 V, I$_O$ = 500 mA, T$_J$ = 150 °C | -- | -- | 426 | mΩ |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LS FET on Resistance (SENSE_A, SENSE_B, GND_HV, and GND Pins are Connected Together, $R_{DS(ON)}$ with Sense Pin = GND, if Sense Pin $V_{DD}$ = 0.5 V, Additional 100 mΩ at Worst Case) | $R_{DS(ON)}$ | $V_{DD2}$ = 13.2 V, $I_O$ = 500 mA, $T_J$ = 25 °C | -- | 182 | -- | mΩ |
| | | $V_{DD2}$ = 13.2 V, $I_O$ = 500 mA, $T_J$ = 150 °C | -- | -- | 332 | mΩ |
| | | $V_{DD2}$ = 9.0 V, $I_O$ =500 mA, $T_J$ = 25 °C | -- | 182 | -- | mΩ |
| | | $V_{DD2}$ = 9.0 V, $I_O$ = 500 mA, $T_J$ = 150 °C | -- | -- | 332 | mΩ |
| | | $V_{DD2}$ = 5.0 V, $I_O$ = 500 mA, $T_J$ = 25 °C | -- | 185 | -- | mΩ |
| | | $V_{DD2}$ = 5.0 V, $I_O$ = 500 mA, $T_J$ = 150 °C | -- | -- | 338 | mΩ |
| | | $V_{DD2}$ = 3.0 V, $I_O$ = 500 mA, $T_J$ = 25 °C | -- | 232 | -- | mΩ |
| | | $V_{DD2}$ = 3.0 V, $I_O$ = 500 mA, $T_J$ = 150 °C | -- | -- | 414 | mΩ |
| Off-state Leakage Current | $I_{OFF}$ | GPO0_HD, GPO1_HD [1], $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 85 °C, PWM is off, including the charge pump OSC | 23.2 | -- | 32.9 | µA |
| | | GPO0_HD, GPO1_HD [1], $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 150 °C, PWM is off, including the charge pump OSC | 23.2 | -- | 35.2 | µA |
| | | GPO2_HD, GPO3_HD, $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 85 °C PWM is off, including the charge pump OSC | -- | -- | 0.2 | nA |
| | | GPO2_HD, GPO3_HD, $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 150 °C, PWM is off, including the charge pump OSC | -- | -- | 1.5 | µA |
| Charge Pump Consumption Current (from $V_{DD1}$ Pin or $V_{DD2}$ Pin) | $I_{CC}$ | $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 150 °C, PWM is off, including the charge pump OSC | -- | -- | 200 | µA |
| | | $V_{DD2}$ = 5.0 V, $T_J$ = -40 °C to 150 °C, PWM = 250 kHz | 100 | -- | 800 | µA |
| Wake-up Time | $t_{WAKE}$ | HV SLEEP OUT high to output transition, BG is always on, another pins SLEEP - disable | -- | 82.3 | 134 | µs |

[1] There is a resistive voltage divider in front of Diff Amplifier that is connected to GPO0_HD and GPO1_HD.

## 3.5   Protection Circuits

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Overcurrent Protection Threshold | $I_{OCP}$ | Per any HS or LS FET | -- | 2.18 | -- | A |
| OCP Deglitch Time [1] | $t_{OCP1}$ | $V_{DD}$ = 5 V, $V_{DD2}$ = 5 V, T = 25 °C, Deglitch = Enable, High Side | -- | 2.497 | -- | µs |
| | | $V_{DD}$ = 5 V, $V_{DD2}$ = 5 V, T = 25 °C, Deglitch = Enable, Low Side | -- | 1.232 | -- | µs |
| OCP Retry Time [2] | $t_{OCP2}$ | Delay = 492 µs | -- | 491 | -- | µs |
| Recover from Undervoltage Lockout | $V_{UVLO}$[3] | At rising edge of $V_{DD2}$ | -- | -- | 2.90 | V |
| Undervoltage Lockout | | At falling edge of $V_{DD2}$ | -- | -- | 2.77 | V |
| Thermal Shutdown Temperature | $T_{TSD}$ | Junction temperature $T_J$ | 135 | 141 | 159 | °C |
| Thermal Shutdown Hysteresis | $T_{HYST}$ | | -- | 16 | -- | °C |

[1] OCP deglitch time option can be enabled by register [873] and register [875] separately for each Full Bridge. The High Side FETs do not have OCP deglitch time if the current through the FET is higher than $I_{OCP}$ level during enable time. This is done to avoid huge currents during retry when the short is persist on the output.

[2] OCP retry time can be selected separately for each HV OUT: HV GPO0 – registers [780:778], HV GPO1 – registers [788:786], HV GPO2 – registers [796:794], HV GPO3 – registers [804:802].

[3] UVLO function can be enabled separately for $V_{DD2\_A}$ by register [864] and $V_{DD2\_B}$ by register [865].

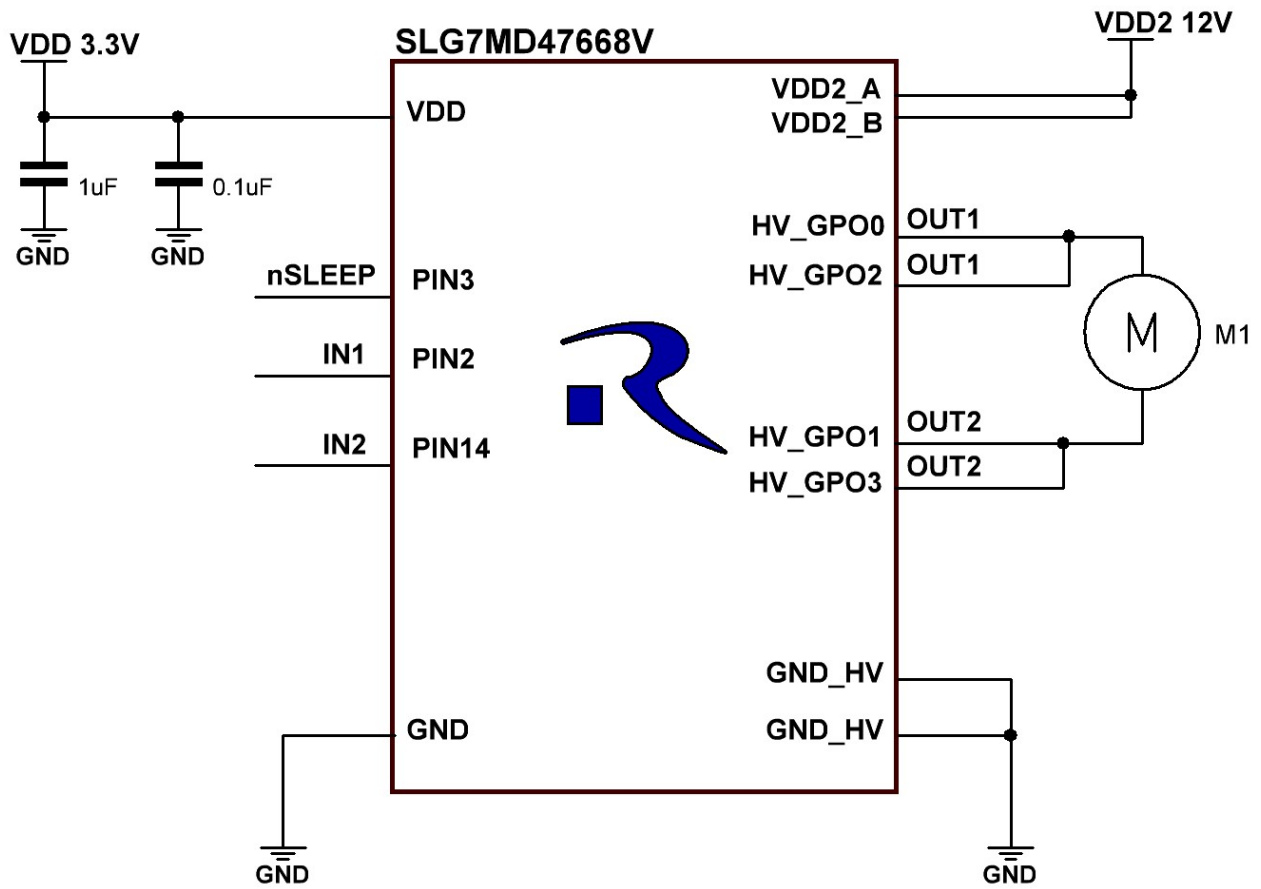# 4. Typical Application Circuit



**Figure 4. Typical Application Circuit**

# 5.   Functionality Waveforms

Channel 1 (yellow/top line) – PIN# 7 (OUT1) and PIN# 9 (OUT1).

Channel 2 (light blue/2nd line) – PIN# 8 (OUT2) and PIN# 10 (OUT2).

D0 – PIN# 3 (nSLEEP).

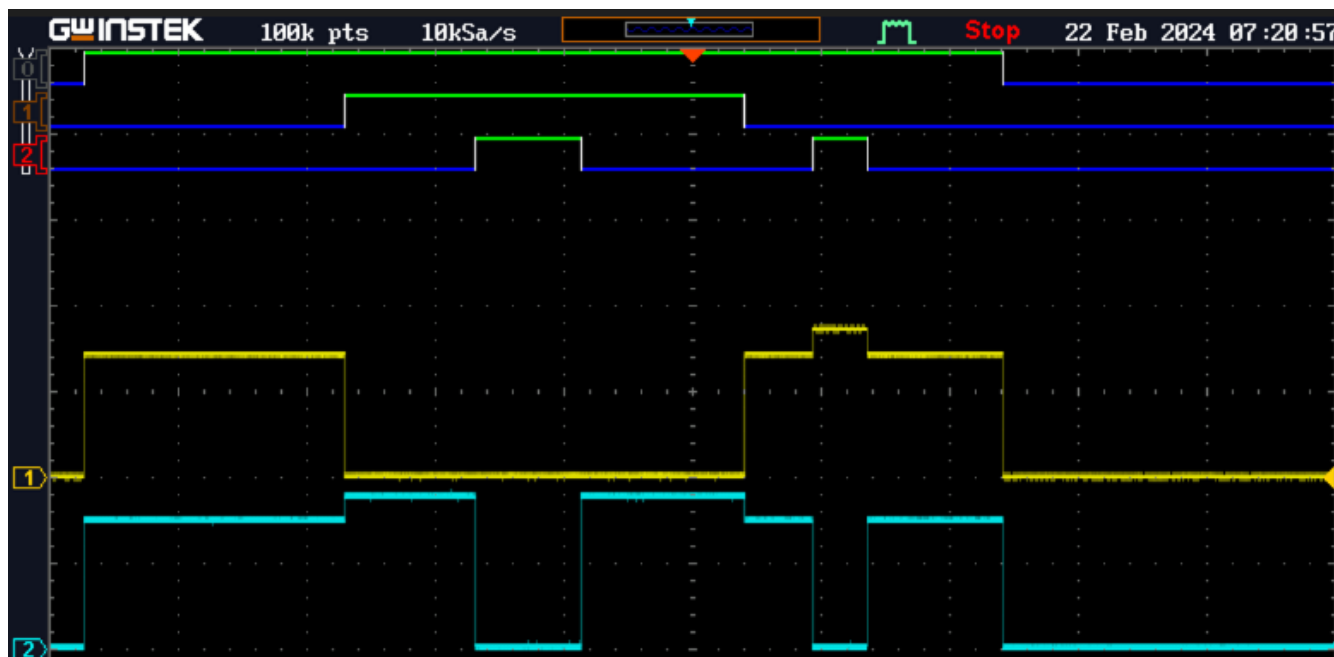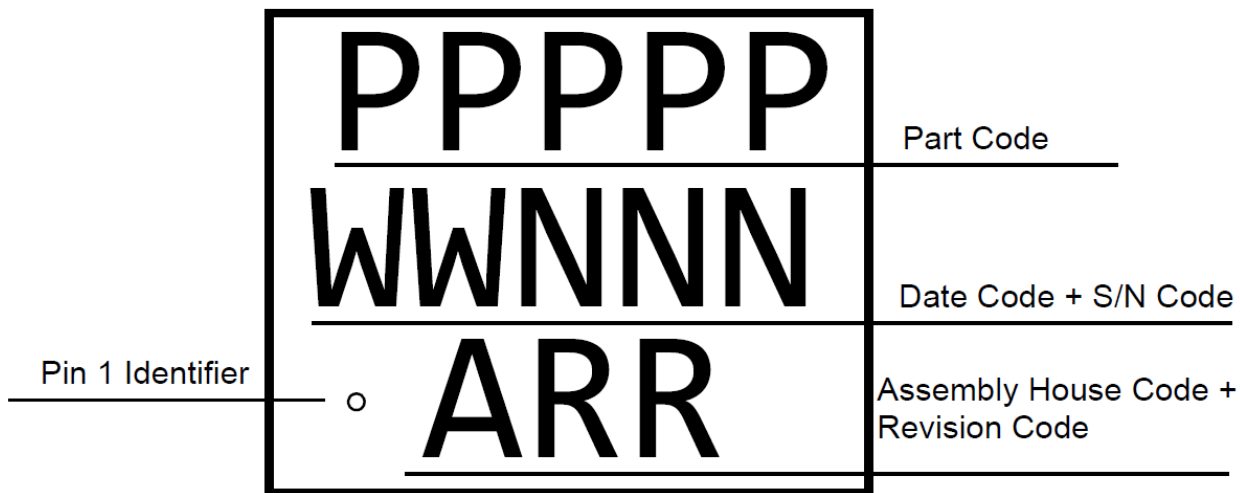D1 – PIN# 2 (IN1).

D2 – PIN# 14 (IN2).



**Figure 5. Chip Functionality**
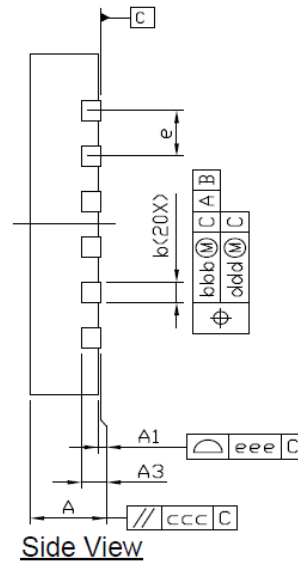
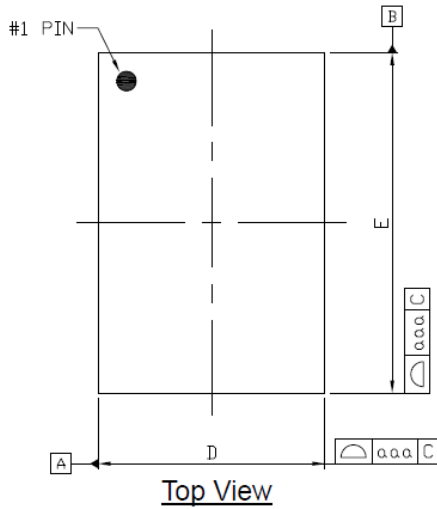# 6. Package Top Marking Definitions



| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|---|---|---|---|---|---|---|
| 1.00 | 001 | U | 0xBFB6A893 | | | 7/5/2024 |

Lock coverage for this part is indicated by √, from one of the following options:

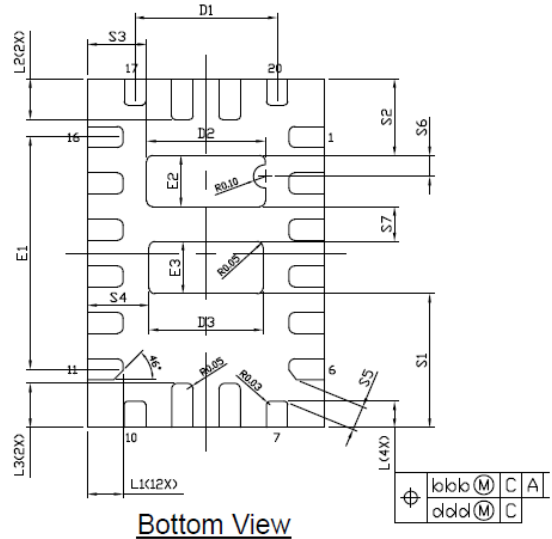| | |
|---|---|
| √ | Unlocked |
| | Partly lock read (mode 1) |
| | Partly lock read2 (mode 2) |
| | Partly lock read2/write (mode 3) |
| | All lock read (mode 4) |
| | All lock write (mode 5) |
| | All lock read/write (mode 6) |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

# 7.  Package Outlines



Top View



Side View

## Notes:

1. All dimensions are in millimeters.

2. Dimension "b" applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.

3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminal.



Bottom View

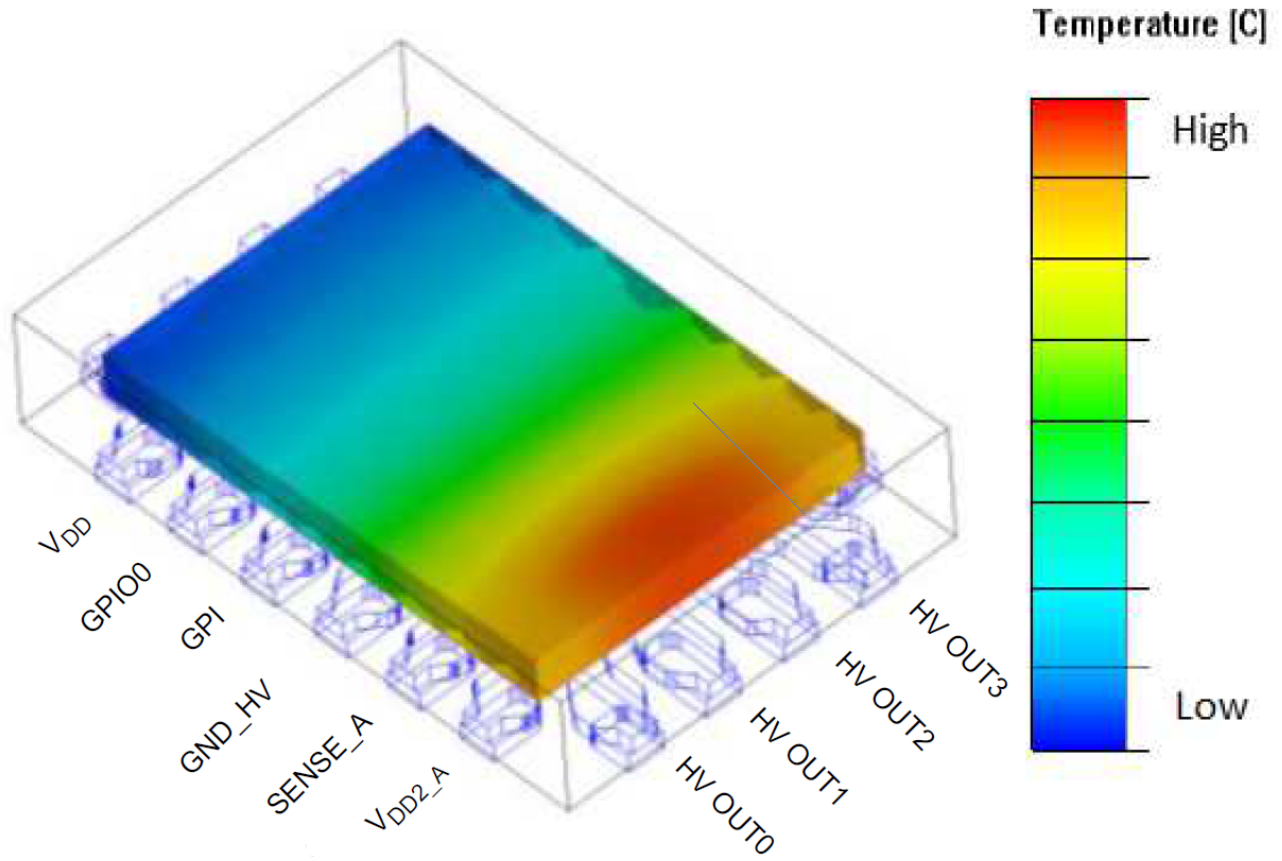Controlling dimension: mm

| Symbol | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.000 | 0.020 | 0.050 | 0.000 | 0.001 | 0.002 |
| A3 | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 1.95 | 2.00 | 2.05 | 0.077 | 0.079 | 0.081 |
| E | 2.95 | 3.00 | 3.05 | 0.116 | 0.118 | 0.120 |
| D1 | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| E1 | 1.95 | 2.00 | 2.05 | 0.077 | 0.079 | 0.081 |
| D2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| E2 | 0.39 | 0.44 | 0.49 | 0.015 | 0.017 | 0.019 |
| D3 | 0.91 | 0.96 | 1.01 | 0.036 | 0.038 | 0.040 |
| E3 | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| S1 | 1.10 | 1.15 | 1.20 | 0.043 | 0.045 | 0.047 |
| S2 | 0.61 | 0.66 | 0.71 | 0.024 | 0.026 | 0.028 |
| S3 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| S4 | 0.47 | 0.52 | 0.57 | 0.018 | 0.020 | 0.022 |
| S5 | 0.208 REF | | | 0.008 REF | | |
| S6 | 0.180 REF | | | 0.007 REF | | |
| S7 | 0.300 REF | | | 0.012 REF | | |

"A1" max lead coplanarity 0.05 mm
Standard tolerance: ±0.05

| Symbol | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.175 | 0.225 | 0.275 | 0.007 | 0.009 | 0.011 |
| L1 | 0.250 | 0.300 | 0.350 | 0.010 | 0.012 | 0.014 |
| L2 | 0.300 | 0.350 | 0.400 | 0.012 | 0.014 | 0.016 |
| L3 | 0.330 | 0.380 | 0.430 | 0.013 | 0.015 | 0.017 |
| b | 0.130 | 0.180 | 0.230 | 0.005 | 0.007 | 0.009 |
| aaa | 0.07 | | | 0.003 | | |
| bbb | 0.07 | | | 0.003 | | |
| ccc | 0.1 | | | 0.004 | | |
| ddd | 0.05 | | | 0.002 | | |
| eee | 0.08 | | | 0.003 | | |

# 8. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to 85 °C. To guarantee reliable operation, the junction temperature of the SLG7MD47668 must not exceed 150 °C.

# 9. Layout Consideration

PCB should have enough ground plane to dissipate heat. SLG7MD47668 has two additional pads, which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from chip to other layers of the PCB.

The sense resistors and power capacitors should be placed as close as possible to the chip for reducing parasitic parameters.
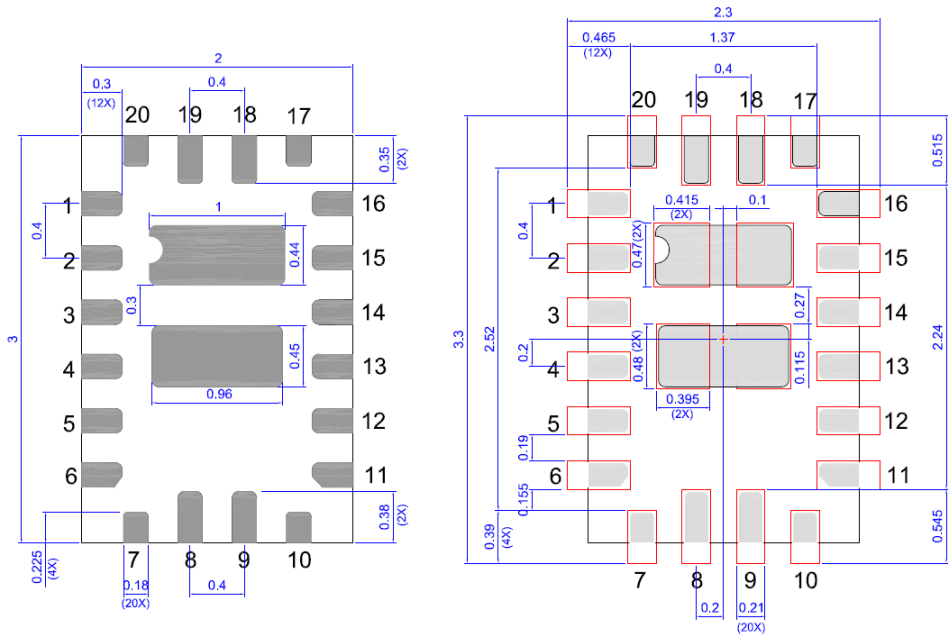
It is highly recommended to place low-ESR capacitor between $V_{DD2\_A}$, $V_{DD2\_B}$, and GND pin to keep input voltage stable and reduce ripple. This capacitor should be placed as close to the pins as possible. Also, the capacitor must have the low input impedance at the switching frequency. The recommended value of this capacitor is 1-10 µF for most applications. Motors with larger armature inductors require larger input capacitors.

Also, it is highly recommended to place 0.1 µF ceramic capacitor between $V_{DD}$ and GND.

# 10. Layout Guidelines

Expose Pad
(Package face down)

Recommended Landing Pattern
(Package face down)



## 10.1 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020. More information can be found at www.jedec.org.
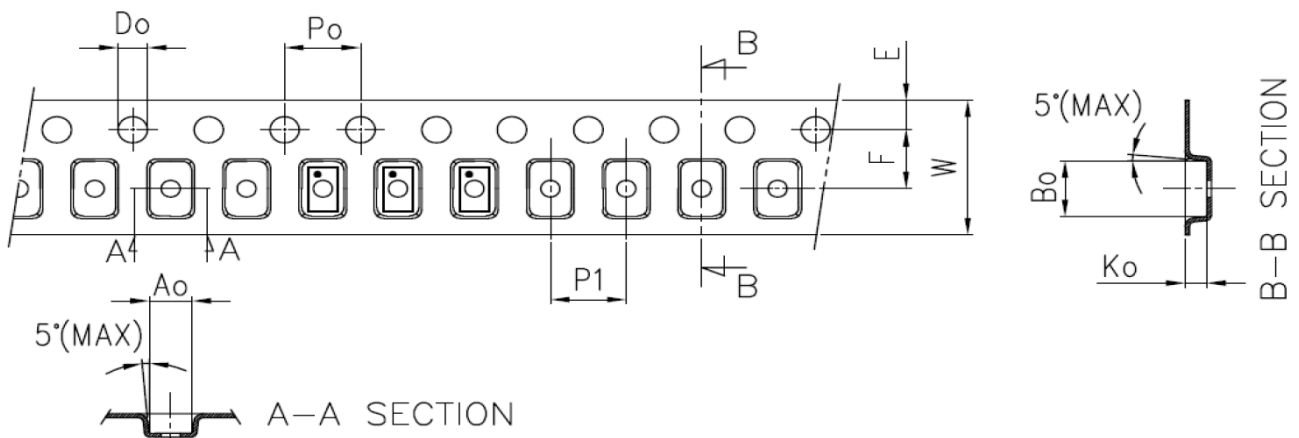
# 11. Ordering Information

| Part Number | Package Type |
|---|---|
| SLG7MD47668V | 20-pin STQFN - Tape and Reel (3k units) |

## 11.1 Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green | 20 | 2.0x3.0x0.55 | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

## 11.2 Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 20L 2.0 mm x 3.0 mm 0.4P FCD Green | 2.2 | 3.15 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |

# 12. Revision History

| Revision | Date | Description |
|----------|------|-------------|
| 1.00 | Jul 5, 2024 | Initial release |