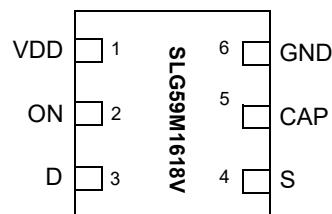


**General Description**

The SLG59M1618V is a 19 mΩ 2.0 A single-channel load switch that is able to switch 0.85 V to 5 V power rails. The product is packaged in an ultra-small 1.0 x 1.4 mm package.

**Features**

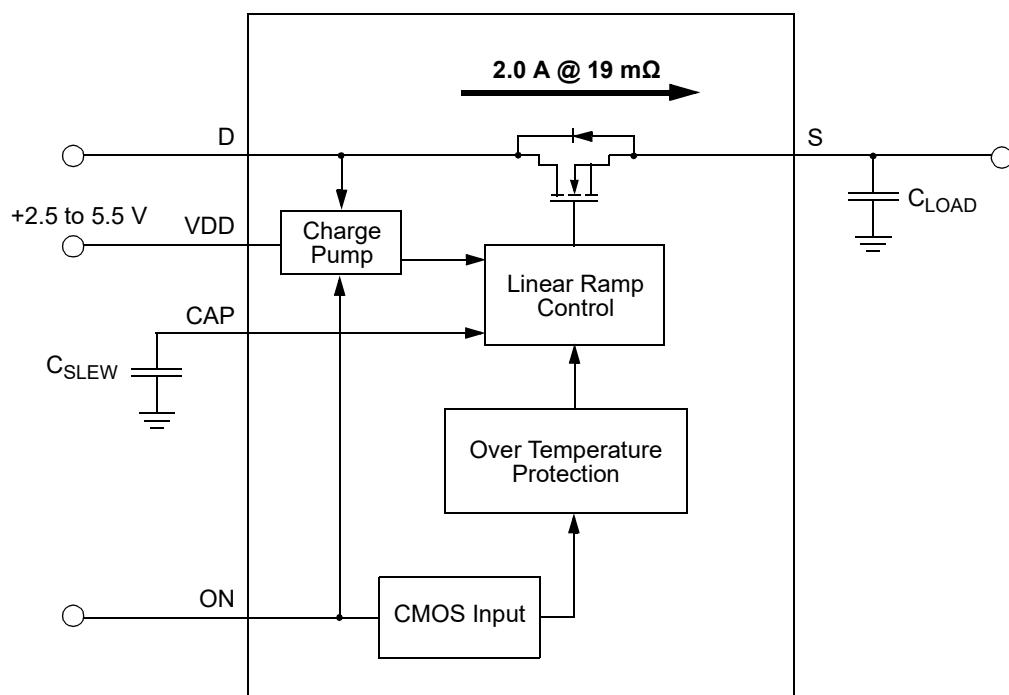
- 1.0 x 1.4 mm STDFN, 0.4 mm pin pitch package
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 19 mΩ  $R_{DS\text{ON}}$  while supporting 2.0 A
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85°C
- Operating Voltage: 2.5 V to 5.5 V

**Pin Configuration**

**6-pin STDFN**  
(Top View)

**Applications**

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

**Block Diagram**

**Pin Description**

| Pin # | Pin Name | Type   | Pin Description   |
|-------|----------|--------|---|
| 1     | VDD      | Power  | With an internal 1.9 V UVLO threshold, VDD supplies the power for the operation of the load switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 $\mu$ F (or larger) capacitor.  |
| 2     | ON       | Input  | A low-to-high transition on this pin initiates the operation of the SLG59M1618V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with $V_{IL} < 0.3$ V and $V_{IH} > 0.85$ V. While there is an internal pull-down circuit to GND (~4 M $\Omega$ ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited. |
| 3     | D        | MOSFET | Drain terminal connection of the n-channel FET. Connect a 10 $\mu$ F (or larger) low-ESR capacitor from this pin to ground. Capacitors used at D should be rated at 10 V or higher.   |
| 4     | S        | MOSFET | Source terminal connection of the n-channel FET. Connect a 10 $\mu$ F (or larger) low-ESR capacitor from this pin to ground. Capacitors used at S should be rated at 10 V or higher.  |
| 5     | CAP      | Output | A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the $V_S$ slew rate and overall turn-on time of the SLG59M1618V. For best performance, the range for $C_{SLEW}$ values are $1\text{ nF} \leq C_{SLEW} \leq 22\text{ nF}$ . Capacitors used at CAP should be rated at 10 V or higher.   |
| 6     | GND      | GND    | Ground connection. Connect this pin to system analog or power ground plane.   |

**Ordering Information**

| Part Number   | Type                     | Production Flow             |
|---------------|--------------------------|-----------------------------|
| SLG59M1618V   | STDFN 6L                 | Industrial, -40 °C to 85 °C |
| SLG59M1618VTR | STDFN 6L (Tape and Reel) | Industrial, -40 °C to 85 °C |

**Absolute Maximum Ratings**

| Parameter                | Description                       | Conditions   | Min. | Typ. | Max. | Unit |
|--------------------------|-----------------------------------|--|------|------|------|------|
| V <sub>DD</sub>          | Power Supply                      |  | --   | --   | 6    | V    |
| T <sub>S</sub>           | Storage Temperature               |  | -65  | --   | 150  | °C   |
| ESD <sub>HBM</sub>       | ESD Protection                    | Human Body Model   | 2000 | --   | --   | V    |
| ESD <sub>CDM</sub>       | ESD Protection                    | Charged Device Model   | 1000 | --   | --   | V    |
| MSL                      | Moisture Sensitivity Level        |  |      |      | 1    |      |
| θ <sub>JA</sub>          | Thermal Resistance                | 1.0 x 1.4 mm 6L STDFN; Determined using 1 in <sup>2</sup> , 1 oz. copper pads under VD and VS terminals and FR4 pcb material | --   | 72   | --   | °C/W |
| W <sub>DIS</sub>         | Package Power Dissipation         |  | --   | --   | 0.4  | W    |
| MOSFET IDS <sub>PK</sub> | Peak Current from Drain to Source | Maximum pulsed switch current, pulse width < 1ms, 1% duty cycle  | --   | --   | 3    | A    |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Electrical Characteristics**

T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated)

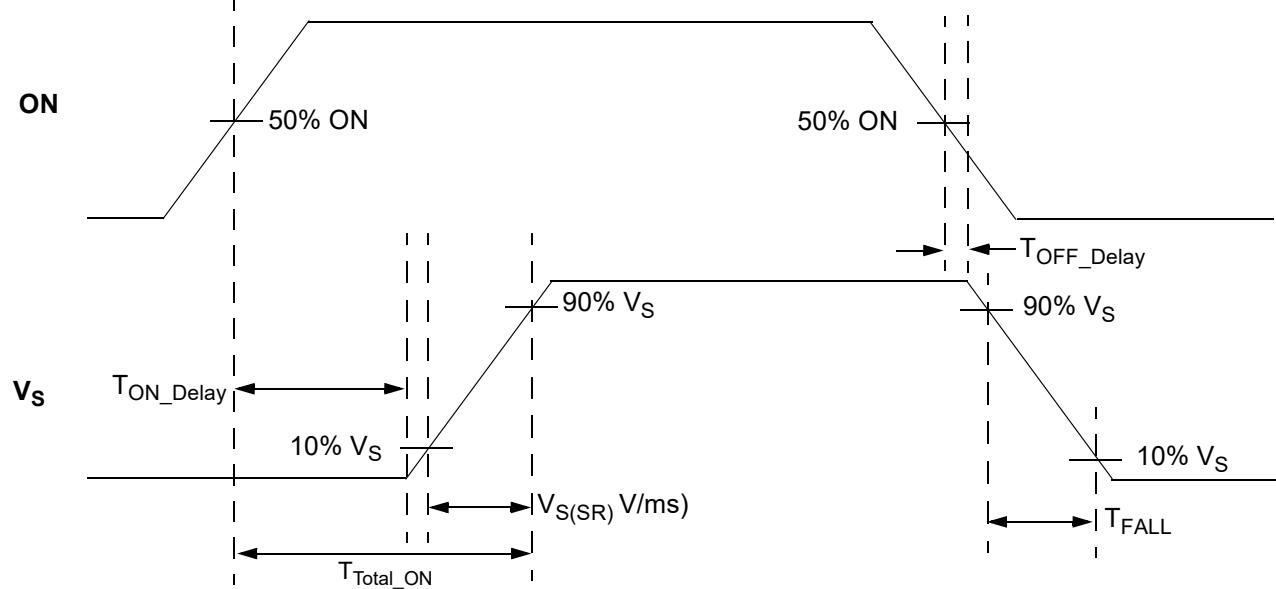
| Parameter              | Description                                    | Conditions   | Min. | Typ. | Max.                      | Unit |
|------------------------|--|--|------|------|---------------------------|------|
| V <sub>DD</sub>        | Power Supply Voltage                           | -40 °C to 85 °C  | 2.5  | --   | 5.5                       | V    |
| V <sub>DD(UVLO)</sub>  | V <sub>DD</sub> Undervoltage Lockout Threshold |  | 1.6  | 1.9  | 2.2                       | V    |
| I <sub>DD</sub>        | Power Supply Current (PIN 1)                   | when OFF   | --   | --   | 1                         | µA   |
|                        |  | when ON, No load   | --   | 100  | 120                       | µA   |
| RDS <sub>ON</sub>      | Static Drain to Source ON Resistance           | T <sub>A</sub> 25°C @ 100 mA   | --   | 19   | 22                        | mΩ   |
|                        |  | T <sub>A</sub> 85°C @ 100 mA   | --   | 20   | 25                        | mΩ   |
| MOSFET IDS             | Current from Drain to Source                   | Continuous   | --   | --   | 2.0                       | A    |
| V <sub>D</sub>         | Drain Voltage                                  |  | 0.85 | --   | V <sub>DD</sub>           | V    |
| T <sub>ON_Delay</sub>  | ON pin Delay Time                              | 50% ON to Ramp Begin   | --   | 400  | 600                       | µs   |
| T <sub>Total_ON</sub>  | Total Turn On Time                             | 50% ON to 90% V <sub>S</sub>   |      |      | Configurable <sup>1</sup> | ms   |
|                        |  | Example: C <sub>SLEW</sub> = 4 nF;<br>V <sub>DD</sub> = V <sub>D</sub> = 5 V, C <sub>LOAD</sub> = 10 µF,<br>R <sub>LOAD</sub> = 20 Ω | --   | 1.80 | --                        | ms   |
| V <sub>S(SR)</sub>     | V <sub>S</sub> Slew Rate                       | 10% V <sub>S</sub> to 90% V <sub>S</sub>   |      |      | Configurable <sup>1</sup> | V/ms |
|                        |  | Example: C <sub>SLEW</sub> = 4 nF;<br>V <sub>DD</sub> = V <sub>D</sub> = 5 V, C <sub>LOAD</sub> = 10 µF,<br>R <sub>LOAD</sub> = 20 Ω | --   | 3    | --                        | V/ms |
| C <sub>LOAD</sub>      | Output Load Capacitance                        | C <sub>LOAD</sub> connected from S to GND  | --   | --   | 500                       | µF   |
| ON_V <sub>IH</sub>     | High Input Voltage on ON pin                   |  | 0.85 | --   | V <sub>DD</sub>           | V    |
| ON_V <sub>IL</sub>     | Low Input Voltage on ON pin                    |  | -0.3 | 0    | 0.3                       | V    |
| THERM <sub>ON</sub>    | Thermal shutoff turn-on temperature            |  | --   | 130  | --                        | °C   |
| THERM <sub>OFF</sub>   | Thermal shutoff turn-off temperature           |  | --   | 100  | --                        | °C   |
| THERM <sub>TIME</sub>  | Thermal shutoff time                           |  | --   | --   | 1                         | ms   |
| T <sub>OFF_Delay</sub> | OFF Delay Time                                 | 50% ON to V <sub>S</sub> Fall, V <sub>DD</sub> = V <sub>D</sub> = 5 V,<br>R <sub>LOAD</sub> = 20 Ω, no C <sub>LOAD</sub>             | --   | 2.0  | --                        | µs   |

**Electrical Characteristics** (continued) $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise stated)

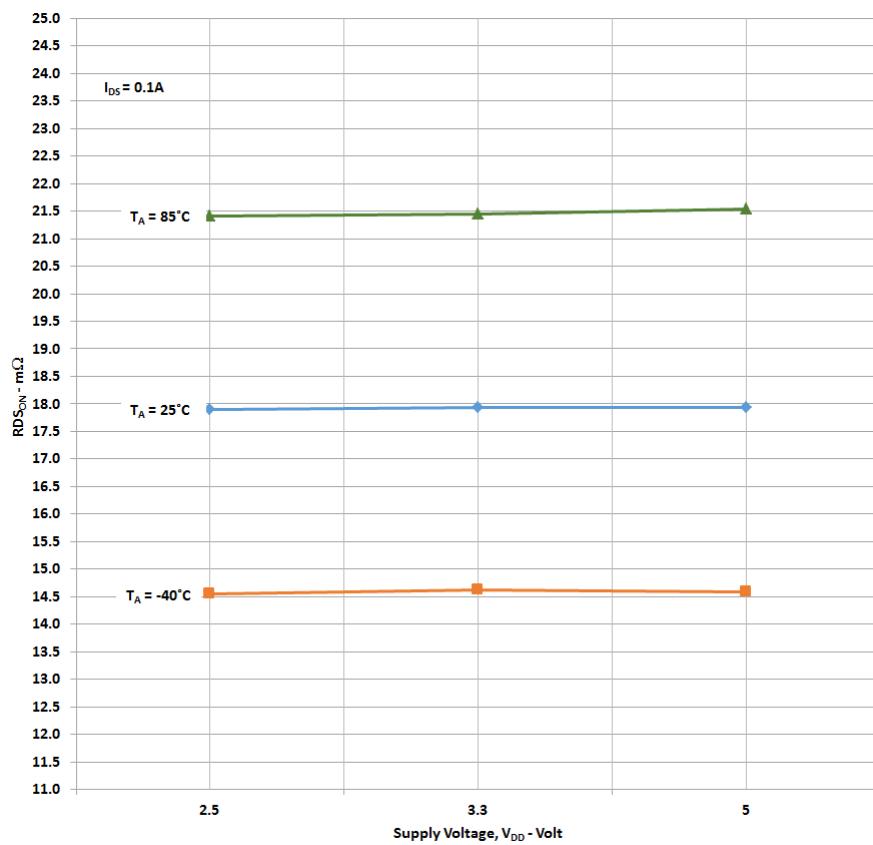
| Parameter  | Description     | Conditions  | Min. | Typ. | Max. | Unit          |
|------------|-----------------|---|------|------|------|---------------|
| $T_{FALL}$ | $V_S$ Fall Time | 90% $V_S$ to 10% $V_S$ , $V_{DD} = V_D = 5\text{ V}$ ,<br>$R_{LOAD} = 20\ \Omega$ , no $C_{LOAD}$ | --   | 0.25 | --   | $\mu\text{s}$ |

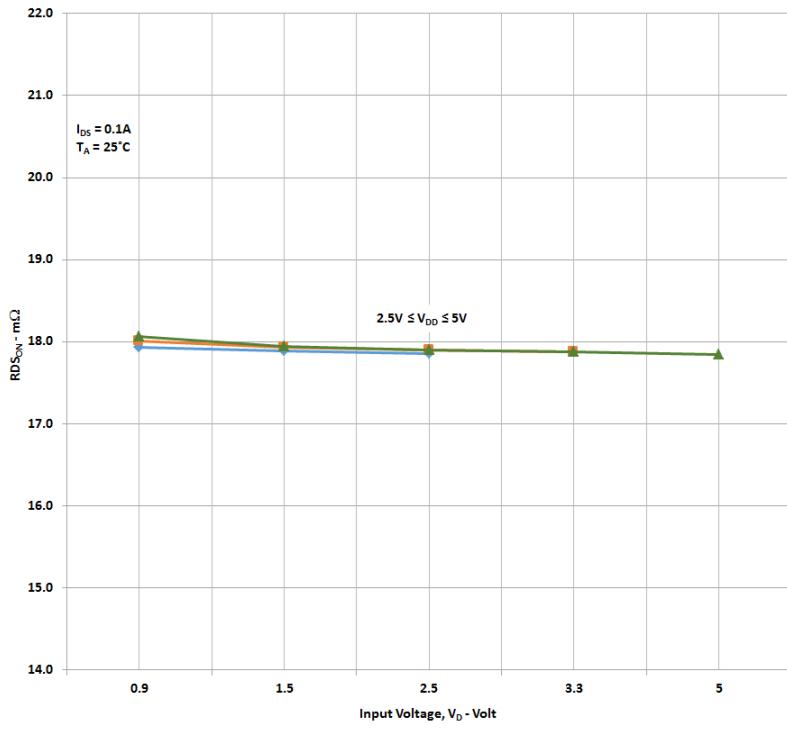
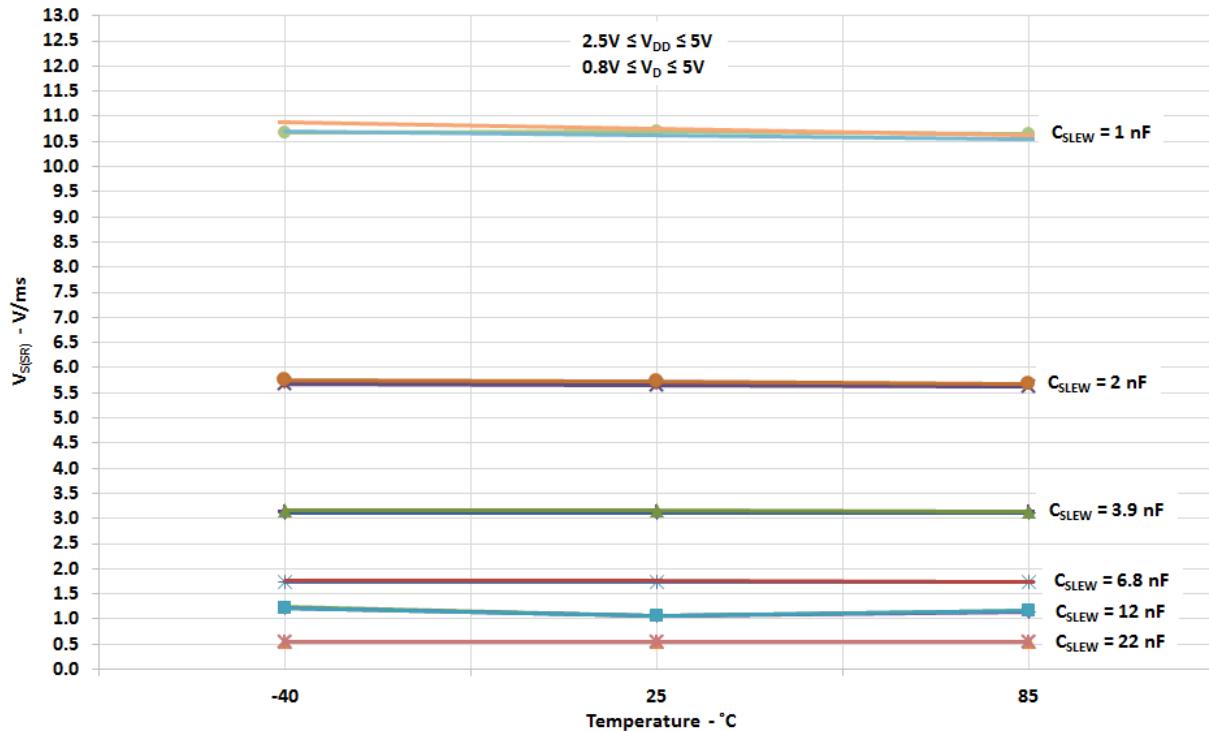
## Notes:

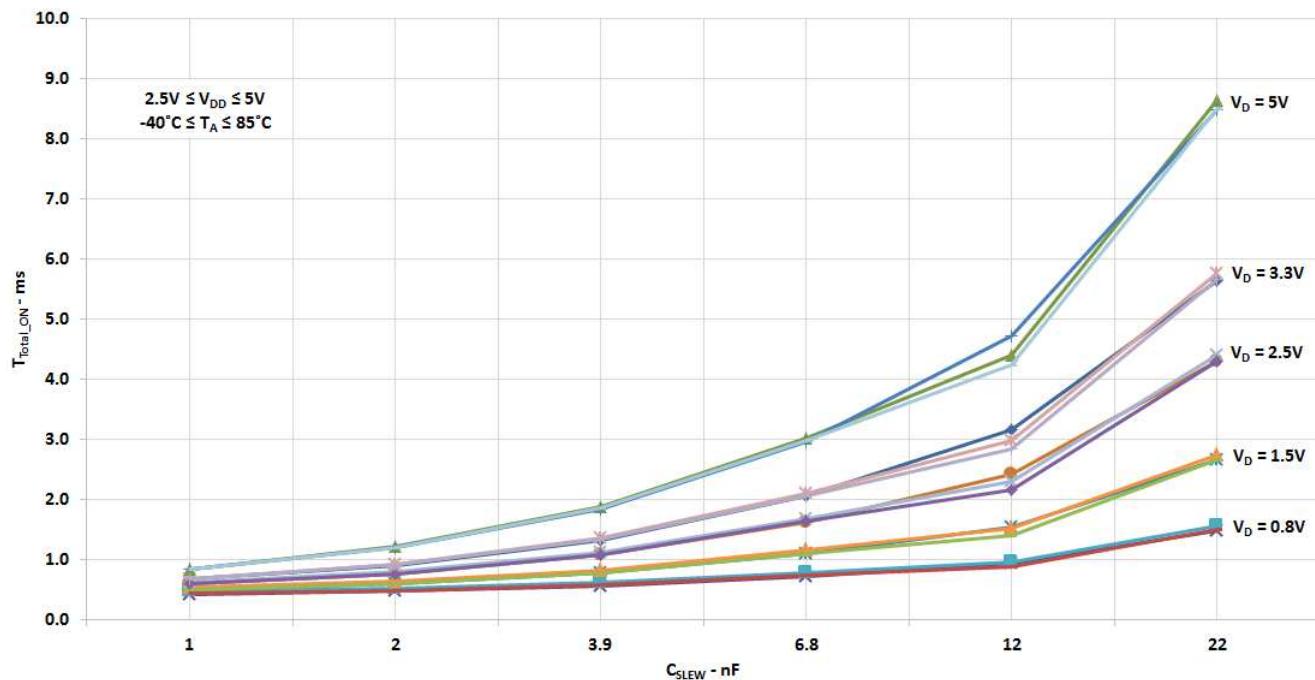
1. Refer to table for configuration details.

**T<sub>Total\_ON</sub>, T<sub>ON\_Delay</sub> and Slew Rate Measurement**

\* Rise and Fall times of the ON signal are 100 ns

**Typical Performance Characteristics****RDS<sub>ON</sub> vs. V<sub>DD</sub> and Temperature**

**RDS<sub>ON</sub> vs. V<sub>D</sub> and V<sub>DD</sub>****V<sub>S</sub> Slew Rate vs. Temperature, V<sub>DD</sub>, V<sub>D</sub>, and C<sub>SLEW</sub>**

T<sub>Total\_ON</sub> vs. C<sub>SLEW</sub>, V<sub>D</sub>, V<sub>DD</sub>, and Temperature

## Typical Turn-on Waveforms

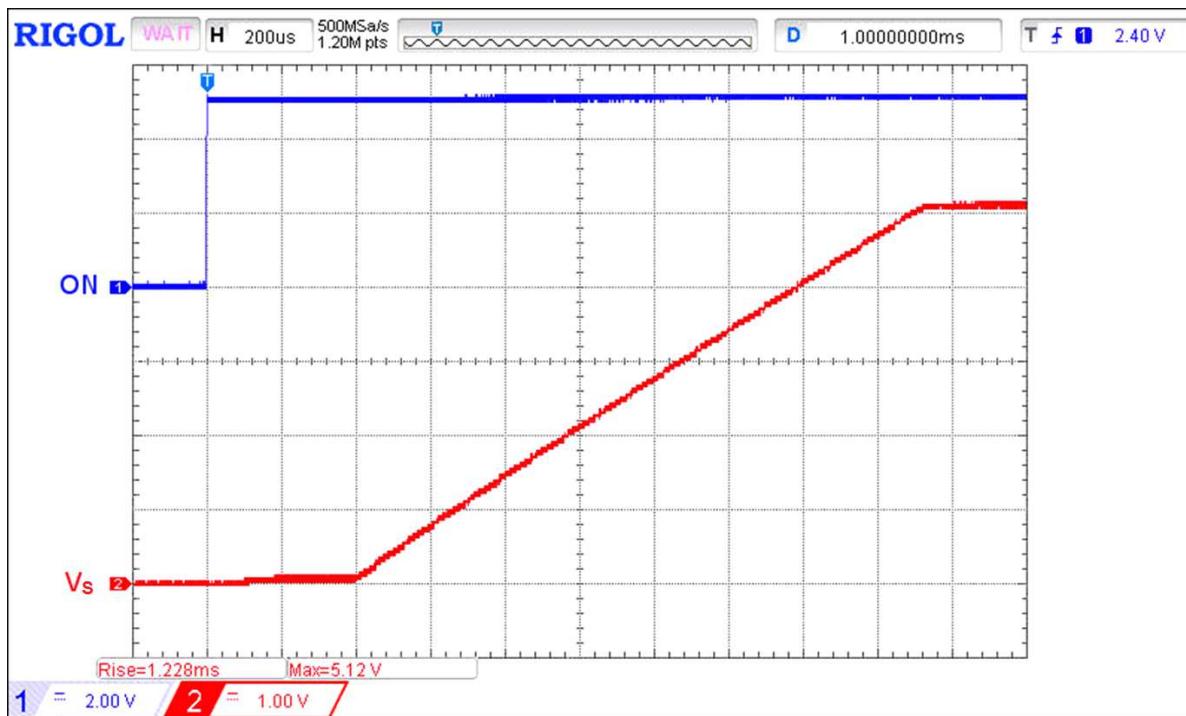


Figure 1. Typical Turn ON operation waveform for  $V_D = 5 \text{ V}$ ,  $C_{\text{SLEW}} = 4 \text{ nF}$ ,  $C_{\text{LOAD}} = 10 \mu\text{F}$ ,  $R_{\text{LOAD}} = 20 \Omega$

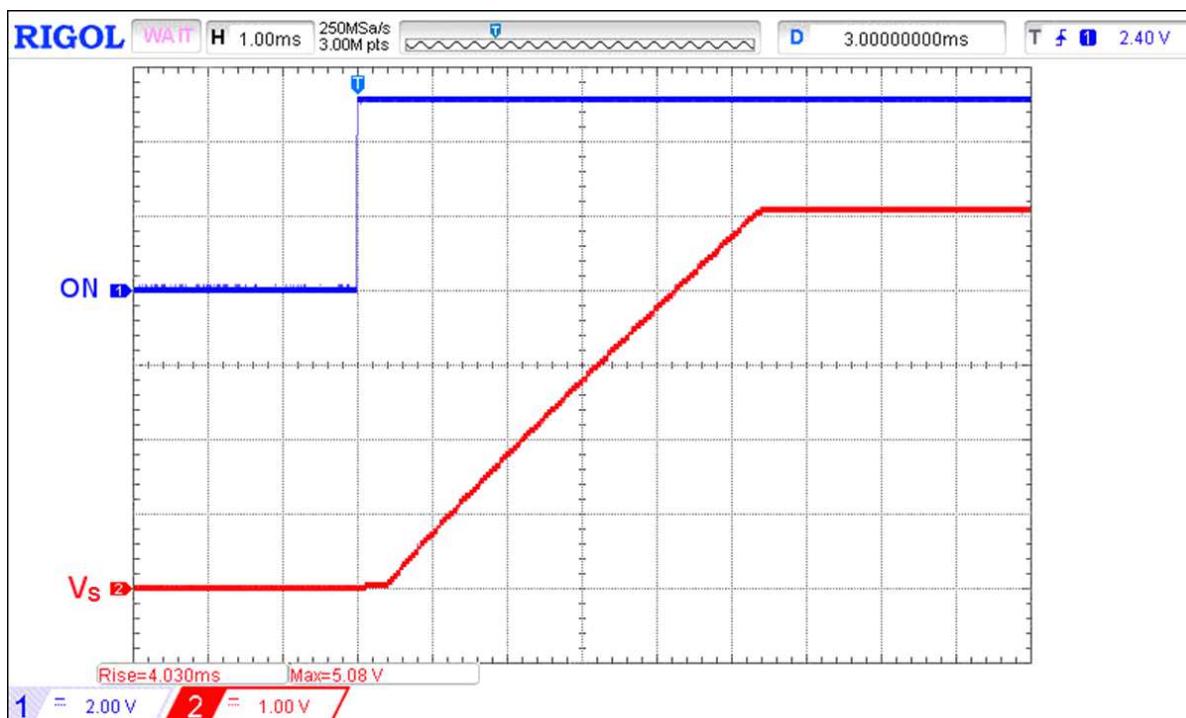
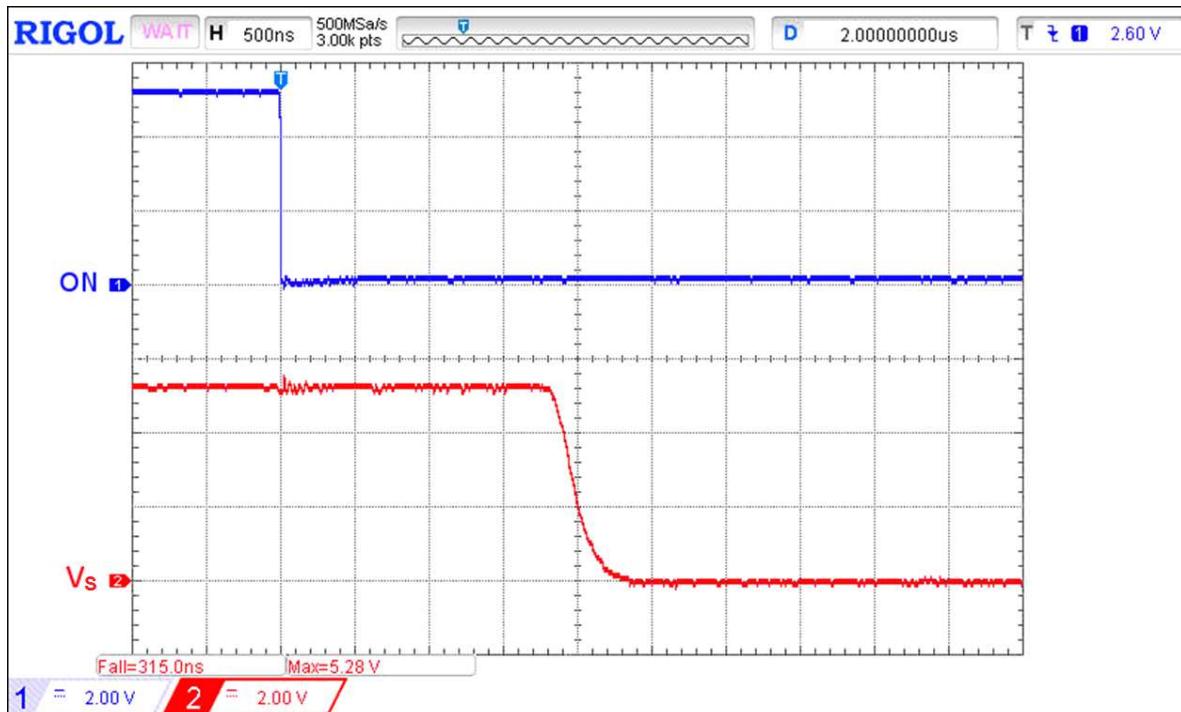
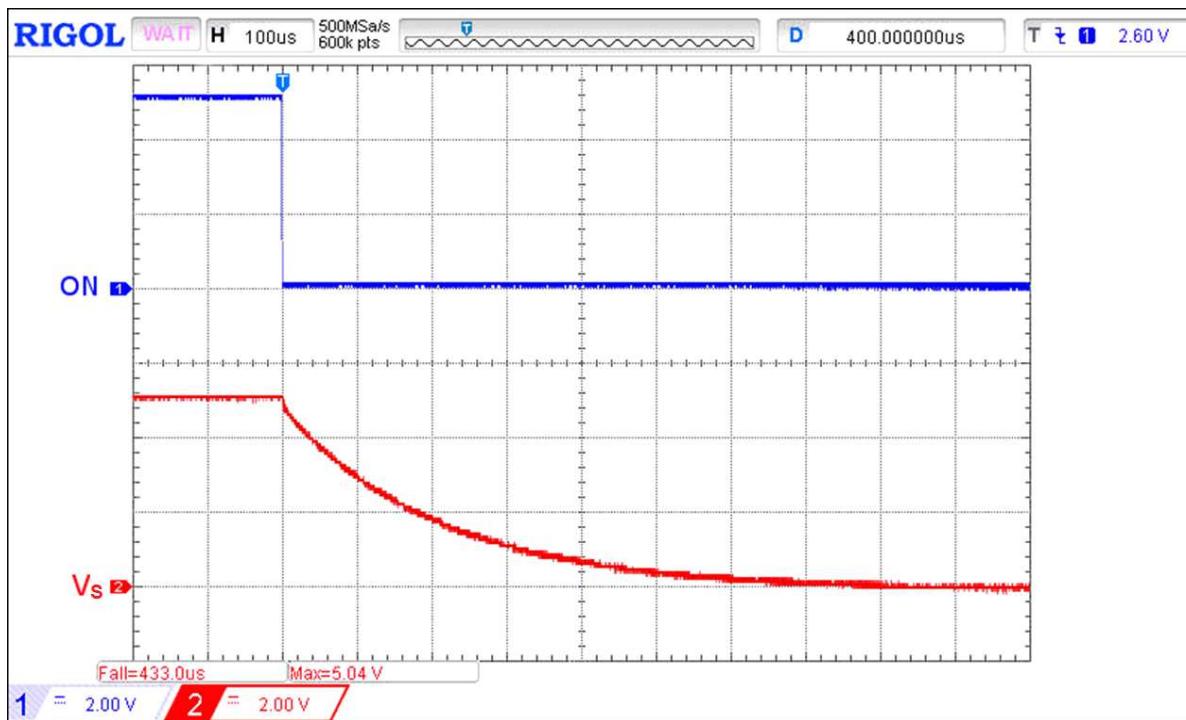


Figure 2. Typical Turn ON operation waveform for  $V_D = 5 \text{ V}$ ,  $C_{\text{SLEW}} = 12 \text{ nF}$ ,  $C_{\text{LOAD}} = 10 \mu\text{F}$ ,  $R_{\text{LOAD}} = 20 \Omega$

## Typical Turn-off Waveforms

Figure 3. Typical Turn OFF operation waveform for  $V_D = 5$  V,  $C_{SLEW} = 4$  nF, no  $C_{LOAD}$ .  $R_{LOAD} = 20$   $\Omega$ Figure 4. Typical Turn OFF operation waveform for  $V_D = 5$  V,  $C_{SLEW} = 4$  nF,  $C_{LOAD} = 10$   $\mu$ F.  $R_{LOAD} = 20$   $\Omega$

### **SLG59M1618V Power-Up/Power-Down Sequence Considerations**

To ensure glitch-free power-up under all conditions, apply  $V_{DD}$  first, followed by  $V_D$  after  $V_{DD}$  exceeds 1.9 V. Then allow  $V_D$  to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If  $V_{DD}$  and  $V_D$  need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10  $\mu$ F  $C_{LOAD}$  will prevent glitches for rise times of  $V_{DD}$  and  $V_D$  higher than 2 ms.

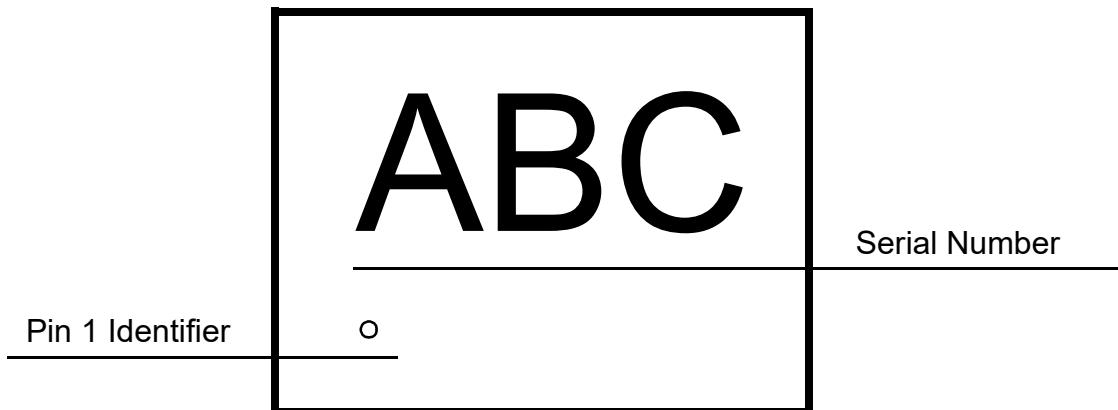
If the ON pin is toggled HIGH before  $V_{DD}$  and  $V_D$  have reached their steady-state values, the load switch timing parameters may differ from datasheet specifications.

The slew rate of output  $V_S$  follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

### **SLG59M1618V Thermal Shutdown Operation**

If a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed  $THERM_{ON}$  specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed  $THERM_{OFF}$  temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

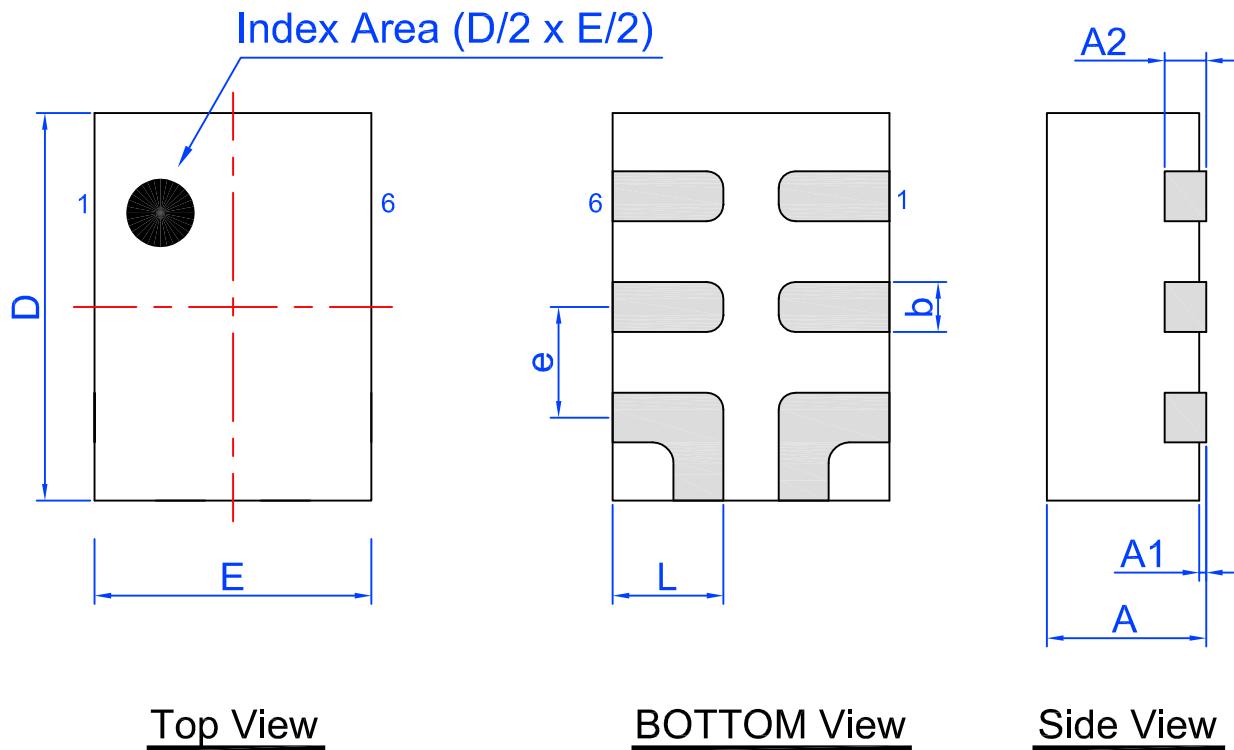
For more information on GreenFET load switch features, please visit our website and see App Note "AN-1068 GreenFET and High Voltage GreenFET Load Switch Basics.

**Package Top Marking System Definition**

ABC - Part Serial Number Field  
each A, B, and C character can be A-Z and 0-9

## Package Drawing and Dimensions

6 Lead STDFN Package 1.0 x 1.4 mm



Unit: mm

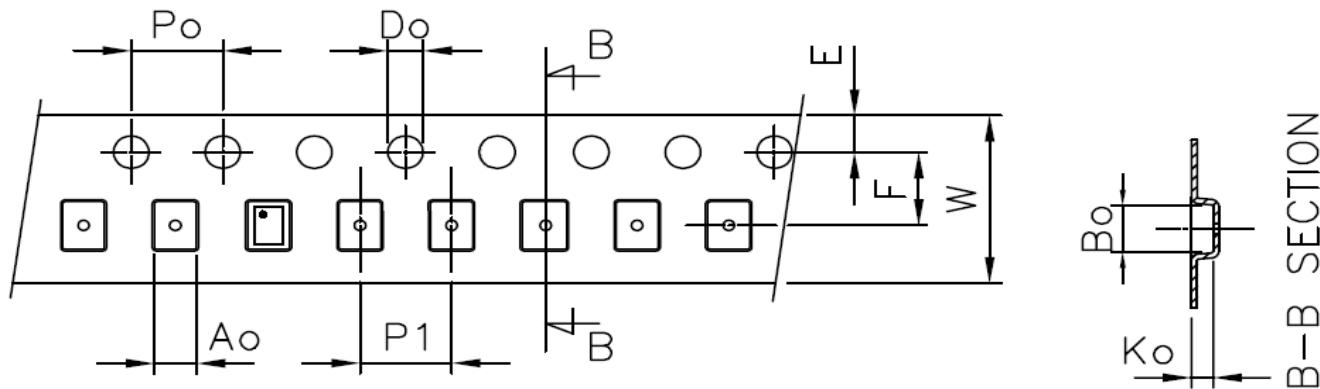
| Symbol | Min   | Nom. | Max   | Symbol | Min      | Nom. | Max  |
|--------|-------|------|-------|--------|----------|------|------|
| A      | 0.50  | 0.55 | 0.60  | D      | 1.35     | 1.40 | 1.45 |
| A1     | 0.005 | -    | 0.060 | E      | 0.95     | 1.00 | 1.05 |
| A2     | 0.10  | 0.15 | 0.20  | L      | 0.35     | 0.40 | 0.45 |
| b      | 0.13  | 0.18 | 0.23  | e      | 0.40 BSC |      |      |

**Tape and Reel Specifications**

| Package Type                            | # of Pins | Nominal Package Size [mm] | Max Units |         | Reel & Hub Size [mm] | Leader (min) |             | Trailer (min) |             | Tape Width [mm] | Part Pitch [mm] |
|---|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
|   |           |                           | per Reel  | per Box |                      | Pockets      | Length [mm] | Pockets       | Length [mm] |                 |                 |
| STDFN 6L<br>1x1.4mm<br>0.4P FC<br>Green | 6         | 1.0 x 1.4 x 0.55          | 3,000     | 3,000   | 178 / 60             | 100          | 400         | 100           | 400         | 8               | 4               |

**Carrier Tape Drawing and Dimensions**

| Package Type                            | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
|   | A0                | B0               | K0           | P0               | P1           | D0                  | E                       | F                           | W          |
| STDFN 6L<br>1x1.4mm<br>0.4P FC<br>Green | 1.21              | 1.62             | 0.75         | 4                | 4            | 1.5                 | 1.75                    | 3.5                         | 8          |


**Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.77 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

**Revision History**

| Date      | Version | Change                            |
|-----------|---------|-----------------------------------|
| 2/14/2022 | 1.01    | Renesas rebranding<br>Fixed typos |
| 2/23/2017 | 1.00    | Production Release                |

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