

Dual Input Single Output 12 V Power Multiplexer

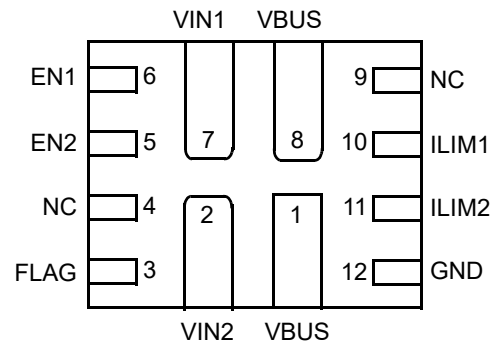
General Description

The SLG59H1405V is designed for 5V/12V manual switchover Power MUX applications. The part comes with one 3 A and one 1.25 A rated load switches that are well suited for a variety of systems having multiple power sources. The device allows manually select and seamlessly transition between available inputs as well as provide different kind of protection features.

Features

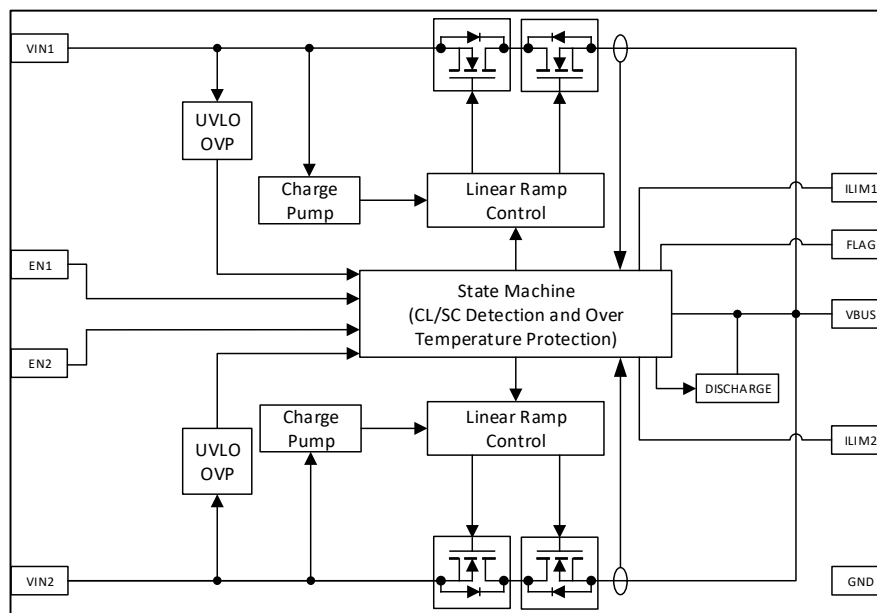
- 5V / 3A and 12V / 1.25A load switches with common output
- Wide Operating Input Voltage Range:
 - V_{IN1} : 4 V to 5.5 V
 - V_{IN2} : 4 V to 13.2 V
- Low Typical $R_{DS(ON)}$:
 - 40 m Ω for Channel 1
 - 67 m Ω for Channel 2
- Individual Channel Enable Control
- Input Under-Voltage Lockout
- Input Over-Voltage Protection
- Channel 1 True Reverse-Current Blocking
- Over-temperature Protection
- Resistor-Adjustable Active Current Limit Protection for each channel
- Internal Short-Circuit Current Limit
- Open Drain Fault FLAG Output
- Output Discharge when off and during switchover
- Robust ESD Capability
 - 2 kV HBM and 1 kV CDM
 - 8 kV Air Discharge and 4 kV Contact Discharge under IEC 61000-4-2
- 2 mm x 2.5 mm, 0.5 mm pitch, 12L FC-QFN
 - Pb-Free / Halogen-Free / RoHS Compliant

Pin Configuration



12-pin FC-QFN
(Bottom View)

Block Diagram



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Pin Description

Pin #	Pin Name	Type	Pin Description
1, 8	VBUS	Output	Output terminal. Capacitors at VBUS should be rated at a voltage higher than maximum input voltage ever present.
2	VIN2	Power	Input terminal of Channel 2. Capacitors at VIN2 should be rated at a voltage higher than maximum input voltage ever present.
3	FLAG	Output	An open-drain output, FLAG is asserted LOW when a $V_{IN[1,2]}$ overvoltage, undervoltage, current-limit, or an over-temperature condition is detected. Connect a 100 k Ω external resistor from the FLAG pin to a local system logic supply. Connect to GND if not used.
4	NC	Input	No Connect.
5	EN2	Input	EN2 turns on Channel 2 and is a low logic-level CMOS input with $EN2_V_{IL} < 0.5\text{ V}$ and $EN2_V_{IH} > 1.5\text{ V}$. While there is an internal pull-down circuit to GND ($\sim 1\text{ M}\Omega$), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
6	EN1	Input	EN1 turns on Channel 1 and is a low logic-level CMOS input with $EN1_V_{IL} < 0.5\text{ V}$ and $EN1_V_{IH} > 1.5\text{ V}$. While there is an internal pull-down circuit to GND ($\sim 1\text{ M}\Omega$), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
7	VIN1	Power	Input terminal of Channel 1. Capacitors at VIN1 should be rated at a voltage higher than maximum input voltage ever present.
9	NC	Input	No Connect.
10	ILIM1	Output	A 1%-tolerance, metal-film resistor sets the active current limit for Channel 1. A 20 k Ω resistor sets the active current limit to 4.08 A
11	ILIM2	Output	A 1%-tolerance, metal-film resistor sets the active current limit for Channel 2. A 20 k Ω resistor sets the active current limit to 1.9 A
12	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59H1405V	FC-QFN 12L	Industrial, -20 °C to 85 °C
SLG59H1405VTR	FC-QFN 12L (Tape and Reel)	Industrial, -20 °C to 85 °C

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Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN1}	Maximum Input Voltage for Channel 1		-0.3	--	6.5	V
V_{IN2}	Maximum Input Voltage for Channel 2		-0.3	--	18	V
V_{BUS}	Maximum Output Voltage		-0.3	--	18	V
V_{EN1}, V_{EN2}	Maximum Control Input Pin Voltage		-0.3	--	6	V
$V_{ILIM1}, V_{ILIM2}, V_{FLAG}$	Maximum Control Output Pin Voltage		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD _{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
ESD _{SYS}	IEC61000-4-2 System Level ESD	Air Gap (VBUS to GND)	8			kV
		Contact (VBUS to GND)	4			kV
Channel 1 I_{PEAK}	Maximum Peak Current from VIN1 to VBUS	For no more than 10 continuous seconds out of every 100 seconds	--	--	4.5	A
Channel 2 I_{PEAK}	Maximum Peak Current from VIN2 to VBUS	For no more than 10 continuous seconds out of every 100 seconds	--	--	2.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

$T_A = -20\text{ °C}$ to 85 °C , unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN1}	Channel 1 Operating Input Voltage		4	--	5.5	V
V_{IN2}	Channel 2 Operating Input Voltage		4	--	13.2	V
I_{VIN1_OFF}	Channel 1 OFF Mode Supply Current	$EN1 < EN1_V_{IL}, EN2 < EN2_V_{IL}$	--	4	10	μA
I_{VIN2_OFF}	Channel 2 OFF Mode Supply Current	$EN1 < EN1_V_{IL}, EN2 < EN2_V_{IL}$	--	0.5	1	μA
I_{VIN1_Q}	Channel 1 Quiescent Supply Current	Channel 1 is ON, Channel 2 is OFF, $V_{BUS} = V_{IN1}$, no load	--	290	400	μA
		Channel 1 is OFF, Channel 2 is ON, $V_{BUS} = V_{IN2}$, no load	--	230	380	μA
I_{VIN2_Q}	Channel 2 Quiescent Supply Current	Channel 1 is ON, Channel 2 is OFF, $V_{BUS} = V_{IN1}$, no load	--	40	100	μA
		Channel 1 is OFF, Channel 2 is ON, $V_{BUS} = V_{IN2}$, no load	--	160	400	μA

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Electrical Characteristics (continued)

T_A = -20 °C to 85 °C, unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
RDS _{ON1}	Channel 1 ON resistance	T _A = 25 °C, V _{IN1} = 5 V ± 10%, V _{IN2} = 12 V ± 10%, V _{BUS} = V _{IN1} , I _{VBUS} = 200 mA	--	40	44	mΩ
		T _A = -20 °C to 85 °C, V _{IN1} = 5 V ± 10%, V _{IN2} = 12 V ± 10%, V _{BUS} = V _{IN1} , I _{VBUS} = 200mA	--	--	53	mΩ
RDS _{ON2}	Channel 2 ON resistance	T _A = 25 °C, V _{IN1} = 5 V ± 10%, V _{IN2} = 12 V ± 10%, V _{BUS} = V _{IN2} , I _{VBUS} = 200 mA	--	67	74	mΩ
		T _A = -20 °C to 85 °C, V _{IN1} = 5 V ± 10%, V _{IN2} = 12 V ± 10%, V _{BUS} = V _{IN2} , I _{VBUS} = 200 mA	--	--	88	mΩ
RDS _{ON[1,2]_SET} ²	RDS _{ON[1,2]} Setting Time	V _{IN1} = 5 V, V _{IN2} = 12 V, From V _{BUS} Starts to Ramp up from 0 V to RDS _{ON1} reaches it's nominal value	--	10	20	ms
		V _{IN1} = 5 V, V _{IN2} = 12 V, From V _{BUS} starts to Ramp Up from V _{IN1} to RDS _{ON2} reaches it's nominal value	--	12	24	ms
I _{VIN1_VBUS}	Current from VIN1 to VBUS	Continuous	--	--	3	A
I _{VIN2_VBUS}	Current from VIN2 to VBUS	Continuous	--	--	1.25	A
I _{ACL_VIN1}	Channel 1 Active Current Limit	V _{IN1} = 5 V, R _{ILIM1} = 20 kΩ	3.59	4.08	4.57	A
		R _{ILIM1} > 600 kΩ or ILIM1 pin open	--	0.52	1.0	A
		R _{ILIM1} < 2 kΩ or ILIM1 pin short to GND	--	0.52	1.0	A
I _{ACL_VIN2}	Channel 2 Active Current Limit	V _{IN2} = 12 V, R _{ILIM2} = 20 kΩ	1.67	1.9	2.13	A
		R _{ILIM2} > 600 kΩ or ILIM2 pin open	--	0.26	0.5	A
		R _{ILIM2} < 2 kΩ or ILIM2 pin short to GND	--	0.26	0.5	A
I _{SCP}	VBUS Short-Circuit Protection Threshold	VBUS Current when Short to GND, V _{IN1} = 5 V, V _{IN2} = 12 V, R _{ILIM1} = R _{ILIM2} = 20 kΩ, T _A = 25 °C, R _{SHORT} is adjusting until SCP protection is triggered.	--	8	--	A
I _{LIM_FOLD1} ¹	Current Limit Foldback Ratio for Channel 1	VBUS Current Limit Reduction Ratio from I _{ACL_VIN1} after Triggering VBUS Short Circuit Protection, V _{IN1} = 5 V, V _{IN2} = 12 V, R _{ILIM1} = R _{ILIM2} = 20 kΩ	4.6	6	7.1	
I _{LIM_FOLD2} ¹	Current Limit Foldback Ratio for Channel 2	VBUS Current Limit Reduction Ratio from I _{ACL_VIN2} after Triggering VBUS Short Circuit Protection, V _{IN1} = 5 V, V _{IN2} = 12 V, R _{ILIM1} = R _{ILIM2} = 20 kΩ	6.7	12	16.9	
T _{OCP_delay}	FLAG Assertion LOW Blanking Time / Switch Off Delay Under Active Current Limit Mode	From Active Current Limit Start to Switch Off, V _{IN1} = 5 V, V _{IN2} = 12 V, R _{ILIM1} = R _{ILIM2} = 20 kΩ	1.3	2	2.85	ms

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Electrical Characteristics (continued)

T_A = -20 °C to 85 °C, unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{Droop_VIN1→VIN2} ¹	Voltage Droop During Switchover from V _{IN1} to V _{IN2}	V _{IN1} = 5 V, V _{IN2} = 12 V, I _{VBUS} = 0 A to 0.35 A, C _{LOAD} = 20 μF	--	--	309	mV
		V _{IN1} = 5 V, V _{IN2} = 12 V, I _{VBUS} = 0.35 A to 1 A, C _{LOAD} = 20 μF	--	11	60	mV
V _{Droop_VIN2→VIN1} ¹	Voltage Droop During Switchover from V _{IN2} to V _{IN1}	V _{IN1} = 5 V, V _{IN2} = 12 V, I _{VBUS} = 1.5 A, C _{LOAD} = 20 μF	--	141	200	mV
I _{VIN1_Reverse} ¹	I _{VIN1} Reverse Current During Switchover from V _{IN1} to V _{IN2}	V _{IN1} = 5 V, V _{IN2} = 12 V, I _{VBUS} = 0 A to 1 A, C _{LOAD} = 20 μF	--	0.05	0.3	A
V _{RCB1_T} ²	Channel 1 Reverse Current Blocking (RCB) Detection Threshold	V _{BUS} > V _{IN1} , Voltage Difference between VIN1 and V _{BUS} , V _{IN1} = 5 V	--	15	--	mV
V _{RCB1_R} ²	Channel 1 RCB Release Voltage	V _{BUS} > V _{IN1} , Voltage Difference between VIN1 and V _{BUS} , V _{IN1} = 5 V	--	0	--	mV
T _{RCB1_T} ¹	Channel 1 RCB Trigger Response Time	V _{BUS} > V _{IN1} , from V _{BUS} > V _{IN1} + V _{RCB1_T} to V _{IN1} Reverse Current Starts to Decrease, V _{IN1} = 5 V, no C _{LOAD} , no R _{LOAD}	--	1	2	μs
T _{RCB1_R} ¹	Channel 1 RCB Release Response Time	V _{BUS} < V _{IN1} , from V _{BUS} < V _{IN1} - V _{RCB1_R} to Channel 1 Turn ON, V _{IN1} = 5 V, no C _{LOAD} , no R _{LOAD}	--	1	3.5	μs
T _{RCB1_R} ²	Channel 1 RCB Release Response Time During Switchover from V _{IN2} to V _{IN1}	From V _{BUS} < V _{IN1} - V _{RCB1_R} to Channel 1 Turn ON, V _{IN1} = 5 V, V _{IN2} = 12 V, C _{VBUS} = 20 μF, I _{VBUS} = 1.5 A	--	0.7	2.1	μs
V _{IN1_UVLO}	Channel 1 Under-Voltage Lockout Threshold	V _{IN1} Rising	3.6	3.8	4.0	V
V _{IN1_UVLO_HYS}	Channel 1 Under-Voltage Lockout Hysteresis	V _{IN1} Falling	0.09	0.2	0.31	V
V _{IN2_UVLO}	Channel 2 Under-Voltage Lockout Threshold	V _{IN2} Rising	3.6	3.8	4.0	V
V _{IN2_UVLO_HYS}	Channel 2 Under-Voltage Lockout Hysteresis	V _{IN2} Falling	0.09	0.2	0.31	V
V _{IN1_OVP}	Channel 1 Over-Voltage Protection Threshold	V _{IN1} Rising	5.5	5.8	6.2	V
V _{IN2_OVP}	Channel 2 Over-Voltage Protection Threshold	V _{IN2} Rising	13.2	13.9	14.5	V
T _{OVP} ¹	OVP Response Time	From V _{IN1} / V _{IN2} > V _{IN[1,2]_OVP} Threshold to V _{BUS} Shutdown, V _{IN1} = 5 V, V _{IN2} = 12 V; V _{IN1} step up from 5 V to 6.5 V or V _{IN2} step up from 12 V to 15 V	--	10	20	μs
THERM _{ON}	Thermal Protection Shutdown Threshold	Junction Temperature Rising	--	140	--	°C
THERM _{HYS} ²	Thermal Protection Hysteresis	Junction Temperature Falling	--	20	--	°C
T _{ON_Delay1}	Channel 1 Turn On Delay Time	From EN1 > EN1_V _{IH} to V _{BUS} Starts to Ramp Up from 0 V, R _{LOAD} = 5 Ω, C _{LOAD} = 20 μF or 490 μF	0.3	0.8	1.5	ms

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Electrical Characteristics (continued)

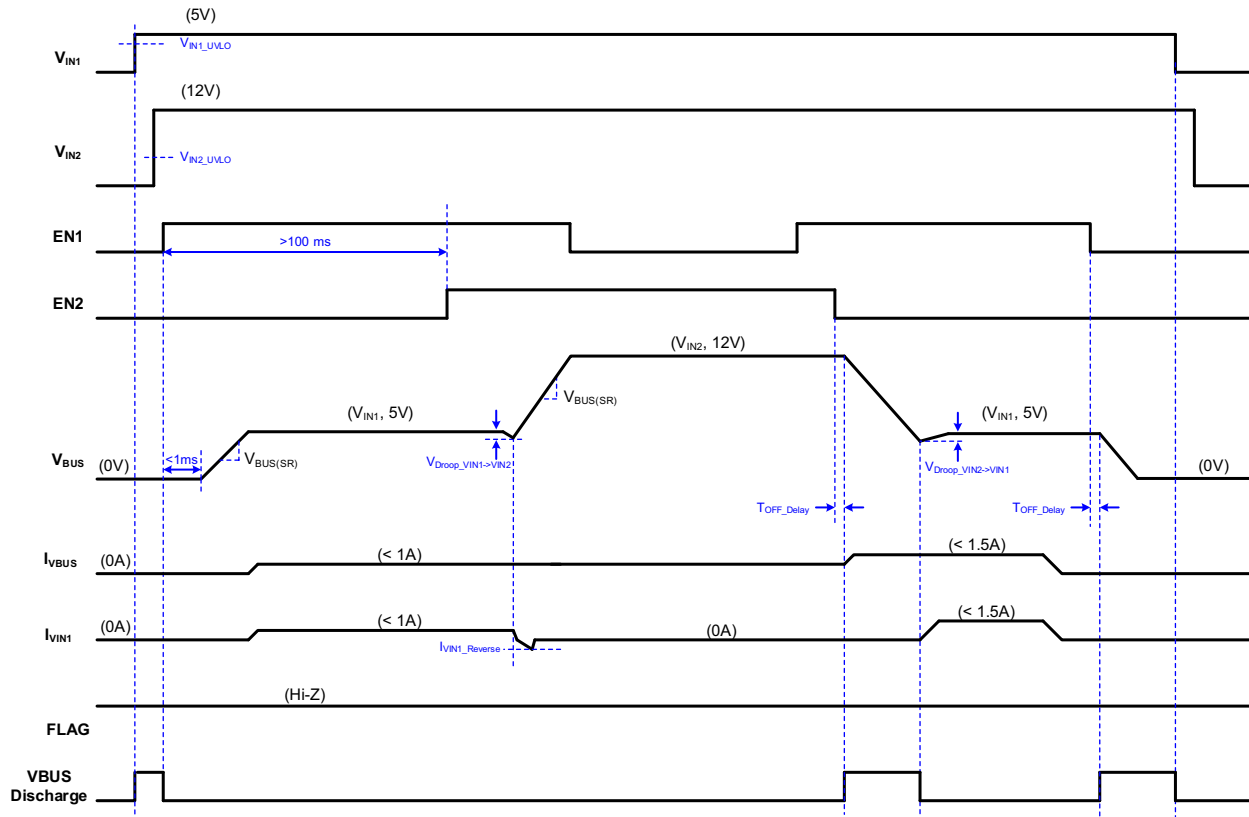
T_A = -20 °C to 85 °C, unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T _{ON_Delay2} ²	Channel 2 Turn On Delay Time	From EN2 > EN2_V _{IH} to VIN2's Internal Ramp Starts to Ramp Up from 0 V	0	0.1	0.5	ms
V _{BUS(SR)}	V _{BUS} Slew Rate	V _{BUS} Rise from 0 V to V _{IN1} , 10% to 90%, R _{LOAD} = 5 Ω, C _{LOAD} = 20 μF or 490 μF	0.6	0.9	1.3	V/ms
		V _{BUS} Rise from V _{IN1} to V _{IN2} , 10% to 90%, V _{IN2} > 9 V, R _{LOAD} = 12 Ω, C _{LOAD} = 20 μF or 490 μF	0.99	1.4	1.9	V/ms
T _{OFF_Delay}	OFF Delay Time	From EN1 < EN1_V _{IL} to V _{BUS} Starts Fall from V _{IN1} , R _{LOAD} = 5 Ω, C _{LOAD} = 20 μF or 490 μF	--	4.5	10	μs
R _{DISCHRG}	VBUS Discharge Resistance	For V _{BUS} = 12 V During Switchover from V _{IN2} = 12 V to V _{IN1} = 5 V, EN1 = High, EN2 = High to Low	1.1	1.3	1.4	kΩ
		For V _{BUS} = 8.5 V During Switchover from V _{IN2} = 12 V to V _{IN1} = 5 V, EN1 = High, EN2 = High to Low	0.8	1.0	1.3	kΩ
		For V _{BUS} = 5.1 V During Switchover from V _{IN2} = 12 V to V _{IN1} = 5 V, EN1 = High, EN2 = High to Low	0.7	0.8	0.9	kΩ
EN[1,2]_V _{IH}	EN[1,2] Input High Voltage	V _{IN1} = 4 V ~ 5.5 V	1.5	--	--	V
EN[1,2]_V _{IL}	EN[1,2] Input Low Voltage	V _{IN1} = 4 V ~ 5.5 V	--	--	0.5	V
V _{FLAG_LOW}	FLAG Pin Output Logic Low Voltage	V _{IN1} = 5 V, FLAG Pin Sink Current = 5 mA	--	--	0.3	V
I _{FLAG_LEAK}	Leakage Current into FLAG Pin	V _{IN1} = 5 V, FLAG Pin = High	--	--	1	μA
Notes: 1. Guaranteed by Characterization 2. Guaranteed by Design						

Timing Diagrams

Typical Power On and Power Off Operation

Power On $\rightarrow V_{BUS} = V_{IN1} \rightarrow V_{BUS} = V_{IN2} \rightarrow V_{BUS} = V_{IN1} \rightarrow$ Power Off

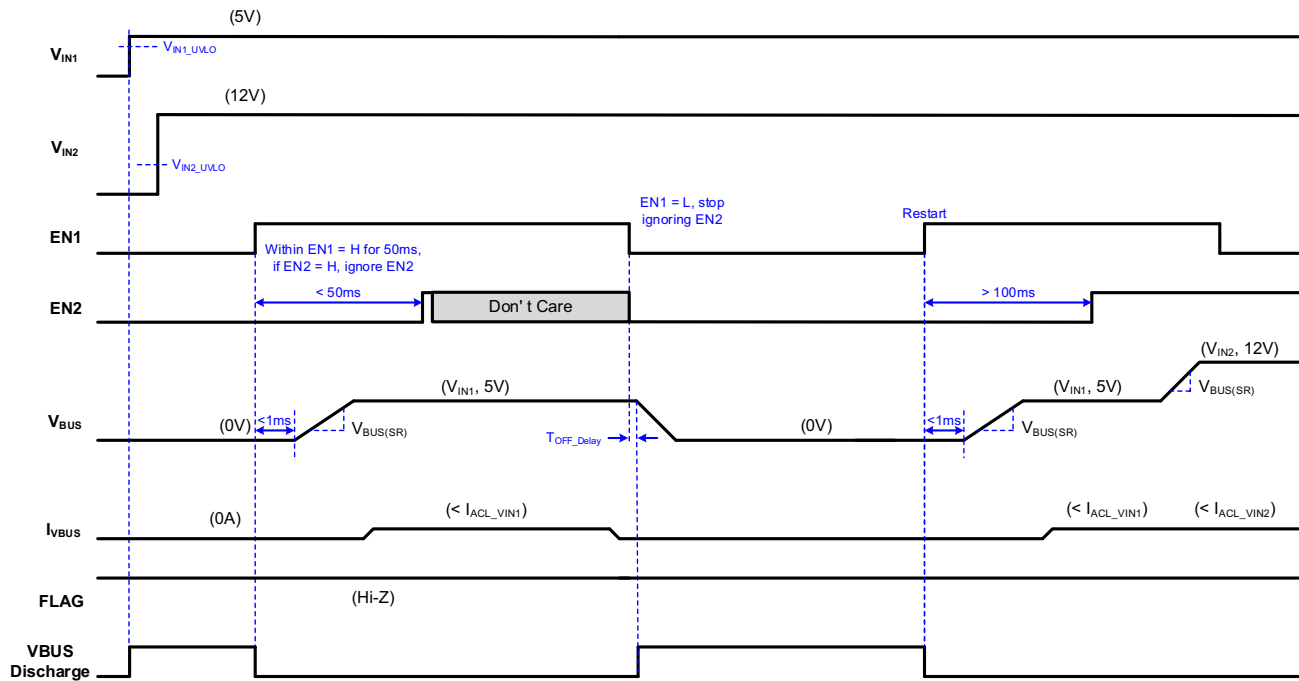


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Typical Power On and Power Off Operation if EN2 is Applied Sooner than 100 ms After EN1

Power On -> $V_{BUS} = V_{IN1}$ -> Ignoring EN2, $V_{BUS} = V_{IN1}$ -> Power Off and Release Ignoring EN2 -> Restart

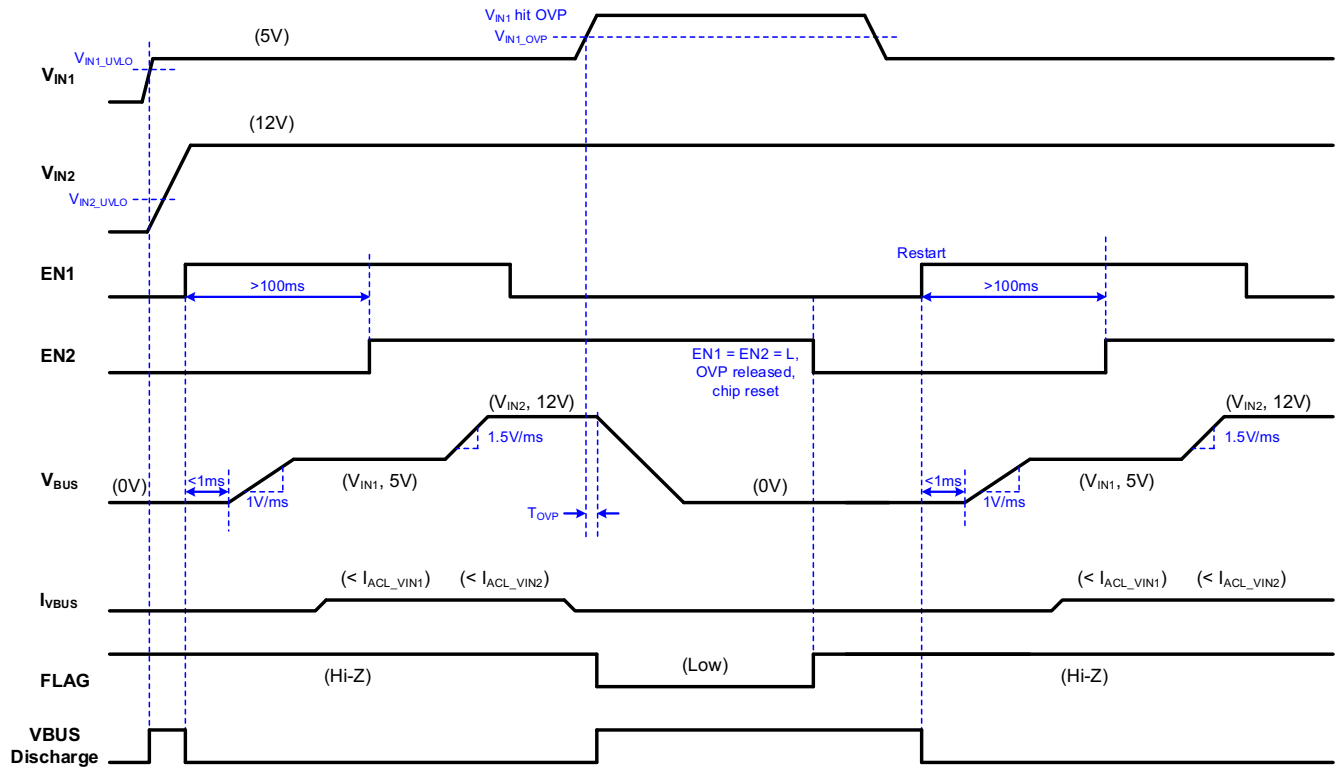


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Dual Input Single Output 12 V Power Multiplexer

Typical Overvoltage Protection Operation on Channel 1

Power On -> $V_{BUS} = V_{IN1}$ -> $V_{BUS} = V_{IN2}$ -> $V_{IN1} \geq V_{IN1_OVP}$ -> Latch Off -> Released by $EN1 = EN2 = L$ -> Restart

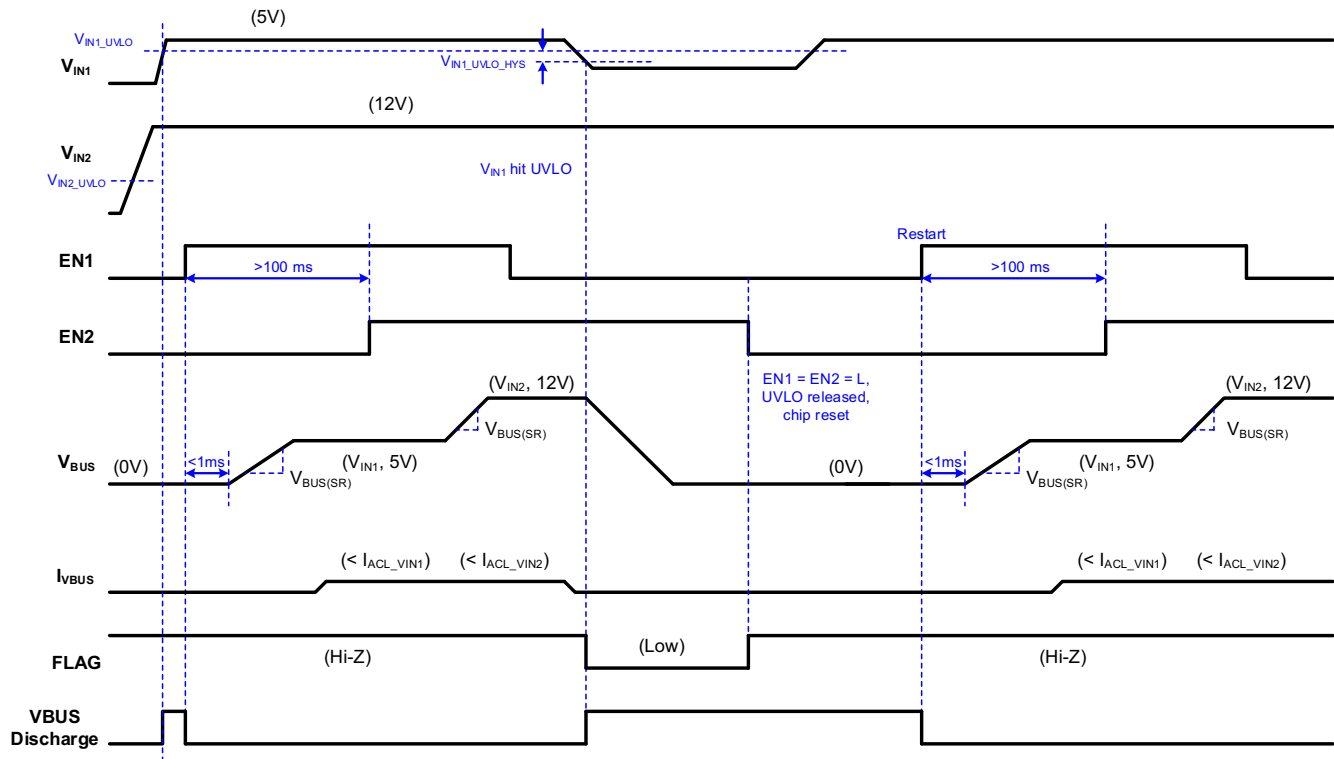


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Typical Undervoltage Lockout Operation on Channel 1

Power On -> $V_{BUS} = V_{IN1}$ -> $V_{BUS} = V_{IN2}$ -> $V_{IN1} \leq V_{IN1_UVLO}$ -> Latch Off -> Released by $EN1 = EN2 = L$ -> Restart



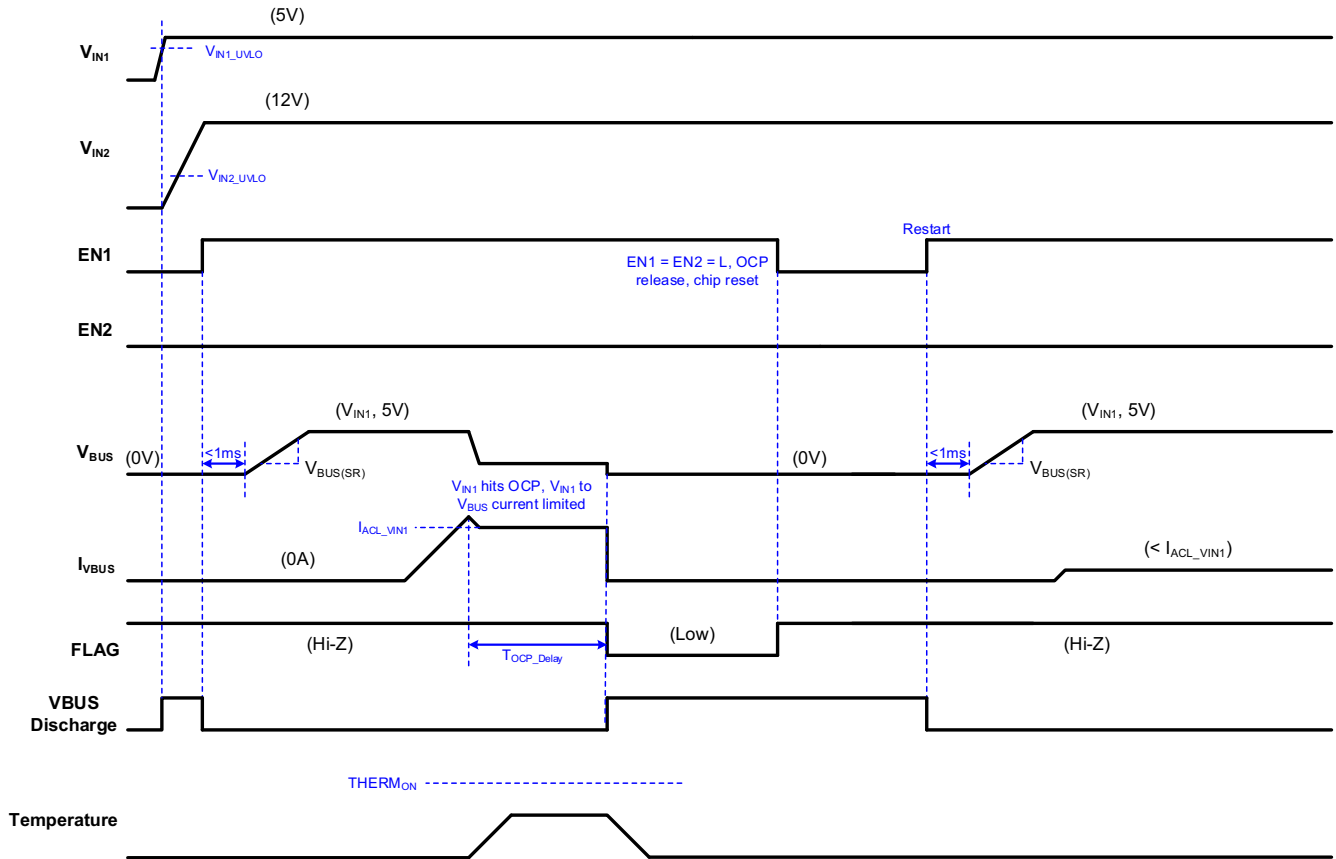
Note: Similar behavior is expected for Channel 2

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Typical Active Current Limit Protection Operation on Channel 1

Power On -> $V_{BUS} = V_{IN1}$ -> $I_{VBUS} \geq I_{ACL_VIN1}$ -> Latch Off -> Released by $EN1 = EN2 = L$ -> Restart

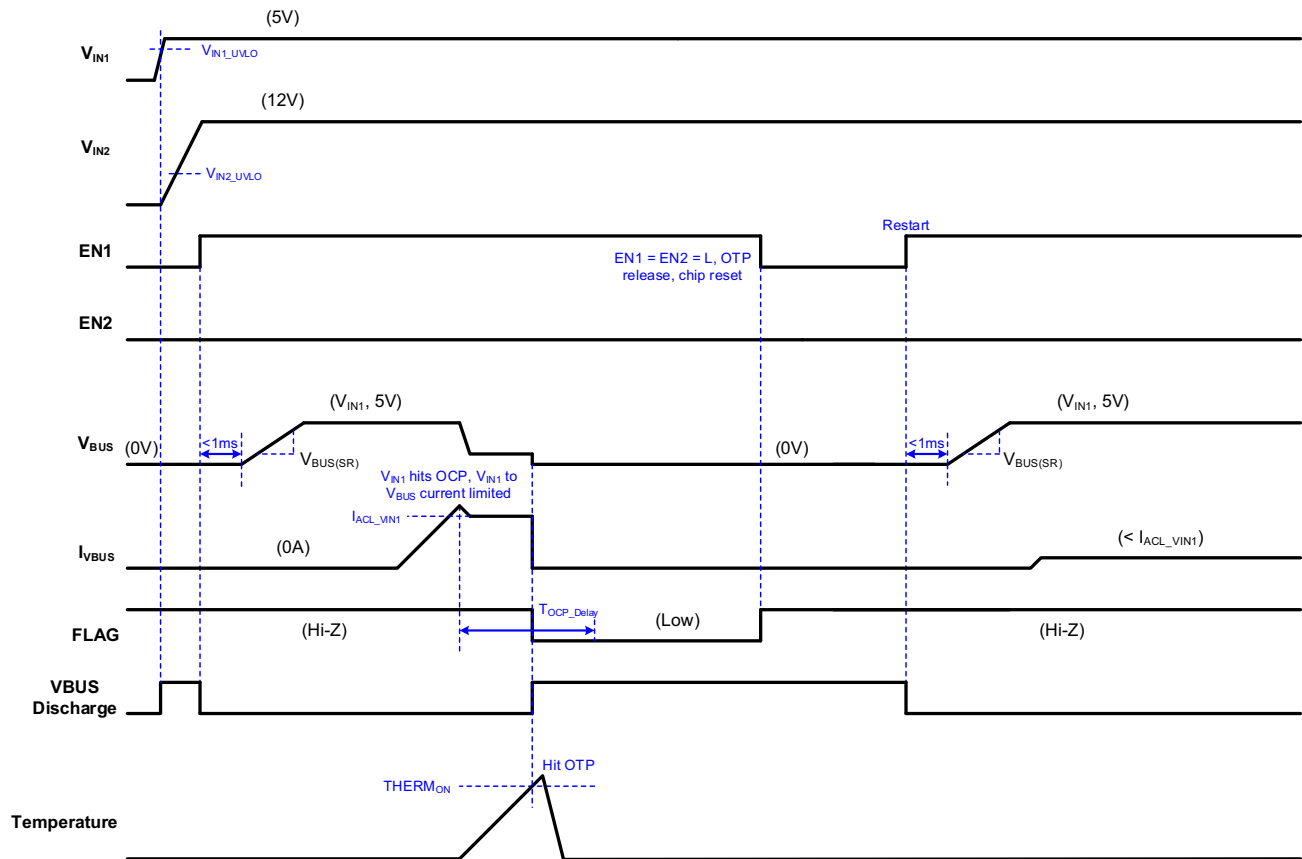


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Dual Input Single Output 12 V Power Multiplexer

Typical Active Current Limit + Overtemperature Protection Operation on Channel 1

Power On $\rightarrow V_{BUS} = V_{IN1} \rightarrow I_{VBUS} \geq I_{ACL_VIN1} \rightarrow T_J \geq THERM_{ON} \rightarrow$ Latch Off \rightarrow Released by $EN1 = EN2 = L \rightarrow$ Restart

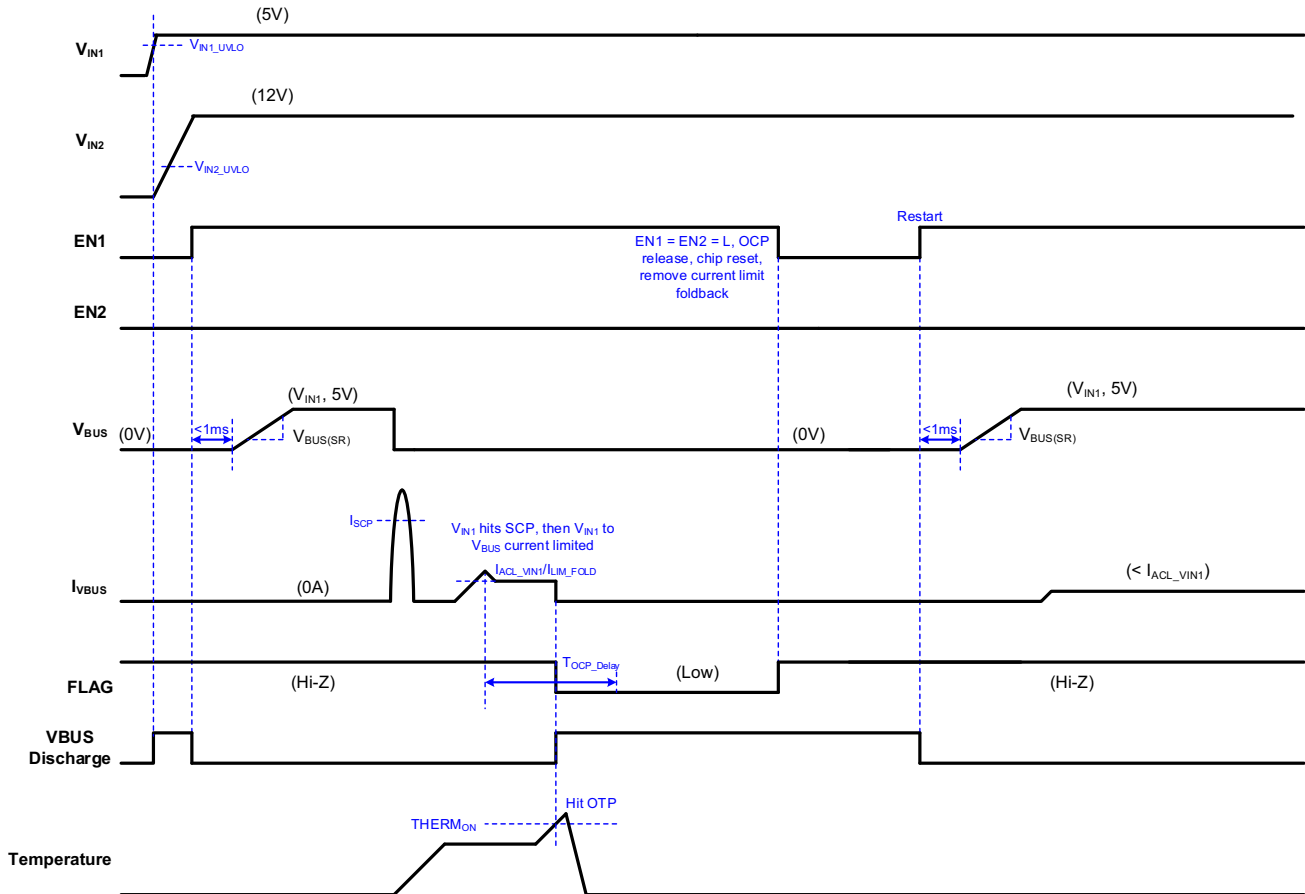


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Typical Short Circuit Protection + Overtemperature Protection Operation on Channel 1

Power On -> $V_{BUS} = V_{IN1}$ -> $I_{V_{BUS}} \geq I_{SCP}$ -> $T_J \geq THERM_{ON}$ -> Latch Off -> Released by $EN1 = EN2 = L$ -> Restart



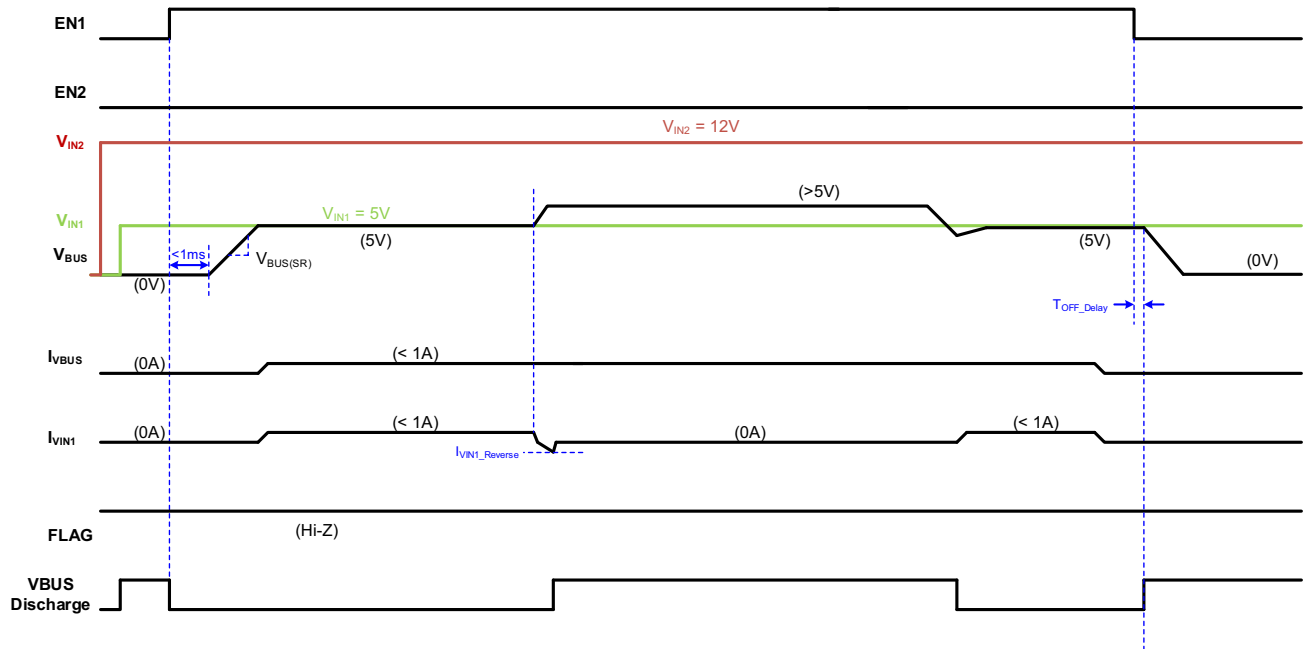
Note: Similar behavior is expected for Channel 2

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Typical Reverse Current Blocking Operation on Channel 1

Power On $\rightarrow V_{BUS} = V_{IN1} \rightarrow V_{BUS} \geq V_{IN1}$ is applied \rightarrow Released when V_{BUS} back to Normal

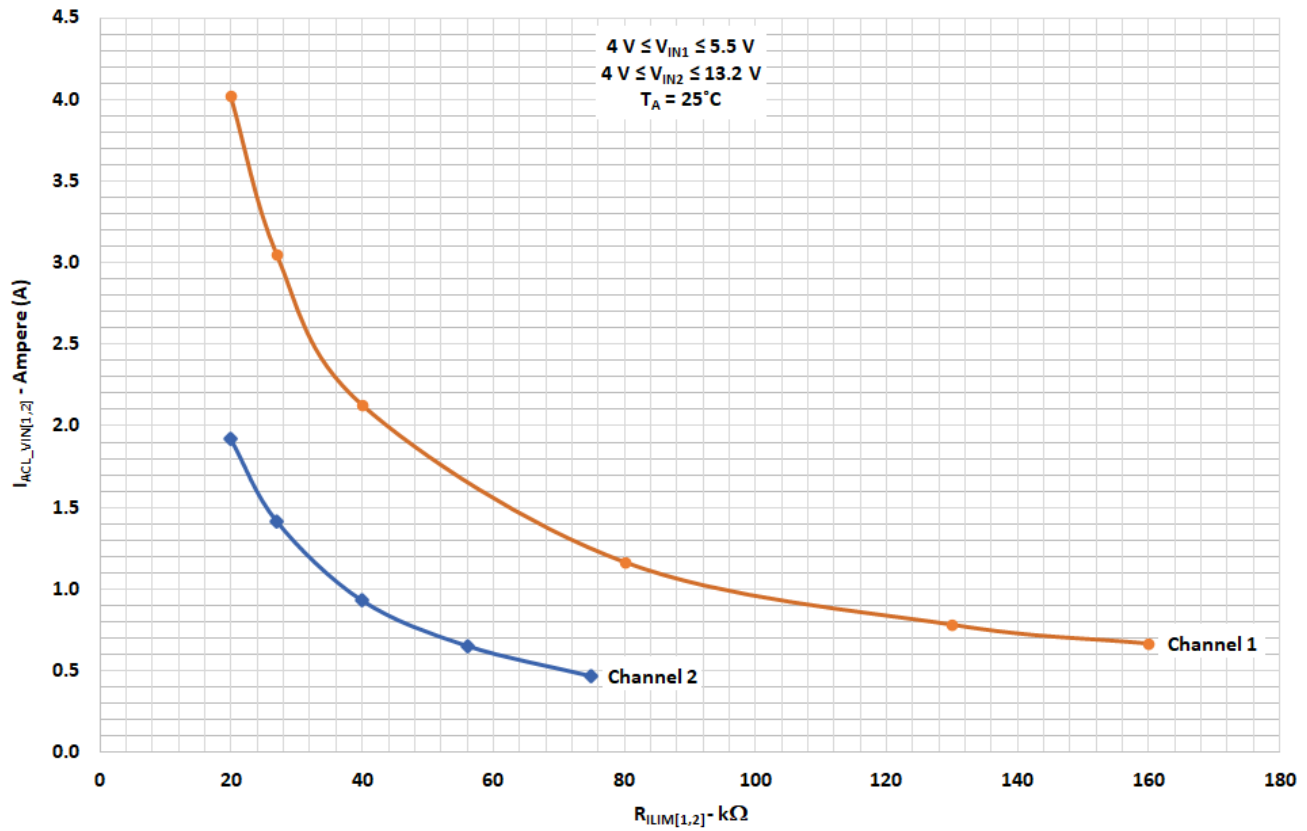


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Typical Performance Characteristics

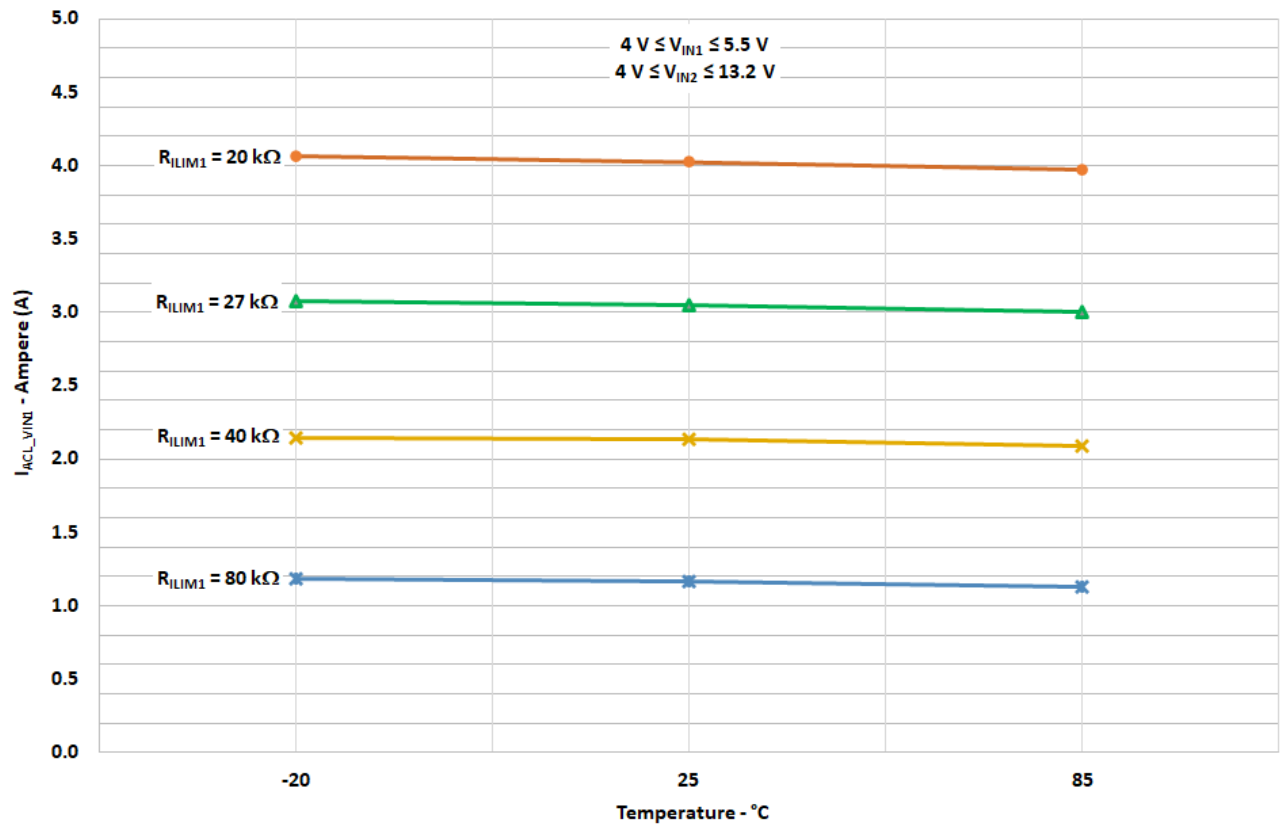
$I_{ACL_VIN[1,2]}$ vs. $R_{ILIM[1,2]}$, and $V_{IN[1,2]}$



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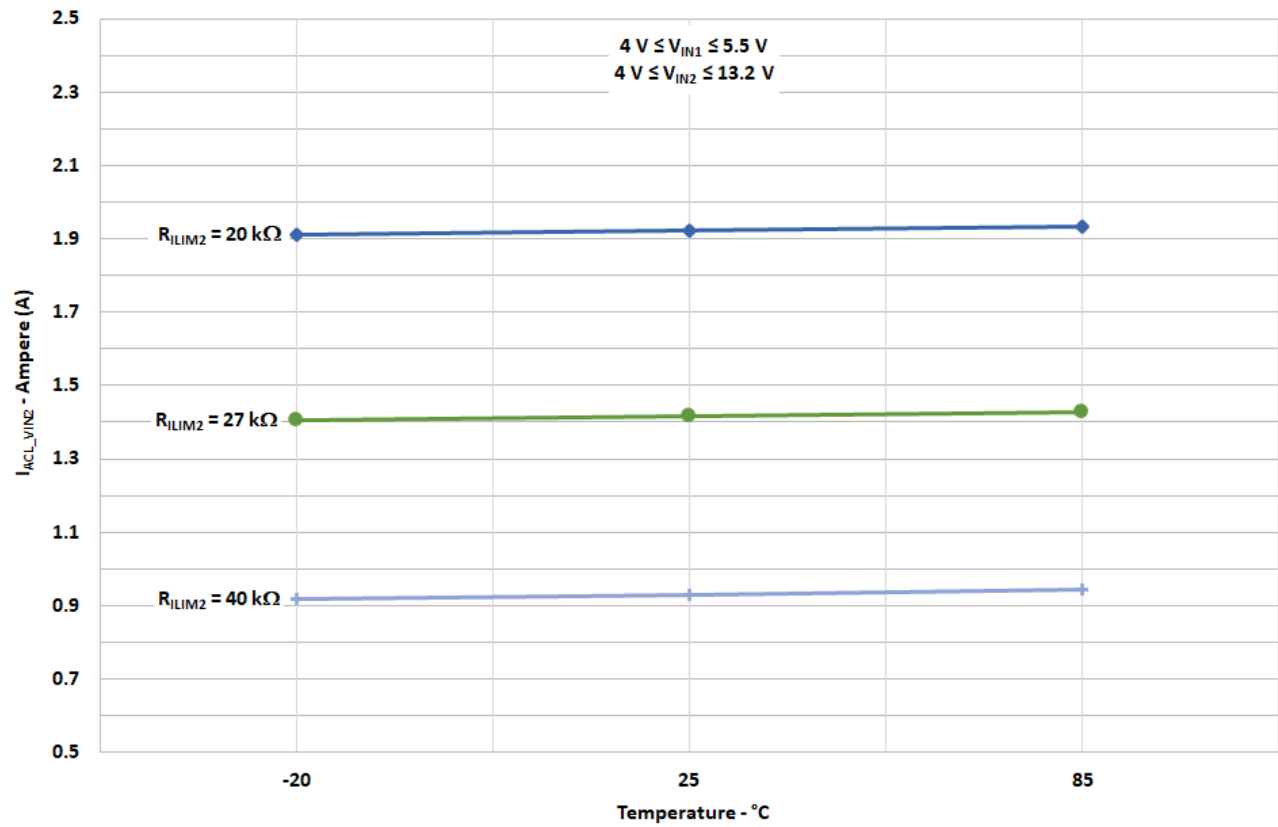
I_{ACL_VIN1} vs. Temperature, $V_{IN[1,2]}$, and R_{ILIM1}



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I_{ACL_VIN2} vs. Temperature, $V_{IN[1,2]}$, and R_{ILIM2}



Typical Turn ON Operation Waveform

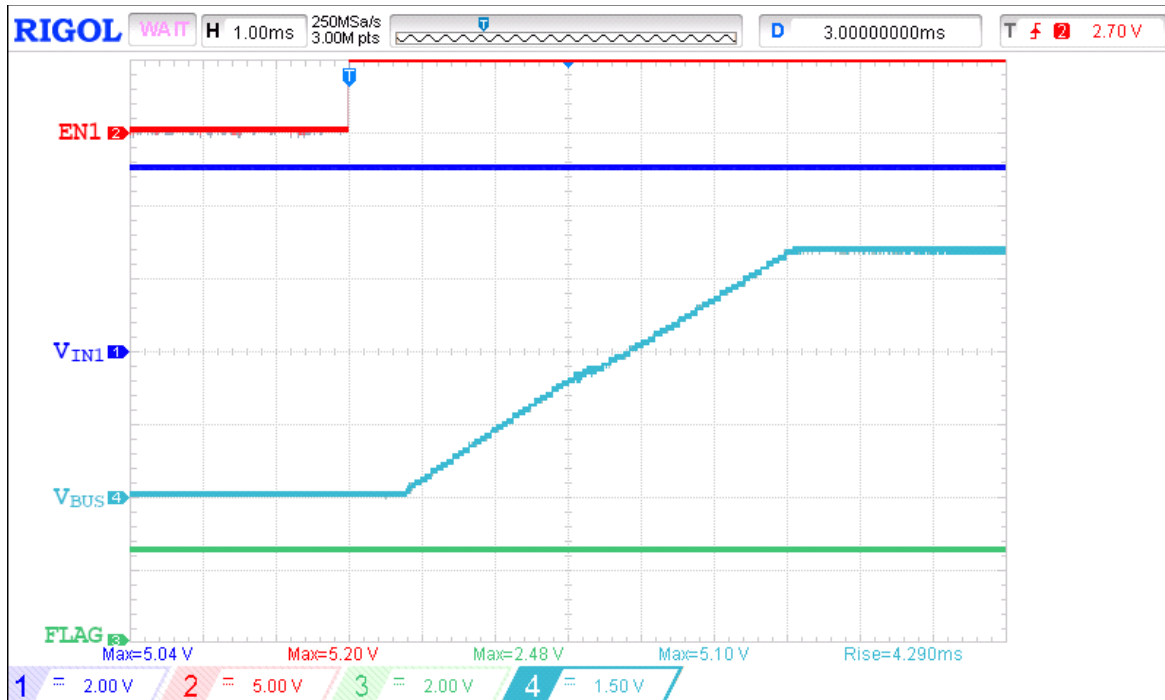


Figure 1. Typical Turn ON operation waveform for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{Low} \rightarrow \text{High}$, $EN2 = \text{Low}$, $R_{LOAD} = 12\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

Typical Switchover Operation Waveforms

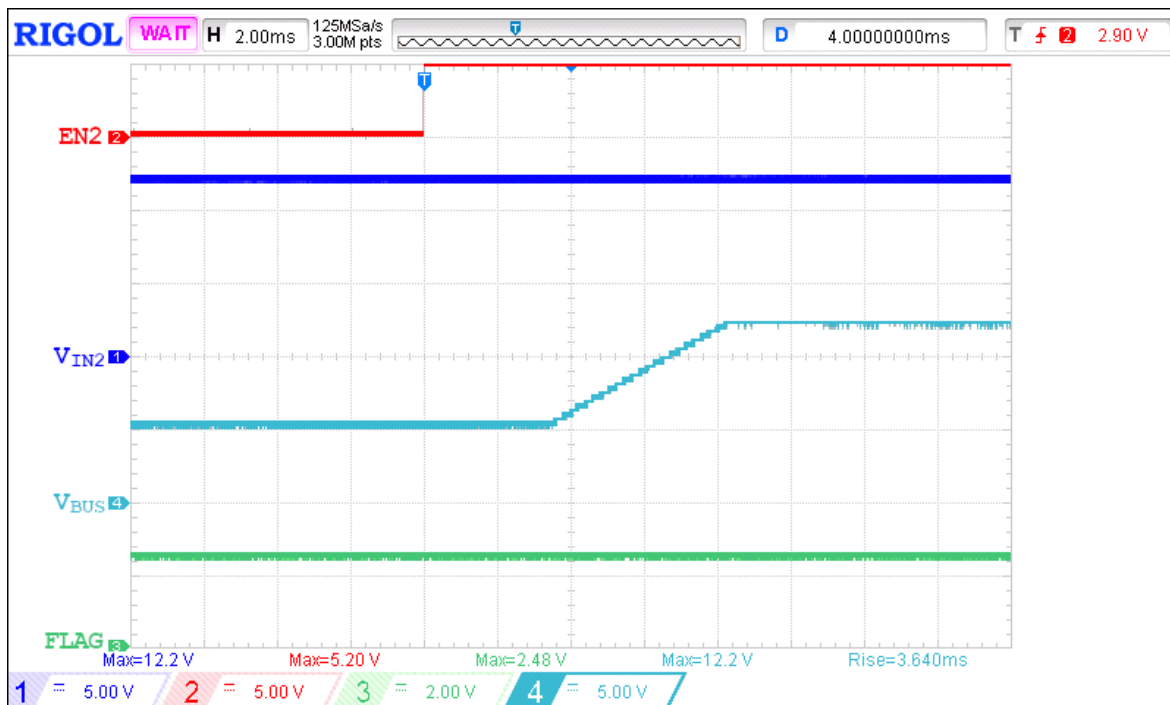


Figure 2. Switchover operation waveform for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High}$, $EN2 = \text{Low} \rightarrow \text{High}$, $R_{LOAD} = 12\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

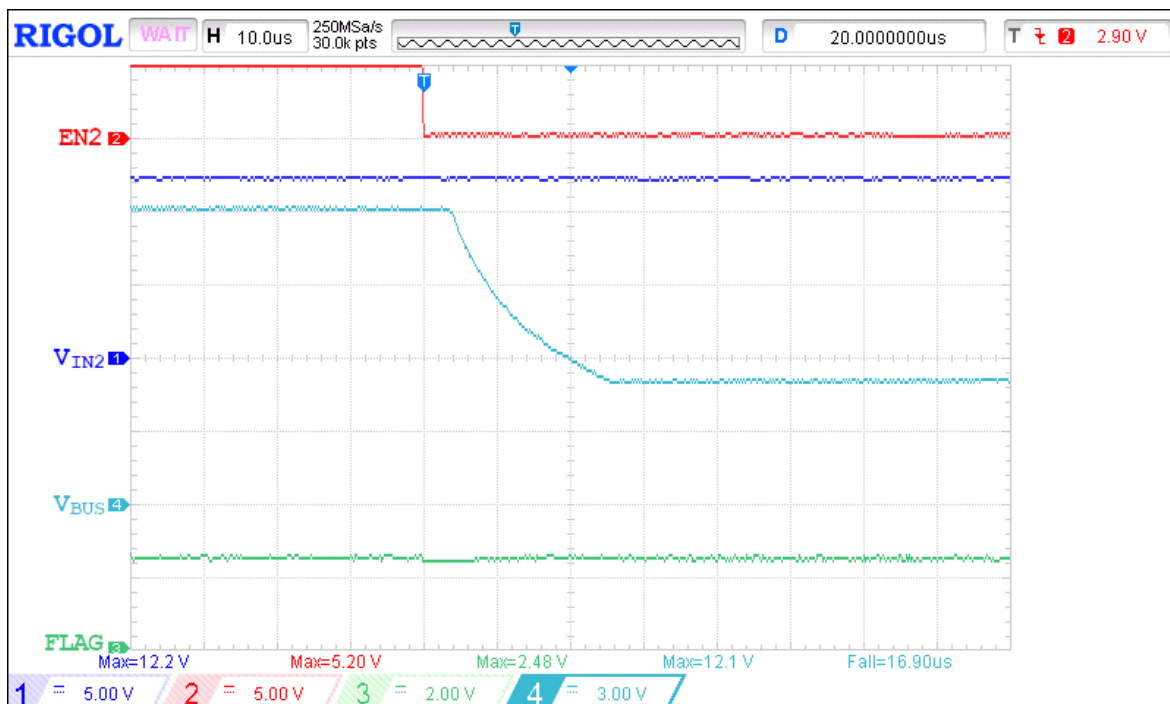


Figure 3. Switchover operation waveform for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High}$, $EN2 = \text{High} \rightarrow \text{Low}$, $R_{LOAD} = 7.8\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

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Dual Input Single Output 12 V Power Multiplexer

Typical Turn OFF Operation Waveforms

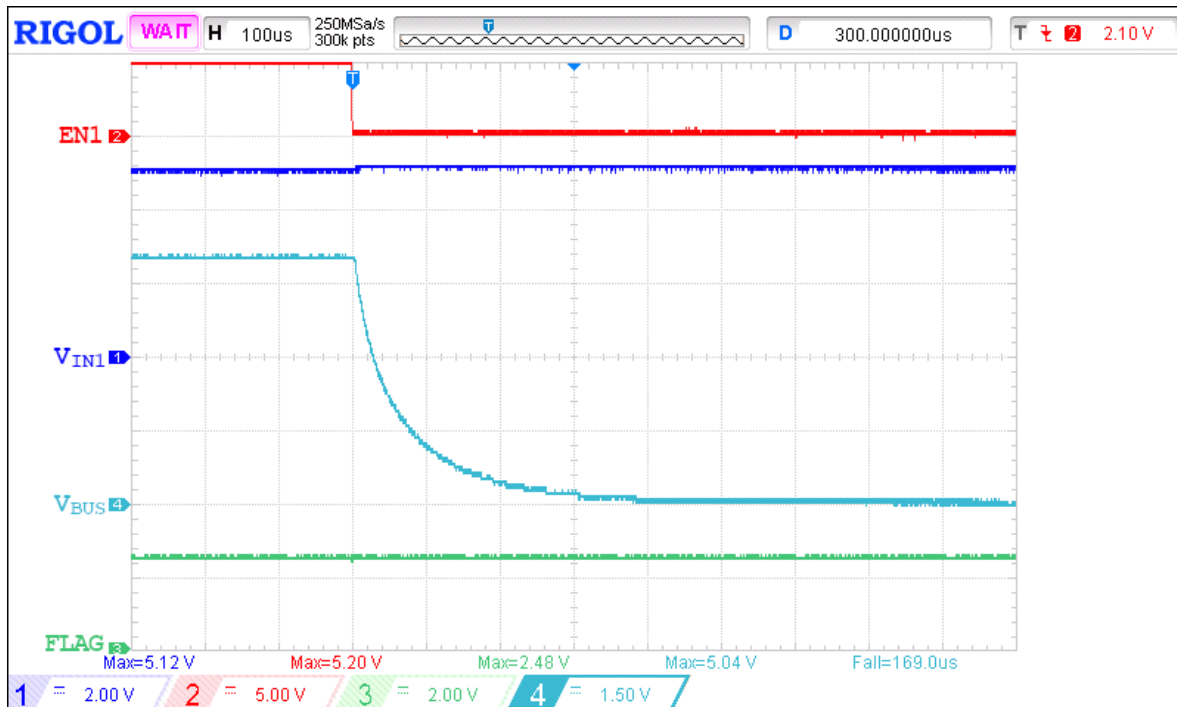


Figure 4. Turn OFF operation waveform for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High} \rightarrow \text{Low}$, $EN2 = \text{Low}$, $R_{LOAD} = 5\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

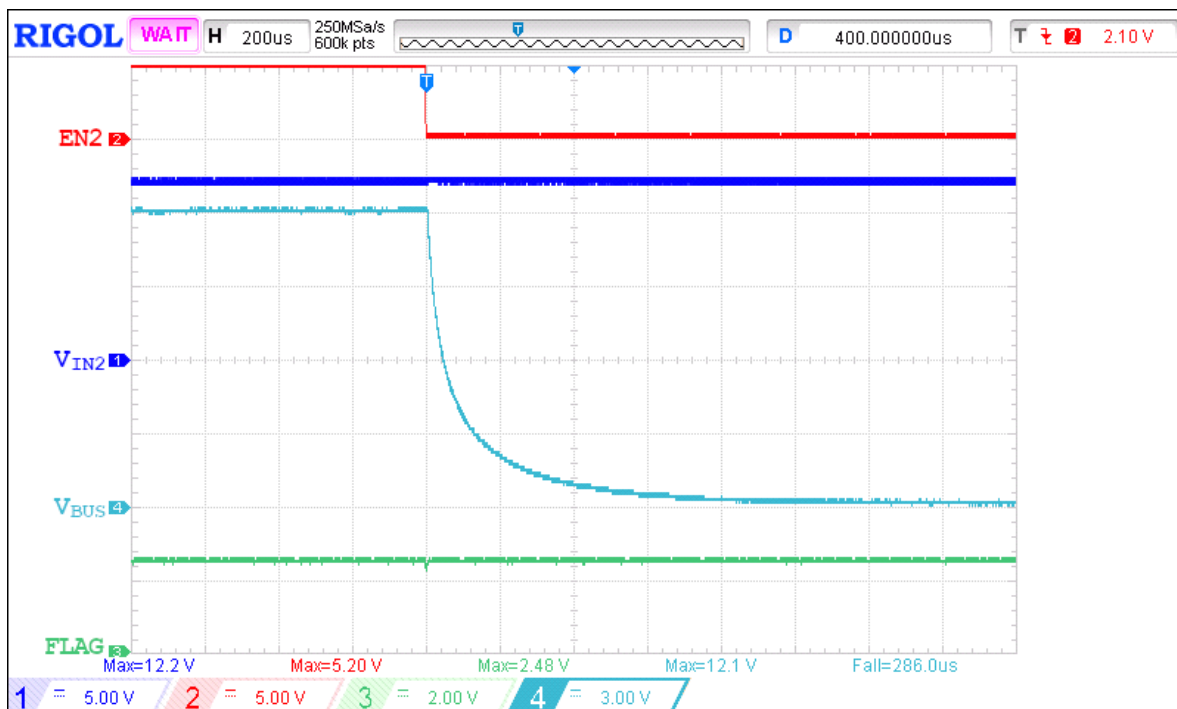


Figure 5. Turn OFF operation waveform for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{Low}$, $EN2 = \text{High} \rightarrow \text{Low}$, $R_{LOAD} = 12\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

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Active Current Limit Operation Waveforms

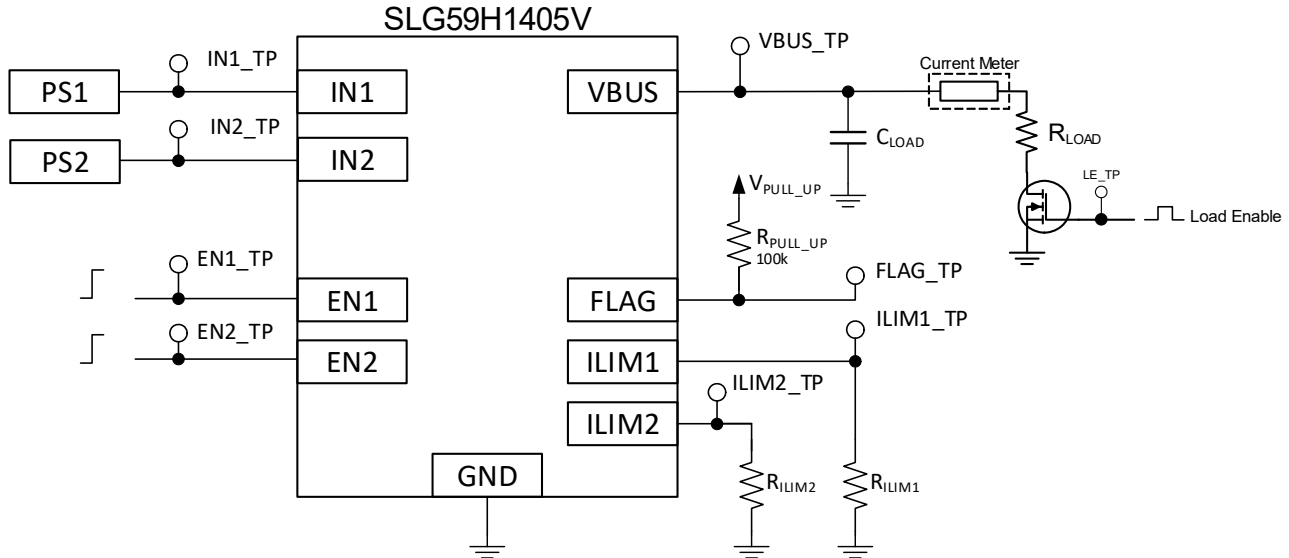


Figure 6. Test setup for Active Current Limit operations

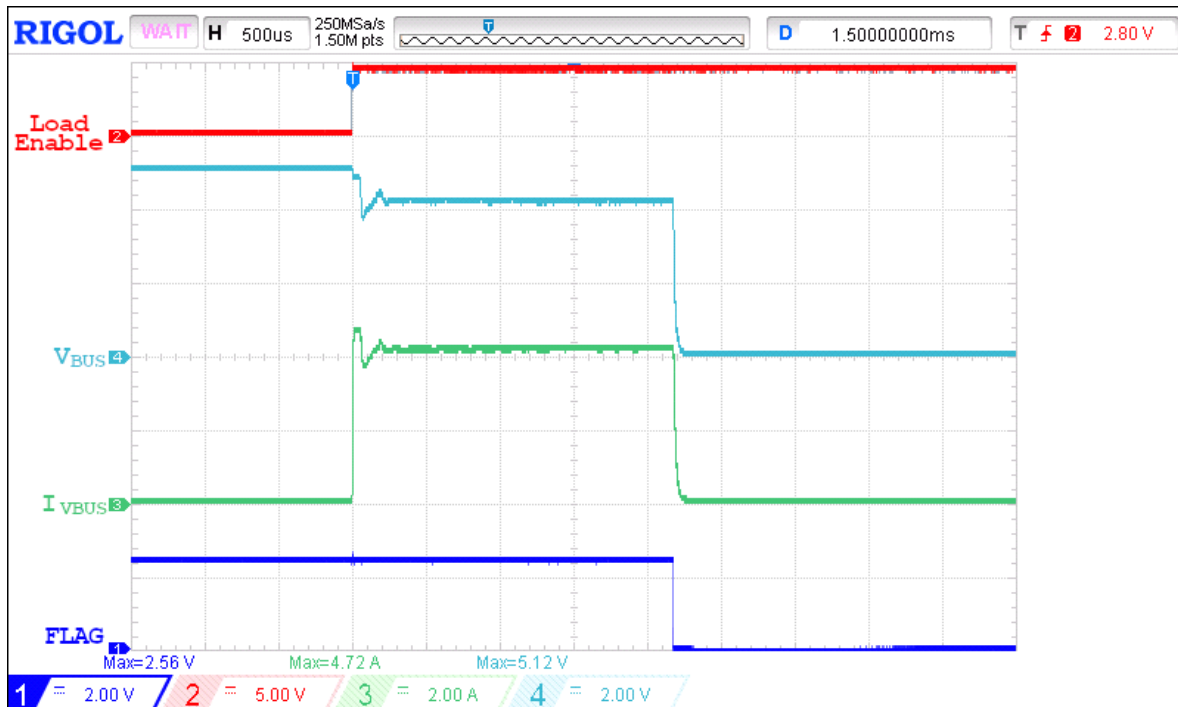


Figure 7. Active Current Limit operation waveform for Channel 1 for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High}$, $EN2 = \text{Low}$, $R_{LOAD} = 1\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

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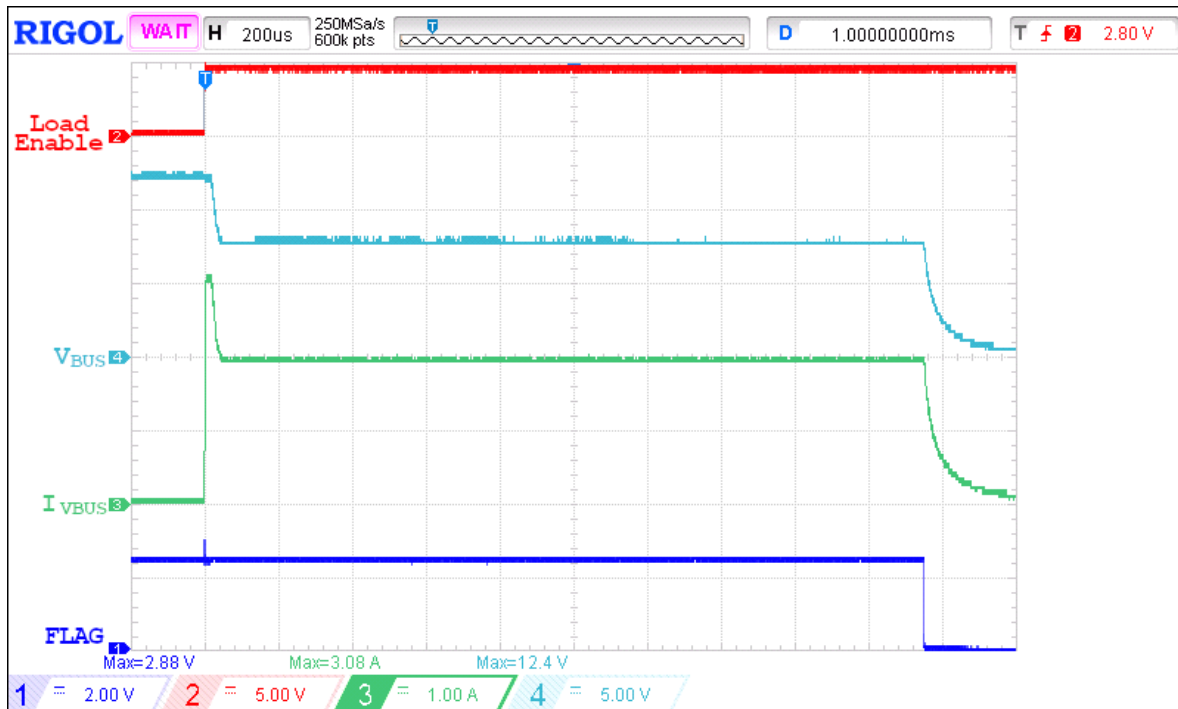


Figure 8. Active Current Limit operation waveform for Channel 2 for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High}$, $EN2 = \text{Low}$, $R_{LOAD} = 3.9\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

Short Circuit Protection Operation Waveforms

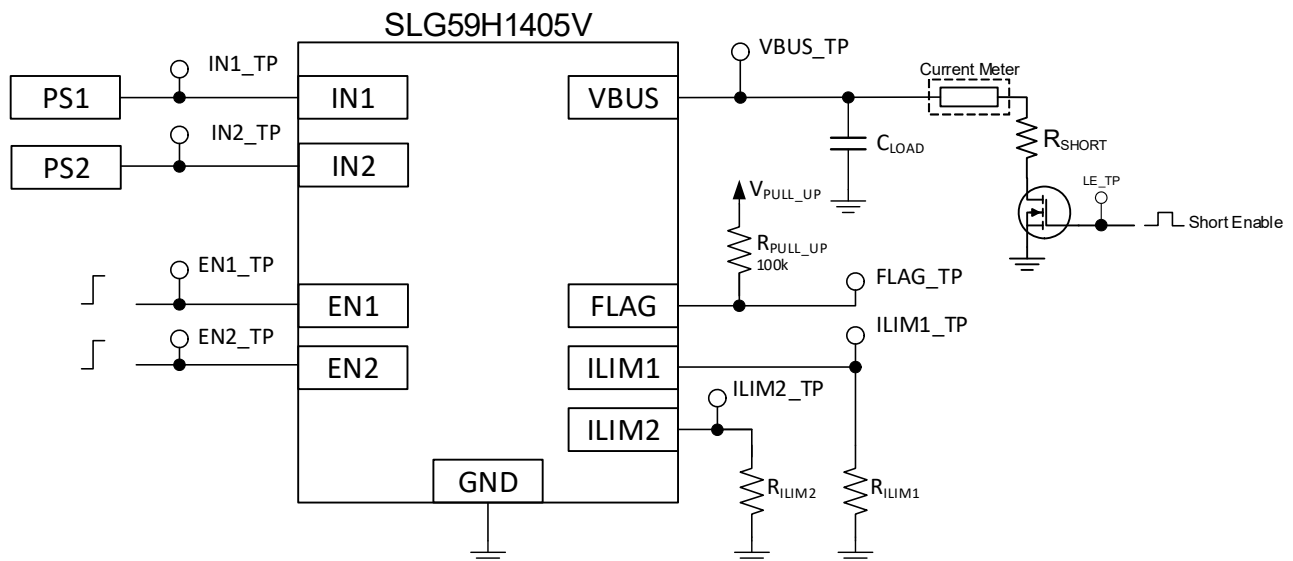


Figure 9. Test setup for Short Circuit Protection operations

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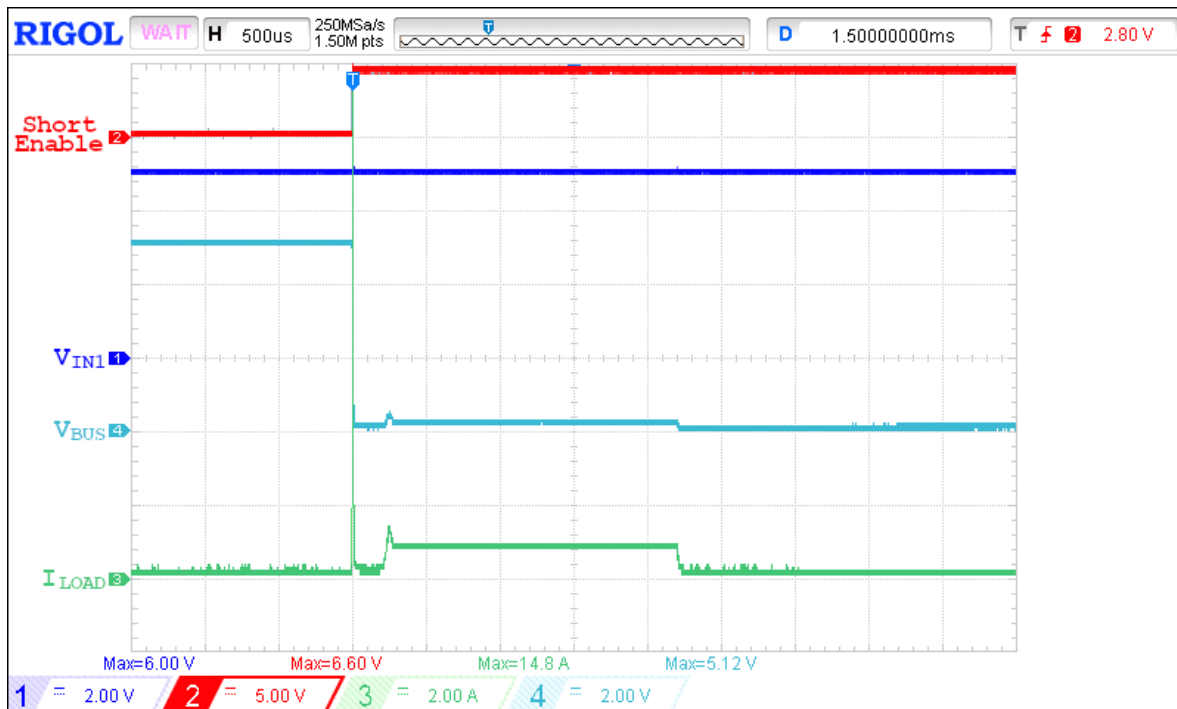


Figure 10. Short Circuit Protection operation waveform for Channel 1 for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High}$, $EN2 = \text{Low}$, $R_{LOAD} = 0.25\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

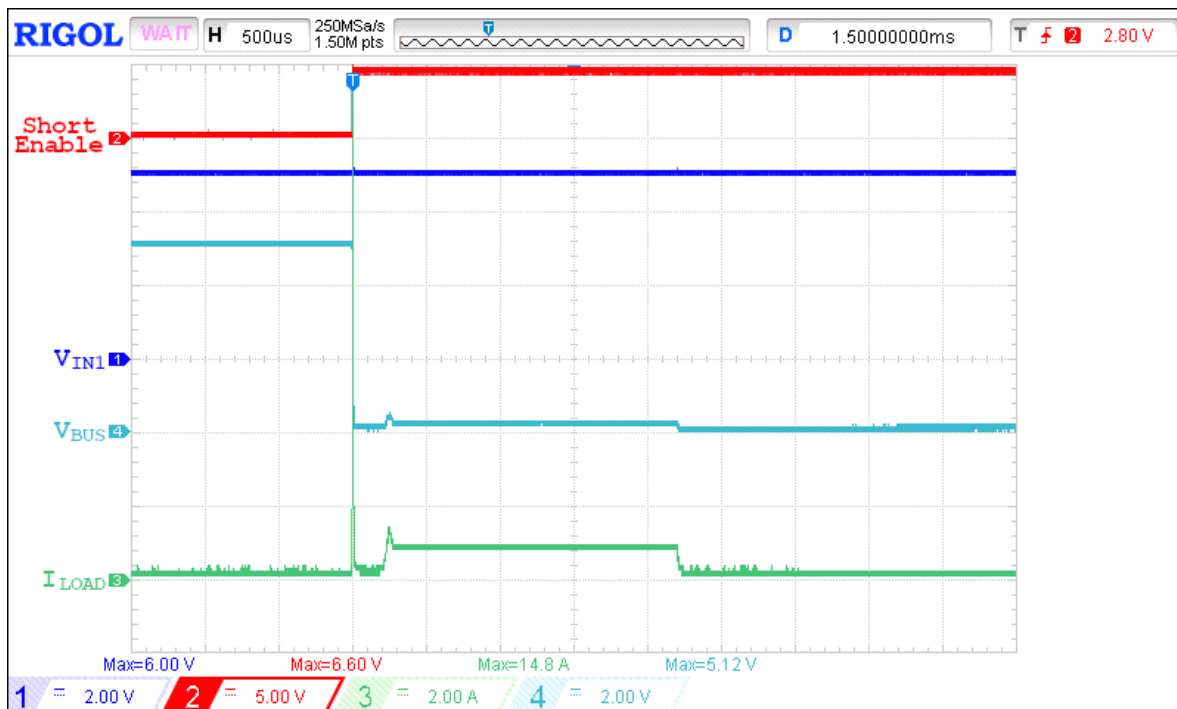


Figure 11. Short Circuit Protection operation waveform for Channel 2 for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{Low}$, $EN2 = \text{High}$, $R_{LOAD} = 0.75\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

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Over-voltage Protection Operation Waveforms

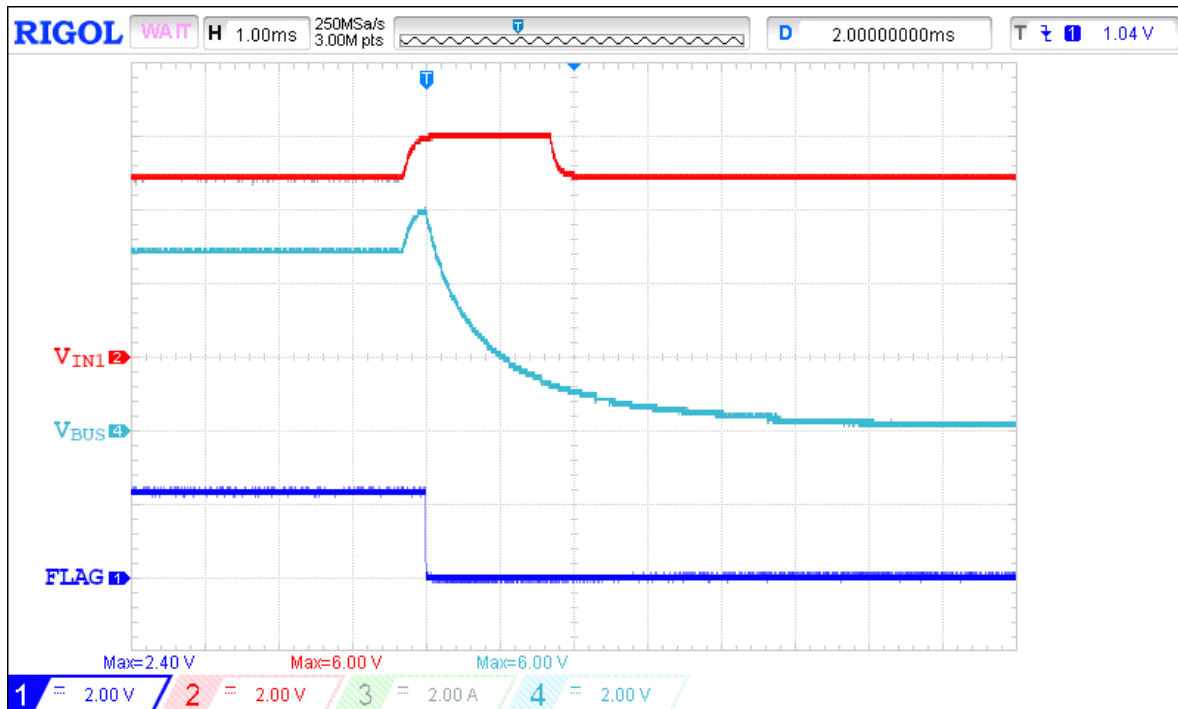


Figure 12. Over-voltage Protection operation waveform for Channel 1 for $V_{IN1} = 5\text{ V}$ step-up to 6 V , $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High} \rightarrow \text{Low}$, $EN2 = \text{Low}$, $R_{LOAD} = 5\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

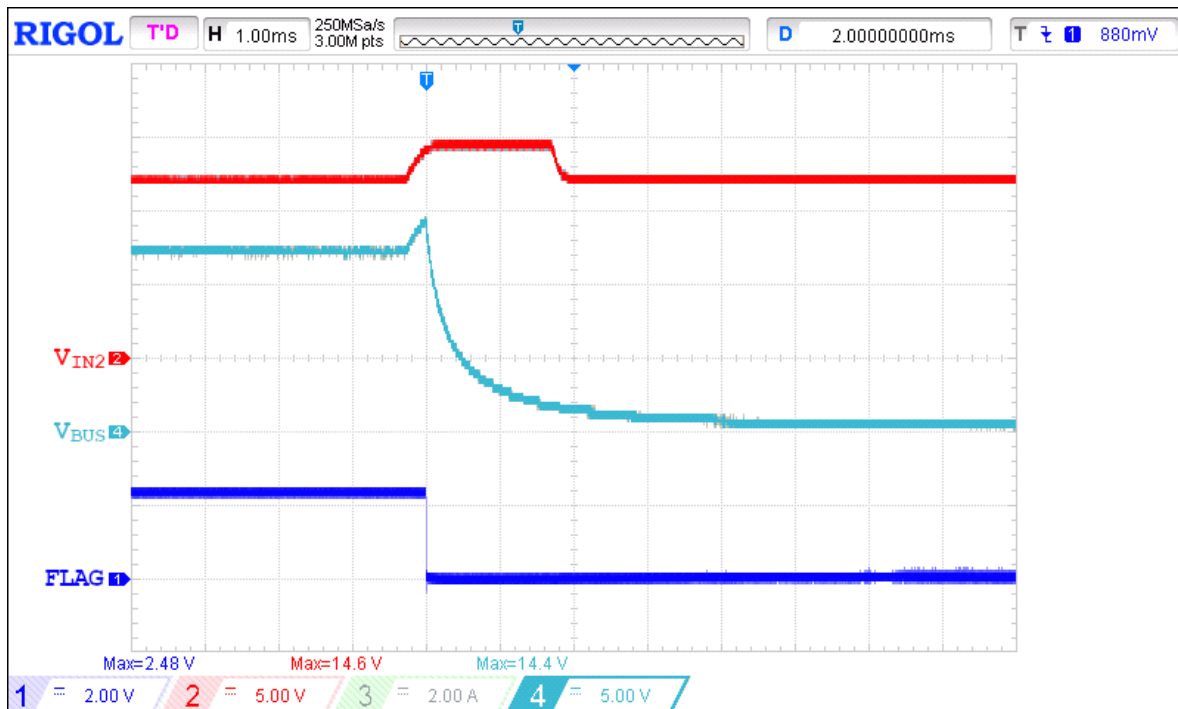


Figure 13. Over-voltage Protection operation waveform for Channel 2 for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$ step-up to 14 V , $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{Low}$, $EN2 = \text{High}$, $R_{LOAD} = 100\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

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Under-voltage Lockout Operation Waveforms

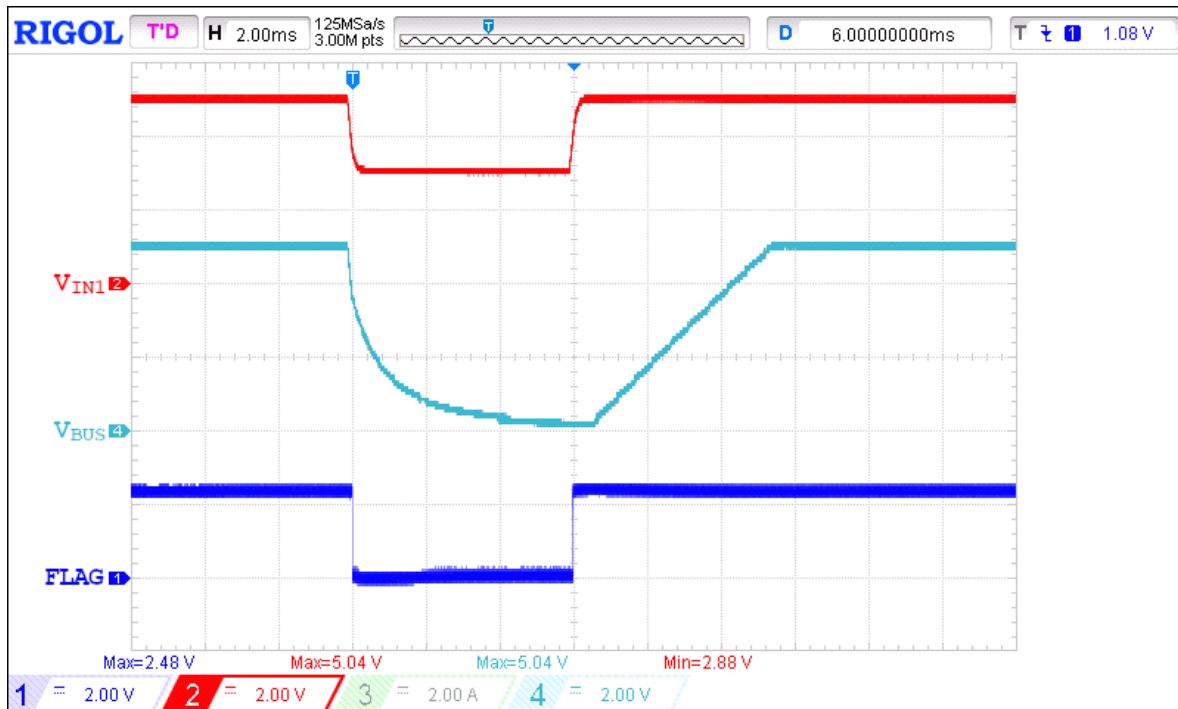


Figure 14. Under-voltage Lockout operation waveform for Channel 1 for $V_{IN1} = 5\text{ V}$ step-down to 3 V , $V_{IN2} = 12\text{ V}$, $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High}$, $EN2 = \text{Low}$, $R_{LOAD} = 100\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

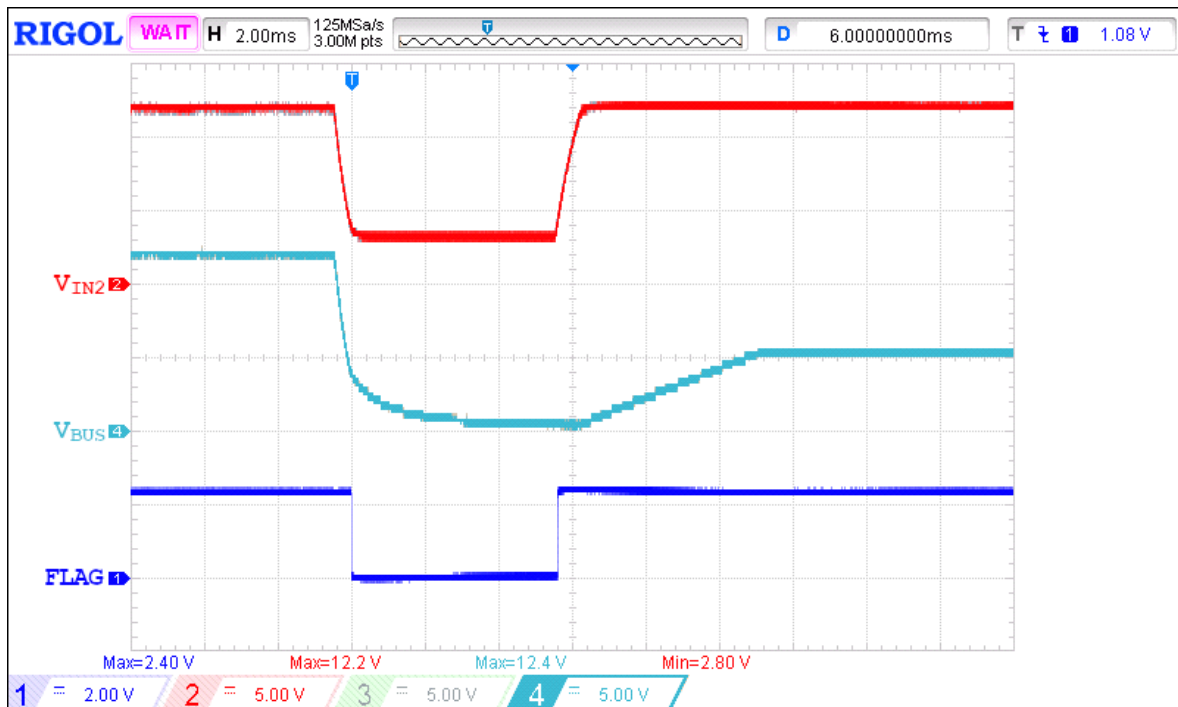


Figure 15. Under-voltage Lockout operation waveform for Channel 2 for $V_{IN1} = 5\text{ V}$, $V_{IN2} = 12\text{ V}$ step-down to 3 V , $R_{ILIM1} = 20\text{ k}\Omega$, $R_{ILIM2} = 20\text{ k}\Omega$, $EN1 = \text{High}$, $EN2 = \text{High}$, $R_{LOAD} = 100\text{ }\Omega$, $C_{LOAD} = 20\text{ }\mu\text{F}$

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APPLICATIONS INFORMATION

1 SLG59H1405V Power-Up Considerations

A normal power up condition is when both V_{IN1} and V_{IN2} voltages are within the operating voltage range ($V_{IN[1,2]} > V_{IN[1,2]_{UVLO}}$ and $V_{IN[1,2]} < V_{IN[1,2]_{OVP}}$), and then $EN1 > EN1_{VIH}$ can be applied to turn on Channel 1. To turn on Channel 2, $EN2 > EN2_{VIH}$ can be applied not sooner than 100 ms after $EN1 > EN1_{VIH}$, otherwise, the $EN2$ signal will be ignored and the switchover to Channel 2 will not be possible until $EN1 < EN1_{VIL}$. In order to turn on Channel 2, Channel 1 should always be turned on first.

2 SLG59H1405V Switchover Considerations

For seamless transition from Channel 1 to Channel 2 and vice versa it is recommended to have V_{IN2} voltage higher than V_{IN1} , otherwise a voltage droop during switchover can be much deeper, but will not have any impact on any other chip functionality.

3 SLG59H1405V Protections

3.1 OVP Latch-Off Operation

Once $V_{IN1} > V_{IN1_{OVP}}$ or $V_{IN2} > V_{IN2_{OVP}}$ the SLG59H1405V will latch-off within T_{OVP} response time. In order to release the part from the latch-off condition, both $EN1$ and $EN2$ should be set lower than $EN[1,2]_{VIL}$.

3.2 UVLO Operation

Once $V_{IN1} < V_{IN1_{UVLO}} - V_{IN1_{UVLO_HYS}}$ or $V_{IN2} < V_{IN2_{UVLO}} - V_{IN2_{UVLO_HYS}}$ the SLG59H1405V is turned off. In order to return to normal operation, $V_{IN[1,2]}$ should be higher than $V_{IN[1,2]_{UVLO}}$.

Note: If UVLO occurred while Channel 2 is selected, then after both input voltages are back to normal, Channel 2 should be turned on according to the sequence described in the Power-Up Considerations section.

3.3 Over-temperature Protection

When internal die temperature exceeds the $THERM_{ON}$ value (for example, during Active Current Limit operation) the SLG59H1405V will latch-off. In order to release the part from latch-off condition, both $EN1$ and $EN2$ should be set lower than $EN[1,2]_{VIL}$.

4 SLG59H1405V Active Current Limit

The SLG59H1405V has two modes of current limiting:

4.1 Standard Current Limiting Mode (with Thermal Protection)

The output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceeding the Active Current Limit for T_{OCP_delay} and then, if overcurrent condition still persists, the SLG59H1405V is latched-off. To release SLG59H1405V from latch-off state both $EN1$ and $EN2$ should be lower than $EN[1,2]_{VIL}$.

The ACL level can be adjusted by choosing the appropriate $\pm 1\%$ -tolerance R_{ILIM1} resistor value for Channel 1 and R_{ILIM2} resistor value for Channel 2 and can be calculated by the following equations:

For R_{ILIM1} ranging from 160 k Ω to 20 k Ω and for R_{ILIM2} ranging from 75 k Ω to 20 k Ω :

$$I_{ACL_VIN1} (A) = 54.985 * R_{ILIM1}^{-0.874}, \text{ and}$$

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$$I_{ACL_VIN2} (A) = 48.08 * R_{ILIM2}^{-1.071}$$

where:

$R_{ILIM[1,2]}$ = Resistor on ILIM[1,2] pins, in kOhms (Ω)

During active current limit operation, the die temperature rise due to the increased FET resistance. If the die temperature exceeds the $THERM_{ON}$ specification, the SLG59H1405V will also latch-off. To release the SLG59H1405V from latch-off state both EN[1,2] should be lower than EN[1,2] $_V_{IL}$.

4.2 Short Circuit Current Limiting Mode

Once the output I_{VBUS} current hits the Short-Circuit Protection Threshold (I_{SCP}) the SLG59H1405V will immediately shutdown, and then repower-up with a lower current limit threshold that can be calculated by following equation:

$$I_{LIM_SCP} = I_{ACL_VIN[1,2]} / I_{LIM_FOLD[1,2]}$$

where:

I_{LIM_SCP} = VBUS Current Limit after Triggering VBUS Short Circuit Protection.

$I_{ACL_VIN[1,2]}$ = Active Current Limit threshold set by $R_{ILIM[1,2]}$

This re-power up will last during T_{OCP_delay} time and then the SLG59H1405V will latch-off. To release the SLG59H1405V from the latch-off state both EN1 and EN2 should be lower than EN[1,2] $_V_{IL}$.

5 Discharge Operation

Initially, the internal discharge resistor ($R_{DISCHRG}$) appears on V_{BUS} once $V_{IN1} > V_{IN1_UVLO}$. Any time that EN1 and EN2 are lower than EN[1,2] $_V_{IL}$ or if any of OVP, UVLO, OCP, SCP, OTP, RCB protections are triggered or during $V_{IN2} \rightarrow V_{IN1}$ switchover operation, the discharge resistance will appear on VBUS.

6 Layout Guidelines

1. Since the VIN[1,2] and VBUS pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 16](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input $C_{IN[1,2]}$ and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59H1405V's VIN[1,2] and VBUS pins;
3. The GND pin should be connected to system analog or power ground plane.
4. 2 oz. copper is recommended for high current operation.

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7 SLG59H1405V Evaluation Board

A High Voltage GreenFET Evaluation Board for SLG59H1405V is designed according to the statements above and is illustrated on [Figure 16](#). Please note that evaluation board has VIN[1,2]_Sense and VBUS_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON}[1,2] evaluation.

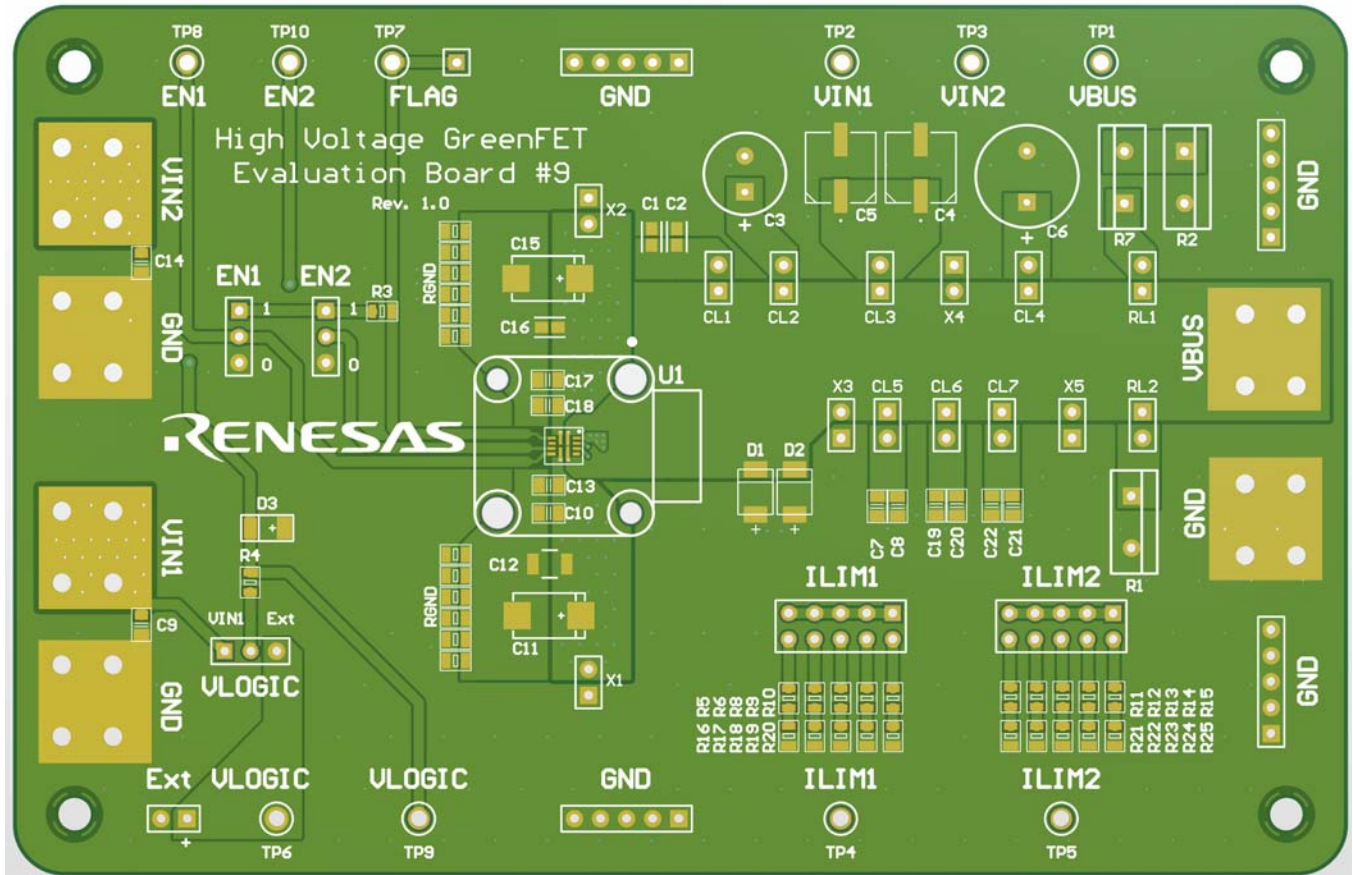


Figure 16. SLG59H1405V Evaluation Board

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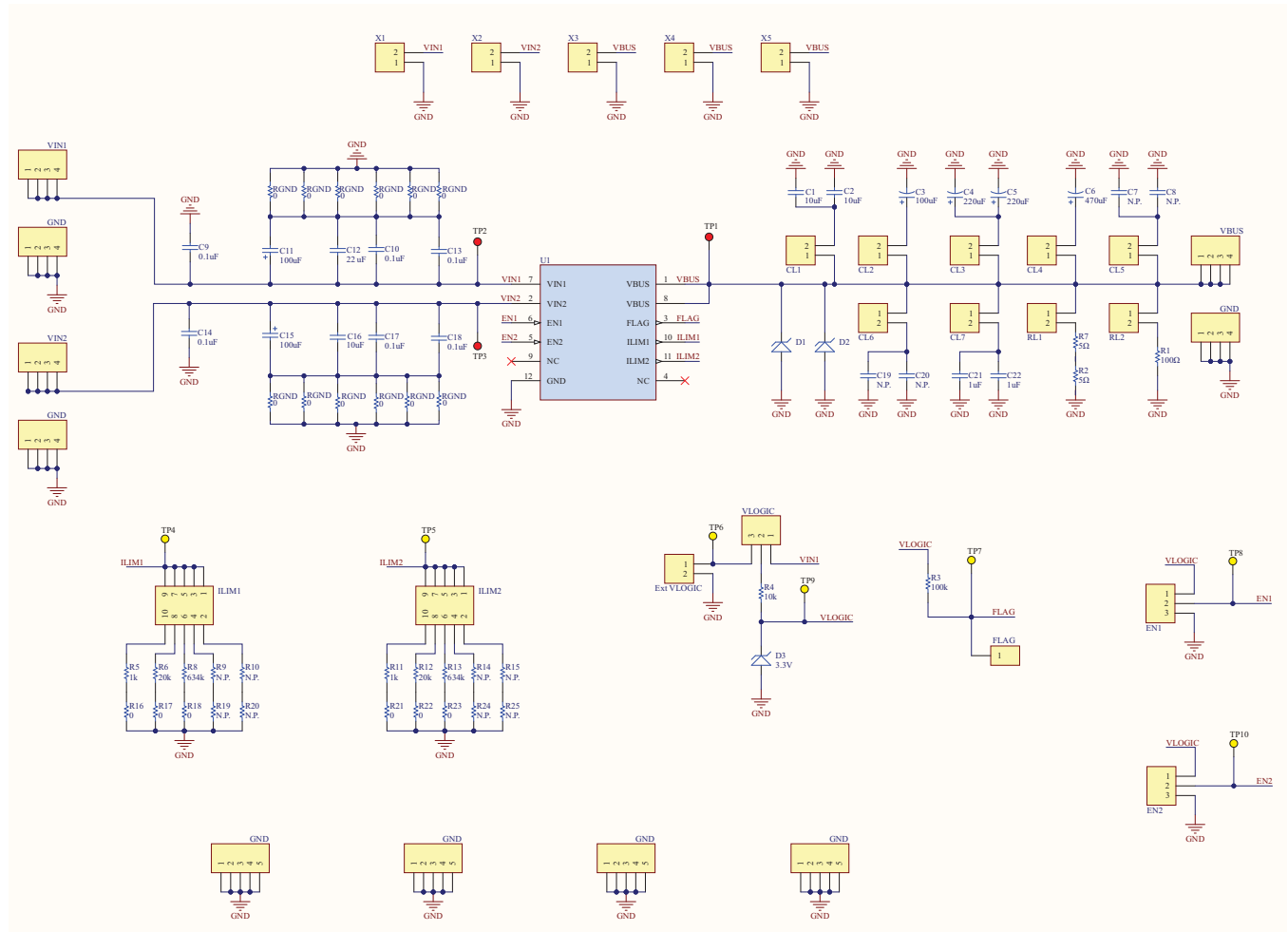


Figure 17. SLG59H1405V Evaluation Board Schematic


8 Basic EVB Configuration

1. Connect oscilloscope probes to VIN[1,2], VBUS, FLAG, etc.;
2. Connect jumpers for ILIM1 and ILIM2 to set desired current limit, VLOGIC to position VIN1, EN1 and EN2 to Logic Low position;
3. Connect jumpers for desired C_{LOAD} from CL1 to CL7 and R_{LOAD} from RL1 to RL2;
4. Toggle the EN1, EN2 signals High or Low to observe SLG59H1405V operation;
5. Please be noted that EN2 can be toggled from Low to High only after min 100 ms delay from EN1 goes Low to High;

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Package Top Marking System Definition

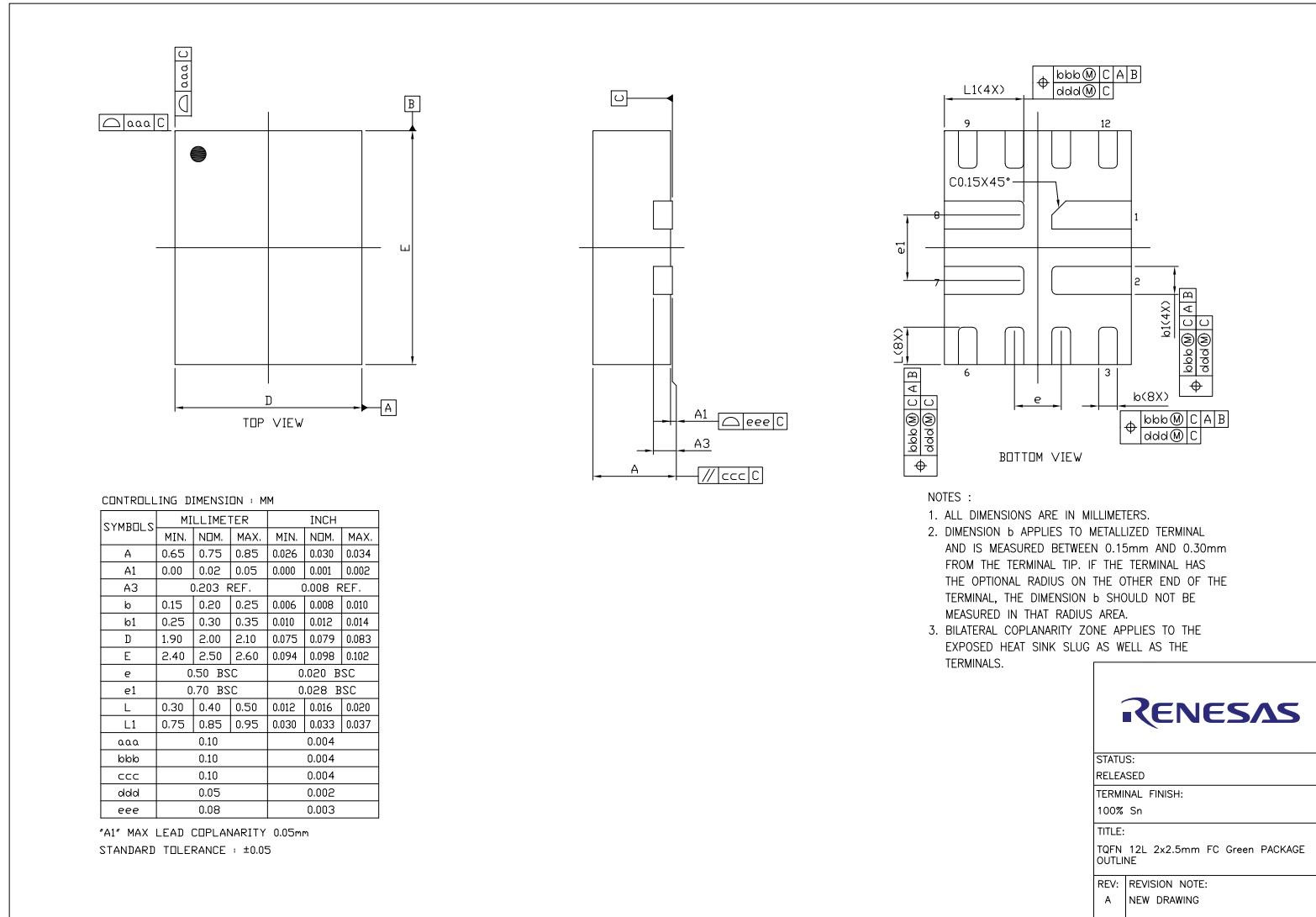
PPPPP	Part Code
YWNNN	Date Code + Serial Code
 ARR	Pin 1 Identifier + Assembly Code + Revision Code

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Package Drawing and Dimensions

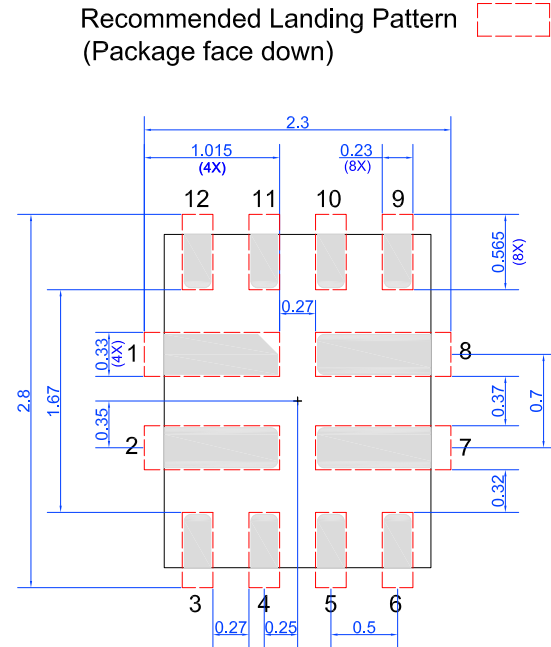
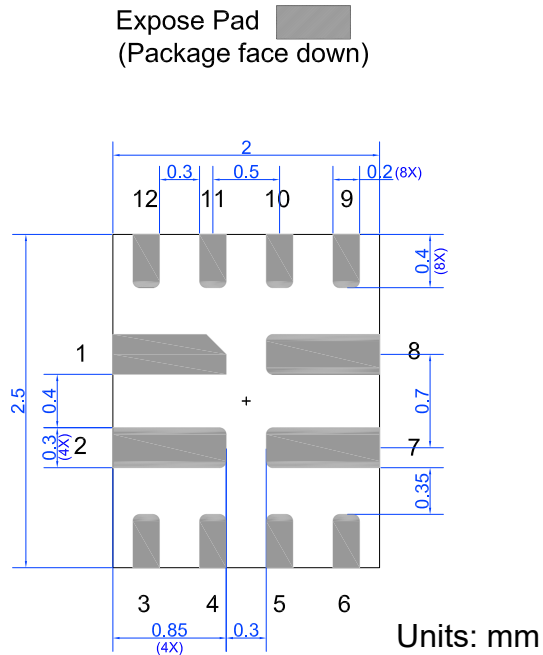
12 Lead FC-QFN Package 2 mm x 2.5 mm



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Recommended Landing Pattern



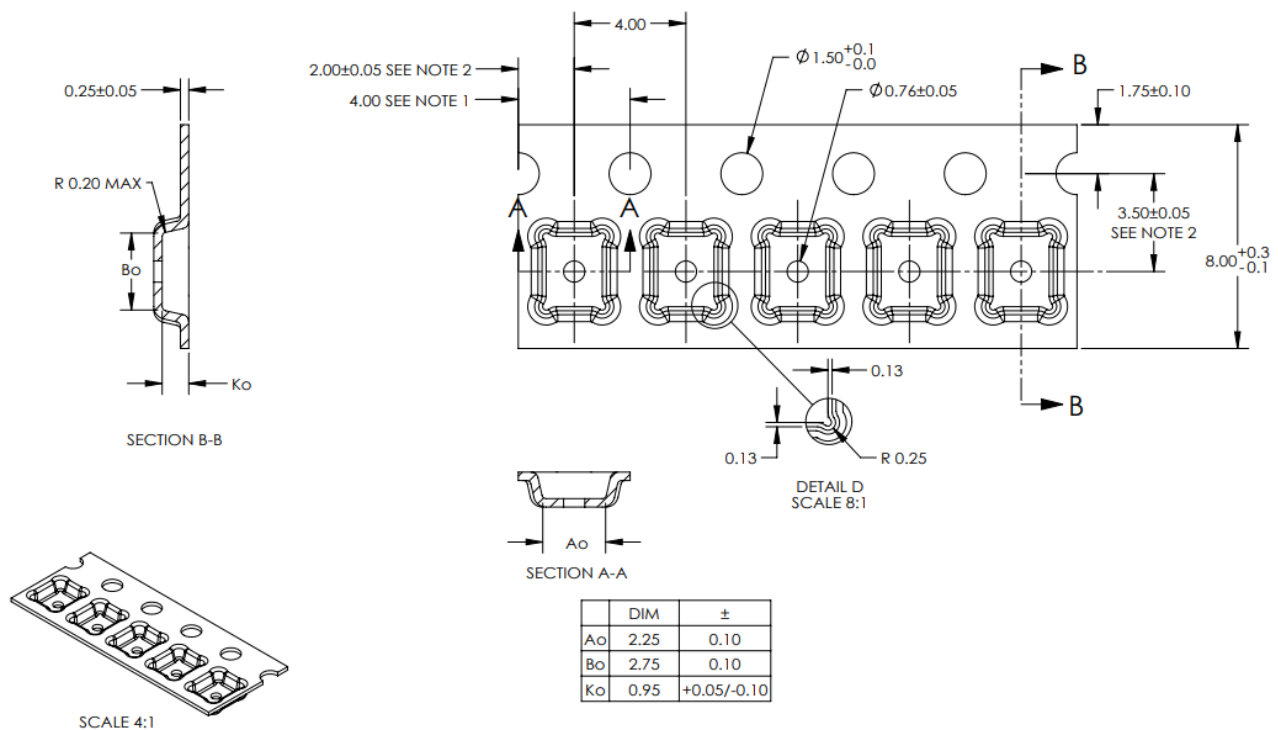
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Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Units per Reel	Max Units per Box	Reel & Hub Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
						Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
FC-QFN 12L 2 x 2.5 mm, 0.4P Green	12	2 x 2.5 x 0.75	3,000	3,000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions



NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.75 mm^3 (nominal). More information can be found at www.jedec.org.

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Revision History

Date	Version	Change
11-Nov-2024	1.02	Updated Figure 2 and Figure 3 captions from "EN1 = Low" to "EN1 = High"
15-May-2023	1.01	Updated V_{IN1_UVLO} and V_{IN2_ULVO} Min from 3.5 V to 3.6 V Updated $V_{BUS(SR)}$ Min from 0.9 V to 0.99 V for $V_{IN2} > 9$ V condition
28-Mar-2023	1.00	Production Release

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