SLG46110

GreenPAK Programmable Mixed-Signal Matrix

Description

The SLG46110 provides a small, low-power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one-time Non-Volatile Memory (NVM) to configure the interconnect logic, the IO pins, and the macrocells of the SLG46110. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low-power, single integrated circuit.

Features

- Two Analog Comparators (ACMP)
- Voltage Reference (V_{REF})
- Four Combinatorial Look-up Tables (LUTs)
  - Two 2-bit LUTs
  - Two 3-bit LUTs
- Seven Combination Function Macrocells
  - Two selectable D Flip-Flop/LATCHs or 2-bit LUTs
  - Two selectable D Flip-Flop/LATCHs or 3-bit LUTs
  - One selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage/2 output
  - One selectable Counter/Delay (CNT/DLY) or 4-bit LUT
  - One Programmable Delay/Deglitch Filter
- Three Counter/Delay Generators
  - Three 8-bit Counter/Delay with external clock/reset
- 25 kHz/2 MHz Oscillator
- One Bandgap
- Power-on Reset (POR)
- 1.8 V (±5 %) to 5 V (±10 %) V_{DD} range
- Operating temperature range: -40 °C to +85 °C
- RoHS compliant/Halogen-free
- Pb-free 12-pin STQFN: 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch

Applications

- Personal computers and servers
- PC peripherals
- Consumer electronics
- Data communications equipment
- Handheld and portable electronics

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1. Overview

1.1 Block Diagram

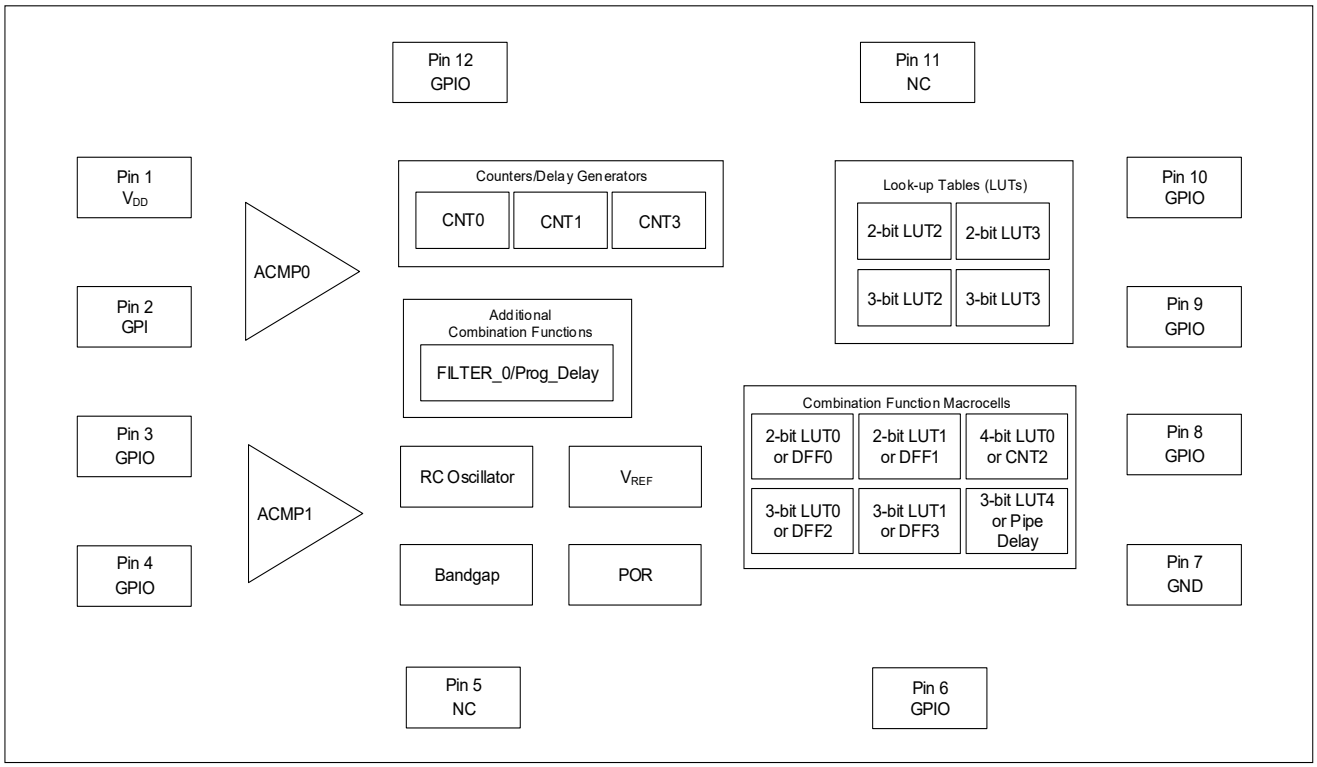


Figure 1. Block Diagram

1.2 User Programmability and Customization

Non-volatile memory (NVM) is used to configure the SLG46110's Connection Matrix routing and macrocells. The NVM is One-Time Programmable (OTP). However, GreenPAK™ development tools can be used to configure the Connection Matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Renesas Electronics Corporation to integrate into the production process.

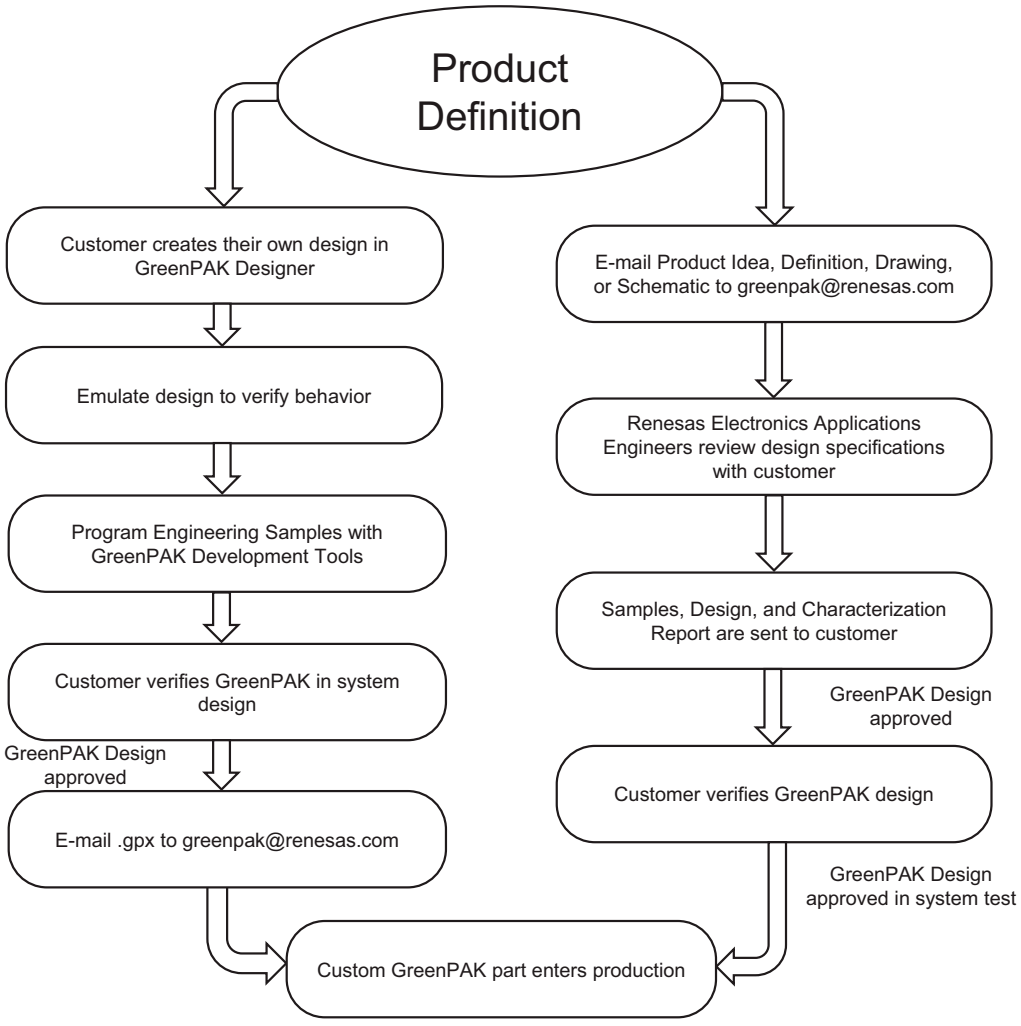


Figure 2. Steps to Create a Custom GreenPAK Device

2. Pin Information

2.1 Pin Assignments

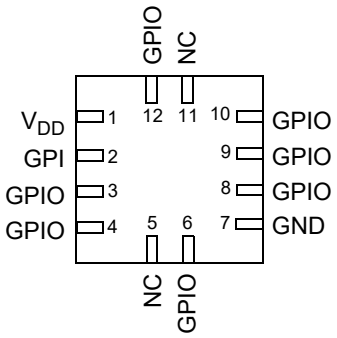


Figure 3. Pin Assignments – STQFN-12 (Top View)

2.2 Pin Descriptions

Table 1. Functional Pin Description

Pin Number	Pin Name	Function
1	V_{DD}	Power Supply
2	GPI	General Purpose Input
3	GPIO	General Purpose IO or Analog Comparator 0 (+)
4	GPIO	General Purpose IO or Analog Comparator 0 (-)
5	NC	No Connect
6	GPIO	General Purpose IO or Analog Comparator 1 (+) with OE
7	GND	Ground
8	GPIO	General Purpose IO
9	GPIO	General Purpose IO
10	GPIO	General Purpose IO with OE and V_{REF} output
11	NC	No Connect
12	GPIO	General Purpose IO or External Clock Input

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} to GND		-0.5	7.0	V
DC Input Voltage	GPIO	GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current Through V_{DD} Pin (Per Chip Side [1])	T_J = +85 °C	-	73	mA
	T_J = +110 °C	-	35	mA
Maximum Average or DC Current Through GND Pin (Per Chip Side [1])	T_J = +85 °C	-	92	mA
	T_J = +110 °C	-	44	mA
Maximum Average or DC Current (Through Pin)	Push-pull 1x	-	12	mA
	Push-pull 2x	-	17	mA
	OD 1x	-	18	mA
	OD 2x	-	28	mA
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	+150	°C
Junction Temperature		-	+150	°C
Moisture Sensitivity Level		1		

1. The GreenPAK's power rails are divided into two sides. Pins 2, 3, 4, and 6 are connected to one side, pins 8, 9, 10, and 12 to another.

3.2 ESD Ratings

Parameter	Value	Unit
ESD Protection (Human Body Model)	±2000	V
ESD Protection (Charged Device Model)	±1000	V

3.3 Recommended Operating Conditions

Parameter	Min	Max	Unit
Supply Voltage (V_{DD})	1.71	5.5	V
Operating Ambient Temperature	-40	+85	°C
Maximal Voltage Applied to any Pin in High-impedance State	-	V_{DD} + 0.3	V
Capacitor Value at V_{DD}	0.1	-	µF

3.4 Electrical Specifications

3.4.1 Logic IO Specifications

V_{DD} = 1.71 V to 1.89 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	1.71	1.80	1.89	V
Quiescent Current	I_Q	Static Inputs and Outputs (when ACMP, V_{REF} and OSC are powered down and non-operational)	-	0.5	-	µA
Analog Input Voltage Range	V_{AIR}	Positive Input	0	-	V_{DD}	V
		Negative Input	0	-	1.1	V
High-level Input Voltage	V_{IH}	Logic input	1.100	-	V_{DD}	V
		Logic input with Schmitt trigger	1.270	-	V_{DD}	V
		Low-level logic input	0.980	-	V_{DD}	V
Low-level Input Voltage	V_{IL}	Logic input	-	-	0.690	V
		Logic input with Schmitt trigger	-	-	0.440	V
		Low-level logic input	-	-	0.520	V
Input Leakage (Absolute Value)	I_{LKG}	-	-	1	1000	nA
High-level Output Voltage	V_{OH}	Push-pull 1x, Open-drain PMOS 1x, I_{OH} = 100 µA	1.680	1.790	-	V
		Push-pull 2x, Open-drain PMOS 2x, I_{OH} = 100 µA	1.702	1.800	-	V
Low-level Output Voltage	V_{OL}	Push-pull 1x, I_{OL} = 100 µA	-	0.020	0.030	V
		Push-pull 2x, I_{OL} = 100 µA	-	0.010	0.020	V
		Open-drain NMOS 1x, I_{OL} = 100 µA	-	0.010	0.020	V
		Open-drain NMOS 2x, I_{OL} = 100 µA	-	0.010	0.010	V
High-level Output Current [1]	I_{OH}	Push-pull 1x, Open-drain PMOS 1x, V_{OH} = V_{DD} - 0.2	1.040	1.400	-	mA
		Push-pull 2x, Open-drain PMOS 2x, V_{OH} = V_{DD} - 0.2	2.150	2.710	-	mA
Low-level Output Current [1]	I_{OL}	Push-pull 1x, V_{OL} = 0.15 V	0.760	1.340	-	mA
		Push-pull 2x, V_{OL} = 0.15 V	1.520	2.660	-	mA
		Open-drain NMOS 1x, V_{OL} = 0.15 V	1.530	2.670	-	mA
		Open-drain NMOS 2x, V_{OL} = 0.15 V	3.060	5.130	-	mA
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	-	0.27	-	ms
Power-on Threshold	PON_{THR}	V_{DD} level required to start up the chip	1.182	1.346	1.505	V
Power-off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.752	0.918	1.110	V
Pull-up or Pull-down Resistance	R_{PULL}	1 MΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	1	-	MΩ
		100 kΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	100	-	kΩ
		10 kΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	10	-	kΩ

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

V_{DD} = 3.0 V to 3.6 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V
Quiescent Current	I_Q	Static Inputs and Outputs (when ACMP, V_{REF} and OSC are powered down and non-operational)	-	0.75	-	µA
Analog Input Voltage Range	V_{AIR}	Positive Input	0	-	V_{DD}	V
		Negative Input	0	-	1.2	V
High-level Input Voltage	V_{IH}	Logic input	1.780	-	V_{DD}	V
		Logic input with Schmitt trigger	2.130	-	V_{DD}	V
		Low-level logic input	1.130	-	V_{DD}	V
Low-level Input Voltage	V_{IL}	Logic input	-	-	1.210	V
		Logic input with Schmitt trigger	-	-	0.950	V
		Low-level logic input	-	-	0.690	V
Input Leakage (Absolute Value)	I_{LKG}	-	-	1	1000	nA
High-level Output Voltage	V_{OH}	Push-pull 1x, Open-drain PMOS 1x, I_{OH} = 3 mA	2.710	3.090	-	V
		Push-pull 2x, Open-drain PMOS 2x, I_{OH} = 3 mA	2.870	3.190	-	V
Low-level Output Voltage	V_{OL}	Push-pull 1x, I_{OL} = 3 mA	-	0.180	0.280	V
		Push-pull 2x, I_{OL} = 3 mA	-	0.090	0.130	V
		Open-drain NMOS 1x, I_{OL} = 3 mA	-	0.090	0.130	V
		Open-drain NMOS 2x, I_{OL} = 3 mA	-	0.050	0.070	V
High-level Output Current [1]	I_{OH}	Push-pull 1x, Open-drain PMOS 1x, V_{OH} = 2.4 V	5.830	10.180	-	mA
		Push-pull 2x, Open-drain PMOS 2x, V_{OH} = 2.4 V	11.264	19.660	-	mA
Low-level Output Current [1]	I_{OL}	Push-Pull 1x, V_{OL} = 0.4 V	4.060	6.440	-	mA
		Push-pull 2x, V_{OL} = 0.4 V	8.130	12.360	-	mA
		Open-drain NMOS 1x, V_{OL} = 0.4 V	8.130	12.410	-	mA
		Open-drain NMOS 2x, V_{OL} = 0.4 V	16.260	22.900	-	mA
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	-	0.27	-	ms
Power-on Threshold	PON_{THR}	V_{DD} level required to start up the chip	1.182	1.346	1.505	V
Power-off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.752	0.918	1.110	V
Pull-up or Pull-down Resistance	R_{PULL}	1 MΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	1	-	MΩ
		100 kΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	100	-	kΩ
		10 kΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	10	-	kΩ

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

V_{DD} = 4.5 V to 5.5 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-	4.5	5.0	5.5	V
Quiescent Current	I_Q	Static Inputs and Outputs (when ACMP, V_{REF} and OSC are powered down and non-operational)	-	1.0	-	µA
Analog Input Voltage Range	V_{AIR}	Positive Input	0	-	V_{DD}	V
		Negative Input	0	-	1.2	V
High-level Input Voltage	V_{IH}	Logic input	2.640	-	V_{DD}	V
		Logic input with Schmitt trigger	3.160	-	V_{DD}	V
		Low-level logic input	1.230	-	V_{DD}	V
Low-level Input Voltage	V_{IL}	Logic input	-	-	1.840	V
		Logic input with Schmitt trigger	-	-	1.510	V
		Low-level logic input	-	-	0.780	V
Input Leakage (Absolute Value)	I_{LKG}	-	-	1	1000	nA
High-level Output Voltage	V_{OH}	Push-pull 1x, Open-drain PMOS 1x, I_{OH} = 5 mA	4.150	4.730	-	V
		Push-pull 2x, Open-drain PMOS 2x, I_{OH} = 5 mA	4.300	4.860	-	V
Low-level Output Voltage	V_{OL}	Push-pull 1x, I_{OL} = 5 mA	-	0.230	0.330	V
		Push-pull 2x, I_{OL} = 5 mA	-	0.120	0.160	V
		Open-drain NMOS 1x, I_{OL} = 5 mA	-	0.120	0.160	V
		Open-drain NMOS 2x, I_{OL} = 5 mA	-	0.070	0.090	V
High-level Output Current [1]	I_{OH}	Push-pull 1x, Open-drain PMOS 1x, V_{OH} = 2.4 V	21.808	29.100	-	mA
		Push-pull 2x, Open-drain PMOS 2x, V_{OH} = 2.4 V	40.598	56.080	-	mA
Low-level Output Current [1]	I_{OL}	Push-pull 1x, V_{OL} = 0.4 V	6.010	9.730	-	mA
		Push-pull 2x, V_{OL} = 0.4 V	11.590	19.460	-	mA
		Open-drain NMOS 1x, V_{OL} = 0.4 V	11.760	19.460	-	mA
		Open-drain NMOS 2x, V_{OL} = 0.4 V	19.120	35.621	-	mA
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	-	0.27	-	ms
Power-on Threshold	PON_{THR}	V_{DD} level required to start up the chip	1.182	1.346	1.505	V
Power-off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.752	0.918	1.110	V
Pull-up or Pull-down Resistance	R_{PULL}	1 MΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	1	-	MΩ
		100 kΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	100	-	kΩ
		10 kΩ for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	-	10	-	kΩ

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.4.2 Estimated Typical Current of Macrocell Configurations

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Current	I_{DD}	Chip Quiescent	0.5	0.8	1.0	µA
		V_{REF}	56.9	56.9	63.3	µA
		V_{REF} Buffer (each)	2.7	13.0	13.7	µA
		OSC 25 kHz, pre-divider = 1	3.1	4.8	6.4	µA
		OSC 25 kHz, pre-divider = 8	3.0	4.5	6.0	µA
		OSC 2 MHz, pre-divider = 1	27.4	45.4	67.4	µA
		OSC 2 MHz, pre-divider = 8	17.5	23.7	29.5	µA
		1st ACMP used (includes V_{REF})	60.6	62.0	68.4	µA
		Each additional ACMP add	3.7	4.9	5.1	µA

3.4.3 Estimated Typical Delay for Each Macrocell

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Delay	t_{PD}	Digital Input without Schmitt Trigger - Push-pull	35.3	34.4	14.5	14.3	10.3	10.5	ns
Delay	t_{PD}	Digital Input with Schmitt Trigger - Push-pull	34.8	32.9	14.2	13.8	10.0	10.1	ns
Delay	t_{PD}	Low-voltage Digital input - Push-pull	37.8	450.0	15.0	208.2	10.5	142.3	ns
Delay	t_{PD}	Digital Input without Schmitt Trigger NMOS	-	73.5	-	26.0	-	16.3	ns
Delay	t_{PD}	Output enable from Pin, OE Hi-Z to 1	44.6	-	17.9	-	12.4	-	ns
Delay	t_{PD}	Output enable from Pin, OE Hi-Z to 0	-	43.0	-	17.6	-	12.5	ns
Delay	t_{PD}	2-bit LUT (LATCH shared macrocell inputs)	29.6	24.8	11.5	10.1	8.2	6.9	ns
Delay	t_{PD}	LATCH (2-bit LUT shared macrocell inputs)	29.2	31.5	11.8	12.5	8.4	8.4	ns
Delay	t_{PD}	3-bit LUT (LATCH shared macrocell inputs)	33.0	27.4	12.8	11.1	9.1	7.5	ns
Delay	t_{PD}	LATCH with nRST/nSET (3-bit LUT shared macrocell inputs)	29.9	32.4	12.1	13.0	8.7	8.7	ns
Delay	t_{PD}	4-bit LUT (shared macrocell inputs)	29.2	27.2	11.2	10.8	8.0	7.3	ns
Delay	t_{PD}	2-bit LUT	19.4	18.8	7.2	7.4	5.1	5.0	ns
Delay	t_{PD}	3-bit LUT	22.3	22.7	8.3	8.9	6.0	5.9	ns
Delay	t_{PD}	CNT/DLY	38.4	36.0	15.2	15.1	10.8	10.4	ns
Delay	t_{PD}	CNT/DLY (shared macrocell inputs)	41.0	36.2	16.3	15.6	11.5	10.9	ns
Delay	t_{PD}	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	39.7	-	15.7	-	11.1	-	ns
Delay	t_{PD}	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	-	41.5	-	16.9	-	11.6	ns
Delay	t_{PD}	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	39.7	41.5	15.7	16.9	11.1	11.6	ns
Delay	t_{PD}	Filter	183.1	186.2	73.5	75.7	47.9	50.2	ns

3.4.4 Counter/Delay Specifications

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	OSC Freq	OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Offset	25 kHz	auto	19	14	12	µs
Offset	2 MHz	auto	7	4	4	µs
Frequency settling time	25 kHz	auto	19	14	12	µs
Frequency settling time	2 MHz	auto	14	14	14	µs
Variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
Variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
Tpd (non-delayed edge)	25 kHz/2 MHz	either	35	14	10	ns

3.4.5 Programmable Delay Typical Delays and Widths

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
time1	Width, 1 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	272.4	128.8	97.5	ns
time1	Width, 2 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	582.7	272.6	205.1	ns
time1	Width, 3 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	893.4	416.6	312.9	ns
time1	Width, 4 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	1203.4	560.6	420.9	ns
time2	Delay, 1 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	39.3	15.7	10.9	ns
time2	Delay, 2 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	39.3	15.7	10.9	ns
time2	Delay, 3 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	39.3	15.7	10.9	ns
time2	Delay, 4 cell	P DLY Mode: (Any) Edge Detect, Edge Detect Output	39.3	15.7	10.9	ns
time1	Delay, 1 cell	P DLY Mode: Both Edge Delay (Shared Macrocell Inputs)	354.0	161.5	120.1	ns
time1	Delay, 2 cell	P DLY Mode: Both Edge Delay (Shared Macrocell Inputs)	664.2	305.2	227.8	ns
time1	Delay, 3 cell	P DLY Mode: Both Edge Delay (Shared Macrocell Inputs)	974.9	449.1	335.7	ns
time1	Delay, 4 cell	P DLY Mode: Both Edge Delay (Shared Macrocell Inputs)	1284.8	593.1	443.6	ns
time1	Width	CNT3/DLY3 Rising Edge Detect (Shared Macrocell Inputs)	63.6	32.4	22.9	ns
time1	Width	CNT3/DLY3 Falling Edge Detect (Shared Macrocell Inputs)	61.3	31.1	22.5	ns
time1	Width	CNT3/DLY3 Both Edge Detect (Shared Macrocell Inputs)	62.2	31.6	22.7	ns

3.4.6 Typical Filter Rejection Pulse Width

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns

4. IO Pins

The SLG46110 has a total of eight multi-function IO pins which can function as either a user-defined input, as well as serving as a special function (such as outputting the voltage reference). Refer to section 2. Pin Information forpin definitions.

Of the eight user-defined IO pins on the SLG46110, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

4.1 Input Modes

Each IO pin can be configured as a digital input pin with or without buffered Schmitt trigger, or can also be configured as a low-voltage digital input. Pins 3, 4, and 6 can also be configured to serve as analog inputs to the on-chip comparators.

4.2 Output Modes

Pins 3, 4, 6, 8, 9, 10, and 12 can all be configured as digital output pins.

4.3 Pull-Up/Down Resistors

All IO pins have the option for user-selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as either pull-up or pull-downs.

4.4 3-State Outputs

Pins 6 and 10 of the SLG46110 can each be configured to build separate 3-state outputs using other components from these pins.

Table 2. 3-State Output Mode Settings (for Pin 6 and 10)

Output Enable	Input Mode	Output Mode
0	Analog Input/Output	-
1	-	Push-pull

4.5 IO Register Settings

4.5.1 Pin 2 Register Settings

Table 3. Pin 2 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 2 Mode Control	reg [380:379]	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 10: Low-voltage digital input 11: Reserved
Pin 2 Pull-Down Resistor Value Selection	reg [382:381]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor

4.5.2 Pin 3 Register Settings

Table 4. Pin 3 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 3 Mode Control	reg [385:383]	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input and Open-drain NMOS
Pin 3 Pull-Up/Down Resistor Value Selection	reg [387:386]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor
Pin 3 Pull-Up/Down Resistor Selection	reg [388]	0: Pull-down resistor 1: Pull-up resistor
Pin 3 Driver Strength Selection	reg [389]	0: 1x 1: 2x

4.5.3 Pin 4 Register Settings

Table 5. Pin 4 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 4 Mode Control	reg [392:390]	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input and Open-drain NMOS
Pin 4 Pull-Up/Down Resistor Value Selection	reg [394:393]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
Pin 4 Pull-Up/Down Resistor Selection	reg [395]	0: Pull-down Resistor 1: Pull-up Resistor
Pin 4 Driver Strength Selection	reg [396]	0: 1x 1: 2x

4.5.4 Pin 6 Register Settings

Table 6. Pin 6 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 6 Mode Control (sig_Pin6_oe = 0)	reg [398:397]	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low-voltage Digital Input 10: Analog Input
Pin 6 Mode Control (sig_Pin6_oe = 1)	reg [400:399]	00: Push-pull 1x 01: Push-pull 1x 10: Open-drain NMOS 1x 11: Open-drain NMOS 1x
Pin 6 Pull-Up/Down Resistor Value Selection	reg [402:401]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
Pin 6 Pull-Up/Down Resistor Selection	reg [403]	0: Pull-down Resistor 1: Pull-up Resistor

4.5.5 Pin 8 Register Settings

Table 7. Pin 8 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 8 Mode Control	reg [406:404]	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input and Open-drain NMOS
Pin 8 Pull-Up/Down Resistor Value Selection	reg [408:407]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
Pin 8 Pull-Up/Down Resistor Selection	reg [409]	0: Pull-down Resistor 1: Pull-up Resistor
Pin 8 Driver Strength Selection	reg [410]	0: 1x 1: 2x

4.5.6 Pin 9 Register Settings

Table 8. Pin 9 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 9 Mode Control	reg [413:411]	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input and Open-drain NMOS
Pin 9 Pull-Up/Down Resistor Value Selection	reg [415:414]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
Pin 9 Pull-Up/Down Resistor Selection	reg [416]	0: Pull-down Resistor 1: Pull-up Resistor
Pin 9 Driver Strength Selection	reg [417]	0: 1x 1: 2x

4.5.7 Pin 10 Register Settings

Table 9. Pin 10 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 10 Mode Control (sig_Pin10_oe = 0)	reg [419:418]	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low-voltage Digital Input 11: Analog Input/Output
Pin 10 Mode Control (sig_Pin10_oe = 1)	reg [421:420]	00: Push-pull 1x 01: Push-pull 2x 10: Open-drain NMOS 1x 11: Open-drain NMOS 1x

Table 9. Pin 10 Register Settings (Cont.)

Signal Function	Register Bit Address	Register Definition
Pin 10 Pull-Up/Down Resistor Value Selection	reg [423:422]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
Pin 10 Pull-Up/Down Resistor Selection	reg [424]	0: Pull-down Resistor 1: Pull-up Resistor

4.5.8 Pin 12 Register Settings

Table 10. Pin 12 Register Settings

Signal Function	Register Bit Address	Register Definition
Pin 12 Mode Control	reg [427:425]	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input and Open-drain NMOS
Pin 12 Pull-Up/Down Resistor Value Selection	reg [429:428]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
Pin 12 Pull-Up/Down Resistor Selection	reg [430]	0: Pull-down Resistor 1: Pull-up Resistor
Pin 12 Driver Strength Selection	reg [431]	0: 1x 1: 2x

4.6 GPI IO Structure

4.6.1 GPI IO Structure (for Pin 2)

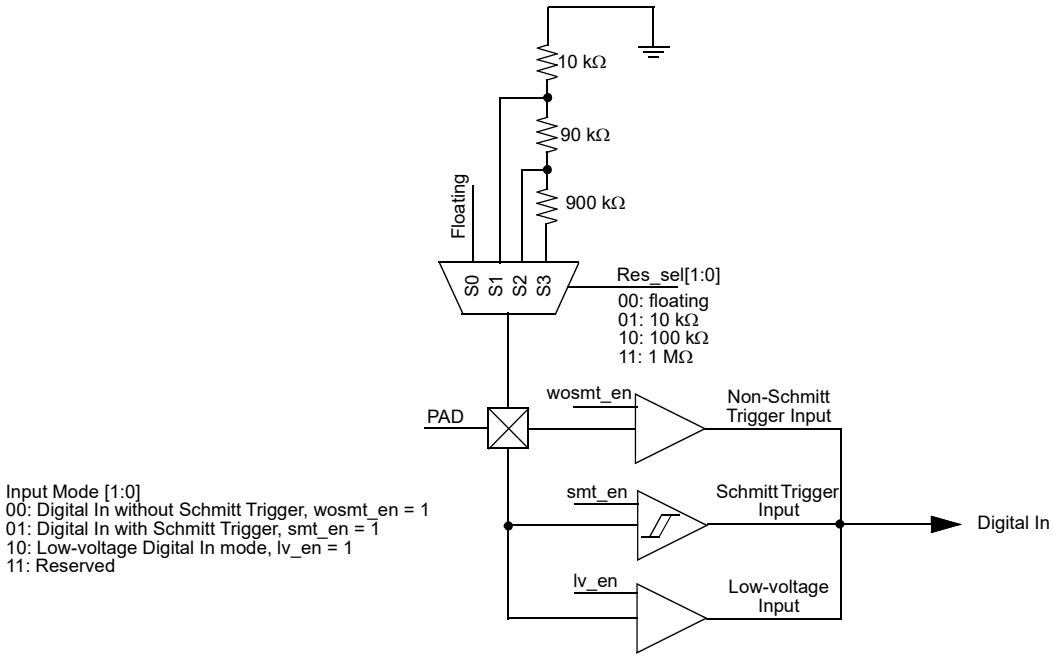


Figure 4. Pin 2 GPI IO Structure Diagram

4.7 Matrix OE IO Structure

4.7.1 Matrix OE IO Structure (for Pins 6 and 10)

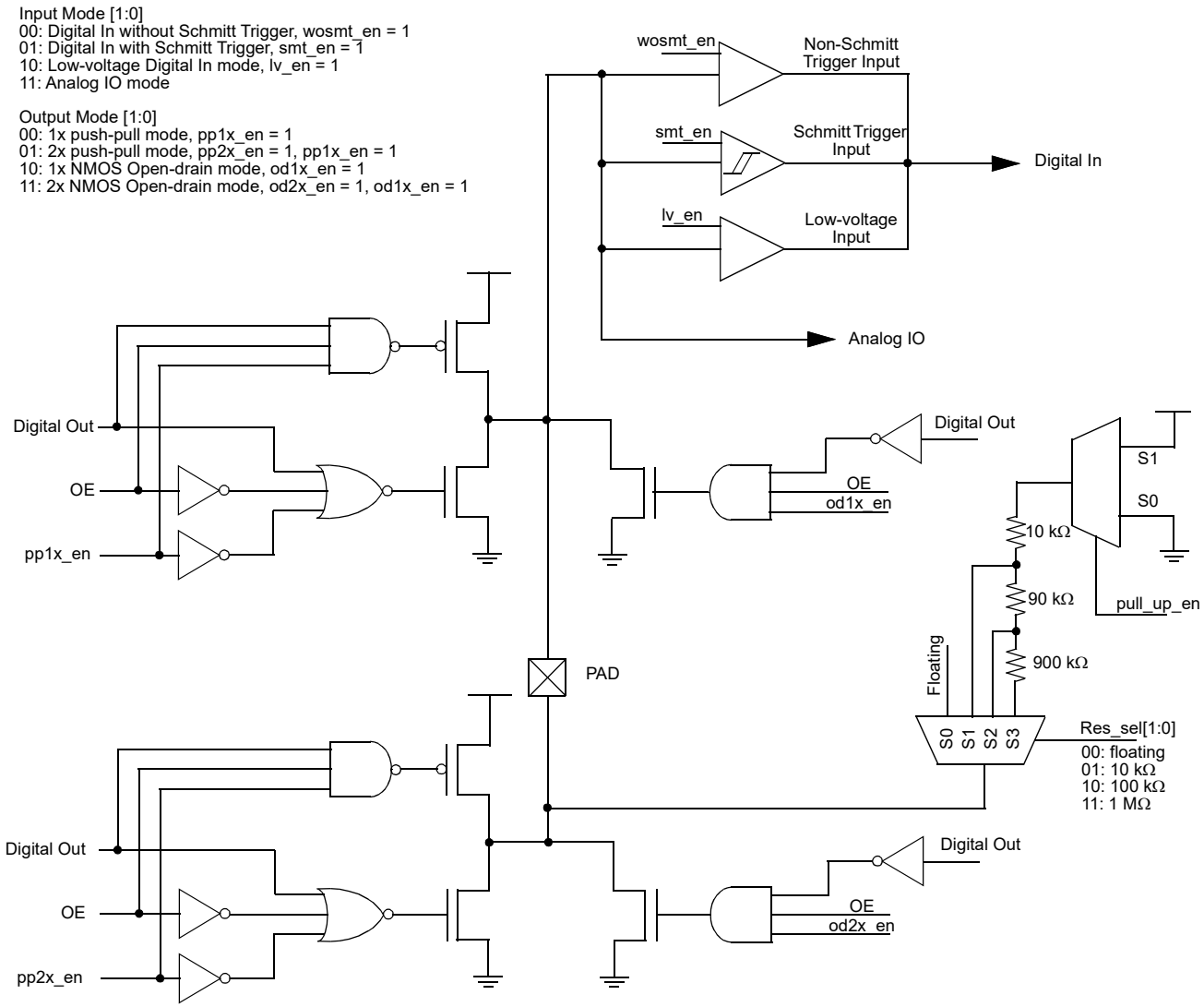


Figure 5. Matrix OE IO Structure Diagram

4.8 Register OE IO Structure

4.8.1 Register OE IO Structure (for Pins 3, 4, 8, 9, 12)

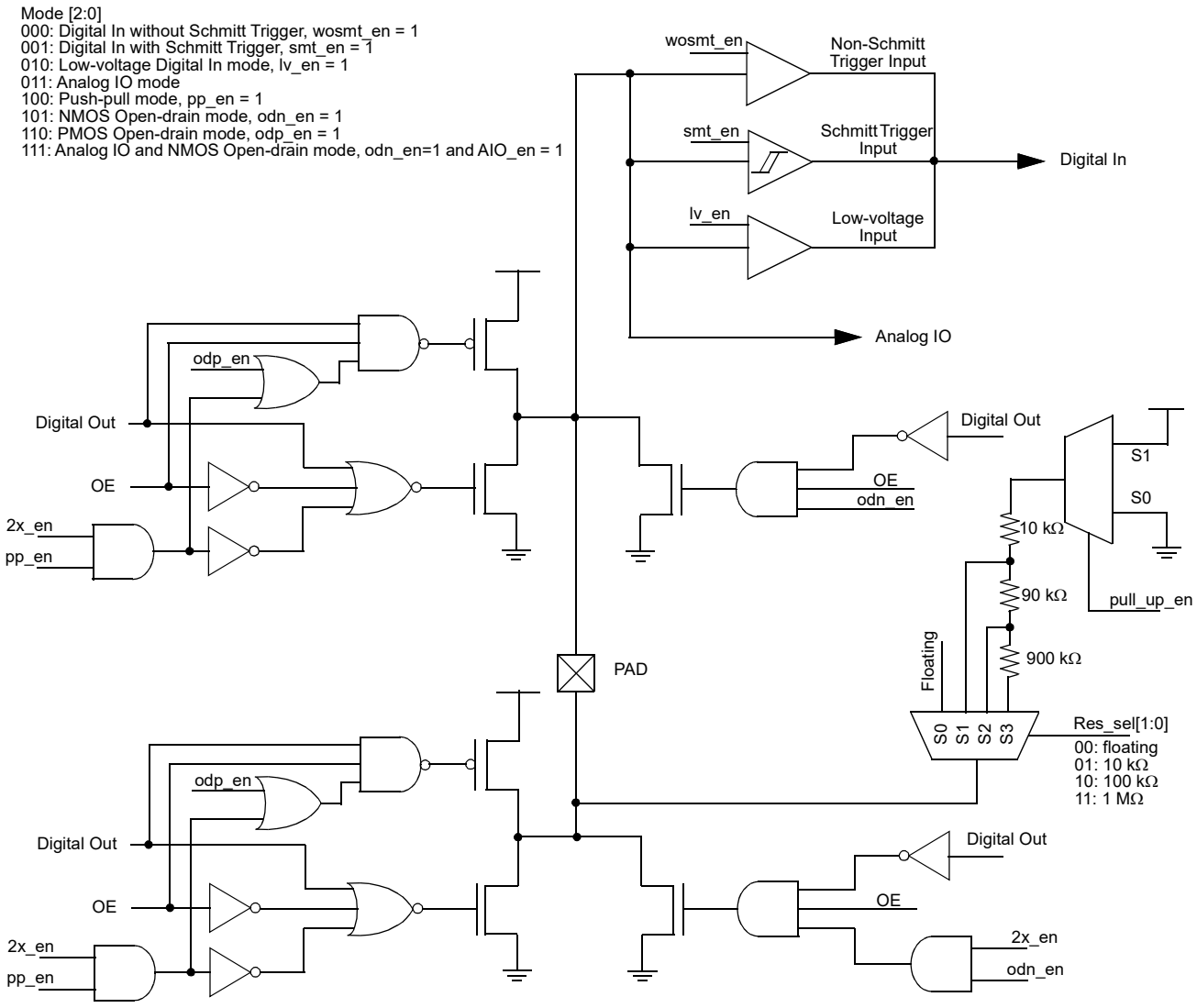


Figure 6. Register OE IO Structure Diagram

5. Connection Matrix

The Connection Matrix in the SLG46110 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46110 has a specific digital bit code assigned to it that is either set to active HIGH or inactive LOW based on the design that is created. Once the 512 register bits within the SLG46110 are programmed a fully custom circuit will be created.

The Connection Matrix has 32 inputs and 44 outputs. Each of the 32 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, V_{DD} and V_{SS}. The input to a digital macrocell uses a 5-bit register to select one of these 32 input lines.

For a complete list of the SLG46110's register table, see section 13. Register Definitions.

Matrix Input Signal Functions	N
V_{SS}	0
Pin 2 Digital In	1
Pin 3 Digital In	2
Pin 4 Digital In	3
⋮	⋮
Pin 12 Digital In	30
V_{DD}	31

Matrix Inputs

Matrix Outputs

N	0	1	2	⋯	43
Registers	reg [4:0]	reg [9:5]	reg [14:10]	⋯	reg [219:215]
Function	Pin 3 Digital Output Source	Pin 4 Digital Output Source	Pin 6 Digital Output Source	⋯	Pin 12 Digital Output Source

Figure 7. Connection Matrix

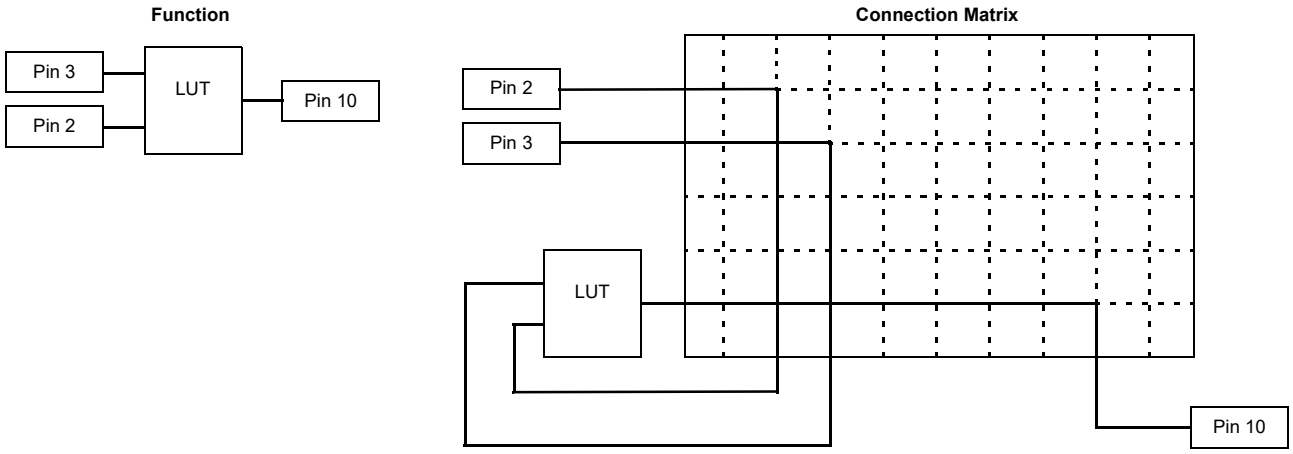


Figure 8. Connection Matrix Example

5.1 Matrix Input Table

Table 11. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode				
		4	3	2	1	0
0	V_{SS}	0	0	0	0	0
1	Pin 2 digital Input	0	0	0	0	1
2	Pin 3 digital Input	0	0	0	1	0
3	Pin 4 digital Input	0	0	0	1	1
4	Pin 6 digital Input	0	0	1	0	0
5	2-bit LUT0 output (DFF/LATCH_0 output)	0	0	1	0	1
6	2-bit LUT1 output (DFF/LATCH_1 output)	0	0	1	1	0
7	2-bit LUT2 output	0	0	1	1	1
8	2-bit LUT3 output	0	1	0	0	0
9	3-bit LUT0 output (DFF/LATCH_2 output with nRST or nSET)	0	1	0	0	1
10	3-bit LUT1 output (DFF/LATCH_3 output with nRST or nSET)	0	1	0	1	0
11	3-bit LUT2 output	0	1	0	1	1
12	3-bit LUT3 output	0	1	1	0	0
13	3-bit LUT4 output (Pipe Delay ouput0)	0	1	1	0	1
14	Pipe Delay ouput1	0	1	1	1	0
15	4-bit LUT0 output (CNT_DLY2 output (8 bit with external clock, reset))	0	1	1	1	1
16	CNT_DLY0 output (8 bit with external clock (shared bottom Delay/CNT), reset)	1	0	0	0	0
17	CNT_DLY1 output (8 bit with external clock (from dedicated matrix output), reset)	1	0	0	0	1
18	CNT_DLY3 (8 bit) output	1	0	0	1	0
19	ACMP_0 output	1	0	0	1	1
20	ACMP_1 output	1	0	1	0	0
21	Edge detect output	1	0	1	0	1
22	Programmable delay with edge detector output (Deglitch Filter output)	1	0	1	1	0
23	Internal oscillator output1 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	0	1	1	1
24	Internal oscillator output2 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	1	0	0	0
25	Bandgap OK signal	1	1	0	0	1
26	POR output to matrix	1	1	0	1	0
27	Pin 8 digital input	1	1	0	1	1
28	Pin 9 digital input	1	1	1	0	0
29	Pin 10 digital input	1	1	1	0	1
30	Pin 12 digital input	1	1	1	1	0
31	V_{DD}	1	1	1	1	1

5.2 Matrix Output Table

Table 12. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[4:0]	Pin 3 digital out source	0
[9:5]	Pin 4 digital out source	1
[14:10]	Pin 6 digital out source	2
[19:15]	Pin 6 output enable	3
[24:20]	In0 of 2-bit LUT0 (Clock Input of DFF0)	4
[29:25]	In1 of 2-bit LUT0 (Data Input of DFF0)	5
[34:30]	In0 of 2-bit LUT1 (Clock Input of DFF1)	6
[39:35]	In1 of 2-bit LUT1 (Data Input of DFF1)	7
[44:40]	In0 of 2-bit LUT2	8
[49:45]	In1 of 2-bit LUT2	9
[54:50]	In0 of 2-bit LUT3	10
[59:55]	In1 of 2-bit LUT3	11
[64:60]	In0 of 3-bit LUT0 (Clock Input of DFF2 with nReset/nSet)	12
[69:65]	In1 of 3-bit LUT0 (Data input of DFF2 with nReset/nSet)	13
[74:70]	In2 of 3-bit LUT0 (nRST or nSET of DFF2 with nReset/nSet)	14
[79:75]	In0 of 3-bit LUT1 (Clock Input of DFF3 with nReset/nSet)	15
[84:80]	In1 of 3-bit LUT1 (Data input of DFF3 with nReset/nSet)	16
[89:85]	In2 of LUT1 (nRST or nSET of DFF3 with nReset/nSet)	17
[94:90]	In0 of 3-bit LUT2	18
[99:95]	In1 of 3-bit LUT2	19
[104:100]	In2 of 3-bit LUT2	20
[109:105]	In0 of 3-bit LUT3	21
[114:110]	In1 of 3-bit LUT3	22
[119:115]	In2 of 3-bit LUT3	23
[124:120]	In0 of 3-bit LUT4 (Input of Pipe Delay)	24
[129:125]	In1 of 3-bit LUT4 (nRST of Pipe Delay)	25
[134:130]	In2 of 3-bit LUT4 (Clock of Pipe Delay)	26
[139:135]	In0 of 4-bit LUT0 (Input for Delay2 external clock or Counter2 external clock)	27
[144:140]	In1 of 4-bit LUT0 (Input for Delay2 or Counter2 reset input)	28
[149:145]	In2 of 4-bit LUT0	29
[154:150]	In3 of 4-bit LUT0	30
[159:155]	Input for Delay0 or Counter0 reset input	31
[164:160]	Input for Delay1 or Counter1 reset input	32
[169:165]	Input for Delay0/1 external clock or Counter1 external clock	33
[174:170]	Input for Delay3 or Counter3 reset input	34
[179:175]	pdb for ACMP0	35
[184:180]	pdb for ACMP1	36

Table 12. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[189:185]	Input for Programmable Delay (Deglitch Filter input)	37
[194:190]	Power-down for OSC (higher priority) (HIGH = power-down)	38
[199:195]	Pin 8 digital out source	39
[204:200]	Pin 9 digital out source	40
[209:205]	Pin 10 digital out source	41
[214:210]	Pin 10 output enable	42
[219:215]	Pin 12 digital out source	43

6. Combinatorial Logic

Combinatorial logic is supported via four Look-up Tables (LUTs) within the SLG46110. There are two 2-bit LUTs and two 3-bit LUTs. The device also includes six combination function macrocells that can be used as LUTs. For more details, please see section 7. Combination Function Macrocells.

Inputs/outputs for the four LUTs are configured from the Connection Matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices: AND, NAND, OR, NOR, XOR, XNOR.

6.1 2-Bit LUT

Two 2-bit LUTs each takes in two input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

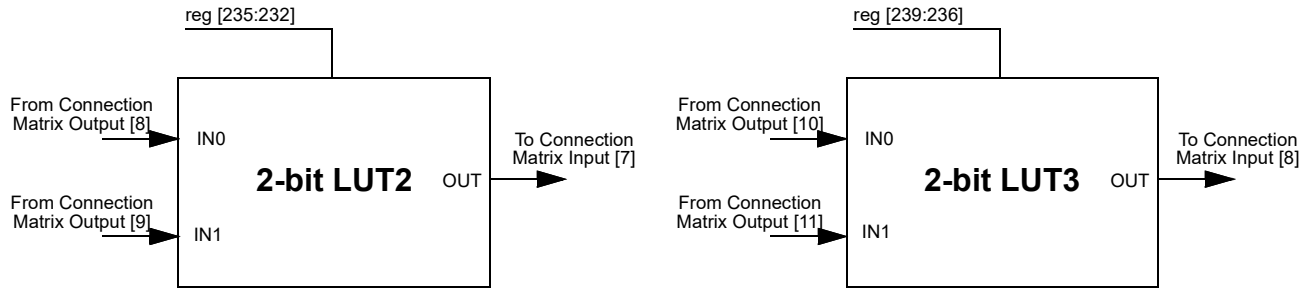


Figure 9. 2-bit LUTs

Table 13. 2-bit LUT2 Truth Table

IN0	IN1	OUT	
0	0	reg [232]	LSB
0	1	reg [233]	
1	0	reg [234]	
1	1	reg [235]	MSB

Table 14. 2-bit LUT3 Truth Table

IN2	IN1	OUT	
0	0	reg [236]	LSB
0	1	reg [237]	
1	0	reg [238]	
1	1	reg [239]	MSB

Each 2-bit LUT uses a 4-bit register signal to define their output functions:

- 2-bit LUT2 is defined by reg [235:232]
- 2-bit LUT3 is defined by reg [239:236]

Table 15 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 15. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

6.2 3-Bit LUT

Two 3-bit LUTs each takes in three input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

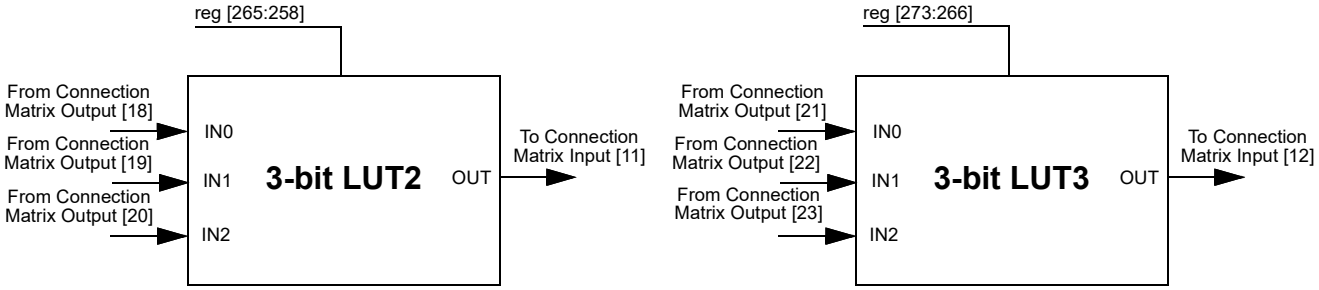


Figure 10. 3-bit LUTs

Table 16. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [258]	LSB
0	0	1	reg [259]	
0	1	0	reg [260]	
0	1	1	reg [261]	
1	0	0	reg [262]	
1	0	1	reg [263]	
1	1	0	reg [264]	
1	1	1	reg [265]	MSB

Table 17. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [266]	LSB
0	0	1	reg [267]	
0	1	0	reg [268]	
0	1	1	reg [269]	
1	0	0	reg [270]	
1	0	1	reg [271]	
1	1	0	reg [272]	
1	1	1	reg [273]	MSB

Each 3-bit LUT uses an 8-bit register signal to define their output functions:

- 3-bit LUT2 is defined by reg [265:258]
- 3-bit LUT3 is defined by reg [273:266]

Table 18 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 3-bit LUT logic cells.

Table 18. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7. Combination Function Macrocells

The SLG46110 has seven Combination Function Macrocells that can serve more than one logic or timing function. In six of these cases, they can serve as a Look-up Table (LUT), or as another logic or timing function. In the last case, it can serve as either a Programmable Delay or Deglitch Filter. See the list below for the functions that can be implemented in these macrocells:

- Two macrocells that can serve as either 2-bit LUTs or as DFF/LATCH.
- Two macrocells that can serve as either 3-bit LUTs or as DFF/LATCH.
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay.
- One macrocells that can serve as either 4-bit LUT or as 8-Bit Counter/Delay.
- One macrocell that can serve as either a Programmable Delay or as a Deglitch Filter.

Inputs/outputs for the seven combination function macrocells are configured from the Connection Matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices: AND, NAND, OR, NOR, XOR, XNOR.

When used as a D Flip-Flop/LATCH, the source and destination of the inputs and outputs for the DFF/LATCHes are configured from the Connection Matrix. All DFF/LATCH macrocells have user selection for initial state, and all have the option to connect both the Q and nQ outputs to the Connection Matrix. The macrocells DFF2, DFF3 have an additional input from the matrix that can serve as an nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.
- LATCH: if CLK = 1, then Q latches D value.

7.1 2-Bit LUT or D Flip-Flop Macrocells

There are two macrocells that can serve as either 2-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 2-bit LUTs each takes in two input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement D Flip-Flop function, the two input signals from the Connection Matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the Connection Matrix.

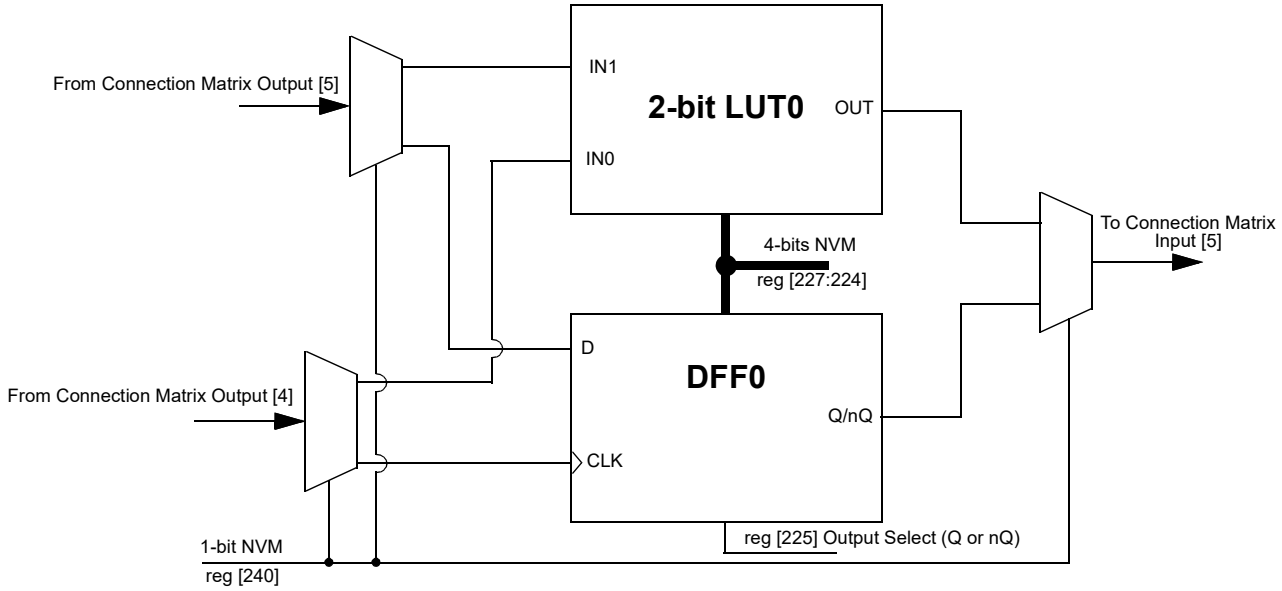


Figure 11. 2-bit LUT0 or DFF0

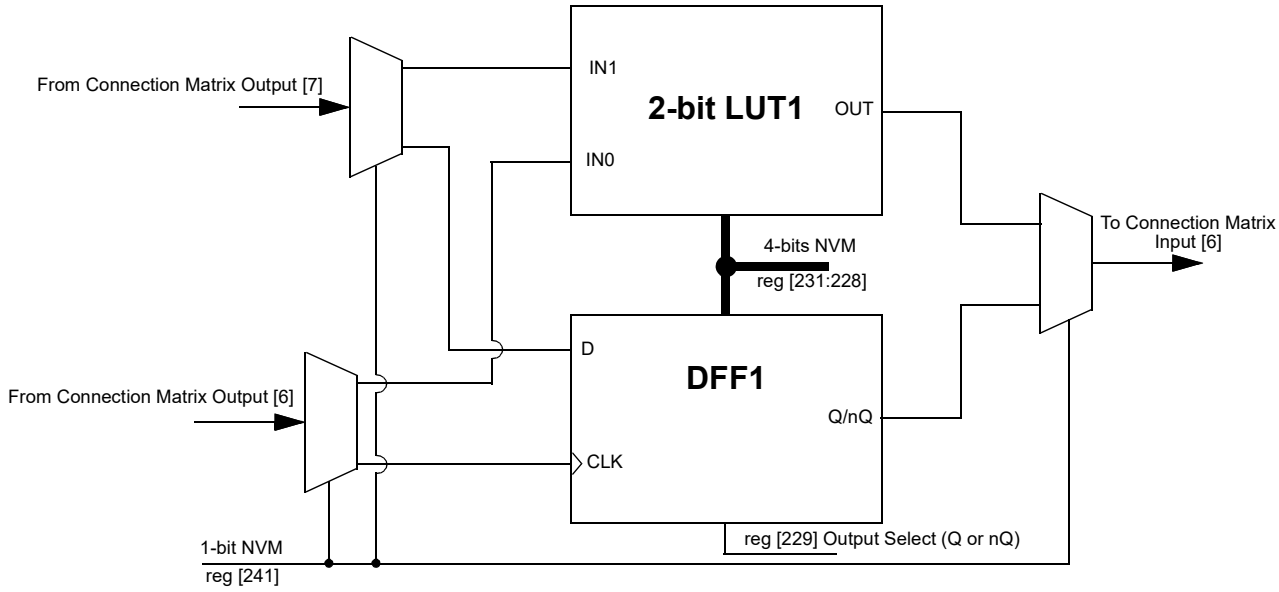


Figure 12. 2-bit LUT1 or DFF1

7.1.1 2-Bit LUT or D Flip-Flop Macrocells Used as 2-Bit LUTs

Table 19. 2-bit LUT0 Truth Table

IN0	IN1	OUT	
0	0	reg [224]	LSB
0	1	reg [225]	
1	0	reg [226]	
1	1	reg [227]	MSB

Table 20. 2-bit LUT1 Truth Table

IN2	IN1	OUT	
0	0	reg [228]	LSB
0	1	reg [229]	
1	0	reg [230]	
1	1	reg [231]	MSB

Each macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-bit LUT0 is defined by reg [227:224]
- 2-bit LUT1 is defined by reg [231:228]

7.1.2 2-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 21. DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF0 or LATCH Select	reg [224]	0: DFF function 1: LATCH function
DFF0 Output Select	reg [225]	0: Q output 1: nQ output
DFF0 Initial Polarity Select	reg [226]	0: LOW 1: HIGH
2-bit LUT0 Data	reg [227:224]	2-bit LUT0 data
2-bit LUT0 or DFF0 Select	reg [240]	0: 2-bit LUT0 1: DFF0

Table 22. DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF1 or LATCH Select	reg [228]	0: DFF function 1: LATCH function
DFF1 Output Select	reg [229]	0: Q output 1: nQ output
DFF1 Initial Polarity Select	reg [230]	0: LOW 1: HIGH
2-bit LUT1 Data	reg [231:228]	2-bit LUT1 data
2-bit LUT1 or DFF1 Select	reg [241]	0: 2-bit LUT1 1: DFF1

7.2 3-Bit LUT or D Flip-Flop with nSet/nReset Macrocells

There are two macrocells that can serve as either 3-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement D Flip-Flop function, the three input signals from the Connection Matrix go to the data (D) and clock (CLK), and nRST/nSET inputs for the Flip-Flop, with the output going back to the Connection Matrix.

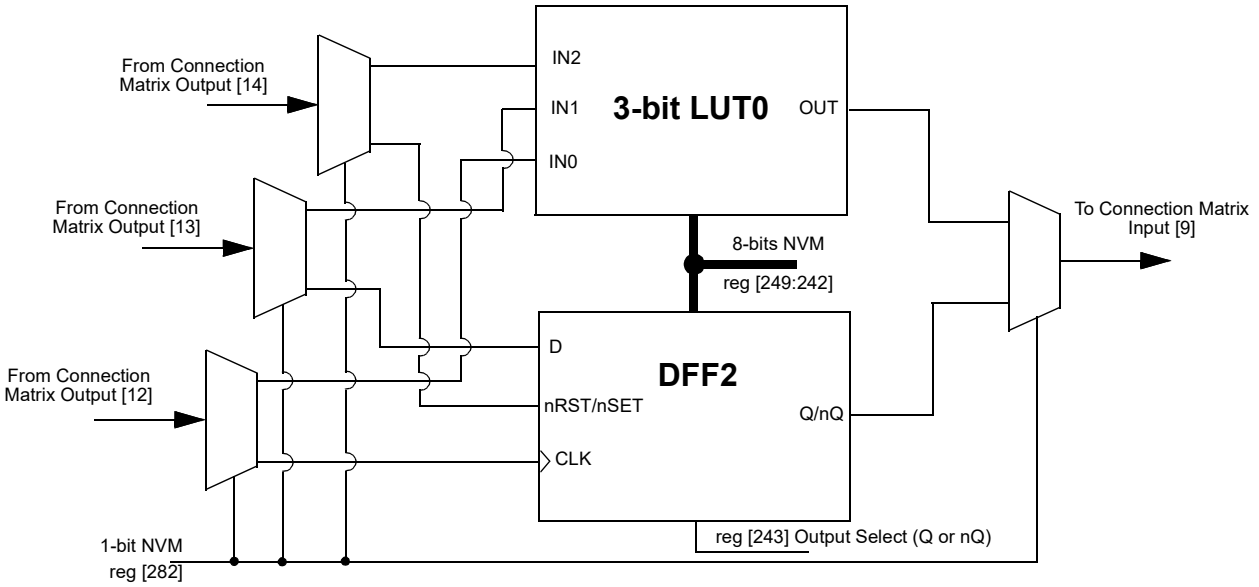


Figure 13. 3-bit LUT0 or DFF2

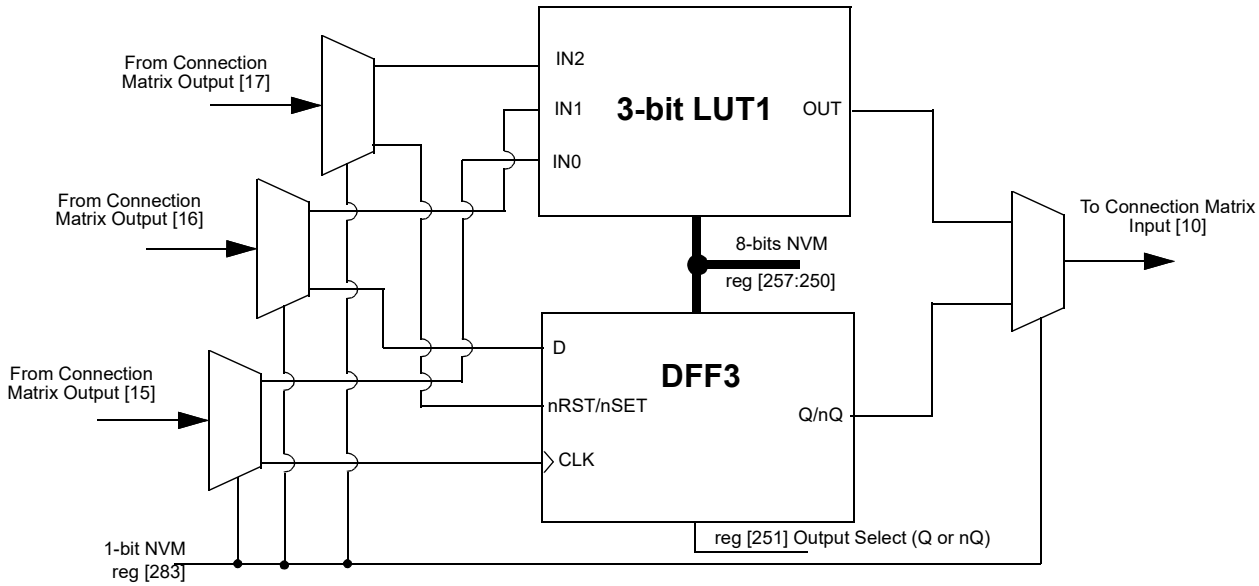


Figure 14. 3-bit LUT1 or DFF3

7.2.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 23. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [242]	LSB
0	0	1	reg [243]	
0	1	0	reg [244]	
0	1	1	reg [245]	
1	0	0	reg [246]	
1	0	1	reg [247]	
1	1	0	reg [248]	
1	1	1	reg [249]	MSB

Table 24. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [250]	LSB
0	0	1	reg [251]	
0	1	0	reg [252]	
0	1	1	reg [253]	
1	0	0	reg [254]	
1	0	1	reg [255]	
1	1	0	reg [256]	
1	1	1	reg [257]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT2 is defined by reg [249:242]
- 3-bit LUT3 is defined by reg [257:250]

7.2.2 3-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 25. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF2 or LATCH Select	reg [242]	0: DFF function 1: LATCH function
DFF2 Output Select	reg [243]	0: Q output 1: nQ output
DFF2 Initial Polarity Select	reg [244]	0: LOW 1: HIGH
DFF2 nRST/nSET Select	reg [245]	1: nSET from matrix out 0: nRST from matrix out
3-bit LUT0 Data	reg [265:258]	3-bit LUT0 data
3-bit LUT0 or DFF2 Select	reg [282]	0: 3-bit LUT0 1: DFF2

Table 26. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF3 or LATCH Select	reg [250]	0: DFF function 1: LATCH function
DFF3 Output Select	reg [251]	0: Q output 1: nQ output
DFF3 nRST/nSET Select	reg [252]	1: nSET from matrix out 0: nRST from matrix out
DFF3 Initial Polarity Select	reg [253]	0: LOW 1: HIGH
3-bit LUT1 Data	reg [273:266]	3-bit LUT1 data
3-bit LUT1 or DFF3 Select	reg [283]	0: 3-bit LUT1 1: DFF3

7.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

When used as an 8-stage Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nReset). The Pipe Delay cell is built from D Flip-Flop logic cells that provide the three delay options, two of which are user-selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The two outputs (OUT0 and OUT1) provide user-selectable options for one to eight stages of delay. Each set of the OUT0 and OUT1 outputs includes delay output points connected to a 3-input MUX. The MUX is controlled by reg [666:663] for OUT0 and reg [670:667] for OUT1.

The 3-input MUX is used to select one of the available delay values.

The overall time of the delay is based on the clock used in the SLG46110 design. Each DFF cell introduces a delay equal to one clock period, where the clock source is either an external clock or the RC oscillator within the SLG46110. The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

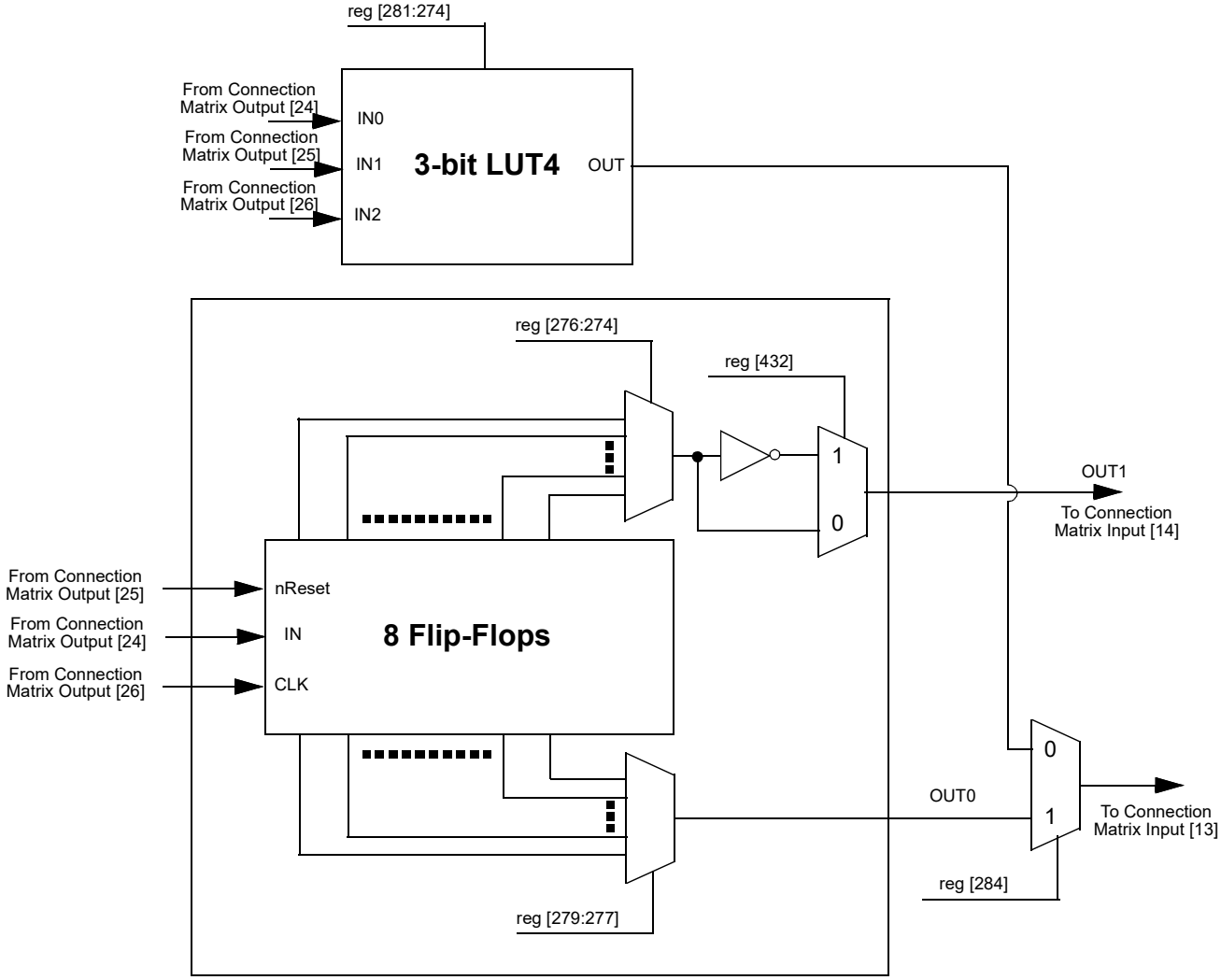


Figure 15. 3-bit LUT4 or Pipe Delay

7.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 27. 3-Bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg [274]	LSB
0	0	1	reg [275]	
0	1	0	reg [276]	
0	1	1	reg [277]	
1	0	0	reg [278]	
1	0	1	reg [279]	
1	1	0	reg [280]	
1	1	1	reg [281]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-bit LUT4 is defined by reg [281:274]

7.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 28. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 Select	reg [276:274]	Data (pipe number)
OUT1 Select	reg [279:277]	Data (pipe number)
3-bit LUT4 or Pipe Delay Output Select	reg [284]	0: 3-bit LUT4 1: Pipe Delay

7.4 4-Bit LUT or 8-Bit Counter/Delay Macrocells

There is one macrocell that can serve as either a 4-bit LUT or as a Counter/Delay. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 8-bit Counter/Delay function, two of the four input signals from the Connection Matrix go to the external clock (ext_clk) and reset (DLY_n/CNT_Reset) for the Counter/Delay, with the output going back to the Connection Matrix.

Note: Counters initialize with counter data after POR.

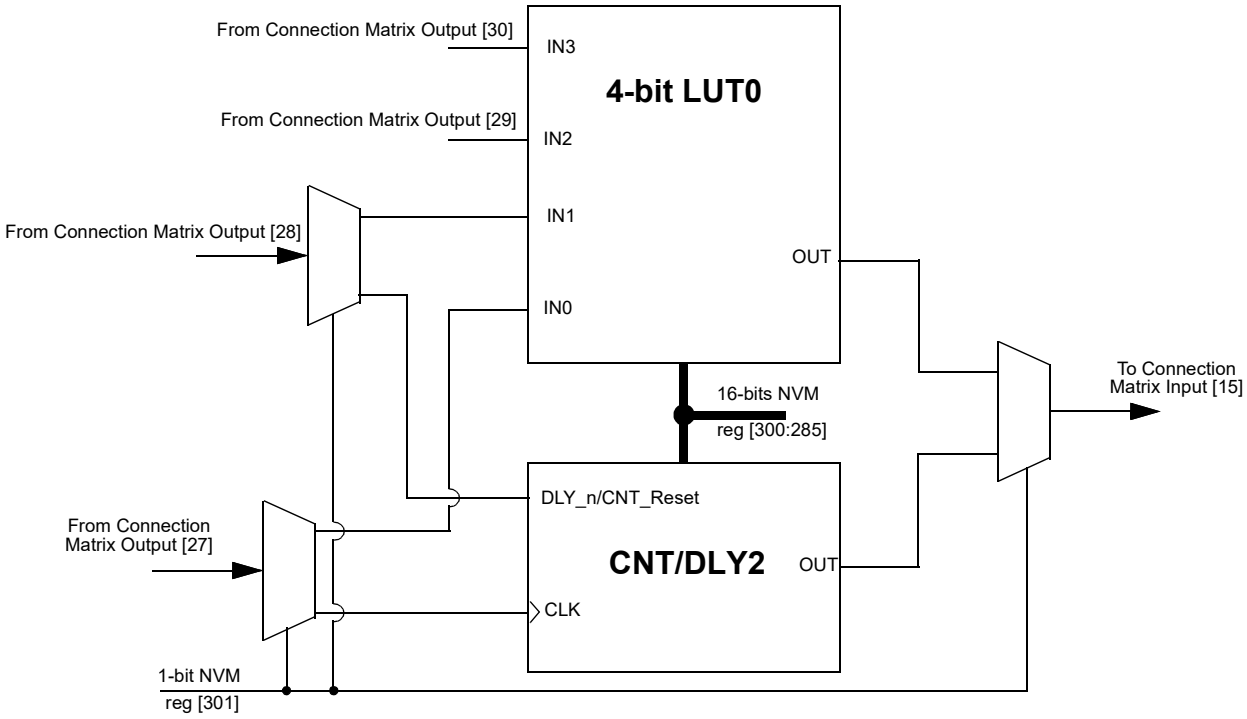


Figure 16. 4-bit LUT0 or CNT/DLY2

7.4.1 4-Bit LUT or 8-Bit Counter/Delay Macrocell Used as 4-Bit LUT

Table 29. 4-Bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	reg [285]	LSB
0	0	0	1	reg [286]	
0	0	1	0	reg [287]	
0	0	1	1	reg [288]	
0	1	0	0	reg [289]	
0	1	0	1	reg [290]	
0	1	1	0	reg [291]	
0	1	1	1	reg [292]	
1	0	0	0	reg [293]	
1	0	0	1	reg [294]	
1	0	1	0	reg [295]	
1	0	1	1	reg [296]	
1	1	0	0	reg [297]	
1	1	0	1	reg [298]	
1	1	1	0	reg [299]	
1	1	1	1	reg [300]	MSB

Each macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-bit LUT0 is defined by reg [300:285]

Table 30. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.4.2 4-bit LUT or 8-Bit Counter/Delay Macrocells Used as 8-Bit Counter/Delay Register Settings

Table 31. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay2 Mode Selection	reg [285]	0: Delay mode 1: Counter mode
Counter/Delay2 Clock Source Select	reg [288:286]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter1 overflow
Counter/Delay2 Control Data	reg [296:289]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay2 Mode Select or Asynchronous Counter Reset	reg [298:297]	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high-level reset for counter mode
4-bit LUT0 or Counter2 Select	reg [301]	0: 4-bit LUT0 1: Counter2

7.5 Programmable Delay/Edge Detector

The SLG46110 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 18 and Figure 19 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

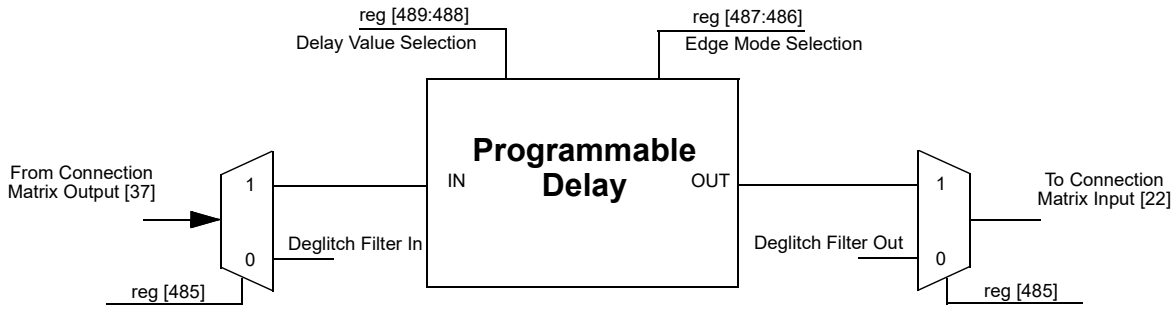


Figure 17. Programmable Delay

7.5.1 Programmable Delay Timing Diagram – Edge Detector Output

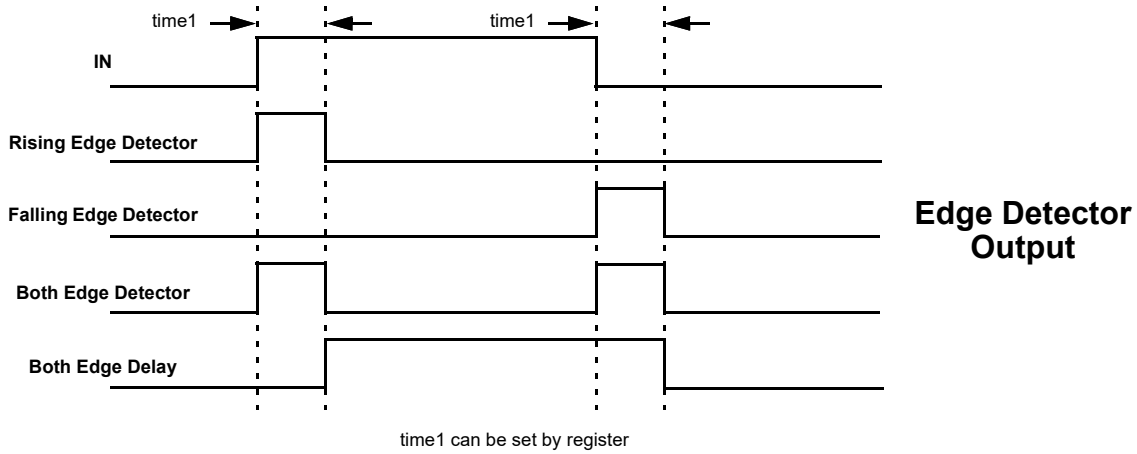


Figure 18. Edge Detector Output

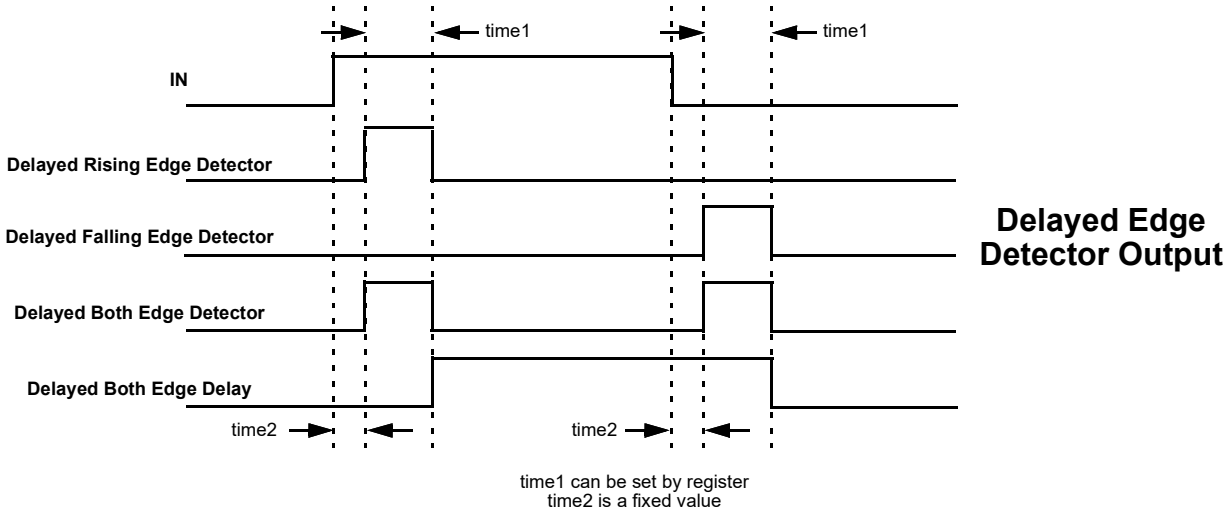


Figure 19. Delayed Edge Detector Output

Note: For delays and widths refer to section 3.4.5 Programmable Delay Typical Delays and Widths.

7.5.2 Programmable Delay Register Settings

Table 32. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Programmable Delay or Filter Output Select	reg [485]	0: Programmable delay output 1: Filter output
Select the Edge Mode of Programmable Delay and Edge Detector	reg [487:486]	00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
Delay Value Select for Programmable Delay and Edge Detector (V_{DD} = 3.3 V, Typical Condition)	reg [489:488]	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns

7.6 Deglitch Filter

The SLG46110 has an additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one Deglitch Filter.

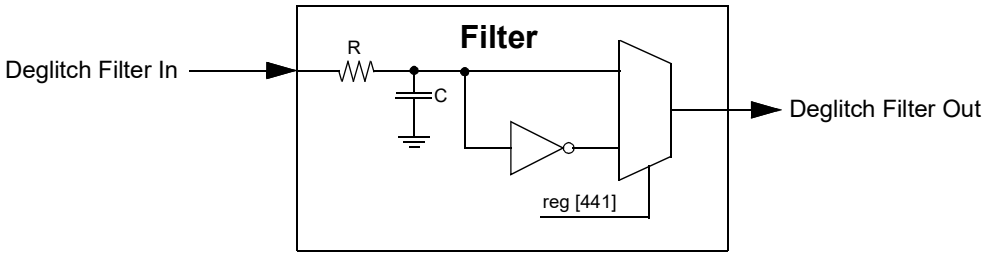


Figure 20. Deglitch Filter

8. Analog Comparators

There are two Analog Comparator (ACMP) macrocells in the SLG46110. In order for the ACMP cells to be used in a GreenPAK design, the power-up signals (ACMP0_pdb and ACMP1_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is LOW.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the Analog Comparator. Each ACMP cell has a negative input signal that is generated either by an internal V_{REF} source or by an external source.

Each of the ACMP cells has a selection for the bandwidth of the input signal, which can be used to save power when low-bandwidth signals are input into the Analog Comparator. And if input frequency > 200 kHz, the output will retain its previous value. Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV, or 200 mV.

During power-up, the ACMP output will remain LOW, and then become valid 110 µs (max) after POR signal goes HIGH, see Figure 21.

Note: Regulator and Charge Pump set to automatic ON/OFF.

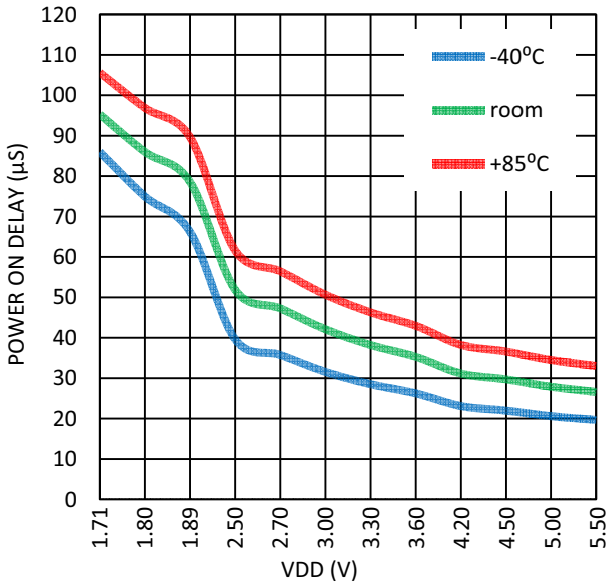


Figure 21. Maximum Power-on Delay vs. V_{DD}

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the Analog Comparator. The gain divider is unbuffered and consists of 250 kΩ (typ.) resistors, see Table 33. IN- voltage range: 0 V - 1.2 V. V_{REF} selection $V_{DD}/4$ and $V_{DD}/3$ can be used to maintain this input range.

Table 33. Gain Divider Input Resistance (typ.)

Gain	1x	0.5x	0.33x	0.25x
Input Resistance	100 MΩ	1 MΩ	0.75 MΩ	1 MΩ

Each of the ACMP cells has a negative input signal that is either created from an internal V_{REF} or provided by the external reference/source. Internal V_{REF} accuracy is optimized near 1000 mV selection.

Note 1: Power supply control options have influence on the ACMP operation.

Note 2: Enabling any ACMP also enables the internal Bandgap circuit. As a result, an analog voltage appears on V_{REF} even when the Force Bandgap option is disabled.

Analog Comparators have the following configurable options:

- Hysteresis: Input signal hysteresis options are Disable, 25 mV, 50 mV, 200 mV
- Low Bandwidth: Enable, Disable
- IN+ Gain: 1x, 0.5x, 0.33x, 0.25x
- IN+ source
  - ACMP0 IN+ options are Pin 3, V_{DD}
  - ACMP1 IN+ options are Pin 6, ACMP0 IN+
- IN- source
  - ACMP0 IN- options are 24 internal reference sources (50 mV to 1200 mV) and $V_{DD}/3$, $V_{DD}/4$, Pin 4
  - PWR UP = 0 – ACMP is powered down; PWR UP = 1 – ACMP is powered up

All ACMPs can have a common negative input. This can be achieved by configuring ACMP0 Pin 4 analog IO connection.

8.1 ACMP0 Block Diagram

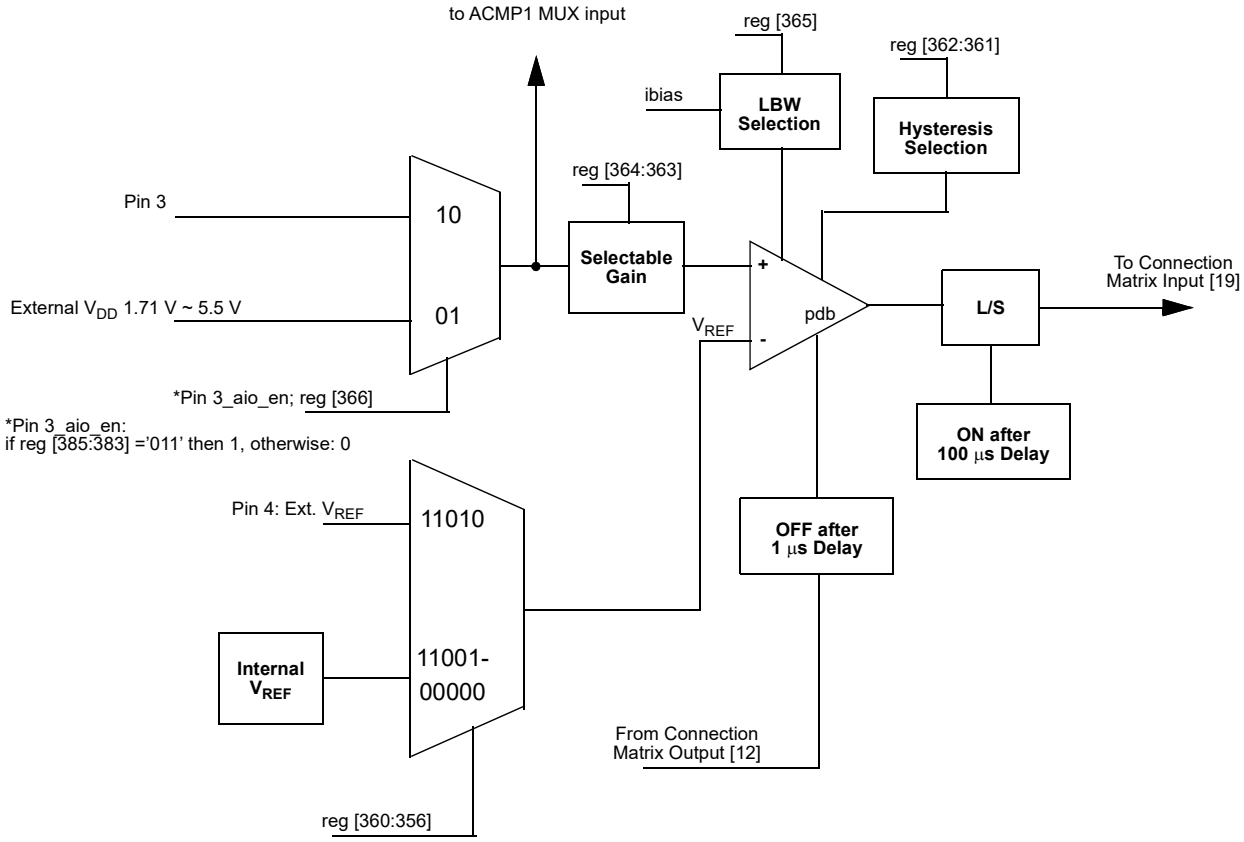


Figure 22. ACMP0 Block Diagram

8.2 ACMP0 Register Settings

Table 34. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 In Voltage Select	reg [360:356]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: EXT_VREF (Pin 4)
ACMP0 Hysteresis Enable	reg [362:361]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP0 Positive Input Divider	reg [364:363]	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg [365]	0: Off 1: On
ACMP0 Positive Input Source Select Pin 3 and V_{DD}	reg [366]	0: Pin 3 1: V_{DD}

8.3 ACMP1 Block Diagram

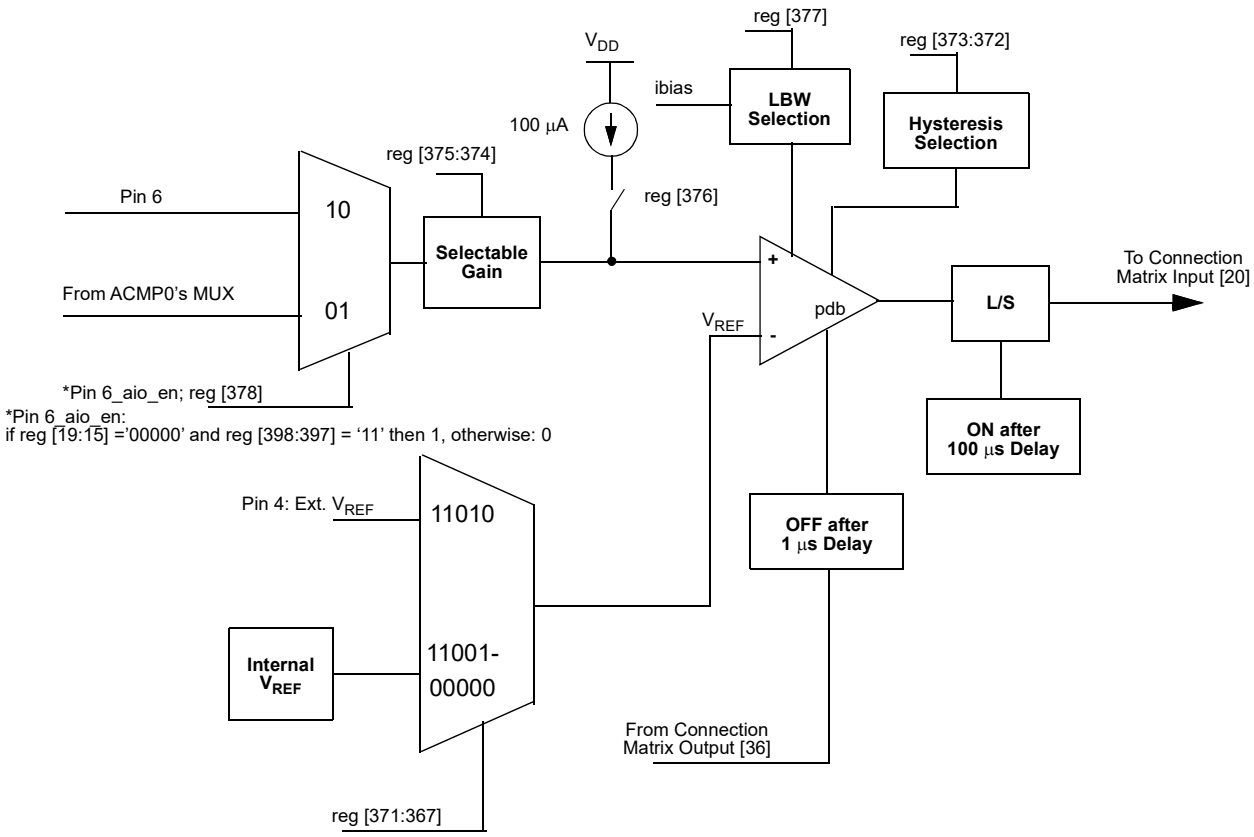


Figure 23. ACMP1 Block Diagram

8.4 ACMP1 Register Settings

Table 35. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 In Voltage Select	reg [371:367]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: EXT_VREF (Pin 4)
ACMP1 Hysteresis Enable	reg [373:372]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP1 Positive Input Divider	reg [375:374]	00: 1.x 01: 0.5x 10: 0.33x 11: 0.25x
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg [377]	1: On 0: Off
ACMP1 Positive Input Source Select Pin 3 and Pin 6	reg [378]	0: Pin 6 1: Pin 3

8.5 Typical Performance Characteristics

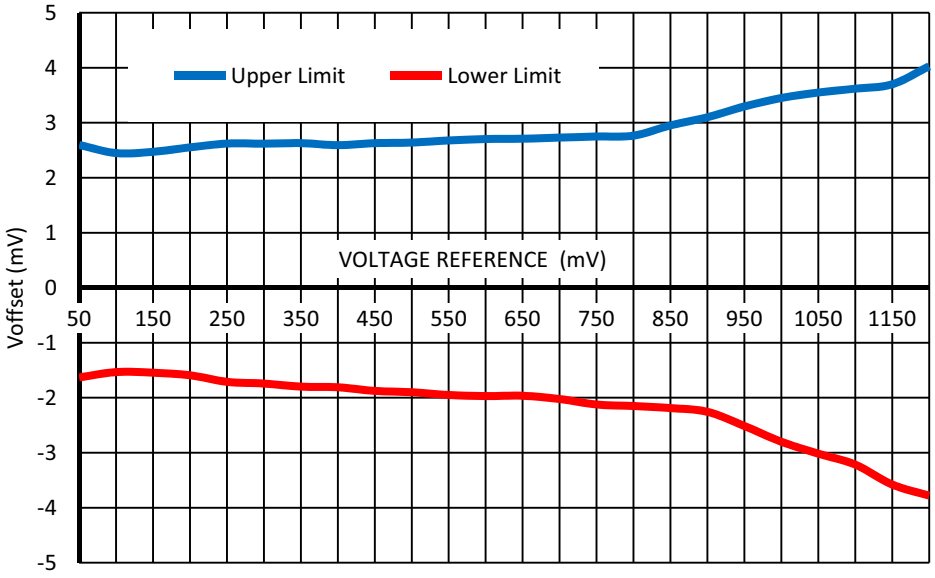


Figure 24. Typical Input Voltage Offset vs. V_{REF} at Room Temp., LBW Mode – Disable, V_{HYS} = 0 mV, V_{DD} = 1.7 V to 5.5 V

Note: When V_{DD} < 1.8 V voltage reference should not exceed 1100 mV.

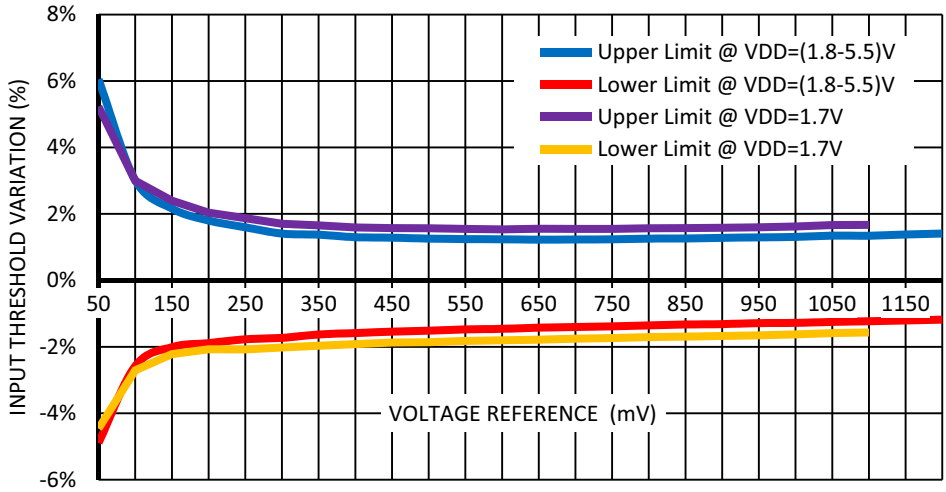


Figure 25. Typical Input Threshold Variation (Including V_{REF} Variation, ACMP Offset) vs. V_{REF} at Room Temp., LBW Mode – Disable, V_{HYS} = 0 mV

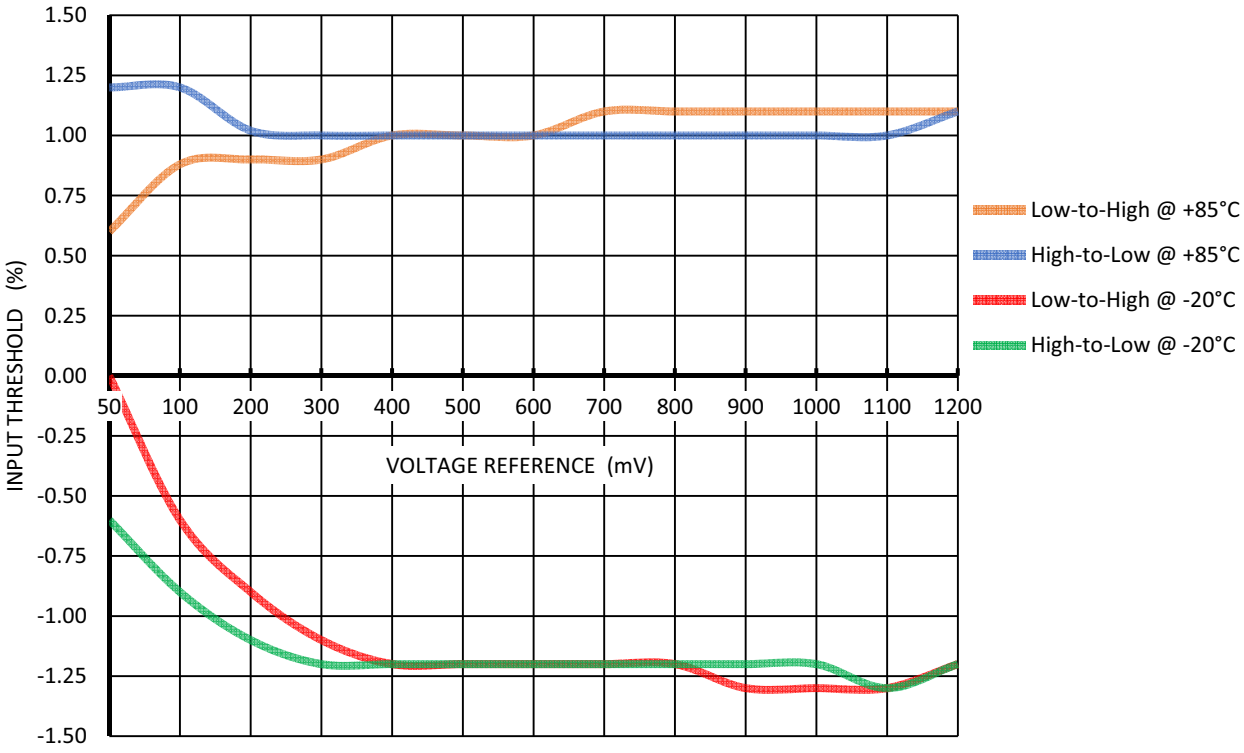


Figure 26. Input Threshold Ratio vs. V_{REF} at V_{DD} = 1.71 V to 5.5 V, V_{HYS} = 0, Gain = 1

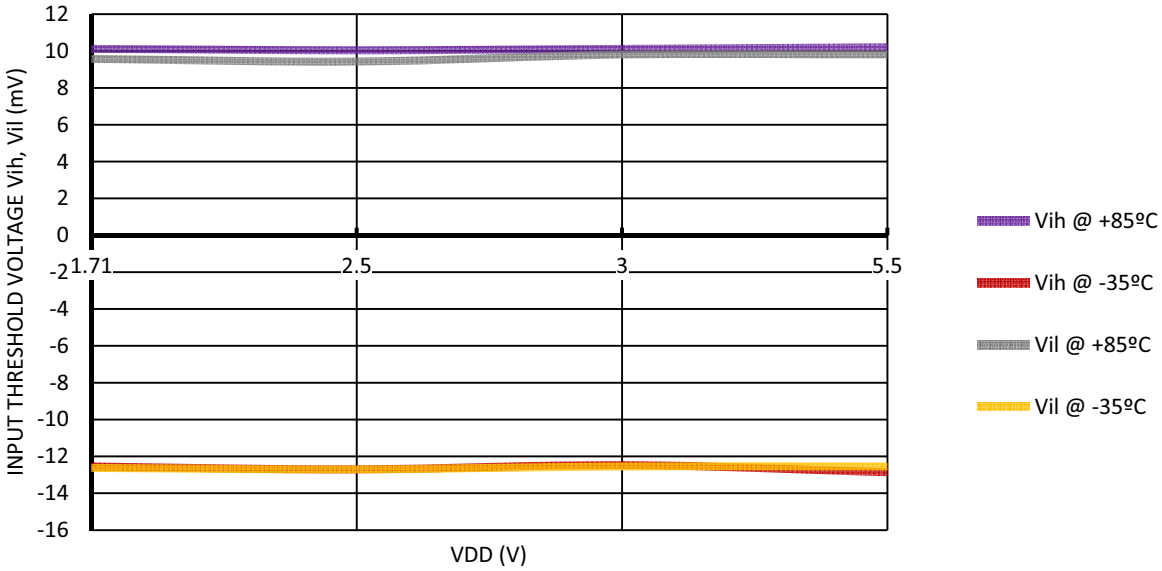


Figure 27. Input Threshold Voltage V_{IH}, V_{IL} vs. V_{DD} at V_{REF} = 1000 mV, Gain = 1

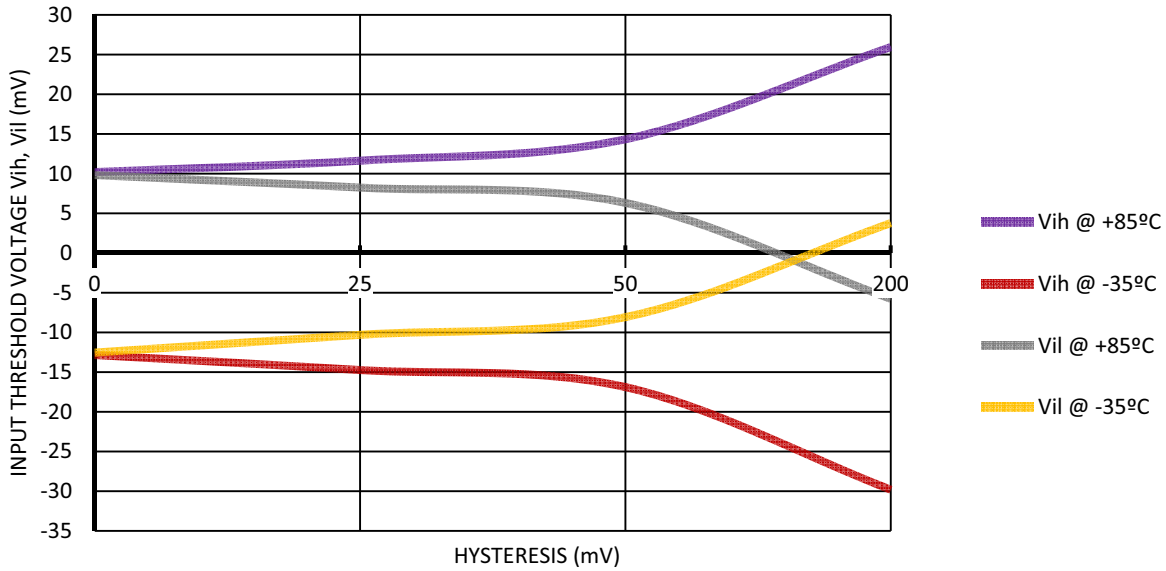


Figure 28. Input Threshold Voltage V_{IH}, V_{IL} vs. Hysteresis at V_{DD} = 5.5 V, V_{REF} = 1000 mV, Gain = 1

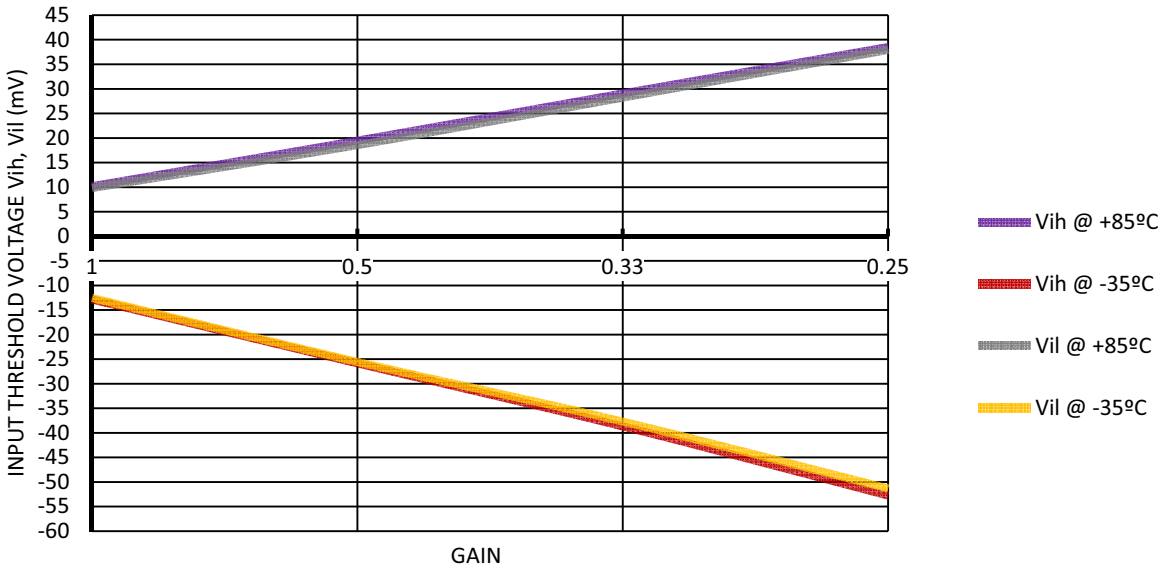


Figure 29. Input Threshold Voltage V_{IH}, V_{IL} vs. Gain at Hysteresis = 0, V_{DD} = 5.5 V, V_{REF} = 1000 mV

Table 36. Built-in Hysteresis Tolerance

V_{HYS} (mV)	V_{DD} = 1.7 V to 1.8 V						V_{DD} = 1.89 V to 5.5 V					
	V_{REF} = 50 mV to 500 mV		V_{REF} = 550 mV to 1000 mV		V_{REF} = 1050 mV to 1200 mV		V_{REF} = 50 mV to 500 mV		V_{REF} = 550 mV to 1000 mV		V_{REF} = 1050 mV to 1200 mV	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
25	18.9	26.4	17.3	26.1	13.0	24.6	18.8	26.5	17.8	26.1	15.6	25.5
50	40.3	50.4	37.9	50.1	28.9	47.7	40.3	50.5	39.5	50.1	34.5	49.5
200	180.5	208.4	172.9	210.7	153.5	217.2	180.6	207.7	180.2	210.8	166.5	211.9

8.6 Timing Characteristics

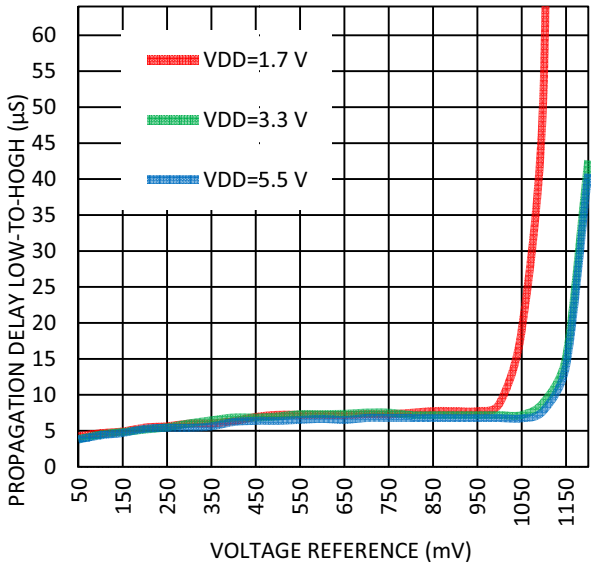


Figure 30. Maximum Propagation Delay Low-to-High vs. V_{REF} at Room Temp., Vod = 2 mV

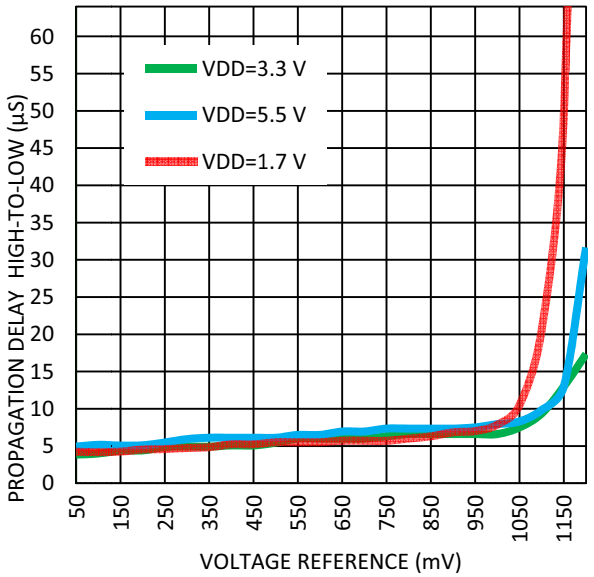


Figure 32. Maximum Propagation Delay High-to-Low vs. V_{REF} at Room Temp., Vod = 2 mV

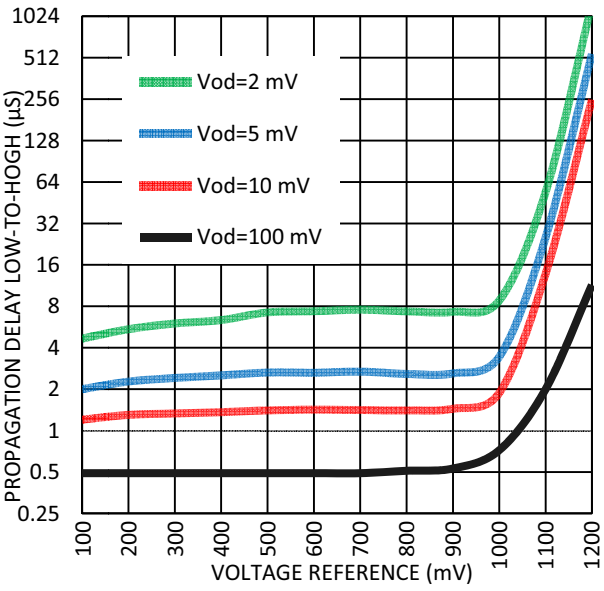


Figure 31. Maximum Propagation Delay Low-to-High vs. V_{REF} at Room Temp., V_{DD} = 1.71 V to 1.89 V

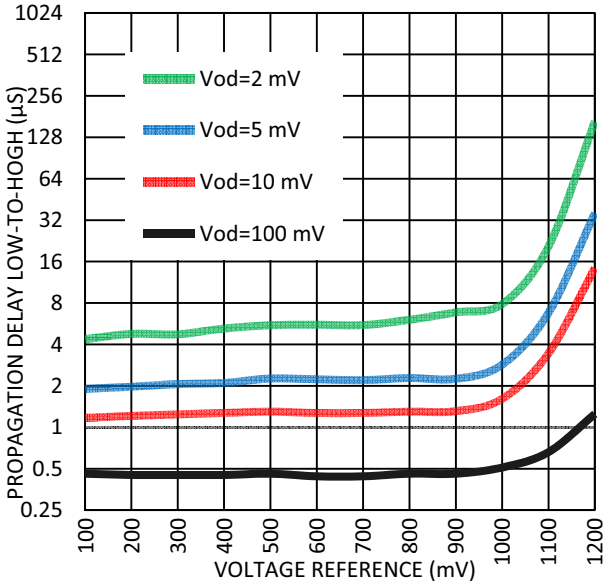


Figure 33. Maximum Propagation Delay High-to-Low vs. V_{REF} at Room Temp., V_{DD}= 1.71 V to 1.89 V

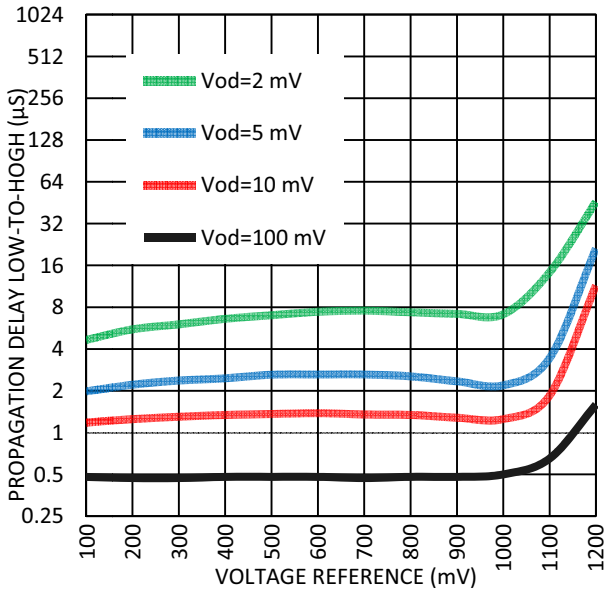


Figure 34. Maximum Propagation Delay Low-to-High vs. V_{REF} at Room Temp., V_{DD} = 1.89 V to 3.6 V

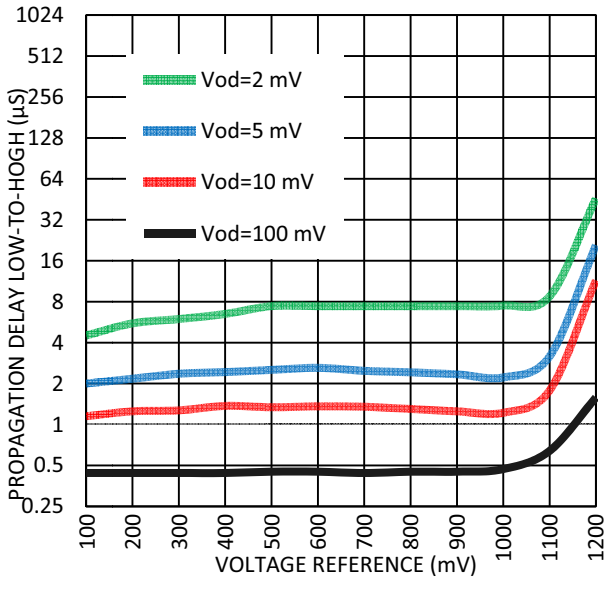


Figure 35. Maximum Propagation Delay Low-to-High vs. V_{REF} at Room Temp., V_{DD} = 3.6 to 5.5 V

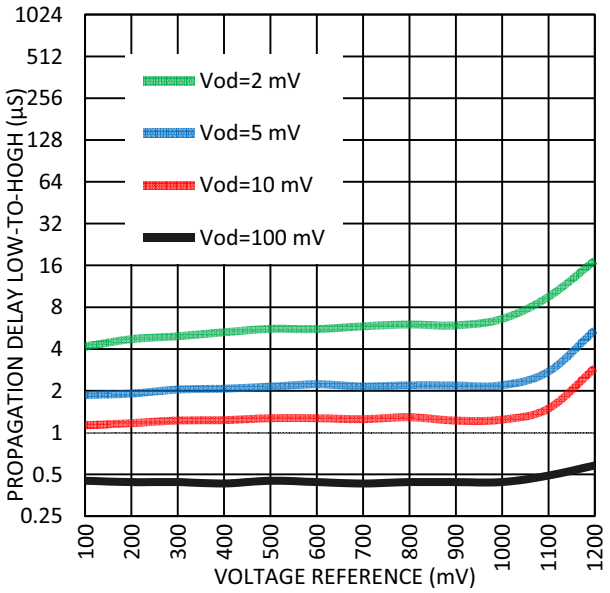


Figure 36. Maximum Propagation Delay High-to-Low vs. V_{REF} at Room Temp., V_{DD} = 1.89 V to 3.6 V

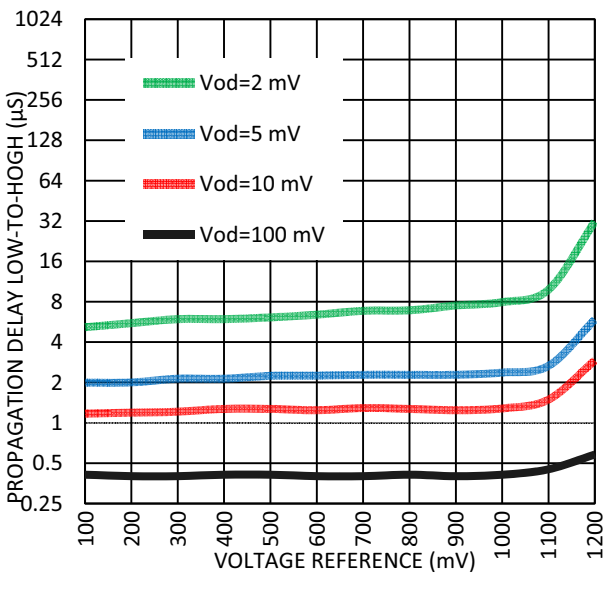


Figure 37. Maximum Propagation Delay High-to-Low vs. V_{REF} at Room Temp., V_{DD} = 3.6 V to 5.5 V

9. Counters/Delay Generators

There are three configurable counters/delays (CNT/DLY) generators in the SLG46110. The three counters/delay generators (CNT/DLY0, CNT/DLY1, and CNT/DLY3) are 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits.

Two of the counter/delay generator macrocells (CNT/DLY0 and CNT/DLY1) have two inputs from the Connection Matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. One of the counter/delay generator macrocells (CNT/DLY3) has one input from the Connection Matrix, which has a shared function of either a Delay Input or an external clock input.

Note that there is also one combination function macrocells that can implement either 4-bit LUTs or 8-bit counter/delays. For more information, see section 7.4 4-Bit LUT or 8-Bit Counter/Delay Macrocells.

Note: Counters initialize with counter data after POR.

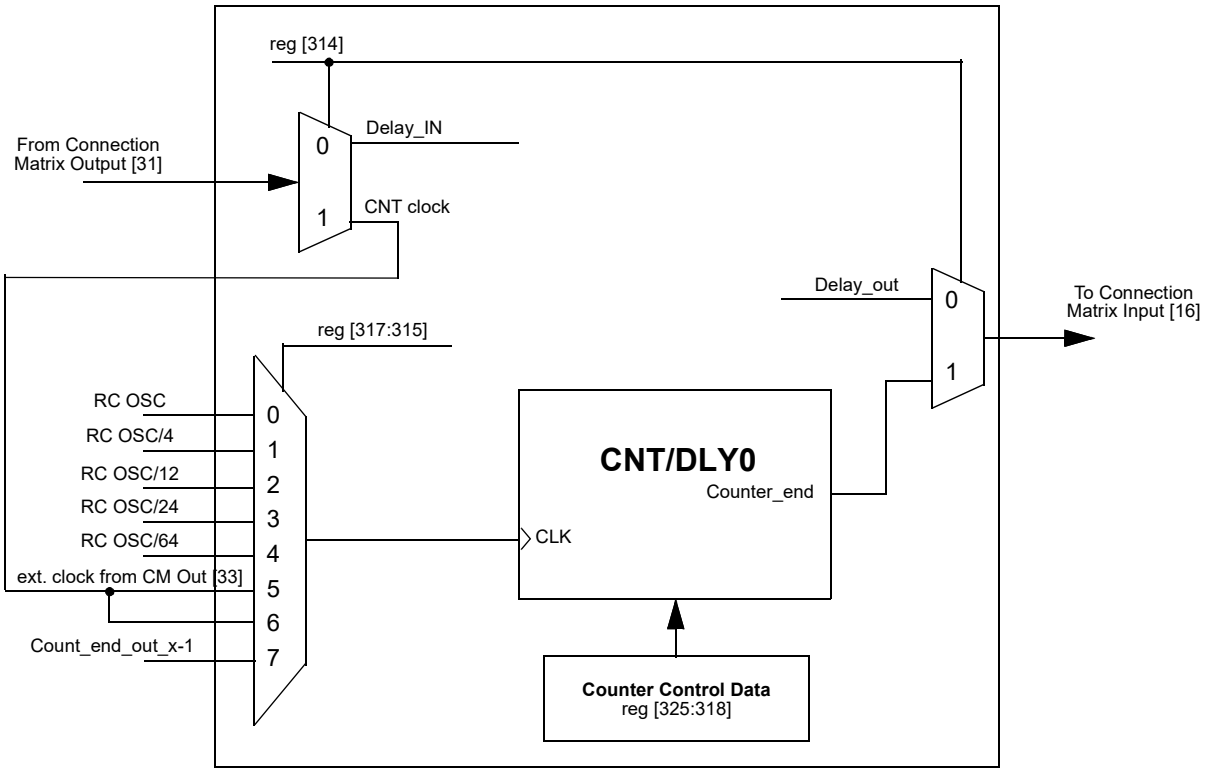


Figure 38. CNT/DLY0

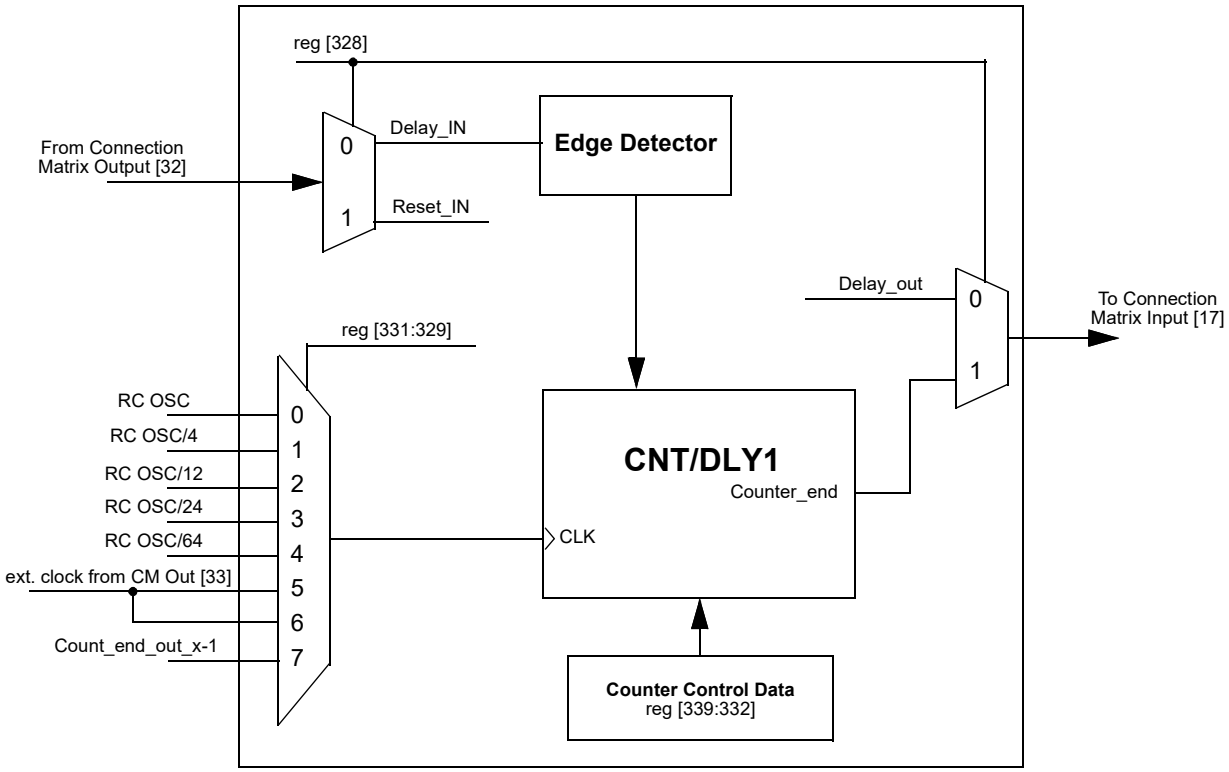


Figure 39. CNT/DLY1

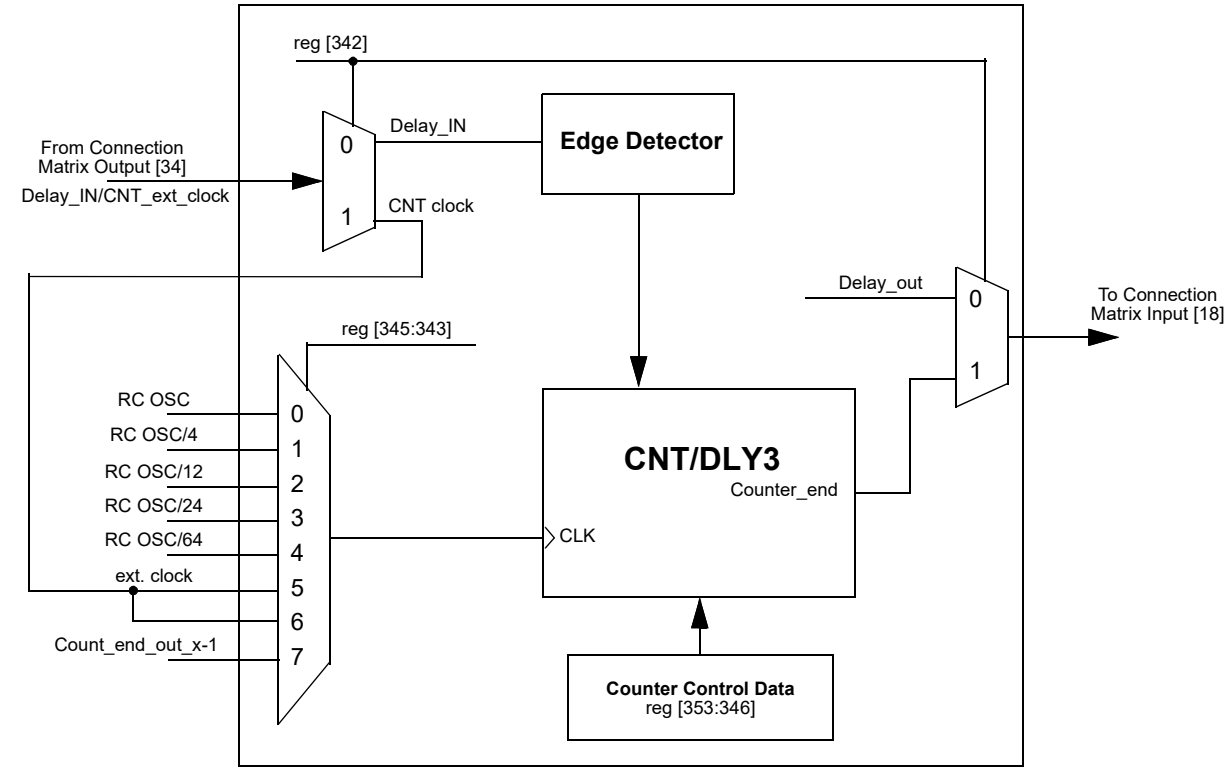


Figure 40. CNT/DLY3

9.1 CNT/DLY0 Register Settings

Table 37. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	reg [314]	0: Delay Mode 1: Counter Mode
Counter/Delay0 Clock Source Select (External Clock Is Only for Counter Mode)	reg [317:315]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter3 overflow
Counter0 Control Data/Delay0 Time Control	reg [325:318]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay0 Mode Select or Asynchronous Counter Reset	reg [327:326]	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high-level reset for counter mode

9.2 CNT/DLY1 Register Settings

Table 38. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg [328]	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source Select (External Clock Is Only for Counter Mode)	reg [331:329]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter0 overflow
Counter1 Control Data/Delay1 Time Control	reg [339:332]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay1 Mode Select or Asynchronous Counter Reset	reg [341:340]	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high-level reset for counter mode

9.3 CNT/DLY3 Register Settings

Table 39. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay3 Mode Select	reg [342]	0: Delay Mode 1: Counter Mode
Counter/Delay3 Clock Source Select (External Clock Is Only for Counter Mode)	reg [345:343]	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter2 Overflow
Counter3 Control Data/Delay3 Time Control	reg [353:346]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay3 Mode Select	reg [355:354]	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

10. Voltage Reference

10.1 Voltage Reference Overview

The SLG46110 has a Voltage Reference (V_{REF}) macrocell to provide references to the two Analog Comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from Pin 4. The macrocell also has the option to output reference voltages on Pin 10. See Table 40 for the available selections for each Analog Comparator. Also, see Figure 41, which shows the reference output structure.

10.2 V_{REF} Selection Table

Table 40. V_{REF} Selection Table

SEL[4:0]	CMP0_V_{REF}	CMP1_V_{REF}
11010	External V_{REF} (Pin 4)	External V_{REF} (Pin 4)
11001	V_{DD}/4	V_{DD}/4
11000	V_{DD}/3	V_{DD}/3
10111	1.20 V	1.20 V
10110	1.15 V	1.15 V
10101	1.10 V	1.10 V
10100	1.05 V	1.05 V
10011	1.00 V	1.00 V
10010	0.95 V	0.95 V
10001	0.90 V	0.90 V
10000	0.85 V	0.85 V
01111	0.80 V	0.80 V
01110	0.75 V	0.75 V
01101	0.70 V	0.70 V
01100	0.65 V	0.65 V
01011	0.60 V	0.60 V
01010	0.55 V	0.55 V
01001	0.50 V	0.50 V
01000	0.45 V	0.45 V
00111	0.40 V	0.40 V
00110	0.35 V	0.35 V
00101	0.30 V	0.30 V
00100	0.25 V	0.25 V
00011	0.20 V	0.20 V
00010	0.15 V	0.15 V
00001	0.10 V	0.10 V
00000	0.05 V	0.05 V

Table 41. V_{REF} Operating Rage

V_{DD}	Practical V_{REF} Range	Note
2.0 V - 5.5 V	50 mV ~1.2 V	
1.7 V - 2.0 V	50 mV ~1.1 V	Higher than 1.1 V negative input, the comparator may show wrong result.

10.3 V_{REF} Block Diagram

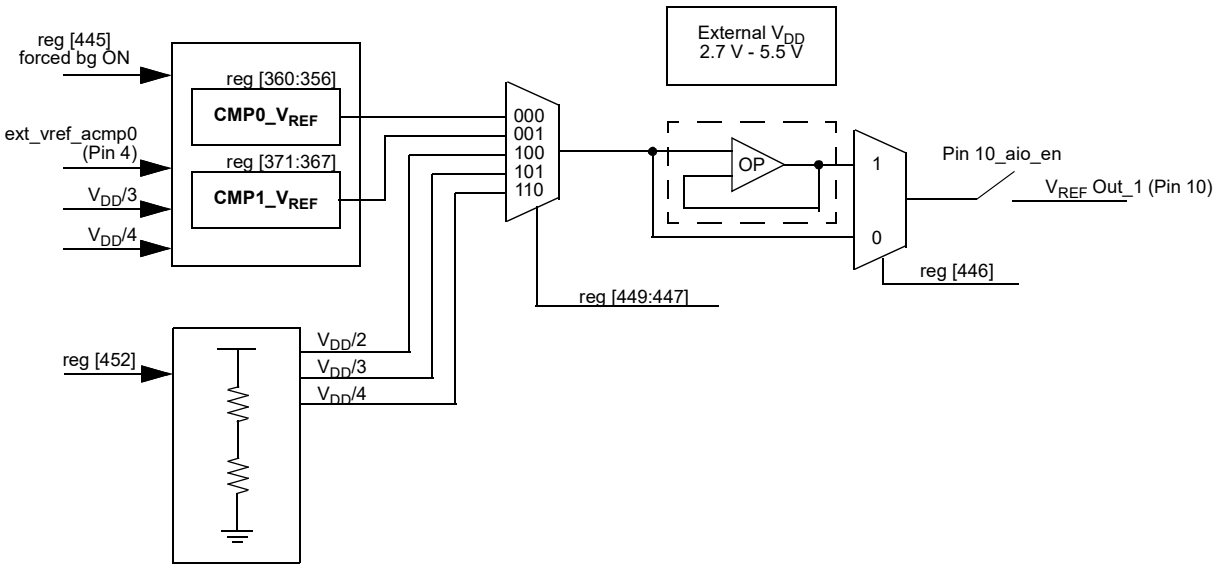


Figure 41. Voltage Reference Block Diagram

11. RC Oscillator

11.1 RC Oscillator Overview

The SLG46110 has one internal RC oscillators, that runs at 25 kHz or at 2 MHz. When using the chip internal RC OSC, a choice is available to Force Power-on, meaning that the RC OSC will always run, or Auto Power-on, meaning that the RC OSC will have an associated startup and settling time associated with it (offset). Figure 42 and Figure 43 show maximum power-on delay vs. V_{DD}.

Note: RC OSC power setting: Auto Power-on.

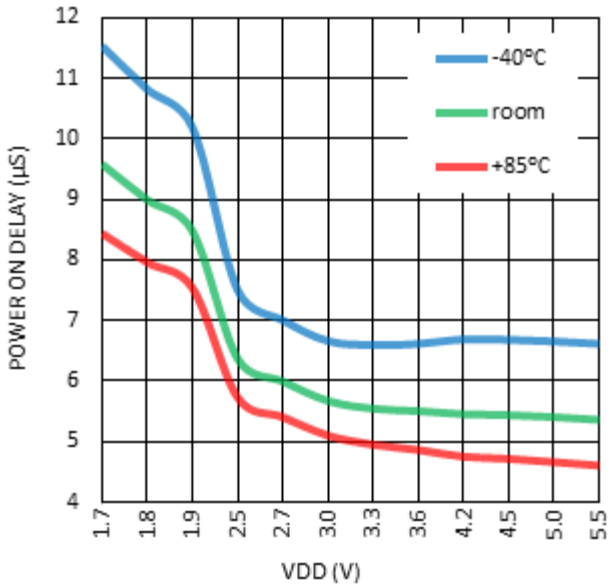


Figure 42. Maximum Power-on Delay vs. V_{DD}, RC OSC = 2 MHz

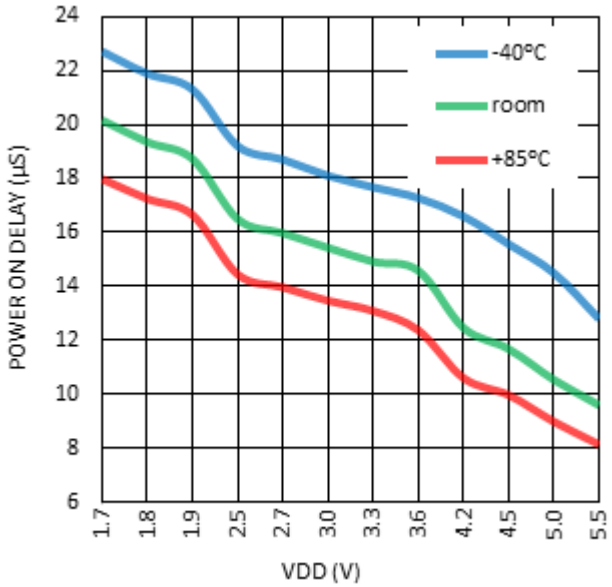


Figure 43. Maximum Power-on Delay vs. V_{DD}, RC OSC = 25 kHz

The user can select one of these fundamental frequencies for the OSC macrocell, or the fundamental frequency can also come from an external clock input (Pin 12). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix input lines. The first stage divider (also known as the clock

pre-divider) allows the selection of /1, /2, /4, or /8 divide down frequency from the fundamental. There are two second stage divider controls (OUT0 and OUT1). Each has its own input of one frequency from the first stage divider, and outputs two different frequencies on Connection Matrix input lines [23] and [24]. See Figure 44 for details of the frequencies for each of these two Connection Matrix inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH, the oscillator will be turned off. The PWR DOWN signal has the highest priority.

11.2 OSC Block Diagram

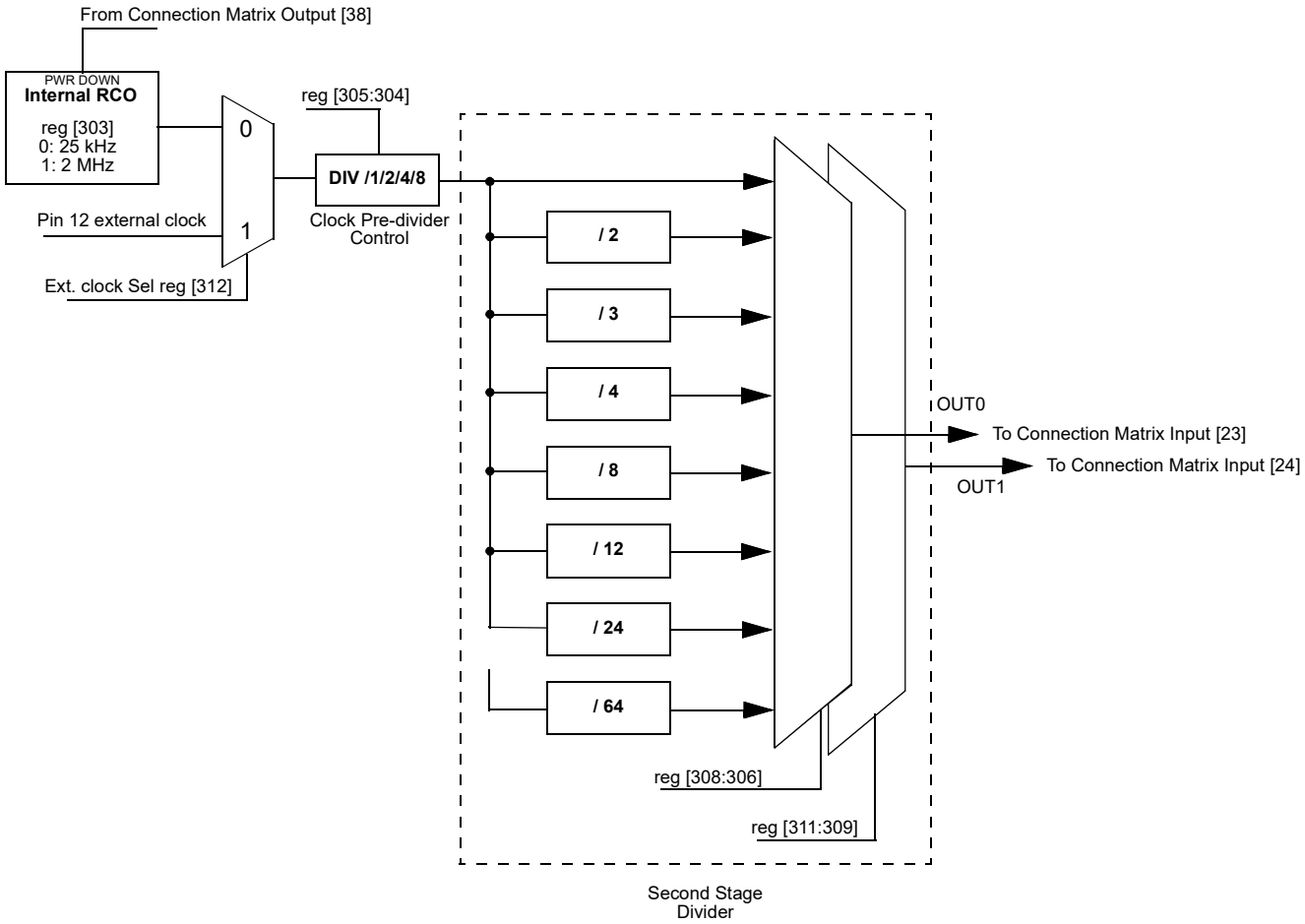


Figure 44. RC OSC Block Diagram

12. Power-on Reset

The SLG46110 has a power-on reset (POR) macrocell to ensure correct initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

12.1 General Operation

The SLG46110 is guaranteed to be powered down and nonoperational when the V_{DD} voltage (voltage on Pin 1) is less than 0.6 V, but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (see **Note 1**) than the V_{DD} voltage is applied to any other pin. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other pin is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46110, the voltage applied on the V_{DD} should be higher than the power-on threshold (see **Note 2**). The full operational V_{DD} range for the SLG46110 is 1.71 V to 5.5 V (1.8 V ±5 % to 5 V ±10 %). This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the power-on threshold. After the POR sequence has started, the SLG46110 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note 2: The power-on threshold can vary by PVT, but typically it is 1.6 V.

To power down the chip, the V_{DD} voltage should be lower than the operational, and to guarantee that chip is powered down, it should be less than 0.6 V.

All pins are in high-impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high-impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on pins cannot be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

12.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 45.

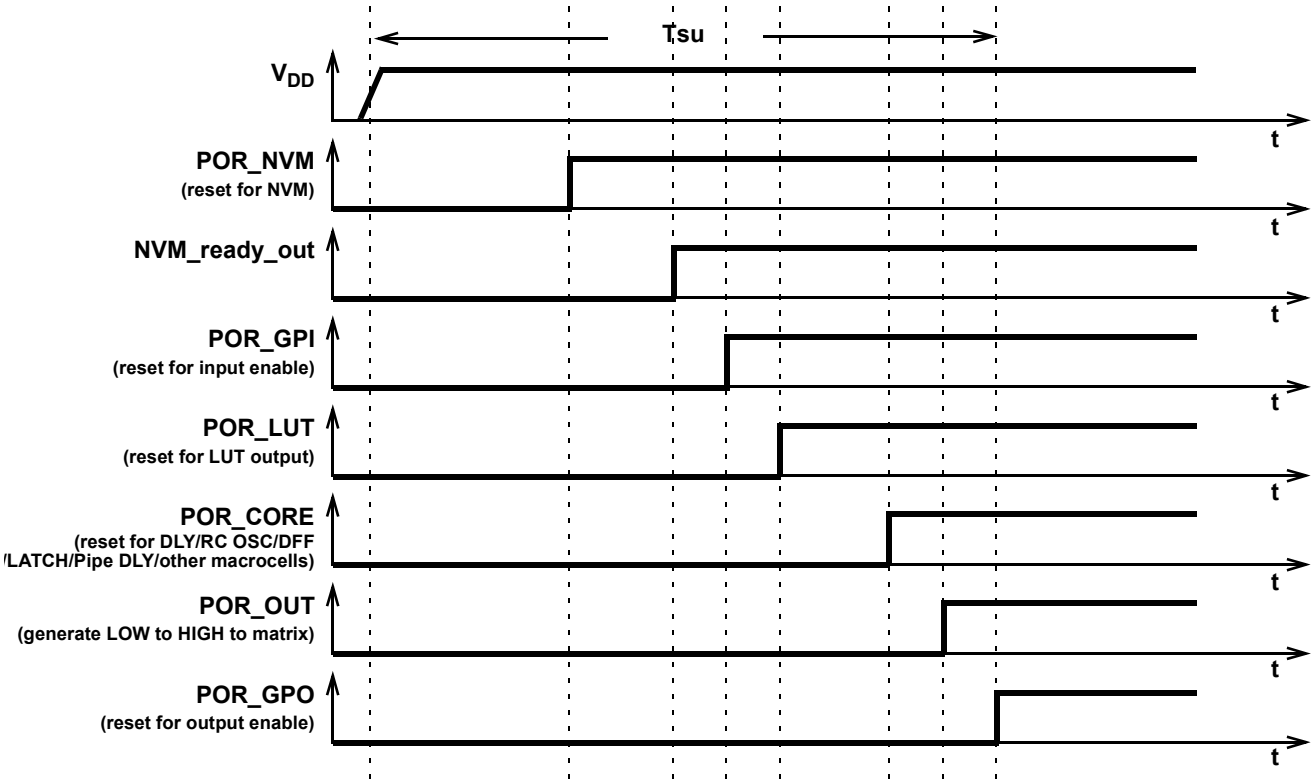


Figure 45. POR Sequence

As can be seen from Figure 45, after the V_{DD} has start ramping up and crosses the power-on threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then enables them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, RC OSC, DFFs, LATCHEs, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high-impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as slew rate, V_{DD} value, temperature, and even varies from chip to chip (process influence).

12.3 Macrocells Output States during POR Sequence

To have a full picture of the SLG46110 operation during powering and POR sequence, review the overview of the macrocell output states during the POR sequence (Figure 46 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high-impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output pins). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

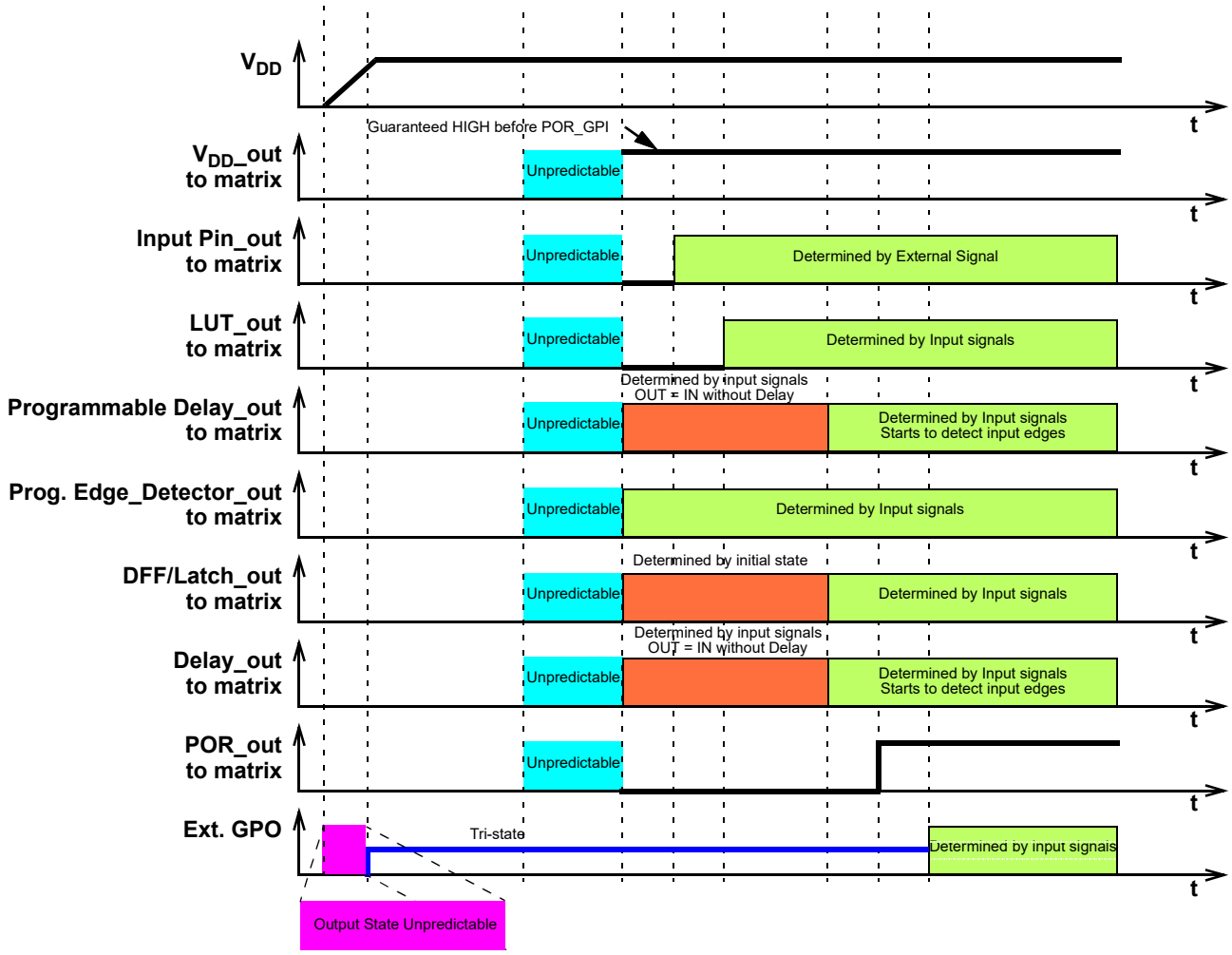


Figure 46. Internal Macrocell States during POR Sequence

13. Register Definitions

13.1 Register Map

Register Bit Address	Signal Function	Register Bit Definition
4:0	Matrix Out: Pin 3 Digital Output Source	
9:5	Matrix Out: Pin 4 Digital Output Source	
14:10	Matrix Out: Pin 6 Digital Output Source	
19:15	Matrix Out: Output Enable of Pin 6	
24:20	Matrix Out: In0 of 2-bit LUT0 or Clock Input of DFF0	
29:25	Matrix Out: In1 of 2-bit LUT0 or Data Input of DFF0	
34:30	Matrix Out: In0 of 2-bit LUT1 or Clock Input of DFF1	
39:35	Matrix Out: In1 of 2-bit LUT1 or Data Input of DFF1	
44:40	Matrix Out: In0 of 2-bit LUT2	
49:45	Matrix Out: In1 of 2-bit LUT2	
54:50	Matrix Out: In0 of 2-bit LUT3	
59:55	Matrix Out: In1 of 2-bit LUT3	
64:60	Matrix Out: In0 of 3-bit LUT0 or Clock Input of DFF2	
69:65	Matrix Out: In1 of 3-bit LUT0 or Data Input of DFF2	
74:70	Matrix Out: In2 of 3-bit LUT0 or nRST Input of DFF2	
79:75	Matrix Out: In0 of 3-bit LUT1 or Clock Input of DFF3	
84:80	Matrix Out: In1 of 3-bit LUT1 or Data Input of DFF3	
89:85	Matrix Out: In2 of 3-bit LUT1 or nRST(nSET) of DFF3	
94:90	Matrix Out: In0 of 3-bit LUT2	
99:95	Matrix Out: In1 of 3-bit LUT2	
104:100	Matrix Out: In2 of 3-bit LUT2	
109:105	Matrix Out: In0 of 3-bit LUT3	
114:110	Matrix Out: In1 of 3-bit LUT3	
119:115	Matrix Out: In2 of 3-bit LUT3	
124:120	Matrix Out: In0 of 3-bit LUT4 or Input of Pipe Delay	
129:125	Matrix Out: In1 of 3-bit LUT4 or nRST of Pipe Delay	
134:130	Matrix Out: In2 of 3-bit LUT4 or Clock of Pipe Delay	
139:135	Matrix Out: In0 of 4-bit LUT0 or Input for delay2 (Counter2) external clock	
144:140	Matrix Out: In1 of 4-bit LUT0 or Input for delay2 data (Counter2 reset)	
149:145	Matrix Out: In2 of 4-bit LUT0	
154:150	Matrix Out: In3 of 4-bit LUT0	
159:155	Matrix Out: Input for delay0 data (counter0 reset)	
164:160	Matrix Out: Input for delay1 data (counter1 reset)	
169:165	Matrix Out: Input for delay0/1 (Counter0 and Counter1) external clock	
174:170	Matrix Out: Input for delay3 (Counter3) external clock	
179:175	Matrix Out: pdb (power-down) for ACMP0	

Register Bit Address	Signal Function	Register Bit Definition
184:180	Matrix Out: pdb (power-down) for ACMP1	
189:185	Matrix Out: Input for Programmable Delay (Deglitch Filter input)	
194:190	Matrix Out: Power-down for OSC	
199:195	Matrix Out: Pin 8 Digital Output Source	
204:200	Matrix Out: Pin 9 Digital Output Source	
209:205	Matrix Out: Pin10 Digital Output Source	
214:210	Matrix Out: Output Enable of Pin 10	
219:215	Matrix Out: Pin 12 Digital Output Source	
223:220	Reserved	Reserved
DFF0/LATCH or 2-bit LUT0 Data		
224	DFF0 or LATCH select	0: DFF function 1: LATCH function
225	DFF0 output select	0: Q output 1: nQ output
226	DFF0 initial polarity select	0: LOW 1: HIGH
227	Unused if DFF/LATCH selected	Unused
DFF1/LATCH or 2-bit LUT1 Data		
228	DFF1 or LATCH select	0: DFF function 1:LATCH function
229	DFF1 output select	0: Q output 1: nQ output
230	DFF1 initial polarity select	0: LOW 1:HIGH
231	Unused if DFF/LATCH selected	Unused
2-bit LUT2 Data		
235:232	2-bit LUT2 data	2-bit LUT2 data
2-bit LUT3 Data		
239:236	2-bit LUT3 data	2-bit LUT3 data
2-bit LUT0/DFF0		
240	2-bit LUT0 or DFF0 select	0: 2-bit LUT0 1: DFF0
2-bit LUT1/DFF1		
241	2-bit LUT1 or DFF1 select	0: 2-bit LUT1 1: DFF1
DFF2/LATCH or 3-bit LUT0 Data		
242	DFF2 or LATCH select nSET	0: DFF function 1: LATCH function
243	DFF2 output select	0: Q output 1: nQ output
244	DFF2 nRST/nSET select	0: nRST from matrix output 1: nSET from matrix output
245	DFF2 initial polarity select	0: LOW 1: HIGH

Register Bit Address	Signal Function	Register Bit Definition
249:246	Unused if DFF/LATCH selected	Unused
DFF3/LATCH or 3-bit LUT1 Data		
250	DFF3 or LATCH select	0: DFF function 1: LATCH function
251	DFF3 output select	0: Q output 1: nQ output
252	DFF3 nRST/nSET select	0: nRST from matrix output 1: nSET from matrix output
253	DFF3 initial polarity select	0: LOW 1: HIGH
257:254	Unused if DFF/LATCH selected	Unused
3-bit LUT2 data		
265:258	3-bit LUT2 data	3-bit LUT2 data
3-bit LUT3 data		
273:266	3-bit LUT3 data	3-bit LUT3 data
Pipe number select or 3-bit LUT4 Data		
276:274	OUT0 select	Data (pipe number)
279:277	OUT1 select	Data (pipe number)
281:280	Unused if Pipe Delay selected	Unused
3-bit LUT0/DFF Select		
282	3-bit LUT0 or DFF2 select	0: 3-bit LUT0 1: DFF2
283	3-bit LUT1 or DFF3 select	0: 3-bit LUT1 1: DFF3
284	3-bit LUT4 or Pipe Delay output select	0: 3-bit LUT4 1: Pipe Delay
4-bit LUT0 or Counter/delay2 Mode Selection		
285	Counter/delay2 mode selection	0: Delay mode 1: Counter mode
288:286	Counter/delay2 Clock Source select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter1 overflow
296:289	Counter/delay2 Control Data	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
298:297	Delay2 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: On rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high-level reset for counter mode
300:299	Unused is Counter/Delay2 selected	Unused

Register Bit Address	Signal Function	Register Bit Definition
301	4-bit LUT0 or Counter2 select 0: 4-bit LUT0, 1: Counter2	0: 4-bit LUT0 1: Counter2
302	Force RC oscillator on	0: Auto Power-on 1: Force Power-on
303	RC Oscillator frequency control	0: 25 kHz 1: 2 MHz
305:304	OSC clock pre-divider	00: div1 01: div2 10: div4 11: div8
308:306	Internal Oscillator frequency divider control 0 for matrix input	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
311:309	Internal Oscillator frequency divider control 1 for matrix input	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
312	External Clock Source Select	0: Internal Oscillator 1: External Clock from Pin 12
313	Reserved	Reserved
Counter/Delay 0		
314	Counter/delay0 mode selection	0: Delay mode 1: Counter mode
317:315	Counter/delay0 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter3 Overflow
325:318	Counter0 Control Data/Delay0 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
327:326	Delay0 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high-level reset for counter mode
Counter/Delay 1		
328	Counter/delay1 mode selection	0: Delay Mode 1: Counter Mode

Register Bit Address	Signal Function	Register Bit Definition
331:329	Counter/delay1 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter0 Overflow
339:332	Counter1 Control Data/Delay1 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
341:340	Delay1 Mode Select or asynchronous counter reset	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high-level reset for counter mode
Counter/Delay 3		
342	Counter/delay3 mode selection	0: Delay Mode 1: Counter Mode
345:343	Counter/delay3 Clock Source select (external clock is only for counter mode)	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter2 Overflow
353:346	Counter3 Control Data/Delay4 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
355:354	Delay3 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
ACMP0		
360:356	ACMP0 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: EXT_VREF (Pin 4)

Register Bit Address	Signal Function	Register Bit Definition
362:361	ACMP0 hysteresis enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
364:363	ACMP0 positive input divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x
365	ACMP0 low bandwidth (max 1 MHz) enable	0: off 1: on
366	ACMP0 positive input source select Pin 3 and V_{DD}	0: Pin 3 1: V_{DD}
ACMP1		
371:367	ACMP1 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: EXT_VREF (Pin 4)
373:372	ACMP1 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
375:374	ACMP1 positive Input divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x
376	ACMP1 100 µA current source option	0: disable 1: enable
377	ACMP1 low bandwidth (max 1 MHz) enable.	0: off 1: on
378	ACMP1 positive input source select Pin 6 and Pin 3	0: Pin 6 1: Pin 3
Pin 2		
380:379	Pin 2 mode control	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 10: Low-voltage digital input 11: Reserved
382:381	Pin 2 pull-down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1 M

Register Bit Address	Signal Function	Register Bit Definition
Pin 3		
385:383	Pin 3 mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input/Output 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input/Output and Open-drain
387:386	Pin 3 pull-up/down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1 M
388	Pin 3 pull-up/down resistor select	0: pull-down resistor enable 1: pull-up resistor enable
389	Pin 3 driver strength selection	0: 1x 1: 2x
Pin 4		
392:390	Pin 4 mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input/Output 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input/Output and Open-drain
394:393	Pin 4 pull-up/down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1 M
395	Pin 4 pull-up/down resistor select	0: pull-down resistor enable 1: pull-up resistor enable
396	Pin 4 driver strength selection	0: 1x 1: 2x
Pin 6		
398:397	Pin 6 mode control (sig_Pin6_oe =0)	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 11: Low-voltage Digital Input 10: Analog Input/Output
400:399	Pin 6 mode control (sig_Pin6_oe =1)	00: Push-pull 1x 01: Push-pull 1x 10: Open-drain NMOS 1x 11: Open-drain NMOS 1x
402:401	Pin 6 pull-up/down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1 M
403	Pin 6 pull-up/down resistor select	0: pull-down resistor enable 1: pull-up resistor enable

Register Bit Address	Signal Function	Register Bit Definition
Pin 8		
406:404	Pin 8 mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input/Output 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input/Output and Open-drain
408:407	Pin 8 pull-up/down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1M
409	Pin 8 pull-up/down resistor select	0: pull-down resistor enable 1: pull-up resistor enable
410	Pin 8 driver strength selection	0: 1x 1: 2x
Pin 9		
413:411	Pin 9 mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input/Output 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input/Output and Open-drain
415:414	Pin 9 pull-down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1 M
416	Pin 9 pull-up/down resistor select	0: pull-down resistor enable 1: pull-up resistor enable
417	Pin 9 driver strength selection	0: 1x 1: 2x
Pin 10		
419:418	Pin 10 mode control (sig_Pin10_oe =0)	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 10: Low-voltage Digital Input 11: Analog Input/Output
421:420	Pin 10 mode control (sig_Pin10_oe =1)	00: Push-pull 1x 01: Push-pull 1x 10: Open-drain NMOS 1x 11: Open-drain NMOS 1x
423:422	Pin 10 pull-up/down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1 M
424	Pin 10 pull-up/down resistor select	0: pull-down resistor enable 1: pull-up resistor enable

Register Bit Address	Signal Function	Register Bit Definition
Pin 12		
427:425	Pin12 mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low-voltage digital input 011: Analog Input/Output 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Analog Input/Output and Open-drain
429:428	Pin12 pull-up/down resistor value selection	00: floating 01: 10 k 10: 100 k 11: 1 M
430	Pin 12 pull-up/down resistor select	0: pull-down resistor enable 1: pull-up resistor enable
431	Pin 12 driver strength selection	0: 1x 1: 2x
432	Pipe Delay OUT1 polarity select bit	0: non-inverting 1: inverting
440:433	8-bit pattern id	8-bit pattern id
441	Filter0 output polarity select	0: non-inverting 1: inverting
443:442	Reserved	Reserved
444	GPIO quick charge enable	0: Disable 1: Enable
445	Force Bandgap on	0: Auto-mode 1: Enable
446	V_{REF1} Output Active Buffer Control	0: Disabled 1: Enabled
449:447	V_{REF1} Output Source Select	000: ACMP0 reference voltage 001: ACMP1 reference voltage 100: $V_{DD}/2$ 101: $V_{DD}/3$ 110: $V_{DD}/4$ 101: Reserved 110: Reserved 111: Reserved
450	NVM data read disable	0: Disable (read enable) 1: Enable (read disable)
451	NVM power-down (or NVM data programming disable)	0: None (or programming enable) 1: Power-down (or programming disable)
452	Power Divider Power	0: Power-down 1: Power-on
453	POR Auto Power detect	0: Enable 1: Disable
454	Charge pump for analog macrocell enable (when V_{DD} <= 2.7 V turn on)	0: Disable (automatic on/off control) 1: Enable (always on)
455	V_{DD} bypass enable	0: Regulator auto on 1: Regulator off (V_{DD} bypass)
471:456	Reserved	Reserved

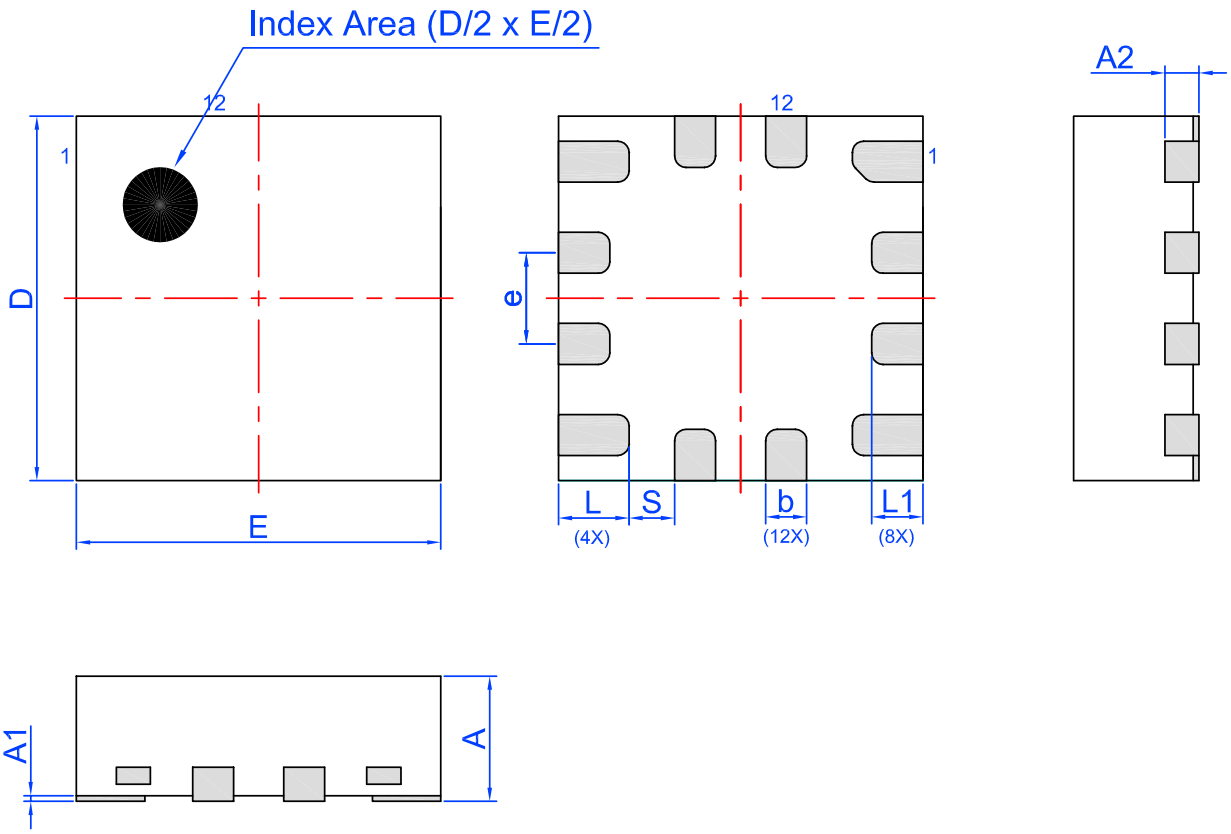
Register Bit Address	Signal Function	Register Bit Definition
479:472	Reserved	Reserved
481:480	Reserved	Reserved
482	Pin 2 edge detect mode	0: rising edge 1: falling edge
483	Bypass the Pin 2	0: Pin 2 edge active 1: Pin 2 high active
484	Pin 2 reset enable	0: Disable 1: Enable
485	Programmable Delay or Filter output select	0: Programmable Delay output 1: Filter output
487:486	Select the edge mode of programmable delay and edge detector	00: rising edge detector 01: falling edge detector 10: both edge detector 11: both edge delay
489:488	Delay value select for programmable delay and edge detector (V_{DD} = 3.3 V, typical condition)	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
490	Reserved	Reserved
495:491	Reserved	Reserved
501:496	Reserved	Reserved
502	Reserved	Reserved
503	Reserved	Reserved
511:504	Reserved	Reserved

14. Package Information

14.1 Package Outlines Drawings

14.1.1 STQFN-12 (1.6 mm x 1.6 mm x 0.55 mm, 0.4P) FC Green Package

IC net weight: 0.0028 g



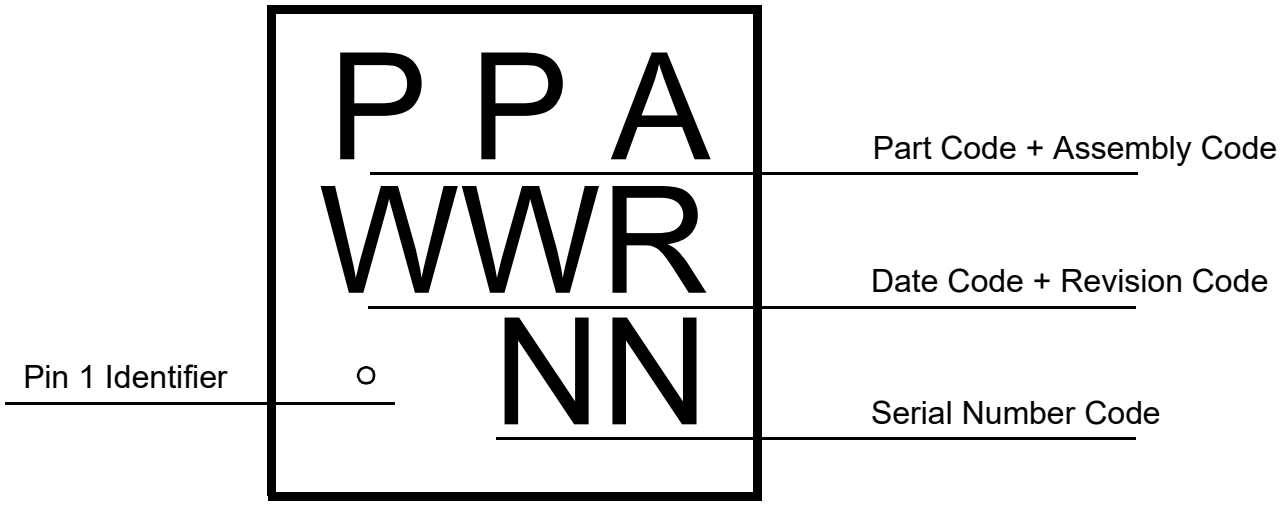
Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

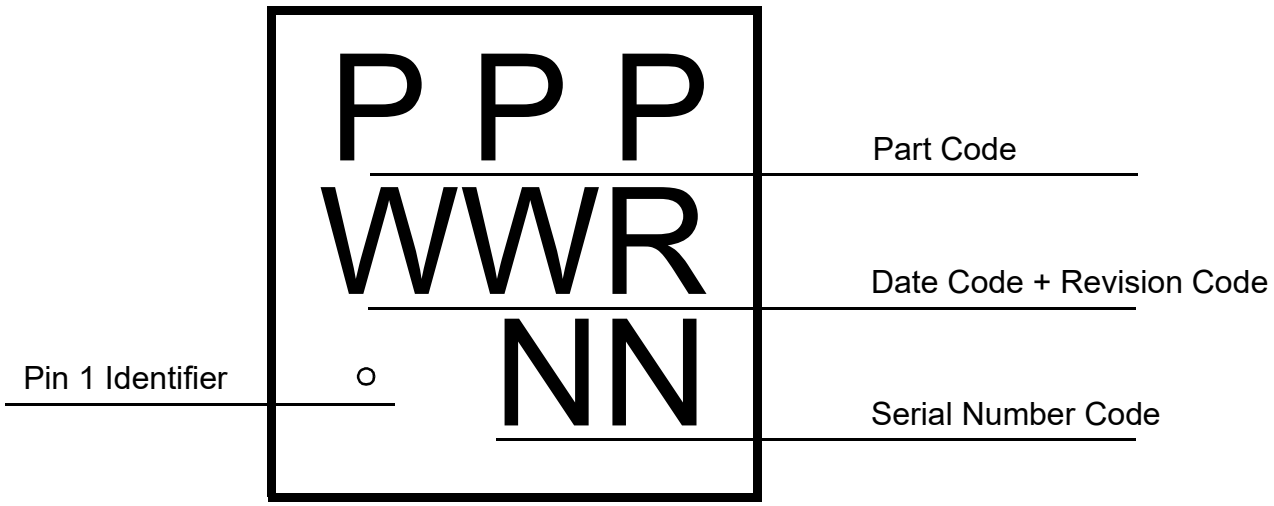
14.2 Package Top Marking

14.2.1 STQFN-12 (1.6 mm x 1.6 mm x 0.55 mm, 0.4P) FC Green Package

14.2.1.1 Before February 1, 2021



14.2.1.2 After February 1, 2021



14.3 STQFN Handling

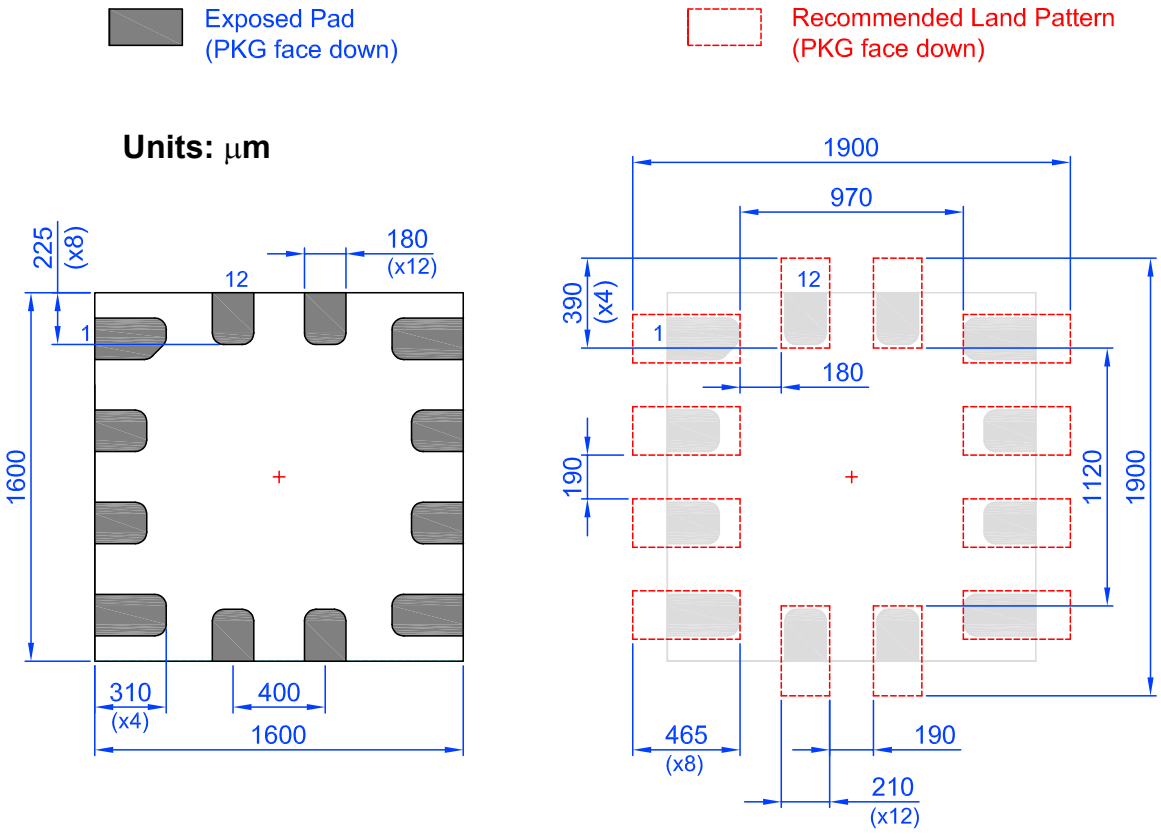
Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

14.4 Soldering Information

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

15. Layout Guidelines

15.1 STQFN-12 (1.6 mm x 1.6 mm x 0.55 mm, 0.4P) FC Green Package



16. Ordering Information

Part Number	Type
SLG46110	12-pin STQFN

Note: Use SLG46110V to order. Shipments are automatically in Tape and Reel.

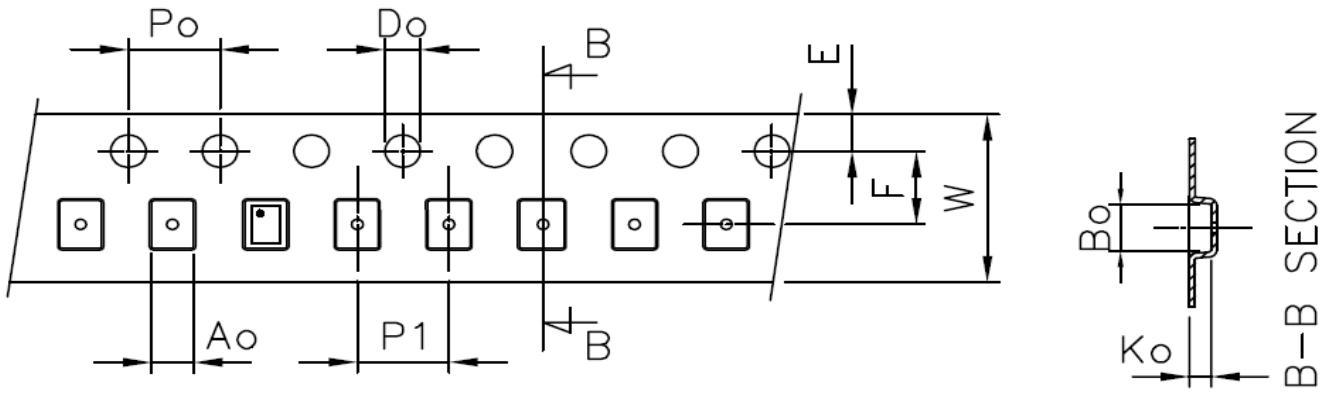
16.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel and Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FC 0.4P Green	12	1.6 x 1.6 x 0.55	3000	3000	178/60	100	400	100	400	8	4

16.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FC 0.4P Green	1.9	1.9	0.8	4	4	1.5	1.75	3.5	8

STQFN-12



Glossary

A

ACMP	Analog Comparator
AIO	Analog Input/Output

B

BG	Bandgap

C

CLK	Clock
CM	Connection matrix
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic Discharge

F

FC	Flip Chip
FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

H

H-Z	High Impedance

I

IC	Integrated Circuit
IN	Input
IO	Input/Output

L

LSB	Least Significant Bit
LBW	Low Bandwidth
LUT	Look-up Table

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NMOS	N-Channel MOSFET
nRST	Reset
nSET	Set
NVM	Non-volatile Memory

O

OD	Open-drain
OE	Output Enable
OSC	Oscillator
OTP	One-time Programmable
OUT	Output

P

PMOS	P-Channel MOSFET
POR	Power-on Reset
PP	Push-pull
PWR	Power
P DLY	Programmable Delay
PVT	Process, Voltage, Temperature

V

V_{REF}	Voltage Reference

Revision History

Revision	Date	Description
1.16	Oct 30, 2026	Removed table Gain Divider Accuracy Updated LUT block names to match with Go Configure™ Software Hub Updated ACMP1 Block Diagram Converted document to Renesas template
1.15	Feb 20, 2026	Updated IO pins description Updated Functional and Programming Pin Description Updated ACMP1 Block Diagram Corrected figure Internal Macrocell States during POR Sequence
1.14	May 22, 2025	Added subsection 3-State Outputs to I/O Pins section
1.13	Aug 14, 2023	Updated tables Electrical Characteristics Fixed typos
1.12	Mar 9, 2023	Added notes to section Ordering Information
1.11	Mar 4, 2022	Added R_{PUP} and R_{PDWN} in section Electrical Specifications Renesas rebranding
1.10	Sept 3, 2021	Updated tables CNT/DLY Register Settings Corrected registers [296:289], [325:318], [339:332], [353:346] in Appendix A - SLG46110 Register Definition
1.09	Feb 2, 2021	Updated section Package Top Marking System Definition Added note for CNTs Updated registers for LUT2_0 data, LUT2_1 data, and LUT2_3 data Corrected registers [353:343], [339:329], [325:315], [296:285]
1.08	Oct 29, 2019	Updated disclaimer
1.07	Nov 14, 2018	Updated to Dialog style
1.06	Oct 10, 2017	Updated Electrical Spec Fixed typos Updated POR sequence
1.05	Jul 7, 2017	Fixed typos Removed references to GPAK families Updated Silego Website & Support Updated Section Programmable Delay/Edge Detector Updated Electrical Spec
1.04	May 27, 2016	Updated Programmable Delay information Added PON_{THR} and $POFF_{THR}$ in Electrical Spec
1.03	Apr 4, 2016	Corrected section 6.0
1.02	Oct 28, 2015	Updated Absolute maximum conditions
1.01	Sept 29, 2015	Fixed typos
1.0	May 26, 2016	Production Release
0.66	May 21, 2015	Updated ACMP Diagrams and added Timing Characteristics Diagrams
0.65	Apr 23, 2015	Updated ACMP section
0.64	Apr 9, 2015	Updated Tsu condition and value
0.63	Mar 27, 2015	Updated ACMP section Updated RC Oscillator section
0.62	Mar 16, 2015	Updated Register table (typos)
0.61	Mar 10, 2015	Added Connection Matrix Example
0.60	Mar 9, 2015	Added POR section
0.59	Jan 14, 2015	Added IDD Estimator, Timing Estimator, Expected Delays sections
0.58	Dec 3, 2014	Updated Electrical Characteristics VIH/VIL/VOH/VOL values (formatting/rounding)

Revision	Date	Description
0.57	Sept 3, 2014	Updated Electrical Characteristics VIH/VIL/VOH/VOL values
0.56	Aug 25, 2014	Added Recommended Land Pattern
0.55	Jul 23, 2014	Fixed ESD information
0.54	Jun 20, 2014	Fixed typo on Electrical Spec
0.53	May 21, 2014	Updated block diagram Fixed typos Moved Programmable Delay and Deglitch Filter to Combination Macrocells section
0.52	Apr 29, 2014	Added ESD Ratings and MSL to Absolute Maximum Conditions
0.5	Mar 28, 2014	Fixed typos Preliminary Release
0.42	Mar 18, 2014	Updated block diagrams and timing diagrams for clarity
0.41	Feb 12, 2014	Fixed typos
0.40	Dec 2, 2013	Updated VIH/VIL in Electrical Characteristics Fixed typos Added IC net weight to Package Specification
0.31	Nov 25, 2013	Added Block Diagram
0.30	Nov 11, 2013	Added Diagrams
0.20	Sept 30, 2013	Updated Electrical Characteristics Added Register Table and Descriptions
0.10	Sept 16, 2013	Initial release

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