Section 1 Overview

1.1 Features

This LSI chip is equipped with a highly power efficient AI accelerator (DRP-AI) and an OpenCV accelerator for pre/post AI processing. It realizes low power consumption of AI inference and allows for a variety of embedded AI products that require image streaming via USB, PCI Express®, or Gigabit Ethernet interfaces.

The AI inference accelerator IP, DRP-AI, which consists of a dynamic reconfigurable processor (DRP) and AI-MAC, provides both high-speed AI inference and low power consumption at the same time. It delivers 1TOPS/W class power performance. The OpenCV accelerator powered by DRP delivers high-performance image processing functions. Application software can be accelerated without any API modification since the accelerator has the same API interface as Linux based open source.

The LSI integrates Cortex-A53 dual CPU cores available to customers and is suitable for a variety of AI integrated applications such as AI gateway, machine vision, security gate, and mobile robot.

■ CPU and DDR Memory Interfaces

- Cortex®-A53 Dual (996 MHz maximum)
- 32-bit LPDDR4-3200

■ Sensing and Analyzing

- AI accelerator: DRP-AI (1.0 TOPS/W class)
- OpenCV accelerator (DRP)

■ Video and Graphics

- H.265/H.264 Multi Codec

  Encoding: H.265 up to 2160p, H.264 up to 1080p

  Decoding: H.265 up to 2160p, H.264 up to 1080p

■ High Speed Interfaces

- 1× Gigabit Ethernet
- 1× USB3.1 Gen1 Host/Peripheral
- 1× PCIe® Gen 2 (2 lanes)
- 2× SDIO 3.0
- 1× eMMC™ 4.5.1

■ Package

- FCBGA (15×15 mm, 0.5-mm pitch)

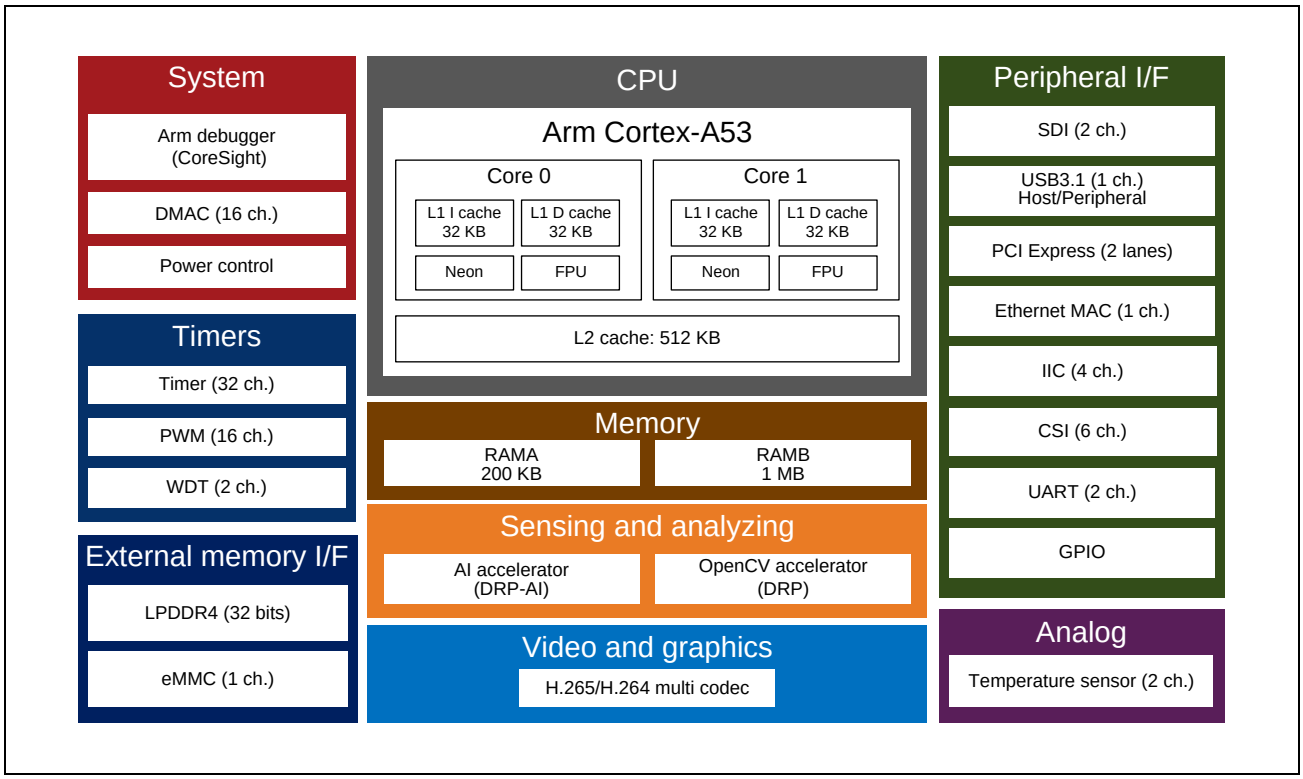


Figure 1.1-1 Diagram of Functional Overview

1.2 Product Lineup

The group currently consists of the following products.

Table 1.2-1 Product Lineup

Product Part Number	Part Number for Ordering	Package	Packing
R9A09G055MA3GBG	R9A09G055MA3GBG#ACC	PRBG0841KA-A	Individual tray
	R9A09G055MA3GBG#BCC	PRBG0841KA-A	Full carton

1.3 Functions

Table 1.3-1 Overview of Functions (1/2)

Item	Function
CPU	• Arm® Cortex-A53 dual core (CA53): 996 MHz – L1 cache: 32 KB (for instructions) + 32 KB (for data) for each core – L2 cache: 512 KB – FPU, Neon™ extension – ECC supported • Debugger interface (JTAG/SWD) – CoreSight™ debugging components incorporated – ETF (64-Kbyte trace RAM), ETR, and STM incorporated – External trace output (16-bit width)
Memory	• RAM A (RAMA): 200 KB (with ECC) • RAM B (RAMB): 1 MB • ROM: 128 KB
Timers	• Watchdog timer (WDT): 2 channels (CA53 core 0, CA53 core 1) • Compare-match timer: 32 channels • Pulse-width modulation timer (PWM): 16 channels
DMA controller	DMA controller (16 channels)
Sensing and analyzing	• AI accelerator (DRP-AI) • OpenCV accelerator
Video & graphics	• H.265/H.264 multi codec – Supported functions H.265 encoding and H.265 decoding, or H.264 encoding and H.264 decoding – Support encoding/decoding standard H.265/HEVC main profile at level 5 H.264/AVC constrained baseline/main/high profile at level 4.2 – I-/P-slice supported for H.264/H.265 encoding and decoding – H.265 encoding and decoding performance 3840 × 2160 p encoding, 3840 × 2160 p decoding – H.264 encoding and decoding performance 1920 × 1080 p encoding, 1920 × 1080 p decoding
External memory interfaces	• LPDDR4 interface – 3200 Mbps – 32-bit data width – Up to 4 GB supported • eMMC interface conforming to eMMC version 4.51 – Supports HS200 (high-speed DDR and HS400 are not supported) – 1/4/8-bit data bus

Table 1.3-1 Overview of Functions (2/2)

Item	Function
Peripheral interfaces	• SD host interface (SDI): 2 channels (SD specification version 3.01 compliant) – SD memory / I/O card interface (1-bit/4-bit SD bus) – SD memory card access for SD, SDHC, and SDXC – Supports default, high-speed, UHS-I/SDR12, SDR25, SDR50, and SDR104 transfer modes (DDR50, not supported) – Supports card detection and write protection • USB interface: 1 channel – USB3.1 Gen1 standard compliant – Dual-role device function supported (static switching of the host controller function and the peripheral controller function) – Supports super-speed (5 Gbps), high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transfer (low-speed is only supported for the host controller) • PCI Express interface Gen2 (5GT/s): 2 lanes – PCI Express base specification revision 4.0 compliant – Supports root complex/endpoint • Ethernet MAC interface: 1 channel – Supports transfer at 1000 Mbps, and 100 Mbps in full-duplex mode – Supports IEEE802.3 PHY GMII, MII compliant interface • IIC bus interface: 4 channels • Clocked serial interface: 6 channels • UART: 2 channels • GPIO
Analog	• Temperature sensor: 2 channels
Power control	• External power supply sequence control • Internal power domain control
Power voltage	• 0.8-V power supply VDD08, UnVDD08 (n = 2, 3, 4, 7), RTVDD08, PWVDD08, LPVDD, PLDVDD08n (n = 1, 2, 3, 4, 6), OTVDD08, TSnDVDD08A (n = 0, 1), PCVDD08, USDVDD, USVP, USVPTX • 1.1-V power supply LPVDDQ • 1.5-V power supply RTVDD • 1.8-V power supply PLVDDn (n = 1, 2, 3, 4, 6), OTVDD18, TSnAVDD18 (n = 0, 1), LPVAA, PCVDD18, USVDDH, PWVDD, VDD18, PAPREDVDD, PBPREDVDD, PCPREDVDD, MMPREDVDD, SD0PREDVDD, SD1FVDD, GEPREDVDD, PREDVDD33, UnVDD18 (n = 10, 11, 2, 3, 4, 5, 6, 7) • 3.3-V power supply USVD330, USVPH, VDD33 • 3.3-V/1.8-V switchable power supply PAMODVDD, PBMODVDD, PCMODVDD, MMMODVDD, SD0MODVDD, SD1FMODVDD, GEMODVDD, UnMODVDD (n = 10, 11)
Operating temperature	Tj = 103ºC (max.) Tj: Junction temperature

Section 2 Pins

2.1 Pin Assignment

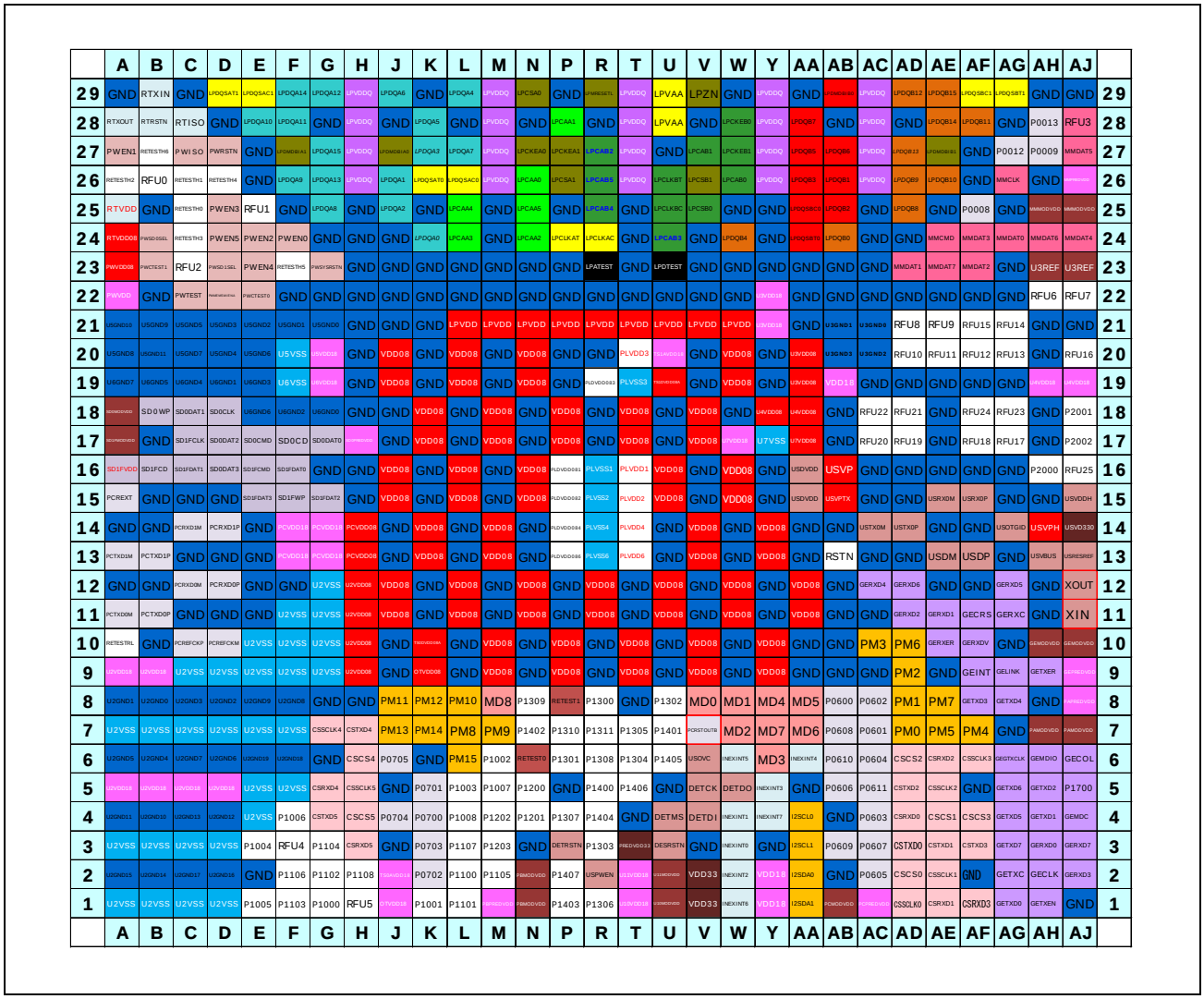


Figure 2.1-1 Pin Assignment (Top view)

Table 2.1-1 Ball Numbers and External Pin Names (1/5)

Ball Num.	External Pin Name
A1	U2VSS
A2	U2GND15
A3	U2VSS
A4	U2GND11
A5	U2VDD18
A6	U2GND5
A7	U2VSS
A8	U2GND1
A9	U2VDD18
A10	RETESTRL
A11	PCTXD0M
A12	GND
A13	PCTXD1M
A14	GND
A15	PCREXT
A16	SD1FVDD
A17	SD1FMODVDD
A18	SD0MODVDD
A19	U6GND7
A20	U5GND8
A21	U5GND10
A22	PWVDD
A23	PWVDD08
A24	RTVDD08
A25	RTVDD
A26	RETESTH2
A27	PWEN1
A28	RTXOUT
A29	GND
B1	U2VSS
B2	U2GND14
B3	U2VSS
B4	U2GND10
B5	U2VDD18
B6	U2GND4
B7	U2VSS
B8	U2GND0
B9	U2VDD18
B10	GND
B11	PCTXD0P
B12	GND
B13	PCTXD1P
B14	GND
B15	GND
B16	SD1FCD
B17	GND
B18	SD0WP
B19	U6GND5
B20	U5GND11
B21	U5GND9
B22	GND
B23	PWCTEST1
B24	PWSD0SEL
B25	GND
B26	RFU0
B27	RETESTH6
B28	RTRSTN
B29	RTXIN
C1	U2VSS
C2	U2GND17
C3	U2VSS
C4	U2GND13
C5	U2VDD18
C6	U2GND7
C7	U2VSS
C8	U2GND3
C9	U2VSS
C10	PCREFCKP
C11	GND
C12	PCRXD0M
C13	GND
C14	PCRXD1M
C15	GND
C16	SD1FDAT1
C17	SD1FCLK
C18	SD0DAT1
C19	U6GND4
C20	U5GND7
C21	U5GND5
C22	PWTEST
C23	RFU2
C24	RETESTH3
C25	RETESTH0
C26	RETESTH1
C27	PWISO
C28	RTISO
C29	GND
D1	U2VSS
D2	U2GND16
D3	U2VSS
D4	U2GND12
D5	U2VDD18
D6	U2GND6
D7	U2VSS
D8	U2GND2
D9	U2VSS
D10	PCREFCKM
D11	GND
D12	PCRXD0P
D13	GND
D14	PCRXD1P
D15	GND
D16	SD0DAT3
D17	SD0DAT2
D18	SD0CLK
D19	U6GND1
D20	U5GND4
D21	U5GND3
D22	PWMEMSWIENA
D23	PWSD1SEL
D24	PWEN5
D25	PWEN3
D26	RETESTH4
D27	PWRSTN
D28	GND
D29	LPDQSAT1
E1	P1005
E2	GND
E3	P1004
E4	U2VSS
E5	U2VSS
E6	U2GND19
E7	U2VSS
E8	U2GND9
E9	U2VSS
E10	U2VSS
E11	GND
E12	GND
E13	GND
E14	GND
E15	SD1FDAT3
E16	SD1FCMD
E17	SD0CMD
E18	U6GND6
E19	U6GND3
E20	U5GND6
E21	U5GND2
E22	PWCTEST0
E23	PWEN4
E24	PWEN2
E25	RFU1
E26	GND
E27	GND
E28	LPDQA10
E29	LPDQSAC1
F1	P1103
F2	P1106
F3	RFU4
F4	P1006
F5	U2VSS
F6	U2GND18
F7	U2VSS
F8	U2GND8
F9	U2VSS
F10	U2VSS
F11	U2VSS
F12	GND
F13	PCVDD18
F14	PCVDD18
F15	SD1FWP
F16	SD1FDAT0
F17	SD0CD
F18	U6GND2
F19	U6VSS
F20	U5VSS
F21	U5GND1
F22	GND
F23	RETESTH5
F24	PWEN0
F25	GND
F26	LPDQA9
F27	LPDMDBIA1
F28	LPDQA11
F29	LPDQA14
G1	P1000
G2	P1102
G3	P1104
G4	CSTXD5
G5	CSRXD4
G6	GND

Table 2.1-1 Ball Numbers and External Pin Names (2/5)

Ball Num.	External Pin Name
G7	CSSCLK4
G8	GND
G9	U2VSS
G10	U2VSS
G11	U2VSS
G12	U2VSS
G13	PCVDD18
G14	PCVDD18
G15	SD1FDAT2
G16	GND
G17	SD0DAT0
G18	U6GND0
G19	U6VDD18
G20	U5VDD18
G21	U5GND0
G22	GND
G23	PWSYSRSTN
G24	GND
G25	LPDQA8
G26	LPDQA13
G27	LPDQA15
G28	GND
G29	LPDQA12
H1	RFU5
H2	P1108
H3	CSRXD5
H4	CSCS5
H5	CSSCLK5
H6	CSCS4
H7	CSTXD4
H8	GND
H9	U2VDD08
H10	U2VDD08
H11	U2VDD08
H12	U2VDD08
H13	PCVDD08
H14	PCVDD08
H15	GND
H16	GND
H17	SD0PREDVDD
H18	GND
H19	GND
H20	GND
H21	GND
H22	GND

Ball Num.	External Pin Name
H23	GND
H24	GND
H25	GND
H26	LPVDDQ
H27	LPVDDQ
H28	LPVDDQ
H29	LPVDDQ
J1	OTVDD18
J2	TS0AVDD18
J3	GND
J4	P0704
J5	GND
J6	P0705
J7	PM13
J8	PM11
J9	GND
J10	GND
J11	VDD08
J12	VDD08
J13	GND
J14	GND
J15	VDD08
J16	VDD08
J17	GND
J18	GND
J19	VDD08
J20	VDD08
J21	GND
J22	GND
J23	GND
J24	GND
J25	LPDQA2
J26	LPDQA1
J27	LPDMDBIA0
J28	GND
J29	LPDQA6
K1	P1001
K2	P0702
K3	P0703
K4	P0700
K5	P0701
K6	GND
K7	PM14
K8	PM12
K9	OTVDD08

Ball Num.	External Pin Name
K10	TS0DVDD08A
K11	GND
K12	GND
K13	VDD08
K14	VDD08
K15	GND
K16	GND
K17	VDD08
K18	VDD08
K19	GND
K20	GND
K21	GND
K22	GND
K23	GND
K24	LPDQA0
K25	GND
K26	LPDQSAT0
K27	LPDQA3
K28	LPDQA5
K29	GND
L1	P1101
L2	P1100
L3	P1107
L4	P1008
L5	P1003
L6	PM15
L7	PM8
L8	PM10
L9	GND
L10	GND
L11	VDD08
L12	VDD08
L13	GND
L14	GND
L15	VDD08
L16	VDD08
L17	GND
L18	GND
L19	VDD08
L20	VDD08
L21	LPVDD
L22	GND
L23	GND
L24	LPCAA3
L25	LPCAA4

Ball Num.	External Pin Name
L26	LPDQSAC0
L27	LPDQA7
L28	GND
L29	LPDQA4
M1	PBPREDVDD
M2	P1105
M3	P1203
M4	P1202
M5	P1007
M6	P1002
M7	PM9
M8	MD8
M9	VDD08
M10	VDD08
M11	GND
M12	GND
M13	VDD08
M14	VDD08
M15	GND
M16	GND
M17	VDD08
M18	VDD08
M19	GND
M20	GND
M21	LPVDD
M22	GND
M23	GND
M24	GND
M25	GND
M26	LPVDDQ
M27	LPVDDQ
M28	LPVDDQ
M29	LPVDDQ
N1	PBMODVDD
N2	PBMODVDD
N3	GND
N4	P1201
N5	P1200
N6	RETEST0
N7	P1402
N8	P1309
N9	GND
N10	GND
N11	VDD08
N12	VDD08

Table 2.1-1 Ball Numbers and External Pin Names (3/5)

Ball Num.	External Pin Name
N13	GND
N14	GND
N15	VDD08
N16	VDD08
N17	GND
N18	GND
N19	VDD08
N20	VDD08
N21	LPVDD
N22	GND
N23	GND
N24	LPCAA2
N25	LPCAA5
N26	LPCAA0
N27	LPCKEA0
N28	GND
N29	LPCSA0
P1	P1403
P2	P1407
P3	DETRSTN
P4	P1307
P5	GND
P6	P1301
P7	P1310
P8	RETEST1
P9	VDD08
P10	VDD08
P11	GND
P12	GND
P13	PLDVDD086
P14	PLDVDD084
P15	PLDVDD082
P16	PLDVDD081
P17	VDD08
P18	VDD08
P19	GND
P20	GND
P21	LPVDD
P22	GND
P23	GND
P24	LPCLKAT
P25	GND
P26	LPCSA1
P27	LPCKEA1
P28	LPCAA1
P29	GND
R1	P1306
R2	USPWEN
R3	P1303
R4	P1404
R5	P1400
R6	P1308
R7	P1311
R8	P1300
R9	GND
R10	GND
R11	VDD08
R12	VDD08
R13	PLVSS6
R14	PLVSS4
R15	PLVSS2
R16	PLVSS1
R17	GND
R18	GND
R19	PLDVDD083
R20	GND
R21	LPVDD
R22	GND
R23	LPATEST
R24	LPCLKAC
R25	LPCAB4
R26	LPCAB5
R27	LPCAB2
R28	GND
R29	LPMRESETL
T1	U10VDD18
T2	U11VDD18
T3	PREDVDD33
T4	GND
T5	P1406
T6	P1304
T7	P1305
T8	GND
T9	VDD08
T10	VDD08
T11	GND
T12	GND
T13	PLVDD6
T14	PLVDD4
T15	PLVDD2
T16	PLVDD1
T17	VDD08
T18	VDD08
T19	PLVSS3
T20	PLVDD3
T21	LPVDD
T22	GND
T23	GND
T24	GND
T25	GND
T26	LPVDDQ
T27	LPVDDQ
T28	LPVDDQ
T29	LPVDDQ
U1	U10MODVDD
U2	U11MODVDD
U3	DESRSTN
U4	DETMS
U5	GND
U6	P1405
U7	P1401
U8	P1302
U9	GND
U10	GND
U11	VDD08
U12	VDD08
U13	GND
U14	GND
U15	VDD08
U16	VDD08
U17	GND
U18	GND
U19	TS1DVDD08A
U20	TS1AVDD18
U21	LPVDD
U22	GND
U23	LPDTEST
U24	LPCAB3
U25	LPCLKBC
U26	LPCLKBT
U27	GND
U28	LPVAA
U29	LPVAA
V1	VDD33
V2	VDD33
V3	GND
V4	DETDI
V5	DETCK
V6	USOVC
V7	PCRSTOUTB
V8	MD0
V9	VDD08
V10	VDD08
V11	GND
V12	GND
V13	VDD08
V14	VDD08
V15	GND
V16	GND
V17	VDD08
V18	VDD08
V19	GND
V20	GND
V21	LPVDD
V22	GND
V23	GND
V24	GND
V25	LPCSB0
V26	LPCSB1
V27	LPCAB1
V28	GND
V29	LPZN
W1	INEXINT6
W2	INEXINT2
W3	INEXINT0
W4	INEXINT1
W5	DETDO
W6	INEXINT5
W7	MD2
W8	MD1
W9	GND
W10	GND
W11	VDD08
W12	VDD08
W13	GND
W14	GND
W15	VDD08
W16	VDD08
W17	U7VDD18
W18	GND

Table 2.1-1 Ball Numbers and External Pin Names (4/5)

Ball Num.	External Pin Name
W19	VDD08
W20	VDD08
W21	LPVDD
W22	GND
W23	GND
W24	LPDQB4
W25	GND
W26	LPCAB0
W27	LPCKEB1
W28	LPCKEB0
W29	GND
Y1	VDD18
Y2	VDD18
Y3	GND
Y4	INEXINT7
Y5	INEXINT3
Y6	MD3
Y7	MD7
Y8	MD4
Y9	VDD08
Y10	VDD08
Y11	GND
Y12	GND
Y13	VDD08
Y14	VDD08
Y15	GND
Y16	GND
Y17	U7VSS
Y18	U4VDD08
Y19	GND
Y20	GND
Y21	U3VDD18
Y22	U3VDD18
Y23	GND
Y24	GND
Y25	GND
Y26	LPVDDQ
Y27	LPVDDQ
Y28	LPVDDQ
Y29	LPVDDQ
AA1	I2SDA1
AA2	I2SDA0
AA3	I2SCL1
AA4	I2SCL0
AA5	GND

Ball Num.	External Pin Name
AA6	INEXINT4
AA7	MD6
AA8	MD5
AA9	GND
AA10	GND
AA11	VDD08
AA12	VDD08
AA13	GND
AA14	GND
AA15	USDVDD
AA16	USDVDD
AA17	U7VDD08
AA18	U4VDD08
AA19	U3VDD08
AA20	U3VDD08
AA21	GND
AA22	GND
AA23	GND
AA24	LPDQSBT0
AA25	LPDQSBC0
AA26	LPDQB3
AA27	LPDQB5
AA28	LPDQB7
AA29	GND
AB1	PCMODVDD
AB2	GND
AB3	P0609
AB4	GND
AB5	P0606
AB6	P0610
AB7	P0608
AB8	P0600
AB9	GND
AB10	GND
AB11	GND
AB12	GND
AB13	RSTN
AB14	GND
AB15	USVPTX
AB16	USVP
AB17	GND
AB18	GND
AB19	VDD18
AB20	U3GND3
AB21	U3GND1

Ball Num.	External Pin Name
AB22	GND
AB23	GND
AB24	LPDQB0
AB25	LPDQB2
AB26	LPDQB1
AB27	LPDQB6
AB28	GND
AB29	LPDMDBIB0
AC1	PCPREDVDD
AC2	P0605
AC3	P0607
AC4	P0603
AC5	P0611
AC6	P0604
AC7	P0601
AC8	P0602
AC9	GND
AC10	PM3
AC11	GND
AC12	GERXD4
AC13	GND
AC14	USTX0M
AC15	GND
AC16	GND
AC17	RFU20
AC18	RFU22
AC19	GND
AC20	U3GND2
AC21	U3GND0
AC22	GND
AC23	GND
AC24	GND
AC25	GND
AC26	LPVDDQ
AC27	LPVDDQ
AC28	LPVDDQ
AC29	LPVDDQ
AD1	CSSCLK0
AD2	CSCS0
AD3	CSTXD0
AD4	CSRXD0
AD5	CSTXD2
AD6	CSCS2
AD7	PM0
AD8	PM1

Ball Num.	External Pin Name
AD9	PM2
AD10	PM6
AD11	GERXD2
AD12	GERXD6
AD13	GND
AD14	USTX0P
AD15	GND
AD16	GND
AD17	RFU19
AD18	RFU21
AD19	GND
AD20	RFU10
AD21	RFU8
AD22	GND
AD23	MMDAT1
AD24	GND
AD25	LPDQB8
AD26	LPDQB9
AD27	LPDQB13
AD28	GND
AD29	LPDQB12
AE1	CSRXD1
AE2	CSSCLK1
AE3	CSTXD1
AE4	CSCS1
AE5	CSSCLK2
AE6	CSRXD2
AE7	PM5
AE8	PM7
AE9	GND
AE10	GERXER
AE11	GERXD1
AE12	GND
AE13	USDM
AE14	GND
AE15	USRX0M
AE16	GND
AE17	GND
AE18	GND
AE19	GND
AE20	RFU11
AE21	RFU9
AE22	GND
AE23	MMDAT7
AE24	MMCMD

Table 2.1-1 Ball Numbers and External Pin Names (5/5)

Ball Num.	External Pin Name
AE25	GND
AE26	LPDQB10
AE27	LPDMDBIB1
AE28	LPDQB14
AE29	LPDQB15
AF1	CSRXD3
AF2	GND
AF3	CSTXD3
AF4	CSCS3
AF5	GND
AF6	CSSCLK3
AF7	PM4
AF8	GETXD3
AF9	GEINT
AF10	GERXDV
AF11	GECRS
AF12	GND
AF13	USDP
AF14	GND
AF15	USRX0P
AF16	GND
AF17	RFU18
AF18	RFU24
AF19	GND
AF20	RFU12
AF21	RFU15
AF22	GND
AF23	MMDAT2
AF24	MMDAT3
AF25	P0008
AF26	GND

Ball Num.	External Pin Name
AF27	GND
AF28	LPDQB11
AF29	LPDQSBC1
AG1	GETXD0
AG2	GETXC
AG3	GETXD7
AG4	GETXD5
AG5	GETXD6
AG6	GEGTXCLK
AG7	GND
AG8	GETXD4
AG9	GELINK
AG10	GND
AG11	GERXC
AG12	GERXD5
AG13	GND
AG14	USOTGID
AG15	GND
AG16	GND
AG17	RFU17
AG18	RFU23
AG19	GND
AG20	RFU13
AG21	RFU14
AG22	GND
AG23	GND
AG24	MMDAT0
AG25	GND
AG26	MMCLK
AG27	P0012
AG28	GND

Ball Num.	External Pin Name
AG29	LPDQSBT1
AH1	GETXEN
AH2	GECLK
AH3	GERXD0
AH4	GETXD1
AH5	GETXD2
AH6	GEMDIO
AH7	PAMODVDD
AH8	GND
AH9	GETXER
AH10	GEMODVDD
AH11	GND
AH12	GND
AH13	USVBUS
AH14	USVPH
AH15	GND
AH16	P2000
AH17	GND
AH18	GND
AH19	U4VDD18
AH20	GND
AH21	GND
AH22	RFU6
AH23	U3REF
AH24	MMDAT6
AH25	MMMODVDD
AH26	GND
AH27	P0009
AH28	P0013
AH29	GND
AJ1	GND

Ball Num.	External Pin Name
AJ2	GERXD3
AJ3	GERXD7
AJ4	GEMDC
AJ5	P1700
AJ6	GECOL
AJ7	PAMODVDD
AJ8	PAPREDVDD
AJ9	GEPREDVDD
AJ10	GEMODVDD
AJ11	XIN
AJ12	XOUT
AJ13	USRESREF
AJ14	USVD330
AJ15	USVDDH
AJ16	RFU25
AJ17	P2002
AJ18	P2001
AJ19	U4VDD18
AJ20	RFU16
AJ21	GND
AJ22	RFU7
AJ23	U3REF
AJ24	MMDAT4
AJ25	MMMODVDD
AJ26	MMPREDVDD
AJ27	MMDAT5
AJ28	RFU3
AJ29	GND
—	—
—	—
—	—

2.2 External Pins

2.2.1 List of External Pins

Table 2.2-1 List of External Pins (1/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
RTXIN	I	1.5	1.5-V OSC	CLOCK	Pull down	—	—	—	—	—
RTXOUT	O	1.5	1.5-V OSC	CLOCK	Open	—	—	—	—	—
RTRSTN	I	1.5	PWC I/O	Don't care	Pull down	●	—	—	—	—
RTISO	I	1.5	PWC I/O	Hi-Z	Pull up	●	—	—	—	—
RTVDD	—	1.5	PWC I/O, PWC clock power supply	—	—	—	—	—	—	—
RTVDD08	—	0.8	XTAL power supply	—	—	—	—	—	—	—
PWRSTN	I	1.8	PWC I/O	Don't care	Pull down	●	—	—	—	—
PWTEST	I	1.8	PWC I/O	Don't care	Pull down	●	—	—	—	—
PWEN0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN1	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN2	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN3	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN4	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN5	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSYSRSTN	O	1.8	PWC I/O	L	Open	—	—	●	Fixed*2	—
PWSD0SEL	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSD1SEL	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWCTEST0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWCTEST1	I	1.8	PWC I/O	Don't care	Pull up	●	—	—	—	—
PWMEMSWIENA	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWISO	O	1.8	PWC I/O	Hi-Z	Open	—	—	●	Fixed*2	—
PWVDD08	—	0.8	PWC core power supply	—	—	—	—	—	—	—
PWVDD	—	1.8	PWC I/O power supply	—	—	—	—	—	—	—
MMDAT0	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMDAT1	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMDAT2	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMDAT3	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMDAT4	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMDAT5	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMDAT6	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)

Table 2.2-1 List of External Pins (2/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
MMDAT7	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
P0008	IO	3.3/1.8	PORT00 I/O	PU	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
P0009	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMCMD	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMCLK	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
P0012	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
P0013	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
MMMODVDD	—	3.3/1.8	PORT00 I/O power supply	—	—	—	—	—	—	—
MMPREDVDD	—	1.8	PORT00 pre-driver power supply	—	—	—	—	—	—	—
PM0	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM1	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM2	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM4	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM5	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM6	IO	3.3/1.8	PORT01(A) I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM7	IO	3.3/1.8	PORT01(A) I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PAMODVDD	—	3.3/1.8	PORT01(A), PORT03 I/O power supply	—	—	—	—	—	—	—

Table 2.2-1 List of External Pins (3/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
PAPREDVDD	—	1.8	PORT01(A), PORT03 pre-driver power supply	—	—	—	—	—	—	—
PM8	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM9	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM10	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM11	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM12	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM13	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM14	IO	3.3/1.8	PORT01(B) I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM15	IO	3.3/1.8	PORT01(B) I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PBMODVDD	—	3.3/1.8	PORT01(B), PORT04, PORT07, PORT21 I/O power supply	—	—	—	—	—	—	—
PBPREDVDD	—	1.8	PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	—	—	—	—	—	—	—
INEXINT0*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT1*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT2*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT3*1,	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT4*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT5*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)

Table 2.2-1 List of External Pins (4/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
INEXINT6*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT7*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
CSTXD0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSSCLK0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSCS0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD1	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD1	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSSCLK1	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSCS1	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSSCLK2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSCS2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSSCLK3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)

Table 2.2-1 List of External Pins (5/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
CSCS3	IO	3.3/1.8	PORT03 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD4	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSRXD4	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSSCLK4	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSCS4	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSTXD5	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSRXD5	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSSCLK5	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSCS5	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
I2SDA0*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)
I2SCL0*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)
I2SDA1*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)
I2SCL1*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)
P0600	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0601	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0602	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0603	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)

Table 2.2-1 List of External Pins (6/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
P0604	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0605	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0606	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0607	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0608	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0609	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0610	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0611	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
PCMODVDD	—	3.3/1.8	PORT06 I/O power supply	—	—	—	—	—	—	—
PCPREDVDD	—	1.8	PORT06 pre-driver power supply	—	—	—	—	—	—	—
P0700	IO	3.3/1.8	PORT07 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
P0701	IO	3.3/1.8	PORT07 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
P0702	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
P0703	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
P0704	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
P0705	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
SD0CMD	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0CLK	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)

Table 2.2-1 List of External Pins (7/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
SD0DAT0	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0DAT1	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0DAT2	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0DAT3	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0WP	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0CD	IO	3.3/1.8	PORT08 I/O	PU	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0MODVDD	—	3.3/1.8	PORT08 I/O power supply	—	—	—	—	—	—	—
SD0PREDVDD	—	1.8	PORT08 pre-driver power supply	—	—	—	—	—	—	—
SD1FCMD	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FCLK	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FDAT0	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FDAT1	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FDAT2	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FDAT3	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FWP	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FCD	IO	3.3/1.8	PORT09 I/O	PU	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FMODVDD	—	3.3/1.8	PORT09 I/O power supply	—	—	—	—	—	—	—
SD1FVDD	—	1.8	PORT09 pre-driver power supply	—	—	—	—	—	—	—
P1000	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)

Table 2.2-1 List of External Pins (8/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
P1001	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
P1002	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
P1003	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
P1004	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
P1005	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
P1006	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
P1007	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
P1008	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
U10MODVDD	—	3.3/1.8	PORT10 I/O power supply	—	—	—	—	—	—	—
U10VDD18	—	1.8	PORT10 pre-driver power supply	—	—	—	—	—	—	—
P1100	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
P1101	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
P1102	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
P1103	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
P1104	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
P1105	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
P1106	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
P1107	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)

Table 2.2-1 List of External Pins (9/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
P1108	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
U11MODVDD	—	3.3/1.8	PORT11 I/O power supply	—	—	—	—	—	—	—
U11VDD18	—	1.8	PORT11 pre-driver power supply	—	—	—	—	—	—	—
P1200	IO	3.3	PORT12 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
P1201	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
P1202	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
P1203	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
P1300	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1301	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1302	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1303	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1304	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1305	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1306	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1307	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1308	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1309	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1310	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)

Table 2.2-1 List of External Pins (10/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
P1311	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
P1400	IO	3.3	PORT14 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
P1401	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
P1402	IO	3.3	PORT14 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
P1403	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
P1404	IO	3.3	PORT14 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
P1405	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
P1406	IO	3.3	PORT14 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
P1407	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
GETXC	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXEN	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXER	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD0	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD1	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD2	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD3	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD4	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)

Table 2.2-1 List of External Pins (11/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
GETXD5	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD6	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD7	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXC	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXDV	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXER	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXD0	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXD1	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXD2	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD3	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD4	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD5	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD6	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD7	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GECRS	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GECOL	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEMDC	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)

Table 2.2-1 List of External Pins (12/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
GEMDIO	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEGTXCLK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GELINK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEINT	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GECLK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
P1700	IO	3.3/1.8	PORT17 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-20**)
GEMODVDD	—	3.3/1.8	PORT15, PORT16, PORT17 I/O power supply	—	—	—	—	—	—	—
GEPREDVDD	—	1.8	PORT15, PORT16, PORT17 pre-driver power supply	—	—	—	—	—	—	—
DETCK	I	1.8	Debugger I/O	PD	Open	—	PD	—	—	—
DETDI	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
DETDO	O	1.8	Debugger I/O	Hi-Z	Open	—	—	—	Selectable*2	—
DETMS	IO	1.8	Debugger I/O	PU	Open	—	PU	—	Selectable*2	—
DETRSTN	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
DESRSTN	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
RETEST0	I	3.3	LSI test I/O	PD	Pull down	●	PD	—	—	—
RETEST1	I	3.3	LSI test I/O	PD	Pull down	●	PD	—	—	—
LPATEST	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA2	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA3	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA4	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA5	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB2	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB3	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB4	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB5	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCKEA0	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEA1	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEB0	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEB1	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCLKAC	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKAT	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKBC	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—

Table 2.2-1 List of External Pins (13/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
LPCLKBT	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSA0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSA1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSB0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSB1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIA0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIA1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIB0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIB1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA2	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA3	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA4	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA5	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA6	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA7	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA8	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA9	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA10	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA11	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA12	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA13	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA14	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA15	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB2	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB3	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB4	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB5	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB6	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB7	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB8	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB9	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB10	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB11	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB12	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB13	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB14	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB15	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAC0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAC1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAT0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAT1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBC0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBC1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBT0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBT1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPMRESETL	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—

Table 2.2-1 List of External Pins (14/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
LPZN	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPVAA	—	1.8	LPDDR4 PLL 1.8-V power supply	—	—	—	—	—	—	—
LPVDD	—	0.8	LPDDR4 core 0.8-V power supply	—	—	—	—	—	—	—
LPVDDQ	—	1.1	LPDDR4 PHY 1.1-V power supply	—	—	—	—	—	—	—
LPDTEST	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
U2VDD18	—	1.8	1.8-V power supply	—	—	—	—	—	—	—
U2VDD08	—	0.8	0.8-V power supply	—	—	—	—	—	—	—
U2VSS	—	0	GND	—	—	—	—	—	—	—
U3VDD18	—	1.8	1.8-V power supply	—	—	—	—	—	—	—
U3REF	—	1.2	1.2-V reference	—	—	—	—	—	—	—
U3VDD08	—	0.8	0.8-V power supply	—	—	—	—	—	—	—
PCRXD0P	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD0M	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCTXD0P	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCTXD0M	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCREFCKP	I	1.8	PCIe PHY	CLOCK	Open	—	—	—	—	—
PCREFCKM	I	1.8	PCIe PHY	CLOCK	Open	—	—	—	—	—
PCREXT	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD1P	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD1M	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCTXD1P	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCTXD1M	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCVDD08	—	0.8	PCIe PHY 0.8-V power supply	—	—	—	—	—	—	—
PCVDD18	—	1.8	PCIe PHY 1.8-V power supply	—	—	—	—	—	—	—
PCRSTOUTB	O	3.3	PCIe I/O	H	Open	—	—	—	Selectable*2	—
USDP	IO	3.3	USB PHY	L	Open	—	-	—	—	—
USDM	IO	3.3	USB PHY	L	Open	—	-	—	—	—
USRESREF	I	0.25	USB RESREF	—	Open	—	—	—	—	—
USVD330	—	3.3	USB PHY HS section 3.3-V power supply	—	—	—	—	—	—	—
USVDDH	—	1.8	USB PHY HS section 1.8-V power supply	—	—	—	—	—	—	—
USDVDD*3	—	0.8	USB PHY HS section 0.8-V power supply	—	—	—	—	—	—	—
USVBUS	I	3.3*4	USB PHY	Hi-Z	Open	—	—	—	—	—
USRX0M	I	0.8	USB PHY	—	Open	—	—	—	—	—
USRX0P	I	0.8	USB PHY	—	Open	—	—	—	—	—
USTX0M	O	0.8	USB PHY	—	Open	—	—	—	—	—
USTX0P	O	0.8	USB PHY	—	Open	—	—	—	—	—
USOTGID	I	1.8	USB PHY	—	Open	—	—	—	—	—
USVP	—	0.8	USB PHY SS section 0.8-V power supply	—	—	—	—	—	—	—
USVPH	—	3.3	USB PHY SS section 3.3-V power supply	—	—	—	—	—	—	—
USVPTX	—	0.8	USB PHY SS section transmitter power supply	—	—	—	—	—	—	—
USPWEN	O	3.3	USB I/O	L	Open	—	—	—	Selectable*2	—
USOVC	I	3.3	USB I/O	Hi-Z	Pull up	—	—	—	—	—
U4VDD18	—	1.8	1.8-V power supply	—	—	—	—	—	—	—

Table 2.2-1 List of External Pins (15/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
U4VDD08	—	0.8	0.8-V power supply	—	—	—	—	—	—	—
P2000	IO	1.8	PORT20 I/O	Hi-Z	Open	●	—	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-21**)
P2001	IO	1.8	PORT20 I/O	Hi-Z	Open	●	—	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-21**)
P2002	IO	1.8	PORT20 I/O	Hi-Z	Open	●	—	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-21**)
U5VDD18	—	1.8	1.8-V power supply	—	—	—	—	—	—	—
U5VSS	—	0	GND	—	—	—	—	—	—	—
U6VDD18	—	1.8	1.8-V power supply	—	—	—	—	—	—	—
U6VSS	—	0	GND	—	—	—	—	—	—	—
MD0	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD1	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD2	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD3	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD4	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD5	I	1.8	MD7-0 I/O	PD	Always in use	—	PD	—	—	—
MD6	I	1.8	MD7-0 I/O	PD	Always in use	—	PD	—	—	—
MD7	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	—	—	—	—
MD8*5	IO	3.3/1.8	PORT21 I/O	Hi-Z	Always in use	—	—	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-22**)
OTVDD18	—	1.8	1.8-V power supply for test	—	—	—	—	—	—	—
OTVDD08	—	0.8	0.8-V power supply for test	—	—	—	—	—	—	—
TS0AVDD18	—	1.8	TSU ch. 0 1.8-V power supply	—	—	—	—	—	—	—
TS0DVDD08A	—	0.8	TSU ch. 0 0.8-V power supply	—	—	—	—	—	—	—
TS1AVDD18	—	1.8	TSU ch. 1 1.8-V power supply	—	—	—	—	—	—	—
TS1DVDD08A	—	0.8	TSU ch. 1 0.8-V power supply	—	—	—	—	—	—	—
XIN	I	1.8	1.8-V OSC	CLOCK	Always in use	—	—	—	—	—
XOUT	O	1.8	1.8-V OSC	CLOCK	Always in use	—	—	—	—	—
RSTN	I	1.8	RSTN I/O	PU	Always in use	●	PU	—	—	—
PLVDD1	—	1.8	PLL ch. 1 1.8-V power supply	—	—	—	—	—	—	—
PLVSS1	—	0	PLL ch. 1 GND	—	—	—	—	—	—	—
PLVDD2	—	1.8	PLL ch. 2 1.8-V power supply	—	—	—	—	—	—	—
PLVSS2	—	0	PLL ch. 2 GND	—	—	—	—	—	—	—

Table 2.2-1 List of External Pins (16/16)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable / Fixed	
PLVDD3	—	1.8	PLL ch. 3 1.8-V power supply	—	—	—	—	—	—	—
PLVSS3	—	0	PLL ch. 3 GND	—	—	—	—	—	—	—
PLVDD4	—	1.8	PLL ch. 4 1.8-V power supply	—	—	—	—	—	—	—
PLVSS4	—	0	PLL ch. 4 GND	—	—	—	—	—	—	—
PLVDD6	—	1.8	PLL ch. 6 1.8-V power supply	—	—	—	—	—	—	—
PLVSS6	—	0	PLL ch. 6 GND	—	—	—	—	—	—	—
U7VDD18	—	1.8	1.8-V power supply	—	—	—	—	—	—	—
U7VSS	—	0	GND	—	—	—	—	—	—	—
PLDVDD081	—	0.8	PLL ch. 1 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD082	—	0.8	PLL ch. 2 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD083	—	0.8	PLL ch. 3 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD084	—	0.8	PLL ch. 4 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD086	—	0.8	PLL ch. 6 0.8-V power supply	—	—	—	—	—	—	—
U7VDD08	—	0.8	0.8-V power supply	—	—	—	—	—	—	—
VDD08	—	0.8	VDD08 0.8-V power supply	—	—	—	—	—	—	—
VDD18	—	1.8	VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O. 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	—	—	—	—	—	—	—
VDD33	—	3.3	VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	—	—	—	—	—	—	—
PREDVDD33	—	1.8	VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	—	—	—	—	—	—	—
RFU0-25	O	1.8	Reserved*6	—	Open	—	—	—	—	—
RETESTH0-6	I	1.8	LSI test I/O	Don't care	Pull up	—	—	—	—	—
RETESTRL	I	1.8	LSI test I/O	Hi-Z	Pull down (10kΩ)	—	—	—	—	—
U2GND0-19, U3GND0-3, U5GND0-11, U6GND0-7	—	0	GND	—	—	—	—	—	—	—
GND	—	0	GND	—	—	—	—	—	—	—

Note 1. For 3.3-V input tolerant

Note 2. For the drive strength, see **Section 3.4.2, Standard I/O Characteristics**.

Note 3. Connect an external resistor (1.1kΩ). For details, refer to *the RZ/V2MA High-Speed Interface PCB Design Guidelines*.

Note 4. See **Section 2.3, Pin Functions of Functional Blocks** for how to connect the USVBUS.

Note 5. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

Note 6. Leave these pins open-circuit.

<Usage Note>

In this LSI, supply power to all power pins.

It is necessary to supply power even if the power pin is an unused function and to connect the ground pin to the ground.

2.2.2 List of Multiplexed Functional Blocks

Table 2.2-2 List of Multiplexed Functional Blocks

I/O Group	Share Group 0	Share Group 1	Share Group 2	Share Group 3	Share Group 4	Share Group 5	Share Group 6	Share Group 7
PORT00	GPIO	—	eMMC	—	—	—	—	—
PORT01	GPIO	PWM	Ex. interrupt	CLK out	—	—	—	—
PORT02	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT03	GPIO	CSI0 CSI1 CSI2 CSI3	UART0 UART1 IIC2 IIC3 CSI3	CSI0 CSI1 CSI2	TRACE	—	—	—
PORT04	GPIO	CSI4 CSI5	CSI4 CSI5	—	TRACE	—	—	—
PORT05	GPIO	—	IIC0 IIC1	—	—	—	—	—
PORT06	GPIO	—	—	—	—	—	—	—
PORT07	GPIO	—	—	—	—	—	—	—
PORT08	GPIO	SDI0	—	—	—	—	—	—
PORT09	GPIO	SDI1	Ex. interrupt	—	—	—	—	—
PORT10	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT11	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT12	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT13	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT14	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT15	GPIO	ETHER	—	—	TRACE	—	—	—
PORT16	GPIO	ETHER	—	—	TRACE	—	—	—
PORT17	GPIO	ETHER	—	—	—	—	—	—
PORT20	GPIO	—	—	—	—	—	—	—
PORT21	GPIO	—	—	—	—	—	—	—

Table 2.2-3 I/O Group PORT00 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	eMMC	—	—	—	—	—
MMDAT0	P00_00	—	MMDAT0	—	—	—	—	—
MMDAT1	P00_01	—	MMDAT1	—	—	—	—	—
MMDAT2	P00_02	—	MMDAT2	—	—	—	—	—
MMDAT3	P00_03	—	MMDAT3	—	—	—	—	—
MMDAT4	P00_04	—	MMDAT4	—	—	—	—	—
MMDAT5	P00_05	—	MMDAT5	—	—	—	—	—
MMDAT6	P00_06	—	MMDAT6	—	—	—	—	—
MMDAT7	P00_07	—	MMDAT7	—	—	—	—	—
P0008	P00_08	—	—	—	—	—	—	—
P0009	P00_09	—	—	—	—	—	—	—
MMCMD	P00_10	—	MMCMD	—	—	—	—	—
MMCLK	P00_11	—	MMCLK	—	—	—	—	—
P0012	P00_12	—	—	—	—	—	—	—
P0013	P00_13	—	—	—	—	—	—	—

Table 2.2-4 I/O Group PORT01 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	PWM	Ex. interrupt	CLK out	—	—	—	—
PM0	P01_00	PM0	INEXINT8	—	—	—	—	—
PM1	P01_01	PM1	INEXINT9	—	—	—	—	—
PM2	P01_02	PM2	INEXINT10	—	—	—	—	—
PM3	P01_03	PM3	INEXINT11	—	—	—	—	—
PM4	P01_04	PM4	INEXINT12	—	—	—	—	—
PM5	P01_05	PM5	INEXINT13	—	—	—	—	—
PM6	P01_06	PM6	INEXINT14	GMCLK0	—	—	—	—
PM7	P01_07	PM7	INEXINT15	GMCLK1	—	—	—	—
PM8	P01_08	PM8	INEXINT16	—	—	—	—	—
PM9	P01_09	PM9	INEXINT17	—	—	—	—	—
PM10	P01_10	PM10	INEXINT18	—	—	—	—	—
PM11	P01_11	PM11	INEXINT19	—	—	—	—	—
PM12	P01_12	PM12	INEXINT20	—	—	—	—	—
PM13	P01_13	PM13	INEXINT21	—	—	—	—	—
PM14	P01_14	PM14	INEXINT22	GMCLK0	—	—	—	—
PM15	P01_15	PM15	INEXINT23	GMCLK1	—	—	—	—

Table 2.2-5 I/O Group PORT02 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
INEXINT0	P02_00	—	INEXINT0	—	—	—	—	—
INEXINT1	P02_01	—	INEXINT1	—	—	—	—	—
INEXINT2	P02_02	—	INEXINT2	—	—	—	—	—
INEXINT3	P02_03	—	INEXINT3	—	—	—	—	—
INEXINT4	P02_04	—	INEXINT4	—	—	—	—	—
INEXINT5	P02_05	—	INEXINT5	—	—	—	—	—
INEXINT6	P02_06	—	INEXINT6	—	—	—	—	—
INEXINT7	P02_07	—	INEXINT7	—	—	—	—	—

Table 2.2-6 I/O Group PORT03 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	CSI0, CSI1, CSI2, CSI3	UART0, UART1, IIC2, IIC3, CSI3	CSI0, CSI1, CSI2	TRACE	—	—	—
CSTXD0	P03_00	CSTXD0	UATX0	CSRXD0	—	—	—	—
CSRXD0	P03_01	CSRXD0	UARX0	—	—	—	—	—
CSSCLK0	P03_02	CSSCLK0	UACTS0N	—	—	—	—	—
CSCS0	P03_03	CSCS0	UARTS0N	—	—	—	—	—
CSTXD1	P03_04	CSTXD1	UATX1	CSRXD1	—	—	—	—
CSRXD1	P03_05	CSRXD1	UARX1	—	—	—	—	—
CSSCLK1	P03_06	CSSCLK1	UACTS1N	—	TRDAT15	—	—	—
CSCS1	P03_07	CSCS1	UARTS1N	—	TRDAT14	—	—	—
CSTXD2	P03_08	CSTXD2	I2SDA2	CSRXD2	TRDAT13	—	—	—
CSRXD2	P03_09	CSRXD2	I2SCL2	—	TRDAT12	—	—	—
CSSCLK2	P03_10	CSSCLK2	I2SDA3	—	TRDAT11	—	—	—
CSCS2	P03_11	CSCS2	I2SCL3	—	TRDAT10	—	—	—
CSTXD3	P03_12	CSTXD3	CSRXD3	—	TRDAT9	—	—	—
CSRXD3	P03_13	CSRXD3	—	—	TRDAT8	—	—	—
CSSCLK3	P03_14	CSSCLK3	—	—	TRDAT7	—	—	—
CSCS3	P03_15	CSCS3	—	—	TRDAT6	—	—	—

Table 2.2-7 I/O Group PORT04 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	CSI4, CSI5	CSI4, CSI5	—	TRACE	—	—	—
CSTXD4	P04_00	CSTXD4	CSRXD4	—	TRDAT5	—	—	—
CSRXD4	P04_01	CSRXD4	—	—	TRDAT4	—	—	—
CSSCLK4	P04_02	CSSCLK4	—	—	TRDAT3	—	—	—
CSCS4	P04_03	CSCS4	—	—	TRDAT2	—	—	—
CSTXD5	P04_04	CSTXD5	CSRXD5	—	TRDAT1	—	—	—
CSRXD5	P04_05	CSRXD5	—	—	TRDAT0	—	—	—
CSSCLK5	P04_06	CSSCLK5	—	—	TRCLK	—	—	—
CSCS5	P04_07	CSCS5	—	—	TRCTL	—	—	—

Table 2.2-8 I/O Group PORT05 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	IIC0, IIC1	—	—	—	—	—
I2SDA0	P05_00	—	I2SDA0	—	—	—	—	—
I2SCL0	P05_01	—	I2SCL0	—	—	—	—	—
I2SDA1	P05_02	—	I2SDA1	—	—	—	—	—
I2SCL1	P05_03	—	I2SCL1	—	—	—	—	—

Table 2.2-9 I/O Group PORT06 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
P0600	P06_00	—	—	—	—	—	—	—
P0601	P06_01	—	—	—	—	—	—	—
P0602	P06_02	—	—	—	—	—	—	—
P0603	P06_03	—	—	—	—	—	—	—
P0604	P06_04	—	—	—	—	—	—	—
P0605	P06_05	—	—	—	—	—	—	—
P0606	P06_06	—	—	—	—	—	—	—
P0607	P06_07	—	—	—	—	—	—	—
P0608	P06_08	—	—	—	—	—	—	—
P0609	P06_09	—	—	—	—	—	—	—
P0610	P06_10	—	—	—	—	—	—	—
P0611	P06_11	—	—	—	—	—	—	—

Table 2.2-10 I/O Group PORT07 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
P0700	P07_00	—	—	—	—	—	—	—
P0701	P07_01	—	—	—	—	—	—	—
P0702	P07_02	—	—	—	—	—	—	—
P0703	P07_03	—	—	—	—	—	—	—
P0704	P07_04	—	—	—	—	—	—	—
P0705	P07_05	—	—	—	—	—	—	—

Table 2.2-11 I/O Group PORT08 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	SDI0	—	—	—	—	—	—
SD0CMD	P08_00	SD0CMD	—	—	—	—	—	—
SD0CLK	P08_01	SD0CLK	—	—	—	—	—	—
SD0DAT0	P08_02	SD0DAT0	—	—	—	—	—	—
SD0DAT1	P08_03	SD0DAT1	—	—	—	—	—	—
SD0DAT2	P08_04	SD0DAT2	—	—	—	—	—	—
SD0DAT3	P08_05	SD0DAT3	—	—	—	—	—	—
SD0WP	P08_06	SD0WP	—	—	—	—	—	—
SD0CD	P08_07	SD0CD	—	—	—	—	—	—

Table 2.2-12 I/O Group PORT09 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	SDI1	Ex. interrupt	—	—	—	—	—
SD1FCMD	P09_00	SD1FCMD	—	—	—	—	—	—
SD1FCLK	P09_01	SD1FCLK	—	—	—	—	—	—
SD1FDAT0	P09_02	SD1FDAT0	—	—	—	—	—	—
SD1FDAT1	P09_03	SD1FDAT1	—	—	—	—	—	—
SD1FDAT2	P09_04	SD1FDAT2	—	—	—	—	—	—
SD1FDAT3	P09_05	SD1FDAT3	—	—	—	—	—	—
SD1FWP	P09_06	SD1FWP	INEXINT24	—	—	—	—	—
SD1FCD	P09_07	SD1FCD	INEXINT25	—	—	—	—	—

Table 2.2-13 I/O Group PORT10 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
P1000	P10_00	—	—	—	—	—	—	—
P1001	P10_01	—	—	—	—	—	—	—
P1002	P10_02	—	—	—	—	—	—	—
P1003	P10_03	—	—	—	—	—	—	—
P1004	P10_04	—	—	—	—	—	—	—
P1005	P10_05	—	—	—	—	—	—	—
P1006	P10_06	—	INEXINT26	—	—	—	—	—
P1007	P10_07	—	INEXINT27	—	—	—	—	—
P1008	P10_08	—	—	—	—	—	—	—

Table 2.2-14 I/O Group PORT11 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
P1100	P11_00	—	—	—	—	—	—	—
P1101	P11_01	—	—	—	—	—	—	—
P1102	P11_02	—	—	—	—	—	—	—
P1103	P11_03	—	—	—	—	—	—	—
P1104	P11_04	—	—	—	—	—	—	—
P1105	P11_05	—	—	—	—	—	—	—
P1106	P11_06	—	INEXINT28	—	—	—	—	—
P1107	P11_07	—	INEXINT29	—	—	—	—	—
P1108	P11_08	—	—	—	—	—	—	—

Table 2.2-15 I/O Group PORT12 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
P1200	P12_00	—	INEXINT30	—	—	—	—	—
P1201	P12_01	—	INEXINT31	—	—	—	—	—
P1202	P12_02	—	INEXINT32	—	—	—	—	—
P1203	P12_03	—	INEXINT33	—	—	—	—	—

Table 2.2-16 I/O Group PORT13 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
P1300	P13_00	—	—	—	—	—	—	—
P1301	P13_01	—	—	—	—	—	—	—
P1302	P13_02	—	—	—	—	—	—	—
P1303	P13_03	—	—	—	—	—	—	—
P1304	P13_04	—	—	—	—	—	—	—
P1305	P13_05	—	—	—	—	—	—	—
P1306	P13_06	—	—	—	—	—	—	—
P1307	P13_07	—	—	—	—	—	—	—
P1308	P13_08	—	—	—	—	—	—	—
P1309	P13_09	—	INEXINT34	—	—	—	—	—
P1310	P13_10	—	INEXINT35	—	—	—	—	—
P1311	P13_11	—	INEXINT36	—	—	—	—	—

Table 2.2-17 I/O Group PORT14 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
P1400	P14_00	—	—	—	—	—	—	—
P1401	P14_01	—	—	—	—	—	—	—
P1402	P14_02	—	INEXINT37	—	—	—	—	—
P1403	P14_03	—	—	—	—	—	—	—
P1404	P14_04	—	—	—	—	—	—	—
P1405	P14_05	—	—	—	—	—	—	—
P1406	P14_06	—	INEXINT38	—	—	—	—	—
P1407	P14_07	—	—	—	—	—	—	—

Table 2.2-18 I/O Group PORT15 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	ETHER	—	—	TRACE	—	—	—
GETXC	P15_00	GETXC	—	—	TRCLK	—	—	—
GETXEN	P15_01	GETXEN	—	—	TRCTL	—	—	—
GETXER	P15_02	GETXER	—	—	—	—	—	—
GETXD0	P15_03	GETXD0	—	—	—	—	—	—
GETXD1	P15_04	GETXD1	—	—	—	—	—	—
GETXD2	P15_05	GETXD2	—	—	—	—	—	—
GETXD3	P15_06	GETXD3	—	—	—	—	—	—
GETXD4	P15_07	GETXD4	—	—	—	—	—	—
GETXD5	P15_08	GETXD5	—	—	TRDAT0	—	—	—
GETXD6	P15_09	GETXD6	—	—	TRDAT1	—	—	—
GETXD7	P15_10	GETXD7	—	—	TRDAT2	—	—	—
GERXC	P15_11	GERXC	—	—	TRDAT3	—	—	—
GERXDV	P15_12	GERXDV	—	—	TRDAT4	—	—	—
GERXER	P15_13	GERXER	—	—	TRDAT5	—	—	—
GERXD0	P15_14	GERXD0	—	—	TRDAT6	—	—	—
GERXD1	P15_15	GERXD1	—	—	TRDAT7	—	—	—

Table 2.2-19 I/O Group PORT16 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	ETHER	—	—	TRACE	—	—	—
GERXD2	P16_00	GERXD2	—	—	TRDAT8	—	—	—
GERXD3	P16_01	GERXD3	—	—	TRDAT9	—	—	—
GERXD4	P16_02	GERXD4	—	—	TRDAT10	—	—	—
GERXD5	P16_03	GERXD5	—	—	TRDAT11	—	—	—
GERXD6	P16_04	GERXD6	—	—	TRDAT12	—	—	—
GERXD7	P16_05	GERXD7	—	—	TRDAT13	—	—	—
GECRS	P16_06	GECRS	—	—	TRDAT14	—	—	—
GECOL	P16_07	GECOL	—	—	TRDAT15	—	—	—
GEMDC	P16_08	GEMDC	—	—	—	—	—	—
GEMDIO	P16_09	GEMDIO	—	—	—	—	—	—
GEGTXCLK	P16_10	GEGTXCLK	—	—	—	—	—	—
GELINK	P16_11	GELINK	—	—	—	—	—	—
GEINT	P16_12	GEINT	—	—	—	—	—	—
GECLK	P16_13	GECLK	—	—	—	—	—	—

Table 2.2-20 I/O Group PORT17 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
P1700	P17_00	—	—	—	—	—	—	—

Table 2.2-21 I/O Group PORT20 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
P2000	P20_00	—	—	—	—	—	—	—
P2001	P20_01	—	—	—	—	—	—	—
P2002	P20_02	—	—	—	—	—	—	—

Table 2.2-22 I/O Group PORT21 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
MD8	P21_00	—	—	—	—	—	—	—

2.3 Pin Functions of Functional Blocks

Table 2.3-1 List of Pin Functions (1/5)

Classification	Pin Name	I/O	Function
Power control (PWC)	RTXIN	I	To connect a 32.768-kHz crystal resonator
	RTXOUT	O	To connect a 32.768-kHz crystal resonator
	RTRSTN	I	PWC reset input (active low)
	RTISO	I	PWC isolation input pin
	PWRSTN	I	PWC reset input (active low)
	PWTEST	I	LSI test pin, fixed to the low level
	PWEN5 to PWEN0	O	Power enable 5 to 0 (active high)
	PWSYSRSTN	O	System reset output. Connected to the RSTN pin to use the power control function of PWC.
	PWSD0SEL	O	PWC SDI0 interface power supply selection
	PWSD1SEL	O	PWC SDI1 interface power supply selection
	PWCTEST0	O	LSI test pin: leave this pin open-circuit.
	PWCTEST1	I	LSI test pin: fixed to the high level. (pulled up by the PWVDD)
	PWMEMSWIENA	O	Enable signal output pin for controlling the LPVDD power supply on/off
	PWISO	O	Open drain output. Connected to the RTISO pin and pulled up (with 10kΩ to 100kΩ) to a 1.5-V power supply.*1
eMMC interface (eMMC)	MMDAT7 to MMDAT0	I/O	eMMC data [7:0]
	MMCMD	I/O	eMMC command
	MMCLK	O	eMMC clock
Pulse-width modulation timer (PWM)	PM15 to PM0	O	PWM output
External interrupt	INEXINT38 to INEXINT0	I	External interrupt
CSI ch. 0 (CSI0)	CSTXD0	O	CSI0 serial data output
	CSRXD0	I	CSI0 serial data input
	CSSCLK0	I/O	CSI0 serial clock
	CSCS0	I	CSI0 serial chip select
CSI ch. 1 (CSI1)	CSTXD1	O	CSI1 serial data output
	CSRXD1	I	CSI1 serial data input
	CSSCLK1	I/O	CSI1 serial clock
	CSCS1	I	CSI1 serial chip select
CSI ch. 2 (CSI2)	CSTXD2	O	CSI2 serial data output
	CSRXD2	I	CSI2 serial data input
	CSSCLK2	I/O	CSI2 serial clock
	CSCS2	I	CSI2 serial chip select
CSI ch. 3 (CSI3)	CSTXD3	O	CSI3 serial data output
	CSRXD3	I	CSI3 serial data input
	CSSCLK3	I/O	CSI3 serial clock
	CSCS3	I	CSI3 serial chip select
CSI ch. 4 (CSI4)	CSTXD4	O	CSI4 serial data output
	CSRXD4	I	CSI4 serial data input
	CSSCLK4	I/O	CSI4 serial clock
	CSCS4	I	CSI4 serial chip select

Table 2.3-1 List of Pin Functions (2/5)

Classification	Pin Name	I/O	Function
CSI ch. 5 (CSI5)	CSTXD5	O	CSI5 serial data output
	CSRXD5	I	CSI5 serial data input
	CSSCLK5	I/O	CSI5 serial clock
	CSCS5	I	CSI5 serial chip select
IIC ch. 0 (IIC0)	I2SDA0	I/O	IIC0 serial data
	I2SCL0	I/O	IIC0 serial clock
IIC ch. 1 (IIC1)	I2SDA1	I/O	IIC1 serial data
	I2SCL1	I/O	IIC1 serial clock
IIC ch. 2 (IIC2)	I2SDA2	I/O	IIC2 serial data
	I2SCL2	I/O	IIC2 serial clock
IIC ch. 3 (IIC3)	I2SDA3	I/O	IIC3 serial data
	I2SCL3	I/O	IIC3 serial clock
UART ch. 0 (UART0)	UATX0	O	UART0 transmission data
	UARX0	I	UART0 reception data
	UACTS0N	I	UART0 transmission enable signal (active low)
	UARTS0N	O	UART0 reception enable signal (active low)
UART ch. 1 (UART1)	UATX1	O	UART1 transmission data
	UARX1	I	UART1 reception data
	UACTS1N	I	UART1 transmission enable signal (active low)
	UARTS1N	O	UART1 reception enable signal (active low)
SD host interface ch. 0 (SDI0)	SD0CMD	I/O	SDI0 command/response signal
	SD0CLK	O	SDI0 clock
	SD0DAT3 to SD0DAT0	I/O	SDI0 data line bits [3:0]
	SD0WP	I	SDI0 write protect signal
	SD0CD	I	SDI0 card detection signal
SD host interface ch. 1 (SDI1)	SD1FCMD	I/O	SDI1 command/response signal
	SD1FCLK	O	SDI1 clock
	SD1FDAT3 to SD1FDAT0	I/O	SDI1 data line bits [3:0]
	SD1FWP	I	SDI1 write protect signal
	SD1FCD	I	SDI1 card detection signal

Table 2.3-1 List of Pin Functions (3/5)

Classification	Pin Name	I/O	Function
Gigabit Ethernet MAC interface (ETHER)	GETXC	I	Transmission clock for Ethernet 100-Mbps mode
	GETXEN	O	Transmission enable signal (active high)
	GETXER	O	Transmission error signal (active high)
	GETXD7 to GETXD0	O	Transmission data [7:0]
	GERXC	I	Ethernet reception clock
	GERXDV	I	Reception data valid signal (active high)
	GERXER	I	Reception error signal (active high)
	GERXD7 to GERXD0	I	Receive data [7:0]
	GECRS	I	Carrier detection signal (active high)
	GECOL	I	Transmission collision signal (active high)
	GEMDC	O	PHY management clock
	GEMDIO	I/O	PHY management I/O data
	GEGTXCLK	O	GMII transmission clock
	GELINK	I	PHY LINK signal
	GEINT	I	PHY interrupt signal
	GECLK*2	I	Clock input
Debugger interface	DETCK	I	JTAG TCK
	DETDI	I	JTAG TDI
	DETDO	O	JTAG TDO
	DETMS	I/O	JTAG TMS
	DETRSTN	I	JTAG TRST (active low)
	DESRSTN	I	System reset from debugger (active low)
For LSI test	RETEST0	I	LSI test enable, fixed to the low level
	RETEST1	I	LSI test enable, fixed to the low level
	RETESTH6 to RETESTH0	I	LSI test enable, fixed to the high level (pulled up by PWVDD)
	RETESTRL	I	External reference resistor connection pin for LSI test * Resistance: 10kΩ±1%
1.2-V reference	U3REF	I	Reference pin. Supplied with 1.2 V by the resistance voltage divider of VDD33. Connected with a capacitor to prevent noise.*3
RFU	RFU25 to RFU0	O	Reserved. Leave these pins open-circuit.

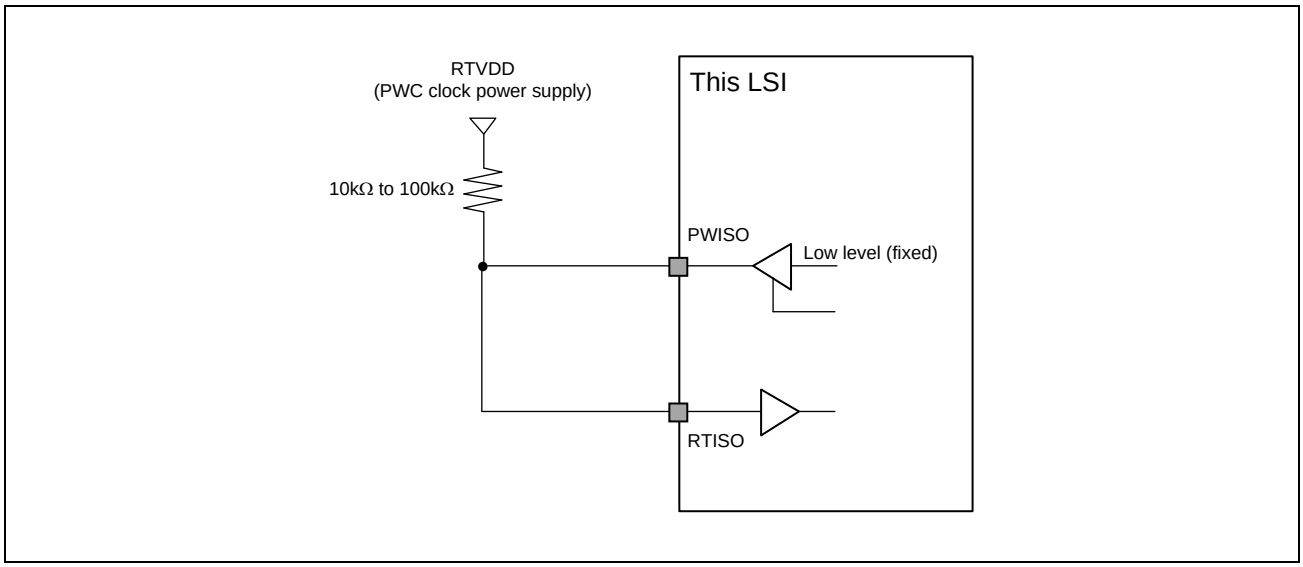
Table 2.3-1 List of Pin Functions (4/5)

Classification	Pin Name	I/O	Function
LPDDR4 interface	LPATEST	O	LSI test pin, leave this pin open-circuit.
	LPCAA5 to LPCAA0	O	DRAM address and command bits: Ch-A command/address input
	LPCAB5 to LPCAB0	O	DRAM address and command bits: Ch-B command/address input
	LPCKEA1, LPCKEA0	O	DRAM address and command bits: Ch-A clock enable
	LPCKEB1, LPCKEB0	O	DRAM address and command bits: Ch-B clock enable
	LPCLKAC	O	DRAM address and command bits: Ch-A clock (negative)
	LPCLKAT	O	DRAM address and command bits: Ch-A clock (positive)
	LPCLKBC	O	DRAM address and command bits: Ch-B clock (negative)
	LPCLKBT	O	DRAM address and command bits: Ch-B clock (positive)
	LPCSA1, LPCSA0	O	DRAM address and command bits: Ch-A chip select
	LPCSB1, LPCSB0	O	DRAM address and command bits: Ch-B chip select
	LPDMDBIA1, LPDMDBIA0	I/O	DRAM data bits and strobes: Ch-A data mask inversion
	LPDMDBIB1, LPDMDBIB0	I/O	DRAM data bits and strobes: Ch-B data mask inversion
	LPDQA15 to LPDQA0	I/O	DRAM data bits and strobes: Ch-A data input/output
	LPDQB15 to LPDQB0	I/O	DRAM data bits and strobes: Ch-B data input/output
	LPDQSAC1, LPDQSAC0	I/O	DRAM data bits and strobes: Ch-A data strobe (negative)
	LPDQSAT1, LPDQSAT0	I/O	DRAM data bits and strobes: Ch-A data strobe (positive)
	LPDQSBC1, LPDQSBC0	I/O	DRAM data bits and strobes: Ch-B data strobe (negative)
	LPDQSBT1, LPDQSBT0	I/O	DRAM data bits and strobes: Ch-B data strobe (positive)
	LPMRESETL	O	DRAM reset. Note that this requires no external resistor.
	LPZN	O	External reference resistor connection pin for use in calibration. * To connect a pull-down resistor. Resistance: 240Ω±1%
	LPDTEST	O	LSI test pin, leave this pin open-circuit.
PCI Express interface	PCRXD1P, PCRXD0P	I	Rx serial data inputs 1, 0 (positive)
	PCRXD1M, PCRXD0M	I	Rx serial data inputs 1, 0 (negative)
	PCTXD1P, PCTXD0P	O	Tx serial data outputs 1, 0 (positive)
	PCTXD1M, PCTXD0M	O	Tx serial data outputs 1, 0 (negative)
	PCREFCKP	I	Differential reference clock (positive)
	PCREFCKM	I	Differential reference clock (negative)
	PCREXT	I	Reference resistor connection pin for band-gap reference (BGR) and bias generator * To connect a pull-down resistor. Resistance: 8.2kΩ ±1%
	PCRSTOUTB	O	Reset output (for other-party PCIe devices) (active low)
USB interface	USDP	I/O	USB2.0 USB D+ signal (positive)
	USDM	I/O	USB2.0 USB D− signal (negative)
	USRESREF	I	Reference resistor connection pin * To connect a pull-down resistor. Resistance: 200Ω ±1%
	USVBUS	I	USB VBUS signal detection pin*4 * Resistance partial pressure outside the chip
	USRX0M	I	USB3.1 super-speed differential reception pair (negative)
	USRX0P	I	USB3.1 super-speed differential reception pair (positive)
	USTX0M	O	USB3.1 super-speed differential transmission pair (negative)
	USTX0P	O	USB3.1 super-speed differential transmission pair (positive)
	USOTGID	I	ID detection (OTG ID input, 0: Host, 1: Peripheral) In the initial state, an internal pull-up resistor is enabled.*5
	USPWEN	O	VBUS control signal (active high)
	USOVC	I	Overcurrent detection (active low)

Table 2.3-1 List of Pin Functions (5/5)

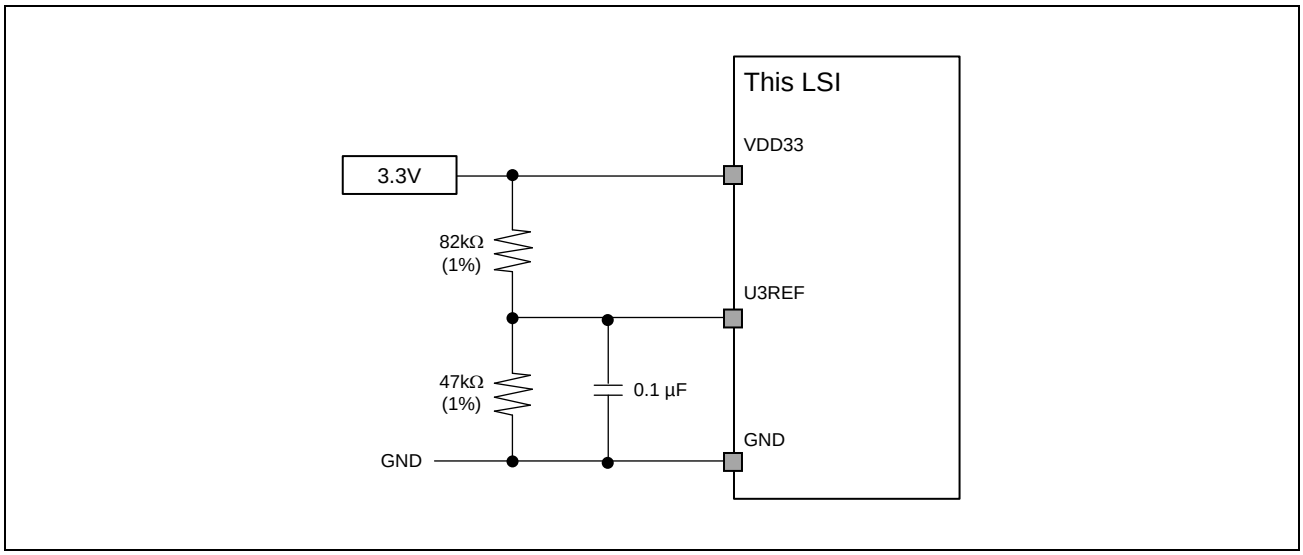
Classification	Pin Name	I/O	Function
Boot	MD2 to MD0	I	Boot device select [2:0]
	MD3	I	Boot device write interface select When not using security, fix the input level to low. When using security, prepare a circuit that is capable of switching the input level externally to low or high (pull up with VDD18).
	MD4, MD5	I	Boot mode select [1:0] (reserved) Fix the pin to the low level.
	MD6	I	Boot mode select [2]
	MD7	I	Boot mode select [3] (reserved) Fix the pin to the low level.
	MD8	I/O	Boot GPIO (LED control when booted)*6
Clock/reset	XIN	I	To connect a 48-MHz crystal resonator
	XOUT	O	To connect a 48-MHz crystal resonator
	RSTN	I	System reset (active low)
Clock output	GMCLK0	O	Clock output 0
	GMCLK1	O	Clock output 1
Trace interface (TRACE)	TRDAT15 to TRDAT0	O	Trace data [15:0]
	TRCLK	O	Trace clock
	TRCTL	O	Trace control
General-purpose input/output ports (GPIO)	P00_13 to P00_00	I/O	GPIO port 00 [13:0]
	P01_15 to P01_00	I/O	GPIO port 01 [15:0]
	P02_07 to P02_00	I/O	GPIO port 02 [7:0]
	P03_15 to P03_00	I/O	GPIO port 03 [15:0]
	P04_07 to P04_00	I/O	GPIO port 04 [7:0]
	P05_03 to P05_00	I/O	GPIO port 05 [3:0]
	P06_11 to P06_00	I/O	GPIO port 06 [11:0]
	P07_05 to P07_00	I/O	GPIO port 07[5:0]
	P08_07 to P08_00	I/O	GPIO port 08[7:0]
	P09_07 to P09_00	I/O	GPIO port 09[7:0]
	P10_08 to P10_00	I/O	GPIO port 10[8:0]
	P11_08 to P11_00	I/O	GPIO port 11[8:0]
	P12_03 to P12_00	I/O	GPIO port 12[3:0]
	P13_11 to P13_00	I/O	GPIO port 13[11:0]
	P14_07 to P14_00	I/O	GPIO port 14[7:0]
	P15_15 to P15_00	I/O	GPIO port 15[15:0]
	P16_13 to P16_00	I/O	GPIO port 16[13:0]
	P17_00	I/O	GPIO port 17[0]
	P20_02 to P20_00	I/O	GPIO port 20[2:0]
	P21_00	I/O	GPIO port 21[0]*6

Note 1. The PWISO and RTISO pins are connected to this LSI, and these nodes should be pulled up with a 10kΩ to 100kΩ resistor. The schematic diagram is shown below.

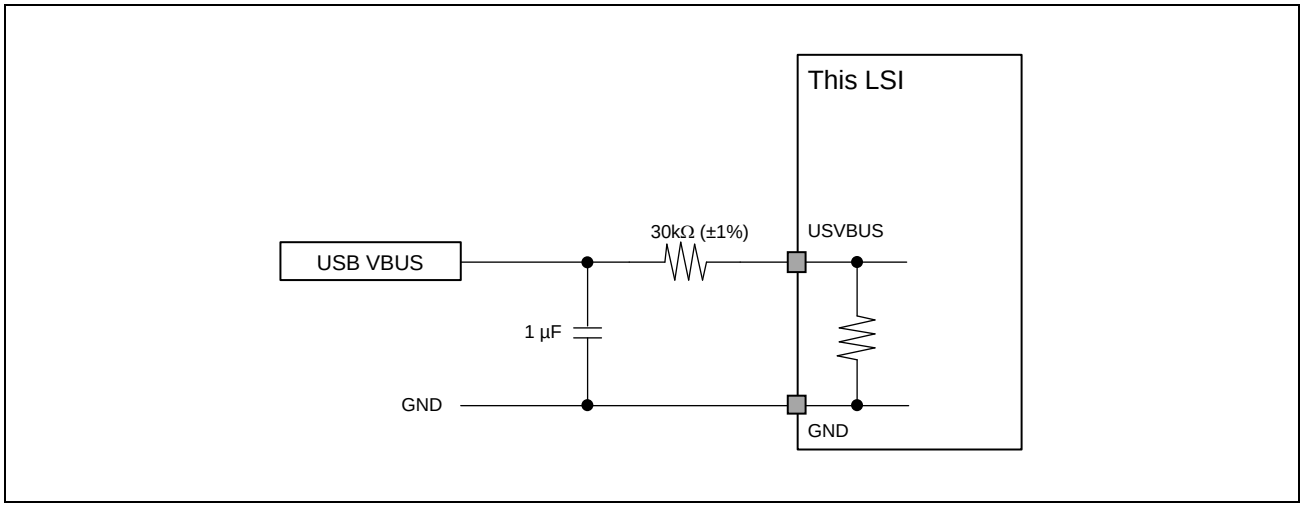


Note 2. GECLK is the input clock for GEGTXCLK.

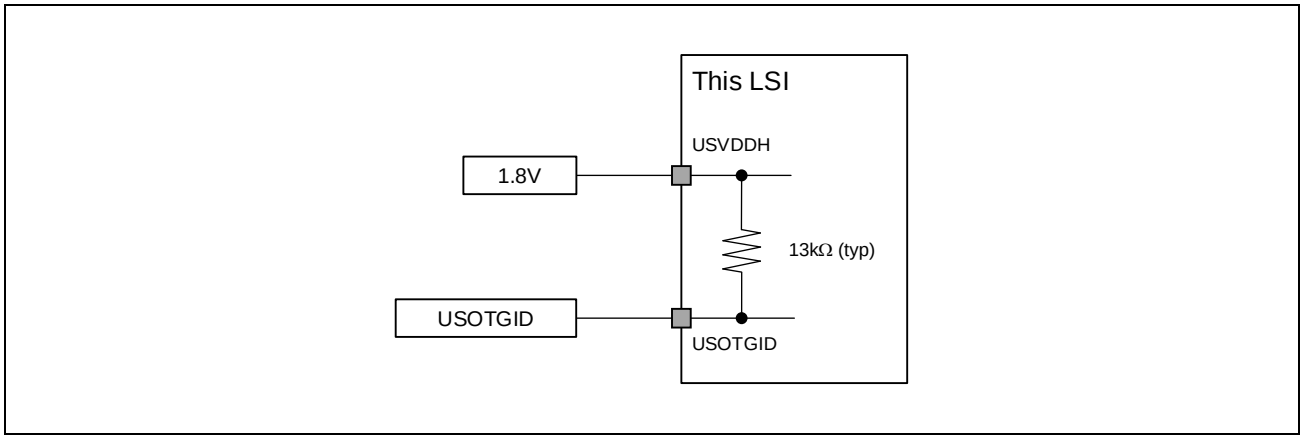
Note 3. U3REF is supplied with 1.2 V by the resistance voltage divider of VDD33. The schematic diagram is shown below.



Note 4. Since this LSI has a resistor mounted between the USVBUS pin and GND, connect the pin to the USVBUS pin via a 30-kΩ (±1%) resistor. The schematic diagram is shown below.
In addition, design so that the voltage is applied to the USVBUS pin after supplying USDVDD, USVP and USVPTX.



Note 5. USOTGID has the internal pull-up resistor.



Note 6. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

Section 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 3.1-1 Absolute Maximum Ratings (1/3)

Item	Symbol	Min.	Max.	Unit
VDD08 core power supply	V_{DD08}	−0.4	1.2	V
XTAL power supply	RTV_{DD08}	−0.4	1.2	V
PWC clock power supply	RTV_{DD}	−0.4	2.5	V
PWC core power supply	PWV_{DD08}	−0.4	1.2	V
PWC I/O power supply	PWV_{DD}	−0.4	2.5	V
PORT01(A), PORT03 pre-driver power supply	$PAPREDV_{DD}$	−0.4	2.5	V
PORT01(A), PORT03 I/O power supply	$PAMODV_{DD}$	−0.4	3.8	V
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	$PBPREDV_{DD}$	−0.4	2.5	V
PORT01(B), PORT04, PORT07, PORT21 I/O power supply	$PBMODV_{DD}$	−0.4	3.8	V
PORT06 pre-driver power supply	$PCPREDV_{DD}$	−0.4	2.5	V
PORT06 I/O power supply	$PCMODV_{DD}$	−0.4	3.8	V
PORT10 pre-driver power supply	$U10V_{DD18}$	−0.4	2.5	V
PORT10 I/O power supply	$U10MODV_{DD}$	−0.4	3.8	V
PORT11 pre-driver power supply	$U11V_{DD18}$	−0.4	2.5	V
PORT11 I/O power supply	$U11MODV_{DD}$	−0.4	3.8	V
PORT00 pre-driver power supply	$MMPREDV_{DD}$	−0.4	2.5	V
PORT00 I/O power supply	$MMMODV_{DD}$	−0.4	3.8	V
PORT08 pre-driver power supply	$SD0PREDV_{DD}$	−0.4	2.5	V
PORT08 I/O power supply	$SD0MODV_{DD}$	−0.4	3.8	V
PORT09 pre-driver power supply	$SD1FV_{DD}$	−0.4	2.5	V
PORT09 I/O power supply	$SD1FMODV_{DD}$	−0.4	3.8	V
PORT15, PORT16, PORT17 pre-driver power supply	$GEPREDV_{DD}$	−0.4	2.5	V
PORT15, PORT16, PORT17 I/O power supply	$GEMODV_{DD}$	−0.4	3.8	V

Table 3.1-1 Absolute Maximum Ratings (2/3)

Item	Symbol	Min.	Max.	Unit
VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O. 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	V_{DD18}	−0.4	2.5	V
VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$PREDV_{DD33}$	−0.4	2.5	V
VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	V_{DD33}	−0.4	3.8	V
PLL ch. 1, 2, 3, 4, 6 0.8-V power supply	$PLDV_{DD08n}$ (n = 1, 2, 3, 4, 6)	−0.4	1.2	V
PLL ch. 1, 2, 3, 4, 6 1.8-V power supply	PLV_{DDn} (n = 1, 2, 3, 4, 6)	−0.4	2.5	V
0.8-V power supply for test	OTV_{DD08}	−0.4	1.2	V
1.8-V power supply for test	OTV_{DD18}	−0.4	2.5	V
TSU ch. 0 0.8-V power supply	$TS0DV_{DD08A}$	−0.4	1.2	V
TSU ch. 1 0.8-V power supply	$TS1DV_{DD08A}$	−0.4	1.2	V
TSU ch. 0 1.8-V power supply	$TS0AV_{DD18}$	−0.4	2.5	V
TSU ch. 1 1.8-V power supply	$TS1AV_{DD18}$	−0.4	2.5	V
Sub-unit 0.8-V power supply	UnVDD08 (n = 2, 3, 4, 7)	−0.4	1.2	V
Sub-unit 1.8-V power supply	UnVDD18 (n = 2, 3, 4, 5, 6, 7)	−0.4	2.5	V
LPDDR4 core 0.8-V power supply	LPV_{DD}	−0.4	1.2	V
LPDDR4 PLL 1.8-V power supply	LPV_{AA}	−0.4	2.5	V
LPDDR4 I/O 1.1-V power supply	LPV_{DDQ}	−0.4	1.5	V
PCIe PHY 0.8-V power supply	PCV_{DD08}	−0.4	1.2	V
PCIe PHY 1.8-V power supply	PCV_{DD18}	−0.4	2.5	V
USB PHY HS section 3.3-V power supply	USV_{D330}	−0.4	3.8	V
USB PHY HS section 1.8-V power supply	USV_{DDH}	−0.4	2.5	V
USB PHY HS section 0.8-V power supply	$USDV_{DD}$	−0.4	1.2	V
USB PHY SS section 0.8-V power supply	USV_{P}	−0.4	1.2	V
USB PHY SS section 3.3-V power supply	USV_{PH}	−0.4	3.8	V
USB3.0 transmitter power supply	USV_{PTX}	−0.4	1.2	V
Input voltage (1.1-V I/O)	V_{in11}	−0.4	LPV_{DDQ}+0.3*3	V
Input voltage (1.5-V I/O)	V_{in15}	−0.4	RTV_{DD} + 0.3*4	V
Input voltage (1.8-V I/O)*1	V_{in18}	−0.4	V_{18} + 0.3*5	V

Table 3.1-1 Absolute Maximum Ratings (3/3)

Item	Symbol	Min.	Max.	Unit
Input voltage (1.8-V I/O (3.3-V tolerant))*2	V_{in18_tol}	−0.4	3.6	V
Input voltage (3.3-V I/O)	V_{in33}	−0.4	V_{33} + 0.3*6	V
Junction temperature	T_j	−40	125	°C
Storage temperature	T_{stg}	−40	150	°C

Note 1. 1.8-V I/O (except for PORT02 I/O and PORT05 I/O)

Note 2. 1.8-V I/O (PORT02 I/O and PORT05 I/O)

Note 3. The voltage to be applied must be within the absolute maximum rating (1.5 V).

Note 4. The voltage to be applied must be within the absolute maximum rating (2.5 V).

Note 5. The voltage to be applied must be within the absolute maximum rating (2.5 V). V18 indicates the power supply voltage for 1.8-V I/O pins.

Note 6. The voltage to be applied must be within the absolute maximum rating (3.8 V). V33 indicates the power supply voltage for 3.3-V I/O pins.

3.2 Recommended Operating Range

Table 3.2-1 Recommended Operating Range (1/2)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
VDD08 core power supply	V_{DD08}	0.76	0.8	0.84	V	
XTAL power supply	RTV_{DD08}	0.76	0.8	0.84	V	
PWC clock power supply	RTV_{DD}	1.425	1.5	1.575	V	
PWC core power supply	PWV_{DD08}	0.76	0.8	0.84	V	
PWC I/O power supply	PWV_{DD}	1.71	1.8	1.89	V	
PORT01(A), PORT03 pre-driver power supply	$PAPREDV_{DD}$	1.71	1.8	1.89	V	
PORT01(A), PORT03 I/O power supply	$PAMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	$PBPREDV_{DD}$	1.71	1.8	1.89	V	
PORT01(B), PORT04, PORT07, PORT21 I/O power supply	$PBMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT06 pre-driver power supply	$PCPREDV_{DD}$	1.71	1.8	1.89	V	
PORT06 I/O power supply	$PCMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT10 pre-driver power supply	$U10V_{DD18}$	1.71	1.8	1.89	V	
PORT10 I/O power supply	$U10MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT11 pre-driver power supply	$U11V_{DD18}$	1.71	1.8	1.89	V	
PORT11 I/O power supply	$U11MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT00 pre-driver power supply	$MMPREDV_{DD}$	1.71	1.8	1.89	V	
PORT00 I/O power supply	$MMMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT08 pre-driver power supply	$SD0PREDV_{DD}$	1.71	1.8	1.89	V	
PORT08 I/O power supply	$SD0MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT09 pre-driver power supply	$SD1FV_{DD}$	1.71	1.8	1.89	V	
PORT09 I/O power supply	$SD1FMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT15, PORT16, PORT17 pre-driver power supply	$GEPREDV_{DD}$	1.71	1.8	1.89	V	
PORT15, PORT16, PORT17 I/O power supply	$GEMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O. 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	V_{DD18}	1.71	1.8	1.89	V	
VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$PREDV_{DD33}$	1.71	1.8	1.89	V	

Table 3.2-1 Recommended Operating Range (2/2)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	V_{DD33}	3.135	3.3	3.465	V	
PLL ch. 1, 2, 3, 4, 6 0.8-V power supply	$PLDV_{DD08n}$, (n = 1, 2, 3, 4, 6)	0.76	0.8	0.84	V	
PLL ch. 1, 2, 3, 4, 6 1.8-V power supply	PLVDDn (n = 1, 2, 3, 4 ,6)	1.71	1.8	1.89	V	
0.8-V power supply for test	OTV_{DD08}	0.76	0.8	0.84	V	
1.8-V power supply for test	OTV_{DD18}	1.71	1.8	1.89	V	
TSU ch. 0 0.8-V power supply	$TS0DV_{DD08A}$	0.76	0.8	0.84	V	
TSU ch. 1 0.8-V power supply	$TS1DV_{DD08A}$	0.76	0.8	0.84	V	
TSU ch. 0 1.8-V power supply	$TS0AV_{DD18}$	1.71	1.8	1.89	V	
TSU ch. 1 1.8-V power supply	$TS1AV_{DD18}$	1.71	1.8	1.89	V	
Sub-unit 0.8-V power supply	UnVDD08 (n = 2, 3, 4, 7)	0.76	0.8	0.84	V	
Sub-unit 1.8-V power supply	UnVDD18 (n = 2, 3, 4, 5, 6, 7)	1.71	1.8	1.89	V	
LPDDR4 core 0.8-V power supply	LPV_{DD}	0.76	0.8	0.84	V	
LPDDR4 PLL 1.8-V power supply	LPV_{AA}	1.71	1.8	1.89	V	
LPDDR4 PHY 1.1-V power supply	LPV_{DDQ}	1.06	1.1	1.17	V	
PCIe PHY 0.8-V power supply	PCV_{DD08}	0.76	0.8	0.84	V	
PCIe PHY 1.8-V power supply	PCV_{DD18}	1.71	1.8	1.89	V	
USB PHY SS section 0.8-V power supply	USV_{P}	0.76	0.8	0.84	V	
USB PHY HS section 1.8-V power supply	USV_{DDH}	1.71	1.8	1.89	V	
USB PHY HS section 3.3-V power supply	USV_{D330}	3.135	3.3	3.465	V	
USB PHY HS section 0.8-V power supply	$USDV_{DD}$	0.76	0.8	0.84	V	
USB PHY SS section transmitter power supply	USV_{PTX}	0.76	0.8	0.84	V	
USB PHY SS section 3.3-V power supply	USV_{PH}	3.135	3.3	3.465	V	
Junction temperature	T_j	—	—	103	°C	

3.3 Power-On/Off Procedures

3.3.1 Power-On Sequence (PWC)

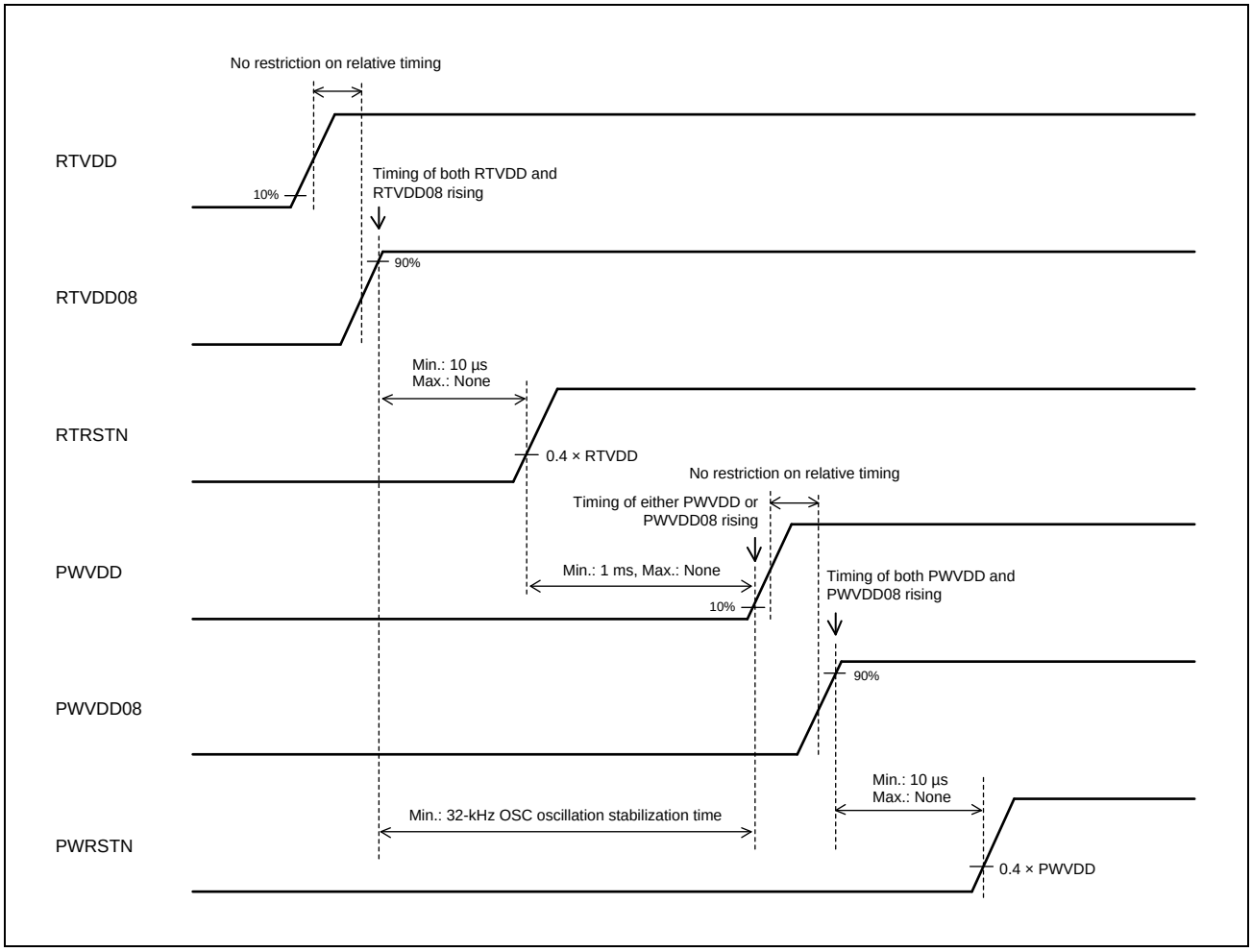
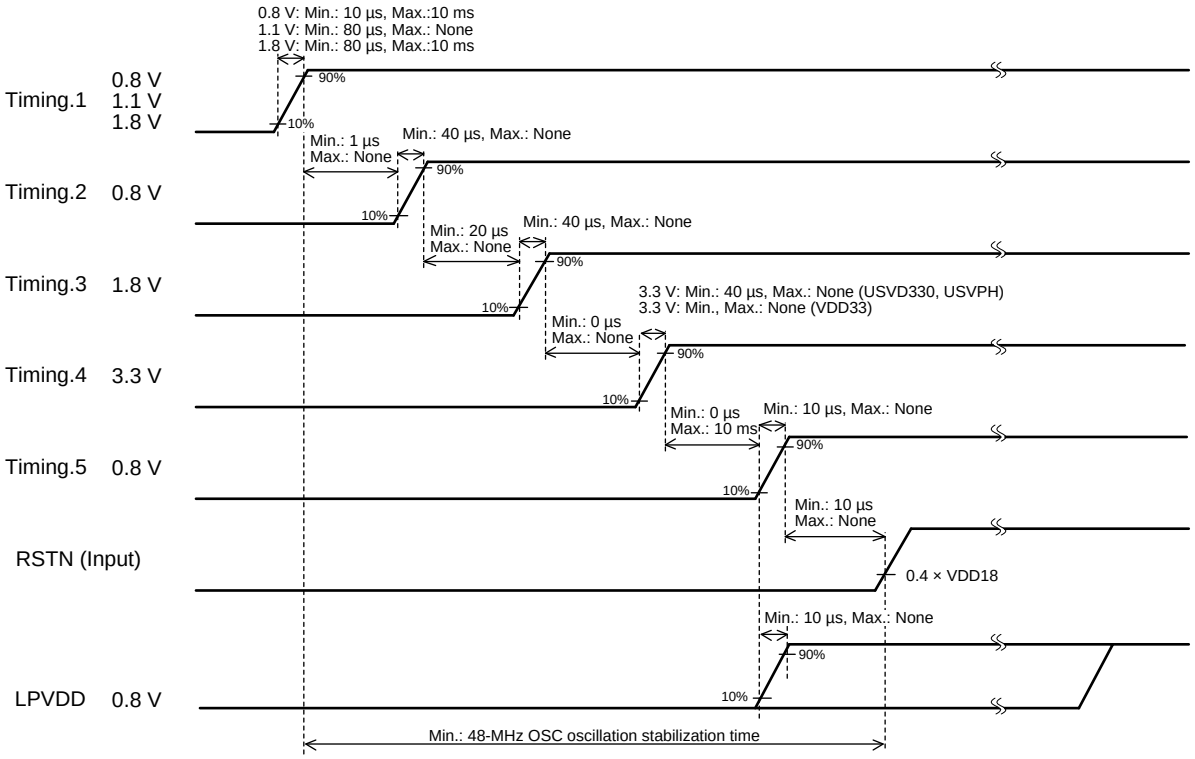


Figure 3.3-1 Power-On Sequence (PWC)

3.3.2 Power-On/Off Sequence (other than for PWC)

3.3.2.1 Power-On Sequence (other than for PWC)



Note: See **Table 3.3-1**, **Table 3.3-2**, and **Table 3.3-3** for the power supplies which are turned on with the given timing.

Figure 3.3-2 Power-On Sequence (other than for PWC)

Table 3.3-1, **Table 3.3-2**, and **Table 3.3-3** show the correspondence between the power supplies and the power-on (off) timings.

Table 3.3-1 Various Power Supplies and Power On/Off Timings

Power Voltage	Power Supply Name	Timing
0.8 V	VDD08	Timing.1
1.1 V	LPVDDQ	
1.8 V	VDD18, LPVAA	
0.8 V	U2VDD08, U3VDD08, U4VDD08, PCVDD08, OTVDD08	Timing.2
1.8 V	U2VDD18, U3VDD18, U4VDD18, PCVDD18, OTVDD18, USVDDH	Timing.3
3.3 V	VDD33, USVD330, USVPH	Timing.4
0.8 V	USDVDD, USVP, USVPTX, LPVDD*1	Timing.5

Note 1. When not controlled by the System FW, the power is on (off) at Timing.5.
When controlled by the System FW, connect the 0.8-V power supply to the LPVDD pin of this LSI via the power switch. In addition, connect the PWMEMSWIENA pin of this LSI to an enable pin of this power switch.

Table 3.3-2 Various Power Supplies and Power On/Off Timings (PLL, TSU, etc.)

Power Voltage	Power Supply Name	Timing
0.8 V	U7VDD08, PLDVDD08n (n = 1, 2, 3, 4, 6), TSnDVDD08A (n = 0, 1)	Timing.1 or Timing.2
1.8 V	U5VDD18, U6VDD18, U7VDD18, PLVDDn (n = 1, 2, 3, 4, 6), TSnAVDD18 (n = 0, 1), PREDVDD33	Timing.1 or Timing.3

Table 3.3-3 Various Power Supplies and Power On/Off Timings (1.8-V/3.3-V Switching I/O)

I/O Voltage	Power Supply Name	Case	Timing
Used as the 1.8-V I/O	Pre-driver power supply*1	1	Timing.1
	I/O power supply*2		
	Pre-driver power supply*1	2	Timing.1
	I/O power supply*2		Timing.3
	Pre-driver power supply*1	3	Timing.3
	I/O power supply*2		
Used as the 3.3-V IO	Pre-driver power supply*1	4	Timing.1
	I/O power supply*2		Timing.4
	Pre-driver power supply*1	5	Timing.3
	I/O power supply*2		Timing.4

Note 1. MMPREDVDD, PAPREDVDD,PBPREDVDD, PCPREDVDD, SD0PREDVDD, SD1FVDD, U10VDD18, U11VDD18, GEPREDVDD

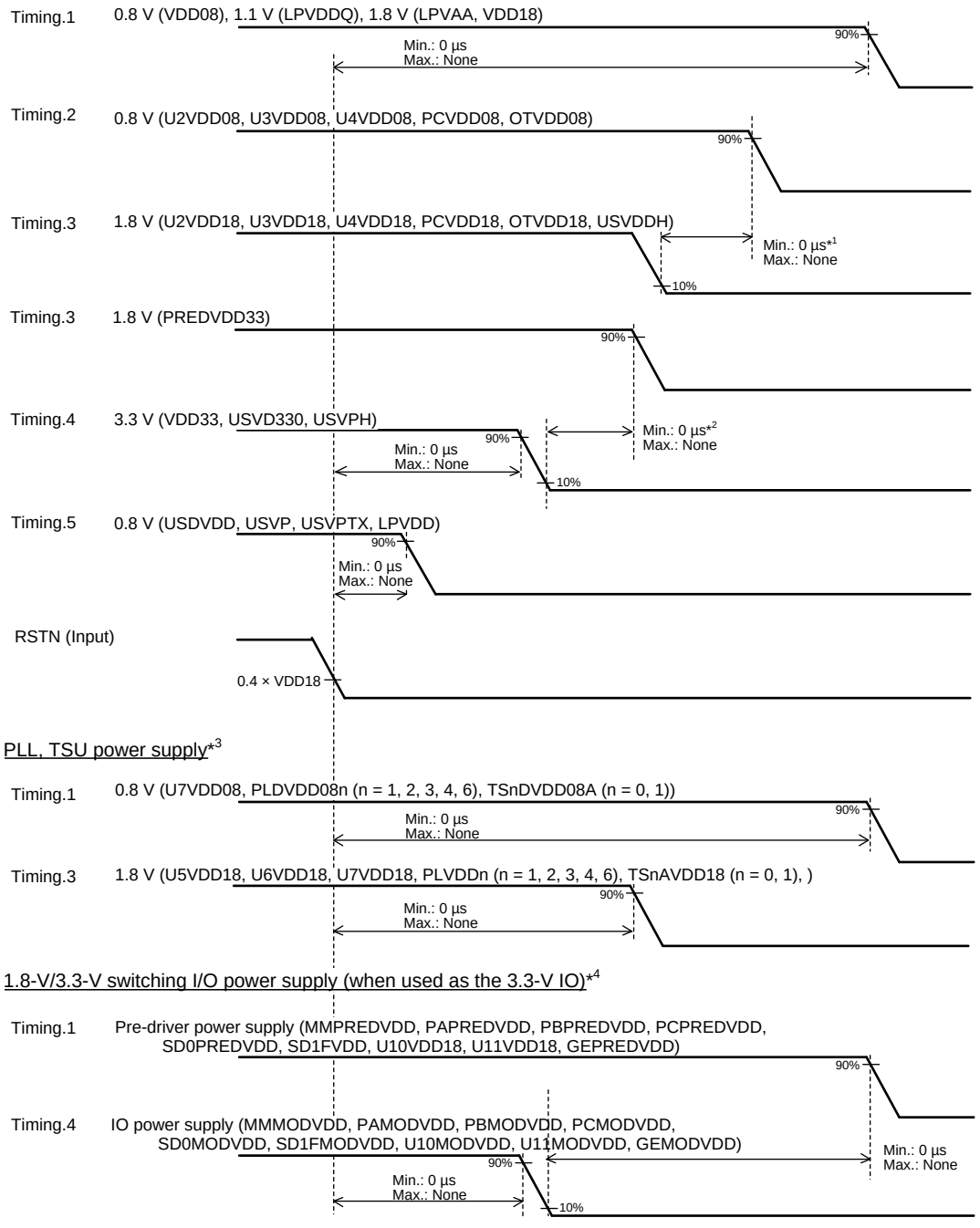
Note 2. MMMODVDD, PAMODVDD, PBMODVDD, PCMODVDD, SD0MODVDD, SD1FMODVDD, U10MODVDD, U11MODVDD, GEMODVDD

The following restrictions apply to the order of turning on the pre-driver power supply and the I/O power supply for the power supply of the 1.8-V/3.3-V switching I/O.

- When used as the 1.8-V I/O, “the pre-driver power supply and the I/O power supply are turned on at the same time” or “the pre-driver power supply is turned on first and then the I/O power supply”.
- When used as the 3.3-V I/O, “the pre-driver power supply is turned on first and then the I/O power supply”.

When used as the 1.8-V I/O, the pre-driver power supply and the I/O power supply must be turned on or off in case 1, 2, or 3. When used as the 3.3-V I/O, they must be turned on or off in case 4 or 5.

3.3.2.2 Power-Off Sequence (other than for PWC)



Note: The power off time difference must be minimized.

Note 1. The power supply in the case of Timing.2 (0.8 V) must be turned off no less than 0 ns after the power supply in the case of Timing.3 (1.8 V) is turned off

Note 2. The power supply in the case of Timing.3 (1.8 V) must be turned off no less than 0 ns after the power supply in the case of Timing.4 (3.3 V) is turned off.

Note 3. The 0.8-V power supply and the 1.8-V power supply are indicated in the case of Timing.1 and Timing.3, respectively. No restrictions apply to the order of turning off the 0.8-V power supply and the 1.8-V power supply.

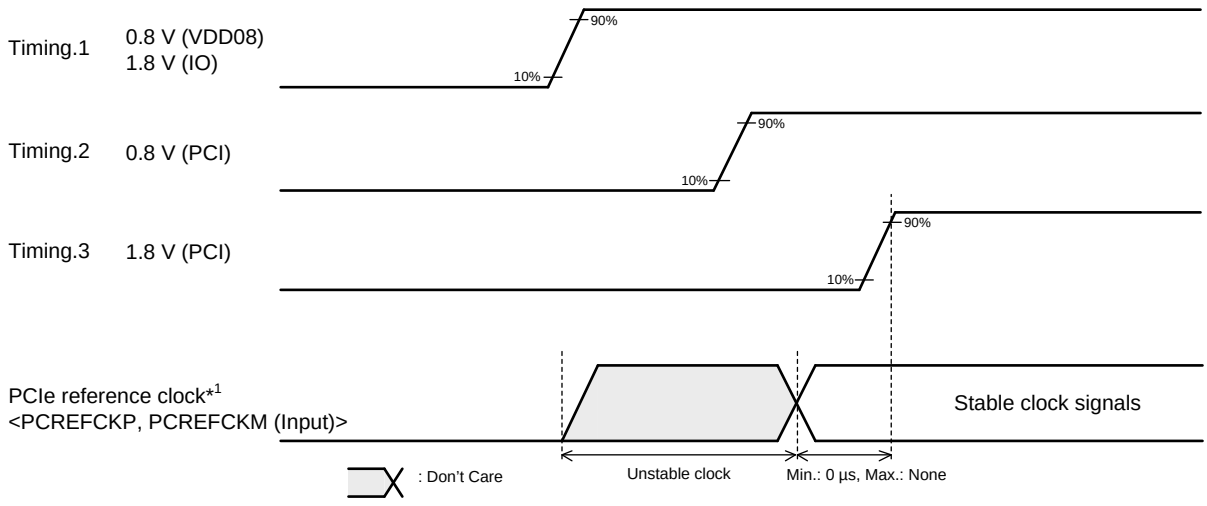
(*Continuation of the previous page*)

Note 4. This is used as the 3.3-V I/O, and the pre-driver power supply and the I/O power supply are indicated in the case of Timing.1 and Timing.4, respectively.
The pre-driver power supply must be turned off no less than 0 ns after the I/O power supply is turned off.
When used as the 1.8-V I/O, no restrictions apply to the order of turning on the pre-driver power supply and the I/O power supply.

Figure 3.3-3 Power-Off Sequence (other than for PWC)

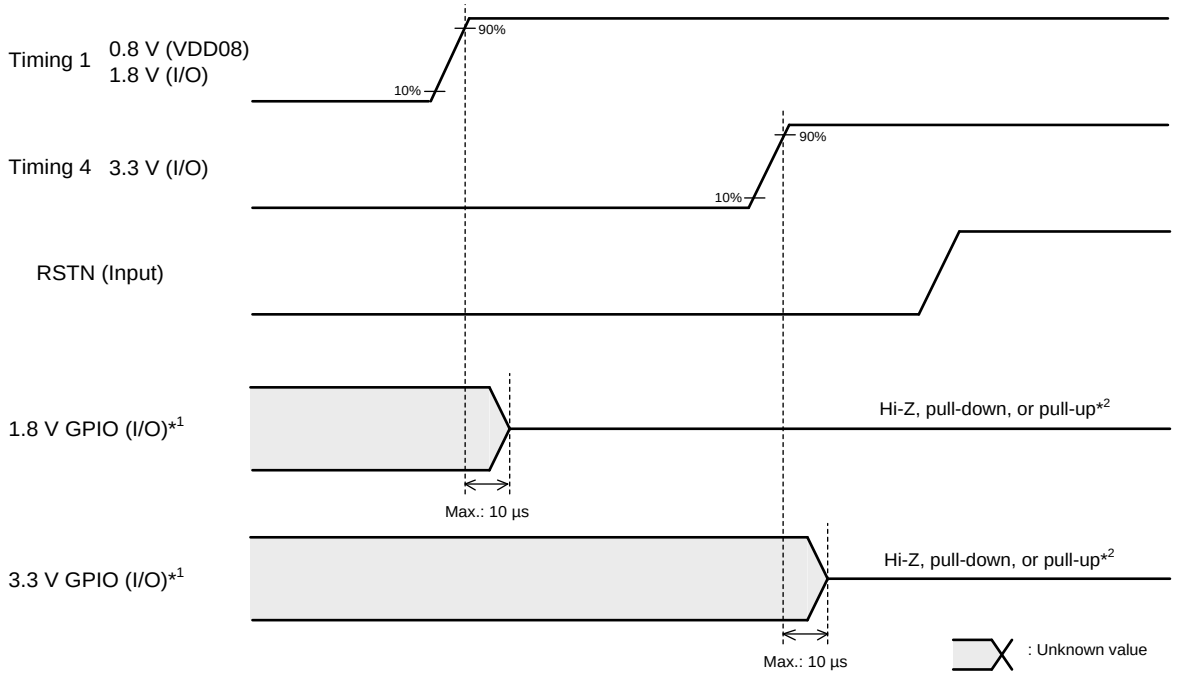
3.3.3 Timing Limitations when Power is being Turned On

Control the input signals according to the timing limitations for power being turned on.



Note 1. For the PCIe reference clock, input the clock signal after the oscillation stabilization before the PCI 1.8-V power supply (PCVDD18) is risen.

Figure 3.3-4 PCI Reference Clock Input Timing



Note 1. After both the internal power and I/O power supply voltages (1.8 V or 3.3 V) have risen, the reset is effective by the time 10 µs (max.) have elapsed and the pin states are stable. The pin states are not guaranteed between the supply voltages rising and the reset becoming effective.

Note 2. The state depends on the pin. For the initial states of the respective pins, refer to “Initial Value after POR” in the list of external pins.

Figure 3.3-5 GPIO Timing at Power-On

3.4 DC Characteristics

3.4.1 Supply Current

3.4.1.1 Maximum Supply Current

Conditions for the supply current: Power supply voltage = Max. value, Tj = −40 to 125ºC

Table 3.4-1 Max. Supply Currents during Operation (1/2)

Item	Symbol	Max.	Unit	Note
VDD08 core power supply current	I_{DD08}	3816	mA	The current must be within the maximum supply current.
XTAL power supply current	$I_{DDRTVDD08}$	700	µA	RTV_{DD08}*1
PWC clock power supply current	$I_{DDRTVDD}$	300*3	µA	RTV_{DD}*2
PWC core power supply current	$I_{DDPWVDD08}$	1	mA	PWV_{DD08}
PWC I/O power supply current	$I_{DDPWVDD}$	3	mA	PWV_{DD}
PORT01(A), PORT03 pre-driver power supply current	$I_{DDPAPRE}$	2	mA	$PAPREDV_{DD}$: PWM0 - 7, CSI0, TRDAT6 - 15
PORT01(A), PORT03 I/O power supply current	$I_{DDPAMOD}$	23	mA	$PAMODV_{DD}$: PWM0 - 7, CSI0, TRDAT6 - 15
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply current	$I_{DDPBPRE}$	1	mA	$PBPREDV_{DD}$: PWM8 - 15, TRACE0 - 6
PORT01(B), PORT04, PORT07, PORT21 I/O power supply current	$I_{DDPBMOD}$	16	mA	$PBMODV_{DD}$: PWM8 - 15, TRACE0 - 6
PORT06 pre-driver power supply current	$I_{DDPCPRE}$	1	mA	$PCPREDV_{DD}$: P0600 - 11
PORT06 I/O power supply current	$I_{DDPCMOD}$	11	mA	$PCMODV_{DD}$: P0600 - 11
PORT10 pre-driver power supply current	$I_{DDU10PRE}$	1	mA	$U10V_{DD18}$
PORT10 I/O power supply current	$I_{DDU10MOD}$	4	mA	$U10MODV_{DD}$
PORT11 pre-driver power supply current	$I_{DDU11PRE}$	1	mA	$U11V_{DD18}$
PORT11 I/O power supply current	$I_{DDU11MOD}$	4	mA	$U11MODV_{DD}$
PORT00 pre-driver power supply current	$I_{DDMMPRE}$	2	mA	$MMPREDV_{DD}$: eMMC HS200
PORT00 I/O power supply current	$I_{DDMMMOD}$	10	mA	$MMMODV_{DD}$: eMMC HS200
PORT08 pre-driver power supply current	$I_{DDSD0PRE}$	1	mA	$SD0PREDV_{DD}$: SDIO SDR104
PORT08 I/O power supply current	$I_{DDSD0MOD}$	16	mA	$SD0MODV_{DD}$: SDIO SDR104
PORT09 pre-driver power supply current	I_{DDSD1F}	1	mA	$SD1FV_{DD}$: SDIO SDR104
PORT09 I/O power supply current	$I_{DDSD1MOD}$	16	mA	$SD1FMODV_{DD}$: SDIO SDR104
PORT15, PORT16, PORT17 pre-driver power supply current	$I_{DDGEPRE}$	1	mA	$GEPREDV_{DD}$
PORT15, PORT16, PORT17 I/O power supply current	$I_{DDGEMOD}$	17	mA	$GEMODV_{DD}$
VDD18 group I/O power supply current (PORT02 I/O, PORT05 I/O, PORT20 I/O. 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	I_{DD18}	3	mA	V_{DD18}: IIC0 - 1, DEBUG

Table 3.4-1 Max. Supply Currents during Operation (2/2)

Item	Symbol	Max.	Unit	Note
VDD33 group pre-driver power supply current (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$I_{DDPRE33}$	2	mA	$PREDV_{DD33}$
VDD33 group I/O power supply current (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	I_{DD33}	20	mA	V_{DD33}
PLL ch. 1, 2, 3, 4, 6 0.8-V power supply current	I_{DDPL08}	16	mA	Total of $PLDV_{DD081}$, $PLDV_{DD082}$, $PLDV_{DD083}$, $PLDV_{DD084}$, $PLDV_{DD086}$
PLL ch. 1, 2, 3, 4, 6 1.8-V power supply current	I_{DDPL18}	14	mA	Total of PLV_{DD1}, PLV_{DD2}, PLV_{DD3}, PLV_{DD4}, PLV_{DD6}
0.8-V power supply current	I_{DDOT08}	9	mA	OTV_{DD08}
1.8-V power supply current	I_{DDOT18}	60	mA	OTV_{DD18}
TSU ch. 0 0.8-V power supply current	I_{DDTS08}	1	mA	$TS0DV_{DD08A}$
TSU ch. 1 0.8-V power supply current	I_{DDTS08}	1	mA	$TS1DV_{DD08A}$
TSU ch. 0 1.8-V power supply current	I_{DDTS18}	4	mA	$TS0AV_{DD18}$
TSU ch. 1 1.8-V power supply current	I_{DDTS18}	4	mA	$TS1AV_{DD18}$
Sub-unit 0.8-V power supply	I_{DDU08}	15	mA	Total of $U2V_{DD08}$, $U3V_{DD08}$, $U4V_{DD08}$, $U7V_{DD08}$
Sub-unit 1.8-V power supply	I_{DDU18}	8	mA	Total of $U2V_{DD18}$, $U3V_{DD18}$, $U4V_{DD18}$, $U5V_{DD18}$, $U6V_{DD18}$, $U7V_{DD18}$
LPDDR4 core 0.8-V power supply current	$I_{DDLPVDD}$	800	mA	LPV_{DD}: 3200 Mbps
LPDDR4 PLL 1.8-V power supply current	$I_{DDLPVAA}$	6	mA	LPV_{AA}: 3200 Mbps
LPDDR4 PHY 1.1-V power supply current	$I_{DDLPVDDQ}$	314	mA	LPV_{DDQ}: 3200 Mbps
PCIe PHY 0.8-V power supply current	I_{DDPC08}	188	mA	PCV_{DD08}
PCIe PHY 1.8-V power supply current	I_{DDPC18}	132	mA	PCV_{DD18}
USB PHY 0.8-V power supply current	I_{DDUS08}	88	mA	Total of $USDV_{DD}$, USV_{P}, USV_{PTX}
USB PHY 1.8-V power supply current	I_{DDUS18}	21	mA	USV_{DDH}
USB PHY 3.3-V power supply current	I_{DDUS33}	57	mA	Total of USV_{D330}, USV_{PH}

Note 1. Reference value for the XTAL power supply current (at normal temperature at 0.8 V): 35 µA

Note 2. Reference value for the PWC clock power supply current (at normal temperature at 1.5 V): 10 µA

Note 3. In normal operation, current flows to the PWISO pin via a pull-up resistor, so this amount of current must be taken into account when the current drawn is estimated.
[*Example*] When the pull-up resistance is 10kΩ, 1.5 V/10kΩ = 150 µA

3.4.2 Standard I/O Characteristics

For the I/O groups, refer to the multiplexed pin group numbers in the list of external pins.

Table 3.4-2 DC Characteristics

V_{DD} = 1.35 V to 1.65 V (I.5-V I/O group), V_{DD} = 1.65 V to 1.95 V (1.8-V I/O groups 1, 2, 3, and 4), V_{DD} = 1.65 V to 3.60 V (3.3/1.8-V switching I/O groups 1 and 2), V_{DD} = 3.00 V to 3.60 V (3.3-V I/O group)

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
External voltage tolerance	1.8-V I/O group 3*4	V_{TOL}	—	—	3.6	V	V_{DD} power-off & on
High-level input voltage	—	V_{IH}	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low-level input voltage	—	V_{IL}	−0.3	—	0.3 × V_{DD}	V	—
Hysteresis voltage	1.5-V I/O group*1	ΔV	0.1 × V_{DD}	—	—	V	—
	1.8-V I/O group 1*2 1.8-V I/O group 2*3	ΔV	0.1 × V_{DD}	—	—	V	
	1.8-V I/O group 3*4	ΔV	0.08 × V_{DD}	—	—	V	
	3.3/1.8-V switching I/O group 1*6	ΔV	0.08 × V_{DD}	—	—	V	
	3.3/1.8-V switching I/O group 2*7	ΔV	0.1	—	—	V	
	3.3-V I/O group*8	ΔV	0.08 × V_{DD}	—	—	V	
High-level input current (Non-tolerant input buffer)	1.5V I/O group*1	I_{IH}	—	—	12	μA	V_{in15} = V_{DD} max & V_{DD} power-on
	1.8-V I/O group 1*2 1.8-V I/O group 2*3 1.8-V I/O group 4*5	I_{IH}	—	—	12	μA	V_{in18} = V_{DD} max & V_{DD} power-on
	3.3/1.8-V switching I/O group 1*6 3.3/1.8-V switching I/O group 2*7	I_{IH}	—	—	12	μA	Vin_{33} = V_{DD} max & V_{DD} power-on
	3.3-V I/O group*8	I_{IH}	—	—	12	μA	
High-level input current (Tolerant input buffer)	1.8-V I/O group 3*4	I_{IH}	—	—	12	μA	V_{in18_tol} = V_{DD} max & V_{DD} power-on
High-level input current (Input buffer with pull-down resistor)	1.8-V I/O group 3*4 1.8-V I/O group 4*5	I_{IH}	—	—	200	μA	V_{in18} = V_{DD} max
	3.3/1.8-V switching I/O group 1*6	I_{IH}	—	—	200	μA	V_{in33} = V_{DD} max
	3.3/1.8-V switching I/O group 2*7	I_{IH}	—	—	150	μA	
	3.3-V I/O group*8	I_{IH}	—	—	200	μA	
Low-level input current (Non-tolerant input buffer)	1.5-V I/O group*1	I_{IL}	−12	—	—	μA	V_{in15} = V_{SS}
	1.8-V I/O group 1*2 1.8-V I/O group 2*3	I_{IL}	−12	—	—	μA	V_{in18} = V_{SS}
	1.8-V I/O group 4*5	I_{IL}	−12	—	—	μA	
	3.3/1.8-V switching I/O group 1*6	I_{IL}	−12	—	—	μA	V_{in33} = V_{SS}
	3.3/1.8-V switching I/O group 2*7	I_{IL}	−12	—	—	μA	
	3.3-V I/O group*8	I_{IL}	−12	—	—	μA	
Low-level input current (Tolerant input buffer)	1.8-V I/O group 3*4	I_{IL}	−12	—	—	μA	V_{in18_tol} = V_{SS}
Low-level input current (Input buffer with pull-down resistor)	1.8-V I/O group 2*3	I_{IL}	−180	—	—	μA	V_{in18} = V_{SS}
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	I_{IL}	−200	—	—	μA	
	3.3/1.8-V switching I/O group 1*6	I_{IL}	−200	—	—	μA	V_{in33} = V_{SS}
	3.3/1.8-V switching I/O group 2*7	I_{IL}	−190	—	—	μA	
	3.3-V I/O group*8	I_{IL}	−200	—	—	μA	

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
High-level output voltage	1.5-V I/O group*1	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.8 mA-
	1.8-V I/O group 1*2	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −3.8 mA
	1.8-V I/O group 2*3	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.8/−3.8/−7.8/−11 mA (drive strength X1/X2/X4/X6)
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.6/−3.2/−6.4/−9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.6/−3.2/−6.4/−9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −5/−6/−7/−10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	V_{OH}	0.8×V_{DD}	—	V_{DD}	V	I_{OH} = −9/−11/−13/−18 mA (drive strength X1/X2/X4/X6)
	3.3-V I/O group*8	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
Low-level output voltage	1.5-V I/O group*1	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.8 mA
	1.8-V I/O group 1*2	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 3.8 mA
	1.8-V I/O group 2*3	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.8/3.8/7.8/11 mA (drive strength X1/X2/X4/X6)
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.6/3.2/6.4/9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.6/3.2/6.4/9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 5/6/7/10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	V_{OL}	0	—	0.2×V_{DD}	V	I_{OL} = 9/11/13/18 mA (drive strength X1/X2/X4/X6)
	3.3-V I/O group*8	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
Pull-up resistance	1.8-V I/O group 2*3	R_{PU}	11	—	47	kΩ	—
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	R_{PU}	11	—	49	kΩ	—
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	R_{PU}	11	—	49	kΩ	—
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	R_{PU}	15	—	83	kΩ	—
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	R_{PU}	12	—	92	kΩ	—
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	R_{PU}	18	—	72	kΩ	—
	3.3-V I/O group*8	R_{PU}	15	—	83	kΩ	—

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Pull-down resistance	1.8-V I/O group 3*4 1.8V I/O group 4*5	R_{PD}	12	—	45	kΩ	—
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	R_{PD}	12	—	45	kΩ	—
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	R_{PD}	20	—	75	kΩ	—
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	R_{PD}	13	—	92	kΩ	—
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	R_{PD}	24	—	87	kΩ	—
	3.3-V I/O group*8	R_{PD}	20	—	75	kΩ	—
Input capacitance	—	C_{in}	—	—	10	pF	

Note 1. Target I/O group: 1.5-V PWC I/O

Note 2. Target I/O group: PWC I/O

Note 3. Target I/O group: PORT20 I/O, RSTN I/O, 1.8-V OSC

Note 4. Target I/O group: PORT02 I/O, PORT05 I/O

Note 5. Target I/O group: MD0-7 I/O, debugger I/O

Note 6. Target I/O group:
PORT01(A) I/O, PORT03 I/O, PORT01(B) I/O, PORT04 I/O, PORT07 I/O, PORT21 I/O, PORT06 I/O, PORT10 I/O, PORT11 I/O

Note 7. Target I/O group:
PORT00 I/O, PORT08 I/O, PORT09 I/O, PORT15 I/O, PORT16 I/O, PORT17 I/O

Note 8. Target I/O group:
PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O

3.5 AC Characteristics

AC characteristics measurement conditions

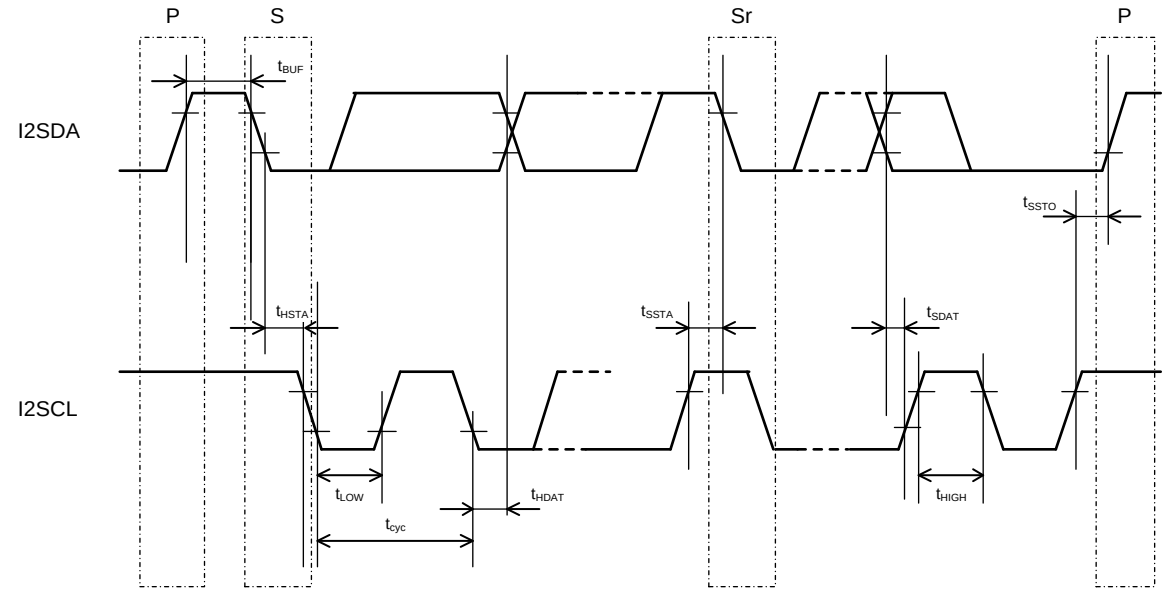
- I/O signal reference levels:
  $V_{DD18}/2$, $V_{DD33}/2$, $MMMODV_{DD}/2$, $PAMODC_{DD}/2$, $PBMODV_{DD}/2$, $PCMODV_{DD}/2$, $SD0MODV_{DD}/2$, $SD1FMODV_{DD}/2$, $U10MODV_{DD}/2$, $GEMODV_{DD}/2$, $U11MODV_{DD}/2$, V_{IH}, V_{OH} (min.), V_{IL}, V_{OL} (max.)
  (Refer to the corresponding timing charts.)
- Output load: C_L = 20 pF if not otherwise stated

3.5.1 IIC Bus Interface

Table 3.5-1 IIC Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
I2SCLn cycle time	t_{cyc}	2500	—	—	ns	
I2SCLn low level width	t_{LOW}	1300	—	—	ns	
I2SCLn high level width	t_{HIGH}	600	—	—	ns	
Bus free time (time from start to stop condition)	t_{BUF}	1300	—	—	ns	
Start condition hold time	t_{HSTA}	600	—	—	ns	
Restart condition setup time	t_{SSTA}	600	—	—	ns	
Stop condition setup time	t_{SSTO}	600	—	—	ns	
I2SDAn setup time	t_{SDAT}	100	—	—	ns	
I2SDAn hold time	t_{HDAT}	0	—	900	ns	

Note: n = 0 to 3



Note: S: START condition
P: STOP condition
Sr: Repeated START condition

Figure 3.5-1 IIC Timing

3.5.2 Clocked Serial Interface (CSI)

3.5.2.1 Master Mode

Table 3.5-2 Master Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
CSSCLKn cycle time	t_{cyc}	41.66	—	—	ns	
CSSCLKn output low level width	t_{LOW}	18	—	—	ns	Falling edge mode*1
CSSCLKn output high level width	t_{HIGH}	18	—	—	ns	Rising edge mode*1
CSRXDn setup time (CSSCLKn rising and falling edges)	t_{SRXD}	t_{LOW} − 9	—	—	ns	
CSRXDn hold time (CSSCLKn rising and falling edges)	t_{HRXD}	5.0	—	—	ns	
CSTXDn output delay time (CSSCLKn rising and falling edges)	t_{DTXD}	−5.0	—	7.5	ns	*1

Note: n = 0 to 5

Note 1. The 3-wire serial interface (CSI) should be used with a driving ability of at least X2.
Select one of the driving abilities listed below according to the load capacitance.
X2@C_L = 15 pF, X4@C_L = 20 pF

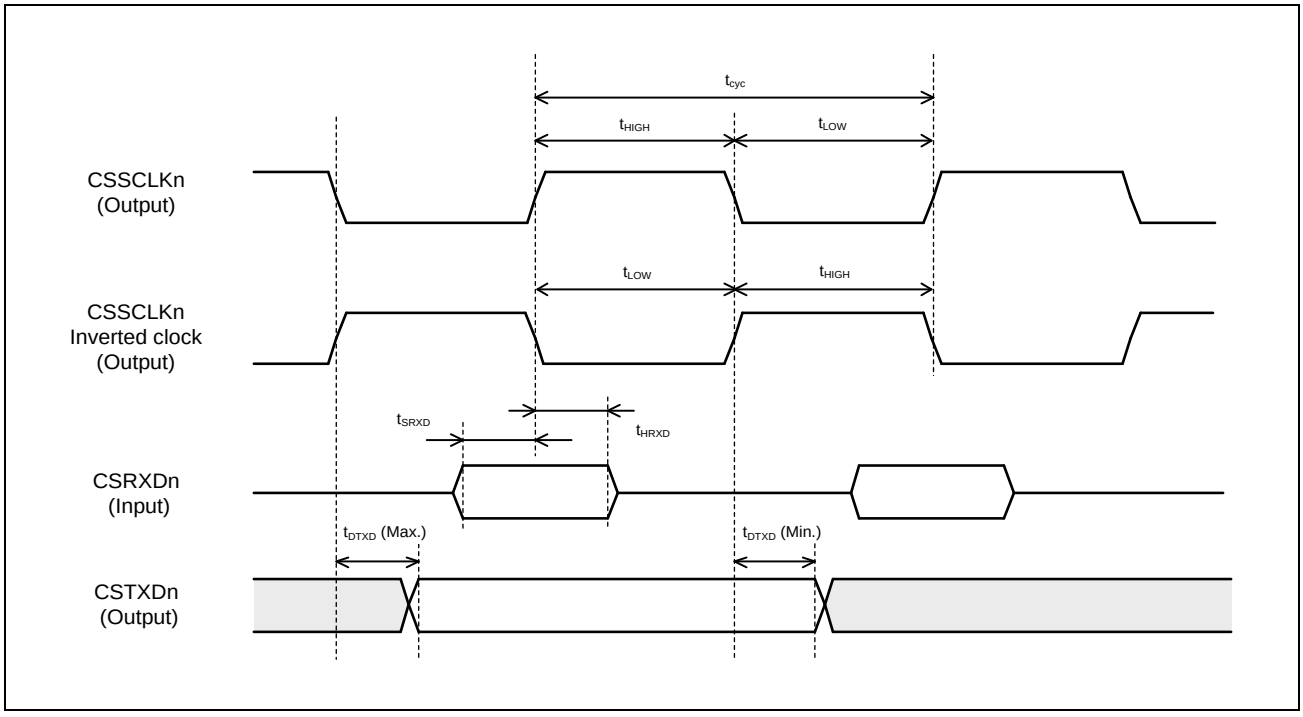


Figure 3.5-2 Master Mode Timing

3.5.2.2 Slave Mode

Table 3.5-3 Slave Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
CSSCLKn cycle time	t_{cyc}	41.66	—	—	ns	
CSSCLKn input low level width	t_{LOW}	18	—	—	ns	Falling edge mode
CSSCLKn input high level width	t_{HIGH}	18	—	—	ns	Rising edge mode
CSRXDn setup time (CSSCLKn rising and falling edges)	t_{SRXD}	7.5	—	—	ns	
CSRXDn hold time (CSSCLKn rising and falling edges)	t_{HRXD}	5.0	—	—	ns	
CSCSn setup time (CSSCLKn rising and falling edges)	t_{SCS}	84	—	—	ns	
CSCSn hold time (CSSCLKn rising and falling edges)	t_{HCS}	21	—	—	ns	
CSTXDn output delay time (CSSCLKn rising and falling edges)	t_{DTXD}	−5.0	—	10.5	ns	*1

Note: n=0 to 5

Note 1. The 3-wire serial interface (CSI) should be used with a driving ability of at least X2.
Select one of the driving abilities listed below according to the load capacitance.
X2@C_L = 15 pF, X4@C_L = 20 pF

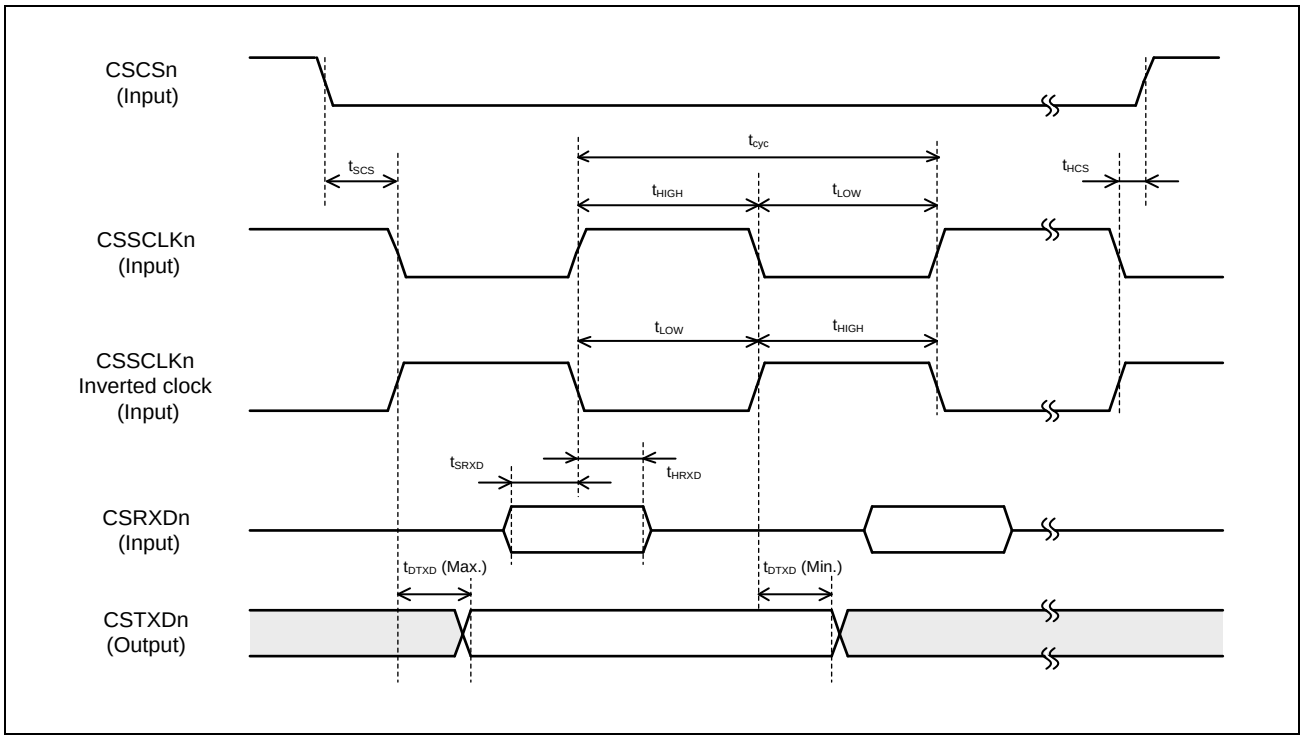


Figure 3.5-3 Slave Mode Timing

3.5.3 Ethernet MAC interface (ETHER)

3.5.3.1 100-Mbps Ethernet Mode

Table 3.5-4 100-Mbps Ethernet Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
GETXC cycle time	t_{Tcyc}	39.5	40	40.5	ns	
GETXEN output delay time	t_{DTXE}	0	—	25	ns	
GETXD output delay time	t_{DTXD}	0	—	25	ns	
GERXC cycle time	t_{Rcyc}	39.5	40	40.5	ns	
GERXDV setup time	t_{SRXV}	10	—	—	ns	
GERXDV hold time	t_{HRXV}	10	—	—	ns	
GERXD setup time	t_{SRXD}	10	—	—	ns	
GERXD hold time	t_{HRXD}	10	—	—	ns	
GERXER setup time	t_{SRER}	10	—	—	ns	
GERXER hold time	t_{HRER}	10	—	—	ns	

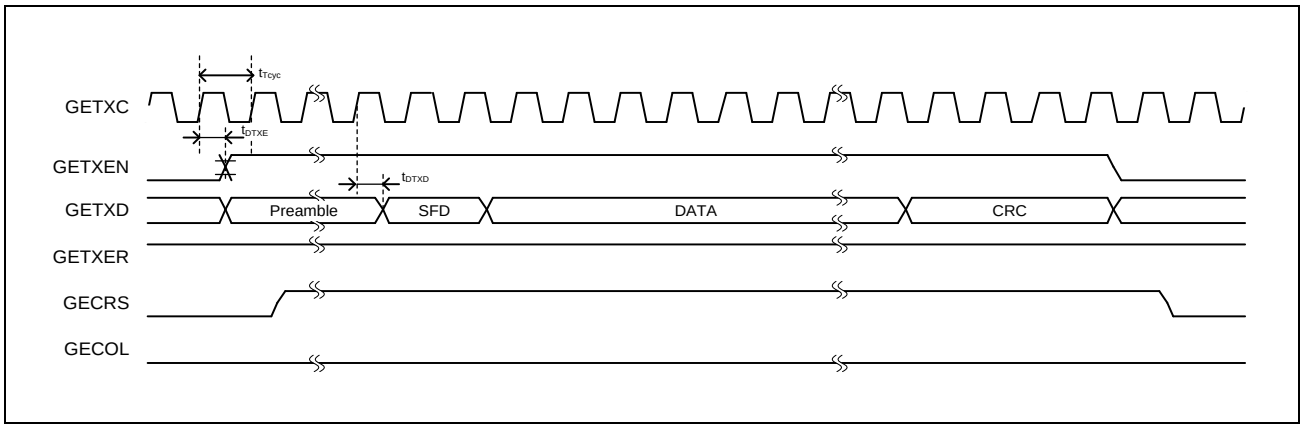


Figure 3.5-4 Transmission Timing

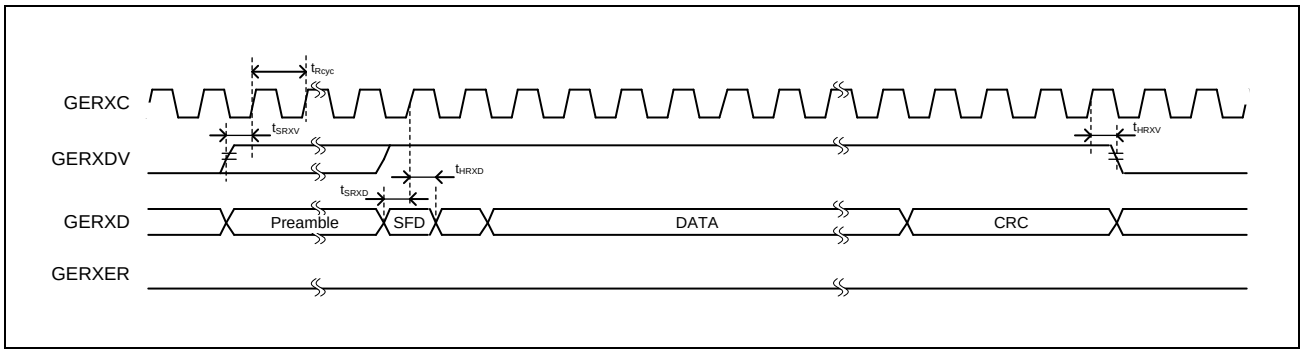


Figure 3.5-5 Reception Timing (Normal)

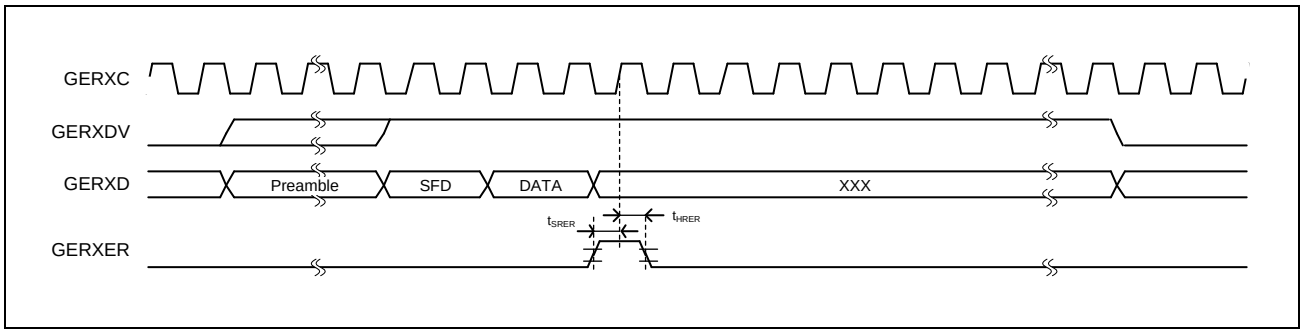


Figure 3.5-6 Reception Timing (in Cases of Error)

3.5.3.2 1-Gbps Ethernet Mode

Table 3.5-5 1-Gbps Ethernet Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
GECLK input frequency	$f_{REF125CK}$	125 − 100 ppm	—	125 + 100 ppm	MHz	
GECLK input duty ratio	I_{DUTY}	45	50	55	%	
GEGTXCLK cycle time	t_{GTcyc}	7.5	8	8.5	ns	
GETXEN output delay time	t_{DGTXE}	0.5	—	5.5	ns	
GETXD output delay time	t_{DGTXD}	0.5	—	5.5	ns	
GERXC cycle time	t_{GRcyc}	7.5	8	8.5	ns	
GERXDV setup time	t_{SGRXV}	2.5	—	—	ns	
GERCDV hold time	t_{HGRXV}	0.5	—	—	ns	
GERXD setup time	t_{SGRXD}	2.5	—	—	ns	
GERXD hold time	t_{HGRXD}	0.5	—	—	ns	
GERXER setup time	t_{SGRER}	2.5	—	—	ns	
GERXER hold time	t_{HGRER}	0.5	—	—	ns	

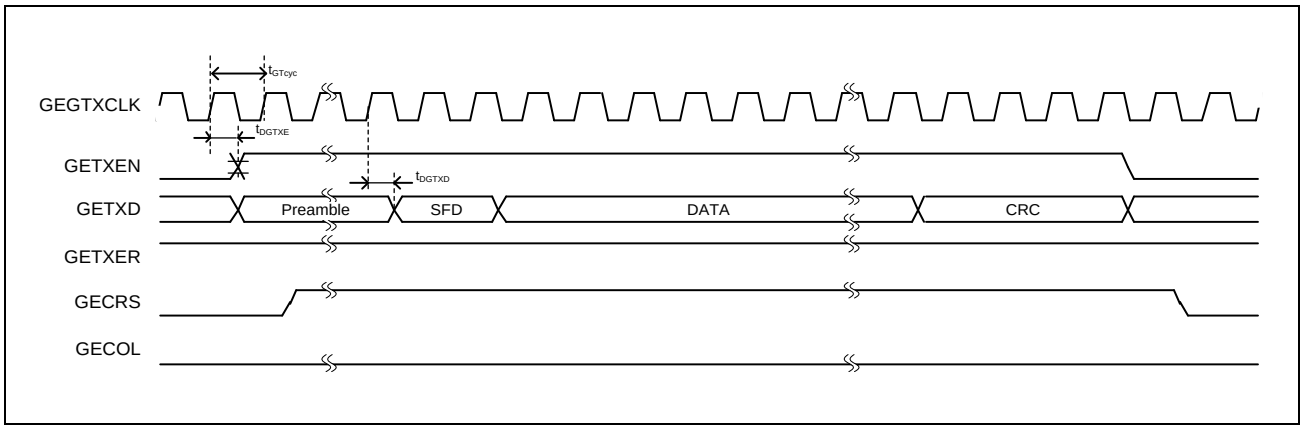


Figure 3.5-7 Transmission Timing

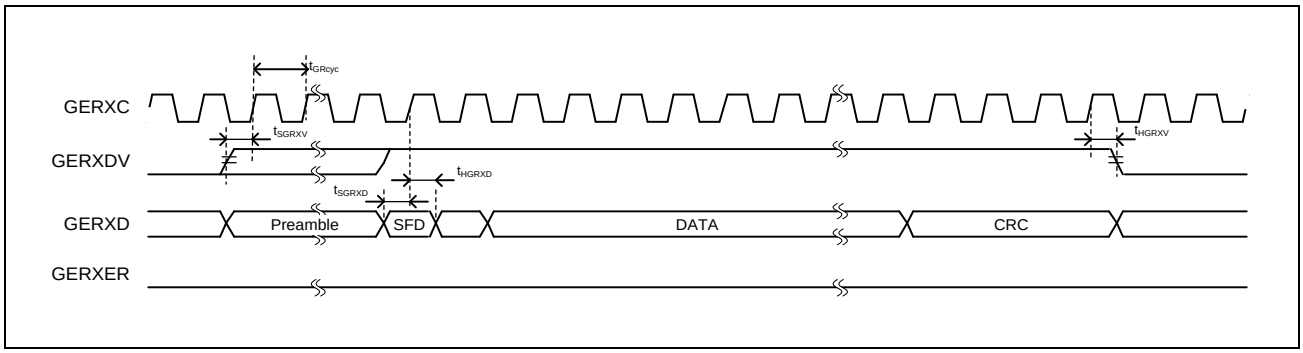


Figure 3.5-8 Reception Timing (Normal)

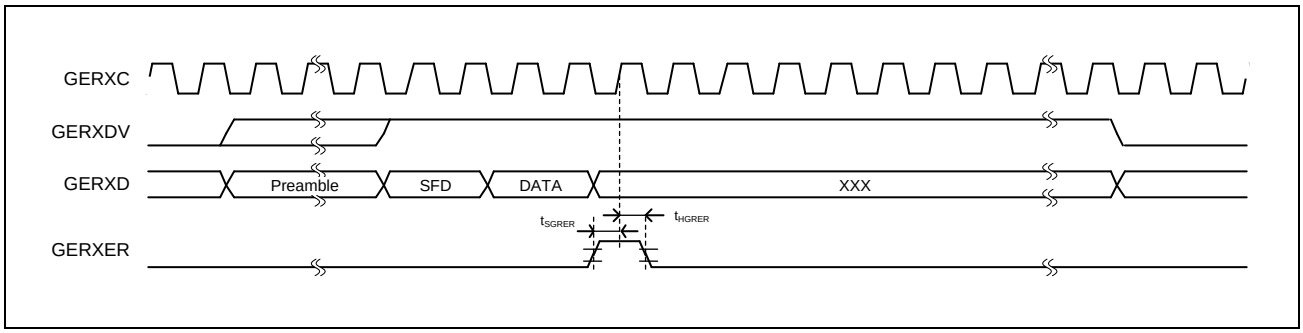


Figure 3.5-9 Reception Timing (in Cases of Error)

3.5.4 SD Host Interface (SDI)

This LSI includes *the SD host interfaces that are compliant with the SD specification version 3.01*.

3.5.5 eMMC Interface (eMMC)

The eMMC interface should be used with a driving ability of at least X2.

Table 3.5-6 HS200 Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	5	—	10	ns	C_L = 15 pF V_{OH} = 0.65 × V_{DD}(MMMODV$_{DD}$) V_{OL} = 0.35 × V_{DD}(MMMODV$_{DD}$)
MMCLK output low level width	t_{LOW}	1.5	—	—	ns	
MMCLK output high level width	t_{HIGH}	1.5	—	—	ns	
MMCLK rise time	t_r	—	—	1	ns	
MMCLK fall time	t_f	—	—	1	ns	
MMCMD/ MMDAT output delay time	t_{DDAT}	−1.5	—	0.9	ns	
MMCMD/ MMDAT setup time*1	t_{SDAT}	—	—	—	ns	
MMCMD/ MMDAT hold time*1	t_{HDAT}	—	—	—	ns	
MMCMD/ MMDAT data width*1	t_{WDAT}	2.88	—	—	ns	

Note 1. In HS200 mode, the sampling clock controller (SCC) must be used for tuning.

Table 3.5-7 High Speed Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	20	—	—	ns	C_L = 30 pF 1.8-V operation: V_{OH} = 0.65 × V_{DD}(MMMODV$_{DD}$) V_{OL} = 0.35 × V_{DD}(MMMODV$_{DD}$) 3.3-V operation: V_{OH} = 0.625 × V_{DD}(MMMODV$_{DD}$) V_{OL} = 0.25 × V_{DD}(MMMODV$_{DD}$)
MMCLK output low level width	t_{LOW}	6.5	—	—	ns	
MMCLK output high level width	t_{HIGH}	6.5	—	—	ns	
MMCLK rise time	t_r	—	—	3	ns	
MMCLK fall time	t_f	—	—	3	ns	
MMCMD/ MMDAT output delay time	t_{DDAT}	−6.5	—	2.5	ns	
MMCMD/ MMDAT setup time	t_{SDAT}	4.0	—	—	ns	
MMCMD/ MMDAT hold time	t_{HDAT}	2.0	—	—	ns	

Table 3.5-8 Backward Compatible Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	40	—	—	ns	C_L = 30 pF 1.8-V operation: V_{OH} = 0.65 × V_{DD}(MMMODV$_{DD}$) V_{OL} = 0.35 × V_{DD}(MMMODV$_{DD}$) 3.3-V operation: V_{OH} = 0.625 × V_{DD}(MMMODV$_{DD}$) V_{OL} = 0.25 × V_{DD}(MMMODV$_{DD}$)
MMCLK output low level width	t_{LOW}	10	—	—	ns	
MMCLK output high level width	t_{HIGH}	10	—	—	ns	
MMCLK rise time	t_r	—	—	10	ns	
MMCLK fall time	t_f	—	—	10	ns	
MMCMD/ MMDAT output delay time	t_{DDAT}	−7.5	—	2.5	ns	
MMCMD/ MMDAT setup time	t_{SDAT}	4.0	—	—	ns	
MMCMD/ MMDAT hold time	t_{HDAT}	2.0	—	—	ns	

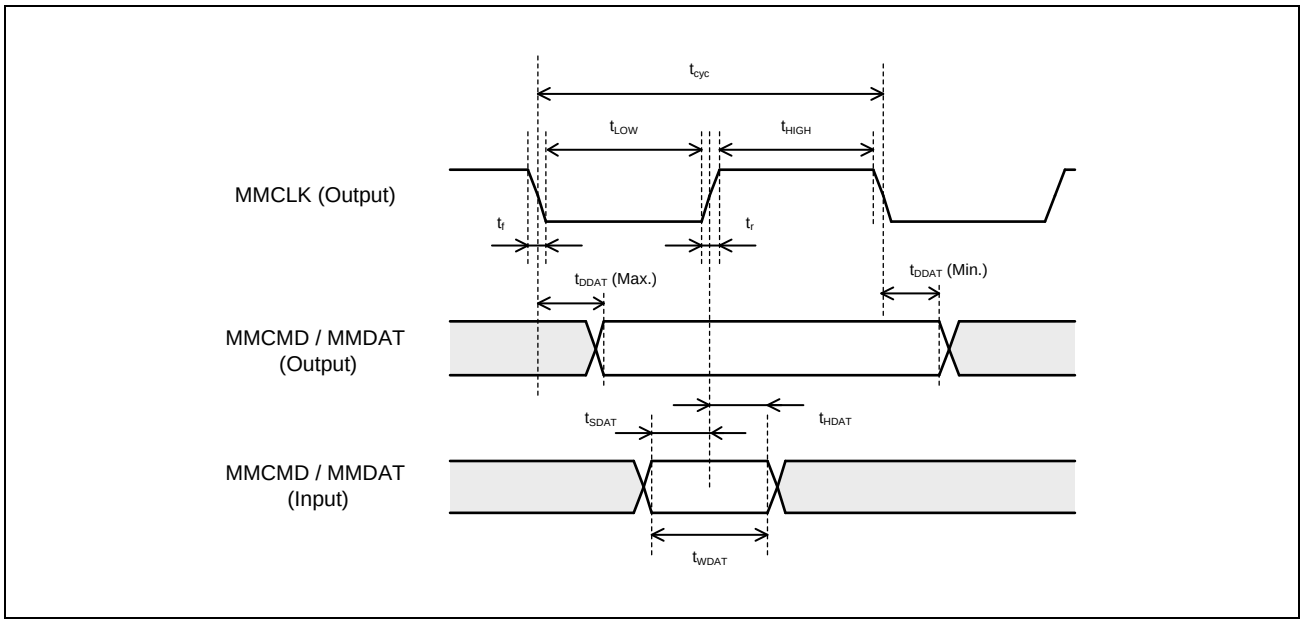


Figure 3.5-10 eMMC Timing

3.5.6 TRACE Interface (TRACE)

Table 3.5-9 TRACE Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
TRCLK cycle time	t_{cyc}	20	—	—	ns	
TRCLK output low level width	t_{LOW}	9	—	—	ns	
TRCLK output high level width	t_{HIGH}	9	—	—	ns	
TRCTL/ TRDATA output delay time (TRCLK rising edge)	t_{DRDAT}	2	—	7	ns	
TRCTL/ TRDATA output delay time (TRCLK falling edge)	t_{DFDAT}	2	—	7	ns	

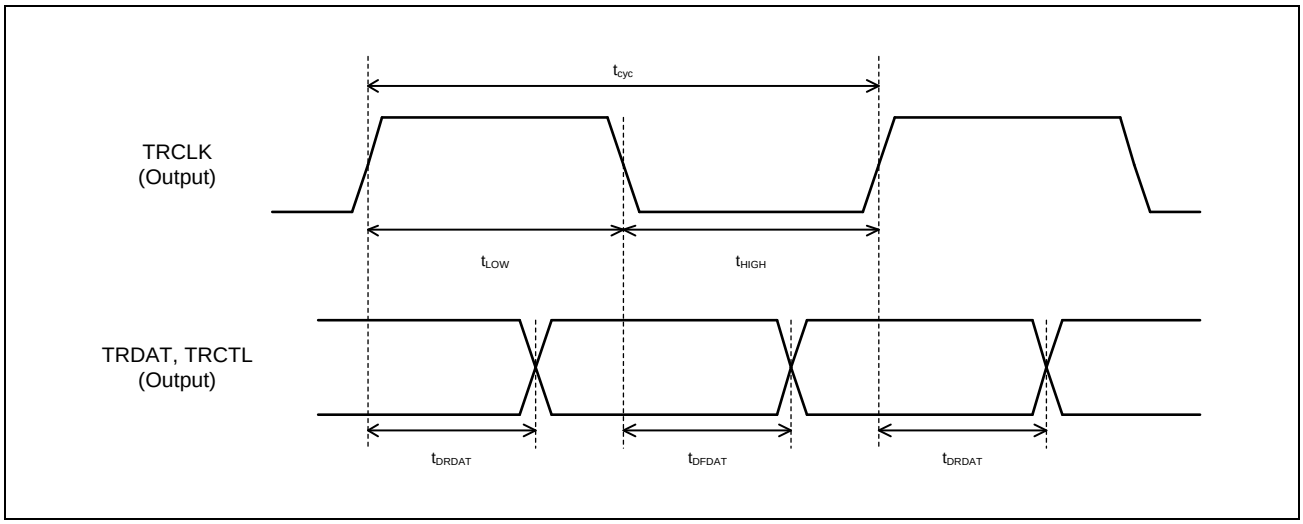


Figure 3.5-11 TRACE Interface Timing

3.6 Various Analog Characteristics

3.6.1 LPDDR4 PHY Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4A standard.

3.6.2 USB PHY Characteristics

The USB PHY of this LSI is compliant with the following USB 3.1 GEN1 standard:

Universal Serial Bus 3.1 Specification

3.6.3 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of *the PCI Express® Base Specification* for Gen1/Gen 2

3.6.4 Temperature Sensor Characteristics

Table 3.6-1 Temperature Sensor Characteristics

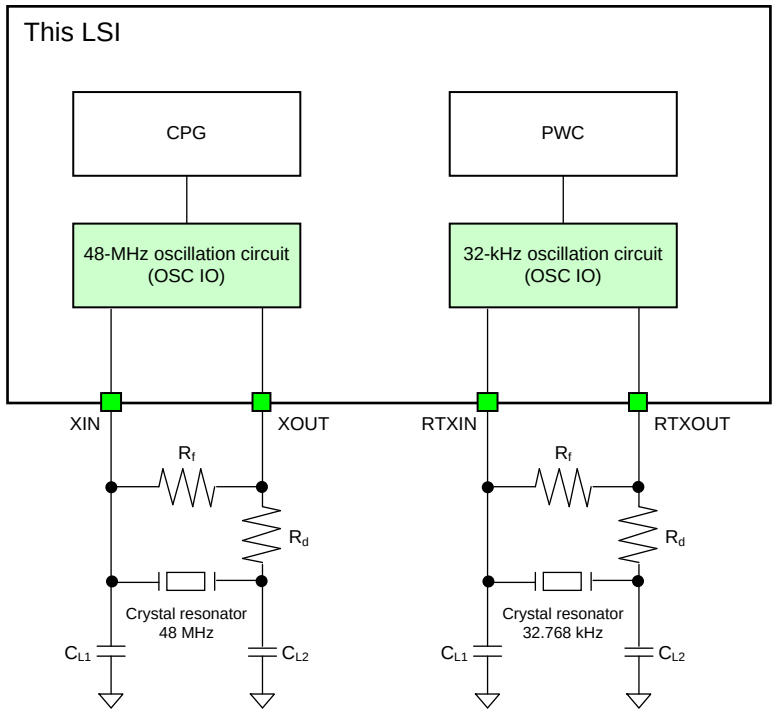
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Accuracy from 70°C to 125°C	Acc70_125	—	±2.0	±3.0	°C	
Accuracy from −40°C to 70°C	Accm40_70	—	±3.0	±5.0	°C	

3.7 Oscillation Circuits for Connecting Crystal Resonators (OSC)

This LSI chip includes two oscillation circuits (OSC) for connection to crystal resonators, specifically a 48-MHz crystal resonator for the system clock and a 32.768-kHz crystal resonator for the real-time clock. **Table 3.7-1** lists the pins for connecting the crystal resonators and the clock frequencies. **Figure 3.7-1** shows an example of the connections with crystal resonators.

Table 3.7-1 Pins for Connecting Crystal Resonators and Clock Frequency

External Pin Name	I/O	Clock Frequency
For the system clock		
XIN	Input	48 MHz (frequency deviation: ±50 ppm, frequency temperature characteristic: ±30 ppm)
XOUT	Output	48 MHz
For the power sequence clock		
RTXIN	Input	32.768 kHz (frequency deviation: ±20 ppm)
RTXOUT	Output	32.768 kHz



Note: R_f: Feedback resistor
R_d: Dumping resistor
C_{load} (load capacitance of the crystal): See below for the formula.

$$C_{load} = \{C_{L1} \times C_{L2} / (C_{L1} + C_{L2})\} + \text{PCB's floating capacitance}$$

Figure 3.7-1 Example of Connections with Crystal Resonators

Place the crystal resonators and the capacitors C_{L1} and C_{L2} as close as possible to the pins to connect crystal resonators. To avoid interference and to ensure correct oscillation, the grounding points of the capacitors appended to the crystal resonators should be shared, and no wiring patterns should be placed near these components.

The characteristics of the crystal resonators are closely related to the design of the user board. Therefore, the user should sufficiently evaluate them with reference to the example of connection of crystal resonators in **Figure 3.7-1**.

The circuit rating of a crystal resonator depends on the crystal resonator and the stray capacitance of the mounting circuit. Therefore, contact the manufacturer of the crystal resonator before deciding upon the circuit rating. The user should thoroughly evaluate and then set the parameters (resistor and capacitor values).

Table 3.7-2 is a list of recommended values for the crystal resonators.

Table 3.7-2 Recommended Model Values for the Crystal Resonators

	Model Values for the Crystal Resonators			
Clock Frequency	Max. ESR*1	Max. C_L*2	Max. C_0*3	Max. Drive Level
32.768 kHz	70 kΩ	12.5 pF	1.4 pF	1 µW
48 MHz	50 Ω	10 pF	7 pF	100 µW

Note 1. ESR means the equivalent series resistor of the crystal resonator.

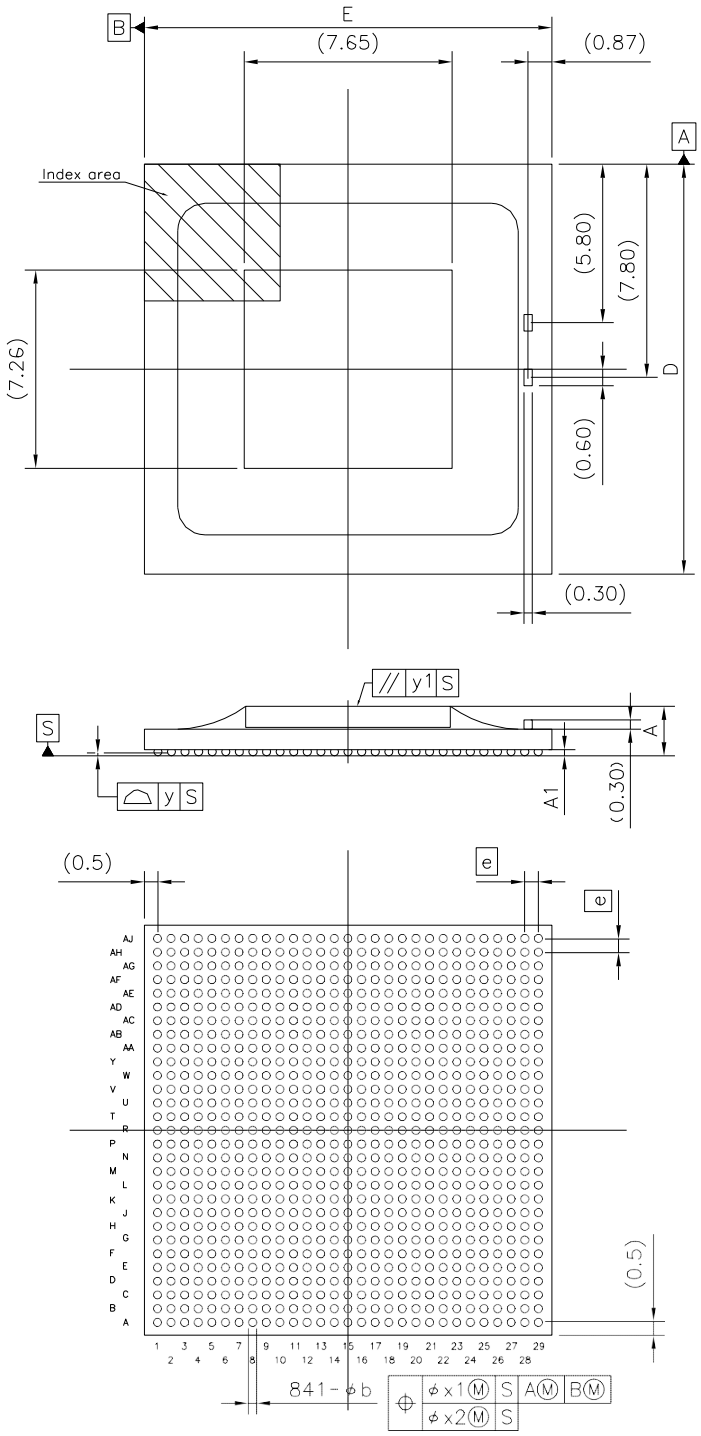
Note 2. C_L is the load capacitance of the crystal resonator.

Note 3. C_0 is the parallel capacitance of the crystal resonator.

Section 4 Package Dimensions

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA841-15x15-0.50	PRBG0841KA-A	–	0.71

Unit:mm



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.85	15.00	15.15
E	14.85	15.00	15.15
e	–	0.50	–
A	(1.70)	(1.90)	2.10
A1	0.15	(0.25)	–
b	0.25	0.30	0.35
x1	–	–	0.20
x2	–	–	0.05
y	–	–	0.12
y1	–	–	0.20

Figure 4.1 Package Dimensions

REVISION HISTORY	RZ/V Series, VisionAI_ASSP RZ/V2MA Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Jul 24, 2024	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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