RZ/G3L Group, RZ/G3SE Group

RZ Family, RZ/G Series

R01DS0469EJ0110
Rev.1.10
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Features

This LSI includes:

■ CPU

- On-chip Quad 64-bit Arm® Cortex®-A55 Core processors [option]

  Application processing (up to 1.2 GHz)
- 32-bit Arm® Cortex®-M33 processor

  System management (up to 200 MHz)

■ Boot

- Selectable boot CPU from Arm® Cortex®-M33 or Arm® Cortex®-A55

■ Video and Graphics

- H.264 Video codec processor [option]
- 3D Graphics Engine of Arm® Mali™-G31 [option]
- Image Scaling Unit 2

■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (512-Kbyte on-chip SRAM with ECC)
- External DDR memory interface

  1-channel memory controller for DDR4-2133 or LPDDR4-2133 with a 16-bit bus width
- xSPI interface
- SDHI (eMMC/SD (1-, 4-, 8-bit bus width) supported)
- External Bus state controller with 16bit for SRAM

■ Camera and display interfaces

- MIPI CSI-2 (1 ch.: 1 or 2 lanes)
- Selectable 1 display interfaces from the following

  MIPI DSI (1 ch.: 1, 2, or 4 lanes)

  Parallel interface (1 ch.)

  LVDS (1 ch.)

■ Various communication/storage/network interfaces

- Ethernet (2 ch.: 10/100/1000 BASE) with TSN
- USB2.0 (2 ch.: Host/Function)
- PCIe Gen2 (1 ch : 1 lane, Root Complex only)
- CANFD (compliant with ISO11898-1) (3 ch.)
- RSCI (4 ch : UART/SPI/I2C-host)
- SCIF (6 ch)
- RSPI (3 ch.)
- RIIC (4 ch.)
- I3C (1 ch.)

■ Extended-function timers

- General-purpose PWM timer (8 ch : 32-bit)
- Multi-Function Timer Pulse Unit (8 ch : 16-bit, 1 ch : 32-bit)

■ Audio

- Serial sound interface (full-duplex 4 ch)
- SPDIF input/output interfaces (1 ch.)
- Pulse density modulation (PDM) input interfaces (3 ch.)

■ Analog/Digital converter (ADC) and sensors

- 1.0 Msps 12-bit ADC (8 ch.)
- Internal temperature sensors (1 ch.)

■ Security

- Hardware cryptographic engine

NOTE

- Products with #AC0 or #BC0 in the part number have limitations in the MIPI DSI feature.
- For details, please contact a Renesas Electronics sales representative.

1. Overview

1.1 Outline of Specification

1.1.1 CPU

Item	Description
Application Processor Cortex-A55 (CA55) [option]	• Arm Cortex-A55 Quad Core 1.2 GHz • L1 I-cache 32 Kbytes (with parity) and D-cache 32 Kbytes (with ECC) per core • L2 cache: 0 Kbyte • L3 cache: 512 Kbyte (with ECC) • MMU supported • Neon™ and FPU supported • Cryptographic extension supported • Armv8-A architecture
System Manager Cortex-M33 (CM33)	• Arm Cortex-M33 Processor 200 MHz • Security Extension supported • Armv8-M architecture
Debug Interface	• Arm® CoreSight® architecture • JTAG and SWD interfaces supported • ETF: Total of 32 Kbytes for program flow tracing • JTAG disabling supported [option]

1.1.2 Boot

Item	Description
Boot	• Selectable boot from Arm Cortex-A55 or Arm Cortex-M33 • CA55 boot – Boot Mode 0: Booting from eSD 3.3 V – Boot Mode 1: Booting from eMMC 3.3 V – Boot Mode 2: Booting from a serial flash memory connected to the xSPI bus space 3.3 V – Boot Mode 3: Booting from SCIF download – Boot Mode 5: Booting from eMMC 1.8 V – Boot Mode 6: Booting from a serial flash memory connected to the xSPI bus space 1.8 V • CM33 boot – Boot Mode 2: Booting from a serial flash memory connected to the xSPI bus space 3.3 V – Boot Mode 3: Booting from SCIF download – Boot Mode 6: Booting from a serial flash memory connected to the xSPI bus space 1.8 V

1.1.3 Graphics Unit

Item	Description
3D Graphics Engine (GE3D) [option]	• Arm Mali-G31 600 MHz • One single-pixel shader core • 8 Kbytes L2 cache • Vulkan 1.2 • OpenGL ES™ 1.1, 2.0 and 3.2 • OpenCL 2.0 full profile

1.1.4 Video Processing Unit

Item	Description
Video Codec Processor (VCP) [option]	• H.264 codec module • Support for encoding and decoding – H.264 / AVC (High Profile / Main Profile / Baseline Profile) – H.264 / MVC (Stereo High Profile • Maximum pixel rate: 1920 × 1080 × 30 fps • Input image Size (max): 1920 × 1080 • Output image Size (max): 1920 × 1080 • Color format (input in encoding): YcbCr 4:2:0 8-bits, 2-planar supported – Color format (output in decoding): YcbCr 4:2:0, semi-planar supported
Image Scaling Unit2 (ISU2)	• Scaling up and down function with bilinear interpolation • Input image size(max): 2048 × 2048 • Output image size(max): 2048 × 2048 • Support color format conversion (YCbCr422, YCbCr420, RGB, ARGB / RAW(Grayscale))

1.1.5 Internal Memory

Item	Description
System RAM	• 512 Kbytes (with ECC)

1.1.6 External Memory Interface

Item	Description
External Bus Controller for DDR4/LPDDR4 SDRAM (DDR)	• 1 channel • Support DDR4-2133 – Bus Width: 16-bit – Memory Size: Up to 4 Gbytes, Single rank • Support LPDDR4-2133 – Bus Width: 16-bit – Memory Size: Up to 2 Gbytes, Single rank • In line ECC supported (support for error detection interrupts) • Auto Refresh/Self Refresh/IO Retention supported • Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported)
xSPI Controller (xSPI)	• 1 channel (2 chip select signals) • Compliant with the xSPI protocol • Protocol mode —1, 4 or 8 pins with SDR or DDR (1S-1S-1S, 4S-4D-4D, 8D-8D-8D) —2 or 4 pins with SDR (1S-4S-4S, 4S-4S-4S) • Support for XiP mode • Support for up to 256-Mbyte address space (support for up to 128 Mbytes per channel address space in boot sequence)
SD Card Host Interface/ Multimedia Card Interface (SD/MMC)	• 3 channels —Channel 0 supports SDHI/e-MMC (boot supported) —Channel 1 supports SDHI/e-MMC —Channel 2 supports SDHI • SD memory I/O card interface (1-bit/4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD 3.0 • Default, high-speed, UHS-I/SDR50, SDR104 and DDR50 transfer modes supported • Error check function: CRC7 (Command), CRC16 (Data) • Support for card detection and write protection • MMC interface —Channel 0 (1-bit/4-bit/8-bit MMC bus) —Channel 1 (1-bit/4-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 5.1(No Command Queue supported) • High-speed, HS400 transfer modes supported (Channel 0) • High-speed, HS200 transfer modes supported (Channel 0 and 1)
External Bus state controller with 16-bits for SRAM (EBSC)	• 1 channel • Support SRAM interface • Bus width: 8- or 16-bits • Support up to 2Mbytes address space

1.1.7 CPU Peripheral

Item	Description
Clock Pulse Generator (CPG)	• Generates the clocks from an external clock or external resonator (24 MHz). – Maximum Arm Cortex-A55 clock: 1.2 GHz – Maximum Arm Cortex-M33 clock: 200 MHz – Maximum DDR clock: 1066 MHz (DDR4-2133 / LPDDR4-2133) – Maximum 3DGE clock: 600 MHz – Maximum Video Codec processor clock: 200 MHz – Maximum System Bus clock: 200 MHz • SSC (Spread Spectrum Clock) supported
Direct Memory Access Controller (DMAC)	• 32 channels • Transfer modes: Single transfer mode and block transfer mode • LINK mode (DMA transfer under descriptor control) supported • Transfer size: 1, 2, 4, 8, 16, 32, 64, or 128 bytes • Transfer request: Software trigger, external DMA requests (DREQ) and interrupt requests from peripheral functions • A specific DMA transfer interval can be specified to adjust the bus occupancy.
Interrupt Controller	• Arm® CoreLink™ Generic Interrupt Controller (GIC-600) for Arm Cortex-A55 (32 priority levels available) • Nested Vectored Interrupt Controller (NVIC) for Arm Cortex-M33 • External Interrupt pins (NMI, IRQ0 to IRQ15, and TINT0 to TINT31) • On-chip peripheral Interrupts: priority level set for each module
Message Handling Unit (MHU)	• Message handling function between Arm Cortex-A55 and Arm Cortex-M33 • Assert interrupt to inform message and response from/to every core
General-purpose I/O (PFC)	• 113 General-purpose I/O ports

1.1.8 Camera Interface

Item	Description
MIPI CSI-2 Interface with camera image processing (CRU)	• Number of lanes: 1 or 2 lanes • MIPI CSI-2 v2.1 compliant • Maximum bandwidth: 1.5 Gbps per lane • Support for the throughput up to 2000 x 1200 RAW12 60 fps • Support for 4 virtual channels selected from VC0 to VC15 • Support for input data formats: – YUV422 8 bits or 10 bits – RGB444, RGB555, RGB565, RGB666, RGB888 – RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20 – YUV420 8-bits or 10-bits (image processing not supported) – Legacy YUV420 8-bits (image processing not supported) – YUV420 8-bits or 10-bits (chroma shifted pixel sampling) (image processing not supported) – User defined byte-based data • The other formats from the MIPI CSI-2 interface can also be output without image processing. • Generic long packet data types 1 to 4 • User defined 8-bit data types 1 to 8

1.1.9 Display Interfaces

Item	Description
LCD Controller (LCDC)	• 1 channel • 2 planes blending (can blend 2 different size images) • Support Image Processing: – Dither processing (RGB666) – Clipping – RGB Gamma Correction LUT • Support Input Data Format: – RGB565 / RGB666 / RGB888 – ARGB1555 / ARGB4444 / ARGB8888 – YCbCr444 8-bit / YCbCr422 8-bit / YCbCr420 8-bit • Selectable 1 display interfaces from the following – 1 channel MIPI DSI (1/2/4-Lane) interface – 1 parallel interface – 1 LVDS interface • Support 1920 pixels × 1920 lines Pixel clock must be within the following range – MIPI DSI = 5.4 to 187.5 MHz – Parallel = 5.4 to 87 MHz – LVDS (single) = 25 to 87 MHz
MIPI DSI Interface (DSI)	• 1 channel • The number of Lanes: 1,2 or 4-lane • Support 1920 × 1200, 60 fps (RGB888) • Maximum Bandwidth: 1.5 Gbps per lane • Support Output Data Format: RGB666 / RGB888
Parallel Output Interface	• 1 channel • Support WXGA (1280×800), 60 fps • Support Output Data Format: RGB666 / RGB888 • CLK/HD/VD timing signal supported
LVDS Interface (LVDS)	• 1 channel • Number of support lanes – Single-link: 4 lanes (Data) + 1 lane (Clock) • Single-link target – RGB888 640×480 (VGA) – RGB888 800×480 (QVGA) – RGB888 1366×768 60 Hz (WXGA) – RGB888 1280×800 60 Hz (WXGA) • Output clock range: 25 to 87 MHz • Clock Duty: 4:3 • Color: 8 bits or 6 bits • ViD: 250 to 450 mV • Vcm (Vos): 1.125 to 1.375 V • SSC supported (The SSCG function and delta-sigma modulator cannot be enable at the same time) – Spread Spectrum Modulation Frequency: 30 to 30 kHz – Center Spread: ±0.5, ±1.0, ±1.5 [%] – Down Spread: −1.0, −2.0, −3.0 [%]

1.1.10 Storage and Network

Item	Description
USB2.0 Host/Function (USB2)	• 2 channels • Compliance with USB2.0 • Support for On-The-Go (OTG) functionality • Supports Control/Bulk/Interrupt/Isochronous transfer • Internal dedicated DMA
PCI Express 2.0 (PCIE)	• 1 channel • PCIe Gen2 • 1-lane • Supported Root complex only
Gigabit Ethernet Interface (GBETH)	• 2 channels • Compliant with IEEE802.3 • Compliant with IEEE802.1Qav, IEEE802.1Qat, IEEE802.1AS, IEEE802.1Qbv • Compliant with IEEE1588-2008 with nano second timer in ch. 0 (master) and ch. 1 (slave) • Supports 10BASE, 100BASE, 1000BASE • Supports full duplex and half duplex • Supports RGMII / RMII Interfaces
CANFD Interface (CANFD)	• 3 channels • ISO 11898-1 (2003) compliant • CAN-FD ISO 11898-1 (CD2014) compliant • Support 1Mbps for arbitration phase and up to 8Mbps for data phase • Message buffer – 32 transmit message buffers per channel – 192 shared buffers for RXMB and FIFO buffers per channel

1.1.11 Peripheral Module

Item	Description
I3C Bus Interface (I3C)	• 1 channel • Master (Main Master/Secondary Master) mode and Slave mode selectable • SDR (I3C Single Data Rate) Mode – Private Message – Broadcast Message (Common Command Code) – Direct Message (Common Command Code) • Legacy I2C Message – Fast-mode (Fm): 0 to 400 kbit/s – Fast-mode Plus (Fm+): 0 to 1 Mbit/s • Slave Interrupt Request • Master Ship Request (Secondary Master only) • Support for 7-bits slave address formats • Synchronous Timing Control – Sync Mode: Synchronous Basic Mode • Asynchronous Timing Control – Async Mode 0: Asynchronous Basic Mode – Async Mode 1: Asynchronous Advanced Mode • Error Detection
I2C Bus Interface (RIIC)	• 4 channels • Master or Slave mode selectable • Support for the multi-master • Support for Standard mode (100 kHz), Fast mode (400 kHz), and Fast mode+ (1 MHz) • Support for DMAC
Renesas Serial Communication Interface (RSCI)	• 4 channels • 6 communication mode – Asynchronous interfaces – 8-bit clock synchronous interface – Simple IIC (host-only) – Simple SPI (with one chip select signal) – Smart card interface – Simple LIN (expanded SCIX mode) • 32-stage FIFO registers for transmission and reception • Clock sources is select from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and Half-duplex communication • Data length: 7 to 9 bits • Bit rate modulation • Double speed mode • Loopback function to enable self-diagnosis • Support for DMAC • Support for CRC calculation by the CRC unit

Item	Description
Renesas Serial Peripheral Interface (RSPI)	• 3 channels • SPI transfer facility – Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (SPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) – Capable of handling serial transfer as a master or slave • Data formats – Switching between MSB first and LSB first – The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. – 32 bits × 16 stage buffers for transmission and reception – Up to for frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure – 16 stages/channels for MOSI and MISO independently – Double buffers for both transmission and reception • RSPCK can be stopped automatically with the reception buffer full for master reception • Support for DMAC • Support CRC calculation by the CRC unit
Serial Communication Interface with FIFO (SCIF)	• 6 channels • Clock synchronous mode or asynchronous mode selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud-rate generator • Separate 16-byte FIFO registers for transmission and reception • Modem control function (channel 0, 1 and 2 in asynchronous mode)

1.1.12 Timer

Item	Description
Multi-function Timer Pulse Unit 3 (MTU3a)	• 9 channels (16-bits x 8 channels, 32-bits x 1 channels) • Module clock frequency (P1φ): 100 MHz • Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs • 14 types of count clocks selectable • Input capture function • 39 outputs compare and input capture registers • Counter clear operation (Simultaneous counter clearing by Compare match or Input capture is available) • Simultaneous writing to multiple timer counters (TCNT) • Synchronous input/output of each register due to synchronous operation of the counter • Buffered operation • Cascade-connected operation • 43 types of interrupt sources • Automatic transfer of register data • Pulse output modes • Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Phase counting mode • 16-bits mode (channel 1 and 2) • 32-bits mode (channel 1 and 2) • Counter function of dead time compensation • Digital filter functions for the input capture and external count clock pin
Port Output Enable 3 (POE3)	• Control of the high-impedance state of the MTU3a waveform output pins • Activation with four input pins • Activation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Activation by register write • Additional programming of output control target pins is possible.
General PWM Timer (GPT)	• 32 bits × 8 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Synchronous start / stop / clear of counters on arbitrary channels • Starting, stopping, and clearing up/down counters in response to a maximum of eight events • Starting, stopping, and clearing up/down counters in response to input level comparison • Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers • Output pin invalidation functions due to dead time error or detection of short circuit between output pins • Digital filter functions for the input capture and external trigger pins
Port Output Enable for GPT (POEG)	• Output prohibition control of the GPT waveform output pin • Activation with up to four input pins • Activation by dead time error detection or output short detection • Activation by register write

Item	Description
Watchdog Timer (WDT)	• 3 channels • A counter overflow can reset the LSI • CPU parity error can reset the LSI
General Timer (GTM)	• 32 bits × 3 channels • Two operating modes: – Interval timer mode – Free-running comparison mode
Real Time Clock (RTC)	• A 100-year calendar from 2000 to 2099 • BCD code display • Clock source is an oscillator dedicated to RTC (32.768 kHz) • Automatic adjustment function for leap years • Alarm function

1.1.13 Audio Interface

Item	Description
Serial Sound Interface (SSIF)	• 4 channels bidirectional serial transfer • 2 external clock sources available • Full Duplex communication • Support of I2S / Monaural / TDM audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8-, 16-, 18-, 20-, 22-, 24-, and 32-bits data formats • Support of 32-stage FIFO for transmission and reception • Support of LR-clock continue function in which the LR-clock signal is not stopped
SPDIF Interface (SPDIF)	• 1 channel • Support of IEC60958 standard (stereo and consumer use modes only) • Sampling Rate: 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Biphase mark encoding • Double buffered data • Parity encoded serial data • Simultaneous transmit and receive • Receiver autodetects IEC 61937 compressed mode data
Pulse Density Modulation (PDM)	• 3 channels • Direction: input • Sampling Rate: 8, 10, 12, 15, 16, 20, 24, 25, 30, 40, or 48 kHz • Capable of filtering 1-bit digital input data and converting them into 20-bit or 16-bit digital data • supports stereo microphone (L/R sampling by rising/falling clock edge) • supports sound activity detector to wake up CPU from WFI • Supports DMAC

1.1.14 Analog

Item	Description
A/D Converter (ADC)	• 8 channels • Resolution: 12 bits • Input range: 0 V to 1.8 V • Conversion rate: 1.0 Msps • Operation mode: Single scan, continuous scan • Condition for starting A/D conversion – Software trigger – Asynchronous trigger: External ADTRG trigger supported – Synchronous trigger: MTU3a and GPT timers
Temperature Sensor Unit (TSU)	• 1 channel for internal temperature

1.1.15 Battery backup function

Item	Description
Battery backup function (VBATT)	• Backup register (128 bytes) • Tamper detection – Triggered by input pin and software – Record RTC timestamp – Erase backup register – Reboot signal output for PMIC

1.1.16 Security

Item	Description
Secure IP (RSIP)	• Security algorism – Common key encryption: AES – Non-common key encryption: RSA, ECC • Other features – TRNG (true-random number generator) – Hash value generation: SHA-1, SHA-2, SHA-3 – Support of Unique ID

1.1.17 Others

Item	Description
Boundary Scan	Boundary scan based on IEEE 1149.1 via JTAG interface is supported. Note that some module pins are not available on this boundary scan.

1.1.18 Power Supply Voltage

Item	Description
Power supply voltage	• Refer to **3. Electrical Characteristics**

1.1.19 Temperature Range

Item	Description
Temperature range	• Tj: −40°C to +125°C

1.1.20 Quality Level

Item	Description
Quality level	• Industrial usage, etc.

1.1.21 Package

Item	Description
Package	• 368 pin LFBGA 17 mm square / 0.65 mm pitch • 400 pin LFBGA 14 mm square / 0.5 mm pitch

1.2 Block Diagram

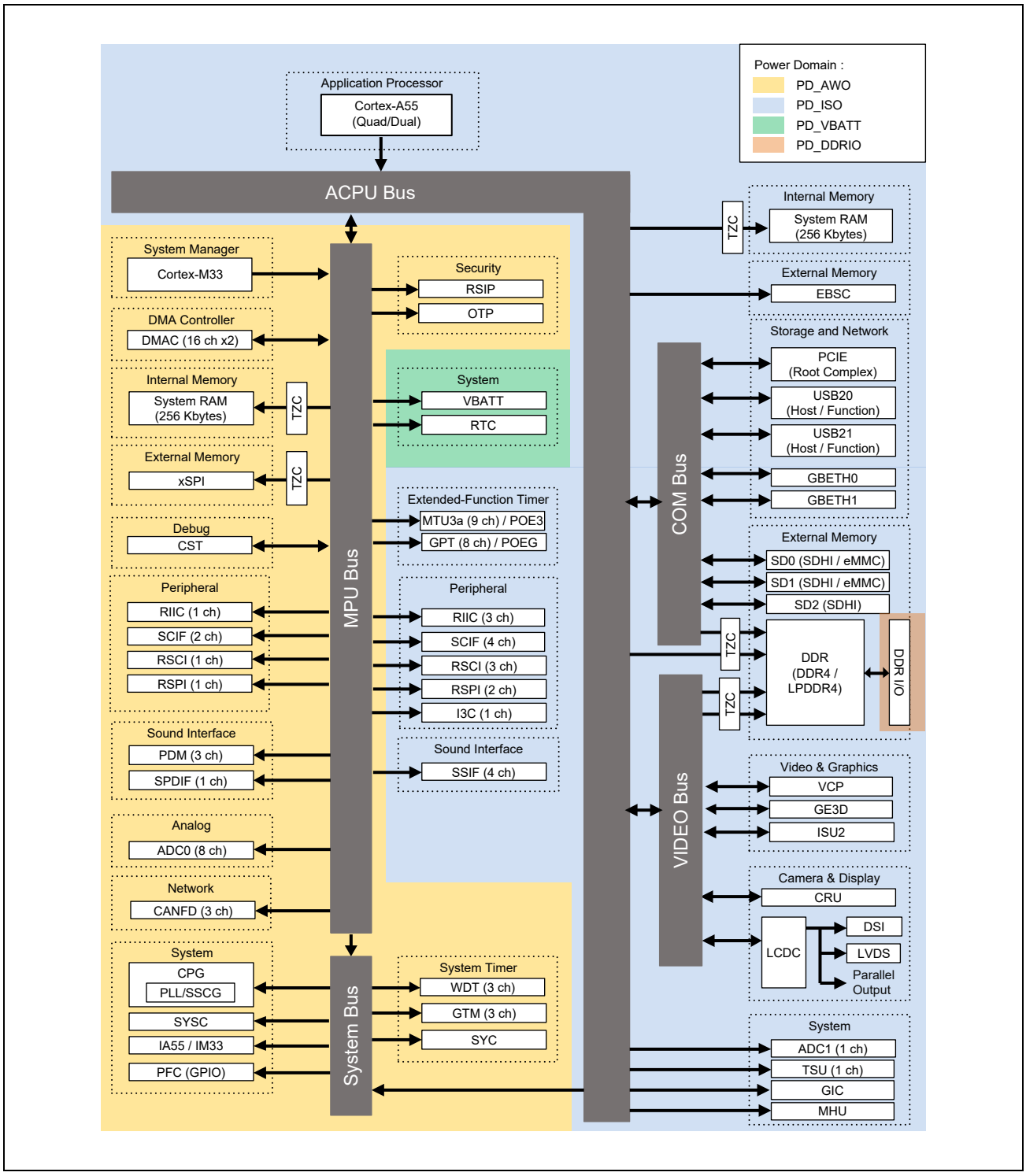


Figure 1.1 Block Diagram

Table 1.1 List of Units (1/2)

Unit Name	Function
ADC0	A/D converter
ADC1	A/D Converter for TSU
CA55	Arm Cortex-A55
CANFD	CAN-FD interface
CM33	Arm Cortex-M33
CPG	Clock pulse generator
CRU	Camera data receive unit (MIPI CSI-2 interface)
CST	Debug interface (Arm CoreSight)
DDR	DDR4 / LPDDR4 controller
DMAC	Direct memory access (DMA) controller
DSI	MIPI DSI interface
EBSC	External Bus State Controller
GBETH	Gigabit Ethernet interface
GE3D	3D graphics engine
GIC	Generic interrupt controller
GPT	General PWM timer
GTM	General timer
I3C	I3C bus interface
IA55	Synchronized Interrupt signals for CA55
IM33	Synchronized Interrupt signals for CM33
ISU2	Image Scaling Unit2
LCDC	LCD controller
LVDS	Low Voltage Differential Signal interface
MHU	Massage Handling Unit
MTU3a	Multi-function Timer Unit3
OTP	One-time programmable memory
PCIE	PCIe Express 2.0 interface (Root Complex only)
PDM	Pulse density modulation (PDM) interface
PFC	Pin function controller
POE3	Port Output Enable for MTU3a
POEG	Port Output Enable for GPT
RIIC	I2C bus interface
RSCI	Serial communication interface
RSIP	Renesas Security IP
RSPI	Serial peripheral interface
RTC	Realtime clock
SCIF	Serial communication interface with FIFO
SD	SD/MMC host interface
SPDIF	Sony Philips Digital Interface
SRAM	System RAM
SSIF	Serial sound interface
SYC	System counter
SYSC	System controller
TSU	Temperature sensor unit
TZC	CoreLink TrustZone Address Space Controller

Table 1.1 List of Units (2/2)

Unit Name	Function
USB2	USB2.0 Host / Function interface
VBATT	Battery backup function
VCP	H.264 Video Codec Processor
WDT	Watchdog timer
xSPI	xSPI controller

1.3 Product Lineup

Figure 1.2 shows the product part number information. **Table 1.2** shows a list of products.

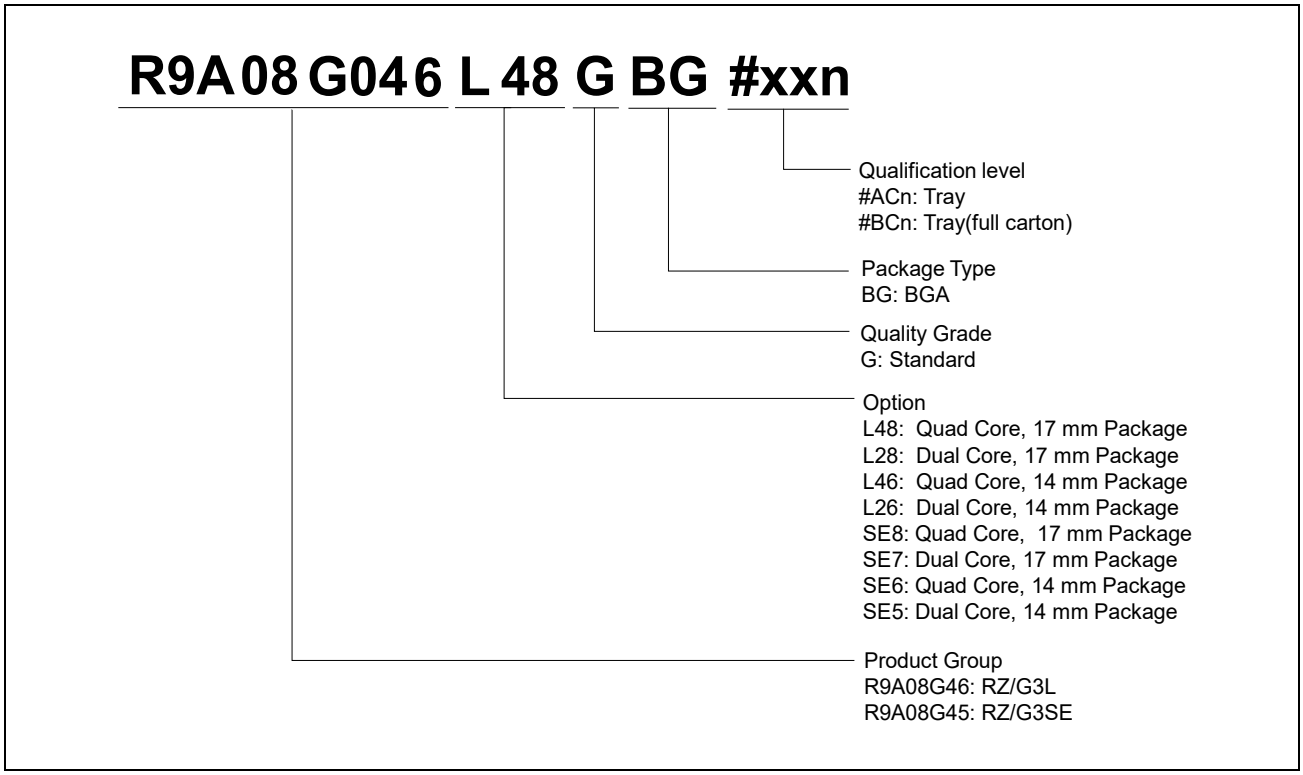


Figure 1.2 Part Numbering Scheme

Table 1.2 Product Lineup

Group	Package	Part Number	CPU	GE3D/VCP
RZ/G3L	17 mm LFBGA	R9A08G046L48GBG	4x Cortex-A55, 1x Cortex-M33	Available
		R9A08G046L28GBG	2x Cortex-A55, 1x Cortex-M33	
	14 mm LFBGA	R9A08G046L46GBG	4x Cortex-A55, 1x Cortex-M33	
		R9A08G046L26GBG	2x Cortex-A55, 1x Cortex-M33	
RZ/G3SE	17 mm LFBGA	R9A08G045SE8GBG	4x Cortex-A55, 1x Cortex-M33	Not supported
		R9A08G045SE7GBG	2x Cortex-A55, 1x Cortex-M33	
	14 mm LFBGA	R9A08G045SE6GBG	4x Cortex-A55, 1x Cortex-M33	
		R9A08G045SE5GBG	2x Cortex-A55, 1x Cortex-M33	

Note:

- Products with #AC0 or #BC0 in the part number have limitations in the MIPI DSI feature.
- For details, please contact a Renesas Electronics sales representative.

1.4 Function Comparison

The following table shows the function difference between RZ/G3L and RZ/G3SE.

There is no function difference between 14 mm package and 17 mm package.

Table 1.3 Function Comparison for RZ/G3L and RZ/G3SE (1/2)

Item		RZ/G3L		RZ/G3SE	
CPU	Cortex-A55 [Option]	Arm Cortex-A55 Processor 1.2 GHz			
		[Quad Core]	[Dual Core]	[Quad Core]	[Dual Core]
	Cortex-M33	Arm Cortex-M33 Processor 200 MHz			
	CST	Arm CoreSight architecture			
Boot		Selectable boot from Arm Cortex-A55 or Arm Cortex-M33			
Graphics	GE3D [option]	[Available] Arm Mali-G31 600 MHz		[Not supported]	
Video Processing	VCP [option]	[Available] H.264 codec		[Not supported]	
	ISU2	Scaling up and down function with bilinear interpolation			
Internal Memory	SRAM	512 Kbytes (with ECC)			
External Memory	DDR	DDR4-2133: Bus Width: 16-bit, Memory Size: Up to 4 Gbytes, Single rank			
		LPDDR4-2133: Bus Width: 16-bit, Memory Size: Up to 2 Gbytes, Single rank			
	xSPI	1 channel (2 chip select signals)			
	SD	3 channels			
	EBSC	1 channel			
CPU Peripheral	CPG	Generates the clocks from an external clock or external resonator (24 MHz)			
	DMAC	32 channels			
	GIC	Arm CoreLink Generic Interrupt Controller (GIC-600) for Arm Cortex-A55			
	MHU	Message handling function between Arm Cortex-A55 and Arm Cortex-M33			
	PFC	113 General-purpose I/O ports			
Camera Interface	CRU	1 channel (1 or 2-lanes)			
Display Interface	LCDC	1 channel			
	MIPI DSI	Selectable 1 display interface –1 channel MIPI DSI (1, 2 or 4-lanes) –1 channel LVDS –1 channel parallel output			
	LVDS				
	Parallel Output				
Storage and Network	USB2.0	2 channels (Host / Function)			
	PCIE	1 channel (Gen2, 1-lane, Root Complex only)			
	GBETH	2 channels			
	CANFD	3 channels			
Peripheral Modules	I3C	1 channel			
	RIIC	4 channels			
	RSCI	4 channels			
	RSPI	3 channels			
	SCIF	6 channels			
Timer	MTU3a with POE3	9 channels (16-bits × 8 channels, 32-bits × 1 channels)			
	GPT with POEG	32 bits × 8 channels			
	WDT	3 channels			
	GTM	32 bits × 3 channels			
	RTC	1 channel			

Table 1.3 Function Comparison for RZ/G3L and RZ/G3SE (2/2)

Item		RZ/G3L	RZ/G3SE
Audio Interface	SSIF	4 channels	
	SPDIF	1 channel	
	PDM	3 channels	
Analog	ADC	8 channels	
	TSU	1 channel	
Battery backup function	VBATT	Backup register / Tamper detection / Real time clock	
Security	RSIP	Hardware cryptographic engine	

2. Pin

This section describes the pins of this LSI.

2.1 Pin Assignment

Refer to attached excel file for the “ball view” about pin assignment of this LSI.
(Please double-click the icon on the right side)

2.2 External Pins and Multiplexed Functional Pins

Refer to attached excel file for the “pin function list” about information of external pins and multiplexed functional pins of this LSI.
(Please double-click the icon on the right side)

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 3.1 Absolute Maximum Ratings (1/2)

Power Domain	Item		Pin Name	Symbol	Min.	Max.	Unit
PD_VBATT	Power supply voltage (VBATT)		VDD_VBATT	VBATT_V_{DD}	−0.3	2.50	V
PD_AWO	Power supply voltage (1.0 V)		VDD10_AWO	AWO_V_{DD10}	−0.3	1.26	V
			VAA10_PLL23	PLL23_V_{AA10}			
	Power supply voltage (1.8 V)		PVDD18_AWO	AWO_PV_{DD18}	−0.3	2.45	V
			VAA18_ADC	ADC_V_{AA18}			
			VAA18_OTP	OTP_V_{AA18}	−0.3	2.50	V
	Power supply voltage	(1.8 V)	PVDD1833_OTH_AWO	OTH_AWO_PV_{DD1833}	−0.3	2.45	V
		(3.3 V)			−0.3	4.10	V
	Power supply voltage (xSPI)	(1.8 V)	PVDD1833_XSPI_AWO	XSPI_AWO_PV_{DD1833}	−0.3	2.45	V
		(3.3 V)			−0.3	4.10	V
PD_ISO	Power supply voltage (1.0 V)		VDD10_ISO	ISO_V_{DD10}	−0.3	1.26	V
			VAA10_PLLn (n = 16, 47, 5)	PLLn_V_{AA10}			
	Power supply voltage (1.8 V)		PVDD18_PRE_ISO	PRE_ISO_PV_{DD18}	−0.3	2.45	V
	Power supply voltage (SD)	(1.8 V)	PVDD1833_SDn_ISO (n = 0 to 2)	SDn_ISO_PV_{DD1833}	−0.3	2.45	V
		(3.3 V)			−0.3	4.10	V
	Power supply voltage (Ether)	(1.8V)	PVDD182533_ETn_ISO (n = 0, 1)	ETn_ISO_$PV_{DD182533}$	−0.3	2.45	V
		(2.5V)			−0.3	3.20	V
		(3.3V)			−0.3	4.10	V
	Power supply voltage	(1.8 V)	PVDD1833_OTH_ISO	OTH_ISO_PV_{DD1833}	−0.3	2.45	V
		(3.3 V)			−0.3	4.10	V
	Power supply voltage (I3C)	(1.2 V)	PVDD1218_I3C_ISO	I3C_ISO_PV_{DD1218}	−0.3	1.80	V
		(1.8 V)			−0.3	2.45	V
	Power supply voltage (PCIe)	(0.9 V)	VAA09_PCIE	PCIE_V_{AA09}	−0.3	1.26	V
		(1.8 V)	VAA18_PCIE	PCIE_V_{AA18}	−0.3	2.50	V
	Power supply voltage (DSI)		VAA18_DSI	DSI_V_{AA18}	−0.3	2.45	V
	Power supply voltage (CSI)		VAA18_CSI	CSI_V_{AA18}	−0.3	2.45	V
	Power supply voltage (TSU)		VAA18_TSU	TSU_V_{AA18}	−0.3	2.50	V
	Power supply voltage (USB2)	(1.8 V)	VAA18_USB2	USB2_V_{AA18}	−0.3	2.50	V
		(1.8 V)	VDD18_USB2	USB2_V_{DD18}	−0.3	2.50	V
		(3.3 V)	VAA33_USB2	USB2_V_{AA33}	−0.3	4.10	V

Table 3.1 Absolute Maximum Ratings (2/2)

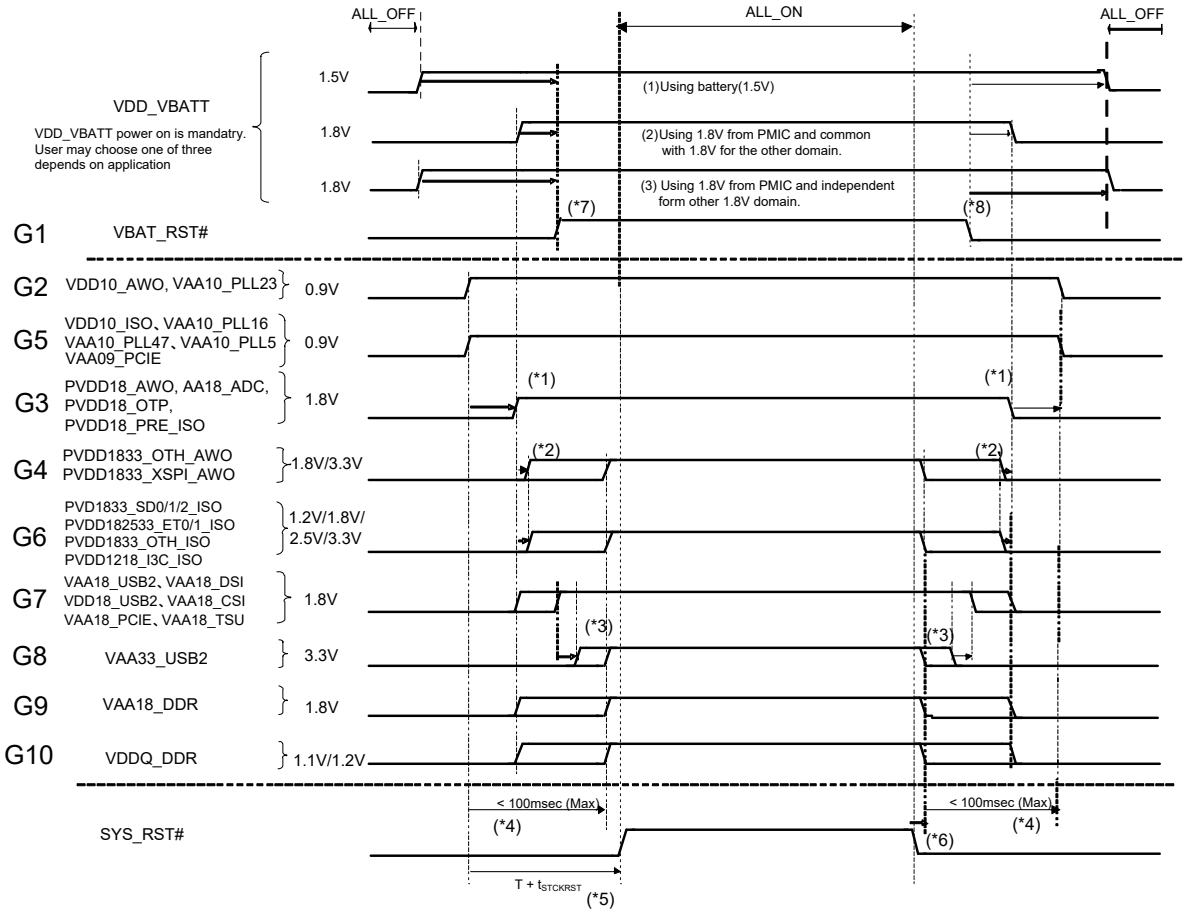
Power Domain	Item		Pin Name	Symbol	Min.	Max.	Unit
PD_ISO	Power supply voltage (DDR)	(1.8 V)	VAA18_DDR	DDR_VAA18	−0.3	2.50	V
		(1.1 V/ 1.2 V)	VDDQ_DDR	VDDR_VDDQ	−0.3	1.68	V
PD_AWO PS_ISO	Input voltage (3.3 V I/O input signal)		—	—	−0.5	3.3 V power supply + 0.5	V
PD_AWO PD_ISO	Input voltage (2.5 V I/O input signal)		—	—	−0.5	2.5 V power supply + 0.5	V
PD_VBATT PD_AWO PD_ISO	Input voltage (1.8 V I/O input signal)		—	—	−0.5	1.8 V power supply + 0.5	V
—	Operating temperature		Ambient	Ta	−40	85	°C
—			Junction	Tj	−40	125	°C
—	Storage temperature		Ambient	Tstg	-40	150	°C

3.2 Recommended Operating Range

Table 3.2 Recommended Operating Range

Unit Name	Item		Pin Name	Symbol	Min.	Typ.	Max.	Unit	Group
PD_VBATT	Power supply voltage (VBATT)		VDD_VBATT	VBATT_V_{DD}	1.5	—	1.95	V	G1
PD_AWO	Power supply voltage (1.0 V)		VDD10_AWO	AWO_V_{DD10}	0.97	1.0	1.05	V	G2
			VAA10_PLL23	PLL23_V_{AA10}					
	Power supply voltage (1.8 V)		PVDD18_AWO	AWO_PV_{DD18}	1.65	1.8	1.95	V	G3
			VAA18_ADC	ADC_V_{AA18}					
			VAA18_OTP	OTP_V_{AA18}					
	Power supply voltage	(1.8 V)	PVDD1833_OTH_AWO	OTH_AWO_PV_{DD1833}	1.65	1.8	1.95	V	G4
		(3.3 V)			3.00	3.3	3.60	V	
	Power supply voltage (xSPI)	(1.8 V)	PVDD1833_XSPI_AWO	XSPI_AWO_PV_{DD1833}	1.65	1.8	1.95	V	
		(3.3 V)			3.00	3.3	3.60	V	
PD_ISO	Power supply voltage (1.0 V)		VDD10_ISO	ISO_V_{DD10}	0.97	1.0	1.05	V	G5
			VAA10_PLLn (n = 16, 47, 5)	PLLn_V_{AA10}					
	Power supply voltage (1.8 V)		PVDD18_PRE_ISO	PRE_ISO_PV_{DD18}	1.65	1.8	1.95	V	G3
	Power supply voltage (SD)	(1.8 V)	PVDD1833_SDn_ISO (n = 0 to 2)	SDn_ISO_PV_{DD1833}	1.65	1.8	1.95	V	G6
		(3.3 V)			3.00	3.3	3.60	V	
	Power supply voltage (Ether)	(1.8 V)	PVDD182533_ETn_ISO (n = 0, 1)	ETn_ISO_$PV_{DD182533}$	1.65	1.8	1.95	V	
		(2.5 V)			2.30	2.5	2.70	V	
		(3.3 V)			3.00	3.3	3.60	V	
	Power supply voltage	(1.8 V)	PVDD1833_OTH_ISO	OTH_ISO_PV_{DD1833}	1.65	1.8	1.95	V	
		(3.3 V)			3.00	3.3	3.60	V	
	Power supply voltage (I3C)	(1.2 V)	PVDD1218_I3C_ISO	I3C_ISO_PV_{DD1218}	1.10	1.2	1.30	V	
		(1.8 V)			1.65	1.8	1.95	V	
	Power supply voltage (PCIe)	(0.9 V)	VAA09_PCIE	PCIE_V_{AA09}	0.89	0.94	0.99	V	G5
		(1.8 V)	VAA18_PCIE	PCIE_V_{AA18}	1.65	1.8	1.95	V	G7
	Power supply voltage (DSI)		VAA18_DSI	DSI_V_{AA18}	1.65	1.8	1.95	V	G7
	Power supply voltage (CSI)		VAA18_CSI	CSI_V_{AA18}	1.65	1.8	1.95	V	G7
	Power supply voltage (TSU)		VAA18_TSU	TSU_V_{AA18}	1.65	1.8	1.95	V	G7
	Power supply voltage (USB2)	(1.8 V)	VAA18_USB2	USB2_V_{AA18}	1.65	1.8	1.95	V	G7
		(1.8 V)	VDD18_USB2	USB2_V_{DD18}					
		(3.3 V)	VAA33_USB2	USB2_V_{AA33}	3.00	3.3	3.60	V	G8
	Power supply voltage (DDR)	(1.8 V)	VAA18_DDR	DDR_V_{AA18}	1.65	1.8	1.95	V	G9
		(1.1 V)	VDDQ_DDR (LPDDR4)	DDR_V_{DDQ}	1.06	1.1	1.17	V	G10
		(1.2 V)	VDDQ_DDR (DDR4)		1.14	1.2	1.26	V	

3.3 Power-On/Power-Off Sequence



Note 1. G3 must be powered on after G2, G5 and powered off before G2, G5. G3 and G7 may be powered on / off at the same time.

Note 2. G4, G6 must be powered on after G3 and powered off before G3. If G4 voltage is 1.8V, G4 can be powered on/off along with G3, this also applies to G6.

Note 3. G8 must be powered on after G7 and powered off before G7.

Note 4. It is recommended that all the power domains are powered on or off within approximately 100 msec.

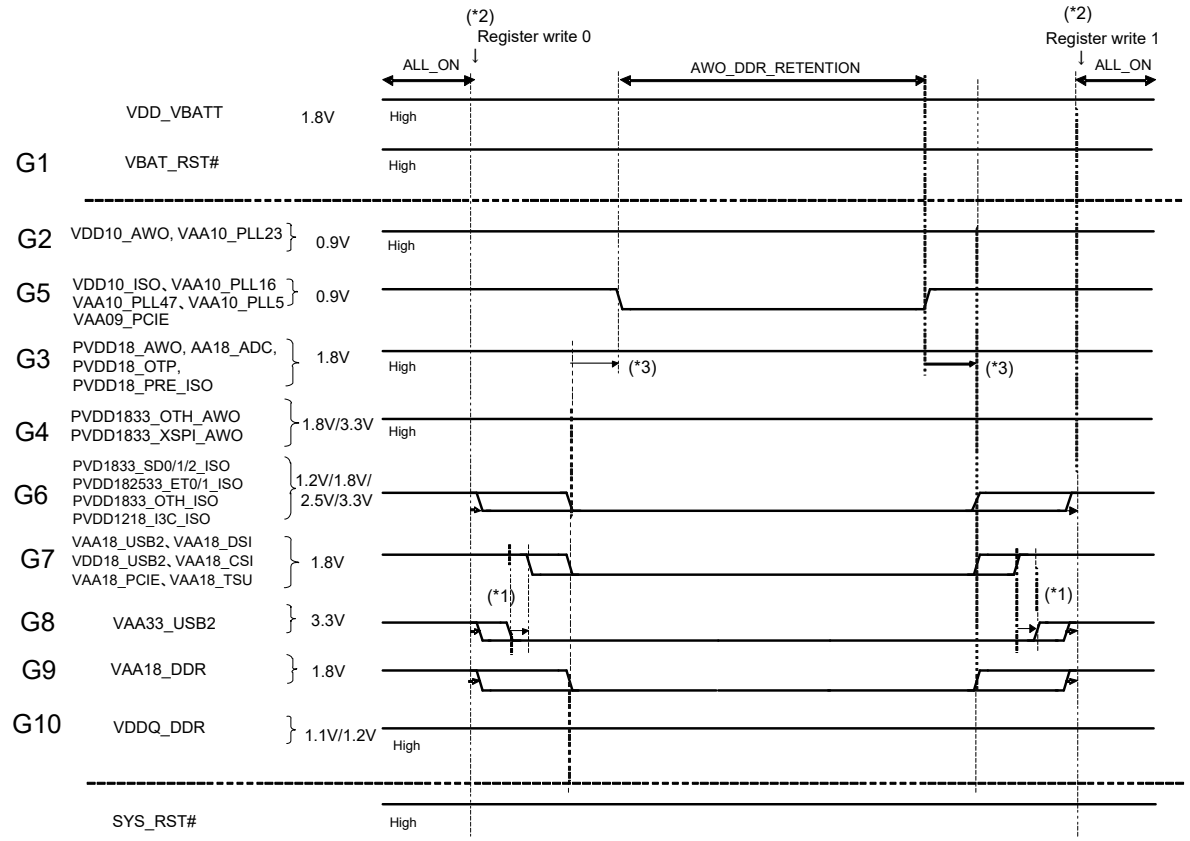
Note 5. SYS_RST# must be deasserted at least (T + $t_{STCKRST}$) after G2 is powered on.

Note 6. SYS_RST# must be changed to Low before powered off.

Note 7. VBAT_RST# must be high after 50 μ sec from VDD_VBATT power on.

Note 8. When power off, VBAT_RST# should be low before or at the same time as VDD_VBATT is powered off.

Figure 3.1 Power-On/Power-Off Sequence 1 (All_OFF to ALL_ON, ALL_ON to ALL_OFF)



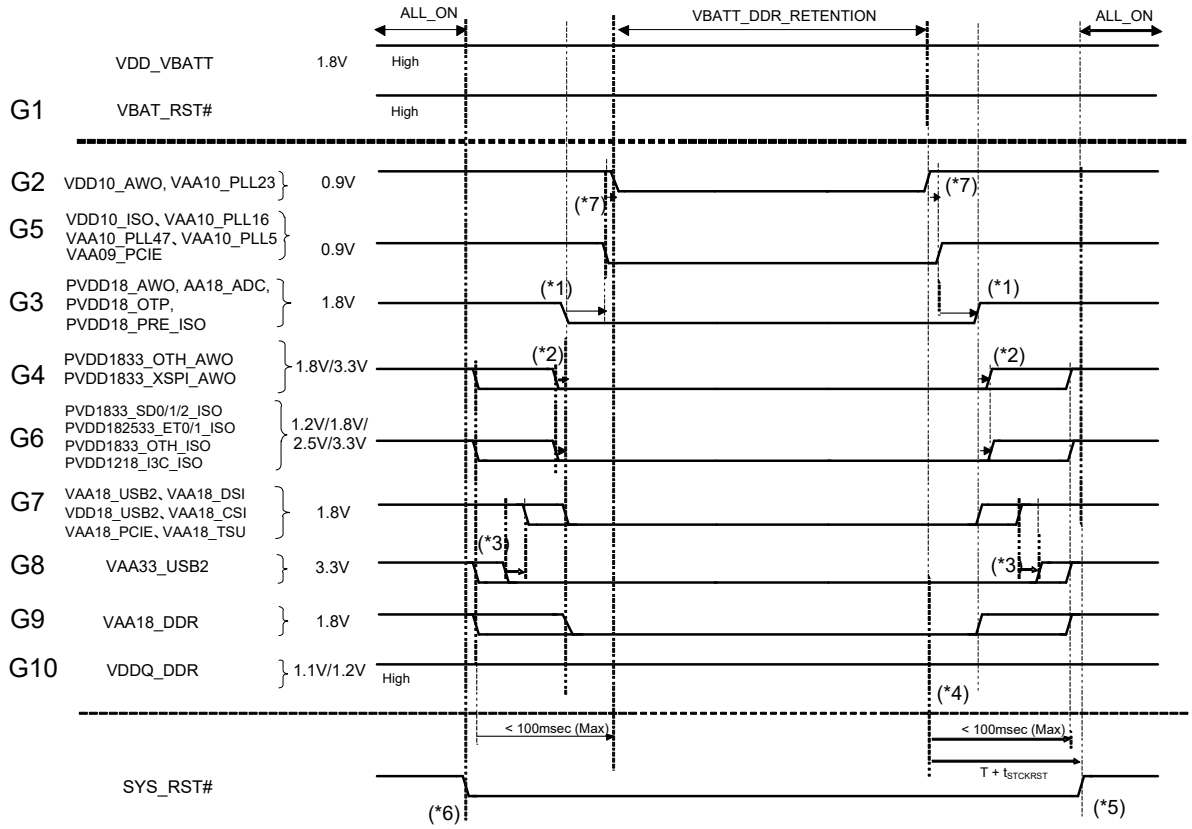
Note 1. G8 must be powered off before G7 and powered on after G7.

Note 2. The following registers must be written before G6, G7, G8, G9, G10 are powered off and after G6, G7, G8, G9, G10 are powered on.

- SYS_PD_ISO_CTRL
- ISO_IOBUF_SE18_CTRL
- SYS_PWRRDY_N
- CPG_RST_PCI (in CPG)

Note 3. G5 must be powered off after G6 to G10 are powered off and powered on before G6 to G10 are powered on.

Figure 3.2 Power-On/Power-Off Sequence 2 (ALL_ON to AWO_DDR_RETENTION, AWO_DDR_RETENTION to ALL_ON)



Note 1. G3 must be powered off before G2, G5 and powered on after G2, G5. G3 and G7 can be powered on / off at the same time.

Note 2. G4, G6 must be powered off before G3 and powered on after G3. If G4 voltage is 1.8 V, G4 can be powered on / off along with G3, this also applies to G6.

Note 3. G8 must be powered off before G7 and powered on after G7.

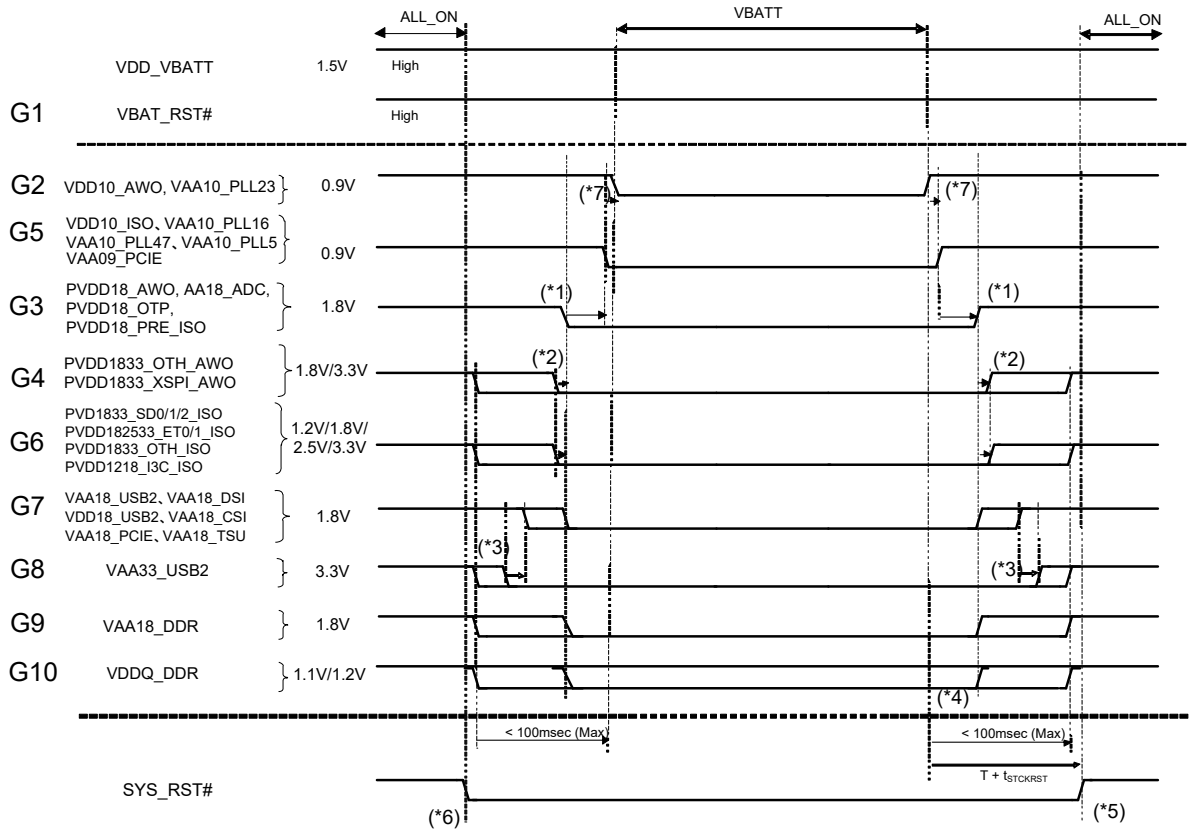
Note 4. It is recommended that all the power domains are powered on or off within approximately 100 msec.

Note 5. SYS_RST# must be deasserted at least (T + $t_{STCKRST}$) after G2 is powered on.

Note 6. SYS_RST# must be changed to Low before powered off.

Note 7. G5 must be powered off before G2 and powered on after G2.

Figure 3.3 Power-On/Power-Off Sequence 3 (ALL_ON to VBATT_DDR_RETENTION, VBATT_DDR_RETENTION to ALL_ON)



Note 1. G3 must be powered off before G2, G5 and powered on after G2, G5. G3 and G7 can be powered on / off at the same time.

Note 2. G4, G6 must be powered off before G3 and powered on after G3. If G4 voltage is 1.8 V, G4 can be powered on / off along with G3, this also applies to G6.

Note 3. G8 must be powered off before G7 and powered on after G7.

Note 4. It is recommended that all the power domains are powered on or off within approximately 100 msec.

Note 5. SYS_RST# must be deasserted at least (T + $t_{STCKRST}$) after G2 is powered on.

Note 6. SYS_RST# must be changed to Low before powered off.

Note 7. G5 must be powered off before G2 and powered on after G2.

Figure 3.4 Power-On/Power-Off Sequence 4 (ALL_ON to VBATT, VBATT to ALL_ON)

3.4 DC Characteristics

Table 3.3 DC Characteristics (1) [GP I/O (1.8/3.3 V)]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage		V_{IH}	2	—	—	V	3.3 V mode
Low-level input voltage		V_{IL}	—	—	0.8	V	
Hysteresis threshold ↑		V_T+	2.1	—	—	V	
Hysteresis threshold ↓		V_T-	—	—	0.7	V	
Output logic high voltage	(I_{OH} = –1.9 mA)	V_{OH}	V_{CCQ} – 0.4	—	—	V	
	(I_{OH} = –4 mA)						
	(I_{OH} = –8 mA)						
	(I_{OH} = –9 mA)						
Output logic low voltage	(I_{OL} = 1.9 mA)	V_{OL}	—	—	0.4	V	
	(I_{OL} = 4 mA)						
	(I_{OL} = 8 mA)						
	(I_{OL} = 9 mA)						
High-level input voltage		V_{IH}	1.16	—	—	V	1.8 V mode
Low-level input voltage		V_{IL}	—	—	0.5	V	
Hysteresis threshold ↑		V_T+	1.40	—	—	V	
Hysteresis threshold ↓		V_T-	—	—	0.41	V	
Output logic high voltage	(I_{OH} = –2.2 mA)	V_{OH}	V_{CCQ} − 0.45	—	—	V	
	(I_{OH} = –4.4 mA)						
	(I_{OH} = –9 mA)						
	(I_{OH} = –10 mA)						
Output logic low voltage	(I_{OL} = 2.2 mA)	V_{OL}	—	—	0.45	V	
	(I_{OL} = 4.4 mA)						
	(I_{OL} = 9 mA)						
	(I_{OL} = 10 mA)						
Weak pull-up resistor (input mode)		R_{UP}	10 K	50 K	90 K	Ω	
Weak pull-down resistor (input mode)		R_{DN}	10 K	50 K	90 K	Ω	
Input leakage current		I_{LI}	—	—	10	μA	0V ≤ V_{in} ≤ PV_{DD}*1 In case of 3state buffer, the leak current when output mode OFF

Note: V_{in} means input voltage of external input pin.

Note 1. PVDD1833_OTH_ISO, PVDD1833_OTH_AWO, PVDD18_PWC

Table 3.4 DC Characteristics (2) [SD I/O (1.8/3.3 V)]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage		V_{IH}	V_{DDQ} × 0.625	—	—	V	3.3 V mode
Low-level input voltage		V_{IL}	—	—	V_{DDQ} × 0.25	V	
Output logic high voltage	(I_{OH} = –4 mA)	V_{OH}	V_{CCQ} – 0.4	—	—	V	
	(I_{OH} = –6 mA)						
	(I_{OH} = –8 mA)						
	(I_{OH} = –9 mA)						
Output logic low voltage	(I_{OL} = 4 mA)	V_{OL}	—	—	0.4	V	
	(I_{OL} = 6 mA)						
	(I_{OL} = 8 mA)						
	(I_{OL} = 9 mA)						
High-level input voltage		V_{IH}	1.27	—	—	V	1.8 V mode
Low-level input voltage		V_{IL}	—	—	0.58	V	
Output logic high voltage	(I_{OH} = –7 mA)	V_{OH}	V_{CCQ} – 0.45	—	—	V	
	(I_{OH} = –8 mA)						
	(I_{OH} = –9 mA)						
	(I_{OH} = –10 mA)						
Output logic low voltage	(I_{OL} = 7 mA)	V_{OL}	—	—	0.45	V	
	(I_{OL} = 8 mA)						
	(I_{OL} = 9 mA)						
	(I_{OL} = 10 mA)						
Weak pull-up resistor (input mode)		R_{UP}	10 K	50 K	90 K	Ω	3.3 V/1.8 V mode
Weak pull-down resistor (input mode)		R_{DN}	10 K	50 K	90 K	Ω	

Table 3.5 DC Characteristics (3) [RGMII (1.8/2.5/3.3 V)]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage	V_{IH}	V_{CCQ} × 0.65	—	—	V	3.3 V mode
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.35	V	
Output logic high voltage	V_{OH}	V_{CCQ} – 0.4	—	—	V	
Output logic low voltage	V_{OL}	—	—	0.4	V	
High-level input voltage	V_{IH}	1.7	—	—	V	2.5 V mode
Low-level input voltage	V_{IL}	—	—	0.7	V	
Output logic high voltage	V_{OH}	V_{CCQ} – 0.4	—	—	V	
Output logic low voltage	V_{OL}	—	—	0.4	V	
High-level input voltage	V_{IH}	V_{CCQ} × 0.65	—	—	V	1.8 V mode
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.35	V	
Output logic high voltage	V_{OH}	V_{CCQ} – 0.45	—	—	V	
Output logic low voltage	V_{OL}	—	—	0.45	V	

Table 3.6 DC Characteristics (4) [I3C (1.2/1.8 V)]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.8 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I3C Open Drain mode
Output logic low voltage	IOL = 3 mA	V_{OL}	—	—	0.27	V	
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.8 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I2C Open Drain mode*1
Output logic low voltage	IOL = 20 mA	V_{OL}	—	—	0.4	V	
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.8 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I3C CMOS mode
Output logic high voltage	IOL= −3 mA	V_{OH}	V_{CCQ} − 0.27	—		V	
Output logic low voltage	IOL= 3 mA	V_{OL}	—	—	0.27	V	
High-level input voltage		V_{IH}	V_{CCQ} × 0.7	—	—	V	1.2 V
Low-level input voltage		V_{IL}	—	—	V_{CCQ} × 0.3	V	I3C CMOS mode
Output logic high voltage	IOL = −2 mA	V_{OH}	V_{CCQ} − 0.18	—		V	
Output logic low voltage	IOL = 2 mA	V_{OL}	—	—	0.18	V	

Note 1. fast-mode, fast-mode plus

Table 3.7 DC Characteristics (5) [Input (Schmitt/1.8 V)]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage	V_{IH}	V_{CCQ} × 0.75	—	—	V	
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.25	V	

Table 3.8 DC Characteristics (6) [Input (3.3 V tolerant/Schmitt)]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
High-level input voltage	V_{IH}	V_{CCQ} × 0.75	—	—	V	
Low-level input voltage	V_{IL}	—	—	V_{CCQ} × 0.25	V	

Table 3.9 DC Characteristics (7) [USB 2.0]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Input levels for low/full speed						
High (driven)	V_{IH}	2.0	—	—	V	
Low	V_{IL}	—	—	0.8	V	
Differential input sensitivity	V_{DI}	0.2	—	—	V	
Differential common mode range	V_{CM}	0.8	—	2.5	V	
Input levels for high speed						
High-speed squelch detection threshold (differential signal amplitude)	V_{HSSQ}	100	—	150	mV	
High-speed data signaling common mode voltage range (guideline for receiver)	V_{HSCM}	−50	—	500	mV	
Output levels for low/full speed						
Low	V_{OL}	0.0	—	0.3	V	
High (driven)	V_{OH}	2.8	—	3.6	V	
Output signal crossover voltage	V_{CRS}	1.3	—	2.0	V	
Output levels for high-speed						
High-speed idle level	V_{HSOI}	−10.0	—	10.0	mV	
High-speed data signaling high	V_{HSOH}	360	—	440	mV	
High-speed data signaling low	V_{HSOL}	−10.0	—	10.0	mV	
Chirp J level (differential voltage)	V_{CHIRPJ}	700	—	1100	mV	
Chirp K level (differential voltage)	V_{CHIRPK}	−900	—	−500	mV	

Table 3.10 DC Characteristics (8) [ADC]

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Resolution	—	—	12	—	Bit	
Analog input channel	—	—	—	8	Channel	
Analog input range	AIN	V_{SS}	—	ADC_AV_{DD18}	V	
Differential non-linearity	DNL	—	—	±3.0	LSB	
Integral non-linearity	INL	—	—	±6.0	LSB	
Full-scale error	—	—	±10	±20	LSB	
Offset error	—	—	±10	±20	LSB	
Analog input capacitance	C_{IN}	—	—	7.2	pF	
Analog input resistance	R_{IN}	—	—	1755	Ω	
External capacitance	C_{EXT}	—	—	(*1)	pf	
External resistance	R_{EXT}	—	—	(*1)	Ω	

Note 1. Refer to **Figure 3.5** for Cext and Rext.
The Cext and Rext need to satisfy the sampling time.
A/D conversion time = sampling time (71T to 255T) + 29T.
T stands for the cycle of ADIVCLK (100 MHz).
If A/D conversion is performed with the minimum conversion time, the sampling time must be 71T.
(Minimum conversion time per channel is 1 µs when A/D conversion clock ADIVCLK is 100 MHz.)

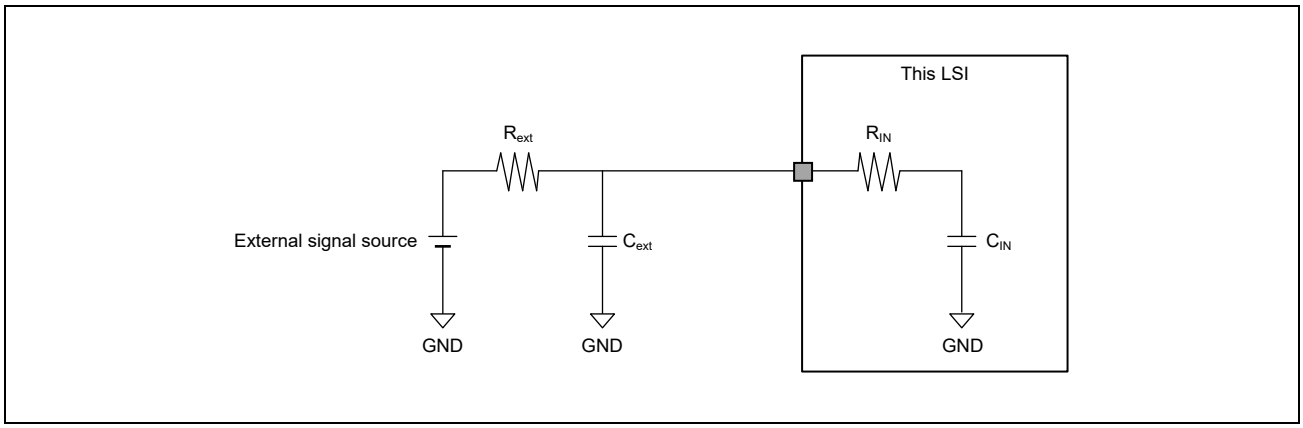


Figure 3.5 Analog Input Equivalent Circuit

Table 3.11 DC Characteristics (9) [Current Consumption]

Item	Power Rail Symbol	Max Current	Unit	Remarks
Power Supply Voltage (VBATT)	VDD_VBATT	10	mA	
Power Supply Voltage (Core)	VDD10_AWO	300	mA	
Power Supply Voltage (ISO)	VDD10_ISO	4200	mA	Condition: Cortex-A55, Dhrystone
Power Supply Voltage (PLL)	VAA10_PLL16	10	mA	
	VAA10_PLL23	10	mA	
	VAA10_PLL47	10	mA	
	VAA10_PLL5	10	mA	
Power Supply Voltage (I/O)	PVDD18_AWO	100	mA	
	PVDD18_PRE_ISO	100	mA	
Power Supply Voltage (Other) (1.8V)	PVDD1833_OTH_AWO	100	mA	
	PVDD1833_OTH_ISO	300	mA	
Power Supply Voltage (Other) (3.3V)	PVDD1833_OTH_AWO	100	mA	
	PVDD1833_OTH_ISO	400	mA	
Power Supply Voltage (ADC)	VAA18_ADC	10	mA	
Power Supply Voltage (ADC/TSU)	VAA18_TSU	10	mA	
Power Supply Voltage (OTP)	VAA18_OTP	20	mA	
Power Supply Voltage (XSPI) (1.8 V)	PVDD1833_XSPI_AWO	200	mA	Max cond.: xSPI-400 (133MHz,15pF)
Power Supply Voltage (XSPI) (3.3 V)	PVDD1833_XSPI_AWO	200	mA	Max cond.: MTU 2ch (16MHz, 30pF)
Power Supply Voltage (I3C) (1.8 V)	PVDD1218_I3C_ISO	10	mA	
Power Supply Voltage (I3C) (1.2 V)	PVDD1218_I3C_ISO	10	mA	
Power Supply Voltage (SD) (1.8 V)	PVDD1833_SD0_ISO	100	mA	Max cond.: HS400 (150MHz,15pF)
	PVDD1833_SD1_ISO	100	mA	Max cond.: SDR50 (100MHz, 43pF)
	PVDD1833_SD2_ISO	100	mA	Max cond.: SDR50 (100MHz, 43pF)
Power Supply Voltage (SD) (3.3 V)	PVDD1833_SD0_ISO	100	mA	Max cond.: HS (50MHz, 30pF)
	PVDD1833_SD1_ISO	100	mA	Max cond.: HS (50MHz, 30pF)
	PVDD1833_SD2_ISO	100	mA	Max cond.: RSPI (50MHz, 30pF)
Power Supply Voltage (Ether) (1.8 V)	PVDD182533_ET0_ISO	100	mA	Max cond.: RSCI-4ch (50MHz, 30pF)
	PVDD182533_ET1_ISO	200	mA	Max cond.: EBSC (133MHz, 30pF)
Power Supply Voltage (Ether) (2.5 V)	PVDD182533_ET0_ISO	100	mA	Max cond.: RSCI-4ch (50MHz, 30pF)
	PVDD182533_ET1_ISO	200	mA	Max cond.: EBSC (133MHz, 30pF)
Power Supply Voltage (Ether) (3.3 V)	PVDD182533_ET0_ISO	200	mA	Max cond.: RSCI-4ch (50MHz, 30pF)
	PVDD182533_ET1_ISO	200	mA	Max cond.: EBSC (133MHz, 30pF)
Power Supply Voltage (USB)	VAA33_USB2	100	mA	
	VAA18_USB2	200	mA	
	VDD18_USB2		mA	
Power Supply Voltage (PCIe)	VAA18_PCIE	100	mA	
	VAA09_PCIE	100	mA	
Power Supply Voltage (CSI)	VAA18_CSI	100	mA	
Power Supply Voltage (DSI)	VAA18_DSI	100	mA	
Power Supply Voltage (DDR)	VAA18_DDR	10	mA	
Power Supply Voltage (DDR) (DDR4)	VDDQ_DDR	300	mA	
Power Supply Voltage (DDR) (LPDDR4)	VDDQ_DDR	300	mA	

Note: T_j = 125°C, Power supply voltage = Max.

3.5 AC Characteristics

Conditions: VDD_VBATT = 1.50 to 1.95 V, VDD10_AWO = VAA10_PLL23 = 0.97 to 1.05 V,
PVDD18_AWO = VAA18_ADC = VAA18_OTP = PVDD18_PRE_ISO = 1.65 to 1.95 V,
PVDD1833_OTH_AWO = PVDD1833_XSPI_AWO = 1.65 to 1.95 V / 3.0 to 3.6 V,
VDD10_ISO = VAA10_PLLn (n=16, 47, 5) = 0.97 to 1.05 V, VAA09_PCIE = 0.89 to 0.99 V,
PVDD1833_SDn_ISO (n=0 to 2) = PVDD1833_OTH_ISO = 1.65 to 1.95 V / 3.0 to 3.6 V,
PVDD1218_I3C_ISO = 1.10 to 1.30 V / 1.65 to 1.95 V,
PVDD182533_ETn_ISO (n=0, 1) = 1.65 to 1.95 V / 2.3 to 2.7 V / 3.0 to 3.6 V,
VAA18_PCIE = VAA18_DSI = VAA18_CSI = VAA18_TSU = VAA18_USB2 = VDD18_USB2 = VAA18_DDR = 1.65 to 1.95 V,
VAA33_USB2 = 3.0 to 3.6 V, VDDQ_DDR = 1.06 to 1.17 V(LPDDR4) / 1.14 to 1.26 V (DDR4),
AVSS_USB2 = AVSS_ADC = AVSS_TSU = 0 V, VSS = 0 V, T_a = −40 to +85°C, T_j = −40 to +125°C

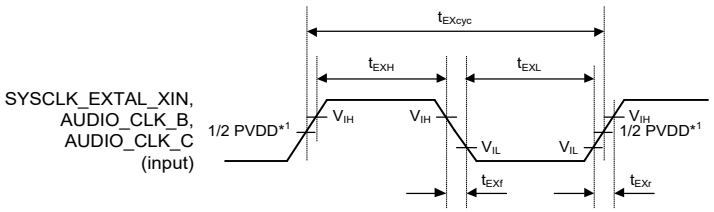
3.5.1 Clock Timing

Table 3.12 Clock Timing Table

Item	Symbol	Min.	Max.	Unit	Figures
SYSCLK_EXTAL_XIN clock input frequency	f_{EX}	24 – 50ppm*1	24 + 50ppm*1	MHz	**Figure 3.6**
SYSCLK_EXTAL_XIN clock input cycle time	t_{EXcyc}	41.67	41.67	ns	
AUDIO_CLK_B, AUDIO_CLK_C clock input frequency (external clock is input)	f_{EX}	10	50	MHz	
AUDIO_CLK_B, AUDIO_CLK_C clock input cycle time (external clock is input)	t_{EXcyc}	20	100	ns	
SYSCLK_EXTAL_XIN, AUDIO_CLK_B, AUDIO_CLK_C clock input low level pulse width	t_{EXL}	0.4	0.6	t_{EXcyc}	
SYSCLK_EXTAL_XIN, AUDIO_CLK_B, AUDIO_CLK_C clock input high level pulse width	t_{EXH}	0.4	0.6	t_{EXcyc}	
SYSCLK_EXTAL_XIN, AUDIO_CLK_B, AUDIO_CLK_C clock input rise time	t_{EXr}	—	4	ns	
SYSCLK_EXTAL_XIN, AUDIO_CLK_B, AUDIO_CLK_C clock input fall time	t_{EXf}	—	4	ns	
Oscillator stabilization time	T	(*2)	—	ms	**Figure 3.7**, **Figure 3.8**
SYSCLK stabilization to SYS_RST# deassertion	$t_{STCKRST}$	1	—	µs	
Mode hold time	t_{MDH}	12	—	µs	
Mode setup time	t_{MDS}	0	—	µs	

Note 1. When using RGMII interface. If not using RGMII mode, this spec is ±100 ppm.

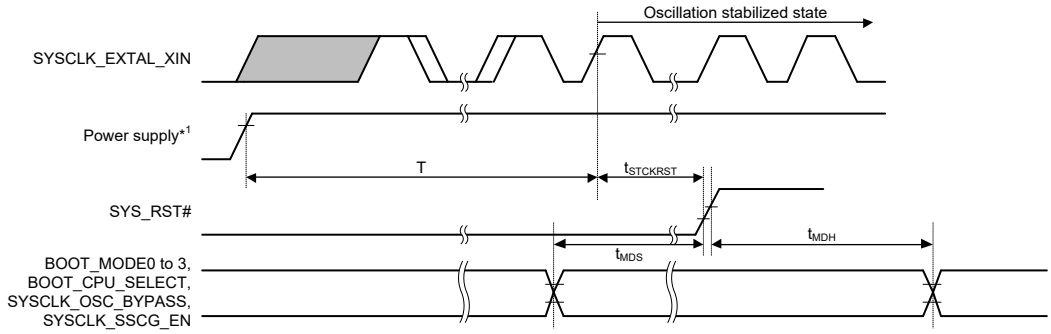
Note 2. The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by a crystal resonator matching test. For details of the stabilization time “T”, please contact the crystal manufacture.



Note: When the clock is input on the SYSCLK_EXTAL_XIN, AUDIO_CLK_B or AUDIO_CLK_C

Note 1. SYSCLK_EXTAL_XIN: PVDD18_AWO,
AUDIO_CLK_B, C: PVDD1833_OTH_AWO, PVDD1833_OTH_ISO, PVDD1833_SDn_ISO(n = 1, 2) or PVDD182533_ET1_ISO

Figure 3.6 EXCLK, AUDIO_CLK1 and AUDIO_CLK2 Clock Input Timing



Note 1. VDD_VBATT, VDD10_AWO, VAA10_PLL23, PVDD18_AWO, VAA18_ADC, VAA18_OTP, PVDD18_PRE_ISO, PVDD1833_OTH_AWO, PVDD1833_XSPI_AWO, VDD10_ISO, VAA10_PLLn (n = 16, 47, 5), VAA09_PCIE, PVDD1833_SDn_ISO (n = 0 to 2), PVDD1833_OTH_ISO, PVDD1218_I3C_ISO, PVDD182533_ETn_ISO (n = 0, 1), VAA18_PCIE, VAA18_DSI, VAA18_CSI, VAA18_TSU, VAA18_USB2, VDD18_USB2, VAA18_DDR, VAA33_USB2, VDDQ_DDR

Figure 3.7 Power-On Oscillation Settling Time

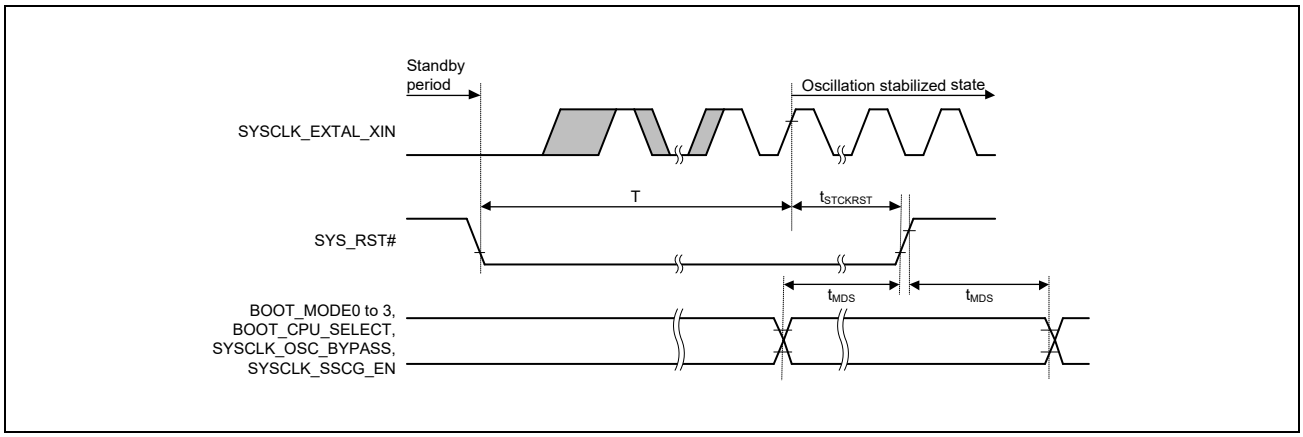


Figure 3.8 Oscillation Settling Time on Return from Standby (Return by Reset)

Table 3.13 32-kHz Clock Oscillator Timing Table

Item	Symbol	Min.	Max.	Unit	Figures
32-kHz clock oscillator stabilization time	t_{ROSC}	—	2.5	sec	

Note: Oscillation stabilization time after enabling the oscillation of the 32-kHz OSC implemented in the VBATTB region

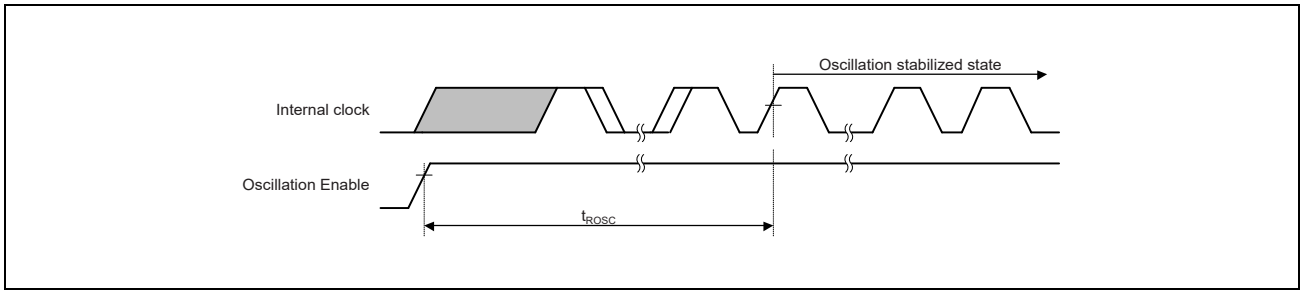


Figure 3.9 32-kHz Clock Oscillator Stabilization Time

3.5.2 Control Signal Access Timing

Table 3.14 Control Signal Timing

Item	Symbol	Min.	Max.	Unit	Figures
SYS_RST# pulse width	t_{RESW}	20	—	t_{cyc}*1	**Figure 3.10**
JTAG_TRST# pulse width	t_{TRSW}	20	—	t_{cyc}*1	
NMI pulse width	t_{NMIW}	20	—	t_{cyc}*1	**Figure 3.11**
IRQ pulse width	t_{IRQW}	20	—	t_{cyc}*1	
TINT pulse width	t_{TINTW}	20	—	t_{cyc}*1	
SYS_RST# input rise time	t_{RSr}	—	500	µs	**Figure 3.12**

Note 1. t_{cyc} = 41.666 ns (24 MHz)

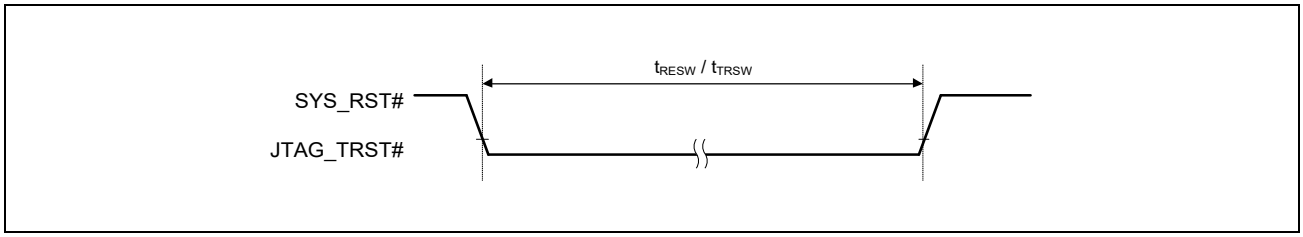


Figure 3.10 Reset Input Timing 1

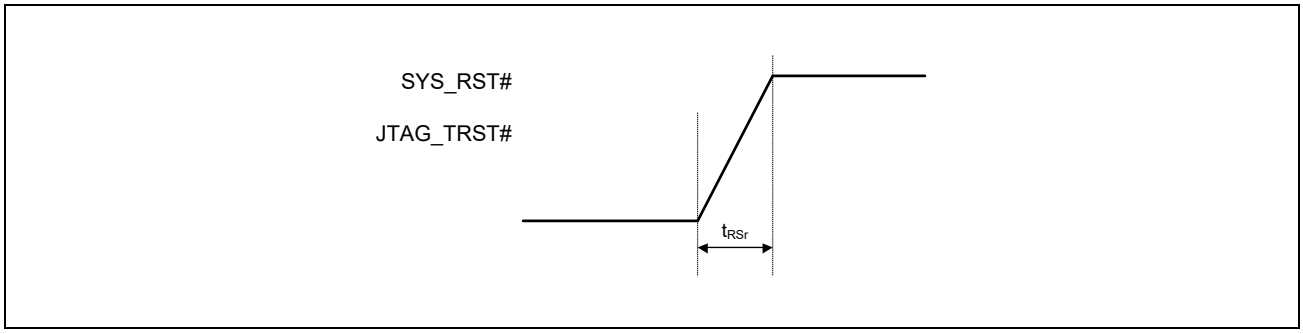
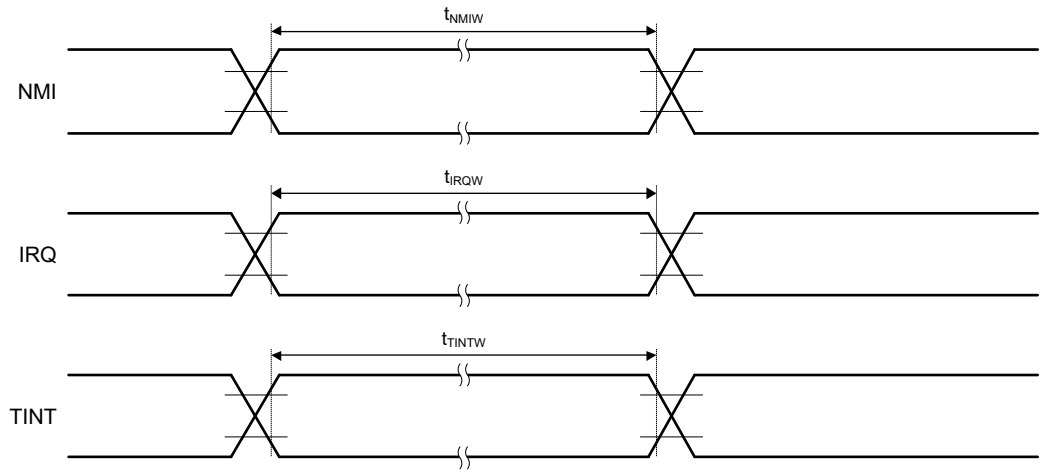


Figure 3.11 Reset Input Timing 2



Note: This specification “(Min. 20 t_{cycle})” is the min. pulse width the case that the digital noise filter is off.

Figure 3.12 Interrupt Signal Input Timing

3.5.3 JTAG Debugger Interface Access Timing

Table 3.15 Debugger IF Timing

Item	Symbol	Min.	Max.	Unit	Figures
JTAG_TCK_SWCLK cycle time	t_{TCKcyc}	50	—	ns	**Figure 3.13**
JTAG_TCK_SWCLK high pulse width	t_{TCKH}	20	—	ns	**Figure 3.14**
JTAG_TCK_SWCLK low pulse width	t_{TCKL}	20	—	ns	
JTAG_TDI setup time	t_{TDIS}	15	—	ns	
JTAG_TDI hold time	t_{TDIH}	15	—	ns	
JTAG_TMS_SWDIO setup time	t_{TMSS}	15	—	ns	
JTAG_TMS_SWDIO hold time	t_{TMSH}	15	—	ns	
JTAG_SWDIO delay time	t_{SWDO}	—	14	ns	
JTAG_TDO delay time	t_{TDOD}	—	14	ns	
Capture register setup time	t_{CAPTS}	10	—	ns	**Figure 3.15**
Capture register hold time	t_{CAPTH}	10	—	ns	
Update register delay time	$t_{UPDATED}$	—	20	ns	

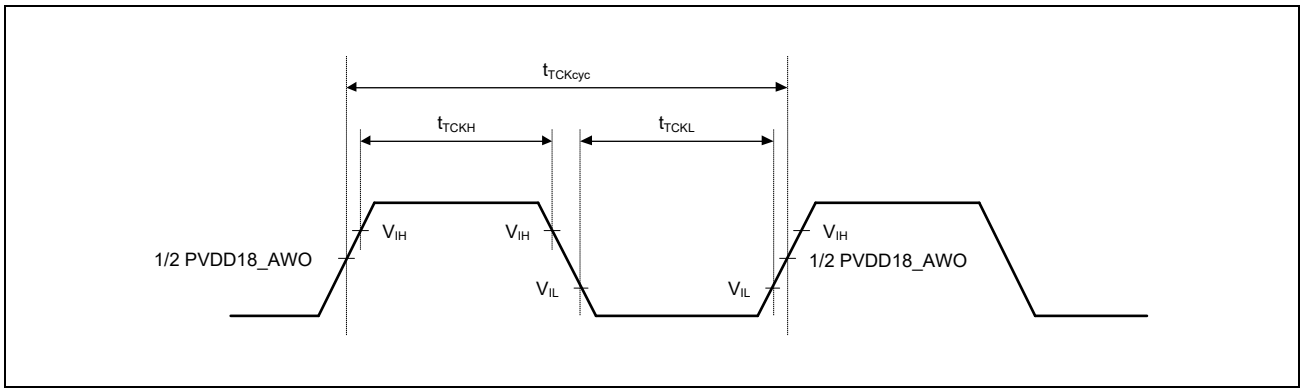


Figure 3.13 JTAG_TCK_SWDCLK Input Timing

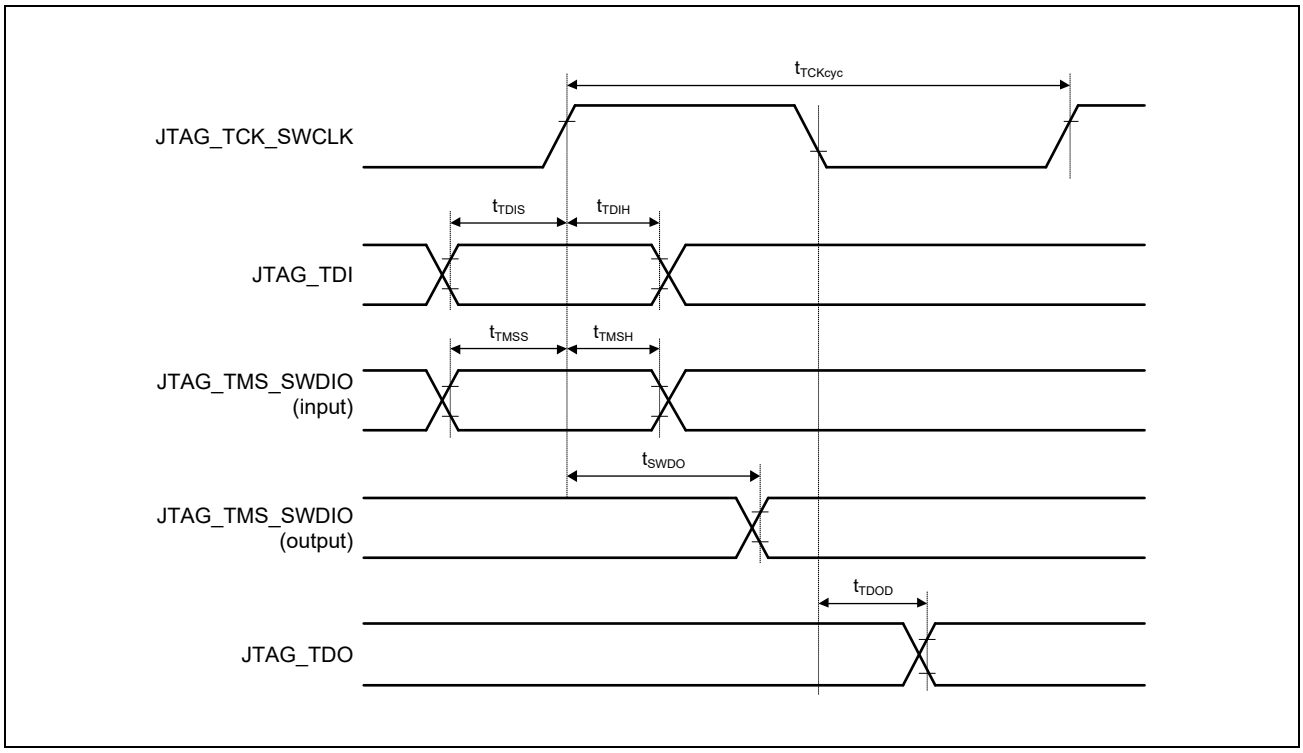


Figure 3.14 Data Transfer Timing

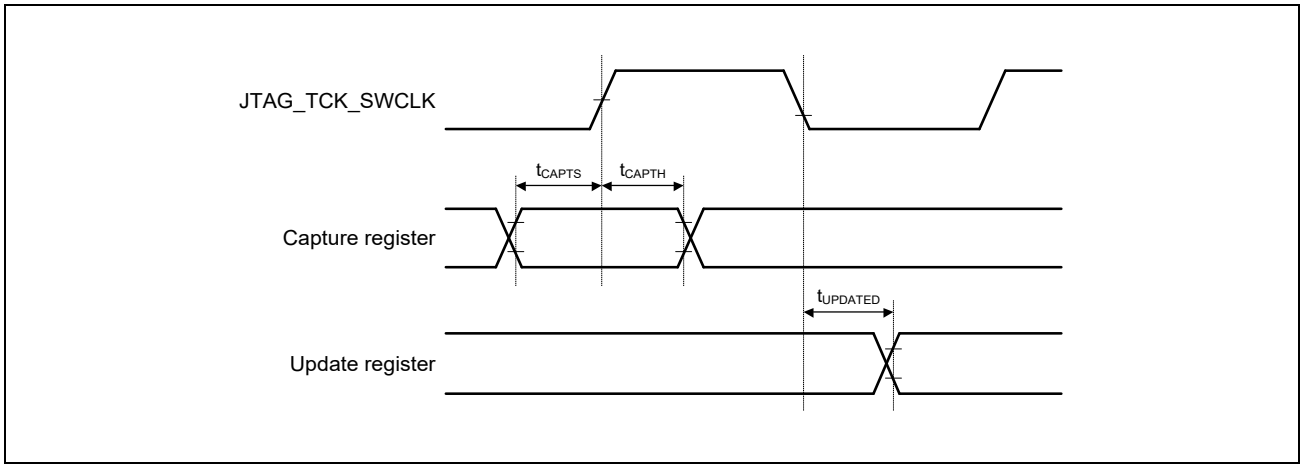


Figure 3.15 Boundary Scan Input/Output I/O Timing

3.5.4 DDR Interface Characteristics

The LPDDR4/DDR4 interface of this LSI is compliant with the JESD209-4E/JESD79-4D standard.

3.5.5 External Bus State Controller Timing

Table 3.16 External Bus State Controller Timing

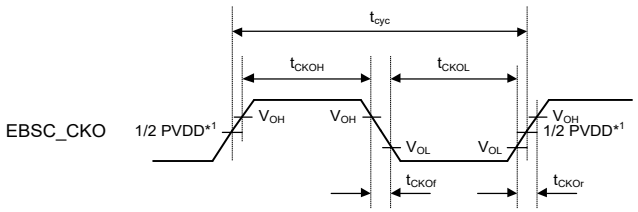
Item	Symbol	EBSC_CKO = 133 MHz*1		Unit	Figure
		Min.	Max.		
EBSC_CKO clock output cycle time	t_{cyc}	7.5	—	ns	**Figure 3.16**
EBSC_CKO clock output rise time	t_{CKOr}	—	1	ns	
EBSC_CKO clock output fall time	t_{CKOf}	—	1	ns	
EBSC_CKO clock output low pulse width	t_{CKOL}	1/2 t_{cyc} − t_{CKOr}	—	ns	
EBSC_CKO clock output high pulse width	t_{CKOH}	1/2 t_{cyc} − t_{CKOf}	—	ns	
Address delay time 1	t_{AD1}	−1.8	1.8	ns	**Figure 3.17** to **Figure 3.22**
Address setup time	t_{AS}	1/2 t_{cyc} − 2	—	ns	**Figure 3.17** to **Figure 3.20**
Chip enable setup time	t_{CS}	1/2 t_{cyc} – 2	—	ns	
Address hold time	t_{AH}	1/2 t_{cyc} – 2	—	ns	
BS delay time	t_{BSD}	—	1.8	ns	**Figure 3.17** to **Figure 3.22**
CS delay time 1	t_{CSD1}	−1.8	1.8	ns	
Read write delay time 1	t_{RWD1}	−1.8	1.8	ns	
Read strobe delay time	t_{RSD}	1/2 t_{cyc} – 1.5	1/2 t_{cyc} + 1.5*3	ns	
Read data setup time 1	t_{RDS1}	1/2 t_{cyc} + 5*3	—	ns	
Read data hold time 1	t_{RDH1}	0	—	ns	
Write enable delay time 1	t_{WED1}	1/2 t_{cyc} – 1.5	1/2 t_{cyc} + 1.5*3	ns	**Figure 3.17** to **Figure 3.21**
Write enable delay time 2	t_{WED2}	—	—	ns	**Figure 3.22**
Write data delay time 1	t_{WDD1}	—	1.8	ns	**Figure 3.17** to **Figure 3.22**
Write data hold time 1	t_{WDH1}	−1.8	—	ns	
Write data hold time 4	t_{WDH4}	1/2 t_{cyc} − 2	—	ns	**Figure 3.17** to **Figure 3.20**
WAIT setup time	t_{WDS}	1/2 t_{cyc} + 5*3	—	ns	**Figure 3.18** to **Figure 3.22**
WAIT hold time	t_{WTH}	1/2 t_{cyc} + 3.5*3	—	ns	

Note: AC access timing condition: drive ability IOLH_xx{1:0} = 11b

Note 1. The maximum value (fmax) of EBSC_CKO (external bus clock) depends on the number of wait cycles and the system configuration of your board.

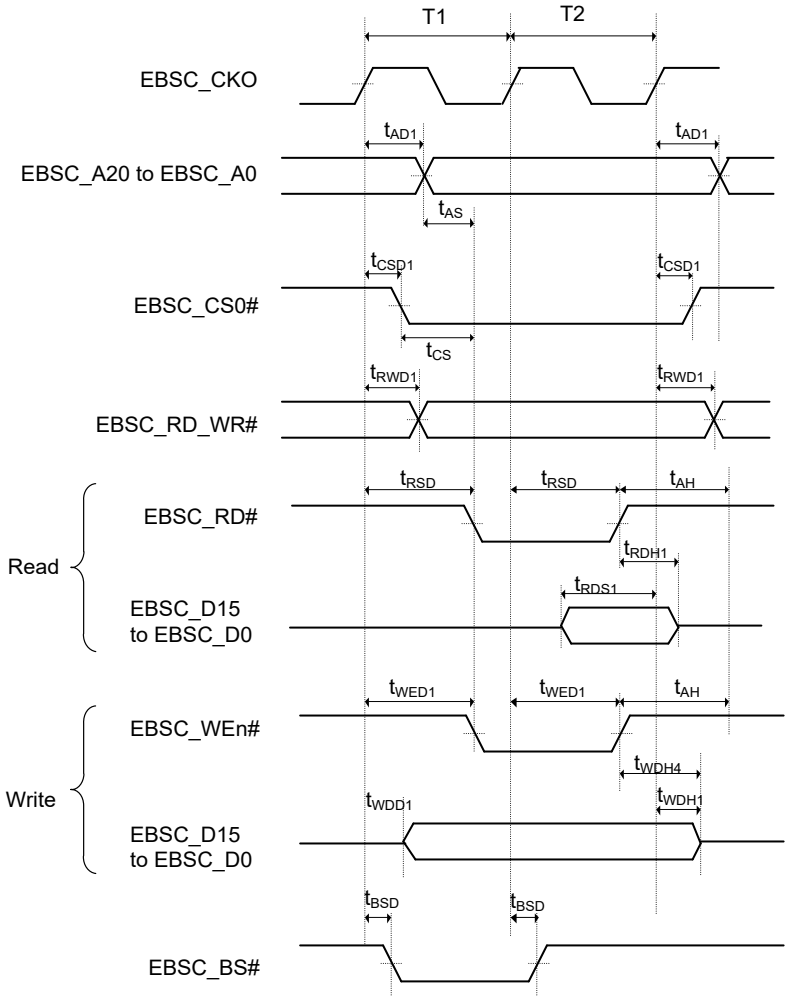
Note 2. 1/2 t_{cyc} indicated in minimum and maximum values for the item of delay, setup, and hold times represents a half cycle from the rising edge with a clock. That is, 1/2 t_{cyc} describes a reference of the falling edge with a clock.

Note 3. Suitable wait cycles need to be set with CS0WCR register to response to connected device and operation frequency.



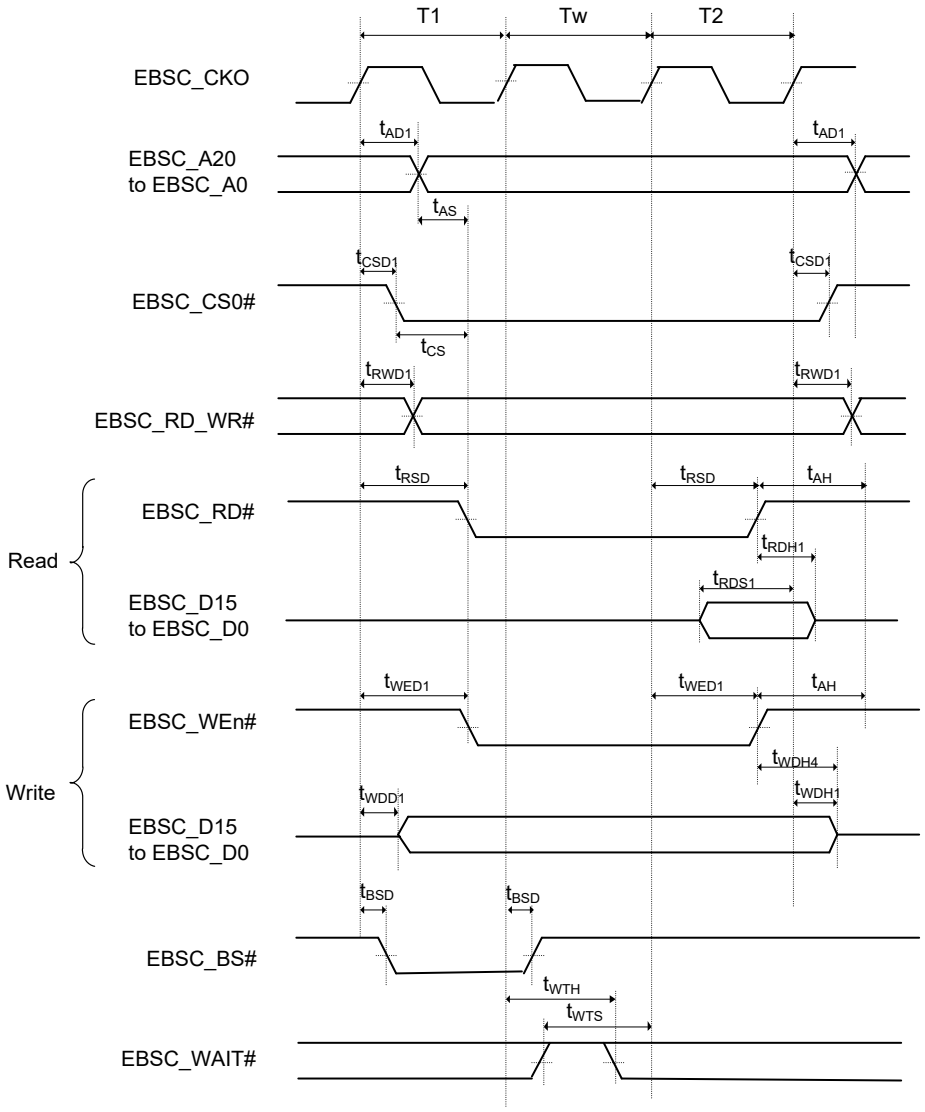
Note 1. PVDD1833_OTH_ISO, PVDD182533_ET0_ISO, PVDD182533_ET0_ISO

Figure 3.16 EBSC_CKO Clock Output Timing



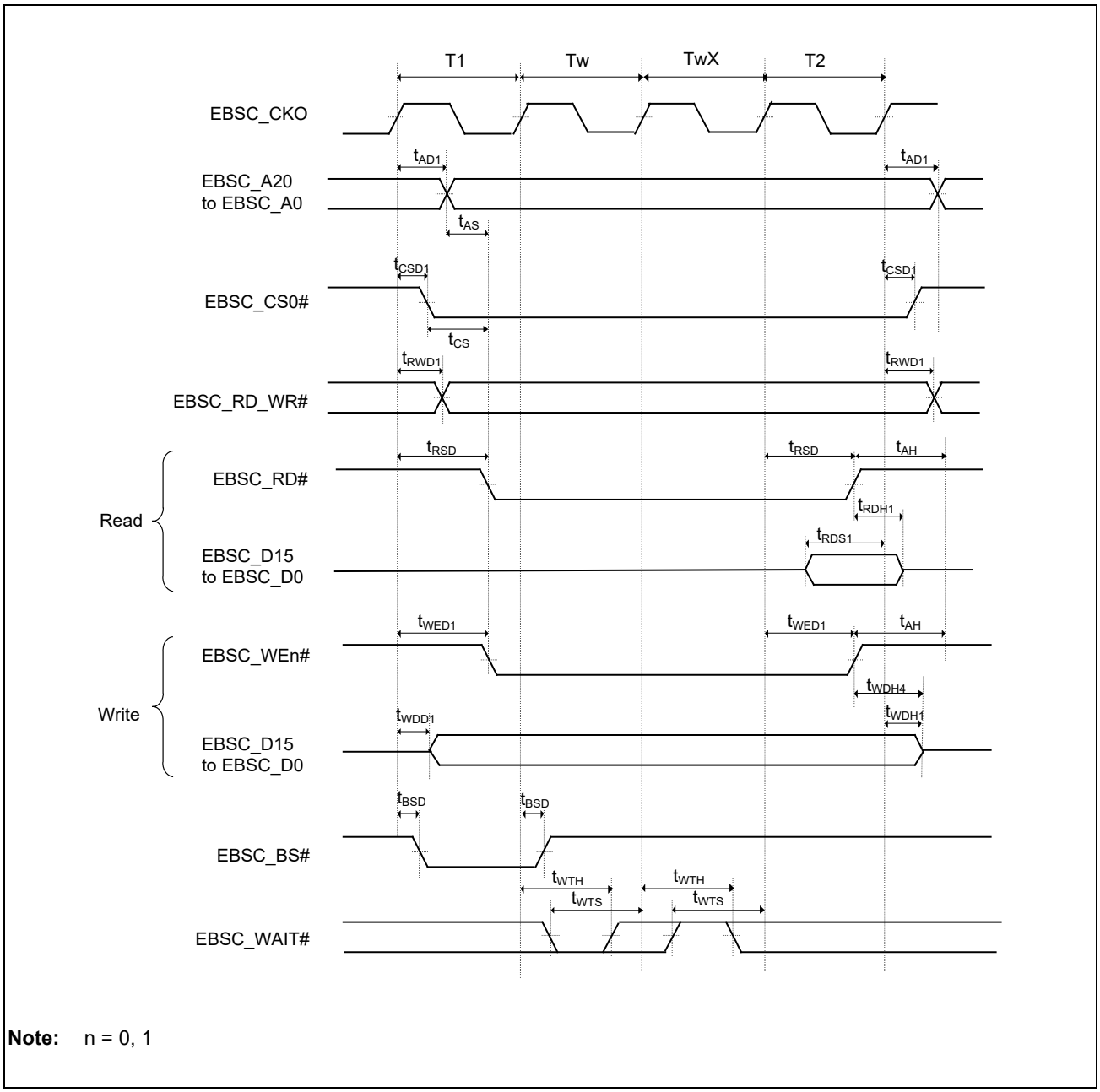
Note: n = 0, 1

Figure 3.17 Basic Bus Timing for Normal Space (No Wait)



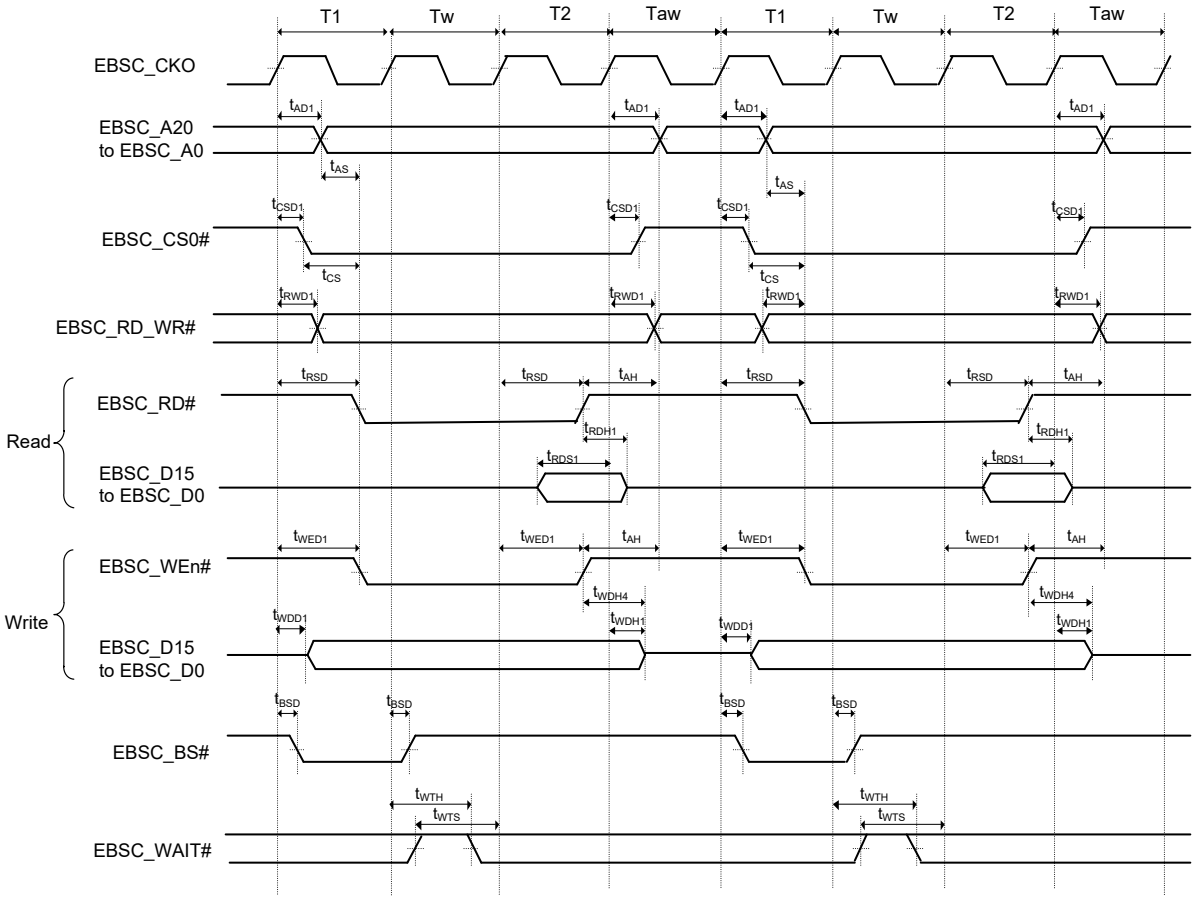
Note: n = 0, 1

Figure 3.18 Basic Bus Timing for Normal Space (One Software Wait Cycle)



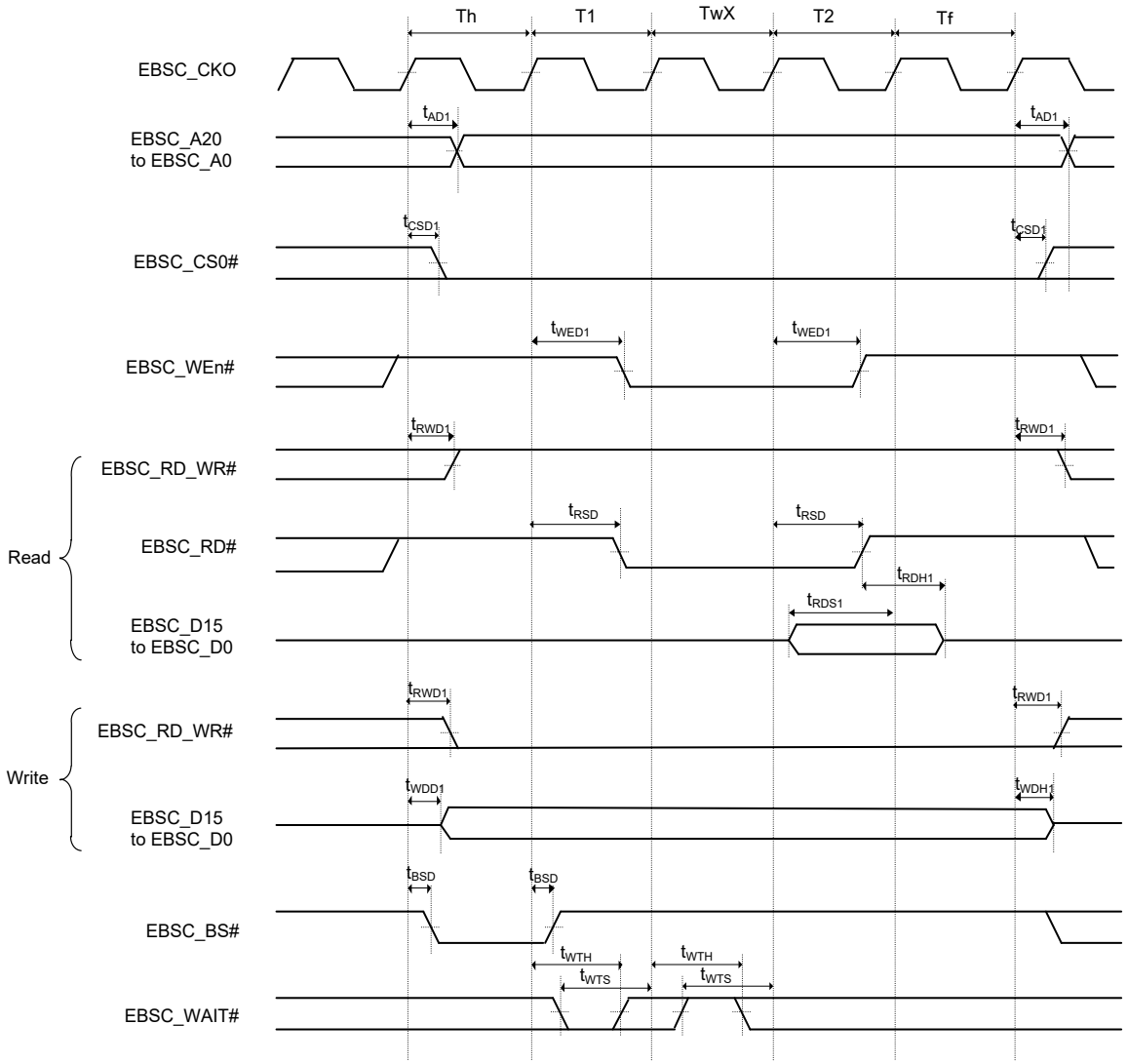
Note: n = 0, 1

Figure 3.19 Basic Bus Timing for Normal Space (One Software Wait Cycle, One External Wait Cycle)



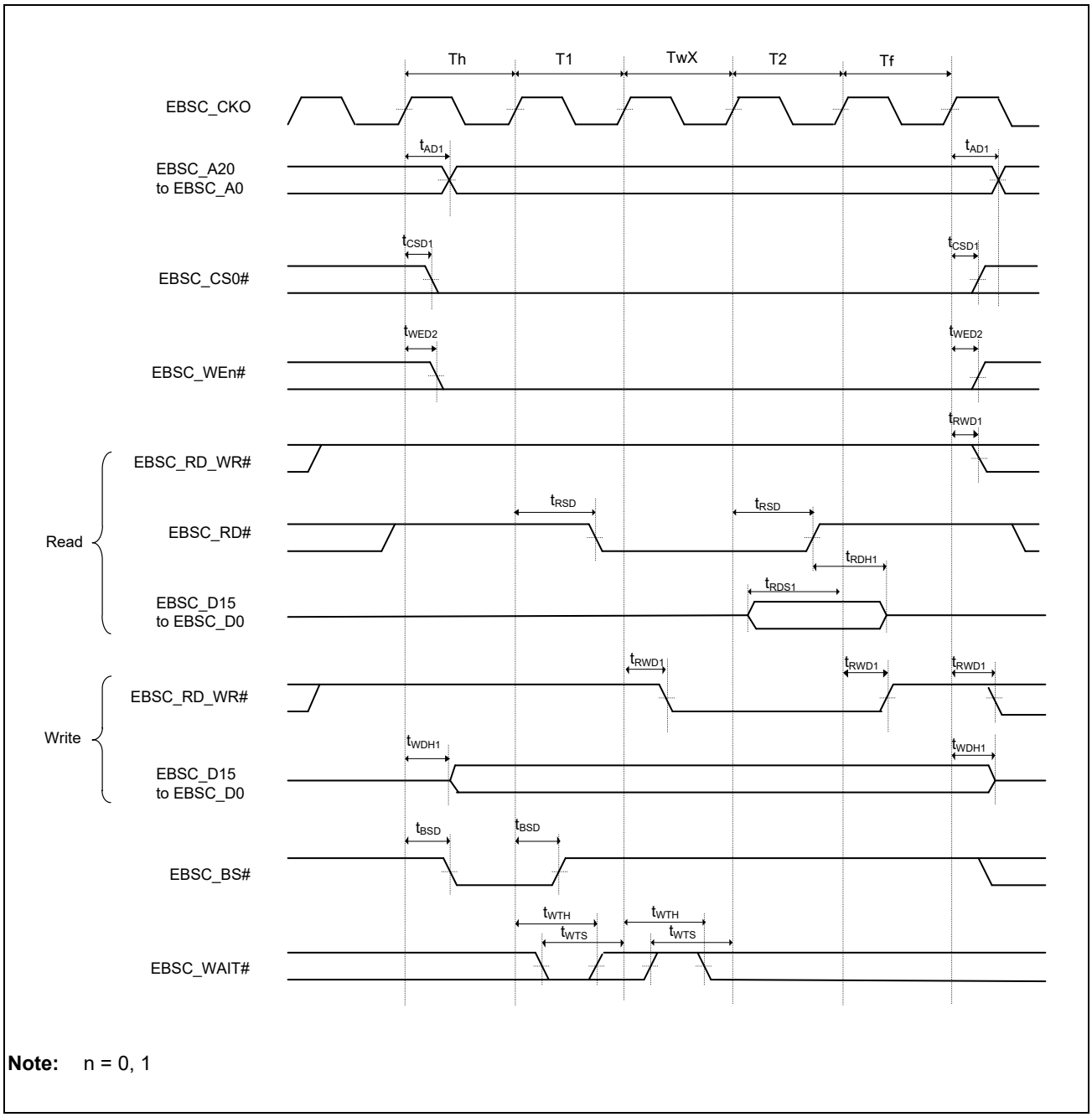
Note: n = 0, 1

Figure 3.20 Basic Bus Timing for Normal Space (One Software Wait Cycle, External Wait Cycle Valid (WM Bit = 0), No Idle Cycle)



Note: n = 0, 1

Figure 3.21 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 0 (Write Cycle UB#/LB# Control))



Note: n = 0, 1

Figure 3.22 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 1 (Write Cycle WE# Control))

3.5.6 Watchdog Timer Access Timing

Table 3.17 Watchdog Timer Timing

Item	Symbol	Min.	Max.	Unit	Figures
WDT_OVF_PERROUT# Output Time	t_L	64	64	t_{P1cyc}*1	**Figure 3.23**

Note 1. t_{P1cyc} indicates peripheral clock means WDTn_CLK (OSCCLK) (n = 0 to 2).

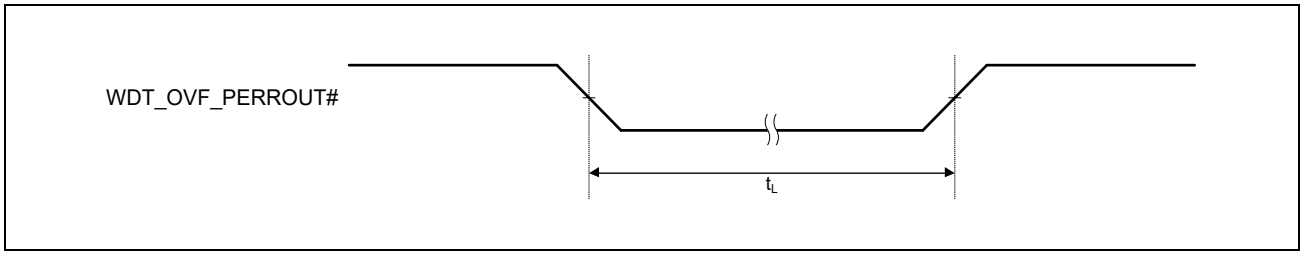


Figure 3.23 Watchdog Timer Output Timing

3.5.7 POEG and GPT Trigger Timings

Table 3.18 GPT Timing

Item			Symbol	Min.	Max.	Unit	Figures
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	1.5	—	t_{p1cyc}*1	**Figure 3.24**
		Both-edge setting		2.5	—		

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF

Note 1. t_{p1cyc} indicates peripheral clock means GPT_PCLK (P0ϕ).

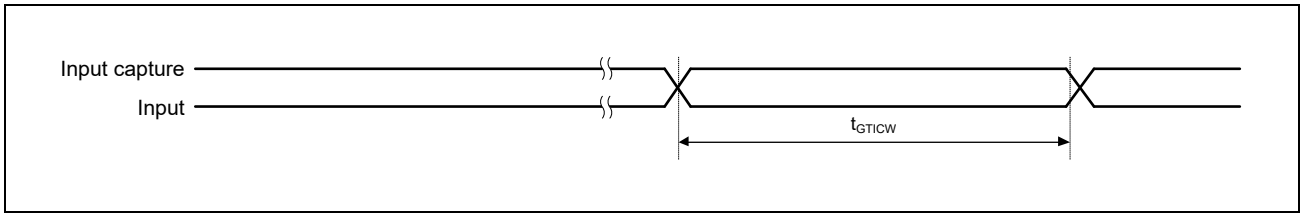


Figure 3.24 GPT Input Capture Input Timing

Table 3.19 POEG Timing

Item		Symbol	Min.	Max.	Unit	Figures
POEG	POEG input pulse width	t_{POEGW}	3	—	t_{p1cyc}*1	**Figure 3.25**

Note 1. t_{p1cyc} indicates peripheral clock means POEG_x_CLKP (P0ϕ) (x = A, B, C, D).

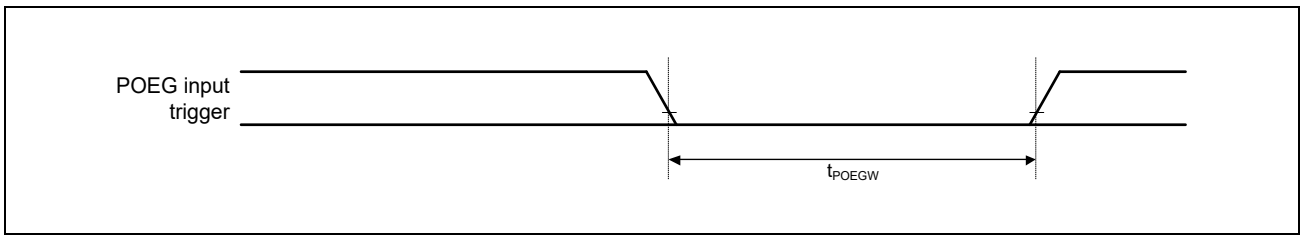


Figure 3.25 POEG Input Trigger Timing

3.5.8 Multi-Function Timer Pulse Unit 3 (MTU3a) Access Timing

Table 3.20 MTU3a Timing

Item			Symbol	Min.	Max.	Unit*1	Figures
MTU3a	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{p1cyc}*1	**Figure 3.26**
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{p1cyc}*1	**Figure 3.27**
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF

Note 1. t_{p1cyc} indicates peripheral clock means MTU_X_MCLK_MTU3 (P0ϕ).

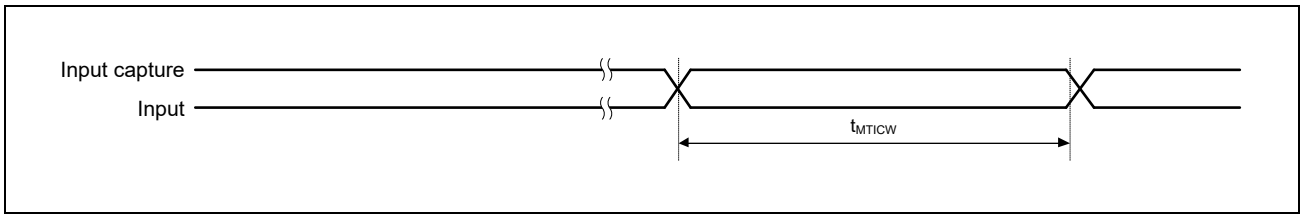


Figure 3.26 MTU3a Input Capture Input Timing

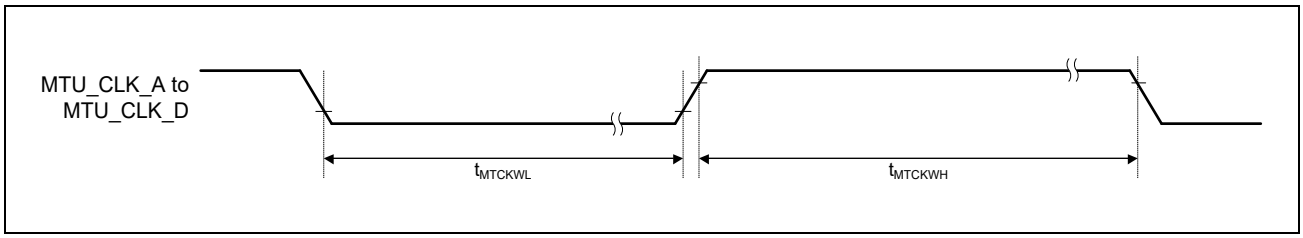


Figure 3.27 MTU3a Clock Input Timing

3.5.9 POE3 Access Timing

Table 3.21 POE3 Timing

Item		Symbol	Min.	Max.	Unit	Figures
POE3	POEn# input pulse width	t_{POE3W}	1.5	—	t_{p1cyc}*1	**Figure 3.28**

Note 1. t_{p1cyc} indicates peripheral clock means POE3_CLKM_POE (P0ϕ).

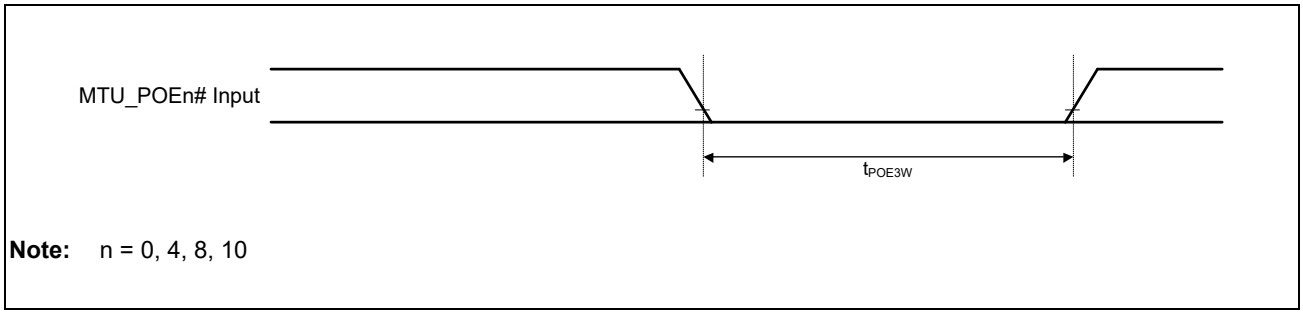


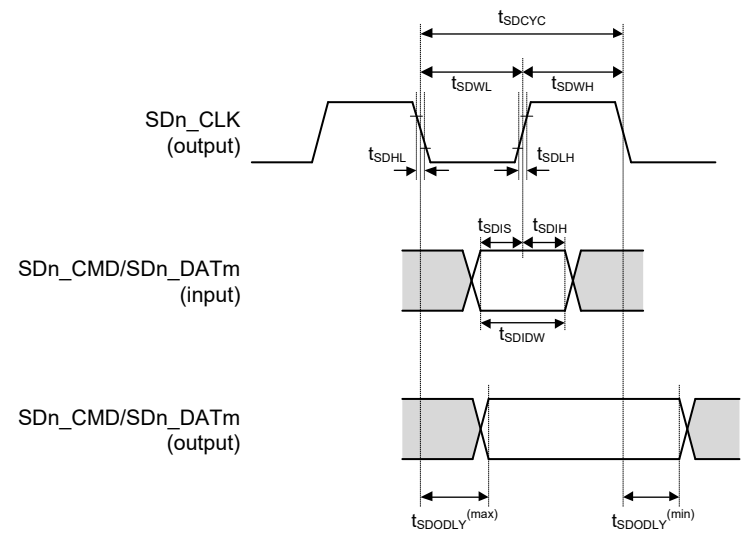
Figure 3.28 POEn# Input Pulse Timing

3.5.10 SD Access Timing

3.5.10.1 SD Access Timing (SDR 3.3-V)

Table 3.22 SD AC Access Timing (SDR at 3.3-V Operation)

Item	Symbol	Default Speed Mode (18.75 MHz)		High Speed Mode (37.5 MHz)		Unit	Figures
		Min.	Max.	Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	53.33	—	26.66	—	ns	**Figure 3.29**
SDnCLK clock high level width	t_{SDWH}	25	—	12.5	—	ns	
SDnCLK clock low level width	t_{SDWL}	25	—	12.5	—	ns	
SDnCLK clock rise time	t_{SDLH}	—	10	—	3	ns	
SDnCLK clock fall time	t_{SDHL}	—	10	—	3	ns	
SDnCMD,SDnDATm output delay	t_{SDODLY}	−7.5	2.5	−6.2	2.5	ns	
SDnCMD,SDnDATm input set up time	t_{SDIS}	4.0	—	4.0	—	ns	
SDnCMD,SDnDATm input hold time	t_{SDIH}	2.0	—	2.0	—	ns	



Note: n = 0 to 2, m = 0 to 3

Figure 3.29 SDHC Interface Timing (SDR 3.3-V Power Supply)

NOTE

The disclosure of other characteristics of the SD interface needs the conclusion of the following agreement.

- SD Host/Ancillary Product License Agreement (SD HALA)

For details, contact Renesas sales representatives.

3.5.11 eMMC Access Timing

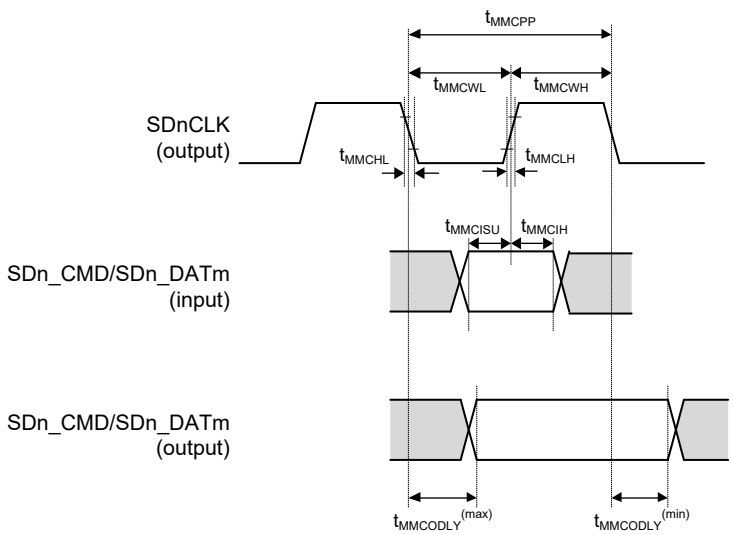
3.5.11.1 eMMC Host Interface Timing (Default)

Table 3.23 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	53.33	—	ns	**Figure 3.30**
SDnCLK clock high level width	t_{MMCWH}	25	—	ns	
SDnCLK clock low level width	t_{MMCWL}	25	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	10	ns	
SDnCLK clock fall time	t_{MMCHL}	—	10	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−7.5	2.5	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	4.0	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	2.0	—	ns	

Table 3.24 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	53.33	—	ns	**Figure 3.30**
SDnCLK clock high level width	t_{MMCWH}	25	—	ns	
SDnCLK clock low level width	t_{MMCWL}	25	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	2.66	ns	
SDnCLK clock fall time	t_{MMCHL}	—	2.66	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−4.30	1.90	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	3.40	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	1.40	—	ns	



Note: n = 0 to 1, m = 0 to 7 (n = 0), m = 0 to 3 (n = 1)

Figure 3.30 eMMC Host Interface Timing (MMC Default 1.8-V/3.3-V Power Supply)

3.5.11.2 eMMC Host Interface Timing (HS-SDR)

Table 3.25 eMMC Host Interface Timing (HS-SDR at 3.3-V Operation)

Item	Symbol	High Speed Mode (37.5 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{MMCPP}	26.66	—	ns	**Figure 3.30**
SDnCLK clock high level width	t_{MMCWH}	12.5	—	ns	
SDnCLK clock low level width	t_{MMCWL}	12.5	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3	ns	
SDnCMD,SDnDATm output delay	$t_{MMCODLY}$	−6.2	2.5	ns	
SDnCMD,SDnDATm input set up time	t_{MMCISU}	4.0	—	ns	
SDnCMD,SDnDATm input hold time	t_{MMCIH}	2.0	—	ns	

Table 3.26 eMMC Host Interface Timing (HS-SDR at 1.8-V Operation)

Item	Symbol	High Speed Mode (37.5 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{MMCPP}	26.66	—	ns	**Figure 3.30**
SDnCLK clock high level width	t_{MMCWH}	12.5	—	ns	
SDnCLK clock low level width	t_{MMCWL}	12.5	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	2.66	ns	
SDnCLK clock fall time	t_{MMCHL}	—	2.66	ns	
SDnCMD,SDnDATm output delay	$t_{MMCODLY}$	−4.30	1.90	ns	
SDnCMD,SDnDATm input set up time	t_{MMCISU}	3.40	—	ns	
SDnCMD,SDnDATm input hold time	t_{MMCIH}	1.40	—	ns	

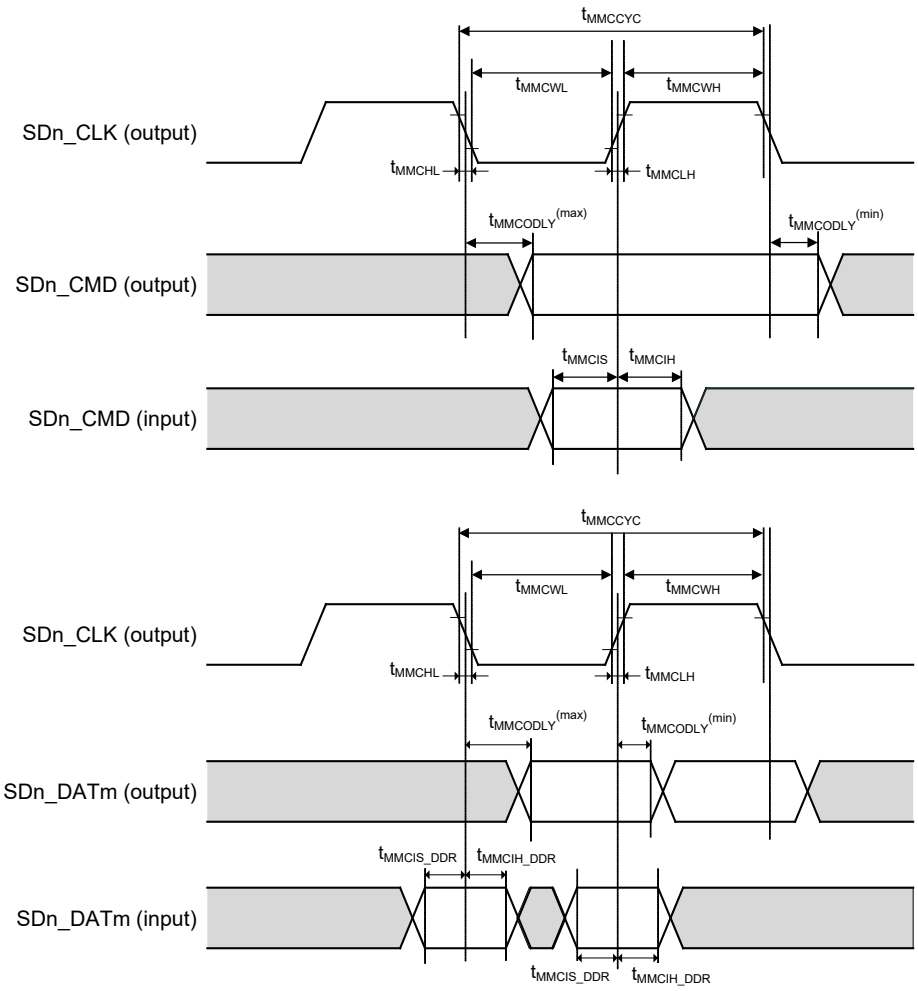
3.5.11.3 eMMC Host Interface Timing (HS-DDR)

Table 3.27 eMMC Host Interface Timing (HS-DDR 3.3-V Power Supply Operation)

Item	Symbol	High Speed Mode (37.5 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	26.66	—	ns	**Figure 3.31**
SDnCLK clock high level width	t_{SDWH}	12.0	14.66	ns	
SDnCLK clock low level width	t_{SDWL}	12.0	14.66	ns	
SDnCLK clock rise time	t_{SDLH}	—	3.0	ns	
SDnCLK clock fall time	t_{SDHL}	—	3.0	ns	
SDnCMD output delay	t_{SDODLY}	−6.6	6.6	ns	
SDnCMD input set up time	t_{SDIS}	5.5	—	ns	
SDnCMD input hold time	t_{SDIH}	2.3	—	ns	
SDnDATm output delay	t_{SDODLY_DDR}	2.3	8.5	ns	
SDnDATm input set up time	t_{SDIS_DDR}	2.4	—	ns	
SDnDATm input hold time	t_{SDIH_DDR}	1.3	—	ns	

Table 3.28 eMMC Host Interface Timing (HS-DDR 1.8-V Power Supply Operation)

Item	Symbol	High Speed Mode (37.5 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{MMCCYC}	26.66	—	ns	**Figure 3.31**
SDnCLK clock high level width	t_{MMCWH}	12.0	14.66	ns	
SDnCLK clock low level width	t_{MMCWL}	12.0	14.66	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3.0	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3.0	ns	
SDnCMD output delay	$t_{MMCODLY}$	−6.6	5.5	ns	
SDnCMD input set up time	t_{MMCIS}	5.5	—	ns	
SDnCMD input hold time	t_{MMCIH}	2.3	—	ns	
SDnDATm output delay	$t_{MMCODLY\_DDR}$	2.3	8.0	ns	
SDnDATm input set up time	t_{MMCIS_DDR}	3.8	—	ns	
SDnDATm input hold time	t_{SMMCIH_DDR}	1.3	—	ns	



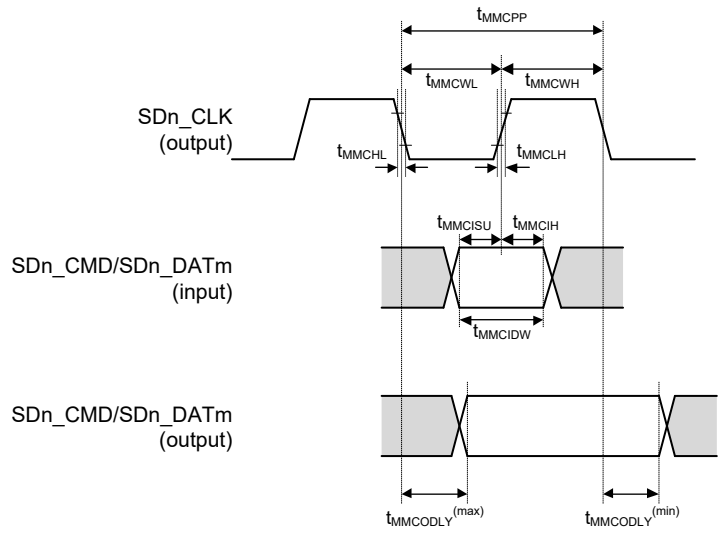
Note: n = 0 to 1, m = 0 to 7 (n = 0), m = 0 to 3 (n = 1))

Figure 3.31 eMMC Host Interface (MMC Interface HS-DDR Mode 1.8/3.3-V Power Supply Selection)

3.5.11.4 eMMC Host Interface Timing (HS200)

Table 3.29 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	6.66	13.33	ns	**Figure 3.32**
SDnCLK clock high level width	t_{MMCWH}	2.66	—	ns	
SDnCLK clock low level width	t_{MMCWL}	2.66	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	1.33	ns	
SDnCLK clock fall time	t_{MMCHL}	—	1.33	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−1.6	0.85	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	—	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	—	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	3.83	—	ns	



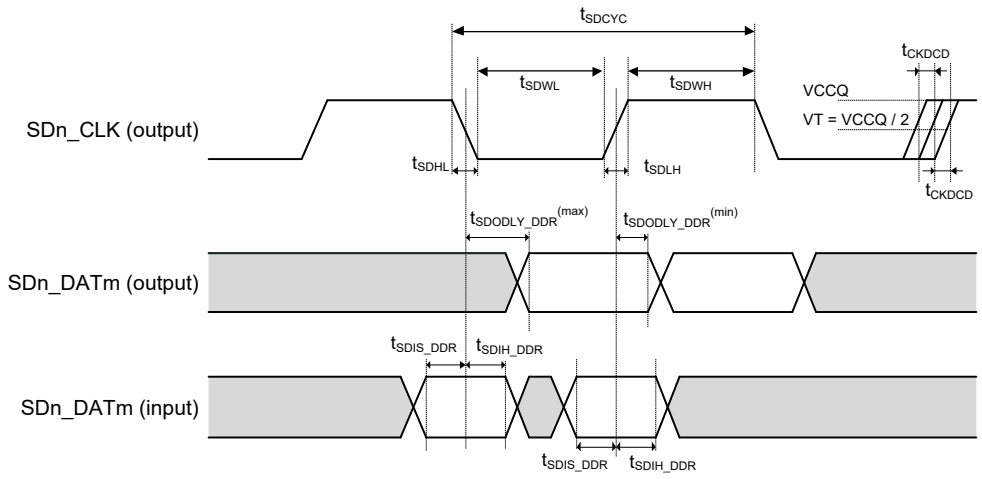
Note: n = 0 to 1, m = 0 to 7 (n = 0), m = 0 to 3 (n = 1)

Figure 3.32 eMMC Host Interface (MMC Interface HS200 Mode 1.8-V Power Supply Selection)

3.5.11.5 eMMC Host Interface Timing (HS400)

Table 3.30 eMMC Host Interface Timing (HS400 1.8-V Power Supply Operation, Output Load 15 pF)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{SDCYC}	6.66	—	ns	**Figure 3.33**
SDnCLK clock high level width	t_{SDWH}	3.00	—	ns	
SDnCLK clock low level width	t_{SDWL}	3.00	—	ns	
SDnCLK duty cycle distortion	t_{CKDCD}	0.00	0.3	ns	
SDnCLK clock rise time	t_{SDLH}	—	0.48	ns	
SDnCLK clock fall time	t_{SDHL}	—	0.48	ns	
SDnCMD output delay	t_{SDODLY}	−2.50	1.60	ns	
SDnDATm output delay	t_{SDODLY_DDR}	0.20	2.15	ns	



Note: n = 0, m = 0 to 7

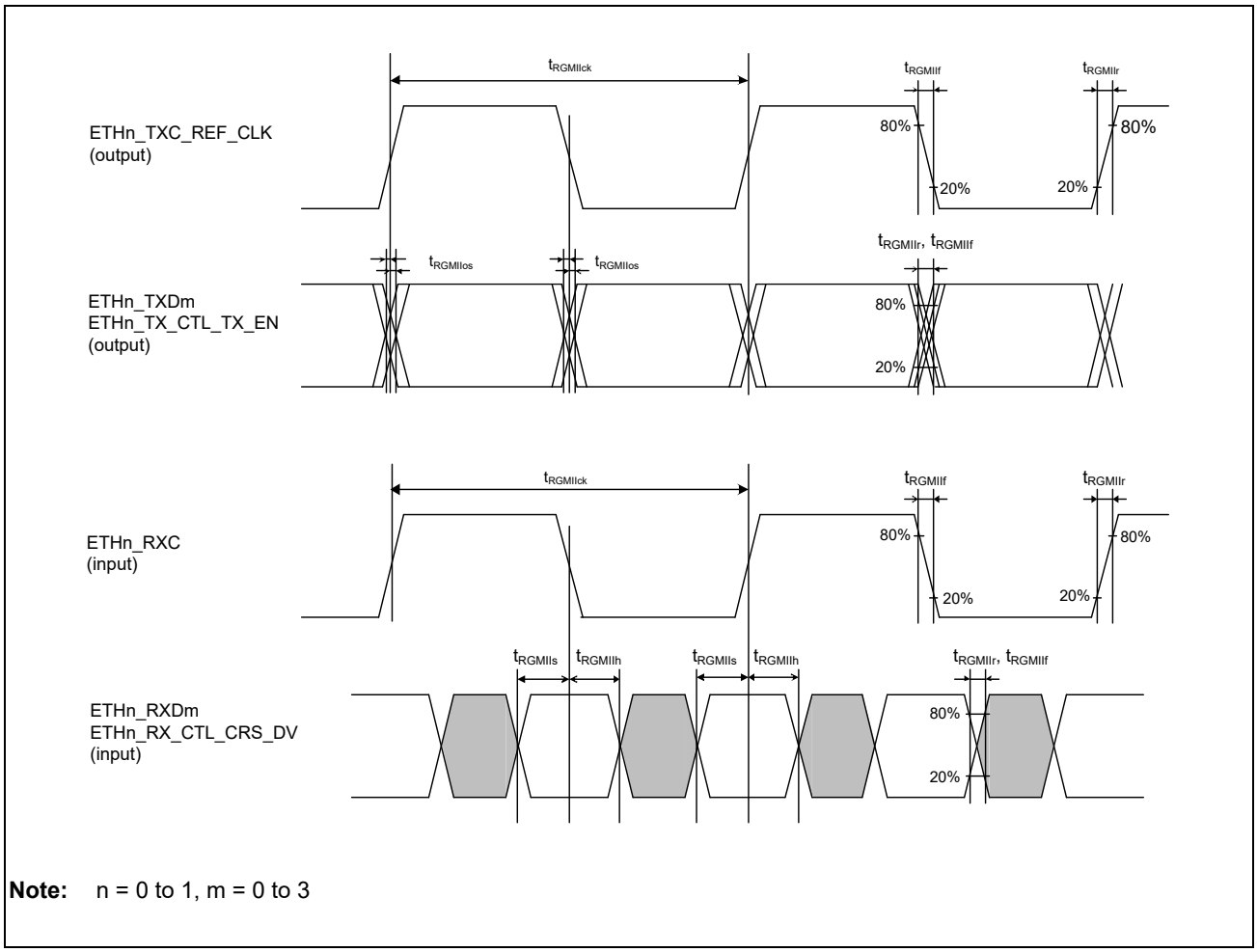
Figure 3.33 eMMC Host Interface (MMC Interface H400 Mode 1.8-V Power Supply Selection)

3.5.12 Ethernet Interface Timing

Table 3.31 Ethernet Interface Timing (n = 0, 1)

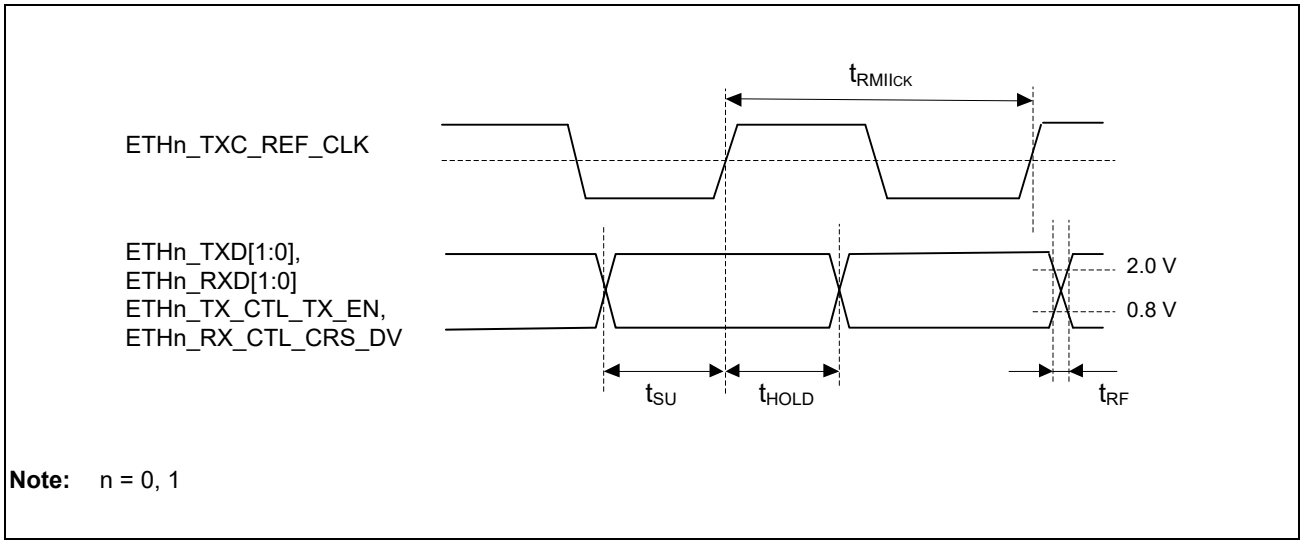
Parameter			Symbol	Min.	Max.	Unit	Figure
Ethernet (RGMII)	ETHn_TXC_REF_CLK, ETHn_RXC cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	**Figure 3.34**
		100 Mbps	$t_{RGMIIck}$	36	44	ns	
		10 Mbps	$t_{RGMIIck}$	360	440	ns	
	ETHn_TXC_REF_CLK, ETHn_RXC frequency	1 Gbps	—	125 − 50 ppm	125 + 50 ppm	MHz	
		100 Mbps	—	25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps	—	2.5 − 50 ppm	2.5 + 50 ppm	MHz	
	ETHn_REF_CLK, ETHn_RXC duty cycle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps	—	40	60	%	
	ETHn_TXC_REF_CLK, ETHn_TXD0 to ETHn_TXD3, ETHn_TX_CTL_TX_EN, ETHn_RXC, ETHn_RXD0 to ETHn_RXD3, ETHn_RX_CTL_CRS_DV rise/fall time		t_{RGMIIr}, t_{RGMIIf}	—	0.75	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TX_CTL_TX_EN, ETHn_TXC_REF_CLK output skew		$t_{RGMIIos}$	−0.5	0.5	ns	
	ETHn_RXD0 to ETn_RXD3, ETHn_RX_CTL_CRS_DV setup time		t_{RGMIIs}	1	—	ns	
	ETHn_RXD0 to ETn_RXD3, ETHn_RX_CTL_CRS_DV hold time		t_{RGMIIh}	1	—	ns	
Ethernet (RMII)	ETHn_TXC_REF_CLK frequency		t_{RMIIck}	50 − 50 ppm	50 + 50 ppm	MHz	**Figure 3.35**
	ETHn_TXC_REF_CLK ducy cycle		—	35	65	%	
	ETHn_TXD[1:0], ETHn_RXD[1:0], ETHn_TX_CTL_TX_EN, ETHn_RX_CTL_CRS_DV data setup to ETHn_TXC_REF_CLK rising edge		t_{SU}	1	20	ns	
	ETHn_TXD[1:0], ETHn_RXD[1:0], ETHn_TX_CTL_TX_EN, ETHn_RX_CTL_CRS_DV data hold from ETHn_TXC_REF_CLK rising edge		t_{HOLD}	10	—	ns	
	rise and fall time		t_{rf}	10	—	ns	

Note: AC access timing condition: output load 8 pF(RGMII) / 25 pF(RMII)



Note: n = 0 to 1, m = 0 to 3

Figure 3.34 RGMII Transmission and Reception Timing



Note: n = 0, 1

Figure 3.35 RMII Transmission and Reception Timing

3.5.13 USB 2.0 Host/Function Module Access Timing

3.5.13.1 USB 2.0 Low-Speed Access Timing

Table 3.32 USB Transceiver Timing (Low-Speed)

Item	Symbol	Min.	Max.	Unit	Figures
Rise time	t_{LR}	75	300	ns	**Figure 3.36**
Fall time	t_{LF}	75	300	ns	
Rise/fall time lag	t_{LR}/t_{LF}	80	125	%	

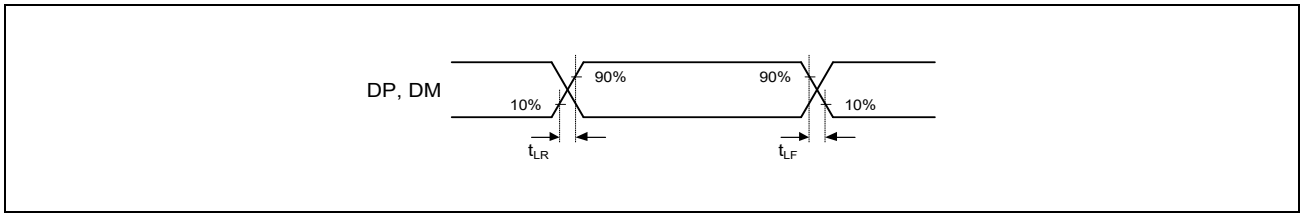


Figure 3.36 USB20_DP, USB21_DP, USB20_DM, and USB21_DM Output Timing (Low-Speed)

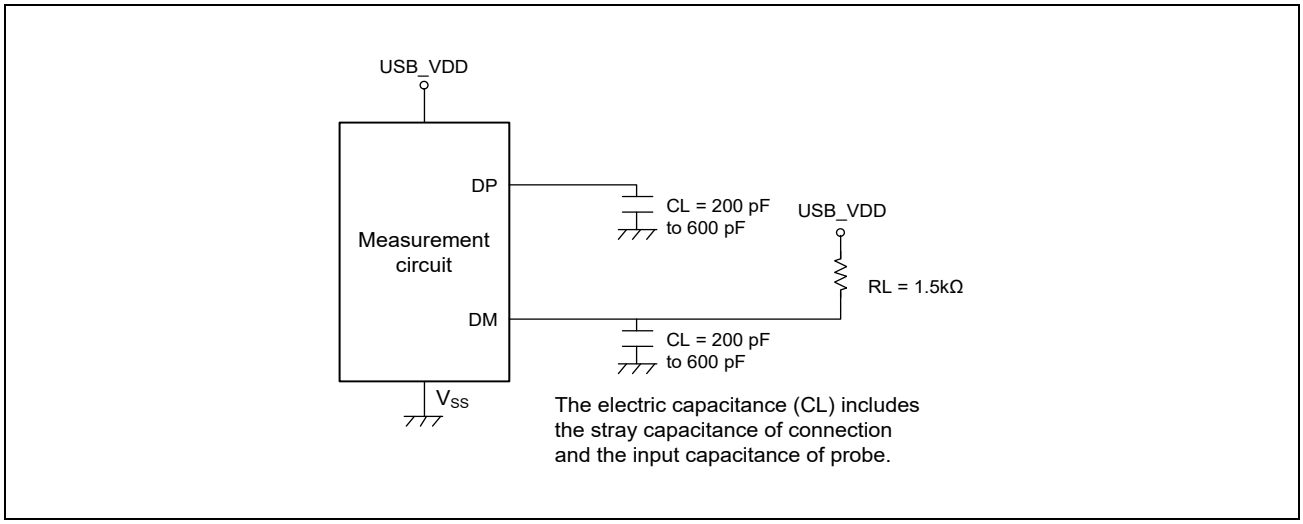


Figure 3.37 Measurement Circuit (Low-Speed)

3.5.13.2 USB 2.0 Full-Speed Access Timing

Table 3.33 USB Transceiver Timing (Full-Speed)

Item	Symbol	Min.	Max.	Unit	Figures
Rise time	t_{FR}	4	20	ns	**Figure 3.38**
Fall time	t_{FF}	4	20	ns	
Rise/fall time lag	t_{FR}/t_{FF}	90	111.11	%	

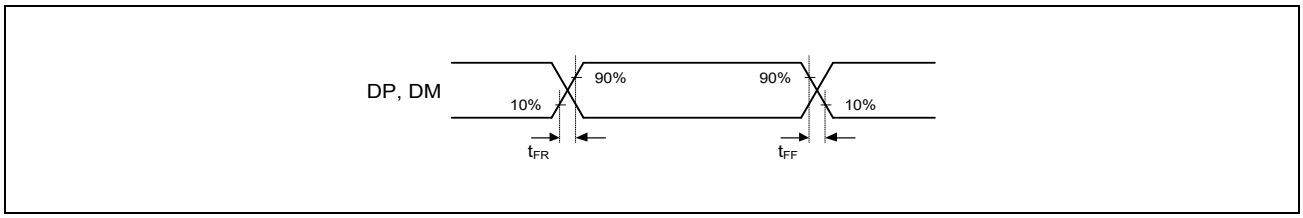


Figure 3.38 USB20_DP, USB21_DP, USB20_DM, and USB21_DM Output Timing (Full-Speed)

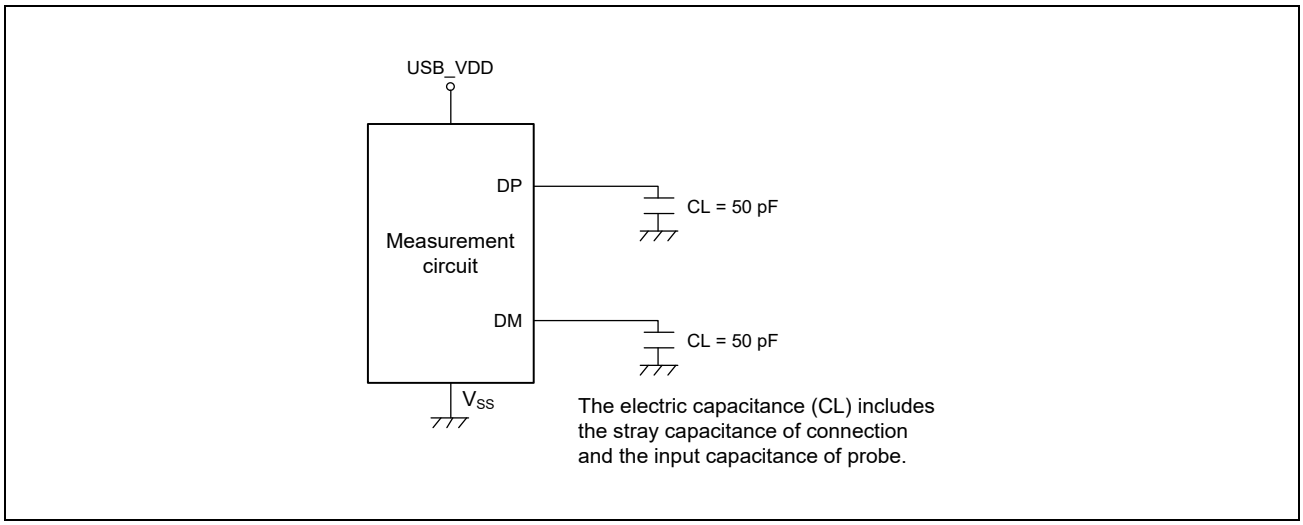


Figure 3.39 Measurement Circuit (Full-Speed)

3.5.13.3 USB 2.0 Hi-Speed Access Timing

Table 3.34 USB Transceiver Timing (Hi-Speed)

Item	Symbol	Min.	Max.	Unit	Figures
Rise edge rate	t_{HSR}	—	2133	V/µs	**Figure 3.40**
Fall edge rate	t_{HSF}	—	2133	V/µs	
Output driver resistance	Z_{HSDRV}	40.5	49.5	Ω	

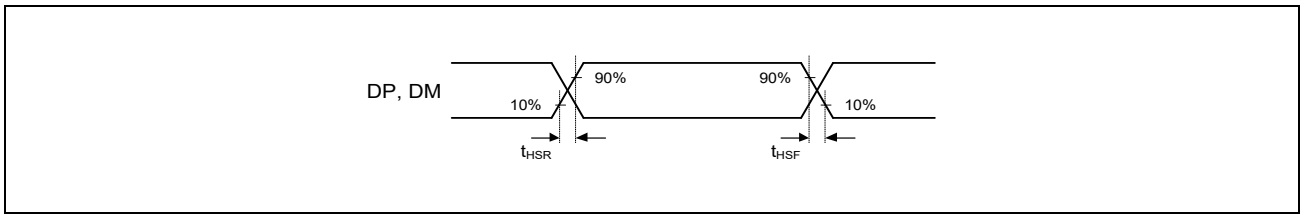


Figure 3.40 USB20_DP, USB21_DP, USB20_DM, and USB21_DM Output Timing (Hi-Speed)

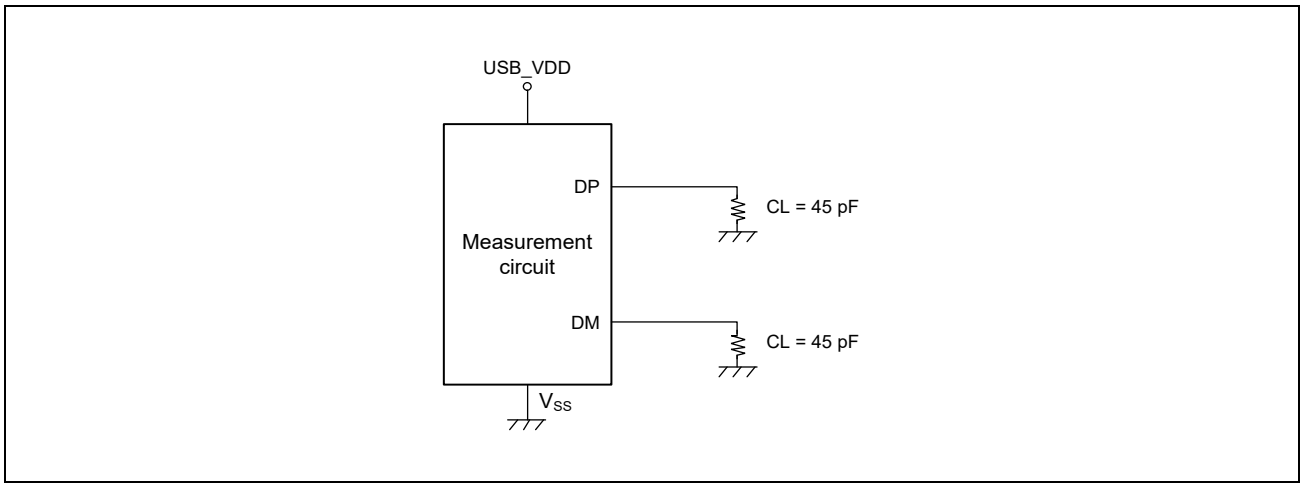


Figure 3.41 Measurement Circuit (Hi-Speed)

3.5.14 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of the PCI Express® Base Specification for Gen1/Gen 2

3.5.15 xSPI Timing

Table 3.35 xSPI Timing

Item		Symbol	1.8 V		3.3 V		Unit	Figures
			Min.	Max.	Min.	Max.		
Clock cycle	SDR	t_{SPBcyc}	10.0	—	15	—	ns	**Figure 3.42**
	DDR		7.5	—	7.5	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56*2	—	1.03*6	—	V/ns	
Clock minimum pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*2	—	1.03*6	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	3.0	—	ns	**Figure 3.43**
Data input hold time (to CK)		t_H	1.0	—	1.0	—	ns	
Data output delay time*3	SDR	t_{OD}	—	2.3	—	2.3	ns	
Data output hold time*3	SDR	t_{OH}	−3.3	—	−3.3	—	ns	
Data output buffer off time	SDR	t_{BOFF}	-3.3	—	−3.3	—	ns	
	DDR		−0.8	—	−0.8	—	ns	
Data input setup time (to DS)	DDR*1,*3	t_{SU}	−0.6/−0.8	—	−0.6/−0.8	—	ns	**Figure 3.44**
Data input hold time (to DS)		t_H	t_{PERIOD} × 0.41 − 0.6/0.8	—	t_{PERIOD} × 0.41 − 0.6/0.8	—	ns	
Data output setup time (to CK)		t_{SUO}	0.8*5	—	0.8*5	—	ns	
Data output hold time (to CK)		t_{HO}	−0.8*5	—	−0.8*5	—	ns	
CS low to clock high*4		t_{CSLCKH}	6.0/8.0*2,*4	—	6.0/8.0	—	ns	**Figure 3.43**, **Figure 3.44**
Clock low to CS high*4		t_{CKLCSH}	6.0/8.0*2	—	6.0/8.0	—	ns	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS low to CS high		t_{DSLCSH}	6.0/8.0*2	—	6.0/8.0	—	ns	**Figure 3.45**
CS high to DS Tri-state		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low*7		t_{CSLDSL}	0.0	12.5*8	0.0	12.5	ns	
DS Tri-state to CS low		t_{DSTCSL}	0.0	—	0.0	—	ns	

Remarks: CK: XSPI_CKP
DS: XSPI_DS
CS: XSPI_CS0#, XSPI_CS1#

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 0_1000b for xSPI200.

Note 2. Specification at 133 MHz / Specification at 100 MHz

Note 3. These are values when the OEN assertion and deassertion are extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1b1) and Output Enable Negating extension bit (COMCFG.OENEGEX = 1b1).

Note 4. These are values when the CS assertion and deassertion are extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1b1) and CS negating extension bit (LIOCFGCSn.CSNEGEX = 1b1).

Note 5. The standard value for xSPI266 is 0.8 ns.

Note 6. When IOLH register is 10b or more.

Note 7. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.

Note 8. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

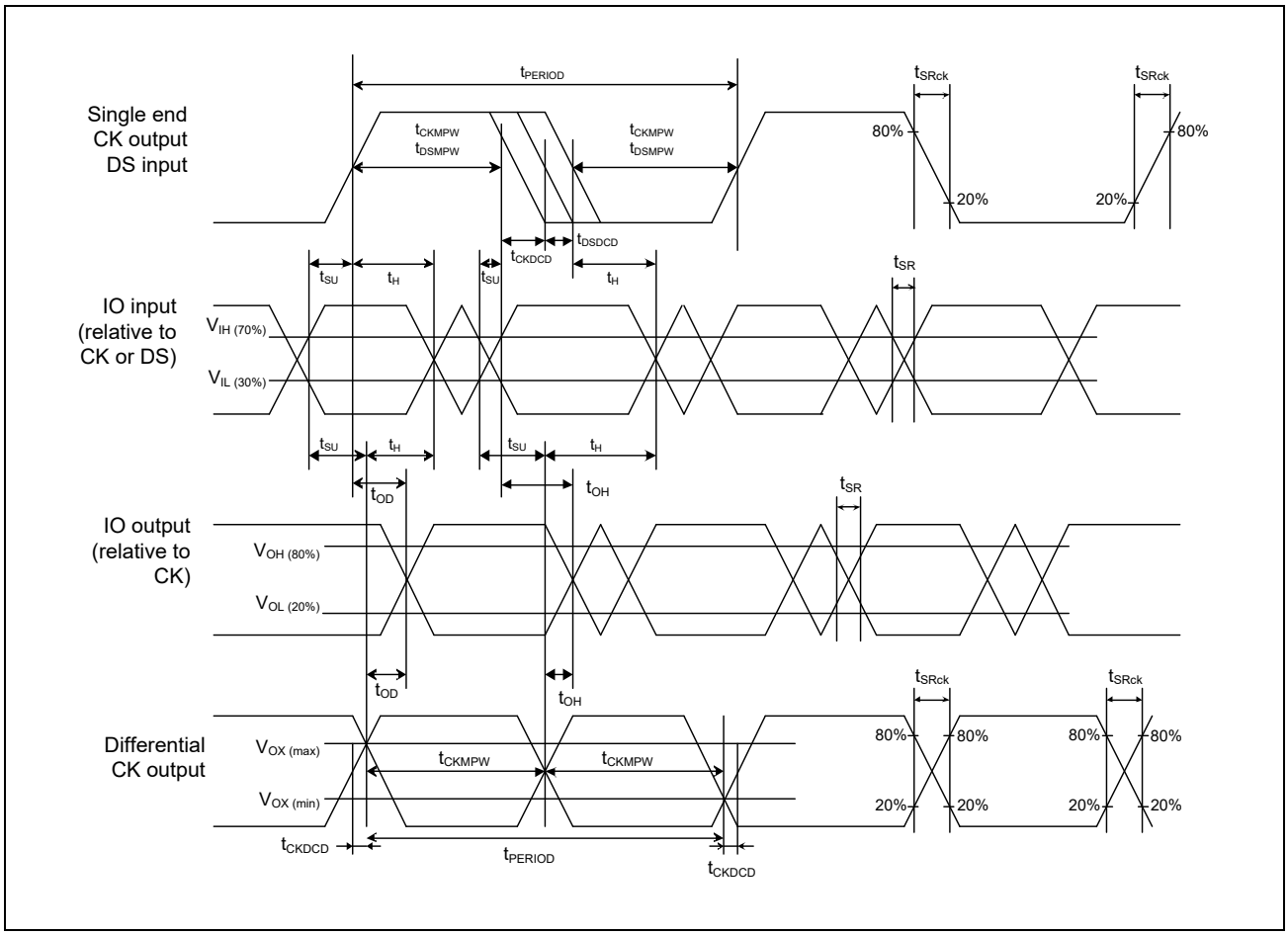
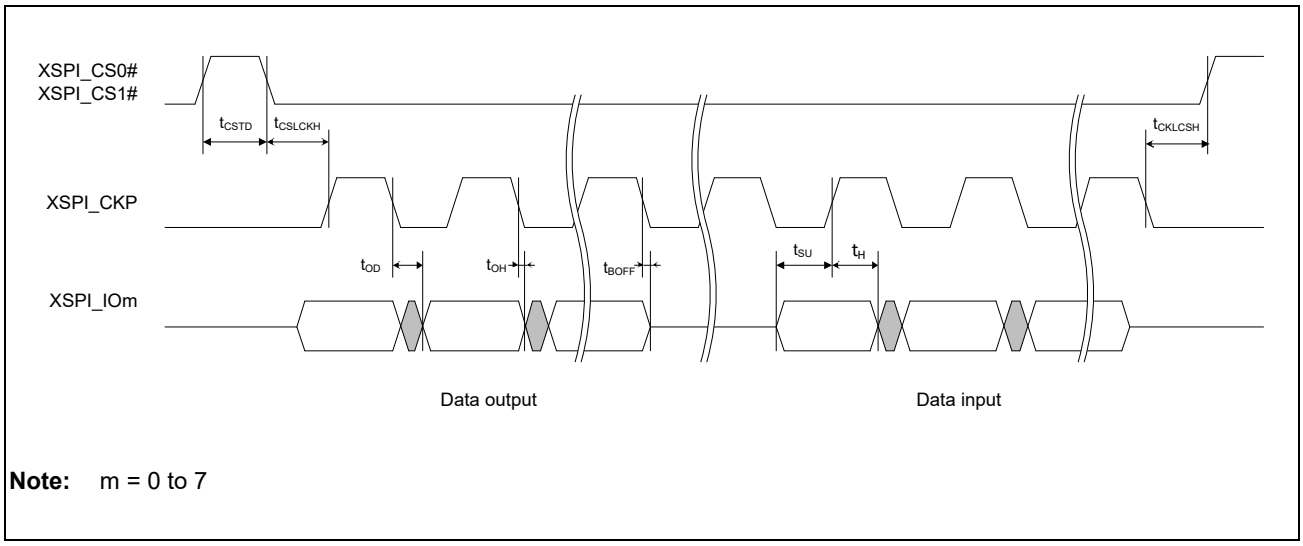
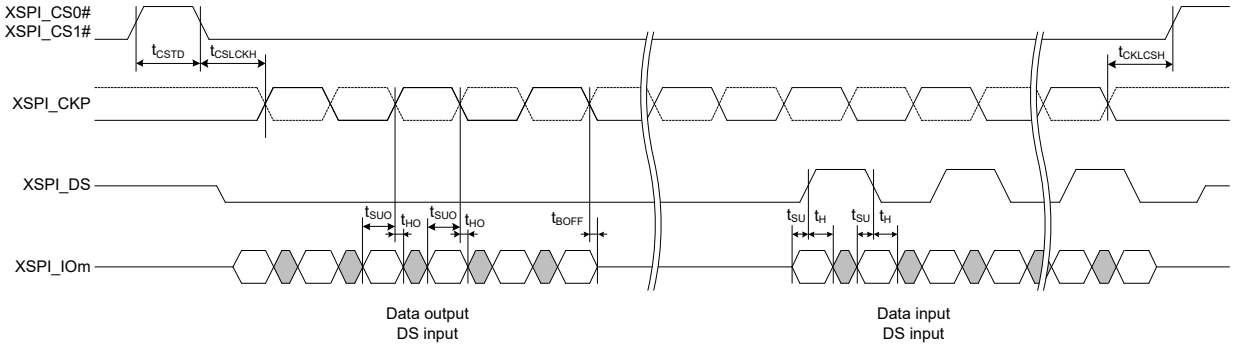


Figure 3.42 XSPI_CKP / XSPI_DS Timing



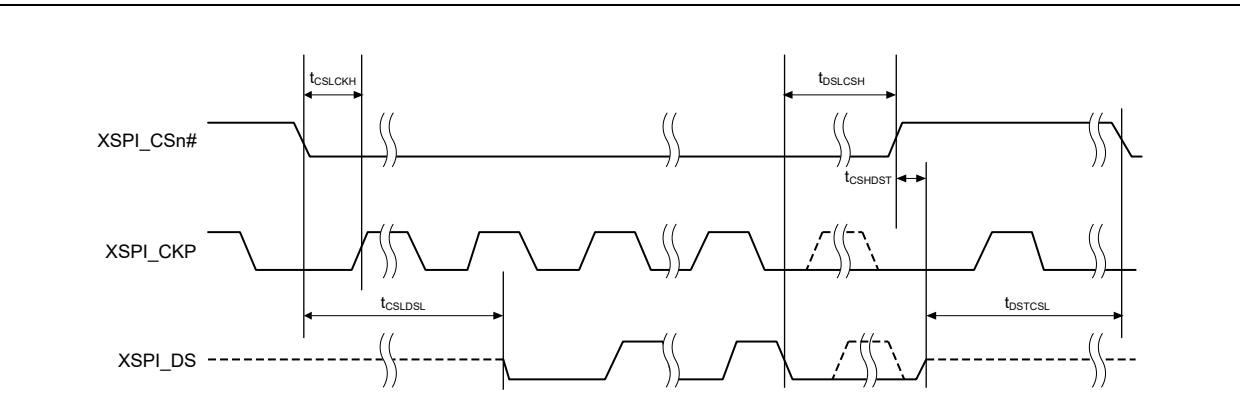
Note: m = 0 to 7

Figure 3.43 SDR Transmit/Receive Timing (1S-1S-1S, 1S-4S-4S, 4S-4S-4S)



Note: m = 0 to 7

Figure 3.44 DDR Transmit/Receive Timing (4S-4D-4D, 8D-8D-8D)



Note: n = 0, 1

Figure 3.45 DS to CS Signal Timing

3.5.16 Serial Communications Interface (RSCI) Access Timing

Table 3.36 RSCI Timing (1/2)

Parameter			Symbol	Min.	Max.	Unit	Figure
RSCI (Asynchronous)	Input clock cycle		t_{Scyc}	4	—	$t_{PSCIcyc}$	**Figure 3.46**
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	3	ns	
	Input clock fall time		t_{SCKf}	—	3	ns	
	Output clock cycle		t_{Scyc}	6	—	$t_{PSCIcyc}$	
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	V_{DD1833} = 1.8 V	t_{SCKr}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Output clock fall time	V_{DD1833} = 1.8 V	t_{SCKf}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
RSCI (Simple I2C, Standard mode)	SDA input rise time		t_{Sr}	—	1000	ns	**Figure 3.47**
	SDA input fall time		t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	2 × NFcyc*1	ns	
	Data input setup time		t_{SDAS}	250	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b	—	400	pF	
RSCI (Simple I2C, Fast mode)	SDA input rise time		t_{Sr}	—	300	ns	**Figure 3.47**
	SDA input fall time		t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	2 × NFcyc*1	ns	
	Data input setup time		t_{SDAS}	100	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b	—	400	pF	

Table 3.36 RSCI Timing (2/2)

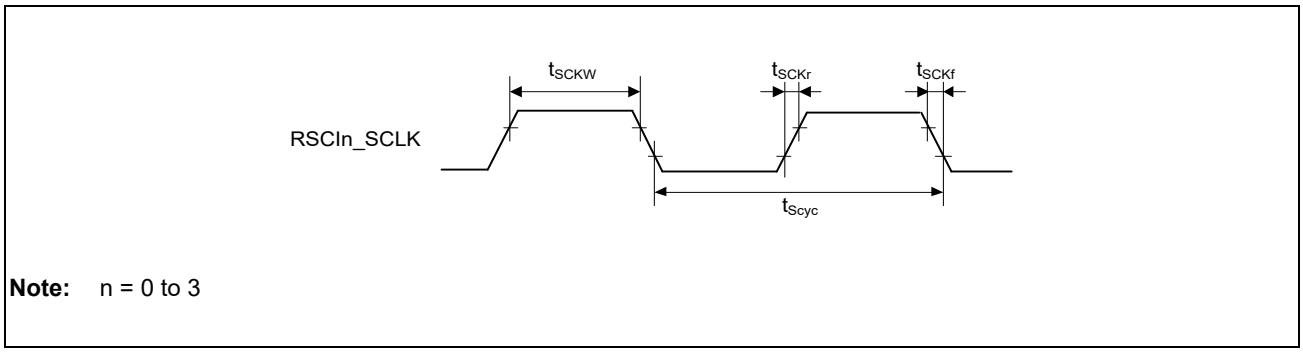
Parameter			Symbol	Min.	Max.	Unit	Figure
RSCI (Clock sync, Simple SPI)	SCK output clock cycle (master)		t_{SPcyc}	4	65536	$t_{PSCIcyc}$	**Figure 3.48** to **Figure 3.53**
	SCK input clock cycle (slave)			4	65536	$t_{PSCIcyc}$	
	SCK clock high-level pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low-level pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKR}, t_{SPCKF}	—	3	ns	
	Data input setup time	Internal clock	t_{SU}	7	—	ns	
		External clock		3	—	ns	
	Data input hold time	Internal clock	t_H	3	—	ns	
		External clock		3	—	ns	
	Data output delay time	Internal clock	t_{OD}	—	3	ns	
		External clock		—	12	ns	
	Data output hold time	Internal clock	t_{OH}	−3	—	ns	
		External clock		0	—	ns	
	Data rise/fall time	V_{DD1833} = 1.8 V	t_{DR}, t_{DF}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Slave access time	Internal clock	t_{SA}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12	ns	
	Slave output release time	Internal clock	t_{REL}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12	ns	
RSCI (Simple SPI)	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	**Figure 3.48** to **Figure 3.53**
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSR}, t_{SSF}	—	3	ns	

Note: AC access timing condition: drive ability IOLH_xx[1:0]=10b, output load 30 pF

Note: $t_{PSCIcyc}$: RSCIn_TCLK cycle (n = 0 to 3)

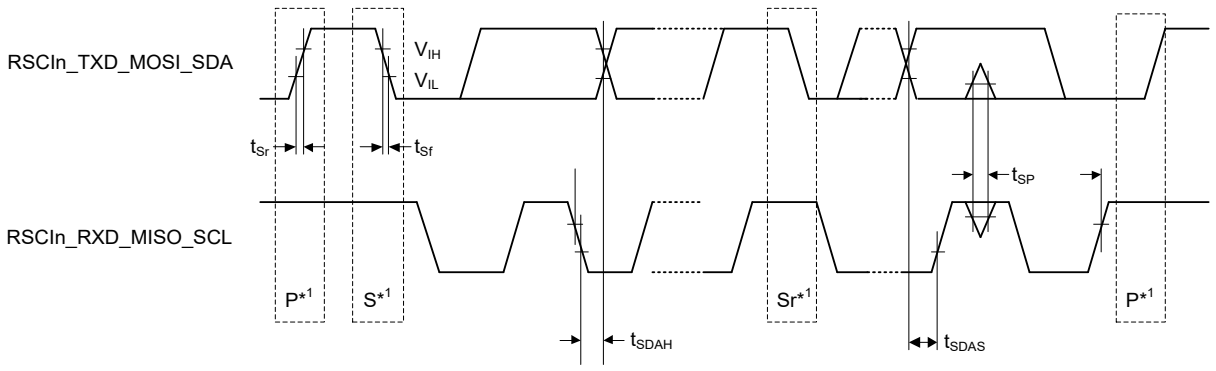
Note 1. NFcyc = 4p × 2q − 1 × $t_{PSCIcyc}$
p: CCR2.CKS[1:0] (p = 0, 1, 2, 3)
q: CCR1.NFCS[2:0] (q = 1, 2, 3, 4)

Note 2. Output transition time from 20% to 80%



Note: n = 0 to 3

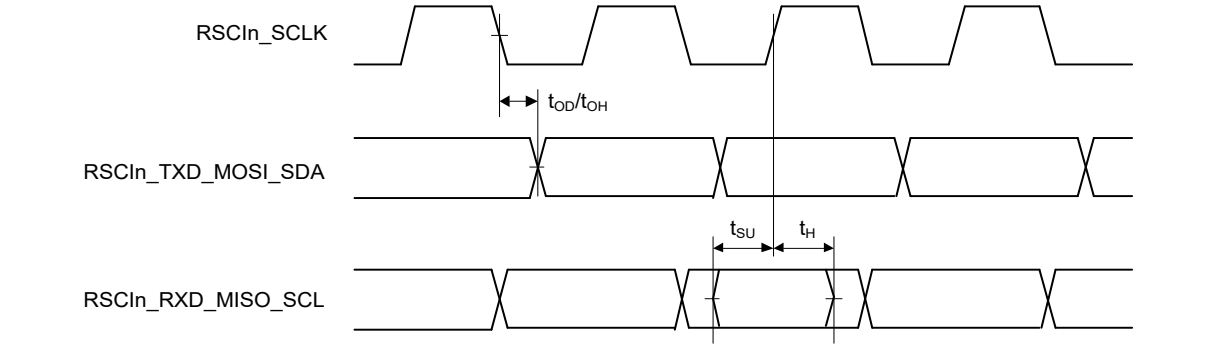
Figure 3.46 SCK Clock Input/Output Timing



Note: n = 0 to 3

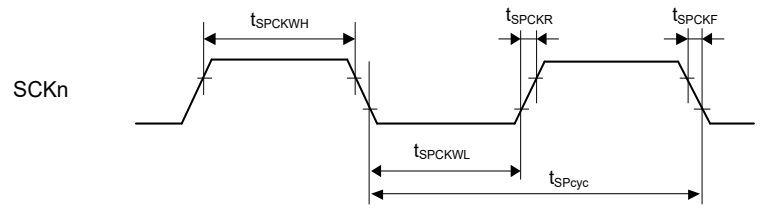
Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 3.47 RSCI Simple I2C Mode Timing



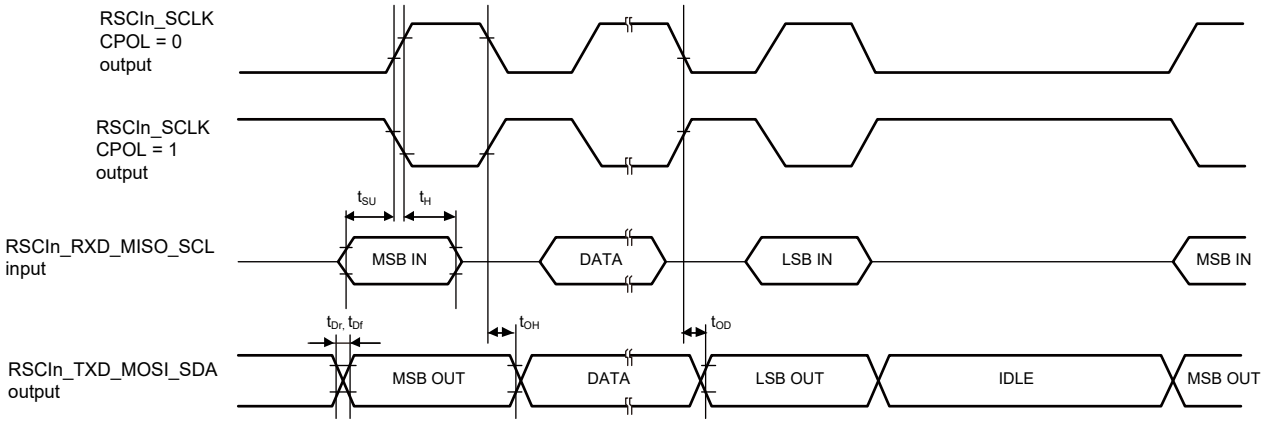
Note: n = 0 to 3

Figure 3.48 RSCI Input/Output Timing in Clock Synchronous Mode



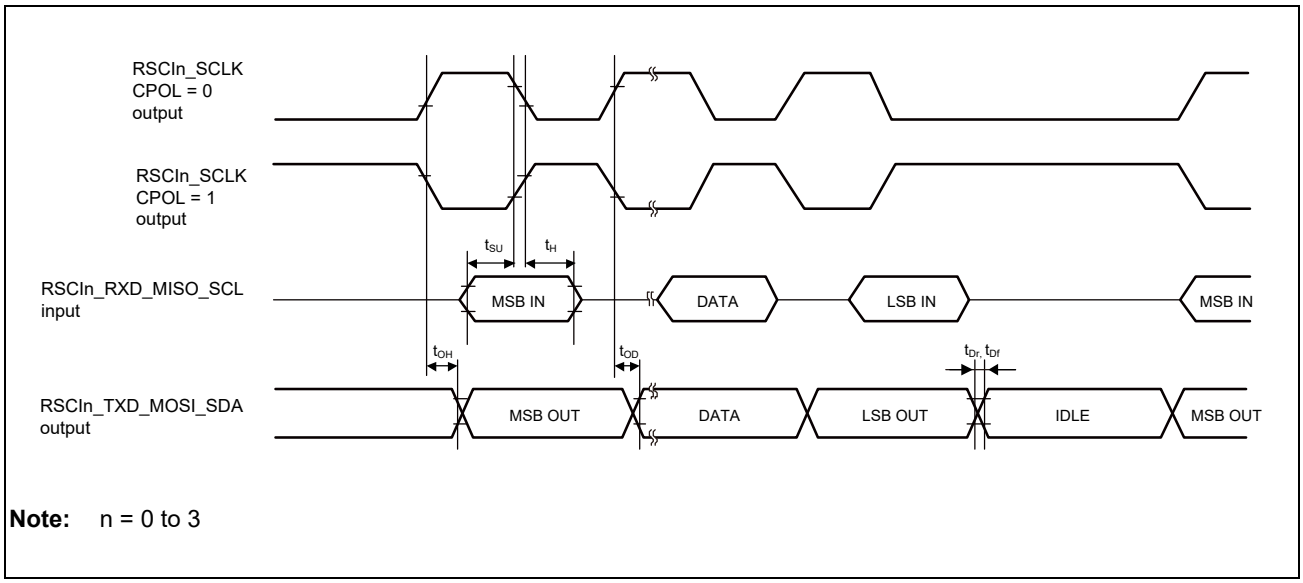
Note: n = 0 to 9

Figure 3.49 RSCI Simple SPI Mode Clock Timing



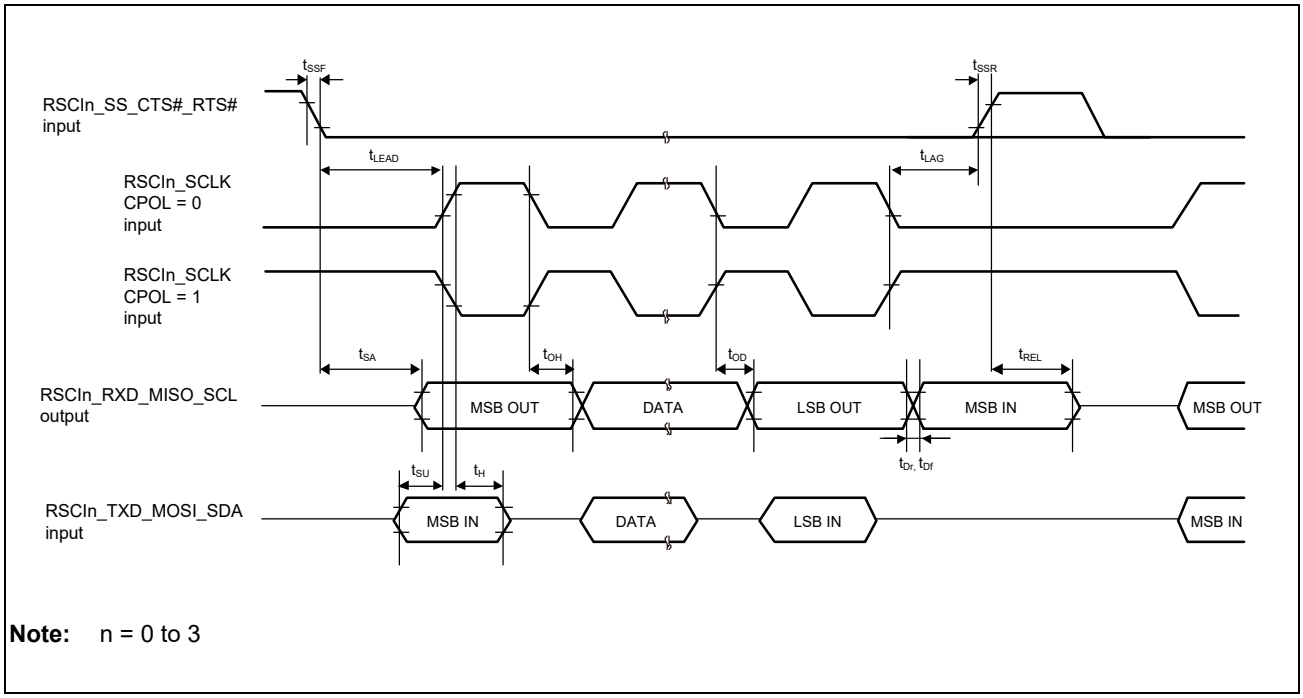
Note: n = 0 to 3

Figure 3.50 RSCI Simple SPI Mode Timing for Master when CPHA = 0



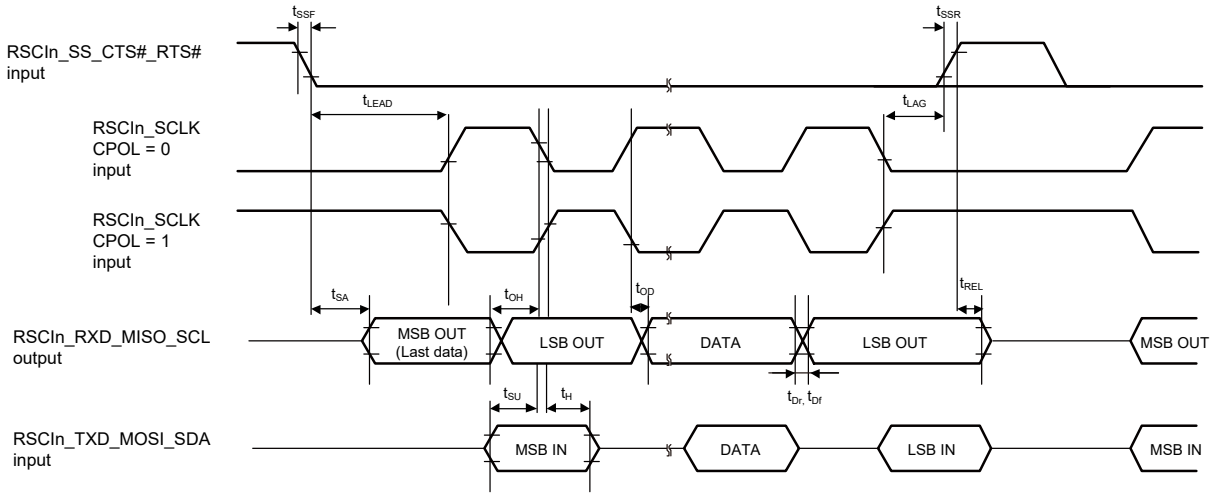
Note: n = 0 to 3

Figure 3.51 RSCI Simple SPI Mode Timing for Master when CPHA = 1



Note: n = 0 to 3

Figure 3.52 RSCI Simple SPI Mode Timing for Slave when CPHA = 0



Note: n = 0 to 3

Figure 3.53 RSCI Simple SPI Mode Timing for Slave when CPHA = 1

3.5.17 Serial Communications Interface with FIFO (SCIFA) Access Timing

Table 3.37 SCIFA Timing

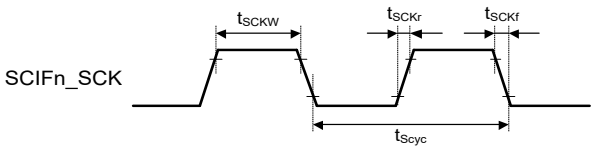
Item			Symbol	Min.	Max.	Unit	Figures
SCIFA	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{p1cyc}*1	**Figure 3.54**
		Clocked synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{p1cyc}*1	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{p1cyc}*1	
		Clocked synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{p1cyc}*1	
	Output clock rise time		t_{SCKr}	—	9	ns	
	Output clock fall time		t_{SCKf}	—	9	ns	
	Transmit data delay time	Internal clock	t_{TXD}	−10	10	ns	**Figure 3.55**
		External clock		3 × t_{p1cyc}*1	4 × t_{p1cyc}*1 + 20		
	Receive data setup time	Internal clock	t_{RXS}	3 × t_{p1cyc}*1 + 20	—	ns	
		External clock		t_{p1cyc}*1 + 10	—		
	Receive data hold time	Internal clock	t_{RXH}	−3 × t_{p1cyc}*1	—	ns	
		External clock		2 × t_{p1cyc}*1 + 10	—		

Note: AC access timing condition: Drive ability IOLH_xx[1:0] = 11b, output load 30 pF.

Note: Max output load is 10pF when connecting SCIF download mode at 1.8V.

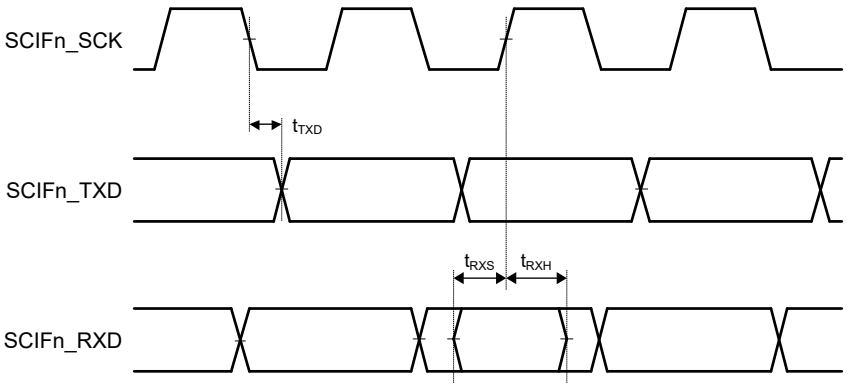
Note 1. t_{p1cyc} indicates peripheral clock means SCIFn_CLK_PCK (P0ϕ) (n = 1 to 5). Channel 0 doesn't support synchronous mode.

Note 2. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1.



Note: n = 1 to 5

Figure 3.54 SCK Input Clock Timing



Note: n = 1 to 5

Figure 3.55 SCIFA Input/Output Timing in Clocked Synchronous Mode

3.5.18 Renesas Serial Peripheral Interface (RSPI) Access Timing

Table 3.38 RSPI Timing

Parameter		Symbol	Min.*1	Max.*1	Unit	Figure
RSPIn_SCK clock cycle	Master	t_{SPcyc}	2/4*8	4096	t_{SPIcyc}	**Figure 3.56**
	Slave		2/4*8	4096	t_{SPIcyc}	
RSPIn_SCK clock high-level pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPIn_SCK clock low-level pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPIn_SCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	3*5	ns	
	Input		—	3*5	ns	
Data input setup time	Master	t_{SU}	5	—	ns	**Figure 3.57** to **Figure 3.63**
	Slave		3 / 5*6	—	ns	
Data input hold time	Master	t_H	3	—	ns	
	Slave		3	—	ns	
SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc} - 3$ *2	$N \times t_{SPcyc} + 3$ *2	ns	**Figure 3.57** to **Figure 3.60**
	Slave		5	—	t_{SPIcyc}	
SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc} - 3$ *3	$N \times t_{SPcyc} + 3$ *3	ns	
	Slave		5	—	t_{SPIcyc}	
Continuous transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{SPIcyc}$	$8 \times t_{SPcyc} + 2 \times t_{SPIcyc}$	ns	
	Slave		$t_{SPcyc} + 5 \times t_{SPIcyc}$	—	ns	
TI-SSP SS input setup time		t_{TISS}	3	—	ns	**Figure 3.61** to **Figure 3.63**
TI-SSP SS input hold time		t_{TISH}	3	—	ns	
TI-SSP next access time		t_{TIND}	M*4	—	t_{SPIcyc}	
TI-SSP Master SS output delay		t_{TISSOD}	−3	3	ns	
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns	
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns	
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	8.5 / 9.5*6	ns	
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	8.5 / 9.5*6	ns	
SSL Activation to Data Output Delay		t_{OD1}	—	3	ns	**Figure 3.57**
Data output delay time	Master	t_{OD}	—	3	ns	**Figure 3.57** to **Figure 3.63**
	Slave		—	8.5 / 9.5*6	ns	
Data output hold time	Master	t_{OH}	−3	—	ns	
	Slave		3 / 2.5*7	—	ns	
MOSI, MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	3*5	ns	
	Input		—	1	µs	
SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	3*5	ns	**Figure 3.57**, **Figure 3.58**
	Input		—	1	µs	
Slave access time		t_{SA}	—	8 / 9*6	ns	**Figure 3.59**, **Figure 3.60**
Slave output release time		t_{REL}	—	8 / 9*6	ns	

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 11b, output load 30 pF.

Note 1. t_{SPIcyc}: RSPIn_TCLK cycle (n = 0 to 2)

Note 2. N: RSPIm_SPCKD.SCKDL[2:0] set value + 1 (1 to 8)

Note 3. N: RSPIm_SSLND.SLNDL[2:0] set value + 1 (1 to 8)

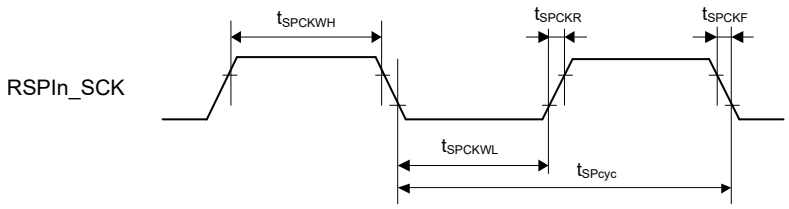
Note 4. M: RSPIm_SSLND.SLNDL[2:0] set value + 2 (2 to 9)

Note 5. Output transition time from 20% to 80%

Note 6. This value is applied to P3x, PHx, P6x, P7x and P8x pins.

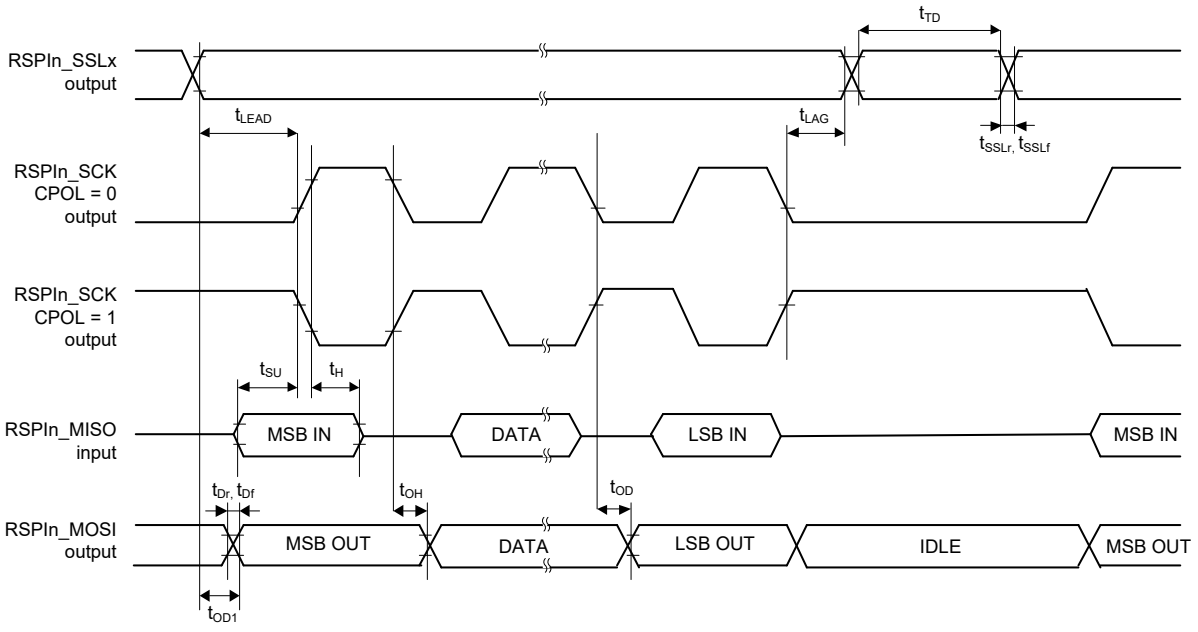
Note 7. This value is applied to PLx, PDx, PHx, P5x and PEx pins.

Note 8. This value is applied when RSPIn_TCLK is over 100 MHz.



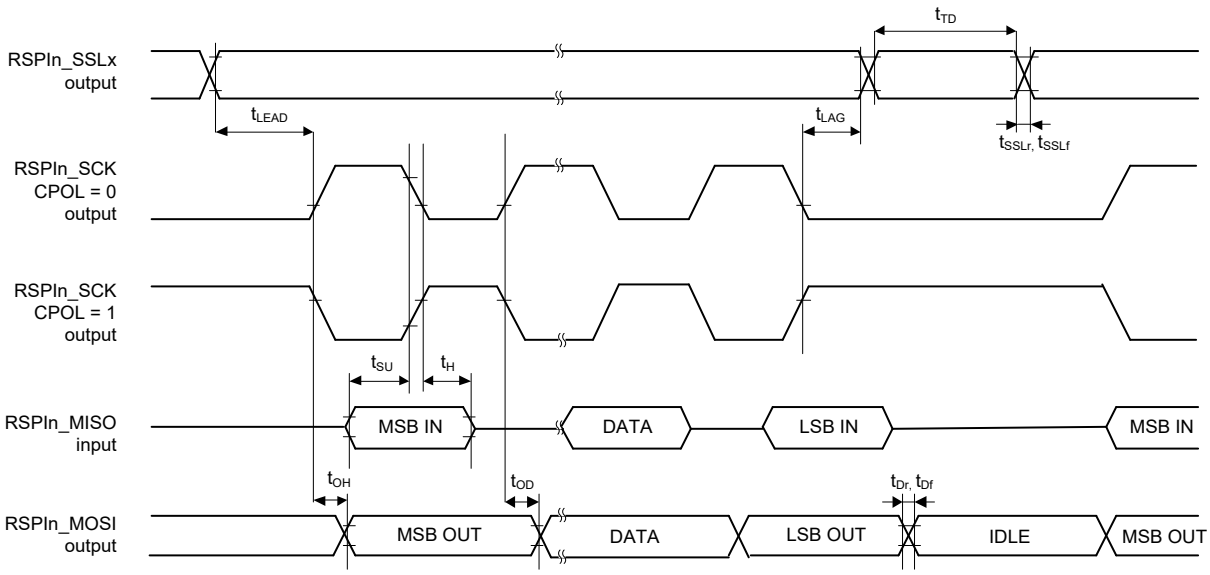
Note: n = 0 to 2

Figure 3.56 RSPI Clock Timing



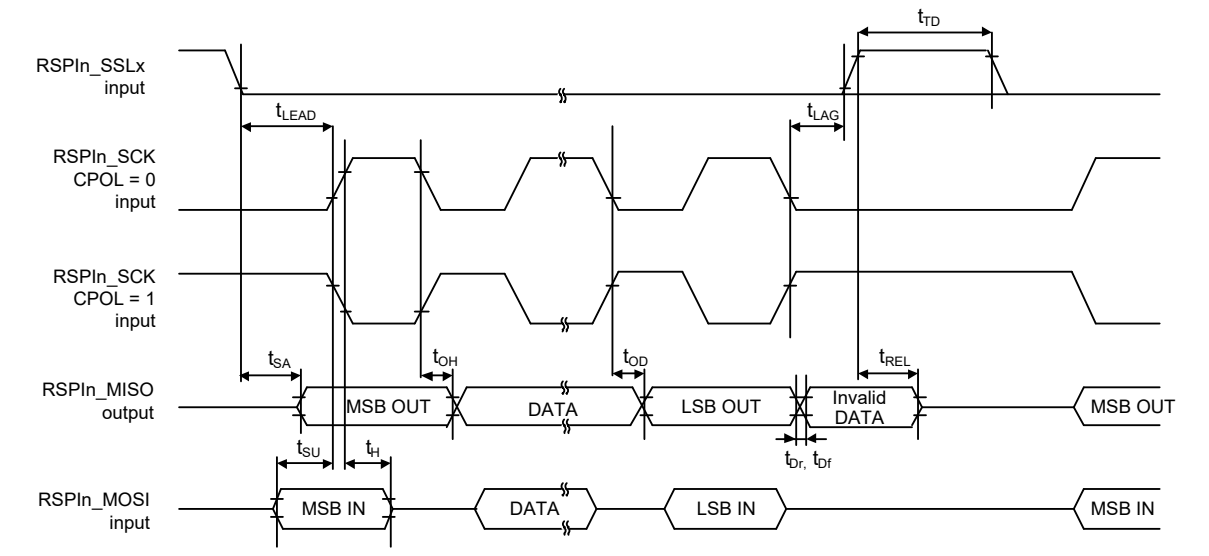
Note: n = 0 to 2
x = A, B, C, D

Figure 3.57 RSPI Timing (Master, Motorola RSPI, CPHA = 0)



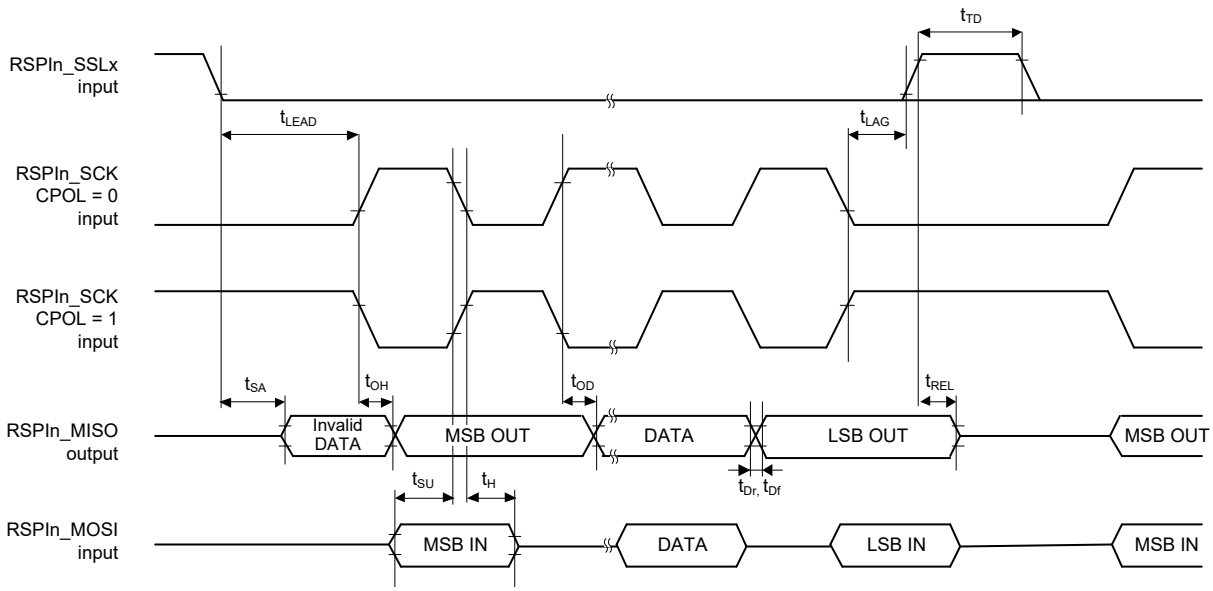
Note: n = 0 to 2
x = A, B, C, D

Figure 3.58 RSPI Timing (Master, Motorola RSPI, CPHA = 1)



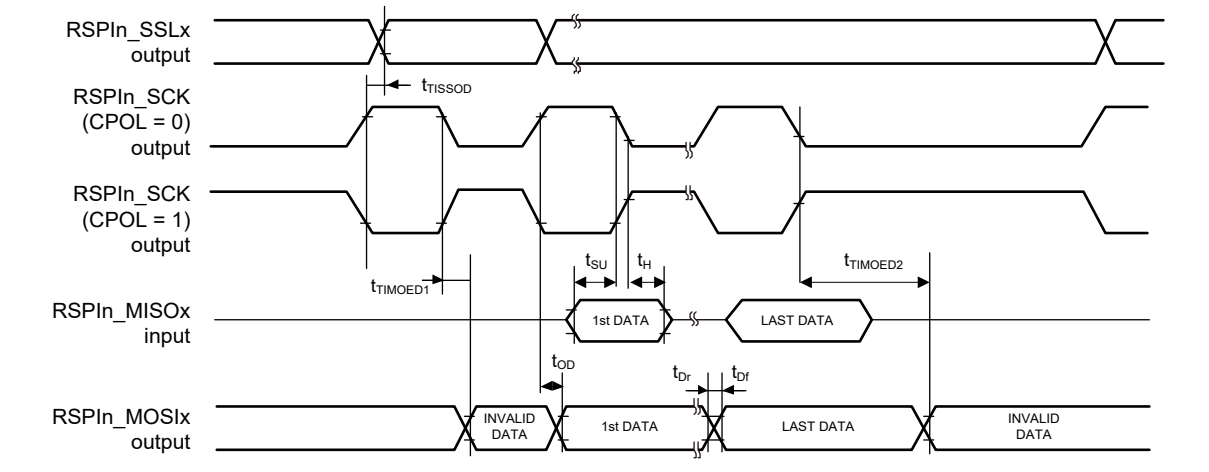
Note: n = 0 to 2
x = A, B, C, D

Figure 3.59 RSPI Timing (Slave, Motorola RSPI, CPHA = 0)



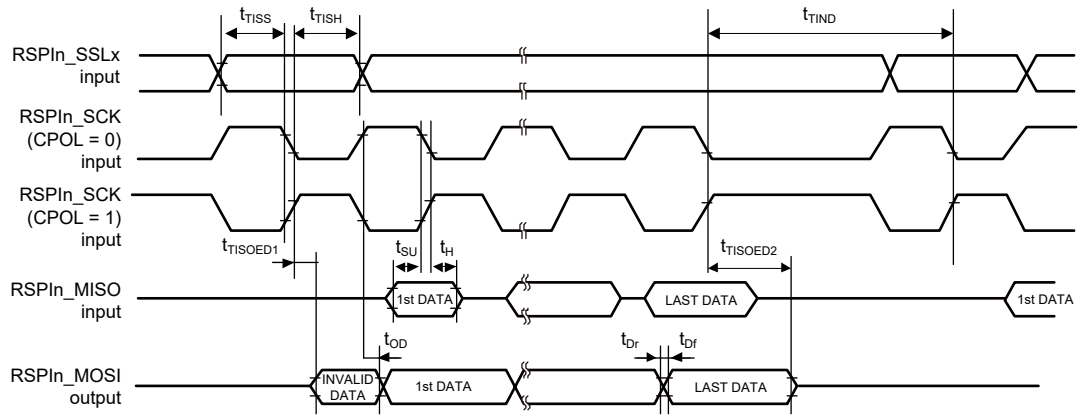
Note: n = 0 to 2
x = A, B, C, D

Figure 3.60 RSPI Timing (Slave, Motorola RSPI, CPHA = 1)



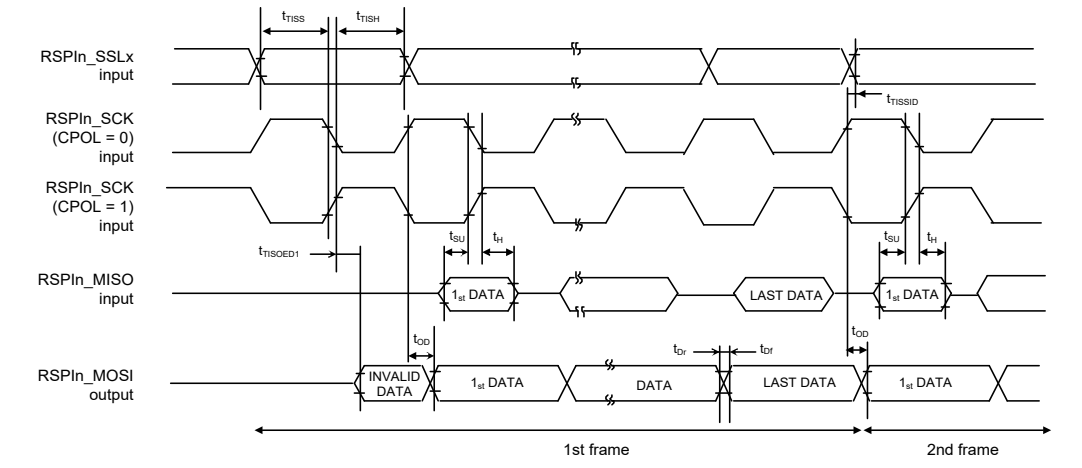
Note: n = 0 to 2
x = A, B, C, D

Figure 3.61 RSPI Timing (Master, TI SSP)



Note: n = 0 to 2
x = A, B, C, D

Figure 3.62 RSPI Timing (Slave, TI-SSP, with delay in burst transfer)



Note: n = 0 to 2
x = A, B, C, D

Figure 3.63 RSPI Timing (Slave, TI-SSP, without delay in burst transfer)

3.5.19 Renesas IIC Bus Interface (RIIC) Access Timing

Table 3.39 I^2C Bus Interface Timing

Item	Symbol	Input/ Output	Standard Mode (Sm)		Fast Mode (Fm)		Fast Mode Plus (Fm+)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{CLK}	I/O	0	100	0	400	0	1000	kHz
Bus free time (between stop and start condition)	t_{BUF}	I/O	4.7	—	1.3	—	0.5	—	µs
Hold time*1	$t_{HD:STA}$	I/O	4.0	—	0.6	—	0.26	—	µs
Low period of SCL clock	t_{LOW}	I/O	4.7	—	1.3	—	0.5	—	µs
High period of SCL clock	t_{HIGH}	I/O	4.0	—	0.6	—	0.26	—	µs
Setup time for start / restart condition	$t_{SU:STA}$	I/O	4.7	—	0.6	—	0.26	—	µs
Data hold time (I^2C bus device)	$t_{HD:DAT}$	I/O	0*2	—	0*2	—	0	—	µs
Data setup time	$t_{SU:DAT}$	I/O	250	—	100*3	—	50	—	ns
SDA and SCL signal rise time	t_R	Input	—	1000	—*6	300	—*6	120	ns
SDA and SCL signal fall time*3	t_F	Input	—	300	—*6	300	—*6	120	ns
		Output	—	300	—*6	300	—*6	120	ns
Setup time for STOP condition	$t_{SU:STO}$	I/O	4.0	—	0.6	—	0.26	—	µs
Capacitive load for each bus line	C_b	—	—	400*4	—	400*4	—	550*4	pF
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	Input	—	—	0	50*5	0	50*5	ns

Note: In the above table and subsequently, SCL and SDA refer to the RIICn_SCL and RIICn_SDA (n = 0 to 3) signals, respectively.

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 11b, output load 400 pF

Note 1. The first clock pulse is generated on the SCL line after the start condition has been issued and the hold time has elapsed.

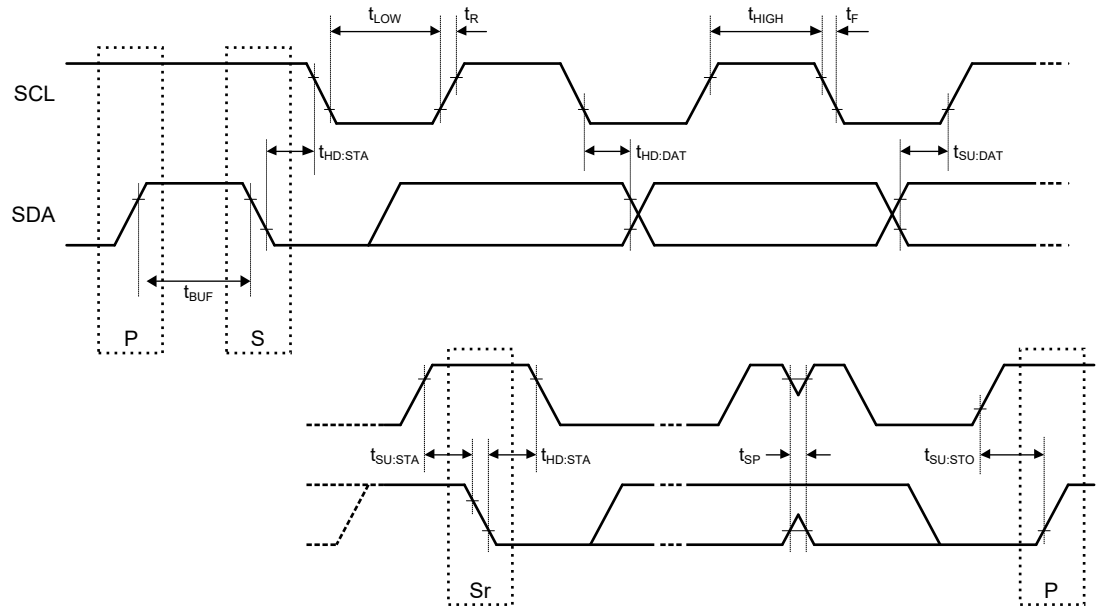
Note 2. This module requires a minimum of 300 ns hold time internally for the SDA signal to handle the period over which the falling edge of SCL has not reached a defined level (time until the CnSCL signal reaches V_{IL} (max.) from V_{IH} (min.)).

Note 3. The fast-mode I^2C bus device can be used in the standard mode I^2C bus system. In this case, the minimum value of the data setup time ($t_{SU:\,DAT}$ (min.) 250 [ns]) must be satisfied.
If the system does not extend the low period of SCL clock (t_{LOW}), this condition is automatically satisfied. If the system extends the low period of SCL clock (t_{LOW}), transmit the subsequent data bit to the SDA line before the SCL line is released (t_R (max.) + $t_{SU:\,DAT}$ (min.) = 1000 + 250 = 1250 [ns]: (standard mode I^2C bus specification)).

Note 4. Total capacitance of one bus line. The allowable maximum bus capacitance may differ from this specification, depending on the actual operating voltage and frequency of an application. For techniques to cope with a large bus capacitance, see the I^2C bus specification provided by NXP Semiconductors.

Note 5. Noise is removed by the analog and digital input filters. The level of noise reduction of the digital input filter is determined by the period of internal reference clock (IICϕ) and the NF[1:0] bits in RIICnMR3.

Note 6. The minimum values are not specified for t_R and t_F in Fast-mode or Fast-mode Plus.



Note: P: Stop condition
S: Start condition
Sr: Start condition for retransmission

Figure 3.64 Input/Output Timing

3.5.20 I3C Timing

Table 3.40 Characteristics of the SDA and SCL Bus Lines for Standard, Fast, and Fast-Mode Plus I²C-Bus Devices*1

Item	Symbol	Conditions	Standard-Mode		Fast-Mode		Fast-Mode Plus		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		0	100	0	400	0	1000	kHz
Hold time (repeated) START condition	$t_{HD:STA}$	After this period,the first clock pulse is generated	4.0	—	0.6	—	0.26	—	µs
LOW period of the SCL clock	t_{LOW}		4.7	—	1.3	—	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	0.26	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	0.26	—	µs
Data hold time*2	$t_{HD:DAT}$	I²C-bus device	0 *3	—*4	0*3	—*4	0	—	µs
Data setup time	$t_{SU:DAT}$		250	—	100	—	50	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	—	120	ns
Fall time of both SDA and SCL signals*3,*6,*7	t_f		—	300	20 × (I3C_PV$_{DD}$/ 5.5 V)	300	20 × (I3C_PV$_{DD}$/ 5.5 V)*8	120*7	ns
Setup time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	0.26	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	0.5	—	µs

Note 1. All values referred to V_{IH}(min) (0.3 × I3C_PV$_{DD}$) and V_{IL}(max) (0.7 × I3C_PV$_{DD}$) levels, refer to **Table 3.6**.

Note 2. $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.

Note 3. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 4. The maximum $V_{HD:DAT}$ could be 3.45 µs and 0.9 µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period () of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock.

Note 5. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU:DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r(max) + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

Note 6. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

Note 7. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

Note 8. Necessary to be backwards compatible to Fast-mode.

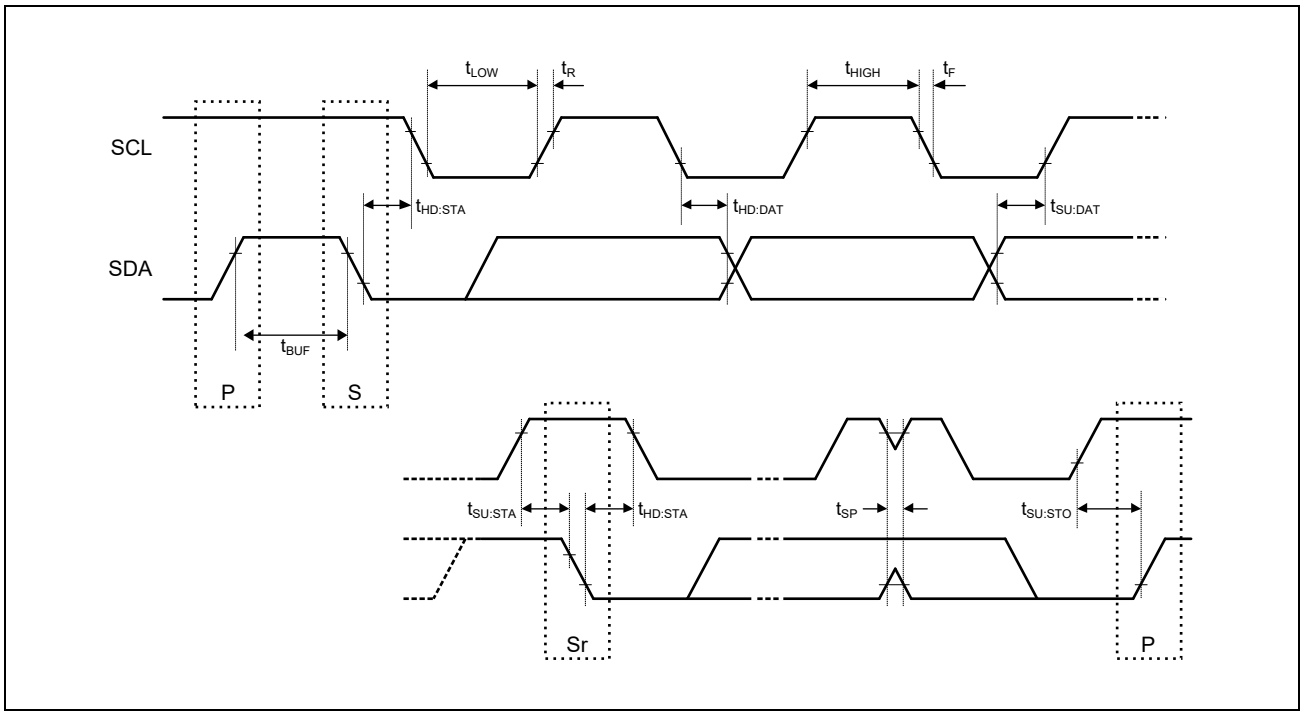


Figure 3.65 Input/Output Timing

Table 3.41 I3C Open Drain Timing Parameters

Item	Symbol	I3C Open Drain Mode			Figures	Notes
		Min.	Max.	Unit		
Low Period of SCL Clock	t_{LOW_OD}	200	—	ns	**Figure 3.69**	*1, *2
	$t_{DIG\_OD\_L}$	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	**Figure 3.69**	
High Period of SCL Clock	t_{HIGH}	—	41	ns	**Figure 3.67**	*3, *4
	t_{DIG_H}	—	t_{HIGH} + t_{CF}	ns	**Figure 3.67**, **Figure 3.76**	
Fall Time of SDA Signal	t_{fDA_OD}	t_{CF}	12	ns	**Figure 3.69**	
SDA Data Setup Time During Open Drain Mode	t_{SU_OD}	13.5 (1.8V) 18.5 (1.2V)	—	ns	**Figure 3.68**, **Figure 3.69**	*1
Clock After START(S) Condition	t_{CAS}	38.4 nano	For ENTAS0: 1 µ For ENTAS1: 100 µ For ENTAS2: 2 milli For ENTAS3: 50 milli	seconds	**Figure 3.69**	*5, *6
Clock Before STOP(P) Condition	t_{CBP}	t_{CASmin}/2	—	seconds	**Figure 3.70**	
Current Master to secondary Master Overlap time during handoff	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	**Figure 3.75**	
Bus Available Condition	t_{AVAL}	1	—	µs	—	*7
Bus Idle Condition	t_{IDLE}	200	—	µs	—	
Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	$t_{AVALmin}$	—	µs	**Figure 3.75**	

Note 1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_ODmin}.

Note 2. The Master may use a shorter low period if it knows that this is safe, i.e., that SDA is already above V_{IH}.

Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect.

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short bus).

Note 5. On a Legacy Bus where I^2C Devices need to see Start, the t_{CAS}(min) value is further constrained.

Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS}(max) value shown for ENTAS3.

Note 7. On a Mixed Bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF}).

Table 3.42 I3C Push-Pull Timing Parameters for SDR Mode

Item		Symbol	Min.	Max.	Unit	Figures	Notes
SCL Clock Frequency		f_{SCL}	0.01	12.5	MHz	—	*1
SCL Clock Low Period		t_{LOW}	24.5	—	ns	**Figure 3.66**	—
		t_{DIG_L}	35	—	ns	**Figure 3.67**	*2, *4
SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	24.5	—	ns	**Figure 3.67**	—
		$t_{DIG\_H\_MIXED}$	35	45	ns	**Figure 3.67**	*2, *3
SCL Clock High Period		t_{HIGH}	24.5	—	ns	**Figure 3.66**	—
		t_{DIG_H}	35	—	ns	**Figure 3.66, Figure 3.67**	*2
Clock in to Data Out for Slave		t_{SCO}	—	12 (1.8V) 14 (1.2V)	ns	**Figure 3.72**	*7, *8
SCL Clock Rise Time		t_{CR}	—	150 × 1 / f_{SCL} (capped at 60)	ns	**Figure 3.66**	*5
SCL Clock Fall Time		t_{CF}	—	150 × 1 / f_{SCL} (capped at 60)	ns	**Figure 3.66**	*5
SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP}	t_{CR} + 3 and t_{CF} +3	—	—	**Figure 3.71**	*4, *6
	Slave	t_{HD_PP}	0	—	—	**Figure 3.73**	*6
SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	13.5 (1.8V) 18.5 (1.2V)	N/A	ns	**Figure 3.71**, **Figure 3.72**	—
Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns	**Figure 3.74**	—
Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	N/A	ns	**Figure 3.74**	—
Capacitive Load per Bus Line (SDA/SDL)		C_b	—	50	pF	—	—

Note 1. FSCL = 1 / (t_{DIG_L} + t_{DIG_H})

Note 2. t_{DIG_L} and t_{DIG_H} are the clock low and high periods as seen at the receiver end of the I3C bus using V_{IL} and V_{IH} (see **Figure 3.66**).

Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.

Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

Note 5. The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.

Note 6. t_{HD_PP} is a Hold time parameter for Push-Pull Mode that has a different value for Master mode vs. Slave mode. In SDR Mode the Hold time parameter is referred to as t_{HD_SDR}.

Note 7. Devices with more than 12 ns of t_{SCO} delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Master to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.

Note 8. Pad delay based on 50 pF load. Note that Master may be a Slave in a multi-Master system, and thus shall also adhere to this requirement.

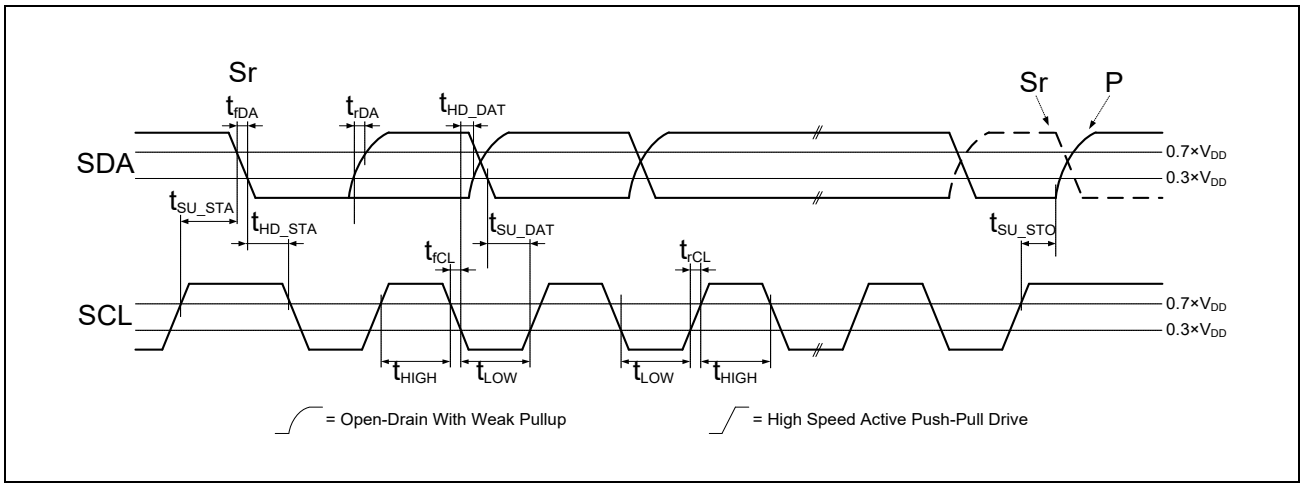


Figure 3.66 I3C Legacy Mode Timing

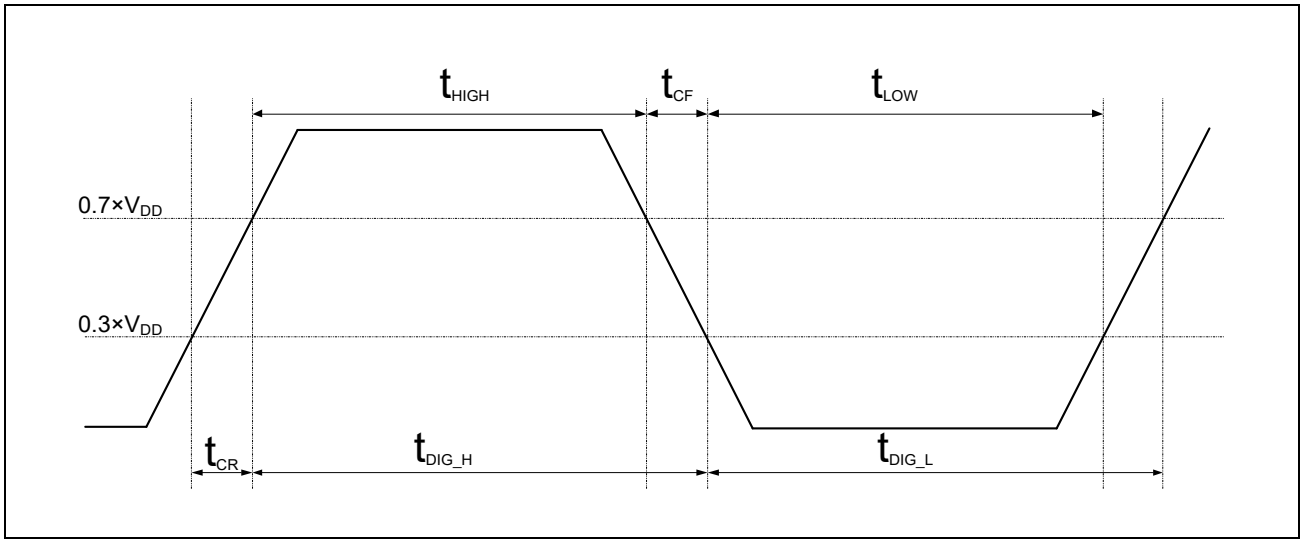


Figure 3.67 t_{DIG_H} and t_{DIG_L}

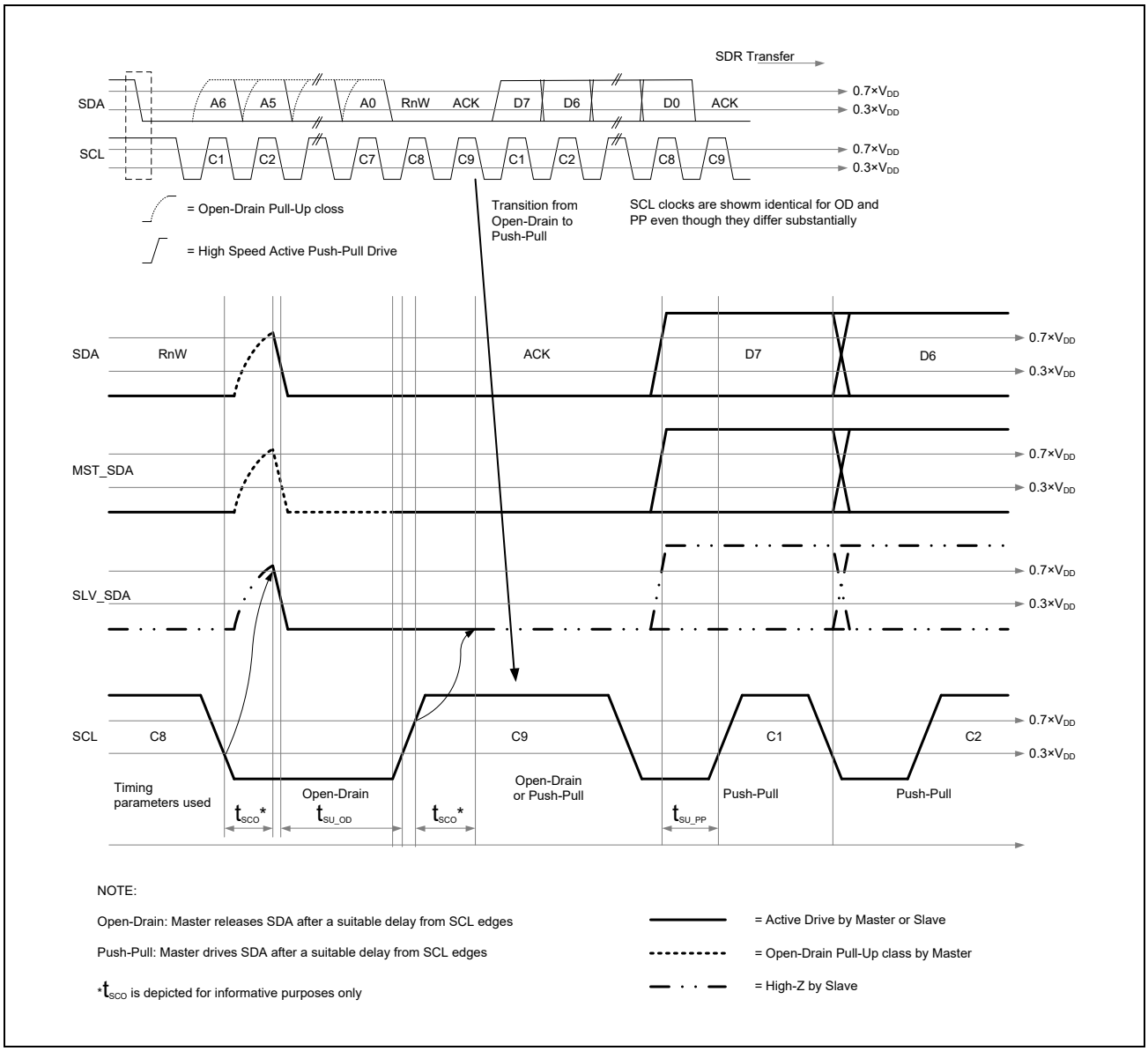


Figure 3.68 I3C Data Transfer – ACK by Slave

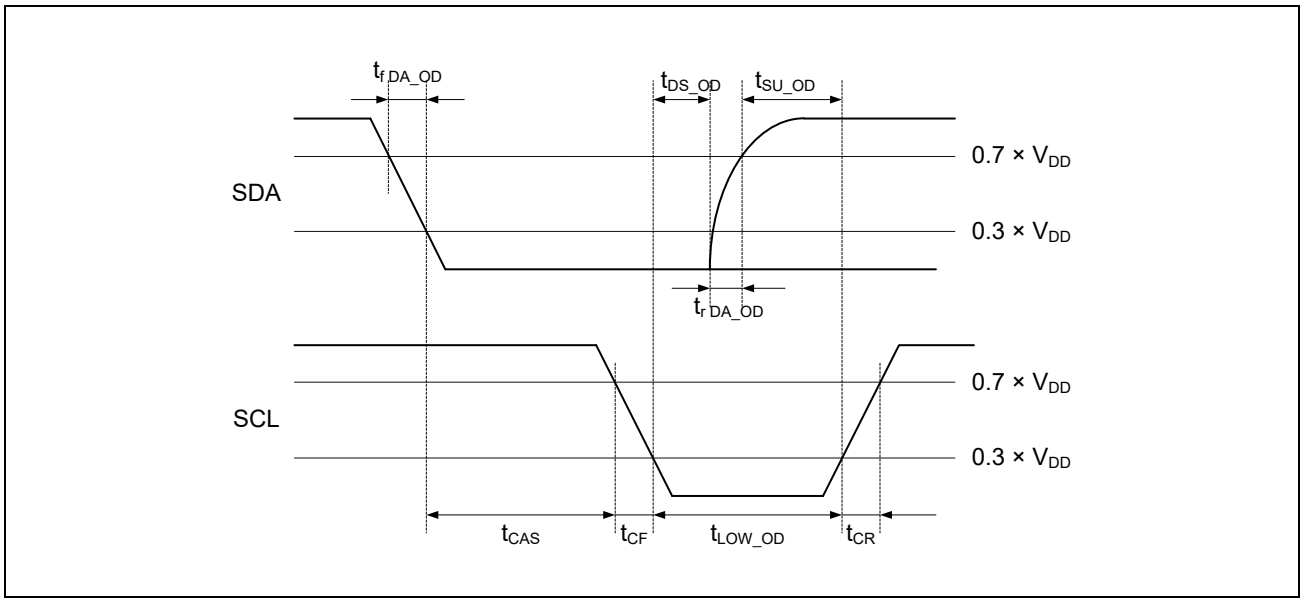


Figure 3.69 I3C START Condition Timing

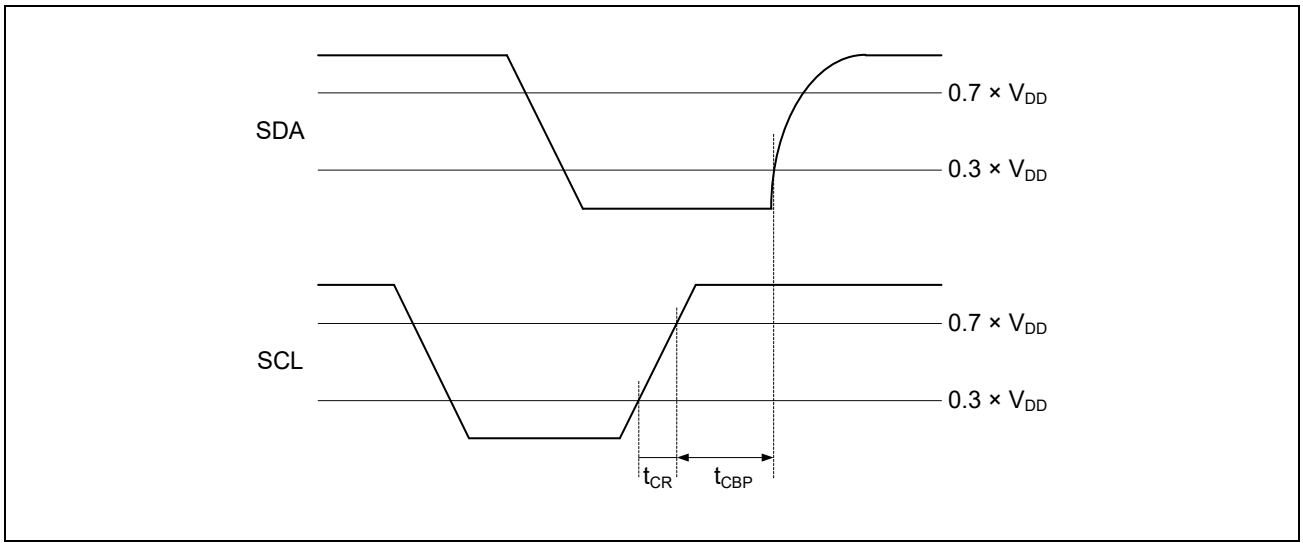


Figure 3.70 I3C STOP Condition Timing

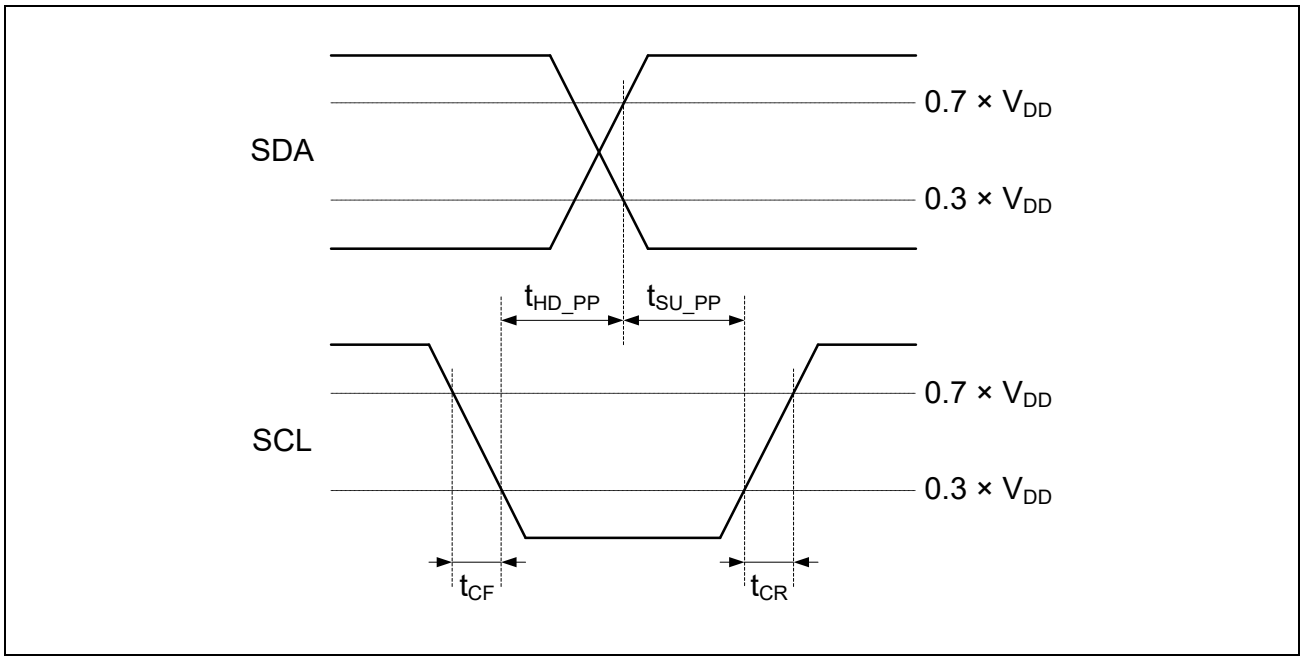


Figure 3.71 I3C Master Out Timing

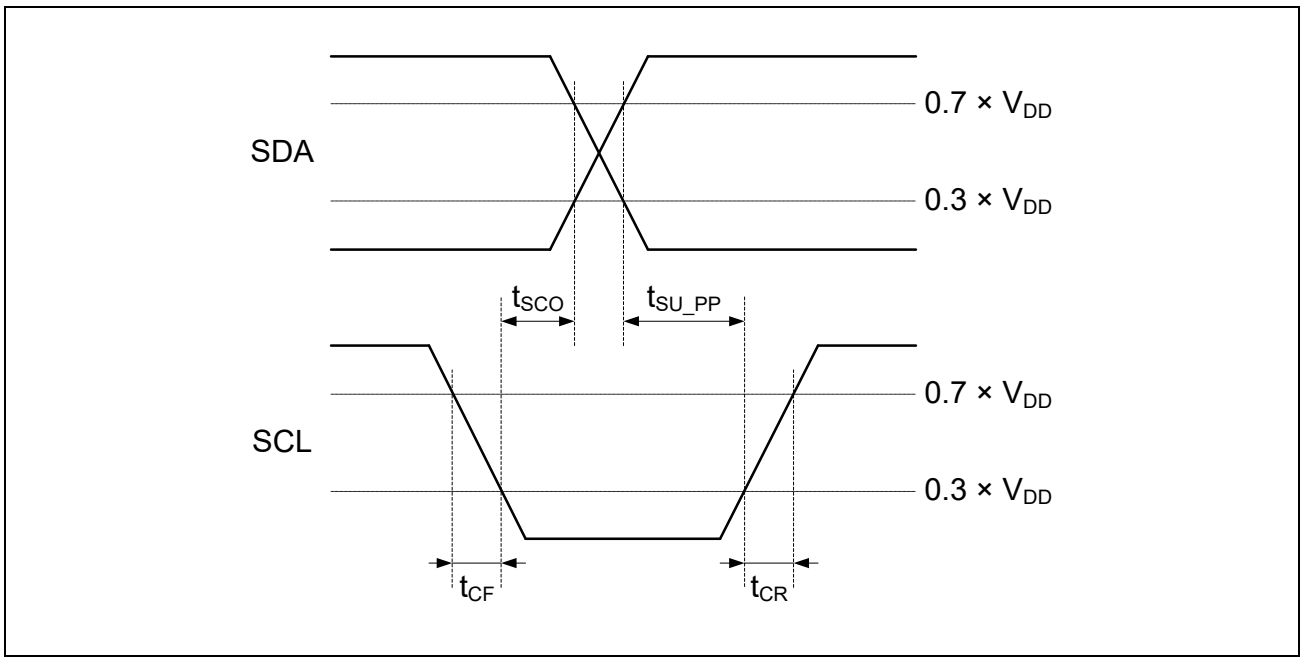


Figure 3.72 I3C Slave Out Timing

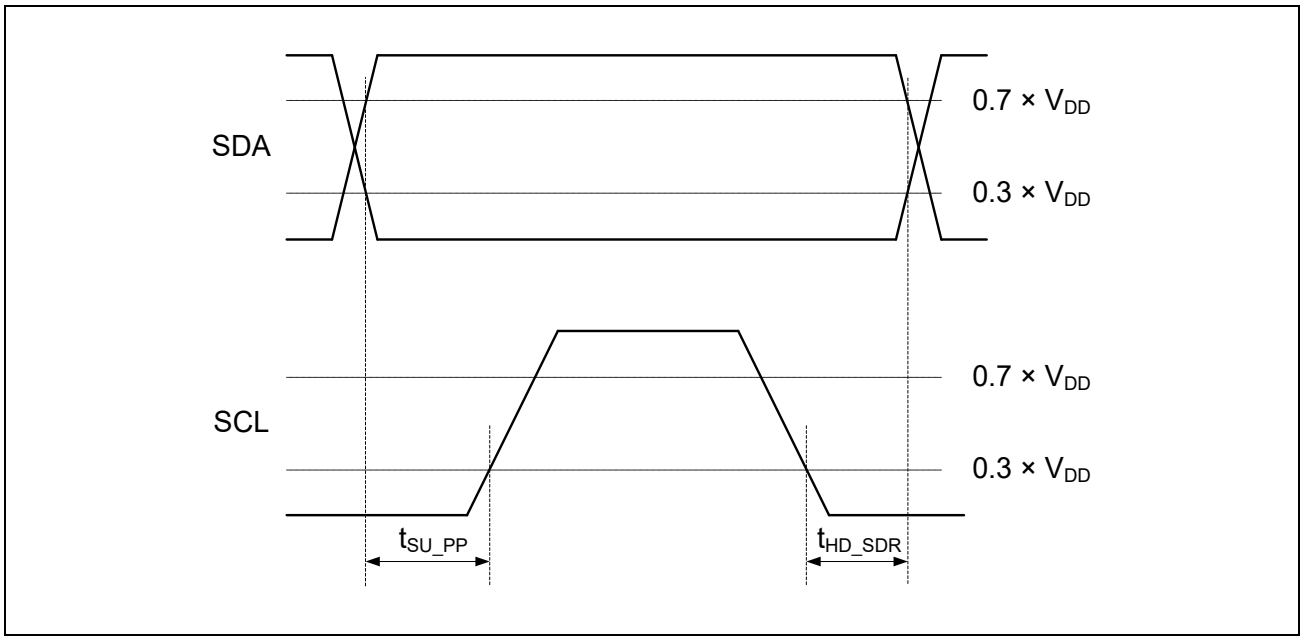


Figure 3.73 Master SDR Timing

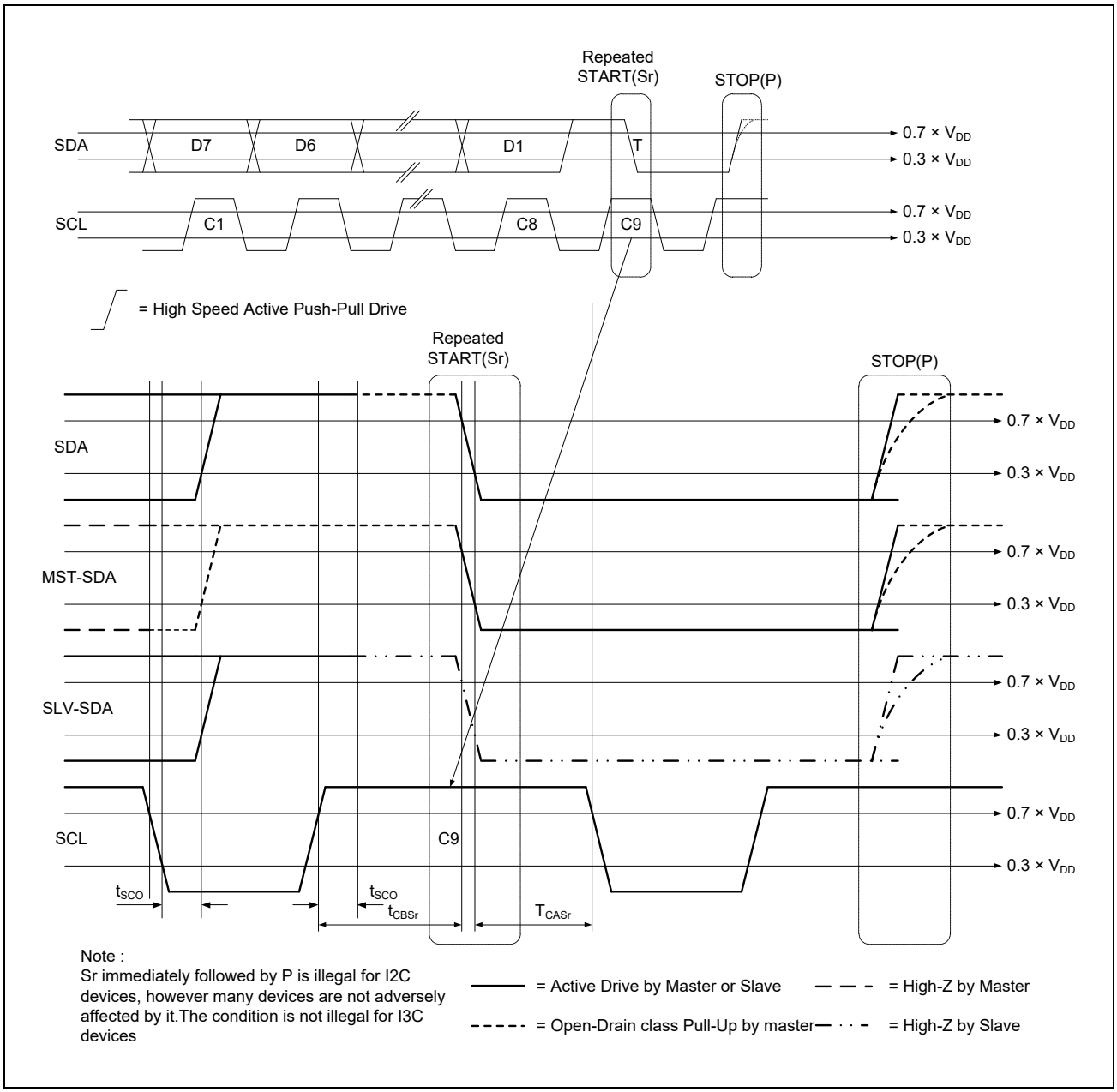


Figure 3.74 T-Bit When Master Ends Read with Repeated START and STOP

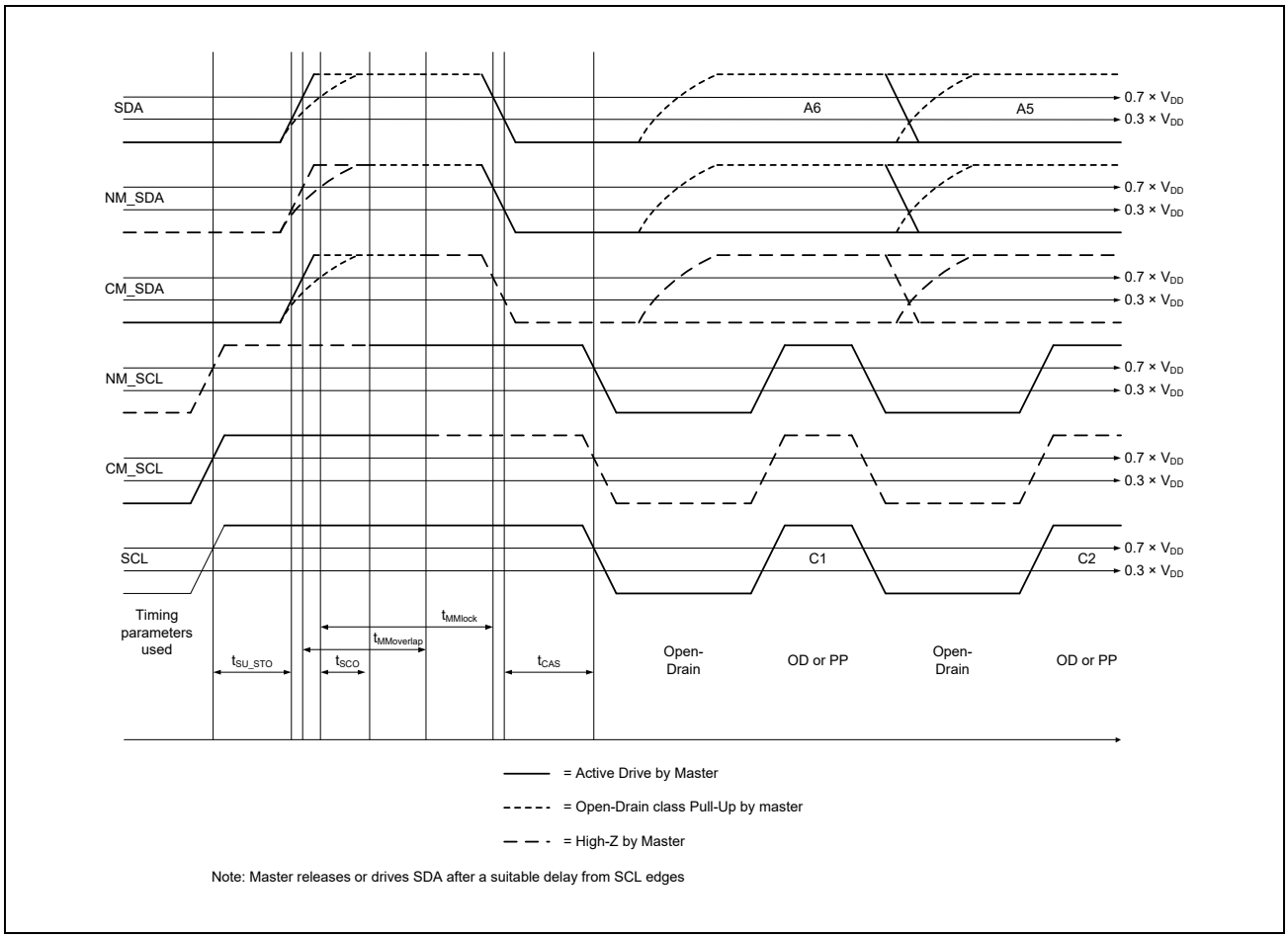


Figure 3.75 I3C Timing

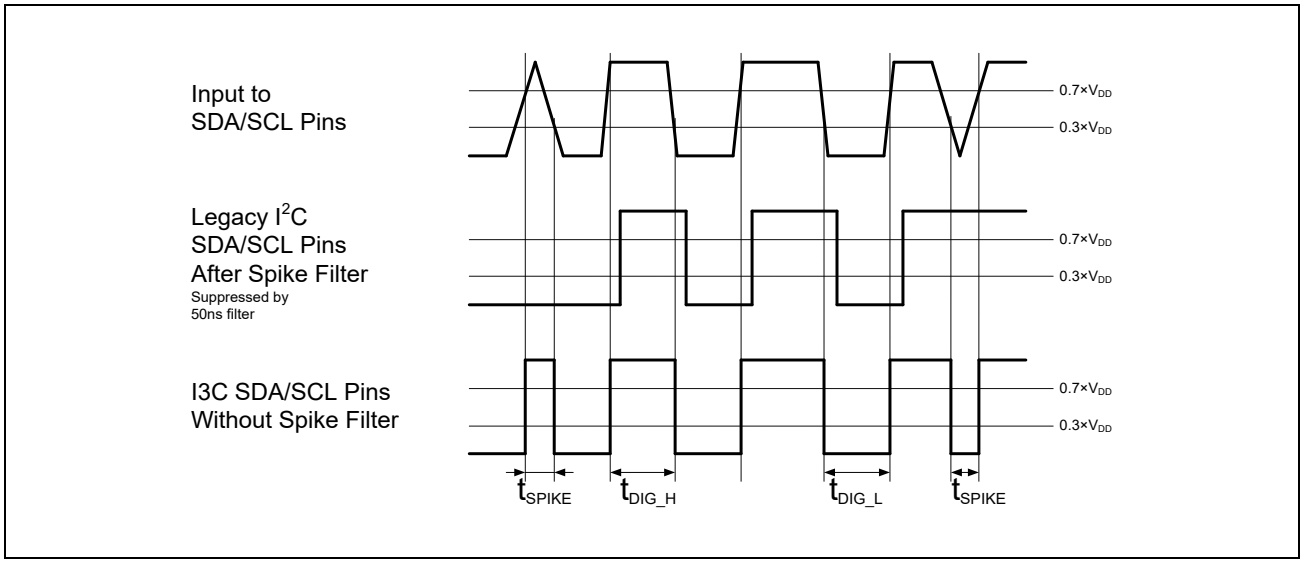


Figure 3.76 I2C Spike Filter Behavior

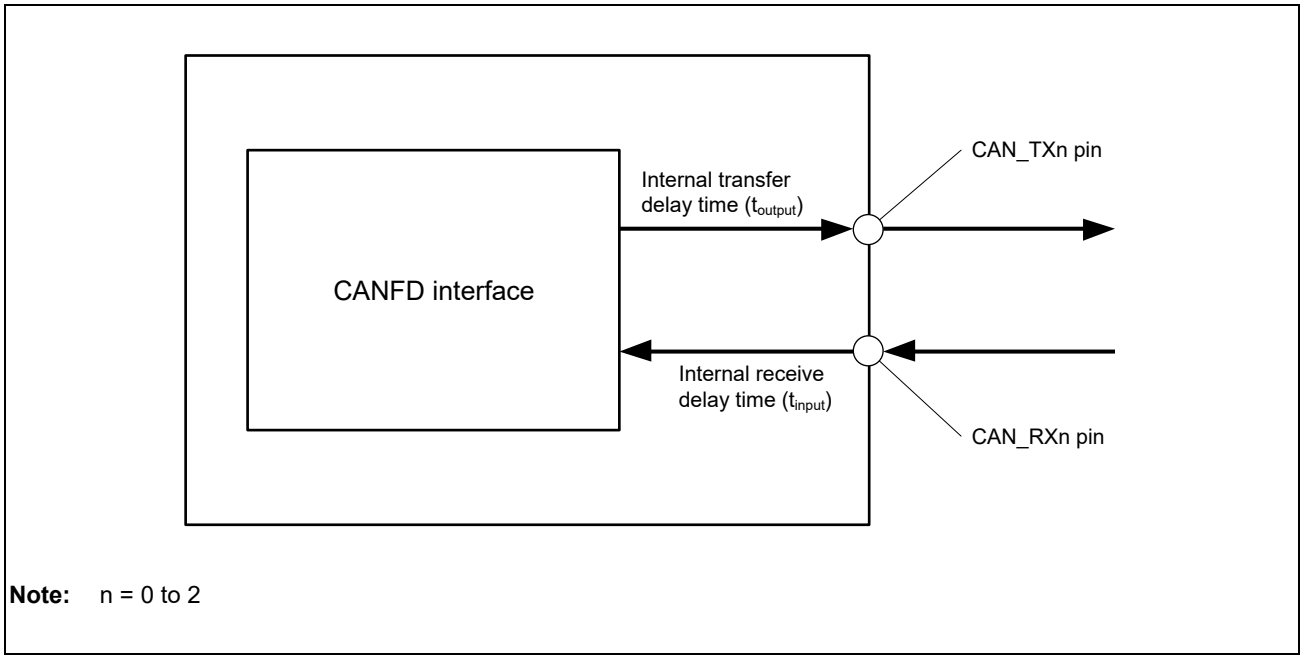
3.5.21 CANFD Interface Access Timing

Table 3.43 CANFD Interface Timing

Parameter		Symbol	CAN		CANFD		Unit	Figures
			Min.	Max.	Min.	Max.		
CANFD	Internal delay time	t_{node}*1	—	100	—	50	ns	**Figure 3.77**
	Transmission rate	—	—	1	—	8	Mbps	

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF

Note 1. Internal delay time (t_{node}) = Internal transfer delay time (t_{output}) + Internal receive delay time (t_{input})



Note: n = 0 to 2

Figure 3.77 CANFD Interface Condition

3.5.22 A/D Converter Access Timing

Table 3.44 A/D Converter Trigger Timing

Item	Symbol	Min.	Max.	Unit	Figure
A/D converter trigger input pulse width	t_{TRGW}	1.5*2	—	t_{P1cyc}*1	**Figure 3.78**

Note 1. t_{p1cyc} indicates peripheral clock means ADCn_ADCLK (P20ϕ)(n = 0,1).

Note 2. When a noise filter in ADC is off.

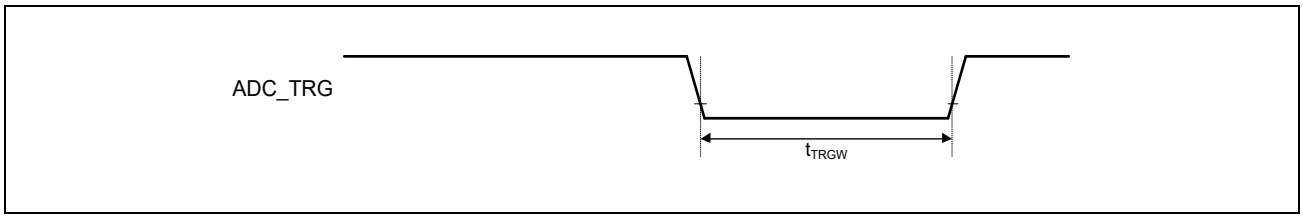


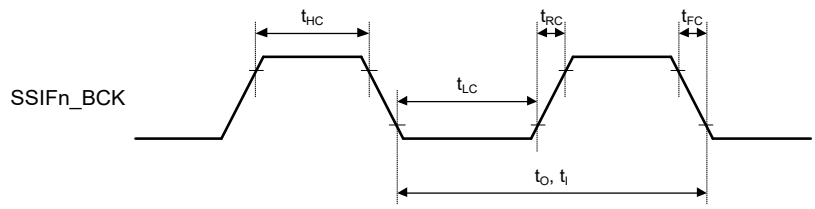
Figure 3.78 ADC Trigger Input Timing

3.5.23 Serial Sound Interface (SSIF-2) Access Timing

Table 3.45 SSIF-2 Timing

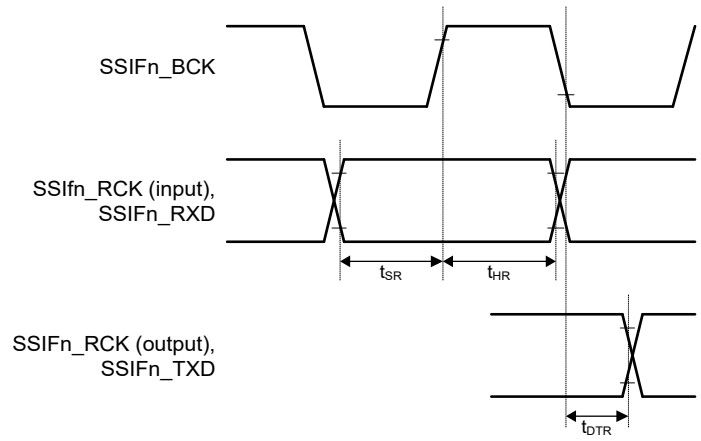
Item	Input/Output	Symbol	Min.	Max.	Unit	Figures
Output clock cycle	Output	t_O	80	64000	ns	**Figure 3.79**
Input clock cycle	Input	t_I	80	—	ns	
Clock high	Bidirectional	t_{HC}	32	—	ns	
Clock low		t_{LC}	32	—	ns	
Clock rise time/clock fall time	Output	t_{RC}/t_{FC}	—	25	ns	
Setup time	Input	t_{SR}	25	—	ns	**Figure 3.80** to **Figure 3.82**
Hold time		t_{HR}	5	—	ns	
SILRCK output delay time	Output	t_{DTR}	−5	25	ns	
Data output delay time (Noise canceler not in use)		t_{DTR}	−5	25	ns	
Data output delay time (Noise canceler in use)		t_{DTR}	10	50	ns	

Note: AC access timing condition: drive ability IOLH_xx[1:0] = 10b, output load 30 pF



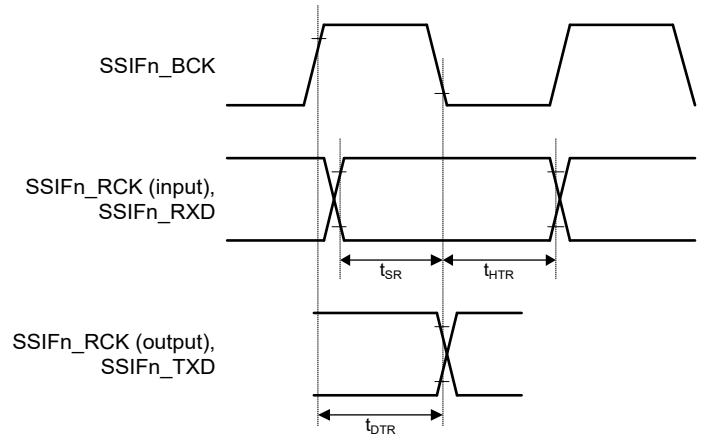
Note: n = 0 to 3

Figure 3.79 Bit Clock Input/Output Timing



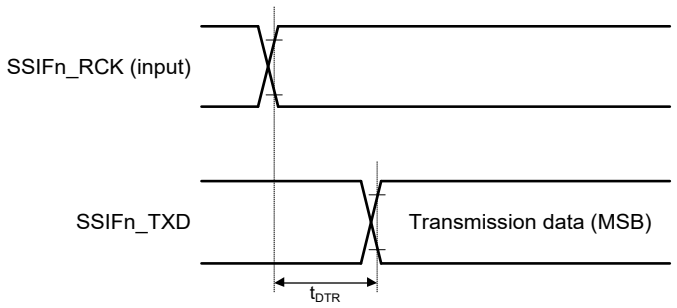
Note: n = 0 to 3

Figure 3.80 Transmission and Reception Timing (SSIBCK Falling Output)



Note: n = 0 to 3

Figure 3.81 Transmission and Reception Timing (SSIBCK Rising Output)



Note: n = 0 to 3

Note: Output timing of the MSB when slave transmission satisfies the following condition a) or b)

a) SSICR.DEL = 1, SSICR.SDTA = 0

b) SSICR.DEL = 1, SSICR.SDTA = 1, without padding

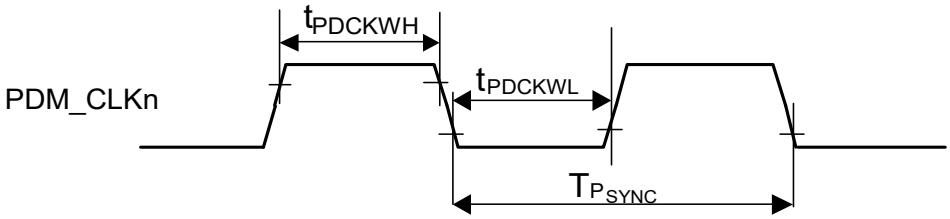
Figure 3.82 Transmission Timing (Slave, in Synchronization with SSILRCK)

3.5.24 PDM Timing

Table 3.46 PDM Interface Timing

Item	Symbol	Min.	Max.	Unit	Remarks
Clock period	t_{PSYNC}	2	32	t_{CCcyc} = 125 ns (8 MHz)	
Clock High level period	t_{PDCKWH}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	
Clock Low level period	t_{PDCKWL}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	

Note: I/O driving ability: IOLH_xx[1:0] = 11b, CL = 30 pF



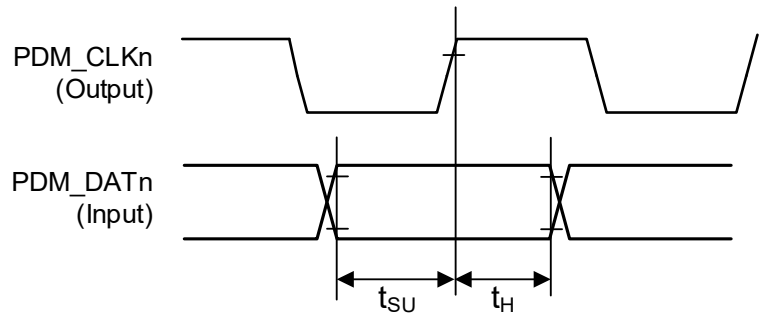
Note: n = 0 to 2

Figure 3.83 Timing of Clock Output (PDMn_CLK)

Table 3.47 PDM Interface Timing

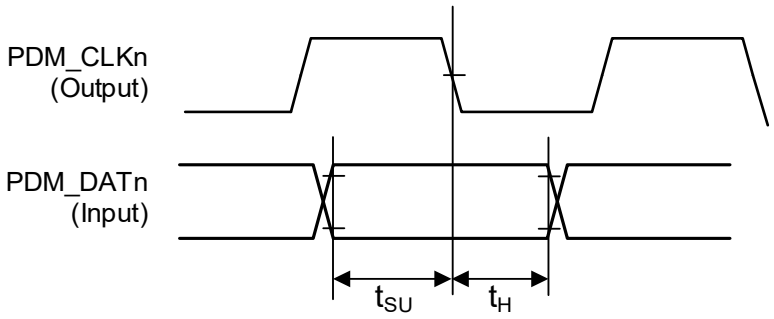
Item	Symbol	Min.	Max.	Unit	Remarks
PDMn_DAT input setup time	t_{SU}	16.5	—	ns	
PDMn_DAT input hold time	t_H	0.0	—	ns	

Note: I/O driving ability: IOLH_xx[1:0] = 11b, CL = 30 pF



Note: n = 0 to 2

Figure 3.84 Receive Timing (Synchronized with the Rise of PDMn_CLK)



Note: n = 0 to 2

Figure 3.85 Receive Timing (Synchronized with the Fall of PDMn_CLK)

3.5.24.1 MIPI CSI-2 PHY Characteristics

The MIPI CSI-2 Rx D-PHY of this LSI is equivalent to the MIPI D-PHY Version 2.1.

For details, refer to the MIPI specification.

3.5.24.2 MIPI DSI Tx D-PHY Characteristics

The MIPI DSI Tx D-PHY of this LSI is compliant with the MIPI D-PHY Version 2.1.

For details, refer to the MIPI specification.

3.5.25 LCDC Access Timing

Table 3.48 LCDC IF Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
DPI_CLK period	t_{Lcyc}	11.49	—	185.19	ns
DPI_CLK low pulse width	t_{LOL}	$t_{Lcyc}/2 - 1.06$	—	$t_{Lcyc}/2 + 1.06$	ns
DPI_CLK high pulse width	t_{LOH}	$t_{Lcyc}/2 - 1.06$	—	$t_{Lcyc}/2 + 1.06$	ns
DPI_CLK rise time	t_{LOR}	—	—	3	ns
DPI_CLK fall time	t_{LOF}	—	—	3	ns
Data output dealy	t_{DD}	−1.5	—	1.5	ns

Note: AC access timing condition: Drive ability IOLH_xx[1:0] = 10b, output load 30 pF

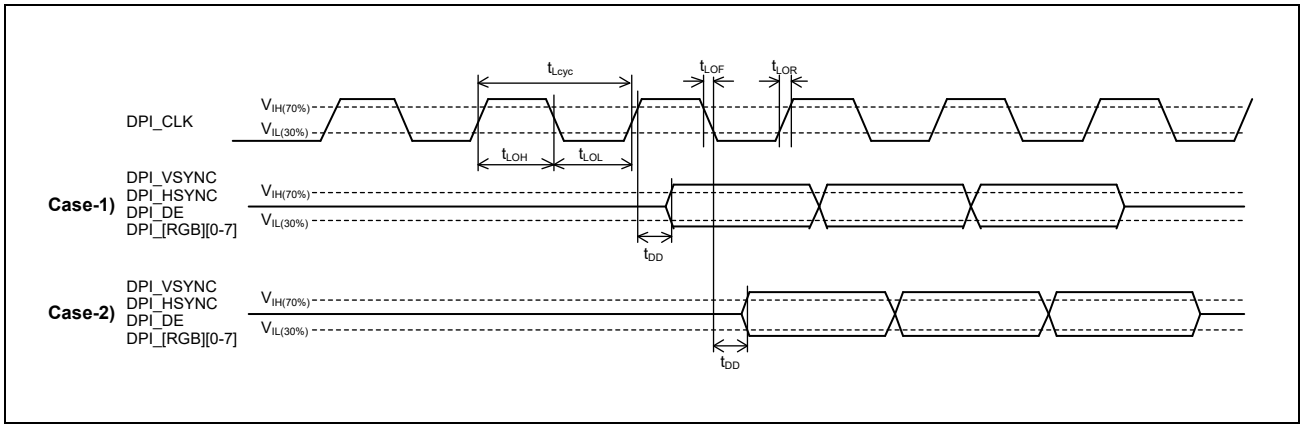
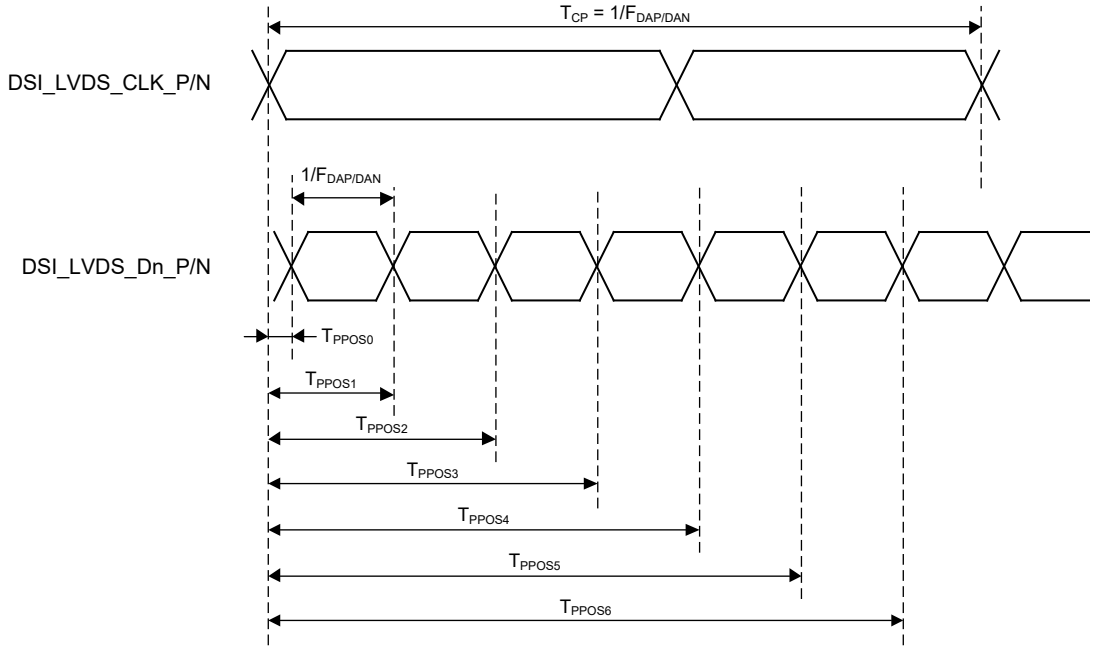


Figure 3.86 LCDC AC Access Timing

3.5.26 LVDS Interface Access Timing

Table 3.49 LVDS IF Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Output Clock Frequency of LVDS	$F_{CLKP/CLKN}$	25	—	87	MHz	**Figure 3.87**
Output Clock of LVDS	T_{CP}	11.494	—	40	ns	
Output Data Rate of LVDS	$F_{DAP/DAN}$	175	—	609	Mbps	
LVDS Output Pulse Position 0	T_{PPOS0}	−0.200	0	0.200	ns	
LVDS Output Pulse Position 1	T_{PPOS1}	$(T_{CP}/7) - 0.200$	$(T_{CP}/7)$	$(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 2	T_{PPOS2}	$2(T_{CP}/7) - 0.200$	$2(T_{CP}/7)$	$2(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 3	T_{PPOS3}	$3(T_{CP}/7) - 0.200$	$3(T_{CP}/7)$	$3(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 4	T_{PPOS4}	$4(T_{CP}/7) - 0.200$	$4(T_{CP}/7)$	$4(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 5	T_{PPOS5}	$5(T_{CP}/7) - 0.200$	$5(T_{CP}/7)$	$5(T_{CP}/7) + 0.200$	ns	
LVDS Output Pulse Position 6	T_{PPOS6}	$6(T_{CP}/7) - 0.200$	$6(T_{CP}/7)$	$6(T_{CP}/7) + 0.200$	ns	

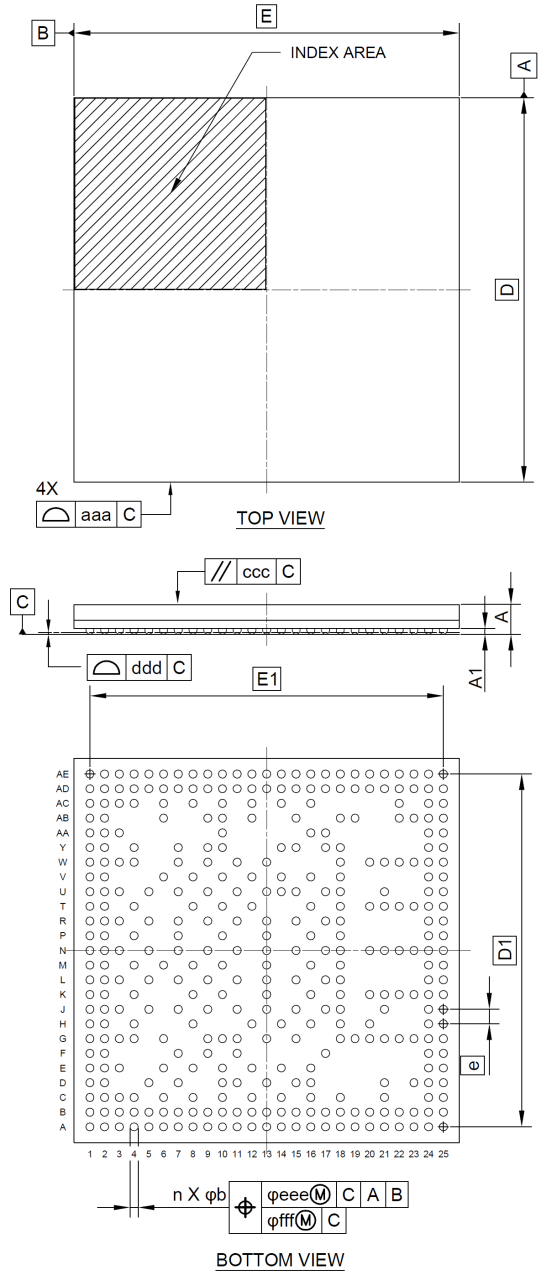


Note: n = 0 to 3

Figure 3.87 T_{CP}, $F_{DAP/DAN}$, T_{PPOS}

4. Package Dimensions

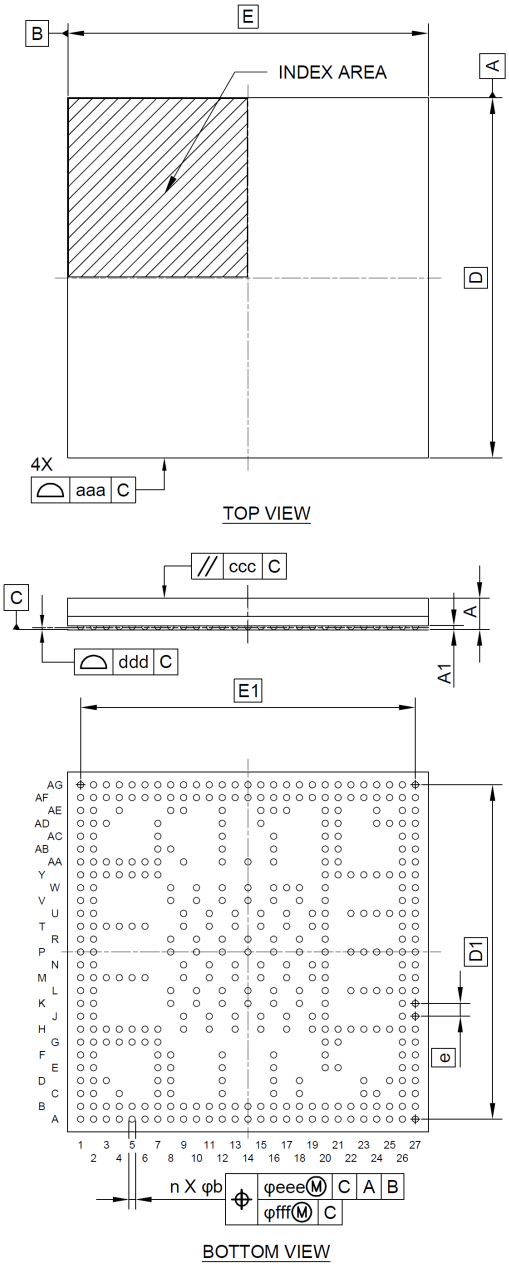
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA368-17x17-0.65	PLBG0368JA-A	0.70



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	17.00	—
E	—	17.00	—
D1	—	15.60	—
E1	—	15.60	—
A	—	—	1.40
A1	0.20	—	—
b	0.31	0.36	0.41
e	—	0.65	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.13
eee	—	—	0.15
fff	—	—	0.08
n	—	368	—

Figure 4.1 Package Dimensions (368-pin LFBGA, 17 mm□ BGA 0.65 mm pin-pitch)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA400-14x14-0.50	PLBG0400KA-A	0.46



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	14.00	—
E	—	14.00	—
D1	—	13.00	—
E1	—	13.00	—
A	—	—	1.40
A1	0.11	—	—
b	0.20	0.25	0.30
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.08
n	—	400	—

Figure 4.2 Package Dimensions (400-pin LFBGA, 14 mm□ BGA 0.5 mm pin-pitch)

Appendix A ECAD Design Information

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
R9A08G046L48GBG	368	LFBGA	PLBG0368JA-A
R9A08G046L28GBG	368	LFBGA	PLBG0368JA-A
R9A08G046L46GBG	400	LFBGA	PLBG0400KA-A
R9A08G046L26GBG	400	LFBGA	PLBG0400KA-A
R9A08G045SE8GBG	368	LFBGA	PLBG0368JA-A
R9A08G045SE7GBG	368	LFBGA	PLBG0368JA-A
R9A08G045SE6GBG	400	LFBGA	PLBG0400KA-A
R9A08G045SE5GBG	400	LFBGA	PLBG0400KA-A

A.2 Symbol Pin Information

For detailed information, refer to the given link: EDI-Appendix_RZG3L

Serial Number	Pin-Package	Applicable Part Number
A.2.1	368-LFBGA	R9A08G046L48GBG, R9A08G046L28GBG, R9A08G045SE8GBG, R9A08G045SE7GBG
A.2.2	400-LFBGA	R9A08G046L46GBG, R9A08G046L26GBG, R9A08G045SE6GBG, R9A08G045SE5GBG

A.3 Symbol Parameters

Orderable Part Number	Min Input Voltage	Max Input Voltage	Max Frequency	Min Operating Temperature	Max Operating Temperature	Memory Size	Interface	Number of A/D Converters	Number of RIIC Channels	Number of RSPI Channels	Number of UART Channel	Number of Timers/Counters
R9A08G046L48GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch
R9A08G046L28GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch
R9A08G046L46GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch
R9A08G046L26GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch
R9A08G045SE8GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch
R9A08G045SE7GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch
R9A08G045SE6GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch
R9A08G045SE5GBG	3.00 V	3.60 V	24 MHz	-40 °C	85 °C	N/A	I3C, I2C, SCI, SPI, SCIF, SD, MMC, xSPI, DDR	1	4	3	N/A	16-bit x 8-Ch, 32-bit x 1-Ch

A.4 Footprint Design Information

For detailed information, refer to the attachment

Serial Number	Pin-Package	Applicable Part Number	Attachment
A.4.1	368-LFBGA	R9A08G046L48GBG, R9A08G046L28GBG, R9A08G045SE8GBG, R9A08G045SE7GBG	PLBG0368JA-A-EFDI.pdf
A.4.2	400-LFBGA	R9A08G046L46GBG, R9A08G046L26GBG, R9A08G045SE6GBG, R9A08G045SE5GBG	PLBG0400KA-A-EFDI.pdf

REVISION HISTORY	RZ/G3L Group, RZ/G3SE Group DATASHEET

Rev.	Date	Description	
		Page	Summary
1.00	Oct 31, 2025	—	First edition issued
1.10	Jul 10, 2026	Features	
		1	Features: NOTE, added
		1. Overview	
		6	1.1.9 Display Interfaces: LVDS Interface: The description, modified (Color: 8 bits → Color: 8 bits or 6 bits)
		17	Table 1.2 Product Lineup: Note, added
		3. Electrical Characteristics	
		21	Table 3.1 Absolute Maximum Ratings (1/2), modified (VAA10_PLLn (n = 16, 45, 7) → VAA10_PLLn (n = 16, 47, 5))
		23	Table 3.2 Recommended Operating Range, modified (VAA10_PLLn (n = 16, 45, 7) → VAA10_PLLn (n = 16, 47, 5))
		24	Figure 3.1 Power-On/Power-Off Sequence 1 (All_OFF to ALL_ON, ALL_ON to ALL_OFF), modified. (G5: VAA10_PLL45, VAA10_PLL7 → G5: VAA10_PLL47, VAA10_PLL5) (SYS_RST#: > 2msec (Min) → T + $t_{STCKRST}$) (Note 5, modified)
		25	Figure 3.2 Power-On/Power-Off Sequence 2 (ALL_ON to AWO_DDR_RETENTION, AWO_DDR_RETENTION to ALL_ON), modified. (G5: VAA10_PLL45, VAA10_PLL7 → G5: VAA10_PLL47, VAA10_PLL5)
		26	Figure 3.3 Power-On/Power-Off Sequence 3 (ALL_ON to VBATT_DDR_RETENTION, VBATT_DDR_RETENTION to ALL_ON), modified. (G5: VAA10_PLL45, VAA10_PLL7 → G5: VAA10_PLL47, VAA10_PLL5) (SYS_RST#: > 2msec (Min) → T + $t_{STCKRST}$) (Note 5, modified)
		27	Figure 3.4 Power-On/Power-Off Sequence 4 (ALL_ON to VBATT, VBATT to ALL_ON), modified. (G5: VAA10_PLL45, VAA10_PLL7 → G5: VAA10_PLL47, VAA10_PLL5) (SYS_RST#: > 2msec (Min) → T + $t_{STCKRST}$) (Note 5, modified)
		34	3.5 AC Characteristics: Conditions, modified (VAA10_PLLn (n=16, 45, 7) → VAA10_PLLn (n=16, 47, 5))
		34	Table 3.12 Clock Timing Table: The table, modified. Note 2, added.
		35	Figure 3.7 Power-On Oscillation Settling Time: The figure, modified. Note 1, modified (VAA10_PLLn (n=16, 45, 7) → VAA10_PLLn (n=16, 47, 5)).
		36	Figure 3.8 Oscillation Settling Time on Return from Standby (Return by Reset): The figure, modified. Note, deleted.
		75	Table 3.38 RSPI Timing: RSPIn_SCK clock cycle: The Min values, modified. Note, added. Note 8, added.
		Appendix A ECAD Design Information	
		104, 105	Appendix A ECAD Design Information, added

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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