# Features

This LSI has following features.

## ■ CPU

- AndesCore™ AX45MP, single-core

  Max. operating frequency: 1.0 GHz

## ■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (128-Kbytes on-chip SRAM with ECC)
- External DDR memory interface

  1-channel memory controller for DDR3L-1333 or DDR4-1600 with a 16-bit bus width
- SPI Multi I/O Bus Controller × 1 channel (4-bit Double data rate)
- SD card host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

## ■ Various communication/storage/network interfaces

- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- Gigabit Ethernet controller × 2 channels
- CANFD interface × 2 channels
- $I^2C$ bus interface × 4 channels
- Serial communication interface (SCI) × 2 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial Peripheral Interface (RSPI) × 3 channels

## ■ Extended-function timers

- Multi-Function Timer Pulse Unit

  32-bit × 1 channel, 16-bit × 8 channels

## ■ Audio

- Serial sound interface × 4 channels

## ■ Analog/Digital converter (ADC) and sensor

- 12-bit A/D converter × 2 channels
- Thermal Sensor Unit × 1 channel

## ■ Security

- Hardware cryptographic engine [option]

# 1. Overview

## 1.1 Outline of Specification

### 1.1.1 CPU Core

| Item | Description |
|---|---|
| System CPU AX45MP | [RZ/Five]<br>● AndesCore™ AX45MP Single core 1.0 GHz<br>● L1 I-cache 32 Kbytes (Parity) / D-cache 32 Kbytes (ECC)<br>● ILM 64 Kbytes (ECC) / DLM 64 Kbytes (ECC), Total 128 Kbytes*1<br>● L2 cache 256 KBytes (ECC)<br>● Floating point extension DSP/SIMD ISA<br>● AndeStar™ V5 Instruction Set Architecture (ISA)<br>*Note 1.* The ILM and DLM are generally not used in Linux.<br>Please refer also AndesCoreAX45MP-1C Processor Reference Manual for details. |
| Boot | [RZ/Five]<br>● 6 boot modes<br>Boot Mode 0: Booting from eSD<br>Boot Mode 1: Booting from eMMC (1.8 V)<br>Boot Mode 2: Booting from eMMC (3.3 V)<br>Boot Mode 3: Booting from a serial flash memory (Single / Quad) connected to the SPI Multi I/O bus space (1.8 V)<br>Boot Mode 4: Booting from a serial flash memory (Single / Quad) connected to the SPI Multi I/O bus space (3.3 V)<br>Boot Mode 5: Booting from SCIF download |
| Debug Interface | [RZ/Five]<br>● AndesCore™ AX45MP Debug Subsystem<br>● JTAG interface supported<br>● Embedded Debug Module with up to 8 triggers |

### 1.1.2 CPU Peripheral

| Item | Description |
|---|---|
| Clock Pulse Generator (CPG) | [RZ/Five]<br>● Generates the clocks from external clock (EXCLK 24 MHz).<br>Maximum AndesCore™ AX45MP Single core clock: 1.0 GHz<br>Maximum DDR clock: 666 MHz (DDR3L-1333), 800 MHz (DDR4-1600)<br>Maximum AXI-bus clock: 200 MHz<br>Maximum APB-bus clock: 100 MHz<br>● SSC (Spread Spectrum Clock) supported |
| Direct Memory Access Controller (DMAC) | [RZ/Five]<br>● 2 modules, 16 channels per module<br>● Transfer request: On-chip peripheral request / auto request (software trigger)<br>● A specific DMA transfer interval can be specified to adjust the bus occupancy.<br>● LINK mode (DMA transfer under descriptor control) supported<br>● Transfer information can be automatically reloaded |
| Platform-Level Interrupt Controller (PLIC) | [RZ/Five]<br>● Andes Platform-Level Interrupt Controller<br>● 255 priority levels available<br>● Software-programmable interrupt generation<br>● External Interrupt pins (NMI, IRQ7 to IRQ0, TINT31-0)<br>● On-chip peripheral Interrupts: priority level set for each module |
| General-purpose I/O (GPIO) | [RZ/Five]<br>● General-purpose I/O ports |
| Thermal Sensor Unit (TSU) | [RZ/Five]<br>● 1 channel |

### 1.1.3 Internal Memory

| Item | Description |
|---|---|
| System RAM | [RZ/Five]<br>● RAM of 128 Kbytes (ECC) |

### 1.1.4 External Memory Interface

| Item | Description |
|---|---|
| External Bus Controller for DDR3L / DDR4 SDRAM (DDR) | [RZ/Five]<br>• Support DDR3L-1333 / DDR4-1600<br>• Bus Width: 16-bit<br>• In line ECC supported (Support error detection interrupt)<br>• Memory Size: Up to 4 Gbyes<br>• Auto Refresh supported |
| SPI Multi I/O Bus Controller | [RZ/Five]<br>• 1 channel (4-bit Double data rate)<br>• 1 serial flash memory with multiple I/O bus sizes (single / quad) can be connected<br>• External address space read mode (built-in read cache)<br>• SPI operation mode<br>• Maximum Clock Frequency:<br>– 50 MHz (Quad-SPI DDR)<br>– 66 MHz (Quad-SPI SDR) |
| SD Card Host Interface / Multimedia Card Interface (SD/MMC) | [RZ/Five]<br>• 2 channels<br>• Channel 0 supports SDHI / e-MMC (boot supported)<br>• Channel 1 supports SDHI<br>• SD memory I/O card interface (1-bit / 4-bit SD bus)<br>• SD, SDHC and SDXC SD memory card access supported<br>• Compliant with SD 3.0<br>• Default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported<br>• Error check function: CRC7 (Command), CRC16 (Data)<br>• Card detection function, write protect supported<br>• MMC interface (1-bit / 4-bit / 8-bit MMC bus)<br>• e-MMC device access supported<br>• Compliant with eMMC 4.51<br>• High-speed, HS200 transfer modes supported |

### 1.1.5 Sound Interface

| Item | Description |
|---|---|
| Serial Sound Interface (SSI) | [RZ/Five]<br>• 4 channels bidirectional serial transfer<br>• 2 external clock sources available<br>• Duplex communication (channel 0, 1, and 3)<br>• Support of I2S / Monaural / TDM audio formats<br>• Support of master and slave functions<br>• Generation of programmable word clock and bit clock<br>• Multi-channel formats<br>• Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats<br>• Support of 32-stage FIFO for transmission and reception<br>• Support of LR-clock continue function in which the LR-clock signal is not stopped |

### 1.1.6 Storage and Network

| Item | Description |
|---|---|
| USB2.0 Host / Function (USB) | [RZ/Five]<br>• 2 channels (ch0: Host-Function ch1: Host only)<br>• Compliance with USB2.0<br>• Supports On-The-Go (OTG) Function<br>• Supports Battery Charging Function<br>• Internal dedicated DMA |
| Gigabit Ethernet Interface (GbE) | [RZ/Five]<br>• Number of channels<br>– 2 channels: Support by 361-pin BGA<br>– 1 channel: Support by 266-pin BGA<br>• Supports transfer at 1000 Mbps and 100 Mbps, 10 Mbps<br>• Supports filtering of Ethernet frames<br>• Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface)<br>• Supports interface conforming to IEEE802.3 PHYMII (Media Independent Interface) |
| Controller Area Network Interface (CAN) | [RZ/Five]<br>• 2 channels<br>• ISO 11898-1 (2003) compliant<br>• CAN-FD ISO 11898-1 (CD2014) compliant<br>• Message buffer<br>– Up to 64 × 2-channel receive message buffer: Shared among all channels<br>– 16 transmit message buffers per channel |

### 1.1.7 Timer

| Item | Description |
|---|---|
| Multi-function Timer Pulse Unit 3 (MTU3a) | [RZ/Five]<br>• 9 channels (16 bits × 8 channels, 32 bits × 1 channel)<br>• Module clock frequency (P0ϕ): 100 MHz<br>• Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs<br>• 14 types of count clocks selectable<br>• Input capture function<br>• 39 outputs compare and input capture registers<br>• Counter clear operation (Simultaneous counter clearing by Compare match or Input capture is available)<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Synchronous input/output of each register due to synchronous operation of the counter<br>• Buffered operation<br>• Cascade-connected operation<br>• 43 types of interrupt sources<br>• Automatic transfer of register data<br>• Pulse output modes<br>Toggle, PWM, complementary PWM, and reset-synchronized PWM modes<br>• Synchronization of multiple counters<br>• Phase counting mode<br>– 16-bit mode (channel 1 and 2)<br>– 32-bit mode (channel 1 and 2)<br>• Counter function of dead time compensation<br>• Digital filter functions for the input capture and external count clock pin |
| Port Output Enable 3 (POE3) | [RZ/Five]<br>• Control of the high-impedance state of the MTU3a waveform output pins<br>• Activation with four input pins<br>• Activation on detection of short-circuited outputs<br>• Activation by register write<br>• Additional programming of output control target pins is possible. |
| Watchdog Timer (WDT) | [RZ/Five]<br>• 1 channel<br>• A counter overflow can reset the LSI<br>• CPU parity error can reset the LSI |
| General Timer (GTM) | [RZ/Five]<br>• 32 bits × 3 channels<br>• Two operating modes<br>– Interval timer mode<br>– Free-running comparison mode |

### 1.1.8 Peripheral Module

| Item | Description |
|---|---|
| I2C Bus Interface<br>(I2C) | [RZ/Five]<br>• 4 channels (ch0,1 = Dedicated pin, ch2,3 = Multiplexed pin)<br>• Master mode and slave mode supported<br>• Support for 7-bit and 10-bit slave address formats<br>• Support for multi-master operation<br>• Timeout detection |
| Serial Communication Interface with FIFO<br>(SCIFA) | [RZ/Five]<br>• 5 channels<br>• Clock synchronous mode or asynchronous mode selectable<br>• Simultaneous transmission and reception (full-duplex communication) supported<br>• Dedicated baud rate generator<br>• Separate 16-byte FIFO registers for transmission and reception<br>• Modem control function (channel 0, 1, and 2 in asynchronous mode) |
| Serial Communication Interface<br>(SCI) | [RZ/Five]<br>• 2 channels<br>• Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable<br>• Simultaneous transmission and reception (full-duplex communication) supported<br>• Dedicated baud rate generator<br>• LSB first / MSB first selectable<br>• Modem control function<br>• Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0) |
| Renesas Serial Peripheral Interface (RSPI) | [RZ/Five]<br>• 3 channels<br>• SPI operation<br>• Master mode and slave mode supported<br>• Programmable bit length, clock polarity, clock phase can be selected<br>• Consecutive transfers<br>• LSB first / MSB first selectable |

### 1.1.9 Security

| Item | Description |
|---|---|
| Trusted Secure IP<br>(TSIP)<br>[option] | [RZ/Five]<br>• Security algorism<br>– Common key encryption: AES<br>– Non-common key encryption: RSA, ECC<br>• Other features<br>– TRNG (true-random number generator)<br>– Hash value generation: SHA-1, SHA-224, SHA-256, GHASH<br>– Support of Unique ID |
| One Time Programmable memory<br>(OTP) | [RZ/Five]<br>• A nonvolatile memory that can be written only once<br>• Security setting, authentication setting are possible<br>• Support one time read function (128 bytes) |

### 1.1.10 Analog

| Item | Description |
|---|---|
| A/D Converter (ADC) | [RZ/Five]<br>• 2 channels<br>• Resolution: 12-bit<br>• Input Range: 0 V ~ 1.8 V<br>• Conversion Time: 1 µs<br>• Operation Mode: Single Scan / Continuous Scan<br>• Condition for A/D conversion start<br>– Software trigger<br>– Asynchronous trigger: External trigger supported<br>– Synchronous trigger: MTU timer |

### 1.1.11 Others

| Item | Description |
|---|---|
| Boundary Scan | [RZ/Five]<br>• Boundary scan based on IEEE 1149.1 via JTAG interface is supported.<br>Note that some module pins are not available on this boundary scan. |

### 1.1.12 Power Supply Voltage

| Item | Description |
|---|---|
| Power supply voltage | [RZ/Five]<br>• $V_{DD}$, PLLn_$DV_{DD11}$ (n = 23, 5): 1.05 to 1.15 V<br>• DDR_$V_{DDQ}$: 1.14 to 1.26 V (DDR4) / 1.283 to 1.45 V (DDR3L)<br>• $V_{DD18}$, ADC_$AV_{DD18}$, PLLn_$AV_{DD18}$ (n = 1, 23, 4, 5, 6): 1.62 to 1.98 V<br>• OTP_$V_{DD18}$, USB_$V_{DD18}$: 1.65 to 1.95 V<br>• $PV_{DD}$: 2.97 to 3.63 V<br>• USB_$V_{DD33}$: 3.00 to 3.60 V<br>• SDn_$PV_{DD}$ (n = 0, 1), SPI_$PV_{DD}$: 2.97 to 3.63 V / 1.70 to 1.95 V<br>• $PV_{DD182533}$: 2.97 to 3.63 V / 2.25 to 2.75 V / 1.62 to 1.98 V |

### 1.1.13 Temperature Range

| Item | Description |
|---|---|
| Temperature range | [RZ/Five]<br>• $T_a$: −40°C to +85°C*1<br>• $T_j$: −40°C to +125°C |

Note 1. If wider temp is required than this range, use case has to be investigated.

### 1.1.14 Quality level

| Item | Description |
|---|---|
| Quality level | [RZ/Five]<br>• Industrial usage, etc. |

### 1.1.15 Package

| Item | Description |
|---|---|
| Package | [RZ/Five]<br>• 361-pin LFBGA, 13-mm square, 0.5-mm pitch<br>• 266-pin LFBGA, 11-mm square, 0.5-mm pitch |

## 1.2 Block Diagram

The LSI internal bus of this LSI consists of the ACPU bus, MCPU bus, and system bus. **Figure 1.1** shows the configuration of the buses.

**ACPU bus:**

A bus connected to AX45MP, DDR memory controllers, image processing units, and Storage and Network

**MCPU bus:**

A bus connected to serial interface units

**System bus:**

A bus connected to the control registers of each unit

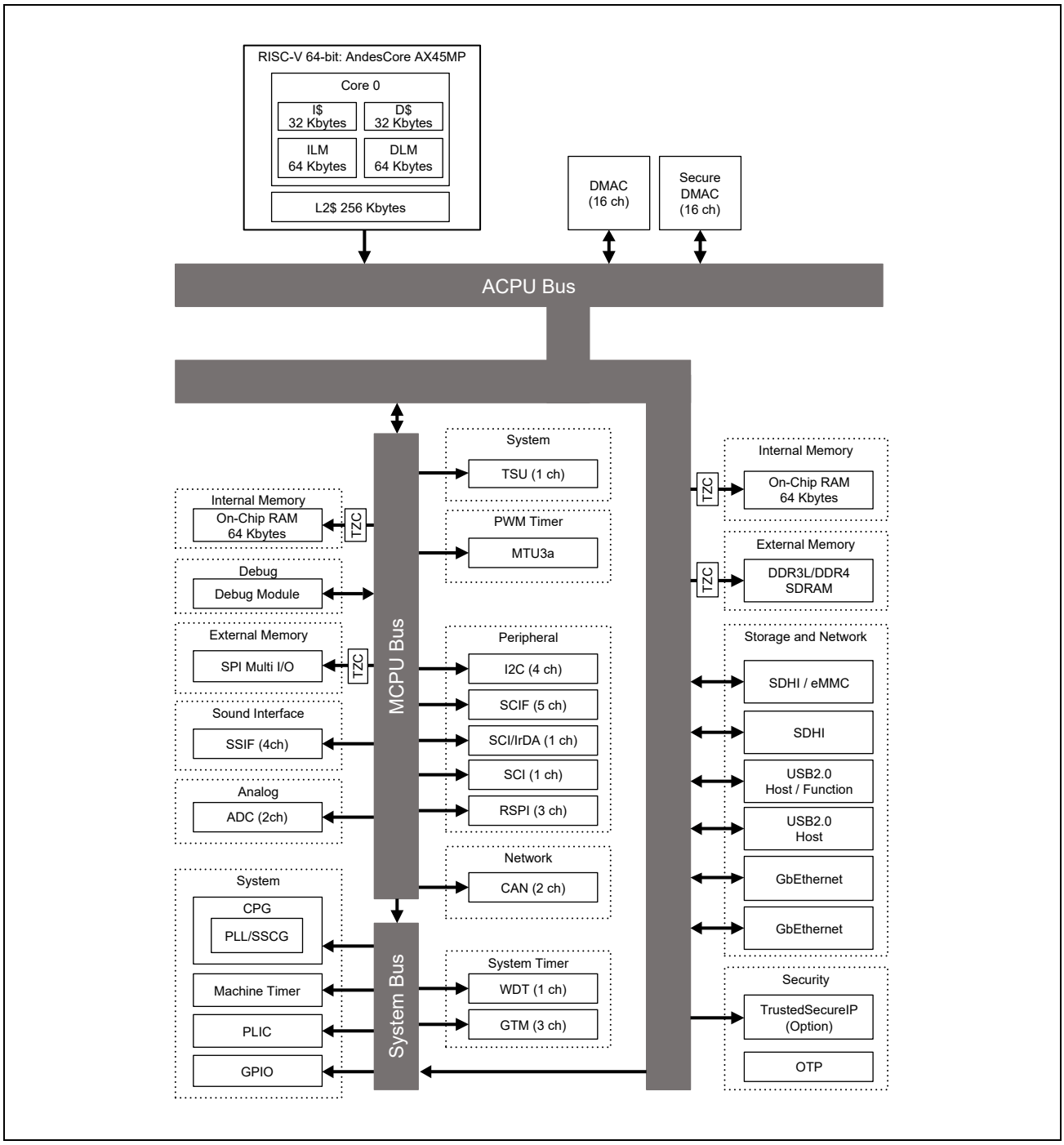



Figure 1.1 Configuration of LSI Internal Bus

## 1.3 Product Lineup

Table 1.1 Product Lineup

| Group | Package | Part Number | Security*1 |
|---|---|---|---|
| RZ/Five | 13 mm BGA | R9A07G043F05GBG | Available |
| | | R9A07G043F01GBG | Not supported |
| | 11 mm BGA | R9A07G043F04GBG | Available |
| | | R9A07G043F00GBG | Not supported |

Note 1. The product with security function supports the following features.
— Trusted Secure IP
— Secure Boot
— Secure Debug
— HW Key protection
— True Random Generator

# 2. Pin

## 2.1 Pin Assignment

Refer to attached excel file for the “ball view” about pin assignment of this LSI.
(Please double-click the icon on the right side) 

## 2.2 External Pins and Multiplexed Functional Pins

Refer to attached excel file for the “pn function list” about information of external pins and multiplexed functional pins of this LSI.
(Please double-click the icon on the right side) 

# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage (3.3 V) | | $PV_{DD}$ | −0.5 to +3.8 | V |
| | | $USB\_V_{DD33}$ | | |
| Power supply voltage (1.8-V/3.3-V switchable) | | $SD0\_PV_{DD}$ | −0.5 to +3.8 | V |
| | | $SD1\_PV_{DD}$ | | |
| | | $SPI\_PV_{DD}$ | | |
| Power supply voltage (1.8-V/ 2.5-V/ 3.3-V switchable) | | $PV_{DD182533\_0/1}$ | −0.5 to +3.8 | V |
| Power supply voltage (1.8 V) | | $V_{DD18}$ | −0.5 to +2.5 | V |
| | | $PLL1\_AV_{DD18}$ | | |
| | | $PLL23\_AV_{DD18}$ | | |
| | | $PLL4\_AV_{DD18}$ | | |
| | | $PLL6\_AV_{DD18}$ | | |
| | | $USB\_V_{DD18}$ | | |
| | | $ADC\_AV_{DD18}$ | | |
| | | $OTP\_V_{DD18}$ | | |
| DDR power supply voltage (DDR4/ DDR3L switchable) | | $DDR\_V_{DDQ}$ | −0.5 to +2.5 | V |
| Power supply voltage (1.1-V) | | $V_{DD}$ | −0.5 to +1.5 | V |
| | | $PLL23\_DV_{DD11}$ | | |
| Input voltage | 3.3-V I/O input pins | — | −0.3 to 3.3-V power supply ($PV_{DD}$, $USB\_V_{DD33}$) + 0.3 | V |
| | 1.8-V/3.3-V switchable I/O input pins | — | −0.3 to 1.8-V/3.3-V switchable power supply ($SD0\_PV_{DD}$, $SD1\_PV_{DD}$, $SPI\_PV_{DD}$) + 0.3 | V |
| | 1.8-V/2.5-V/3.3-V switchable I/O input pins | — | −0.3 to 1.8-V/2.5-V/3.3-V switchable power supply ($PV_{DD182533\_0.1}$) + 0.3 | V |
| | 1.8-V I/O input pins | — | −0.3 to 1.8-V power supply ($V_{DD18}$, $CSI\_V_{DD18}$, $USB\_V_{DD18}$) + 0.3 | V |
| Operating temperature | Ambient temperature | $T_a$ | −40°C to +85°C*1 | °C |
| | Junction temperature | $T_j$ | −40°C to +125°C | °C |
| Storage temperature | Ambient temperature | $T_{stg}$ | −40°C to +150°C | °C |

Note 1. If wider temp is required than this range, use case has to be investigated.

## 3.2 Power Supply

Table 3.2 Power Supply

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Power supply voltage (3.3 V) | $PV_{DD}$ | 2.97 | 3.30 | 3.63 | V | — |
| Power supply voltage (1.8 V) | $V_{DD18}$, $ADC\_AV_{DD18}$ | 1.62 | 1.80 | 1.98 | V | — |
| | $OTP\_V_{DD18}$ | 1.65 | 1.80 | 1.95 | V | — |
| Power supply voltage (1.1 V) | $V_{DD}$ | 1.05 | 1.10 | 1.15 | V | — |
| Power supply voltage (USB) | $USB\_V_{DD33}$ | 3.00 | 3.30 | 3.60 | V | — |
| | $USB\_V_{DD18}$ | 1.65 | 1.80 | 1.95 | V | — |
| Power supply voltage (SD) | $SD0\_PV_{DD}$, $SD1\_PV_{DD}$ | 2.97 | 3.30 | 3.63 | V | When 3.3 V is supplied |
| | | 1.70 | 1.80 | 1.95 | V | When 1.8 V is supplied |
| Power supply voltage (SPI) | $SPI\_PV_{DD}$ | 2.97 | 3.30 | 3.63 | V | When 3.3 V is supplied |
| | | 1.70 | 1.80 | 1.95 | V | When 1.8 V is supplied |
| Power supply voltage (Ether) | $PV_{DD182533\_0/1}$ | 2.97 | 3.30 | 3.63 | V | When 3.3 V is supplied |
| | | 2.25 | 2.50 | 2.75 | V | When 2.5 V is supplied |
| | | 1.62 | 1.80 | 1.98 | V | When 1.8 V is supplied |
| Power supply voltage (DDR) | $DDR\_V_{DDQ}$ | 1.14 | 1.20 | 1.26 | V | When using DDR4 |
| | | 1.283 | 1.35 | 1.45 | V | When using DDR3L |
| Power supply voltage (PLL) | $PLL1\_AV_{DD18}$, $PLL23\_AV_{DD18}$, $PLL4\_AV_{DD18}$, $PLL6\_AV_{DD18}$ | 1.62 | 1.80 | 1.98 | V | — |
| | $PLL23\_DV_{DD11}$ | 1.05 | 1.10 | 1.15 | V | — |

## 3.3 Power-On/Power-Off Sequence

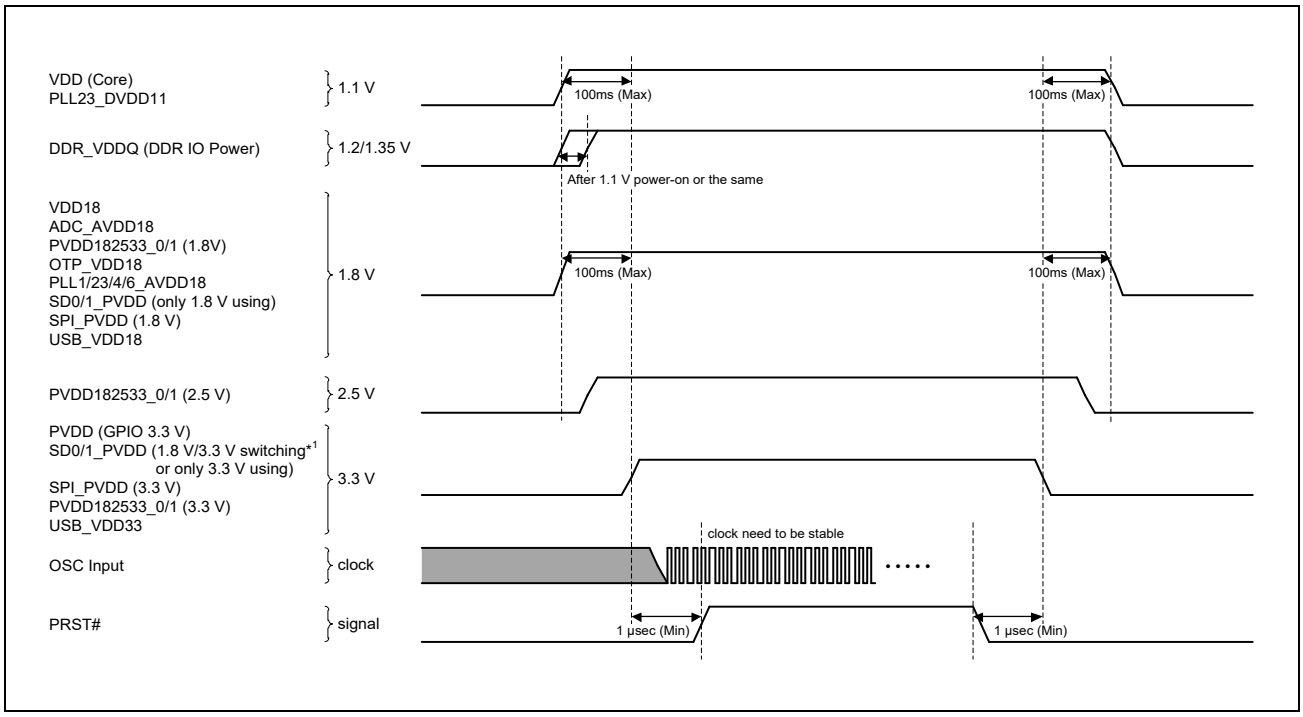


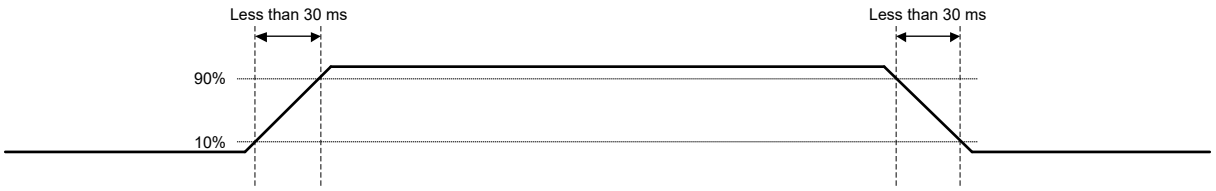

Figure 3.1 Power-On/Power-Off Sequence

NOTES

1. Turn on 3.3 V after 1.1 V/1.8 V.

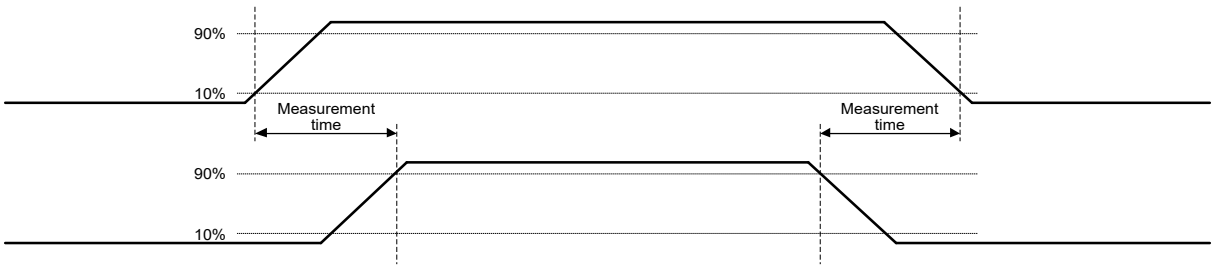
   *Note 1.* About SD0/1_$PV_{DD}$, especially in the case of switching between 1.8 V and 3.3 V at same power rail, 1.8-V power-on/off timing can also follow 3.3-V power rail sequence as shown in the **Figure 3.1**.

2. Turn on the DDR IO power supply at the same time as or after the 1.1-V power supply.
3. From first power rising start to last power rising end must be within 100 ms.
4. The power-off sequence is the reverse of the power-on sequence
   (PRST# → Low ⇨ 3.3 V = OFF ⇨ Other = OFF)
5. PRST# should be changed from Low to High after the 3.3-V power supply is turned on, after 1 µsec, and after the input clock from the oscillator stabilizes.
6. Refer to SD0/1_$PV_{DD}$ when connecting eMMC.




**Note:** The rise/fall time of each power supply should be within 30 msec.
Start point / end point of rising / falling time of each power supply should be 10% or 90% level of each power supply.

Figure 3.2 Power Up Time/Power Down Time (1)




**Note:** In case of there is restriction of sequence between different power supply, measurement time is starting point that is 10% of earlier rising power voltage level to end point that is 90% of later rising power voltage level, and starting point that is 90% of earlier falling power voltage level to end point that is 10% of later falling power voltage level.

Figure 3.3 Power Up Time/Power Down Time (2)

## 3.4 DC Characteristics

Table 3.3 DC Characteristics (1) [3.3-V I/O]

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| High-level input voltage | | $V_{IH}$ | 2 | — | $PV_{DD}$ + 0.3 | V | |
| Low-level input voltage | | $V_{IL}$ | −0.3 | — | 0.8 | V | |
| Hysteresis threshold ↑ | | $V_T$+ | 0.9 | — | 2.1 | V | |
| Hysteresis threshold ↓ | | $V_T$− | 0.7 | — | 1.9 | V | |
| Input hysteresis voltage | | $V_{HYS}$ | 0.306 | — | 0.420 | V | |
| Output logic high voltage | ($I_{OH}$ = –2mA) | $V_{OH}$ | $PV_{DD}$ – 0.4 | — | $PV_{DD}$ | V | |
| | ($I_{OH}$ = –4mA) | | | | | | |
| | ($I_{OH}$ = –8mA) | | | | | | |
| | ($I_{OH}$ = –12mA) | | | | | | |
| Output logic low voltage | ($I_{OL}$ = 2mA) | $V_{OL}$ | 0 | — | 0.4 | V | |
| | ($I_{OL}$ = 4mA) | | | | | | |
| | ($I_{OL}$ = 8mA) | | | | | | |
| | ($I_{OL}$ = 12mA) | | | | | | |
| Weak pull-up resistor (input mode) | | $R_{UP}$ | 7K | — | 100K | Ω | |
| Weak pull-down resistor (input mode) | | $R_{DN}$ | 7K | — | 100K | Ω | |
| Input leakage current | | $I_{LI}$ | — | — | 5 | μA | 0V ≤ $V_{in}$ ≤ $PV_{DD}$<br>In case of 3state buffer, the leak current when output mode OFF |

**Note:** $V_{in}$ means input voltage of external input pin.

**Note:** Schmitt can be used at only RIIC mode.

Table 3.4 DC Characteristics (2) [1.8-V I/O]

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| High-level input voltage | | $V_{IH}$ | 0.65 × $V_{DD18}$ | — | $V_{DD18}$ + 0.3 | V | |
| Low-level input voltage | | $V_{IL}$ | −0.3 | — | 0.35 × $V_{DD18}$ | V | |
| Output logic high voltage | ($I_{OH}$ = –2mA) | $V_{OH}$ | $V_{DD18}$ – 0.4 | — | $V_{DD18}$ | V | |
| | ($I_{OH}$= –4mA) | | | | | | |
| | ($I_{OH}$ = –8mA) | | | | | | |
| | ($I_{OH}$ = –12mA) | | | | | | |
| Output logic low voltage | ($I_{OL}$ = 2mA) | $V_{OL}$ | 0 | — | 0.4 | V | |
| | ($I_{OL}$ = 4mA) | | | | | | |
| | ($I_{OL}$ = 8mA) | | | | | | |
| | ($I_{OL}$ = 12mA) | | | | | | |

Table 3.5 DC Characteristics (3) [3.3-V Input]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2.3 | — | $PV_{DD}$ + 0.3 | V | |
| Low-level input voltage | $V_{IL}$ | −0.3 | — | 0.8 | V | |
| Hysteresis threshold ↑ | $V_T$+ | 0.9 | — | 2.1 | V | |
| Hysteresis threshold ↓ | $V_T$− | 0.7 | — | 1.9 | V | |
| Input hysteresis voltage | $V_{HYS}$ | 0.306 | — | 0.420 | V | |

Table 3.6 DC Characteristics (4) [1.8-V Input]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 0.65 × $V_{DD18}$ | — | $V_{DD18}$ + 0.3 | V | |
| Low-level input voltage | $V_{IL}$ | −0.3 | — | 0.35 × $V_{DD18}$ | V | |

Table 3.7 DC Characteristics (5) [RGMII/MII]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Power supply voltage | $PV_{DD182533\_n}$ | 2.97 | 3.3 | 3.63 | V | 3.3-V RGMII/MII |
| Input logic high | $V_{IH}$ | 2.6 | — | — | V | |
| Input logic low | $V_{IL}$ | — | — | 0.7 | V | |
| Output logic high voltage @ 7.7 mA | $V_{OH}$ | 2.1 | — | 3.6 | V | |
| Output logic low voltage @ 9.3 mA | $V_{OL}$ | 0 | — | 0.5 | V | |
| Power supply voltage | $PV_{DD182533\_n}$ | 2.25 | 2.5 | 2.75 | V | 2.5-V RGMII/MII |
| Input logic high | $V_{IH}$ | 1.9 | — | — | V | |
| Input logic low | $V_{IL}$ | — | — | 0.7 | V | |
| Output logic high voltage | $V_{OH}$ | 2.0 | — | $PV_{DD182533\_n}$ | V | |
| Output logic low voltage | $V_{OL}$ | $V_{SS}$ | — | 0.4 | V | |
| Power supply voltage | $PV_{DD182533\_n}$ | 1.62 | 1.8 | 1.98 | V | 1.8-V RGMII/MII |
| Input logic high | $V_{IH}$ | 0.7 × $PV_{DD182533\_n}$ | — | $PV_{DD182533\_n}$ + 0.3 | V | |
| Input logic low | $V_{IL}$ | $V_{SS}$ − 0.3 | — | 0.3 × $PV_{DD182533\_n}$ | V | |
| Output logic high @ $I_{OH}$ = 100 µA | $V_{OH}$ | 0.85 × $PV_{DD182533\_n}$ | — | $PV_{DD182533\_n}$ | V | |
| Output logic low @ $I_{OL}$ = 100 µA | $V_{OL}$ | $V_{SS}$ | — | 0.15 × $PV_{DD182533\_n}$ | V | |

**Note:** n = 0, 1

Table 3.8 DC Characteristics (6) [3.3 V I/O (SD, QSPI)]

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| High-level input voltage | | $V_{IH}$ | 0.625 × $SDn\_PV_{DD}$ | — | $SDn\_PV_{DD}$ + 0.3 | V | |
| Low-level input voltage | | $V_{IL}$ | $SDn\_PV_{DD}$ − 0.3 | — | 0.25 × $SDn\_PV_{DD}$ | V | |
| Output logic high voltage | (× 0.5) | $V_{OH}$ | 0.75 × $SDn\_PV_{DD}$ | — | $SDn\_PV_{DD}$ | V | |
| | (× 0.75) | | | | | | |
| | (× 1.0) | | | | | | |
| | (× 1.5) | | | | | | |
| Output logic low voltage | (× 0.5) | $V_{OL}$ | 0 | — | 0.125 × $SDn\_PV_{DD}$ | V | |
| | (× 0.75) | | | | | | |
| | (× 1.0) | | | | | | |
| | (× 1.5) | | | | | | |

Table 3.9 DC Characteristics (7) [1.8 V I/O (SD, QSPI)]

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| High-level input voltage | | $V_{IH}$ | 1.27 | — | 2.00 | V | |
| Low-level input voltage | | $V_{IL}$ | $SDn\_PV_{DD}$ − 0.3 | — | 0.58 | V | |
| Output logic high voltage | (× 0.5) | $V_{OH}$ | 0.8 × $SDn\_PV_{DD}$ | — | $SDn\_PV_{DD}$ | V | |
| | (× 0.75) | | | | | | |
| | (× 1.0) | | | | | | |
| | (× 1.5) | | | | | | |
| Output logic low voltage | (× 0.5) | $V_{OL}$ | 0 | — | 0.2 × $SDn\_PV_{DD}$ | V | |
| | (× 0.75) | | | | | | |
| | (× 1.0) | | | | | | |
| | (× 1.5) | | | | | | |

Table 3.10 DC Characteristics(8) [$I^2C$ Open Drain 3.3 V I/O]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| External pull-up supply | $V_{VDDP}$ | 2.7 | — | $PV_{DD}$ | V | |
| Input high voltage | $V_{IH}$ | 0.7 × $V_{VDDP}$ | — | $V_{VDDP}$ + 0.5 | V | |
| Input Low Voltage | $V_{IL}$ | −0.5 | — | 0.3 × $V_{VDDP}$ | V | |
| Low level output current | $I_{OL}$ | 20 | — | — | mA | $V_{OL}$ = 0.4 V |
| Low level output voltage | $V_{OL}$ | — | — | 0.4 | V | $V_{VDDP}$ > 2 V |
| Input hysteresis | $V_{HYST}$ | 0.1 × $V_{VDDP}$ | — | — | mV | |

Table 3.11 DC Characteristics (9) [1.2-V Input (DDR4)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| DC input high level | $V_{IH}$(DC) | $V_{REF}$ + 0.068 | — | — | V | |
| DC input low level | $V_{IL}$(DC) | — | — | $V_{REF}$ − 0.068 | V | |
| AC input high level | $V_{IH}$(AC) | $V_{REF}$ + 0.093 | — | — | V | |
| AC input Low level | $V_{IL}$(AC) | — | — | $V_{REF}$ − 0.093 | V | |
| DC differential input high | $V_{IHdiff}$ | 0.136 | — | — | V | |
| DC differential input low | $V_{ILdiff}$ | — | — | −0.136 | V | |
| AC differential input high | $V_{IHdiff}$(AC) | 2 × ($V_{IH}$(AC) − $V_{REF}$) | — | — | V | |
| AC differential input low | $V_{ILdiff}$(AC) | — | — | 2 × ($V_{REF}$ − $V_{IL}$(AC)) | V | |
| Differential input cross point voltage relative to 0.8 × $V_{DDIO}$ for DQS | $V_{IX}$(DQS) | −0.15 | — | 0.06 | V | |

Table 3.12 DC Characteristics (10) [1.35-V Input (DDR3L)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| DC input high level | $V_{IH}$(DC) | $V_{REF}$ + 0.09 | — | — | V | |
| DC input low level | $V_{IL}$(DC) | — | — | $V_{REF}$ − 0.09 | | $V_{REF}$ =0.5 x DDR_$V_{DDQ}$ |
| AC input high level | $V_{IH}$(AC) | $V_{REF}$ + 0.135 | — | — | V | |
| AC input low level | $V_{IL}$(AC) | — | — | $V_{REF}$ − 0.135 | V | $V_{REF}$ =0.5 x DDR_$V_{DDQ}$ |
| DC differential input high | $V_{IHdiff}$ | 0.18 | — | — | V | |
| DC differential input low | $V_{ILdiff}$ | — | — | −0.18 | V | |
| AC differential input high | $V_{IHdiff}$(AC) | 2 × ($V_{IH}$(AC) − $V_{REF}$) | — | — | V | |
| AC differential input low | $V_{ILdiff}$(AC) | — | — | 2 × ($V_{REF}$ − $V_{IL}$(AC)) | V | $V_{REF}$ =0.5 x DDR_$V_{DDQ}$ |
| Differential input cross point voltage relative to 0.5 × DDR_VDDQ for DQS | $V_{IX}$(DQS) | −0.075 | — | 0.075 | V | |

Table 3.13 DC Characteristics (11) [1.2-V Output (DDR4)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| DC output high measurement level (for IV curve linearity) | $V_{OH}$(DC) | — | 1.1 × DDR_$V_{DDQ}$ | — | V | The swing of ± 0.15 × DDR_$V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of 40Ω and an effective test load of 50Ω to $V_{TT}$ = DDR_$V_{DDQ}$. |
| DC output mid measurement level (for IV curve linearity) | $V_{OM}$(DC) | — | 0.8 × DDR_$V_{DDQ}$ | — | V | |
| DC output low measurement level (for IV curve linearity) | $V_{OL}$(DC) | — | 0.5 × DDR_$V_{DDQ}$ | — | V | |
| AC output high measurement level (for output slew rate) | $V_{OH}$(AC) | — | 0.85 × DDR_$V_{DDQ}$ | — | V | |
| AC output low measurement level (for output slew rate) | $V_{OL}$(AC) | — | 0.55 × DDR_$V_{DDQ}$ | — | V | |

Table 3.14 DC Characteristics (12) [1.35-V Output (DDR3L)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| DC output high measurement level (for IV curve linearity) | $V_{OH}$(DC) | — | 0.8 × DDR_$V_{DDQ}$ | — | V | The swing of ± 0.1 × DDR_$V_{DDQ}$ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT}$ = DDR_$V_{DDQ}$/2. |
| DC output mid measurement level (for IV curve linearity) | $V_{OM}$(DC) | — | 0.5 × DDR_$V_{DDQ}$ | — | V | |
| DC output low measurement level (for IV curve linearity) | $V_{OL}$(DC) | — | 0.2 × DDR_$V_{DDQ}$ | — | V | |
| AC output high measurement level (for output slew rate) | $V_{OH}$(AC) | — | VTT + 0.1 × DDR_$V_{DDQ}$ | — | V | |
| AC output low measurement level (for output slew rate) | $V_{OL}$(AC) | — | VTT − 0.1 × DDR_$V_{DDQ}$ | — | V | |

Table 3.15 DC Characteristics (13) [DDR4 Cross Point Voltage for Differential Output Signals (CK/DQS)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Differential output cross point voltage relative to 0.67 × DDR_VDDQ | $V_{OX}$(CK/DQS) | −0.06 | — | 0.06 | V | |

Table 3.16 DC Characteristics (14) [DDR3L Cross Point Voltage For Differential Output Signals (CK/DQS)]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Differential output cross point voltage relative to 0.5 × DDR_VDDQ | $V_{OX}$(CK/DQS) | −0.1 | — | 0.1 | V | |

Table 3.17 DC Characteristics (15) [USB 2.0]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Input levels for low/full speed | | | | | | |
| High (driven) | $V_{IH}$ | 2.0 | — | — | V | |
| Low | $V_{IL}$ | — | — | 0.8 | V | |
| Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | |
| Differential common mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | |
| Input levels for high speed | | | | | | |
| High-speed squelch detection threshold (differential signal amplitude) | $V_{HSSQ}$ | 100 | — | 150 | mV | |
| High-speed data signaling common mode voltage range (guideline for receiver) | $V_{HSCM}$ | −50 | — | 500 | mV | |
| Output levels for low/full speed | | | | | | |
| Low | $V_{OL}$ | 0.0 | — | 0.3 | V | |
| High (driven) | $V_{OH}$ | 2.8 | — | 3.6 | V | |
| Output signal crossover voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | |
| Output levels for high-speed | | | | | | |
| High-speed idle level | $V_{HSOI}$ | −10.0 | — | 10.0 | mV | |
| High-speed data signaling high | $V_{HSOH}$ | 360 | — | 440 | mV | |
| High-speed data signaling low | $V_{HSOL}$ | −10.0 | — | 10.0 | mV | |
| Chirp J level (differential voltage) | $V_{CHIRPJ}$ | 700 | — | 1100 | mV | |
| Chirp K level (differential voltage) | $V_{CHIRPK}$ | −900 | — | −500 | mV | |

Table 3.18 DC Characteristics (16) [ADC]

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Resolution | — | — | 12 | — | Bit | |
| Analog input channel | — | — | — | 2 | Channel | |
| Analog input range | AIN | $V_{SS}$ | — | ADC_$AV_{DD18}$ | V | |
| Differential non-linearity | DNL | — | — | ±3.0 | LSB | |
| Integral non-linearity | INL | — | — | ±6.0 | LSB | |
| Full-scale error | — | — | ±10 | ±20 | LSB | |
| Offset error | — | — | ±10 | ±20 | LSB | |
| Analog input capacitance | $C_{IN}$ | — | — | 12.5 | pF | |
| Analog input resistance | $R_{IN}$ | — | — | 1754 | Ω | |
| External capacitance | $C_{EXT}$ | — | — | (*1) | pf | |
| External resistance | $R_{EXT}$ | — | — | (*1) | Ω | |

Note 1. Refer to **Figure 3.4** for Cext and Rext.
The Cext and Rext need to satisfy the sampling time.
A/D conversion time = sampling time (6T to 2800T) + 14T.
T stands for the cycle of ADIVCLK (20 MHz).
If A/D conversion is performed with the minimum conversion time, the sampling time must be 6T.
(Minimum conversion time per channel is 1 µs when A/D conversion clock ADIVCLK is 20 MHz.)

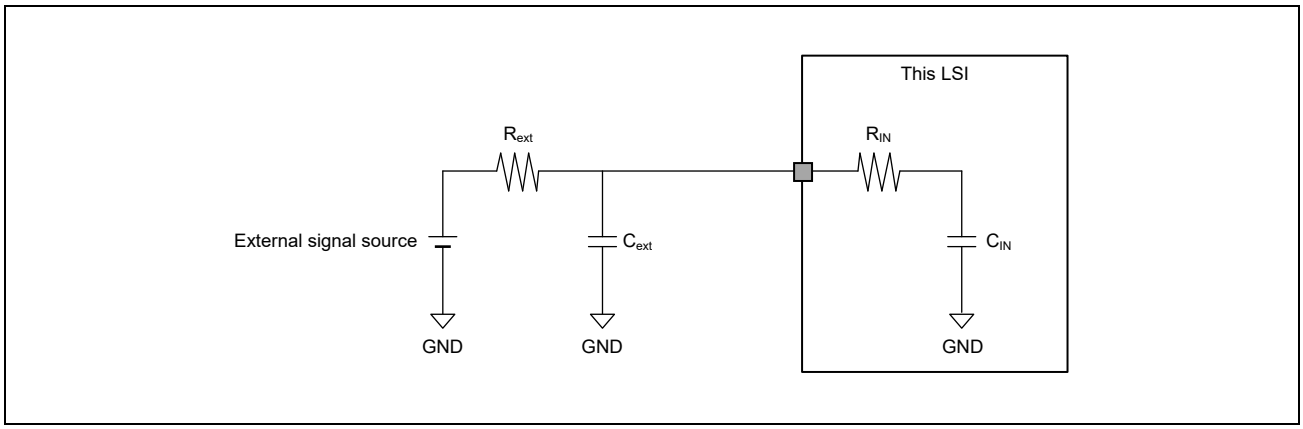



Figure 3.4 Analog Input Equivalent Circuit

Table 3.19 DC Characteristics (17) [Current Consumption]

| Item | Power rail symbol | Max Current | Unit | Remarks |
|---|---|---|---|---|
| Power Supply voltage(3.3V) | $PV_{DD}$ | 430 | mA | $PV_{DD}$=3.6V |
| Power Supply voltage(1.8V) | $V_{DD18}$ | 20 | mA | $V_{DD18}$=1.98V |
| | $OTP\_AV_{DD18}$ | 20 | mA | $OTP\_V_{DD18}$=1.95V |
| | $ADC\_AV_{DD18}$ | 10 | mA | $ADC\_AV_{DD18}$=1.98V |
| Power Supply voltage(1.1V) | $V_{DD}$ | 2010 | mA | $V_{DD}$=1.15V, Condition: AX45MP, Dhrystone |
| Power supply voltage (USB/3.3V) | $USB\_V_{DD33}$ | 20 | mA | $USB\_V_{DD33}$=3.6V |
| Power supply voltage (USB/1.8V) | $USB\_V_{DD18}$ | 140 | mA | $USB\_V_{DD18}$=1.95V |
| Power supply voltage (SD/3.3V) | $SD0\_PV_{DD}$ | 260 | mA | $SD0\_PV_{DD}$=3.63V |
| | $SD1\_PV_{DD}$ | 170 | mA | $SD1\_PV_{DD}$=3.63V |
| Power supply voltage (SD/1.8V) | $SD0\_PV_{DD}$ | 110 | mA | $SD0\_PV_{DD}$=1.95V |
| | $SD1\_PV_{DD}$ | 70 | mA | $SD1\_PV_{DD}$=1.95V |
| Power supply voltage (SPI/3.3V) | $SPI\_PV_{DD}$ | 50 | mA | $SPI\_PV_{DD}$=3.63V |
| Power supply voltage (SPI/1.8V) | $SPI\_PV_{DD}$ | 100 | mA | $SPI\_PV_{DD}$=1.95V |
| Power supply voltage (Ether/3.3V) | $PV_{DD182533\_n}$ | 380 | mA | $PV_{DD182533\_n}$=3.63V when 2 channels are in use |
| Power supply voltage (Ether/2.5V) | $PV_{DD182533\_n}$ | 240 | mA | $PV_{DD182533\_n}$=2.75V when 2 channels are in use |
| Power supply voltage (Ether/1.8V) | $PV_{DD182533\_n}$ | 140 | mA | $PV_{DD182533\_n}$=1.98V when 2 channels are in use |
| Power supply voltage (DDR/1.2V) | $DDR\_V_{DDQ}$ | 220 | mA | $DDR\_V_{DDQ}$=1.26V |
| Power supply voltage (DDR/1.35V) | $DDR\_V_{DDQ}$ | 210 | mA | $DDR\_V_{DDQ}$=1.45V |
| Power supply voltage (PLL/1.8V) | $PLL1\_AV_{DD18}$ | 10 | mA | $PLL1\_AV_{DD18}$=1.98V |
| | $PLL23\_AV_{DD18}$ | 20 | mA | $PLL23\_AV_{DD18}$=1.98V |
| | $PLL4\_AV_{DD18}$ | 10 | mA | $PLL4\_AV_{DD18}$=1.98V |
| | $PLL6\_AV_{DD18}$ | 10 | mA | $PLL6\_AV_{DD18}$=1.98V |
| Power supply voltage (PLL/1.1V) | $PLL23\_DV_{DD11}$ | 20 | mA | $PLL23\_DV_{DD11}$=1.15V |

**Note:** $T_j$ = 125°C, n = 0, 1

# 3.5 AC Characteristics

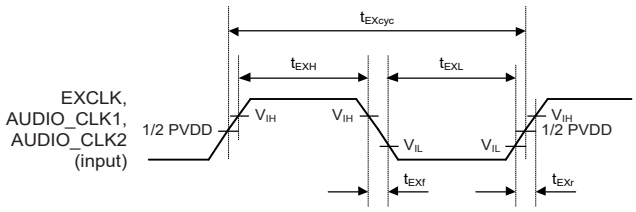
Conditions: $V_{DD}$ = PLL23_$DV_{DD11}$ = 1.1 ± 0.05 V,
PLL1_$AV_{DD18}$ = PLL23_$AV_{DD18}$ = PLL4_$AV_{DD18}$ = PLL6_$AV_{DD18}$ = 1.8 ± 0.18 V,
ADC_$AV_{DD18}$ = $V_{DD18}$ = 1.8 ± 0.18 V, OTP_$V_{DD18}$ = 1.8 V ± 0.15 V,
USB_$V_{DD18}$ = 1.8 ± 0.15 V,
$PV_{DD}$ = 3.3 ± 0.33 V, USB_$V_{DD33}$ = 3.3 ± 0.3 V, DDR_$V_{DDQ}$ = 1.2 ± 0.06 V/1.283 to 1.45 V,
SPI_$PV_{DD}$ = SDn_$PV_{DD}$ (n = 0, 1) = 3.3 ± 0.33 V/1.70 to 1.95 V,
$PV_{DD182533\_n}$ (n = 0, 1) = 3.3 ± 0.33 V/2.5 ± 0.25 V/1.8 ± 0.18 V, $V_{SS}$ = 0 V,
$T_a$ = −40 to +85°C, $T_j$ = −40 to +125°C

## 3.5.1 Clock Timing

Table 3.20 Clock Timing Table

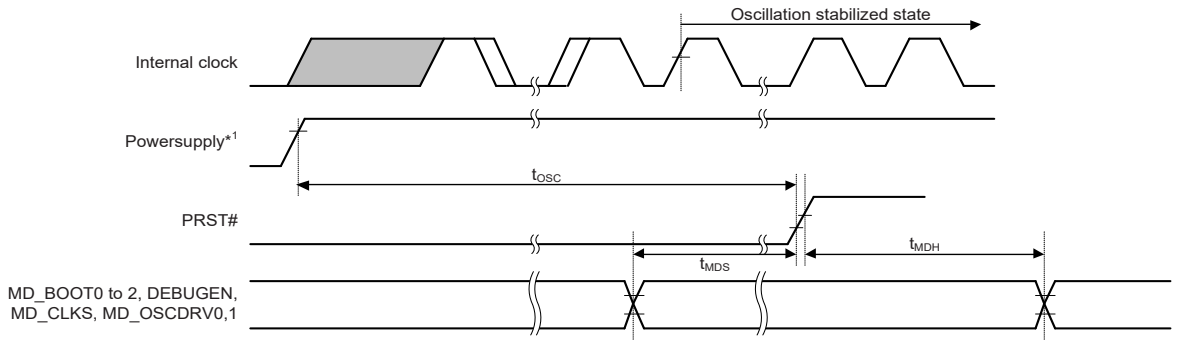
| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| EXCLK clock input frequency | $f_{EX}$ | 24 – 50ppm*1 | 24 + 50ppm*1 | MHz | **Figure 3.5** |
| EXCLK clock input cycle time | $t_{EXcyc}$ | 41.67 | 41.67 | ns | |
| AUDIO_CLK1, AUDIO_CLK2 clock input frequency (external clock is input) | $f_{EX}$ | 10 | 50 | MHz | |
| AUDIO_CLK1, AUDIO_CLK2 clock input cycle time (external clock is input) | $t_{EXcyc}$ | 20 | 100 | ns | |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2 clock input low level pulse width | $t_{EXL}$ | 0.4 | 0.6 | $t_{EXcyc}$ | |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2 clock input high level pulse width | $t_{EXH}$ | 0.4 | 0.6 | $t_{EXcyc}$ | |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2 clock input rise time | $t_{EXr}$ | — | 4 | ns | |
| EXCLK, AUDIO_CLK1, AUDIO_CLK2 clock input fall time | $t_{EXf}$ | — | 4 | ns | |
| Oscillator stabilization time | $t_{OSC}$ | — | 1 | ms | **Figure 3.6**, **Figure 3.7** |
| Mode hold time | $t_{MDH}$ | — | 100 | ns | |
| Mode setup time | $t_{MDS}$ | — | 100 | ns | |

Note 1. When using RGMII interface. If not using RGMII mode, this spec is ±100 ppm.




**Note:** When the clock is input on the EXCLK, AUDIO_CLK1 or AUDIO_CLK2

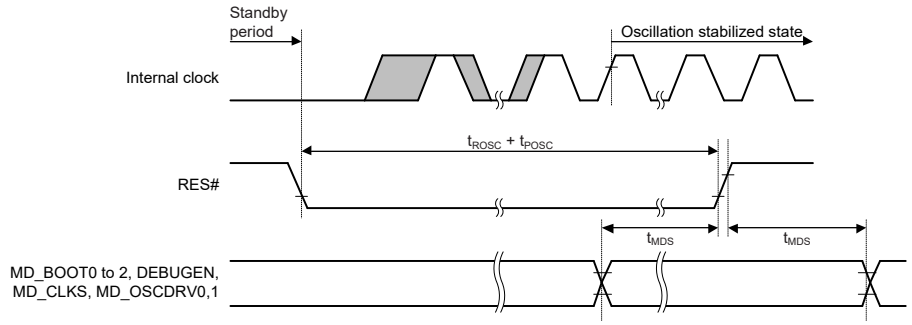
Figure 3.5 EXCLK, AUDIO_CLK1 and AUDIO_CLK2 Clock Input Timing




Note 1.

$V_{DD}$, PLL23_$DV_{DD11}$, PLL1_$AV_{DD18}$, PLL23_$AV_{DD18}$, PLL4_$AV_{DD18}$, PLL6_$AV_{DD18}$, ADC_$AV_{DD18}$, $V_{DD18}$, OTP_$V_{DD18}$, USB_$V_{DD18}$, $PV_{DD}$,USB_$V_{DD33}$, DDR_$V_{DDQ}$, SPI_$PV_{DD}$, SD0_$PV_{DD}$, SD1_$PV_{DD}$, $PV_{DD182533}$_0, $PV_{DD182533}$_1

Figure 3.6 Power-On Oscillation Settling Time




**Note:** Oscillation setting time when the internal oscillator is used.

Figure 3.7 Oscillation Settling Time on Return from Standby (Return by Reset)

## 3.5.2 SDHI Access Timing

### 3.5.2.1 SDHI Access Timing (SDR 3.3-V)

Table 3.21 SDHC AC Access Timing (SDR at 3.3-V Operation)

| Item | Symbol | Default Speed Mode (16.67 MHz) | | High Speed Mode (33.33 MHz) | | Unit | Figures |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| SD_CLK clock cycle | $t_{SDCYC}$ | 60.00 | — | 30.0 | — | ns | **Figure 3.8** |
| SD_CLK clock high level width | $t_{SDWH}$ | 23.50 | — | 13.50 | — | ns | |
| SD_CLK clock low level width | $t_{SDWL}$ | 23.50 | — | 13.50 | — | ns | |
| SD_CLK clock rise time | $t_{SDLH}$ | — | 10 | — | 3 | ns | |
| SD_CLK clock fall time | $t_{SDHL}$ | — | 10 | — | 3 | ns | |
| SD_CMD,SD_DATA output delay | $t_{SDODLY}$ | −4.50 | 4.0 | −4.50 | 4.0 | ns | |
| SD_CMD,SD_DATA input set up time | $t_{SDIS}$ | 5.5 | — | 5.5 | — | ns | |
| SD_CMD,SD_DATA input hold time | $t_{SDIH}$ | 2.0 | — | 2.0 | — | ns | |
| SD_CMD,SD_DATA input data width | $t_{SDIDW}$ | — | — | — | — | ns | |

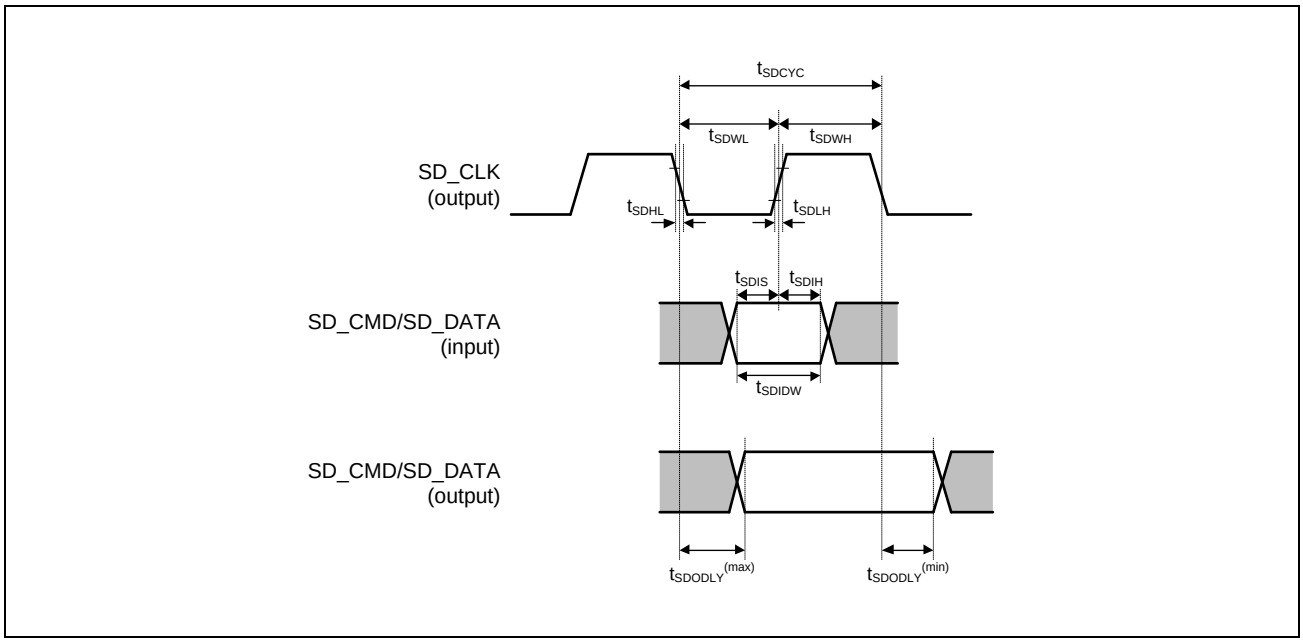



Figure 3.8 SDHC Interface Timing (SDR 3.3-V Power Supply)

NOTE

The disclosure of other characteristics of the SD interface needs the conclusion of the following agreement.

- SD Host/Ancillary Product License Agreement (SD HALA)

For details, contact your local sales representatives.

## 3.5.3 eMMC Access Timing

### 3.5.3.1 eMMC Host Interface Timing (Default)

Table 3.22 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| SD0_CLK clock cycle | $t_{MMCPP}$ | 40.00 | — | ns | **Figure 3.9** |
| SD0_CLK clock high level width | $t_{MMCWH}$ | 18.50 | — | ns | |
| SD0_CLK clock low level width | $t_{MMCWL}$ | 18.50 | — | ns | |
| SD0_CLK clock rise time | $t_{MMCLH}$ | — | 3 | ns | |
| SD0_CLK clock fall time | $t_{MMCHL}$ | — | 3 | ns | |
| SD0_CMD/SDDAT output delay | $t_{MMCODLY}$ | −4.50 | 4.0 | ns | |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | 5.5 | — | ns | |
| SD0_CMD/SDDAT input hold time | $t_{MMCIH}$ | 2.0 | — | ns | |
| SD0_CMD/SDDAT input data width | $t_{MMCIDW}$ | — | — | ns | |

Table 3.23 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| SD0_CLK clock cycle | $t_{MMCPP}$ | 40.00 | — | ns | **Figure 3.9** |
| SD0_CLK clock high level width | $t_{MMCWH}$ | 19.25 | — | ns | |
| SD0_CLK clock low level width | $t_{MMCWL}$ | 19.25 | — | ns | |
| SD0_CLK clock rise time | $t_{MMCLH}$ | — | 2.45 | ns | |
| SD0_CLK clock fall time | $t_{MMCHL}$ | — | 2.45 | ns | |
| SD0_CMD/SDDAT output delay | $t_{MMCODLY}$ | −2.00 | 2.50 | ns | |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | 4.00 | — | ns | |
| SD0_CMD/SDDAT input hold time | $t_{MMCIH}$ | 1.40 | — | ns | |
| SD0_CMD/SDDAT input data width | $t_{MMCIDW}$ | — | — | ns | |

### 3.5.3.2 eMMC host interface timing (HS-SDR)

Table 3.24 eMMC Host Interface Timing (MMC HS-SDR 3.3-V Power Supply)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| SD0_CLK clock cycle | $t_{MMCPP}$ | 30.00 | — | ns | **Figure 3.9** |
| SD0_CLK clock high level width | $t_{MMCWH}$ | 13.50 | — | ns | |
| SD0_CLK clock low level width | $t_{MMCWL}$ | 13.50 | — | ns | |
| SD0_CLK clock rise time | $t_{MMCLH}$ | — | 3 | ns | |
| SD0_CLK clock fall time | $t_{MMCHL}$ | — | 3 | ns | |
| SD0_CMD/SDDAT output delay | $t_{MMCODLY}$ | −4.50 | 4.0 | ns | |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | 5.5 | — | ns | |
| SD0_CMD/SDDAT input hold time | $t_{MMCIH}$ | 2.0 | — | ns | |
| SD0_CMD/SDDAT input data width | $t_{MMCIDW}$ | — | — | ns | |

Table 3.25 eMMC Host Interface Timing (MMC HS-SDR 1.8-V Power Supply)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| SD0_CLK clock cycle | $t_{MMCPP}$ | 20.00 | — | ns | **Figure 3.9** |
| SD0_CLK clock high level width | $t_{MMCWH}$ | 9.25 | — | ns | |
| SD0_CLK clock low level width | $t_{MMCWL}$ | 9.25 | — | ns | |
| SD0_CLK clock rise time | $t_{MMCLH}$ | — | 2.45 | ns | |
| SD0_CLK clock fall time | $t_{MMCHL}$ | — | 2.45 | ns | |
| SD0_CMD/SDDAT output delay | $t_{MMCODLY}$ | −2.00 | 2.50 | ns | |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | 4.00 | — | ns | |
| SD0_CMD/SDDAT input hold time | $t_{MMCIH}$ | 1.40 | — | ns | |
| SD0_CMD/SDDAT input data width | $t_{MMCIDW}$ | — | — | ns | |

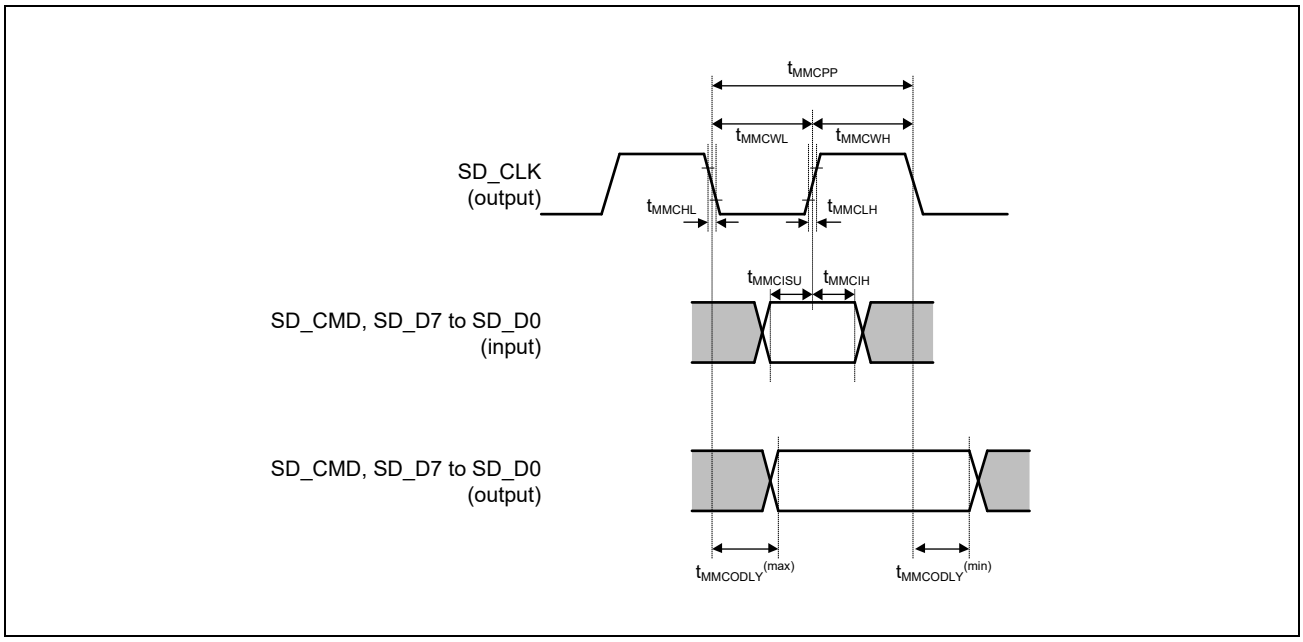



Figure 3.9 eMMC Host Interface Timing (MMC Default/HS-SDR 1.8-V/3.3-V Power Supply)

### 3.5.3.3 eMMC host interface timing (HS200)

Table 3.26 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| SD0_CLK clock cycle | $t_{MMCPP}$ | 7.50 | 15.0 | ns | **Figure 3.10** |
| SD0_CLK clock high level width | $t_{MMCWH}$ | 3.20 | — | ns | |
| SD0_CLK clock low level width | $t_{MMCWL}$ | 3.20 | — | ns | |
| SD0_CLK clock rise time | $t_{MMCLH}$ | — | 1.22 | ns | |
| SD0_CLK clock fall time | $t_{MMCHL}$ | — | 1.22 | ns | |
| SD0_CMD/SDDAT output delay | $t_{MMCODLY}$ | −1.50 | 1.75 | ns | |
| SD0_CMD/SDDAT input set up time | $t_{MMCISU}$ | — | — | ns | |
| SD0_CMD/SDDAT input hold time | $t_{MMCIH}$ | — | — | ns | |
| SD0_CMD/SDDAT input data width | $t_{MMCIDW}$ | 4.31 | — | ns | |

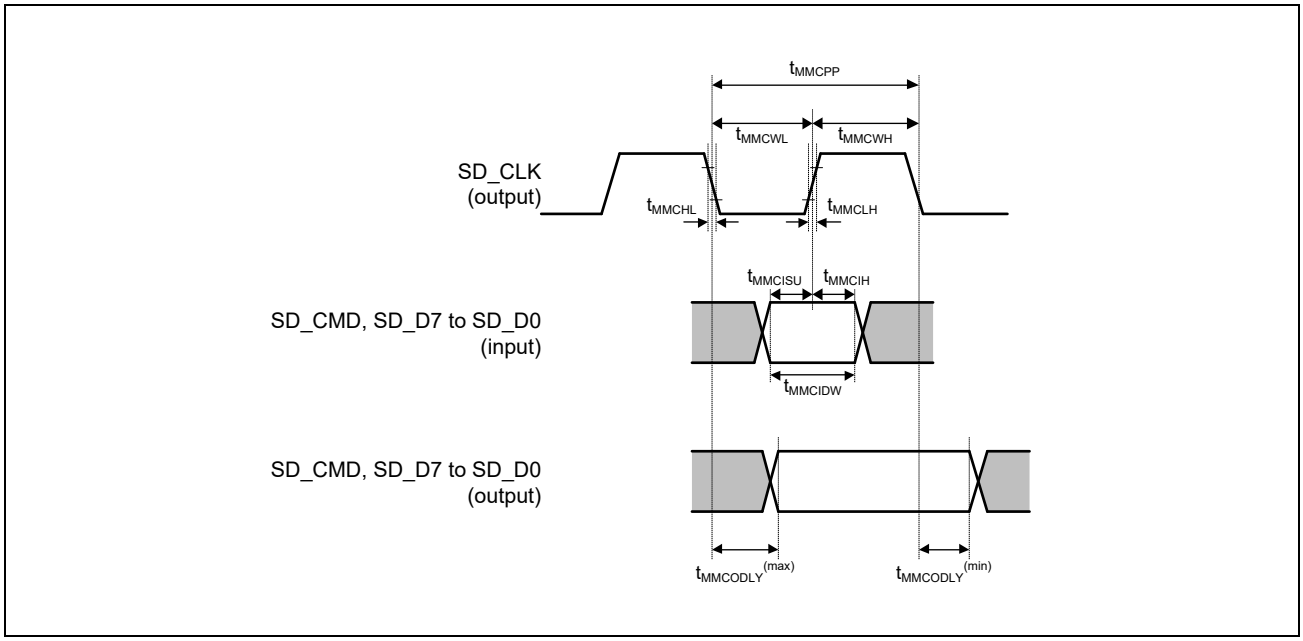



Figure 3.10 eMMC Host Interface (MMC Interface HS200 Mode 1.8-V Power Supply Selection)

## 3.5.4 USB 2.0 Host/Function Module Access Timing

### 3.5.4.1 USB 2.0 Low-Speed Access Timing

Table 3.27 USB Transceiver Timing (Low-Speed)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| Rise time | $t_{LR}$ | 75 | 300 | ns | **Figure 3.11** |
| Fall time | $t_{LF}$ | 75 | 300 | ns | |
| Rise/fall time lag | $t_{LR}/t_{LF}$ | 80 | 125 | % | |

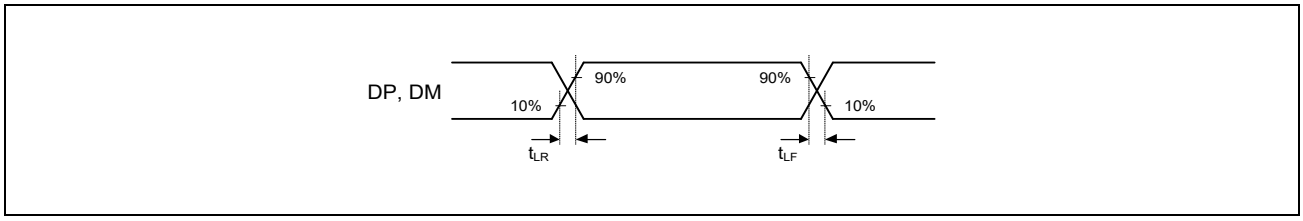



Figure 3.11 USB0_DP, USB1_DP, USB0_DM, and USB1_DM Output Timing (Low-Speed)

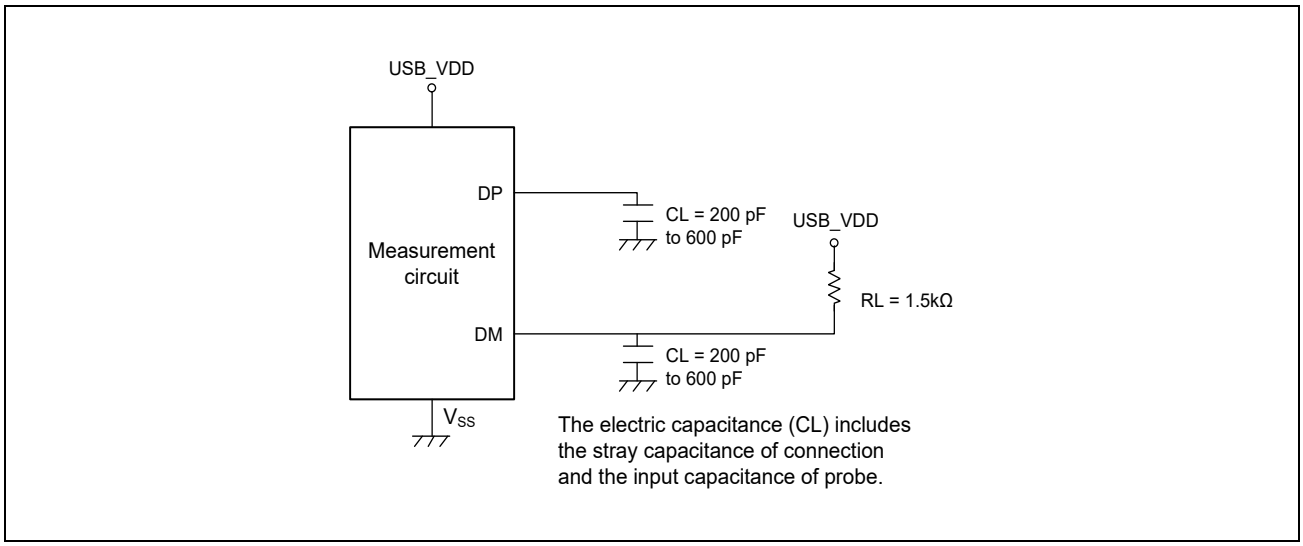



Figure 3.12 Measurement Circuit (Low-Speed)

### 3.5.4.2 USB 2.0Full-Speed Access Timing

Table 3.28 USB Transceiver Timing (Full-Speed)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| Rise time | $t_{FR}$ | 4 | 20 | ns | **Figure 3.13** |
| Fall time | $t_{FF}$ | 4 | 20 | ns | |
| Rise/fall time lag | $t_{FR}/t_{FF}$ | 90 | 111.11 | % | |

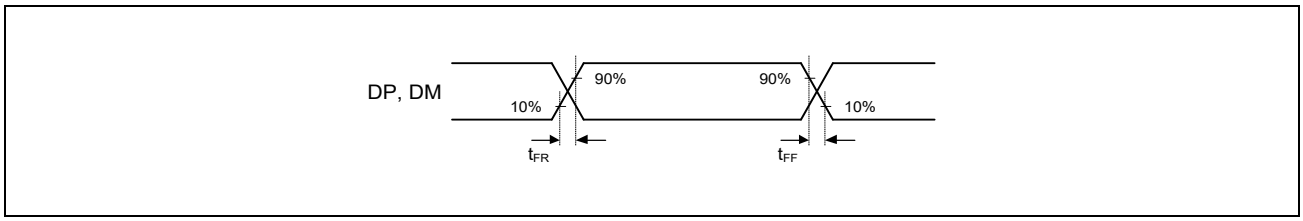



Figure 3.13 USB0_DP, USB1_DP, USB0_DM, and USB1_DM Output Timing (Full-Speed)

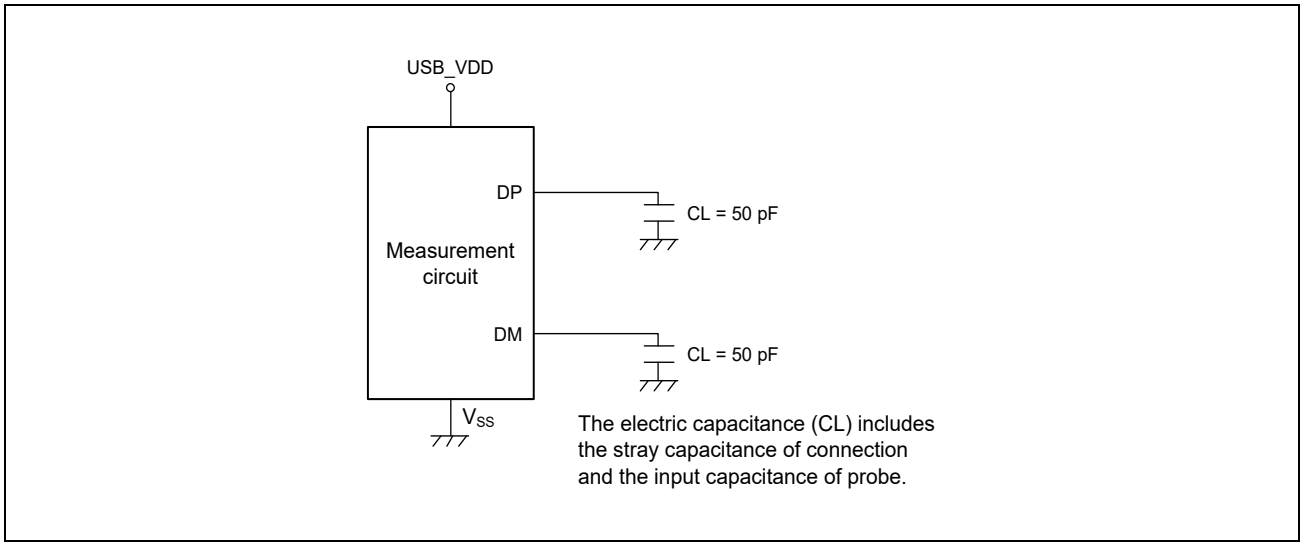



Figure 3.14 Measurement Circuit (Full-Speed)

### 3.5.4.3 USB 2.0 Hi-Speed Access Timing

Table 3.29 USB Transceiver Timing (Hi-Speed)

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| Rise edge rate | $t_{HSR}$ | — | 2133 | V/µs | **Figure 3.15** |
| Fall edge rate | $t_{HSF}$ | — | 2133 | V/µs | |
| Output driver resistance | $Z_{HSDRV}$ | 40.5 | 49.5 | Ω | |

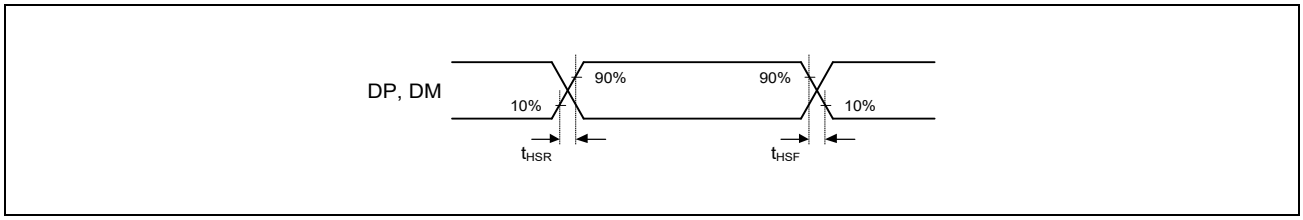



Figure 3.15 USB0_DP, USB1_DP, USB0_DM, and USB1_DM Output Timing (Hi-Speed)

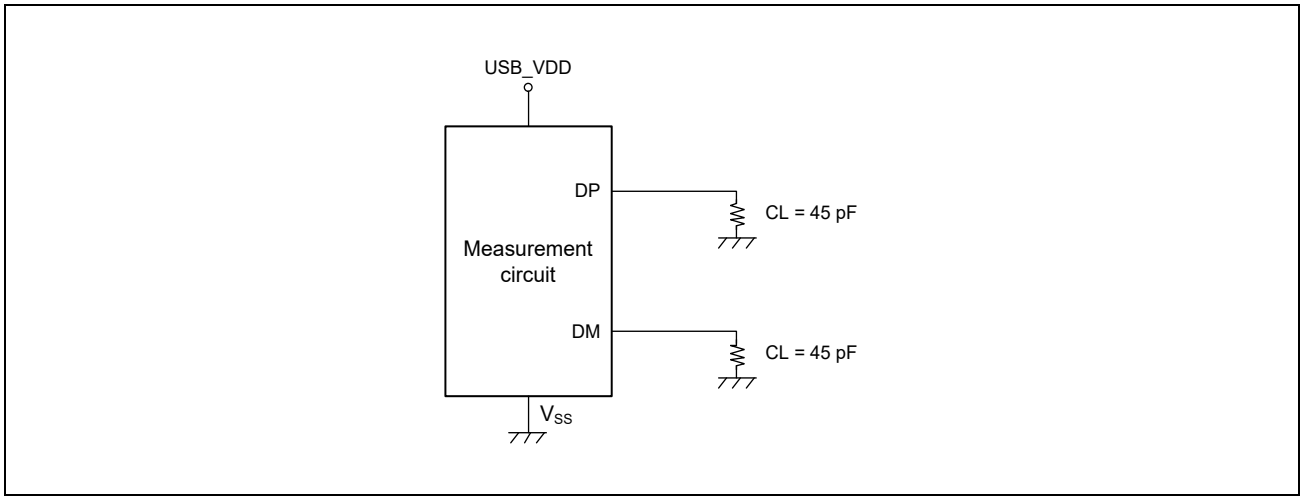
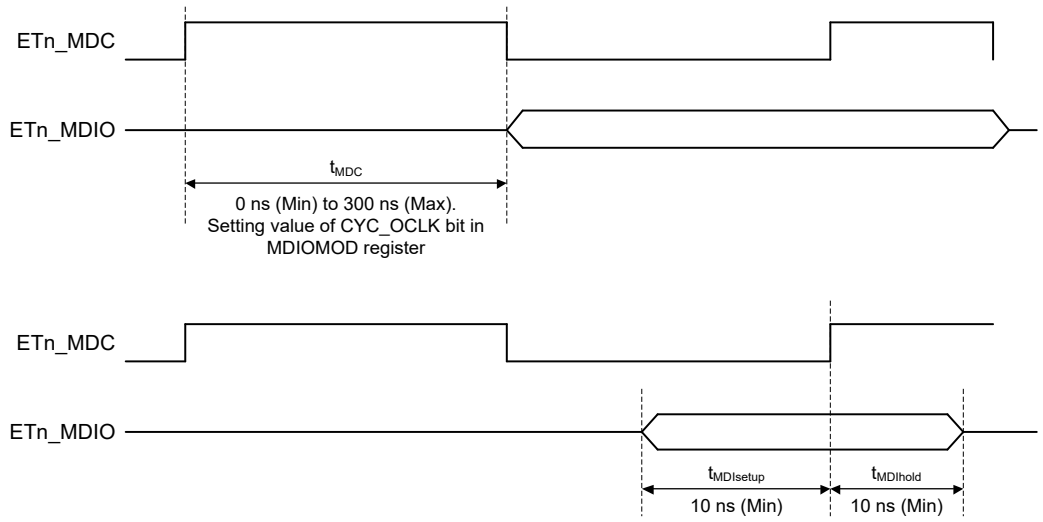



Figure 3.16 Measurement Circuit (Hi-Speed)

### 3.5.5 Ethernet Interface Access Timing

Table 3.30 Ethernet Interface Access Timing

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| MDC half cycle | $t_{MDC}$ | 0 | 300 | ns | **Figure 3.17** |
| MDI setup time | $t_{MDIsetup}$ | 10 | — | ns | |
| MDI hold time | $t_{MDIhold}$ | 10 | — | ns | |




**Note:** (n = 0, 1)

Figure 3.17 Management Interface

### 3.5.5.1 Ethernet-IF (Ether MII)

Table 3.31 Ethernet-IF Access Timing (Ether MII)

| Item | | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|---|
| Ether MII | ETH_GTXTXC_TXC period | $t_{Tcyc}$ | 40 | — | ns | **Figure 3.18** |
| | ETH_TXCTL output delay | $t_{TENd}$ | 0 | 25 | ns | |
| | ETH_TXD3-0 output delay | $t_{MTDd}$ | 0 | 25 | ns | |
| | ETH_RXC period | $t_{Rcyc}$ | 40 | — | ns | |
| | ETH_RXDV setup time | $t_{RDVs}$ | 10 | — | ns | |
| | ETH_RXDV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ETH_RXD3-0 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ETH_RXD3-0 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ETH_RXER setup time | $t_{RERs}$ | 10 | — | ns | |
| | ETH_RXER hold time | $t_{RERh}$ | 10 | — | ns | |

**Note:** I/O driving ability: 8 mA
CL = 8 pF

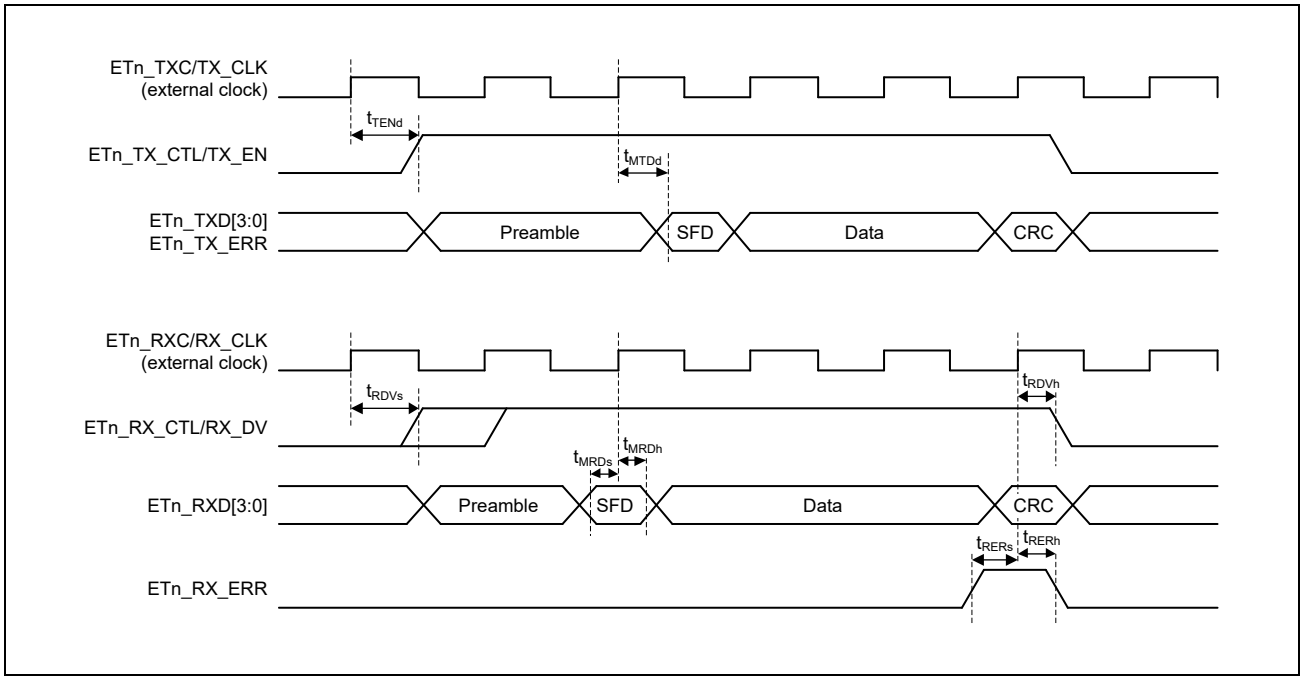



Figure 3.18 MII Transmission Timing

Validated with IEEE802.3 regulation.

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns.

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns.

### 3.5.5.2 Ethernet-IF (Ether RGMII)

Table 3.32 Ethernet-IF Access Timing (Ether RGMII)

| Item | | Symbol | Min. | Typ. | Max. | Unit | capaci-tance | Remarks | Figures |
|---|---|---|---|---|---|---|---|---|---|
| Ether RGMII | Data to clock output skew @ transmitter | $T_{skewT}$ | −500 | 0 | 500 | ps | 8 pF | Tx RGMII | **Figure 3.19** |
| | Data to clock input skew @ receiver | $T_{skewR}$ | 1 | 1.8 | 2.6 | ns | 8 pF | | |
| | Data to clock output setup @ transmitter integrated delay | $T_{setupT}$ | 1.2 | 2.0 | — | ns | 8 pF | Rx RGMII-ID | **Figure 3.20** |
| | Clock to data output hold @ transmitter integrated delay | $T_{holdT}$ | 1.2 | 2.0 | — | ns | 8 pF | | |
| | Data to clock input setup setup @ receiver integrated delay | $T_{setupR}$ | 1.0 | 2.0 | — | ns | 8 pF | Rx RGMII-ID | **Figure 3.20** |
| | Data to clock input setup hold @ receiver integrated delay | $T_{holdR}$ | 1.0 | 2.0 | — | ns | 8 pF | | |
| | Clock cycle duration*1 | $T_{cyc}$ | 7.2 | 8 | 8.8 | ns | 8 pF | — | — |
| | Duty cycle for gigabit | Duty_G | 45 | 50 | 55 | % | 8 pF | | |
| | Duty cycle for 10/100T | Duty_T | 40 | 50 | 60 | % | 8 pF | | |
| | Rise/fall time (20-80%) | $T_r/T_f$ | — | — | 0.75 | ns | 8 pF | | |

Note 1. For 10 Mbps and 100 Mbps, $T_{cyc}$ will scale to 400ns ±40ns and 40ns ±4ns respectively.

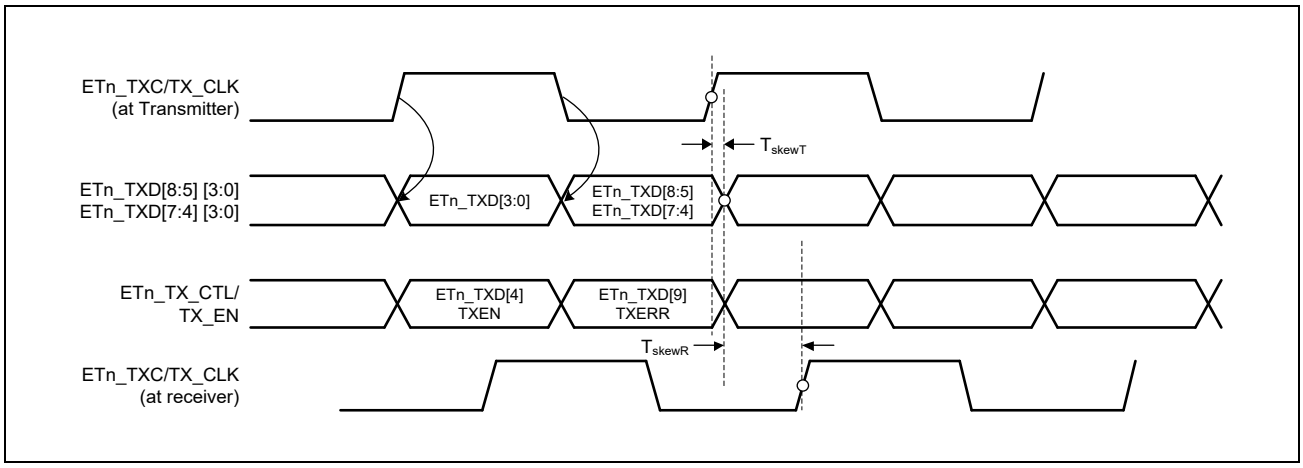



Figure 3.19 Multiplexing & Timing Diagram — RGMII (Transmitter)

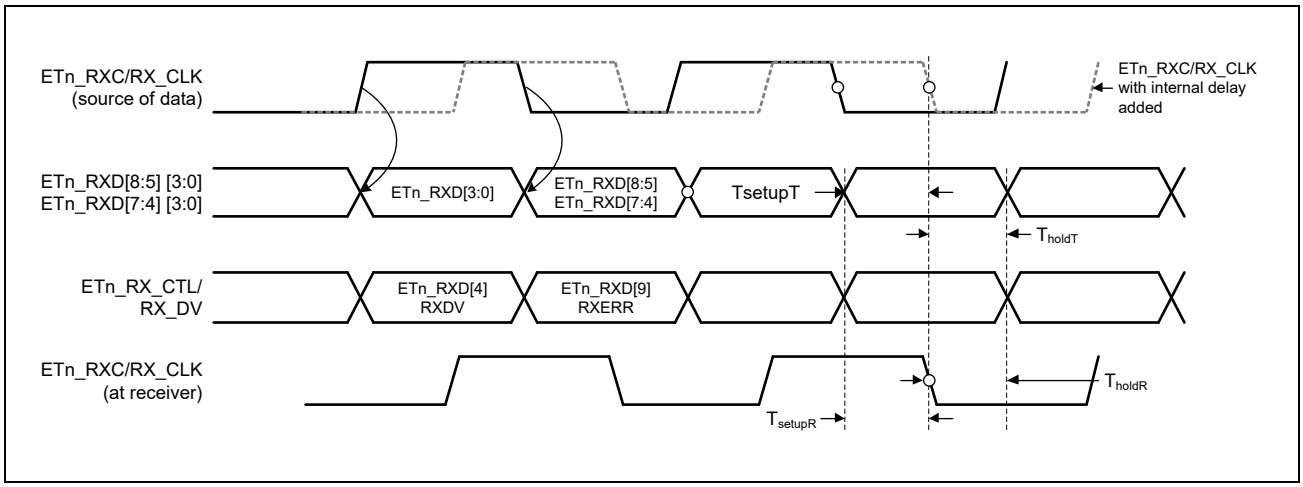



Figure 3.20 Multiplexing & Timing Diagram — RGMII-ID (Receiver)

### 3.5.6 JTAG Debugger Interface Access Timing

Table 3.33 Debugger IF Timing

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| TCK_SWCLK cycle time | $t_{TCKcyc}$ | 50 | — | ns | **Figure 3.21** |
| TCK_SWCLK high pulse width | $t_{TCKH}$ | 20 | — | ns | **Figure 3.22** |
| TCK_SWCLK low pulse width | $t_{TCKL}$ | 20 | — | ns | |
| TDI setup time | $t_{TDIS}$ | 15 | — | ns | |
| TDI hold time | $t_{TDIH}$ | 15 | — | ns | |
| TMS_SWDIO setup time | $t_{TMSS}$ | 15 | — | ns | |
| TMS_SWDIO hold time | $t_{TMSH}$ | 15 | — | ns | |
| SWDIO delay time | $t_{SWDO}$ | — | 14 | ns | |
| TDO delay time | $t_{TDOD}$ | — | 14 | ns | |
| Capture register setup time | $t_{CAPTS}$ | 10 | — | ns | **Figure 3.23** |
| Capture register hold time | $t_{CAPTH}$ | 10 | — | ns | |
| Update register delay time | $t_{UPDATED}$ | — | 20 | ns | |

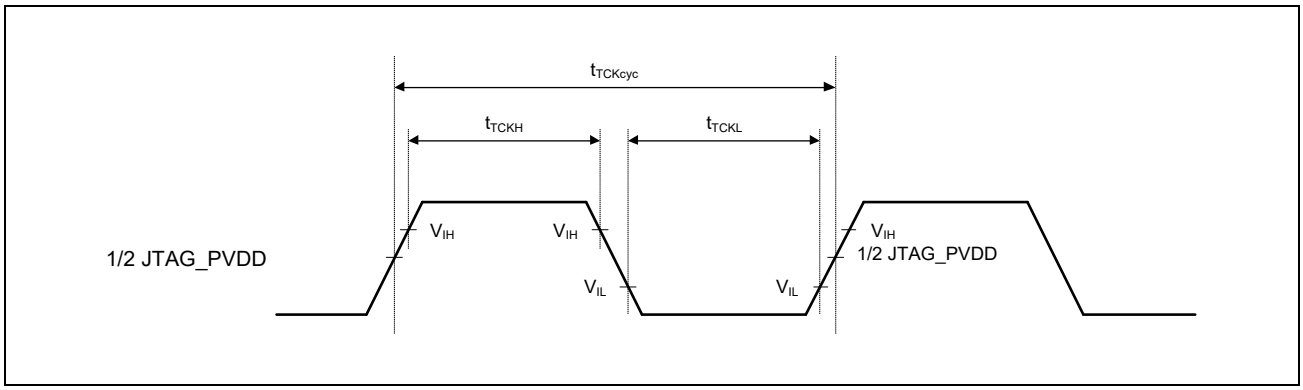



Figure 3.21 TCK_SWDCLK Input Timing

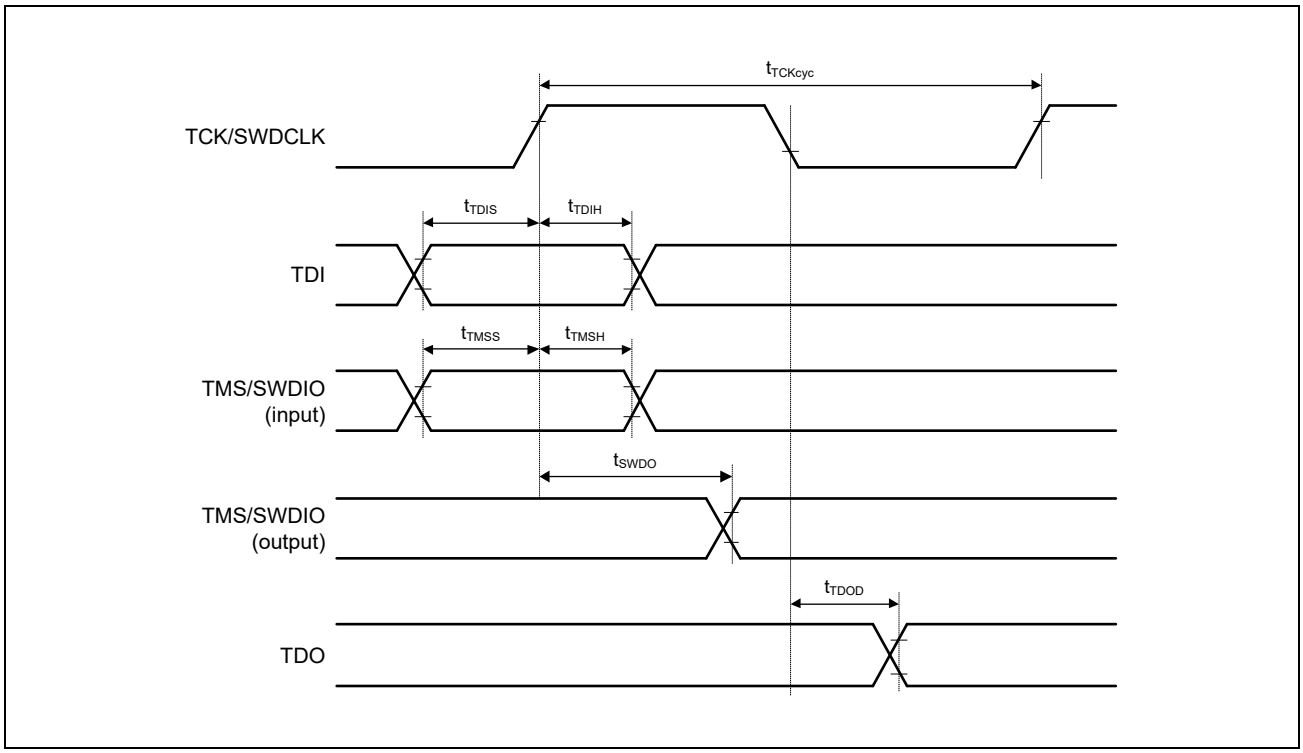



Figure 3.22 Data Transfer Timing

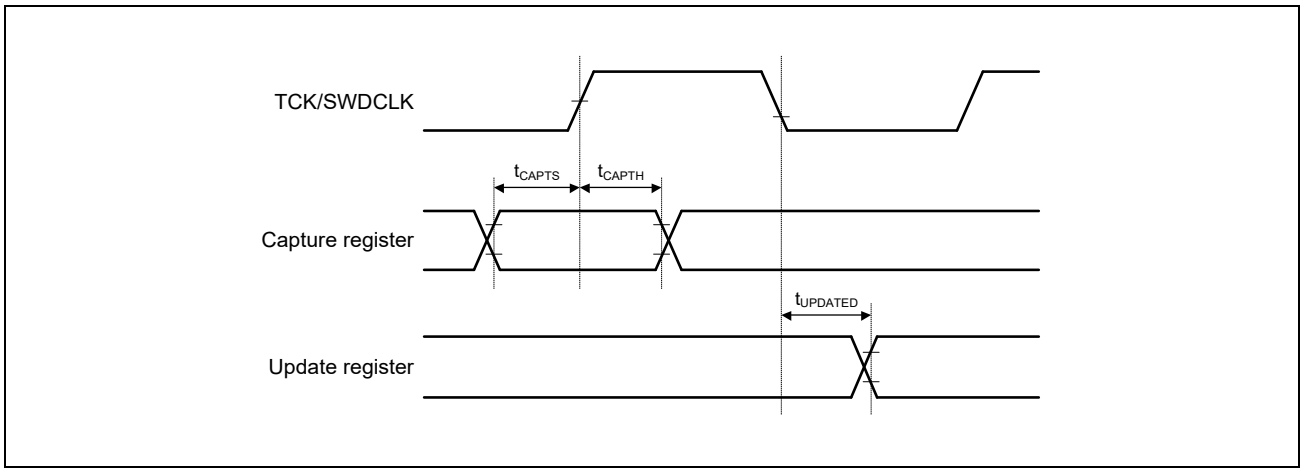



Figure 3.23 Boundary Scan Input/Output I/O Timing

### 3.5.7 SPI Multi I/O Bus Controller Access Timing

Table 3.34 SPI Multi I/O Bus Contoller Access Timing

| Item | | Symbol | 1.8 V (Serial flash connected) Min. | 1.8 V (Serial flash connected) Max. | 3.3 V (Serial flash connected) Min. | 3.3 V (Serial flash connected) Max. | Unit | Figures |
|---|---|---|---|---|---|---|---|---|
| Clock cycle | | $t_{SPBcyc}$ | 15.0 | — | 15.0 | — | ns | **Figure 3.24** |
| CLK high pulse width | | $t_{SPBWH}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{SPBcyc}$ | **Figure 3.24** |
| CLK low pulse width | | $t_{SPBWL}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{SPBcyc}$ | **Figure 3.24** |
| CLK rise time | | $t_{SPBR}$ | — | 1.0 | — | 3.2 | ns | **Figure 3.24** |
| CLK fall time | | $t_{SPBF}$ | — | 1.0 | — | 3.2 | ns | **Figure 3.24** |
| Data input setup time | QSPI0_SPCLK base point (SDR mode timing adjusted) | $t_{SU}$ | 6.7 | — | 7.5 | — | ns | **Figure 3.25** |
| | QSPI0_SPCLK base point (DDR mode timing adjusted) | | 4.5 | — | 4.5 | — | ns | **Figure 3.26** |
| Data input hold time | QSPI0_SPCLK base point (SDR mode timing adjusted) | $t_{H}$ | 0.5 | — | 0.5 | — | ns | **Figure 3.25** |
| | QSPI0_SPCLK base point (DDR mode timing adjusted) | | 1.0 | — | 1.0 | — | ns | **Figure 3.26** |
| SSL setup time | | $t_{LEAD}$ | 1.5 × $t_{SPBcyc}$ − 3 | 8.5 × $t_{SPBcyc}$ + 3 | 1.5 × $t_{SPBcyc}$ − 3 | 8.5 × $t_{SPBcyc}$ + 3 | ns | **Figure 3.25**, **Figure 3.26** |
| SSL hold time | | $t_{LAG}$ | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | ns | **Figure 3.25**, **Figure 3.26** |
| Continuous transfer delay time | | $t_{TD}$ | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | 1 × $t_{SPBcyc}$ − 3 | 8 × $t_{SPBcyc}$ + 3 | ns | **Figure 3.25**, **Figure 3.26** |
| Data output delay time | SDR | $t_{OD}$ | — | 2.0 | — | 5.0 | ns | **Figure 3.25** |
| | DDR | | — | 6.5*2 | — | 7.5*3 | ns | **Figure 3.26** |
| Data output hold time | SDR | $t_{OH}$ | −2.0 | — | -5.0 | — | ns | **Figure 3.25** |
| | DDR | | 1.0*2 | — | 2.1*3 | — | ns | **Figure 3.26** |
| Data output buffer off time | SDR | $t_{BOFF}$ | — | 2.0 | — | 3.0 | ns | **Figure 3.27** |
| | DDR | | — | 2.0 | — | 3.0 | ns | **Figure 3.27** |

Note 1. Output load: 15 pF/driving ability: 12 mA

Note 2. QSPI0_SPCLK frequency: 100 MHz.

Note 3. QSPI0_SPCLK frequency: 66 MHz

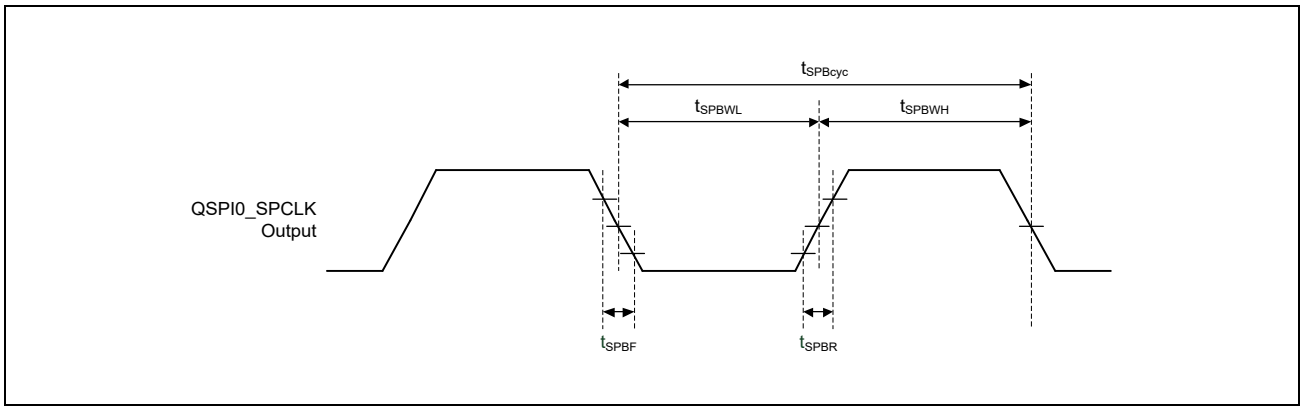



Figure 3.24 Clock Timing

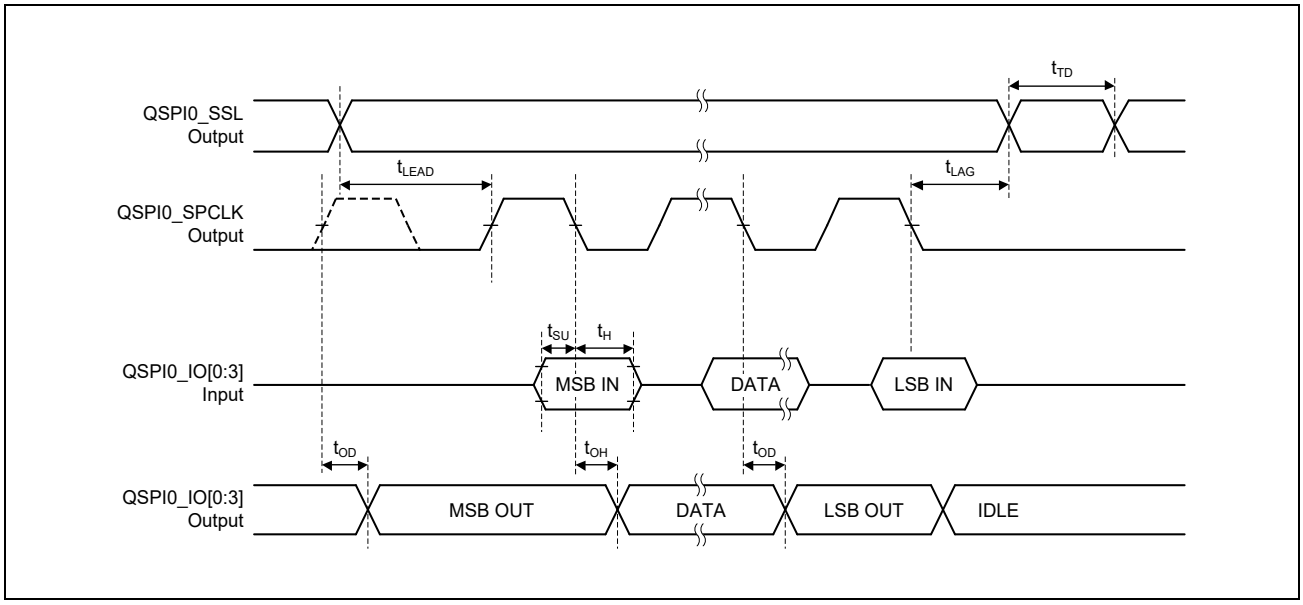



Figure 3.25 SDR Transfer Format Transmission and Reception Timing

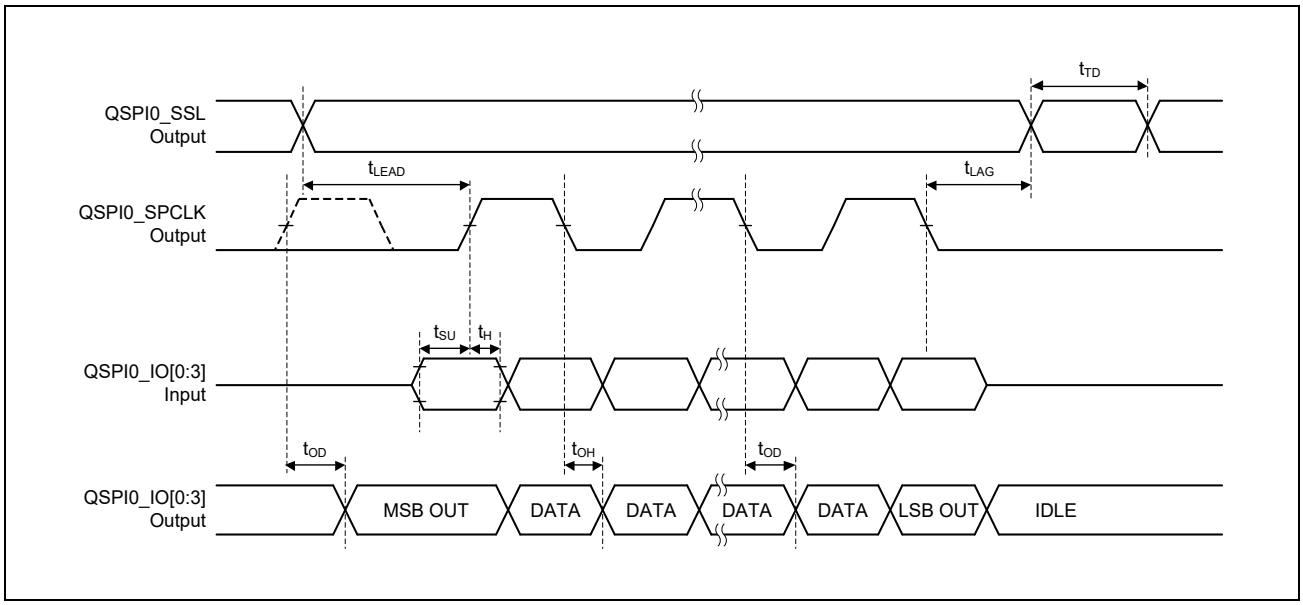



Figure 3.26 DDR Transfer Format Transmission and Reception Timing

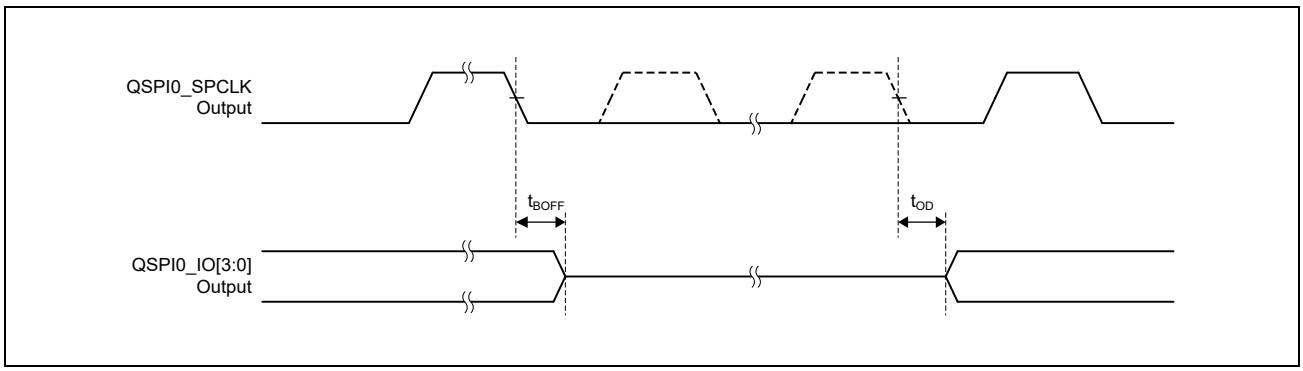



Figure 3.27 Timing for Switching the Buffers On and Off

### 3.5.8 Control Signal Access Timing

Table 3.35 Control Signal Timing

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| PRST# pulse width | $t_{RESW}$ | 20 | — | $t_{cyc}$*1 | **Figure 3.28** |
| TRST# pulse width | $t_{TRSW}$ | 20 | — | $t_{cyc}$*1 | |
| NMI pulse width | $t_{NMIW}$ | 20 | — | $t_{cyc}$*1 | **Figure 3.30** |
| IRQ pulse width | $t_{IRQW}$ | 20 | — | $t_{cyc}$*1 | |
| TINT pulse width | $t_{TINTW}$ | 20 | — | $t_{cyc}$*1 | |
| PRST# input rise time | $t_{RSr}$ | — | 500 | µs | **Figure 3.29** |

Note 1. $t_{cyc}$ = 41.666 ns (24 MHz)

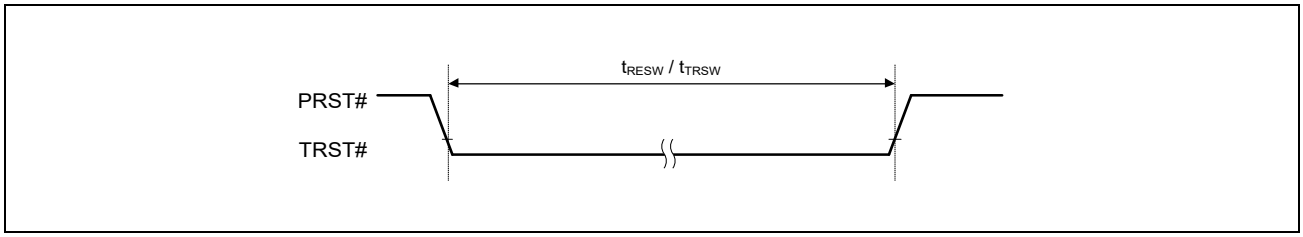



Figure 3.28 Reset Input Timing 1

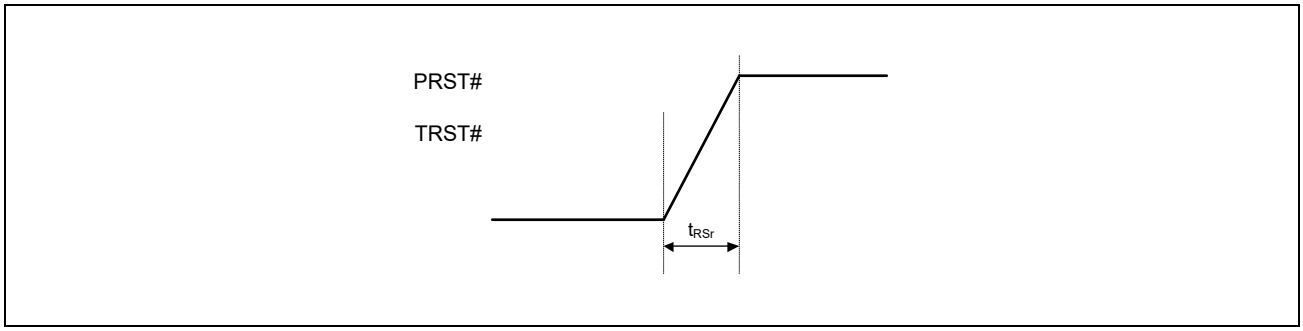
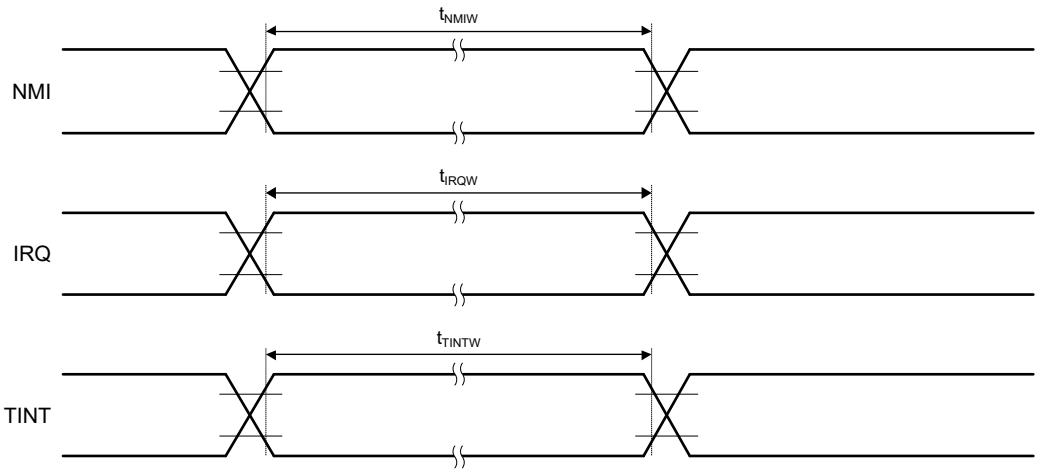



Figure 3.29 Reset Input Timing 2




**Note:** This specification “(Min. 20 $t_{cycle}$)” is the min. pulse width the case that the digital noise filter is off. For details on digital noise filter settings, refer to *Section 41, General Purpose Input Output Port (GPIO)*, in the *User's Manual: Hardware*.

Figure 3.30 Interrupt Signal Input Timing

### 3.5.9 Serial Sound Interface (SSIF-2) Access Timing

Table 3.36 SSIF-2 Timing

| Item | I/O | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|---|
| Output clock cycle | Output | $t_O$ | 80 | 64000 | ns | **Figure 3.31** |
| Input clock cycle | Input | $t_I$ | 80 | — | ns | |
| Clock high | Bidirectional | $t_{HC}$ | 32 | — | ns | |
| Clock low | | $t_{LC}$ | 32 | — | ns | |
| Clock rise time/clock fall time | Output | $t_{RC}/t_{FC}$ | — | 25 | ns | |
| Setup time | Input | $t_{SR}$ | 25 | — | ns | **Figure 3.32**, **Figure 3.33**, **Figure 3.34** |
| Hold time | | $t_{HR}$ | 5 | — | ns | |
| SILRCK output delay time | Output | $t_{DTR}$ | −5 | 25 | ns | |
| Data output delay time (Noise canceler not in use) | | $t_{DTR}$ | −5 | 25 | ns | |
| Data output delay time (Noise canceler in use) | | $t_{DTR}$ | 10 | 50 | ns | |

**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

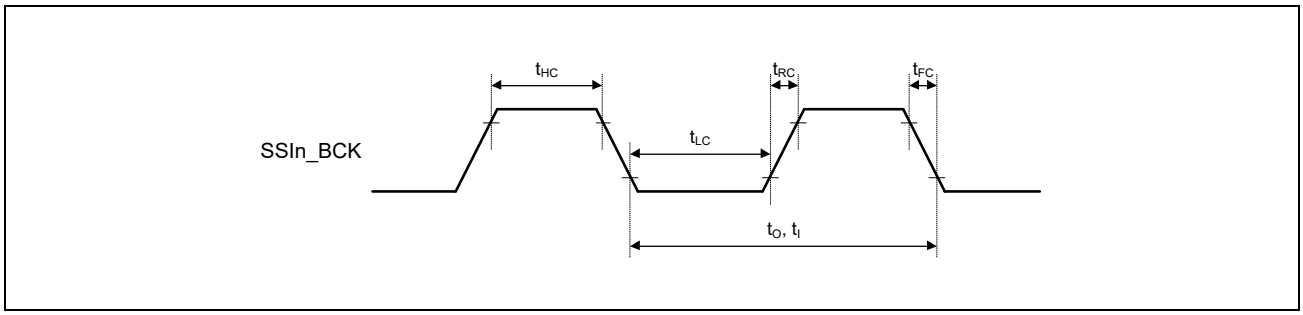



Figure 3.31 Bit Clock Input/Output Timing

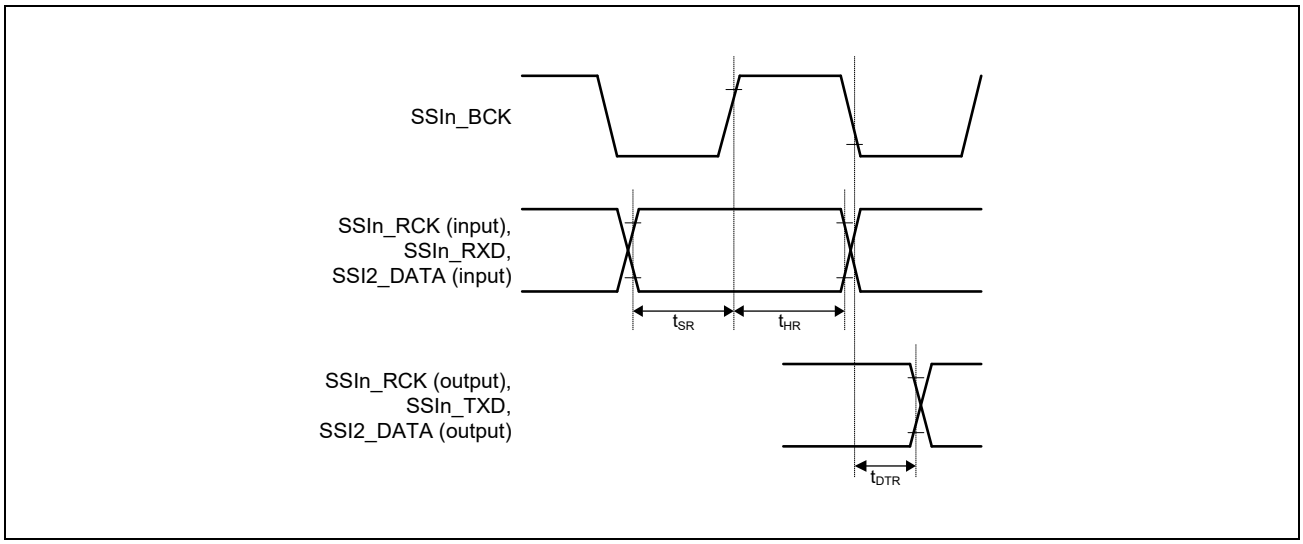



Figure 3.32 Transmission and Reception Timing (SSIBCK Falling Output)

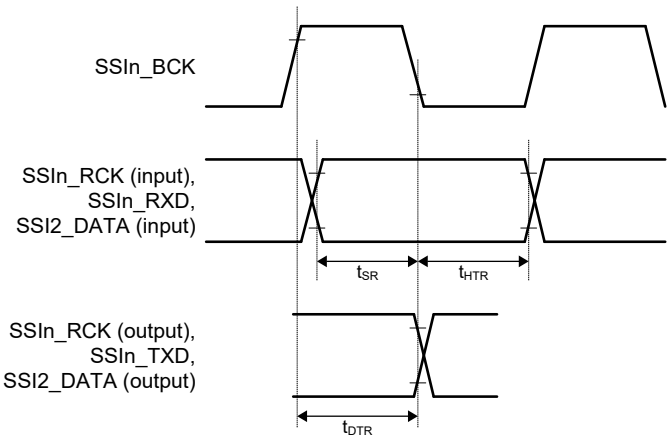
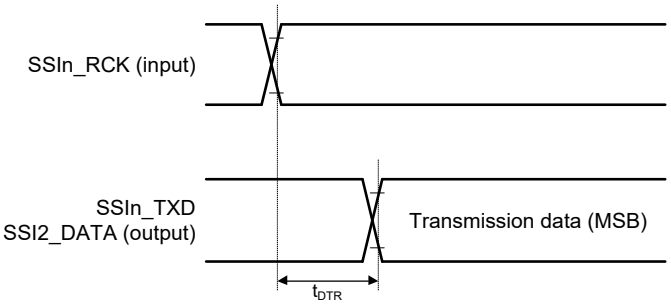



Figure 3.33 Transmission and Reception Timing (SSIBCK Rising Output)




**Note:** Output timing of the MSB when slave transmission satisfies the following condition a) or b)
a) SSICR.DEL = 1, SSICR.SDTA = 0
b) SSICR.DEL = 1, SSICR.SDTA = 1, without padding

Figure 3.34 Transmission Timing (Slave, in Synchronization with SSILRCK)

### 3.5.10 CAN-FD Interface Access Timing

Table 3.37 CAN-FD Interface Timing

| Item | Symbol | CAN | | CAN-FD | | Unit | Figures |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Internal delay time | $t_{node}$*1 | — | 100 | — | 75 | ns | **Figure 3.35** |
| Transmission rate | — | — | 1 | — | 4 | Mbps | |

**Note:** AC access timing condition: drive ability 12mA, output load 15pF, slew rate = fast

Note 1. Internal delay time ($t_{node}$) = Internal transfer delay time ($t_{output}$) + Internal receive delay time ($t_{input}$)

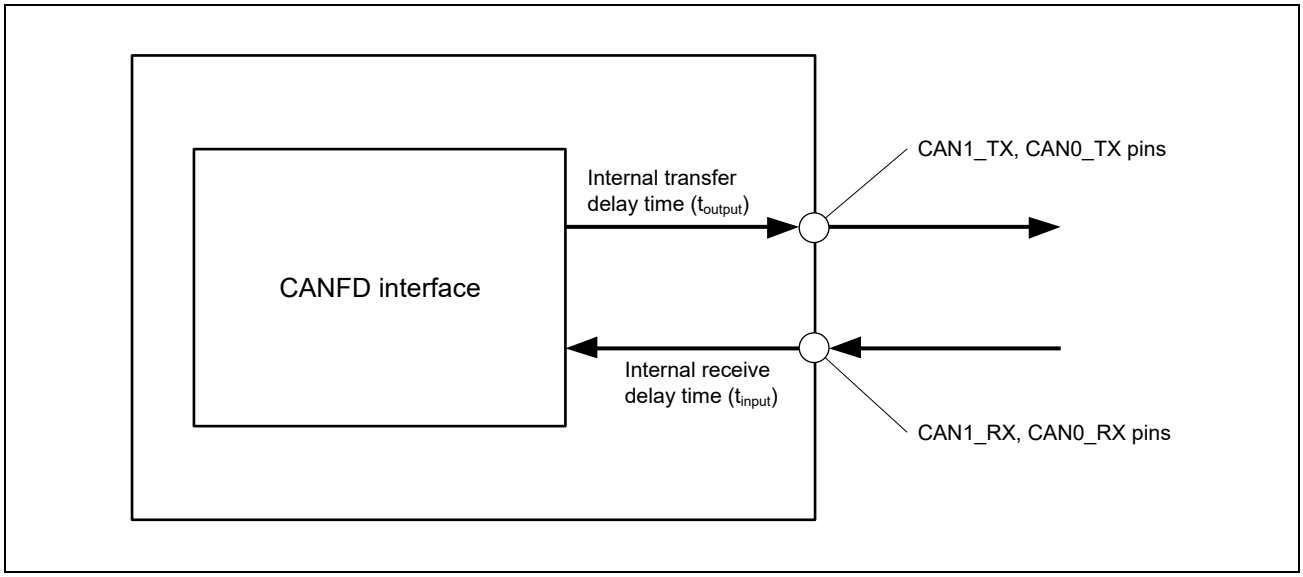



Figure 3.35 CAN-FD Interface Condition

### 3.5.11 Multi-Function Timer Pulse Unit 3 (MTU3a) Access Timing

Table 3.38 MTU3a Timing

| Item | | | Symbol | Min. | Max. | Unit*1 | Figures |
|---|---|---|---|---|---|---|---|
| MTU3a | Input capture input pulse width | Single-edge setting | $t_{MTICW}$ | 1.5 | — | $t_{p1cyc}$*1 | **Figure 3.36** |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{MTCKWH}$, $t_{MTCKWL}$ | 1.5 | — | $t_{p1cyc}$*1 | **Figure 3.37** |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

**Note:** AC access timing condition: drive ability 4mA, output load 30pF, slew rate = fast

Note 1. $t_{p1cyc}$ indicates peripheral clock means MTU_X_MCLK_MTU3 (P0ϕ).

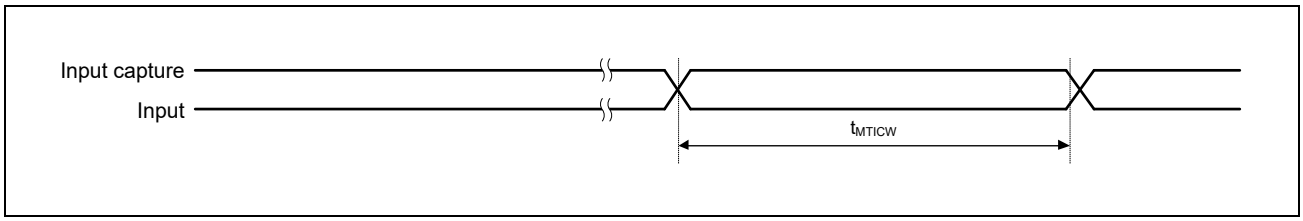



Figure 3.36 MTU3a Input Capture Input Timing

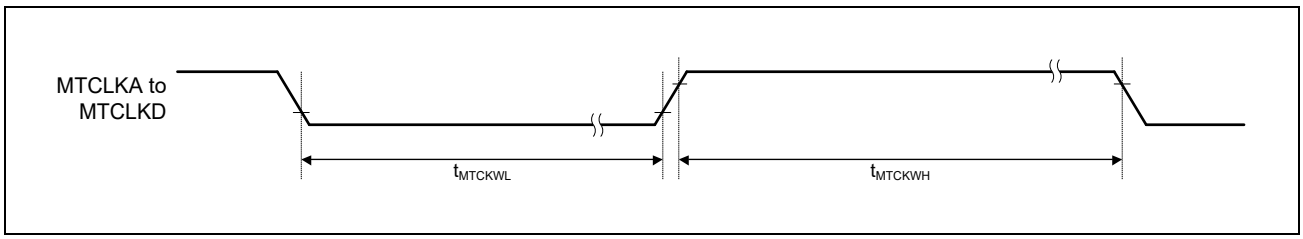



Figure 3.37 MTU3a Clock Input Timing

### 3.5.12 Port Output Enable 3 (POE3) Access Timing

Table 3.39 POE3 Timing

| Item | | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|---|
| POE3 | POEn# input pulse width | $t_{POE3W}$ | 1.5 | — | $t_{p1cy}$*1 | **Figure 3.38** |

Note 1. $t_{p1cyc}$ indicates peripheral clock means POE3_CLKM_POE (P0ϕ).

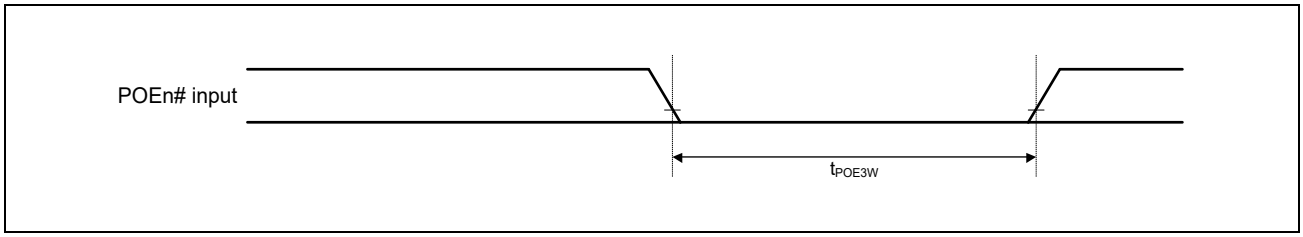



Figure 3.38 POEn# Input Pulse Timing

### 3.5.13 I²C Bus Interface Access Timing

Table 3.40 I²C Bus Interface Timing

| Item | Symbol | I/O | Standard Mode (Sm) | | Fast Mode (Fm) | | Fast Mode Plus (Fm+) | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| SCL clock frequency | $f_{CLK}$ | I/O | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| Bus free time (between stop and start condition) | $t_{BUF}$ | I/O | 4.7 | — | 1.3 | — | 0.5 | — | µs |
| Hold time*1 | $t_{HD:STA}$ | I/O | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| Low period of SCL clock | $t_{LOW}$ | I/O | 4.7 | — | 1.3 | — | 0.5 | — | µs |
| High period of SCL clock | $t_{HIGH}$ | I/O | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| Setup time for start / restart condition | $t_{SU:STA}$ | I/O | 4.7 | — | 0.6 | — | 0.26 | — | µs |
| Data hold time (I²C bus device) | $t_{HD:DAT}$ | I/O | 0*2 | — | 0*2 | — | 0 | — | µs |
| Data setup time | $t_{SU:DAT}$ | I/O | 250 | — | 100*3 | — | 50 | — | ns |
| SDA and SCL signal rise time | $t_R$ | Input | — | 1000 | 20 | 300 | — | 120 | ns |
| SDA and SCL signal fall time*3 | $t_F$ | Input | — | 300 | 20 × ($PV_{DD}$/ 5.5 V) | 300 | 20 × ($PV_{DD}$/ 5.5 V) | 120 | ns |
| | | Output | — | 300 | 20 × ($PV_{DD}$/ 5.5 V)*6 | 300*6 | 20 × ($PV_{DD}$/ 5.5 V)*7 | 120*7 | ns |
| Setup time for STOP condition | $t_{SU:STO}$ | I/O | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| Capacitive load for each bus line | $C_b$ | — | — | 400*4 | — | 400*4 | — | 550*4 | pF |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | Input | — | — | 0 | 50*5 | 0 | 50*5 | ns |

**Note:** In the above table and subsequently, SCL and SDA refer to the RIICnSCL and RIICnSDA signals, respectively.

**Note:** AC access timing condition: drive ability 4mA, output load 400pF, slew rate = slow

Note 1. The first clock pulse is generated on the SCL line after the start condition has been issued and the hold time has elapsed.

Note 2. This module requires a minimum of 300 ns hold time internally for the SDA signal to handle the period over which the falling edge of SCL has not reached a defined level (time until the CnSCL signal reaches $V_{IL}$ (max.) from $V_{IH}$ (min.)).

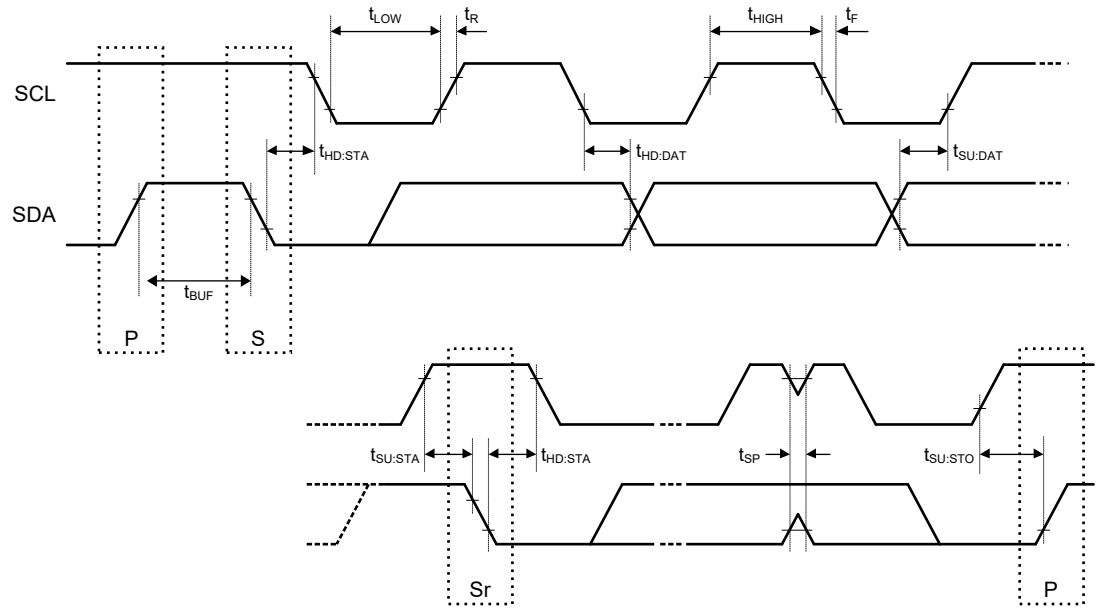
Note 3. The fast-mode I²C bus device can be used in the standard mode I²C bus system. In this case, the minimum value of the data setup time ($t_{SU:DAT}$ (min.) 250 [ns]) must be satisfied.
If the system does not extend the low period of SCL clock ($t_{LOW}$), this condition is automatically satisfied. If the system extends the low period of SCL clock ($t_{LOW}$), transmit the subsequent data bit to the SDA line before the SCL line is released ($t_R$ (max.) + $t_{SU:DAT}$ (min.) = 1000 + 250 = 1250 [ns]: (standard mode I²C bus specification)).

Note 4. Total capacitance of one bus line. The allowable maximum bus capacitance may differ from this specification, depending on the actual operating voltage and frequency of an application. For techniques to cope with a large bus capacitance, see the I²C bus specification provided by NXP Semiconductors.

Note 5. Noise is removed by the analog and digital input filters. The level of noise reduction of the digital input filter is determined by the period of internal reference clock (IICϕ) and the NF[1:0] bits in RIICnMR3. For details, refer to *Section 26, I²C Bus Interface*, in the *User's Manual: Hardware*.

Note 6. External pull-up resistor is required 1077Ω to 1770Ω when using RIIC ch2 or RIIC ch3.

Note 7. External pull-up resistor is required 240Ω to 257Ω when using RIIC ch2 or RIIC ch3.




**Note:** P: Stop condition
S: Start condition
Sr: Start condition for retransmission

Figure 3.39 Input/Output Timing

### 3.5.14 Serial Communications Interface with FIFO (SCIFA) Access Timing

Table 3.41 SCIFA Timing

| Item | | | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|---|---|
| SCIFA | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{p1cyc}$*1 | **Figure 3.40** |
| | | Clocked synchronous | | 12 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{p1cyc}$*1 | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous*2 | $t_{Scyc}$ | 8 | — | $t_{p1cyc}$*1 | |
| | | Clocked synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{p1cyc}$*1 | |
| | Output clock rise time | | $t_{SCKr}$ | — | 9 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 9 | ns | |
| | Transmit data delay time | Internal clock | $t_{TXD}$ | −10 | 10 | ns | **Figure 3.41** |
| | | External clock | | 3 × $t_{p1cyc}$*1 | 4 × $t_{p1cyc}$*1 + 20 | | |
| | Receive data setup time | Internal clock | $t_{RXS}$ | 3 × $t_{p1cyc}$*1 + 20 | — | ns | |
| | | External clock | | $t_{p1cyc}$*1 + 10 | — | | |
| | Receive data hold time | Internal clock | $t_{RXH}$ | −3 × $t_{p1cyc}$*1 | — | ns | |
| | | External clock | | 2 × $t_{p1cyc}$*1 + 10 | — | | |

**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

Note 1. $t_{p1cyc}$ indicates peripheral clock means SCIFn_CLK_PCK (P0ϕ) (n = 0 to 4).

Note 2. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1.

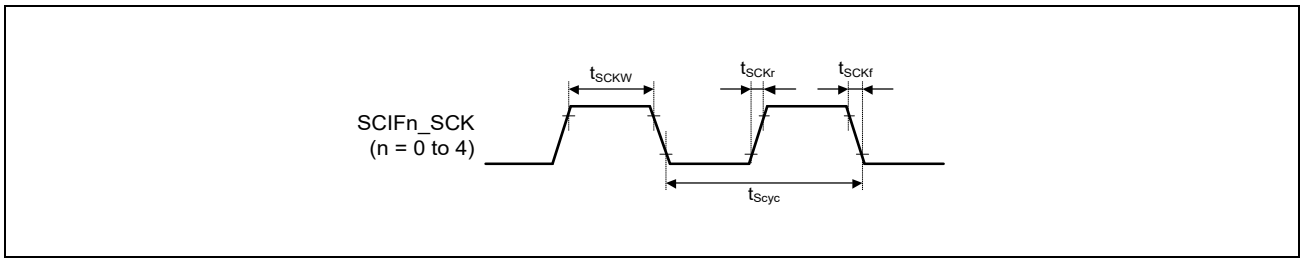
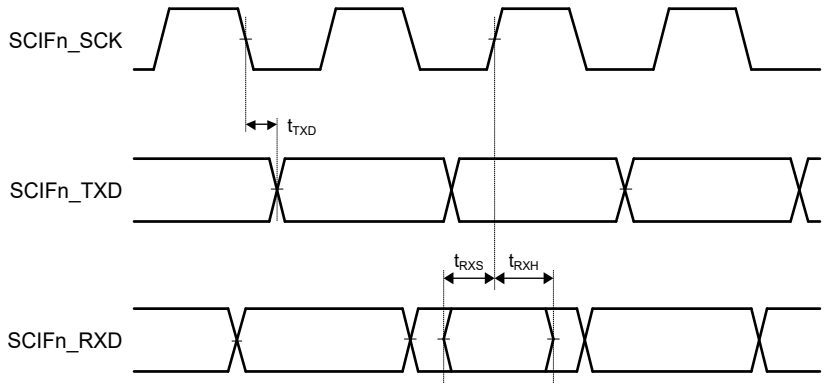



Figure 3.40 SCK Input Clock Timing




**Note:** n = 0 to 4

Figure 3.41 SCIFA Input/Output Timing in Clocked Synchronous Mode

### 3.5.15 Serial Communications Interface (SCIg) Access Timing

Table 3.42 SCIg Timing

| Item | | | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|---|---|
| SCIg | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{p1cyc}$*1 | **Figure 3.42** |
| | | Clocked synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{p1cyc}$*1 | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous*2 | $t_{Scyc}$ | 8 | — | $t_{p1cyc}$*1 | |
| | | Clocked synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{p1cyc}$*1 | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | Clocked synchronous | $t_{TXD}$ | — | 28 | ns | **Figure 3.43** |
| | Receive data setup time | Clocked synchronous | $t_{RXS}$ | 15 | — | ns | |
| | Receive data hold time | Clocked synchronous | $t_{RXH}$ | 5 | — | ns | |

**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

Note 1. $t_{p1cyc}$ indicates peripheral clock means SCIn_CLKP (P0ϕ) (n = 0 to 1).

Note 2. When the SEMR.ABCS0 and SEMR.BGDM bits are set to 1.

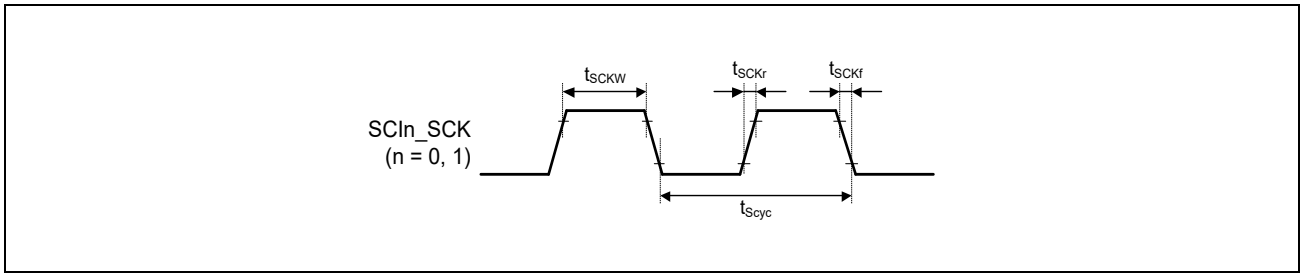
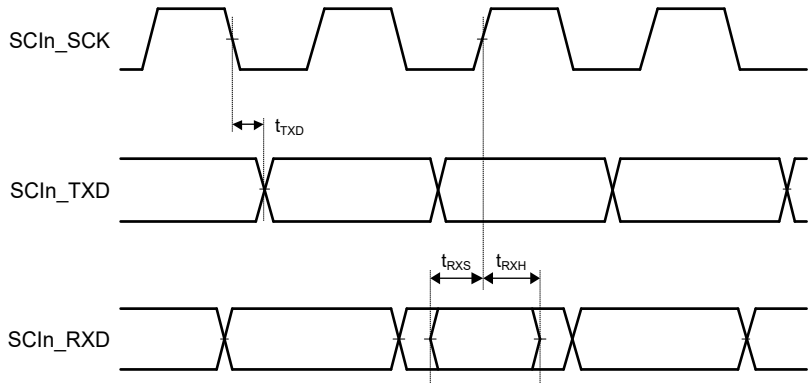



Figure 3.42 SCK Input Clock Timing




**Note:** n = 0, 1

Figure 3.43 SCIFA Input/Output Timing in Clocked Synchronous Mode

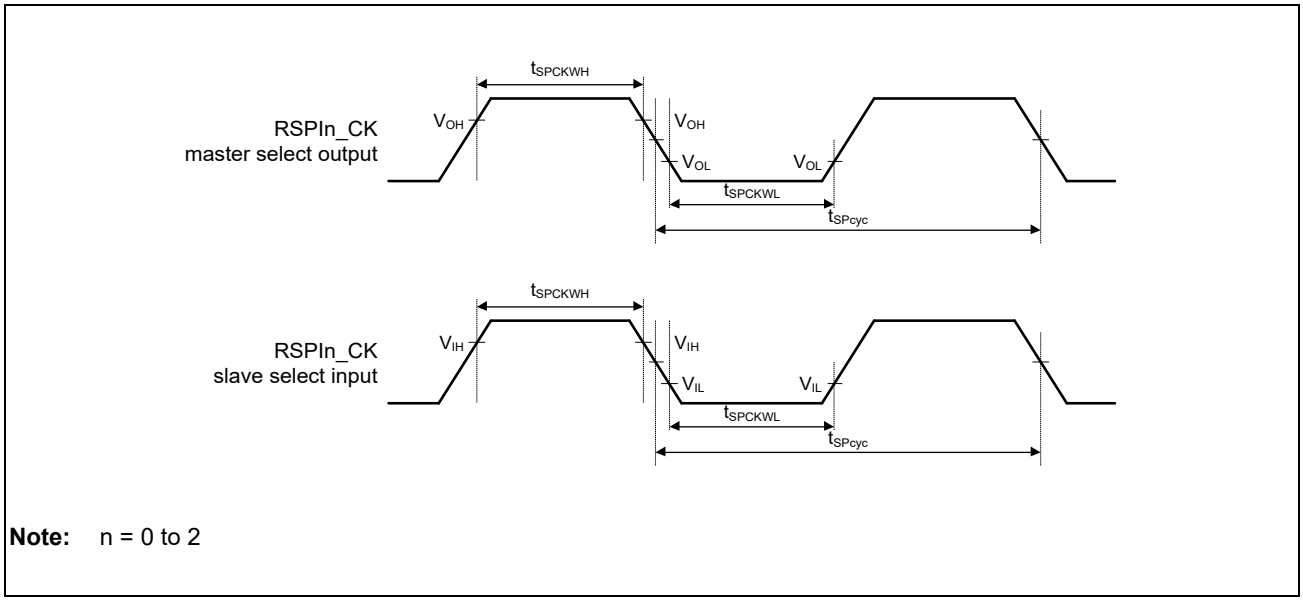
### 3.5.16 Renesas Serial Peripheral Interface (RSPI) Access Timing

Table 3.43 Renesas Serial Peripheral Interface Timing

| Item | | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|---|
| RSPCK clock cycle | Master | $t_{SPcyc}$ | 2 | 4096 | $t_{p1cyc}$*1 | **Figure 3.44** |
| | Slave | | 8 | 4096 | | |
| RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | 0.4 | — | $t_{SPcyc}$*1 | |
| | Slave | | 0.4 | — | | |
| RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | 0.4 | — | $t_{SPcyc}$*1 | |
| | Slave | | 0.4 | — | | |
| Data input setup time | Master | $t_{SU}$ | 10 | — | ns | **Figure 3.45** to **Figure 3.48** |
| | Slave | | 0 | — | $t_{p1cyc}$*1 | |
| Data input hold time | Master | $t_H$ | 0 | — | ns | |
| | Slave | | 4 | — | $t_{p1cyc}$*1 | |
| SSL setup time | Master | $t_{LEAD}$ | 1 × $t_{SPcyc}$ − 20 | 8 × $t_{SPcyc}$ | ns | |
| | Slave | | 4 | — | $t_{p1cyc}$*1 | |
| SSL hold time | Master | $t_{LAG}$ | 1 × $t_{SPcyc}$ | 8 × $t_{SPcyc}$ + 20 | ns | |
| | Slave | | 4 | — | $t_{p1cyc}$*1 | |
| Data output delay time | Master | $t_{OD}$ | — | 19 | ns | |
| | Slave | | — | 4 | $t_{p1cyc}$*1 | |
| Data output hold time | Master | $t_{OH}$ | 5 | — | ns | |
| | Slave | | 2 | — | $t_{p1cyc}$*1 | |
| Continuous transmission delay time | Master | $t_{TD}$ | 1 × $t_{SPcyc}$ + 2 × $t_{cyc}$ | 8 × $t_{SPcyc}$ + 2 × $t_{cyc}$ | ns | |
| | Slave | | 4 × $t_{cyc}$ | — | | |
| Slave access time | | $t_{SA}$ | — | 4 | $t_{p1cyc}$*1 | **Figure 3.47**, **Figure 3.48** |
| Slave out release time | | $t_{REL}$ | — | 3 | $t_{p1cyc}$*1 | |

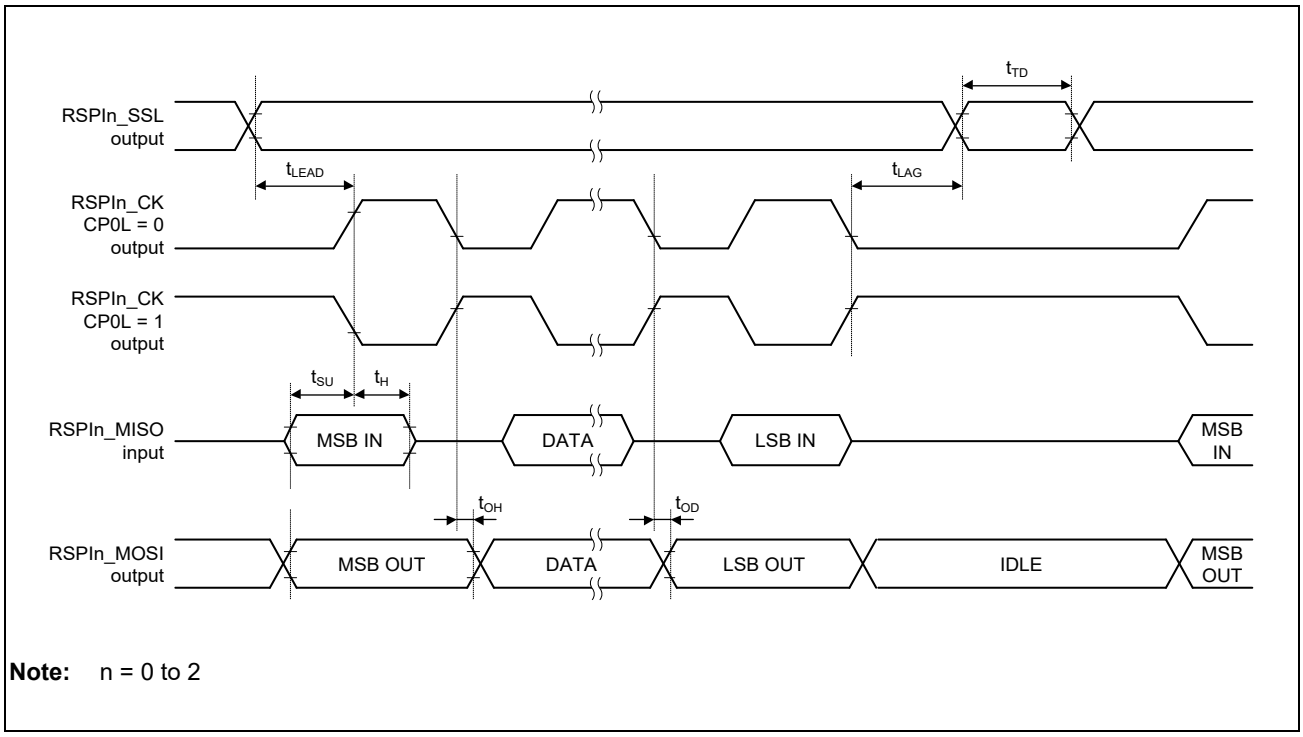
**Note:** AC access timing condition: drive ability 12mA, output load 30pF, slew rate = fast

Note 1. $t_{p1cyc}$ indicates peripheral clock means RSPIn_CLKB (P0ϕ) (0 to 2).



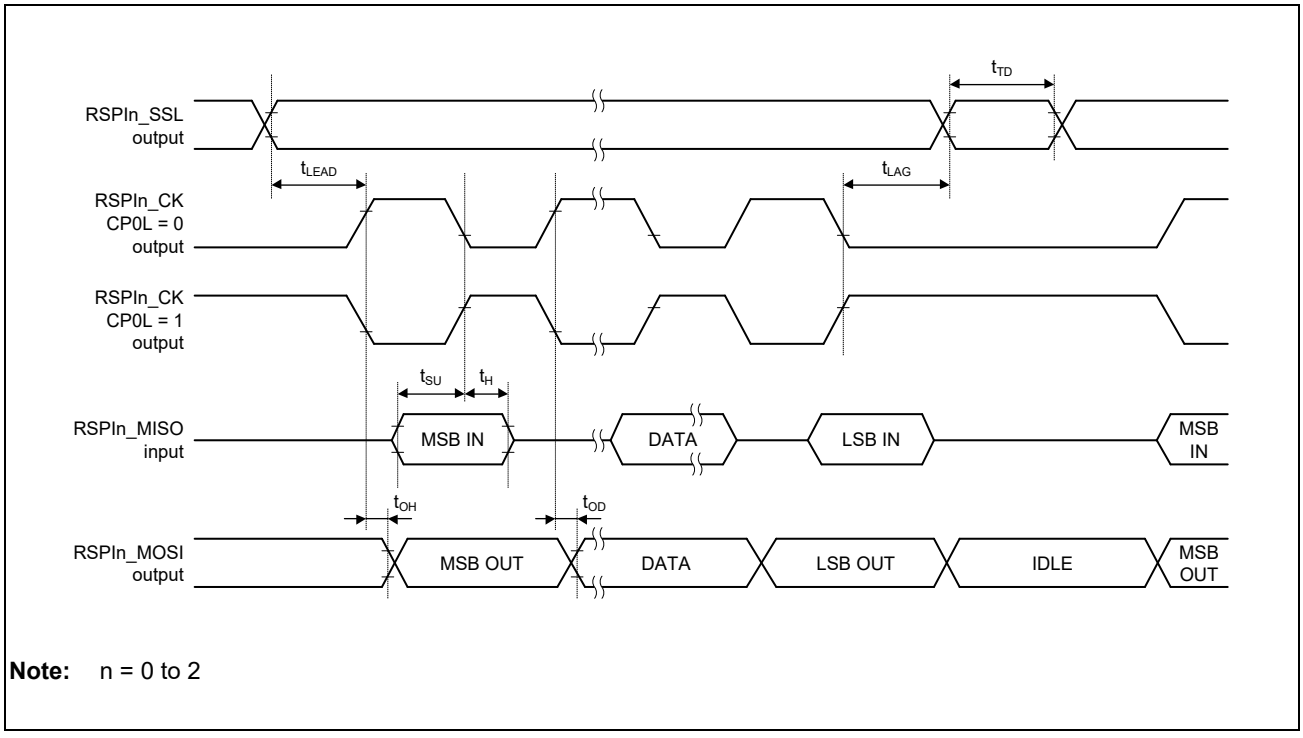

**Note:** n = 0 to 2

Figure 3.44 Clock Timing



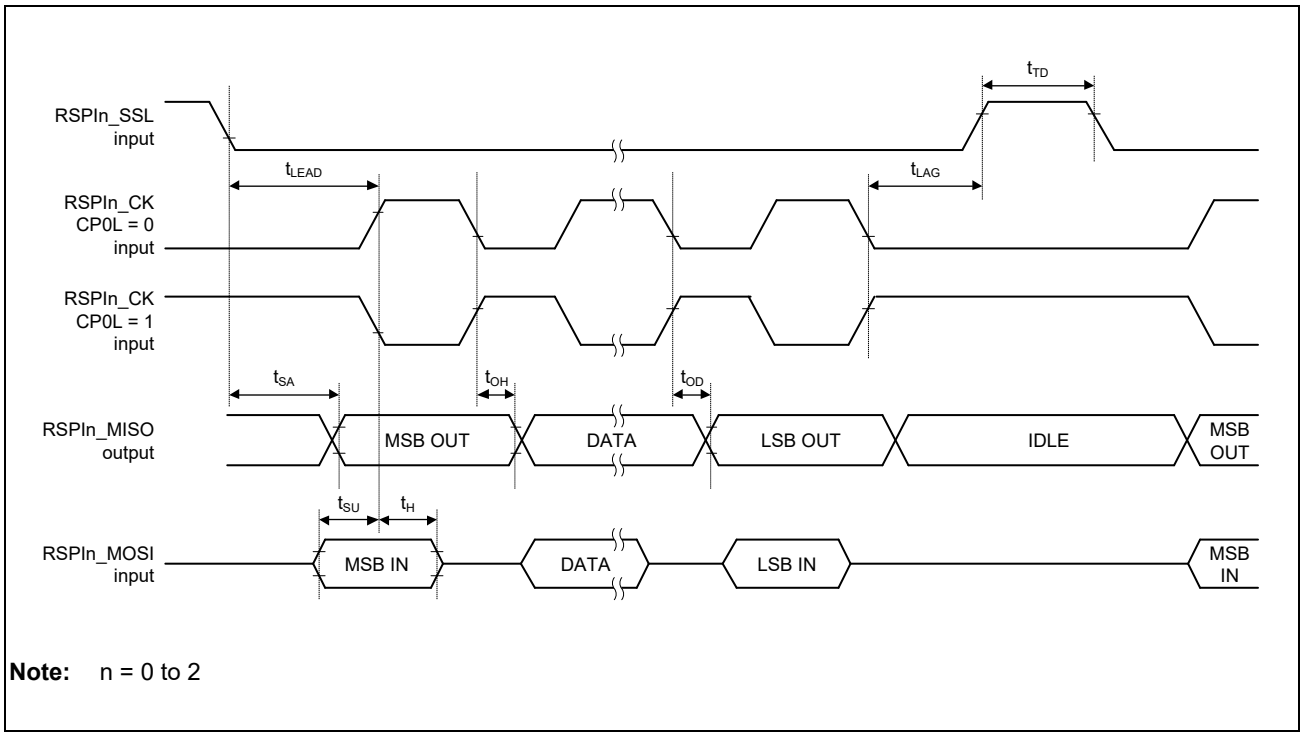

**Note:** n = 0 to 2

Figure 3.45 Transmission and Reception Timing (Master, CPHA = 0)



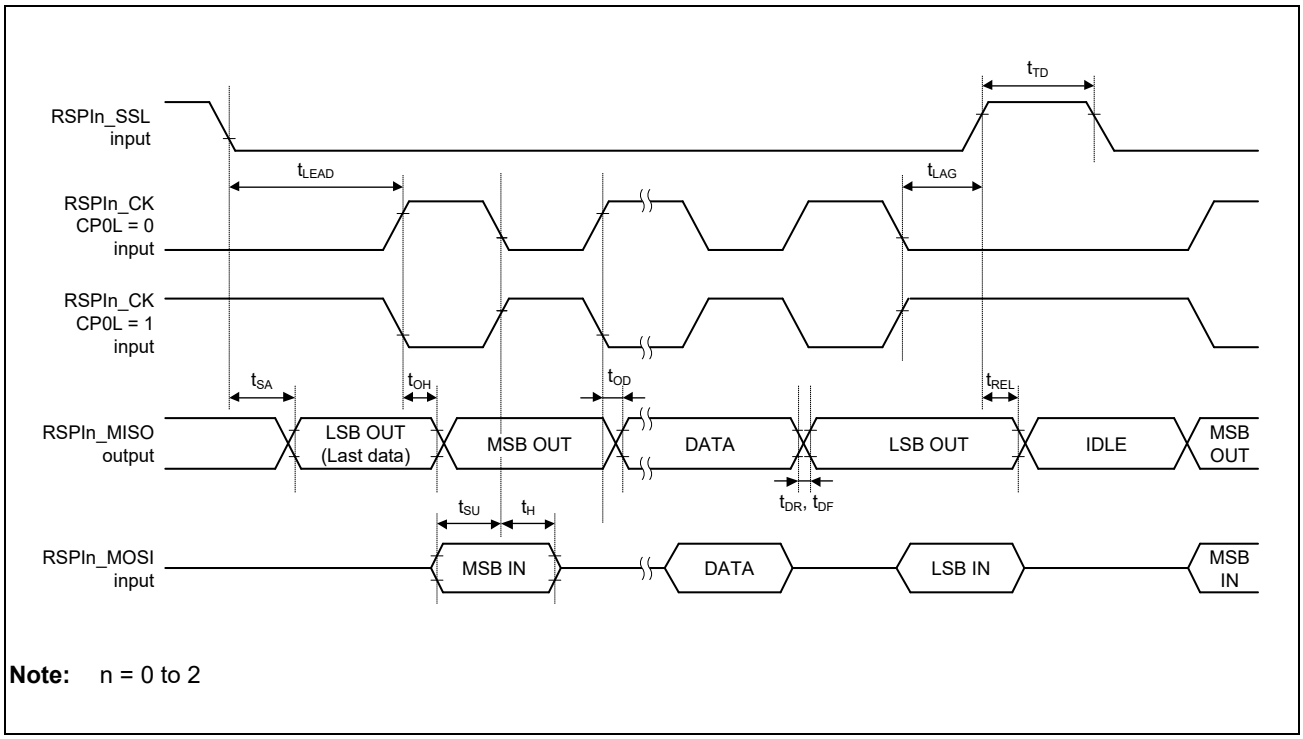

**Note:** n = 0 to 2

Figure 3.46 Transmission and Reception Timing (Master, CPHA = 1)




**Note:** n = 0 to 2

Figure 3.47 Transmission and Reception Timing (Slave, CPHA = 0)




**Note:** n = 0 to 2

Figure 3.48 Transmission and Reception Timing (Slave, CPHA = 1)

## 3.5.17 A/D Converter Access Timing

Table 3.44 A/D Converter Timing

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| ADC Trigger Input Pulse Width | $t_{TRGW}$ | 1.5*2 | | $t_{P1cyc}$*1 | **Figure 3.49** |

Note 1. $t_{p1cyc}$ indicates peripheral clock means ADC_ADCLK (TSUϕ).

Note 2. When a noise filter in ADC is off.

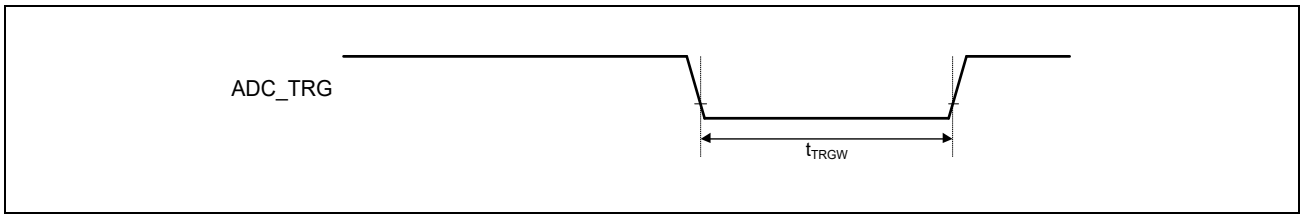



Figure 3.49 ADC Trigger Input Timing

## 3.5.18 Watchdog Timer Access Timing

Table 3.45 Watchdog Timer Timing

| Item | Symbol | Min. | Max. | Unit | Figures |
|---|---|---|---|---|---|
| WDTOVF_PERROUT# Output Time | $t_L$ | 64 | 64 | $t_{P1cyc}$*1 | **Figure 3.50** |

Note 1. $t_{P1cyc}$ indicates peripheral clock means WDTn_CLK (OSCCLK) (n = 0, 2).

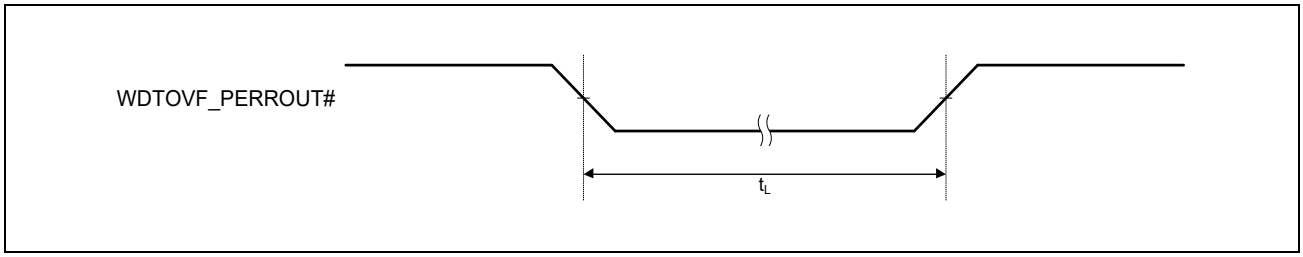
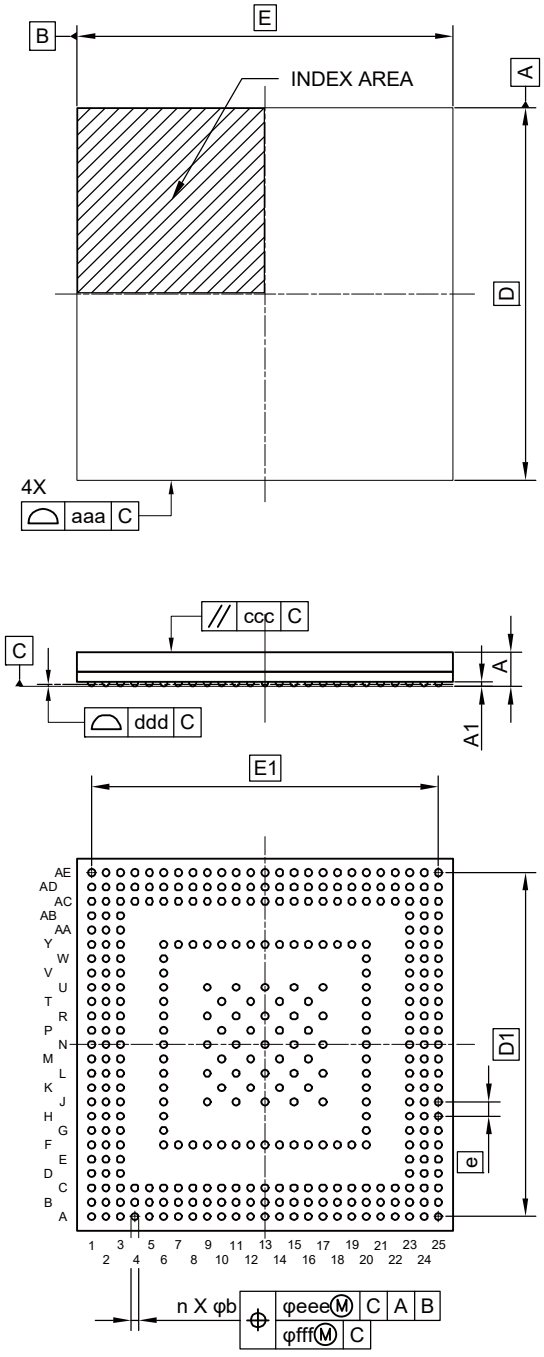



Figure 3.50 Watchdog Timer Output Timing

# 4. Package Dimensions

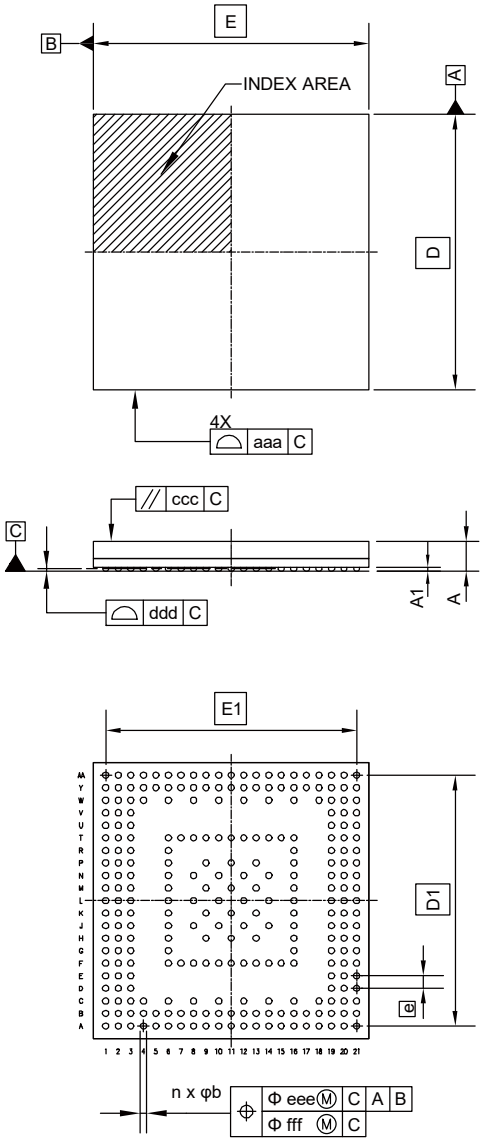
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-LFBGA361-13x13-0.50 | PLBG0361KB-A | 0.40 |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| D | — | 13.00 | — |
| E | — | 13.00 | — |
| D1 | — | 12.00 | — |
| E1 | — | 12.00 | — |
| A | — | — | 1.40 |
| A1 | 0.11 | — | — |
| b | 0.20 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| aaa | — | — | 0.15 |
| ccc | — | — | 0.20 |
| ddd | — | — | 0.08 |
| eee | — | — | 0.15 |
| fff | — | — | 0.08 |
| n | — | 361 | — |

Figure 4.1 Package Dimensions for LFBGA 13 mm□/0.5 mm pitch/361 pin

| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-LFBGA266-11x11-0.50 | PLBG0266KA-A | 0.29 |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| D | — | 11.00 | — |
| E | — | 11.00 | — |
| D1 | — | 10.00 | — |
| E1 | — | 10.00 | — |
| A | — | — | 1.40 |
| A1 | 0.11 | — | — |
| b | 0.20 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| aaa | — | — | 0.15 |
| ccc | — | — | 0.20 |
| ddd | — | — | 0.08 |
| eee | — | — | 0.15 |
| fff | — | — | 0.08 |
| n | — | 266 | — |

Figure 4.2 Package Dimensions for LFBGA 11 mm□/0.5 mm pitch/266 pin

| REVISION HISTORY | RZ/Five Group DATASHEET |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Dec 25, 2024 | — | First edition issued |
| 1.10 | Jun 30, 2025 | 1. Overview | |
| | | 11 | Figure 1.1 Configuration of LSI Internal Bus<br>Text, modified (MPU Bus → MCPU Bus)<br>SRC, deleted |
| | | 3. Electrical Characteristics | |
| | | 18 | Table 3.3 DC Characteristics (1) [3.3-V I/O]<br>Input leakage current, added |
| | | 19 | Table 3.7 DC Characteristics (5) [RGMII/MII]<br>Input logic low (Remarks: 1.8-V RGMII/MII): The Min value, modified |
| | | 20 | Table 3.9 DC Characteristics (7) [1.8 V I/O (SD, QSPI)]<br>Output logic high voltage: The Min value, modified<br>Output logic low voltage: The Max value, modified |
| | | 22 | Table 3.18 DC Characteristics (16) [ADC]<br>Full-scale error, Offset error, Analog input capacitance, Analog input resistance, External capacitance, and External resistance, added<br>Note 1, added |
| | | 23 | Figure 3.4 Analog Input Equivalent Circuit, added |
| | | 27 | Table 3.21 SDHC AC Access Timing (SDR at 3.3-V Operation)<br>SD_CLK clock high level width, SD_CLK clock low level width, SD_CMD,SD_DATA output delay: The Min values, modified |
| | | 28 | Table 3.22 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)<br>SD0_CLK clock cycle, SD0_CLK clock high level width, SD0_CLK clock low level width, SD0_CMD/SDDAT output delay: The Min values, modified |
| | | 28 | Table 3.23 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)<br>SD0_CLK clock cycle, SD0_CLK clock high level width, SD0_CLK clock low level width: The Min values, modified<br>SD0_CMD/SDDAT output delay: The Min and Max values, modified |
| | | 29 | 3.5.3.2 eMMC host interface timing (HS-SDR), modified |
| | | 30 | Table 3.26 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)<br>SD0_CLK clock high level width, SD0_CLK clock low level width: The Min values, modified<br>SD0_CMD/SDDAT output delay: The Min and Max values, modified |
| | | 36 | Table 3.32 Ethernet-IF Access Timing (Ether RGMII)<br>Duty cycle for gigabit: The Min and Max values, modified<br>Note, modified |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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